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Author
Li, Weicong

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ABSTRACT OF THE DISSERTATION

SiGe-Pocket Tunnel FETs for Low Power Logic Applications

by

Weicong Li

Doctor of Philosophy in Electrical Engineering

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Professor Jason C. S. Woo, Chair

Over the last 50 years, conventional scaling (Moore's law) has provided continuous improvement in semiconductor device/circuit technology and has resulted in unprecedented advancement in electronic systems. However, as transistors scale below 45nm, the non-scalability of subthreshold swing (*SS*) in conventional MOSFETs has resulted in increased power consumption. Power/thermal issue has become one of the major roadblocks for the scaling of the devices. Therefore, novel devices with steep *SS* are highly desirable as they offer the same current drive with a reduced supply voltage (V_{DD}) while maintaining a reasonable I_{OFF}. Among all potential device solutions, including negative capacitance FETs (NC-FETs) and NEMS. Tunnel

FETs (TFET) have been widely regarded as the most promising candidates, especially for the power-sensitive Internet of things (IoTs) applications.

State-of-the-art TFETs, both group IV and group III-V-based, have been examined to identify the limitations of the previously proposed devices. SiGe-based device solution is identified as the most promising solution because of its FinFET/GAA compatibility, mature synthesis techniques, and tunable bandgap. Compared with III-V-based TFETs, it is more likely to be adopted by future VLSI technologies. TFET with a counter-doped SiGe-pocket is proposed to take the full advantage of the SiGe material system. By adopting the counter-doped SiGe pocket, both tunneling barrier height and width are reduced, which results in significant improvement in I_{ON} as well as *SS*. Vertical p-type TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket has been experimentally demonstrated. The vertical doping/composition profile was achieved by in-situ doped RPCVD. Improvement in transfer characteristics has been observed when compared with Si TFET and TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket. It provides a potential device solution for low power logic applications.

The dissertation of Weicong Li is approved.

Brian Chris Regan

Oscar Stafsudd, Jr.

Robert Candler

Jason C. S. Woo, Committee Chair

University of California, Los Angeles

2019

To my wife, my family, Zoey, and Wubai.

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VITA

2012	Bachelor of Science, Electrical Engineering University of California, Los Angeles
2014	Master of Science, Electrical Engineering University of California, Los Angeles
2018	Ph. D. Candidate, Electrical Engineering University of California, Los Angeles

Publications

Weicong Li and Jason C. S. Woo, "Vertical P-TFET with a P-type SiGe Pocket," *in IEEE Transactions on Electron Devices* (2019, under review).

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Chapter 1

Introduction

1.1 Overview

Aggressive scaling of transistors has been the driving force for the integrated circuit (IC) industry in the past decades. It has enabled powerful computers, portable electronics, high-speed wireless communication, and recently IoTs. However, with the benefits of scaling, come the challenges such as short channel effects, parasitic components, and power/thermal issues. The industry has invested heavily to mitigate these issues and to maintain the scaling trend.

The industry has seen a transition in architecture from planar FET to FinFET at 22nm node [1]. The 3D device structure provides a better electrostatic control, which helps to mitigate the short channel effects such as drain-induced barrier lowering (DIBL) and *SS* degradation. It has a higher current drive per footprint compared with planar devices, thus provides high-speed logic circuits. FinFET technology has enabled further scaling down to 7nm node [2]-[5]. For 5nm node and beyond, the new technologies such as gate-all-around (GAA) MOSFET [6]-[7] and 2D materials [8]-[9] have been proposed. Compared with FinFET, GAA MOSFET has an additional gate which enhances the electrostatic control and enables further scaling [10]. 2D material such as black phosphorus is an atomically thin layer of material with a high mobility [11]. It is immune to short channel effect due to its 2D nature. In addition, its excellent carrier transport properties make it a potential candidate for future technology node.

The development of contact technology is also critical for device scaling. As the transistor footprint becomes smaller, so does the contact area. International Technology Roadmap for Semiconductors suggests a reduction in parasitic source/drain resistance (Ω-μm) for future

technology [12]. Consequently, it is essential to reduce the specific contact resistance (ρ_c). Record-breaking value of $\rho_c \leq 1x10^{-9}cm^2$ has been achieved with shallow ion implantation, and nanosecond laser anneal (NLA) [13], which reduces the parasitic elements and paves the way for advanced nodes.

However, a breakthrough is needed to alleviate the power dissipation problem. Reducing operating power without sacrificing device performance has risen as a major concern for scaling beyond 10nm because of the inability to reduce V_{DD} [12]. Reducing V_{DD} while maintaining a reasonable I_{ON} is critical for low power logic applications. This requires devices to have steep switching characteristics, preferably sub-60mV/dec *SS* at room temperature. Consequently, novel transport/charge modulation mechanisms have been exploited to enable further scaling of the physical dimensions and V_{DD} of transistors.

1.2 Motivation and Objectives

The switching behavior of conventional MOSFET is governed by Boltzmann's statistics. Based on the long channel theory of conventional MOSFET, *SS* is given by:

$$SS = ln(10)\frac{kT}{q}\left(1 + \frac{C_D}{C_{ox}}\right) = 60\left(1 + \frac{C_D}{C_{ox}}\right) mV/dec \quad (1)$$

where k is Boltzmann constant, T is temperature, q is the elementary charge, C_D is the bulk depletion capacitance, and C_{ox} is the gate capacitance. With both capacitances being positive, *SS* is limited to 60mV/dec at room temperature [14]. In order to achieve sub-60mV/dec switching behaviors, alternative devices have been proposed, including negative capacitance FETs (NC-FETs) [15]-[16], nano-electromechanical switches (NEMS) [17]-[18], and TFETs.

Ferroelectric materials such as hafnium-based oxides have demonstrated negative capacitance [16]. NC-FET utilizes theses ferroelectric insulators as the gate oxide to enhance the

coupling between the gate and the channel potential, therefore results in sharp turn-on behavior [19]. Hysteresis-free NC has been demonstrated up to 10MHz with $Hf_{0.5}Zr_{0.5}O_2$ [20]. However, hysteresis-free NC operating needs to extend to the GHz range for it to be a competitive device option for logic applications. Further investigation is needed to examine the viability of NC-FET at the GHz range. NEMS conducts the current by physically moving the gate closer to the channel via magnetic, thermal, piezoelectric, or electrostatic mechanisms. This allows it to circumvent the SS limit set by Boltzmann's statistics. But the hysteresis in transfer characteristics, relatively low frequency, and short endurance make NEMS less suitable for logic devices [21]. Among all the potential devices, TFET has risen as the most prominent candidate for steep *SS* devices [22]-[24]. Unlike conventional MOSFETs, TFETs conduct current via quantum tunneling (Fig. 1.1). The gate modulates the tunneling probability of electrons injecting from the source into the channel as well as the number of available tunneling states in the channel. Both factors contribute to the sharp turn-on of TFETs.

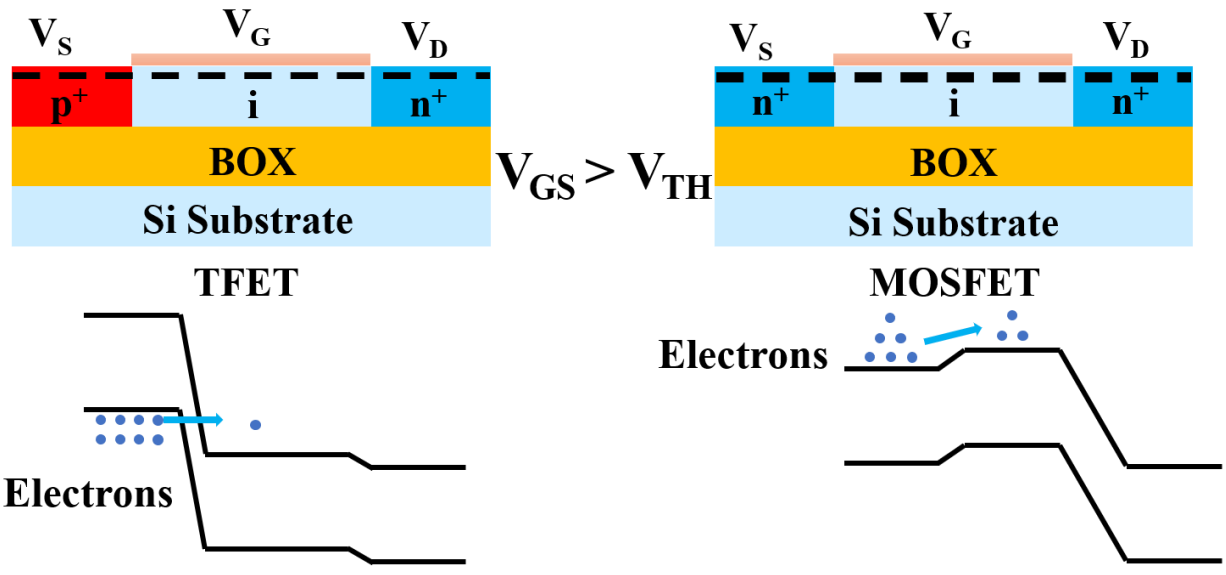


Fig. 1.1 Compared with MOSFET, the current conduction in TFET is dominated by the band-to-band tunneling. Therefore, its *SS* is not limited by Boltzmann statistics (60mV/dec at room temperature).

In the past decade, TFET has been under extensive examination because of its steep *SS*. Though sub-60mV/dec *SS* has been demonstrated, the steep switching behavior only occurs at the small current regime (pA/μm to nA/μm) and is limited to fewer than two decades of I_{DS} [22]-[26]. Additional, *SS* degrades drastically as I_{DS} increases [22][25]-[26]. Several factors contribute to the degradation, including the screening of the gate electric field by mobile carriers as well as the reduced increasing rate of tunneling probability. These drawbacks render TFETs less compelling for high-performance logic applications. However, under reduced V_{DD}, TFETs still exhibits high I_{ON} than conventional MOSFETs do [27]. Device concepts such as bandgap engineering, multi-gate structures, doping profile engineering have been exploited to improve the performance of TFETs for low power logic circuit.

The objective of this work is to determine a TFET structure for low power logic operating (I_{OFF}=10pA/μm) under V_{DD} of 0.5V. The new structure bypasses the drawbacks of previous TFETs and could potentially operate at a reduced V_{DD} while maintaining a reasonable I_{ON}. It is noted that minimum point *SS* is not the goal, because V_{DD} can only be reduced by extending sub-60mV/dec *SS* over a wide range of drain current. Ge-pocket TFET is presented as one of the promising candidates. The device optimization and scalability study have been carried out with a TCAD simulator in great depth. P-type SiGe-pocket TFET has also been examined. The devices have been fabricated, characterized, and analyze to demonstrate the potential for future low power logic applications.

1.3 Organization

This dissertation is organized into the following chapters.

In Chapter 2, the basic operating mechanism of tunneling field-effect transistor has been discussed. State-of-the-art TFETs have been thoroughly examined to identify their drawbacks and limitations. TCAD tool has been calibrated to these experimental data to further assist the device design in the following chapter.

In Chapter 3, based on the previous drawbacks, n-type Ge-pocket TFET is proposed. A detailed simulation has been carried out to optimize Ge-pocket TFET for 14nm node low power technology. And the scalability of the device in terms of both gate length and supply voltage has also been investigated. The scaling rule is presented to guide device design for 10nm node and beyond. The device concept is also applicable to p-type TFET. This chapter is a modified version of "Weicong Li and Jason C. S. Woo, "Optimization and Scaling of Ge-Pocket TFET," in *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5289-5294, Dec. 2018. DOI: 10.1109/TED.2018.2874047."

In Chapter 4, the detailed process flow of p-type TFET with counter-doped $Si_{0.8}Ge_{0.2}$-pocket is presented, and key process steps are explained in detail. Vertical FET structure is chosen to achieve the desired Si/SiGe heterostructure. The experimental results of the fabricated Ge-pocket TFET are presented and discussed extensively. The enhancement in performance due to the incorporation of a counter-doped $Si_{0.8}Ge_{0.2}$-pocket pocket has been demonstrated by comparing TFETs with and without the pocket. The impact of the material quality on the device performance have been analyzed. This chapter is a modified version of "Weicong Li and Jason C. S. Woo, "Vertical P-TFET with P-type SiGe Pocket," *in IEEE Transactions on Electron Devices* (2019, under review). "

Finally, Chapter 5 summarizes the major contributions of this work and suggest future research directions.

Chapter 2

Limitations of Previous TFETs

2.1 Introduction

Tunneling is a unique quantum phenomenon with no counterpart in classical physics. It is the consequence of the wave nature of microscopic particles, which allows the particle to go "through" rather than over a potential barrier. Modeling such process has been attempted with various complexities: from closed-form analytical approaches to non-equilibrium Green function (NEGF) method. A physics-based yet computationally efficient model is critical for understanding TFETs operation. By calibrating the model to experimental data, it will serve as a reliable platform for identifying TFETs limitations and optimizing future devices

As described in the previous chapter, TFETs have been studied. The device concept has been demonstrated with various material systems, including group IV-based, III-V-based, and recently introduced 2D-material-based [28],[29]. Both Sub-60mV/dec switching, and high I_{ON} (~310μA/μm) [30] are observed but on separate platforms. The feasibility of incorporating both features onto the same platform is yet to be demonstrated. Additional concerns like ambipolar conduction also need to be addressed. State-of-the-art TFETs have been thoroughly investigated to determine their strong suits as well as weaknesses, which is instructional for the implementation of TFETs for low power logic devices.

2.2 Modeling Band-to-Band Tunneling

2.2.1 Band-to-Band Tunneling

Band-to-band tunneling describes the quantum phenomenon of electrons in the valence band tunneling into the conduction band through the bandgap under proper band alignment. During the tunneling process, both the energy and the momentum of the electrons must be conserved. The tunneling probability is determined by detailed the band structure and the tunneling path. Semiconductor materials with small direct bandgap are preferable to facilitate high tunneling probability. High tunneling current density of 2.2MA/cm^2 has been demonstrated with III-V Esaki diodes [31]. It is almost two orders of magnitude higher than their Si counterpart [32]. For a fixed bandgap, high electric field reduces tunneling distance and significantly increases the tunneling probability.

2.2.2 Local Tunneling Model

For indirect bandgap semiconductor materials like Si and Ge, the carrier-phonon interaction is needed during the band-to-band tunneling process to conserve the crystal momentum, because of the misalignment of the conduction band minimum and valence band maximum. Modeling the tunneling in these materials has been proven to be more challenging because the carrier-phonon interaction must be included in the Hamiltonian. Rigorous quantum mechanics treatments lead to lengthy results. Different degrees of approximation have been made to enable the incorporation of the tunneling models into simulation tools [33]-[35].

Sentaurus TCAD is adopted in this study. The tunneling model provided by the simulator is broadly characterized into two categories: the local and the nonlocal tunneling model [36]. The

local tunneling model calculates the tunneling rate based on the local electric field. It is a computationally efficient method to study tunneling. However, there are a few drawbacks associated with the approach. First, there is a nonzero tunneling current under zero electric field. Moreover, tunneling can occur without the overlap of the conduction band and valence band. Finally, the model fails to capture the nonlocality of the tunneling process and neglects the impact of the tunneling path. The failure to accurately capture the tunneling physics compromises the accuracy of the simulation and renders the local tunneling model ineffective for TFETs design and optimization.

2.2.3 Nonlocal Tunneling Model

Tunneling is a nonlocal process by nature: it depends on both the densities of states and the carrier distributions at the starting as well as the ending point of tunneling; moreover, it is strongly influenced by the tunneling path that the tunneling carrier takes. Therefore, a nonlocal model is needed.

The dynamic nonlocal tunneling model is provided by the TCAD tool. The model is derived from the Landauer formalism, which is equivalent to NEGF for coherent transport (without electron-electron and electron-phonon scatterings) [37]. The electron-phonon interaction in the indirect tunneling is taken into account by incorporating the phonon emission/absorption into the calculation of the tunneling probability. The number of tunneling channels is calculated by integrating the available density of states perpendicular to the tunneling direction [18]. The simulator considers all mesh points as possible starting points, and the tunneling direction is determined dynamically by following the gradient of the valence band at the starting point. The

tunneling probability is calculated based on the Wentzel–Kramers–Brillouin approximation. During the tunneling process, the carrier energy is conserved. Under the limit of a uniform electric field, the model is reduced to the Kane model:

$$R_{net} = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right)$$

where F_0=1V/cm, P=2.5 for the phonon-assisted tunneling, A and B are material-dependent fitting parameters. Compared with the local tunneling model described in the previous section, the dynamic nonlocal tunneling model is more sophisticated, yet still computationally efficient. It captures the impact of the density of states at the starting point and the ending point, as well as the tunneling path on the process. Two fitting parameters allow a better fit between the simulation and the experimental data. The model emphasizes the importance of the potential profile on tunneling. In short, the model is a reliable platform for TFETs simulation and optimization.

2.2.4 NEGF Model

NEGF is a quantum-mechanics-based treatment to the tunneling process. It has the strongest conceptual basis among all the models discussed. Quantum phenomena such as quantization and tunneling are inherent to the model. It solves coupled Poisson equation and Schrodinger equation self-consistently to obtain the charge distribution and the current [38]. The impact of source, drain, and scatterings can be included by adding their self-energies to the Hamiltonian [39]. However, the associated computational expense rises quickly if the scattering between transverse modes is considered [40]. The matrix size of the Hamiltonian associated with an n-dimensional device with m mesh point in each direction is given by m^{2n} [40]. Device

simulations with a dense mesh are computationally expensive, if not prohibitive. Therefore, the model is not suitable for an optimization study where quick turnaround time is critical.

As the sophistication of the tunneling model increases, so does the computational expense. To design and to optimize TFETs, a conceptually sound model with a quick turnaround time is desired, because the feedback from previous simulations is beneficial for understanding and further improving the design. With all things considered, the dynamic nonlocal tunneling model is chosen as the most suitable option for this study.

2.3 Simulation Calibration

2.3.1 Calibration to Si/Ge Heterojunction

As described in the previous section, and there are two material-dependent fitting parameters in the nonlocal band-to-band tunneling model that can be adjusted. Both parameters need to be calibrated accurately to predict the overall performance of future devices correctly.

The tunneling model is first fitted to a vertical TFET with a Ge source [41]. The doping profile of the device is fitted to scanning spreading resistance measurement data. The simulated transfer characteristic is calibrated to the experimental data measured at 78K. The low-temperature measurement result is better for the calibration because the band-to-band tunneling dominates the conduction, and alternative current conduction mechanisms such as trap-assist tunneling, and Shockley-Read-Hall recombination are suppressed at low temperature. A good agreement between the experimental data and simulation has been obtained (Fig. 2.1).

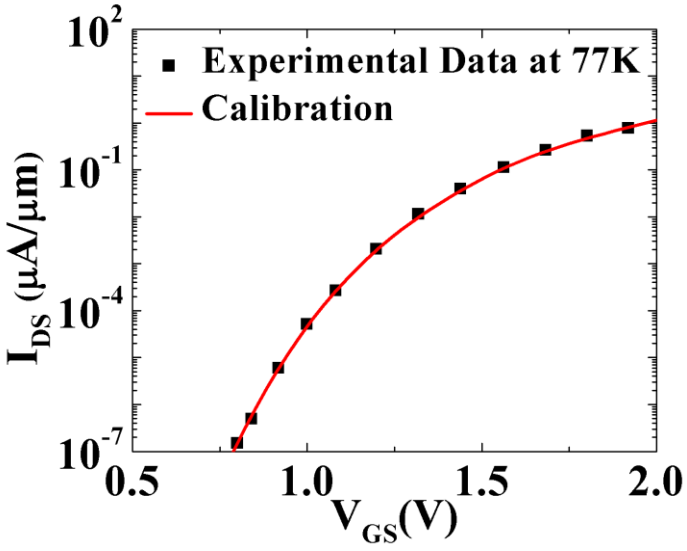


Fig. 2.1 The dynamic nonlocal tunneling model has been calibrated to experimental data of Ge-source TFET from [43]. Good agreement between the experiment and the simulation is achieved with A=1.47×10^{17}cm^{-3}s^{-1} and B=3.49×10^{6}Vcm^{-1} for bulk Ge with strain. Default tunneling parameters are adopted for Si [36].

2.3.2 Generalization to Si_xGe_{1-x} Heterojunction

To study the impact of SiGe composition on tunneling, it is essential to generalize the model to fit the experimental data from the tunneling junctions with arbitrary Ge content. Depending on the Ge composition, the fitting parameters are calculated by linearly interpolating between the values of Si and Ge. And the simulation result agrees with Si/SiGe resonant interband tunneling diode fabricated by low-temperature molecular beam epitaxy (LT-MBE) [42]. Minimum doping diffusion is achieved by suppressing the growth temperature. Thus, a box-shape doping profile is used in the simulation. The simulation result between 0 and 0.3V is presented (Fig. 2.2), because the band-to-band tunneling is the dominant current conduction mechanism in this range. The model agrees with the experiment result, and it is capable of reliably projecting the performance of SiGe-based tunneling devices.

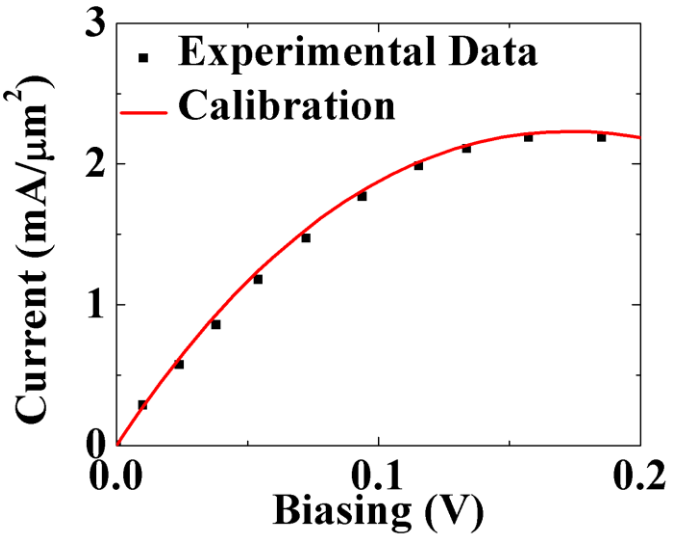


Fig. 2.2 The dynamic nonlocal tunneling model has been calibrated to experimental data of Si/SiGe RITD from [44]. A good agreement between experiment and simulation is achieved.

2.4 Revisit State-of-the-Art TFETs

2.4.1 Si TFET

Si has been the most studied material for TFETs. Due the high materials quality, sub-60mV/dec *SS* [22],[23],[43] and ~pA/μm low leakage current [22],[44],[45] have been demonstrated by various experiments. In addition, a good electrostatic control is critical for Si-based TFETs performance. The *SS* of Si nanowire TFETs is reduced from ~120mV/dec to ~45mV/dec when the diameter decreases from 50nm to 20nm [43]. By adopting the nanowire structure, I_{ON} of 53μA/μm [45] and 75μA/μm [46] have been achieved. Approximately one order of magnitude increase in I_{ON} is observed compared with their SOI counterpart [22],[23]. The impact of the multi-gate structure on the TFETs performance is twofold. The multi-gate structure increases the tunneling area by introducing more conducting surfaces. For logic circuits, the additional gate capacitance has little impact on the performance, because the loading capacitance

is dominated by the interconnect. In addition, the improved electrostatic control enhances the tunneling probability and increases the tunneling area by extending the tunneling further into the body. The success of Si-based TFETs heavily relies on mature material synthesis and processing techniques.

The major drawback of Si-based TFETs lies in its relatively large bandgap of 1.12eV. Since the tunneling probability decreases exponentially with bandgap, the current conduction capability is severely limited. The I_{ON} of Si-based TFET is at least one order of magnitude smaller than it of MOSFET, which leads to compromised performance. In addition, sub-60mV/dec *SS* is limited to ~pA/μm [22] current regimes. Therefore, Si alone is unlikely to fulfill the potential of TFETs for low power logic applications.

2.4.2 SiGe TFET

SiGe has entered the mainstream very-large-scale-integration (VLSI) technology in 90 nm node to boost the hole mobility [47]. TFETs with SiGe heterojunction show great potential in achieving both high I_{ON} and steep switching [48],[49]: the material has a smaller bandgap compared with Si; the well-developed material synthesis and the mature processing technologies give it an edge over III-V materials. And so far, some of the most promising TFET results have been obtained with SiGe. The nanowire SiGe TFETs in [48] have shown I_{ON} of 190μA/μm with V_{DD}=-0.9V and I_{OFF}=10nA/μm. The device performance strongly depends on the perimeter of the nanowire. And both I_{ON} and *SS* exhibits significant improvement as the perimeter reduces. This experiment further illustrates the importance of electrostatic control for TFET performance.

SiGe-based homojunction TFET suffers from ambipolar conduction: under a reversed gate bias, the tunneling occurs at the channel/drain junction [50],[51]. This is one of the major shortcomings of TFETs with a reduced bandgap, which can be alleviated by adopting drain underlap at the cost of added underlap resistance and an increase in transistor dimensions. An asymmetric device structure is another solution, where a small bandgap is adopted at the source side while a large bandgap at the drain side [41]. Overall, SiGe-based TFETs have the potential to replace MOSFET technology for low power logic applications with further optimizations.

2.4.3 GeSn TFET

GeSn has attracted a lot of attention because of its tunable bandgap. The material has a small bandgap and undergoes a transition to direct bandgap when Sn composition exceeds 8% [52]. The smaller direct bandgap is advantageous for enhancing tunneling. So far, the majority of GeSn TFETs are bulk devices with GeSn epitaxial grown on Si or Ge substrates. Despite the promising predictions by simulations, no I_{ON} improvement over the SiGe-based TFET has been observed in the experiments [52]-[54]. The gap between the theoretic predictions and the experiments is under investigation.

2.4.4 III-V TFET

III-V semiconductor compound, specifically InGaAs, has been widely sought-after as the material system for TFETs because of its small direct bandgap, high mobility, and the ability to form type III heterojunction with GaAsSb. High I_{ON} has been demonstrated [30],[55],[56]. With the improvement of processing technology, *SS* of 48mV/dec has been achieved with InAs/GaAsSb/GaSb nanowire TFETs [25].

To reduce V_{DD} while maintaining $I_{ON,}$ it is desirable to extend a sub 60mV/dec *SS* to a wide current range. However, the minimum *SS* only occurs at ~nA/μm current range for all the examined III-V TFETs [25],[55]-[58]. When moving away from this current range, *SS* increases, which results in U-shape when plotting *SS* as a function of I_{DS}. The degradation of *SS* in the low I_{DS} regime is likely the result of enhanced generation current, which is due to the smaller bandgaps and the higher defect densities in III-V materials. The presence of defects is verified by the temperature-dependent transfer characteristics: as the temperature rises, the I_{DS} increases due to trap-assisted-tunneling [25]. The inability to extend the steep *SS* to ~pA/μm regime makes III-V TFET less likely for low power applications.

2.4.5 2D Metal Dichalcogenides (TMD)TFET

2D materials, specifically transition TMD like MoS_2 and WSe_2 have been studied as alternatives material systems for TFETs. The advantage of MoS_2 and WSe_2 lies in their ultimate electrostatic control. The electrostatic screening of the gate electric field is weak for the atomic-thin materials. Therefore, the electrostatic potential can be modulated more efficiently. These material systems are particularly suitable for the bilayer TFET concept, where asymmetric gate bias is applied to a double-gate structure, and the tunneling occurs in the direction normal to the gates [59]. The concept has been experimentally demonstrated by stacking 2D TMDs [28][29], and I_{ON} is on the order of 1μA/μm range.

Despite the good electrostatic control, 2D TMDs have some intrinsic issues that limit their potential for TFET applications. First, the density of states is limited to 2D TMDs because of their monolayer nature. The smaller density of states leads to fewer tunneling channels, thus limits the tunneling current. Secondly, compared with previously discussed material systems, 2D TMDs

suffer from the low mobility [8],[60] and the large contact resistance [61], which leads to a large source/drain parasitic resistance. The current of TFETs strongly depends on the gate-to-source voltage. Thus, any voltage drop on the parasitic resistance is detrimental for the device performance. Finally, TMDs are susceptible to various degradation mechanisms [62], and effective passivation methods are needed to improve the stability of 2D-TMD-based TFETs.

2.5 Summary

A comprehensive comparison between tunneling models is presented. Both their physical validity and computational efficiency have been considered. The local tunneling model lacks the ability to capture the nonlocality of the tunneling process, and NEGF is computationally expensive for the optimization purpose. The nonlocal dynamic band-to-band tunneling overcomes both drawbacks and serves as a reliable simulation platform for analyzing TFETs operation and optimizing their performances. This model has been calibrated to various experimental data with different types of devices. It shows validity over a wide range of Ge composition and will serve as the simulation platform for the study.

Previous TFETs experiments have been thoroughly examined, and there are four main limitations, including large tunneling barrier, small tunneling area, trap-assisted tunneling, and ambipolar conduction. An asymmetric device structure with reduced tunneling barrier with multi-gate-compatibility is a potential solution to circumvent all those issues. The device needs to be FinFET/GAA-FET-compatible for two reasons: on the one hand, the multi-gate configurations will provide the good electrostatic control for good device performance; on the other hand, as FinFET/GAA-FET will be the mainstream VLSI platform for 10nm and beyond. And it will be

implemented in SiGe platform because of its mature material synthesis and processing technology. Both help to reduce material-related issues such as defects, thus suppress trap-assisted tunneling. All these factors are important for improving the subthreshold performance of TFETs.

Chapter 3

Optimization and Benchmark of Ge-Pocket TFET for Low Power Logics

3.1 Motivation and Rationale

TFETs have been studied extensively as potential replacements for conventional MOSFETs for future low power logic VLSI applications because of their potential to achieve sub-60mV/dec *SS*. So far, reducing V_{DD} without sacrificing I_{ON} has been the key challenge to TFETs. Because traditional Si TFETs suffer from low I_{ON}, SiGe and III-V TFETs have been suggested as alternatives due to their reduced tunnel barrier heights. Although high I_{ON} has been obtained from III-V TFETs, the *SS* degradation at the low current level (<nA/μm) [25],[55],[57],[63] renders the devices unsuitable for V_{DD} scaling. The high leakage floor (~100pA/μm) [30],[55],[56] makes the devices incompatible with low power VLSI technologies. Both shortcomings are likely due to the enhanced generation/recombination, which is inherent to III-V materials.

SiGe is one of the promising material systems for TFET applications because of its FinFET/GAA compatibility, mature synthesis techniques, and tunable bandgap. The FinFET/GAA compatibility is essential for a material to be adopted in mainstream VLSI platforms. Additionally, the maturity of synthesis techniques helps to reduce defect formation during material growth and suppress defect-assisted tunneling. The tunable bandgap enables the realization of efficient tunneling injection and the suppression of ambipolar conduction. SiGe TFETs have been demonstrated, and their performance improvement relies on the increasing Ge content [41],[48],[50],[64]. However, increasing the Ge content leads to high leakage current in SiGe homojunction TFETs [50],[64] and degraded *SS* in SiGe heterojunction TFETs [41]. During SiGe heteroepitaxy, defects can form in the case of growth beyond critical thickness [65], resulting in

defect-assisted tunneling, which is responsible for the *SS* degradation in SiGe heterojunction TFETs [41]. In this paper, the Ge-Pocket TFET with a counter-doped pocket is presented.

3.2 Device Concept

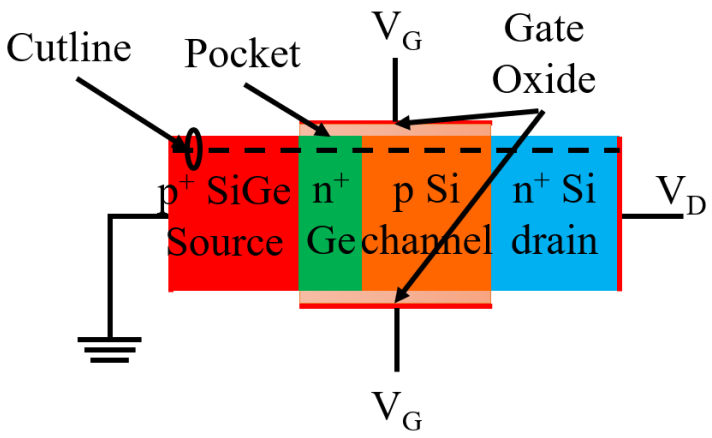


Fig. 3.1 The schematics cross-section of the Ge-Pocket TFET.

A cross-sectional schematic of the n-type Ge-pocket TFET with a counter-doped pocket is shown in Fig. 3.1. The Ge composition in the pocket region is set to be 100% to examine the full potential of the device concept. The key device parameters are listed in Table 3.1. When a positive bias is applied to the gate, the conduction band of the channel is lowered. Once the valence band of the source and the conduction band of the channel overlap, electrons have a finite probability of tunneling through the potential barrier from the source to the channel, which depends on the height and the width of the tunnel barrier [66]. In the proposed structure, the fully-strained Ge (E_g~0.4eV [67]) at the pocket region reduces the tunnel barrier height, whereas the counter-doping reduces the tunnel barrier width by enhancing the lateral electric field across the tunnel junction [22],[68]. As a result, device performance is expected to improve significantly.

Compared with the TFETs with a Ge source [41],[49], Ge in the proposed TFET design is only confined to the pocket region. As the tunneling process occurs across the tunnel barrier around the tunnel junction, extending Ge beyond the pocket region does not improve I_{ON} much, and a thick Ge heteroepitaxy is more challenging to achieve. The pocket thickness is set to 4nm, which is approximately the tunnel barrier width. As the pocket thickness reduces below 4nm, the tunneling process starts to occur outside the pocket region, and the tunneling current decreases significantly due to the large tunneling barrier height outside the pocket region. Due to the large bandgap of Si, the ambipolar conduction at the drain side can be effectively suppressed for low V_{DD} operation.

Table 3.1 The device dimensions and the nominal doping concentrations in each region.

Device Parameters		**WF**	**4.3eV**
L_{gate}	**20nm**	N_{source}	$0.5\text{-}5\times10^{20}cm^{-3}$
T_{ox}	**0.8nm**	N_{pocket}	$2\text{-}6\times10^{19}cm^{-3}$
L_{pocket}	**4nm**	$N_{channel}$	$10^{16}\text{-}10^{18}cm\text{-}3$
T_{body}	**8nm**	N_{drain}	$10^{17}\text{-}10^{20}cm\text{-}3$

3.3 Device Optimization

3.3.1 Simulation Setup

Sentaurus 2012 TCAD is utilized to investigate the performance and optimization of the proposed device. The dynamic nonlocal band-to-band tunneling model has been adopted to capture the transport across the tunneling junction. *SS*~20mV/dec has been demonstrated experimentally in ~pA/μm range [29],[43], which suggests that the impact of band tail on *SS* is negligible for *SS*≥20mV/dec. Therefore, it is ignored in this study. The doping-dependent mobility model, the interface mobility degradation model, and the high-field saturation model are used in the

simulation. The quantum confinement (QC) can be treated rigorously by adopting the Schrodinger-Poisson solver, but the computational burden makes it unsuitable for device optimization. Therefore, the treatment of QC is the following: under the low current regime, the electron density in the channel is small such that the redistribution of electrons due to QC has a negligible impact on the electrostatic potential profile. Therefore, it is ignored in the study. The size-induced bandgap widening has been incorporated into the simulation based on [69]. Note that the tunneling parameters have been adjusted to count for the bandgap change. The field-induced quantization has been ignored due to the small vertical electric field (i.e., small gate voltage for low power), and the difference is partially compensated by the fact that this effect was not included during the previous tunneling model calibration. The physical dimensions of the devices are chosen to enable a fair performance comparison between the proposed device and 14nm FinFETs (Table 3.1). The bandgap of Si, strained Ge, and strained $Si_{0.5}Ge_{0.5}$ are 1.13eV, 0.43eV, and 0.81eV (with size-induced bandgap widening included), respectively, with a constant electron affinity of 4.07eV. The gate work function is set to 4.3eV. All doping profiles are assumed to be abrupt. The doping concentrations are optimized sequentially, which allows a clear interpretation of the simulation results. The values of $N_{source}=10^{20}cm^{-3}$, $N_{pocket}=4\times10^{19}cm^{-3}$, $N_{channel}=10^{16}cm^{-3}$, and $N_{drain}=10^{20}cm^{-3}$ are used as the doping concentrations in the initial simulation study. During SiGe growth, Ge tends to segregate at the surface to minimize the surface free energy. By lowering the growth temperature, the hydrogen passivates the surface and reduces the segregation [70]. To account for the Ge segregation during the growth, a linear composition gradient of 20% per nm is assumed in the simulation (Fig. 3.2). This allows the simulation to yield a more realistic prediction of the device performance. For I_{ON} comparison, I_{OFF} is fixed at 10pA/μm to meet the low operating power

standard for ITRS [12], and V_{DD} is set to 0.5V. This enables a fair comparison of the device performance (i.e., I_{ON}) with fixed power consumption.

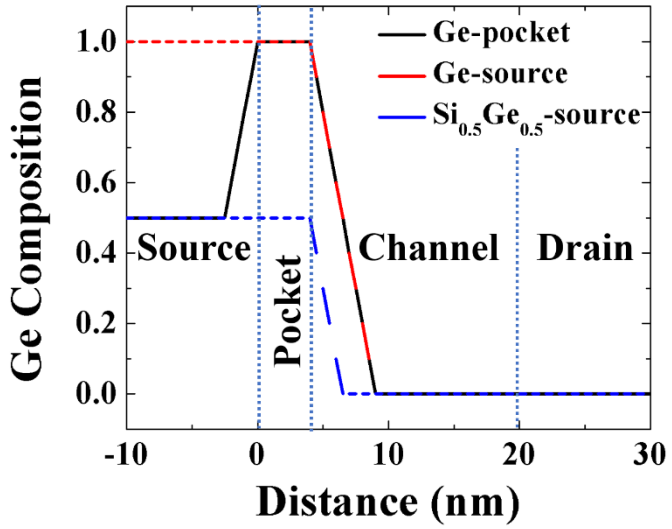


Fig. 3.2 The Ge composition along the cutline (1nm below the gate oxide/channel interface) for the Ge-pocket TFET, the Ge-source TFET, and the $Si_{0.5}Ge_{0.5}$-source TFET.

3.3.2 Ge-Pocket TFET vs SiGe-Source TFET

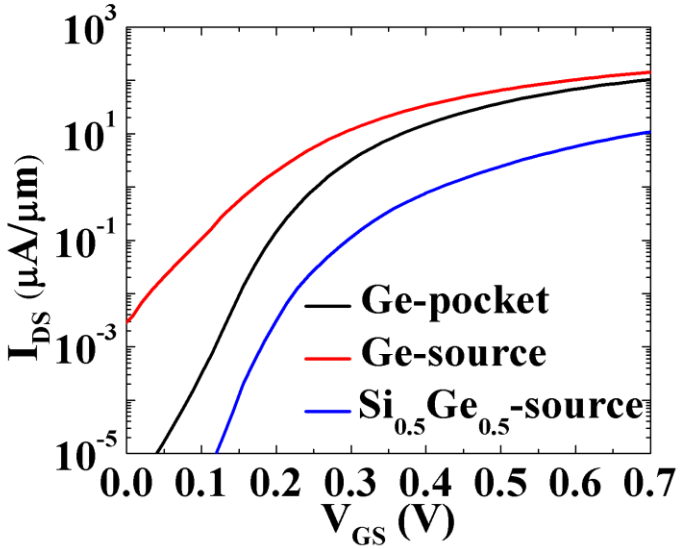
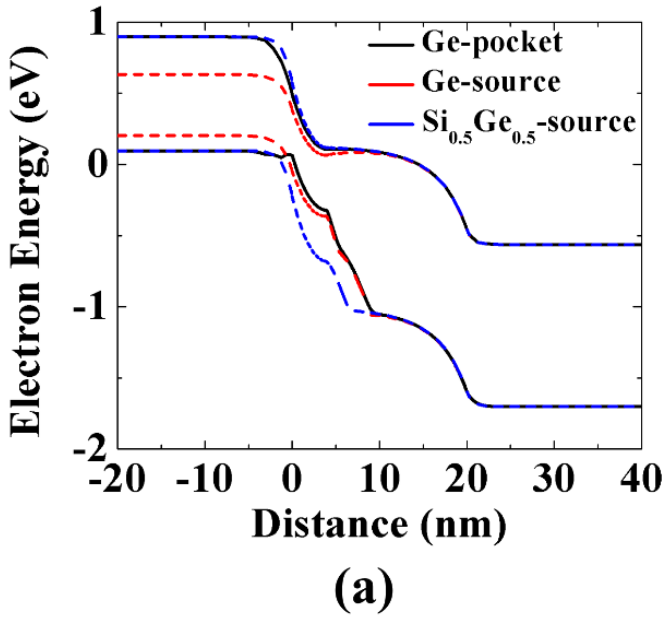


Fig. 3.3 The transfer characteristics of the Ge-pocket, the Ge-source, and the $Si_{0.5}Ge_{0.5}$-source TFETs ($N_{source}=10^{20}cm^{-3}$, $N_{pocket}=4\times10^{19}cm^{-3}$, $N_{channel}=10^{16}cm^{-3}$, and $N_{drain}=10^{20}cm^{-3}$). V_{DS} is set to 0.5V.

Fig. 3.3 shows the transfer characteristics of the Ge-pocket, the Ge-source, and the $Si_{0.5}Ge_{0.5}$-source TFETs. For the latter two devices, Ge and $Si_{0.5}Ge_{0.5}$ have been used for the source and the pocket region, respectively. All three structures have the same doping profile. Ambipolar conduction is absent for all three devices because Si is used for the drain region. The Ge-pocket TFET shows a steep *SS* comparable to the $Si_{0.5}Ge_{0.5}$-source TFET at the low current regime. It also exhibits an I_{DS} comparable to the Ge-source TFET at high V_{GS}. For the Ge-pocket TFET, the large bandgap in the source region blocks the tunneling at a low gate bias, as shown in Fig. 3.4(a). Therefore, the device can be switched off more efficiently, which leads to steep switching. At a high gate bias, the Ge-pocket TFET has a small tunnel barrier that is comparable to the Ge-source TFET, as shown in Fig. 3.4(b), which leads to a high tunneling current. After adjusting the gate voltage to match I_{OFF}, the Ge-pocket TFET (48μA/μm) exhibits a higher I_{ON} than the Ge-source TFET (34μA/μm) and the $Si_{0.5}Ge_{0.5}$-source TFET (7μA/μm). Comparing the Ge-pocket TFET with the $Si_{0.5}Ge_{0.5}$-source TFET, I_{ON} is improved by roughly 6×. This is achieved by reducing the tunneling barrier height from 0.81eV (strained-$Si_{0.5}Ge_{0.5}$) to 0.43eV (strained-Ge) in the pocket region. Note that the discontinuity of the valence band shown in Fig. 3.4 is the result of composition grading, but it does not negatively affect performance. Compared with the devices with an abrupt Ge mole fraction change at the pocket/channel interface, the difference in the current is less than 2%. This is because the channel resistance is dominated by the tunnel resistance at the source/pocket junction.



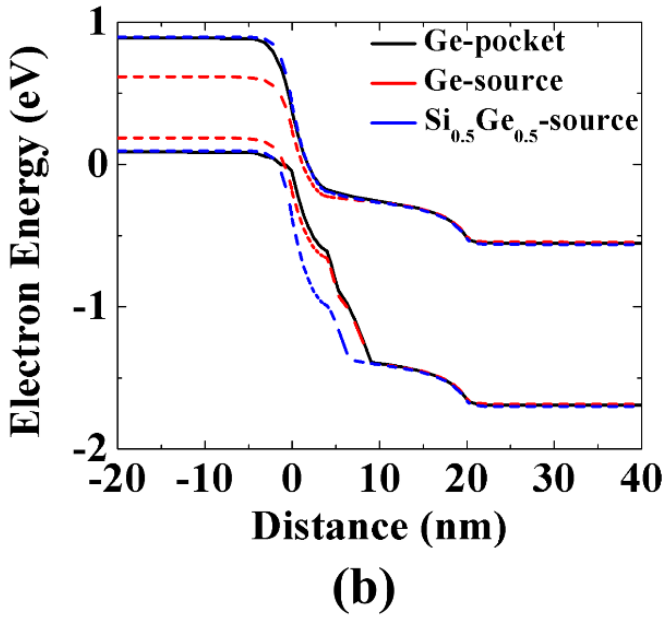


Fig. 3.4 The band diagram of the Ge-pocket, the Ge-source, and the $Si_{0.5}Ge_{0.5}$-source TFETs at (a) low gate bias V_{GS}=0.1V and (b) high gate bias V_{GS}=0.5V. V_{DS} is set to 0.5V.

3.3.3 Impact of Source Doping

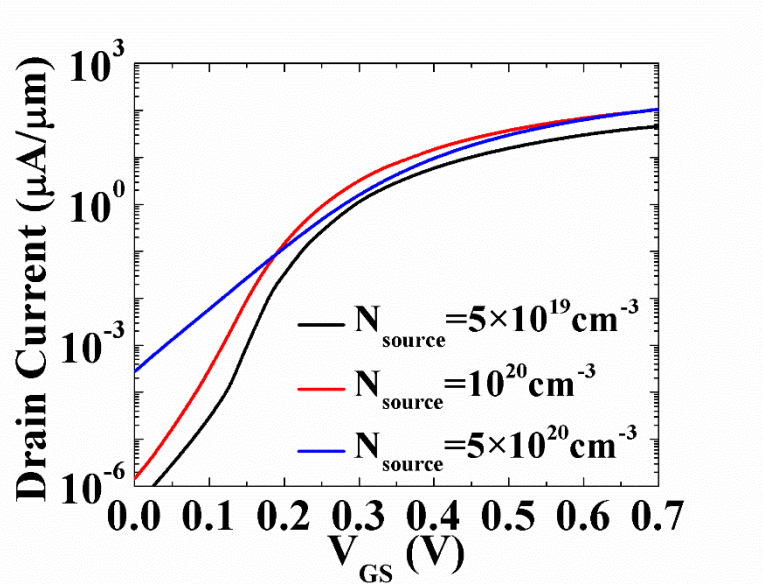


Fig. 3.5 The transfer characteristics of the Ge-pocket TFETs with different source doping concentrations with V_{DS}=0.5V.

Fig. 3.5 shows the transfer characteristics of the Ge-pocket TFET with different source doping concentrations. The device with $N_{source}=5\times10^{20}cm^{-3}$ shows a significantly larger leakage current and a degraded *SS* at the low current regime because of the large overlap between the valence band of the source and the conduction band of the channel even at low gate bias as shown in Fig. 3.6(a). Fig. 3.6(b) shows that increasing the source doping concentration increases the lateral electric field at the tunnel junction, which in turn reduces the tunnel barrier width. This results in a higher tunneling probability that is close to one. However, increasing the source doping moves the hole quasi-Fermi level away from the valence band edge in the source, which reduces the available electrons for tunneling in the source [71]. The tunneling current is the product of the tunneling probability and the number of available electrons. Thus, there exists an optimum source doping concentration for high I_{ON}, as shown in [72]. The optimum source doping concentration is found to be $10^{20}cm^{-3}$ (Fig. 3.7).

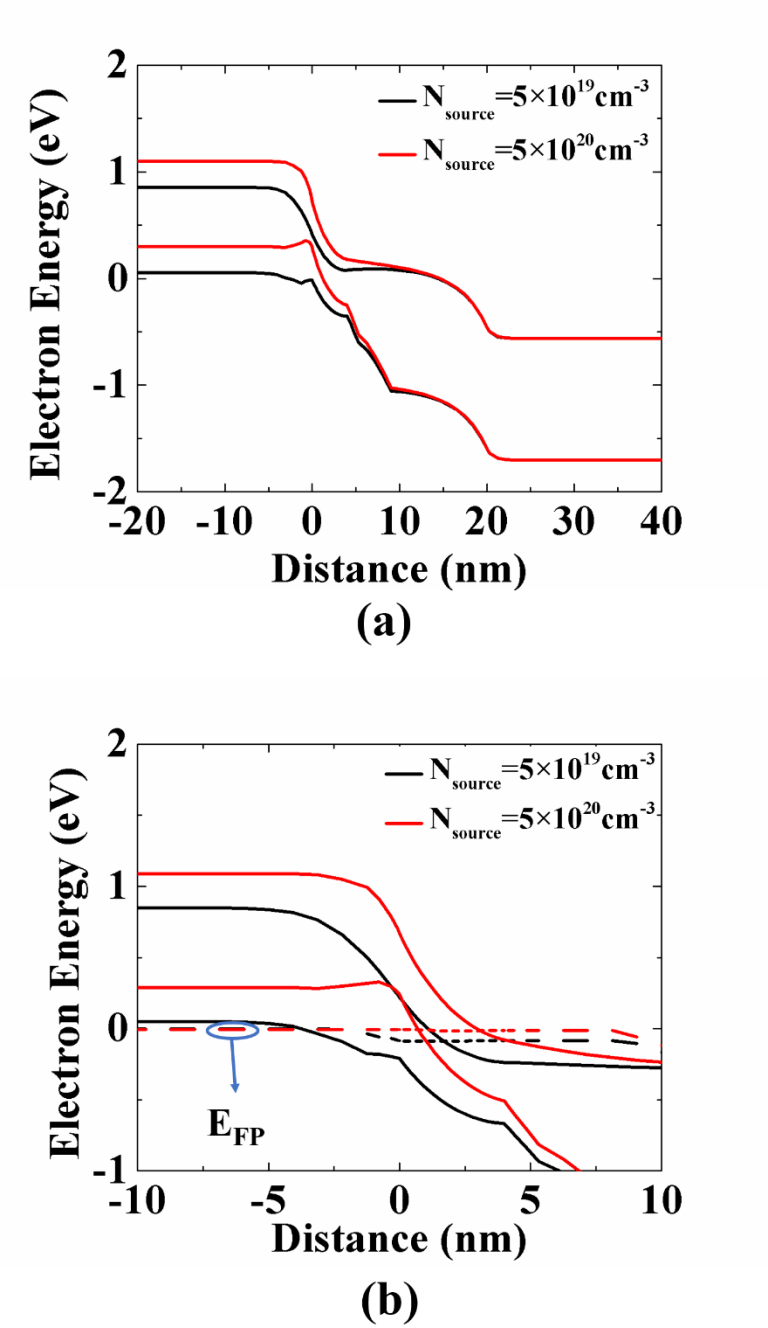


Fig. 3.6 The band diagram of the Ge-pocket TFETs with different source doping concentrations at (a) low gate bias V_{GS}=0.1V and (b) high gate bias V_{GS}=0.5V. V_{DS} is set to 0.5V.

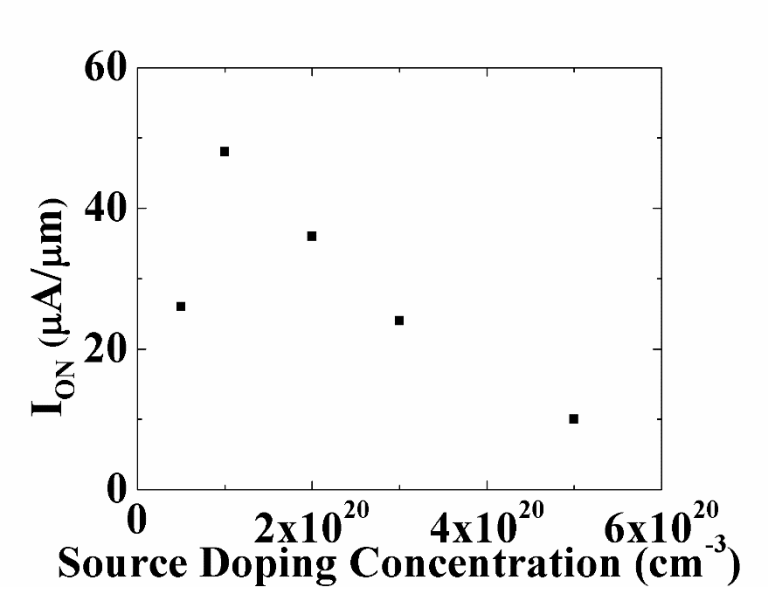


Fig. 3.7 I_{ON} of the Ge-pocket TFET as a function of the source doping concentrations with V_{DD}=0.5V.

3.3.4 Impact of Pocket Doping

The concept of counter-doped pocket has been previously discussed [22],[68]. Increasing the pocket doping concentration significantly improves the performance of TFETs by enhancing the electric field at the tunnel junction and reducing the tunnel barrier width (Fig. 3.8). However, for a pocket doping higher than $5\times10^{19}cm^{-3}$, the pocket comes out of full depletion (Fig. 3.9). The non-depleted n^+ pocket region serves as an intrinsic source, and the device becomes an n^+p^+ tunnel junction in series with a conventional MOSFET. Therefore, the device loses its steep switching characteristics. The pocket doping concentration needs to be optimized to ensure the full depletion of the pocket.

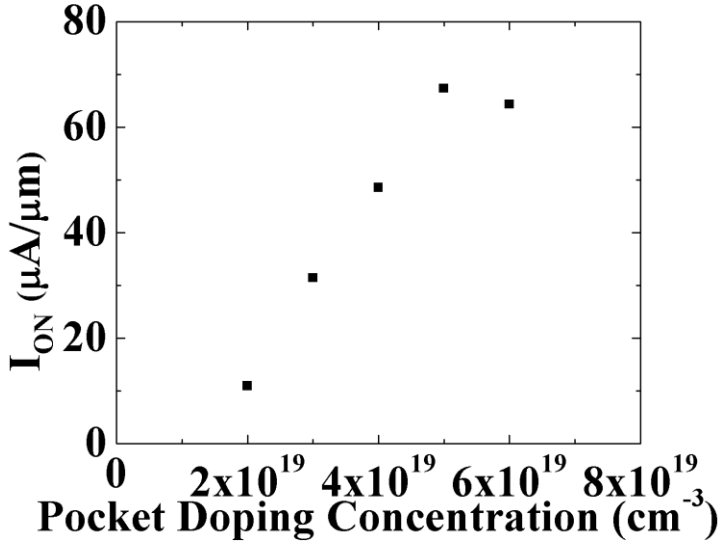


Fig. 3.8 I_{ON} of the Ge-pocket TFET as a function of the pocket doping concentrations with V_{DD}=0.5V.

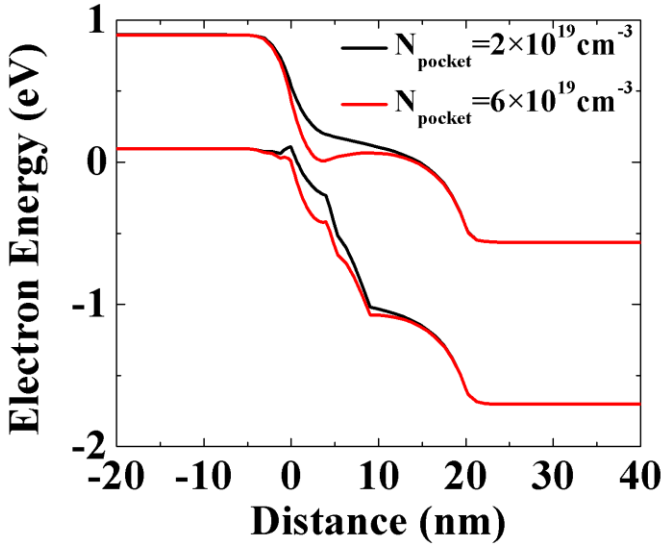


Fig. 3.9 The band diagram of the Ge-pocket TFETs with different pocket doping concentrations at a low gate bias V_{GS}=0.1V. The pocket region comes out of full depletion for high pocket doping concentration. V_{DS} is set to 0.5V.

3.3.5 Impact of Channel Doping

I_{ON} of the proposed structure is independent of channel doping for a concentration up to 10^{18}cm^{-3}. This is due to the fact that the dose of the total depletion charge in the body is small in this doping range because of the thin body of the device. As a result, the doping in the channel has

a negligible impact on the electrostatic profile. In addition, since the channel resistance is dominated by the tunnel junction, the change in the mobility due to the channel doping concentration has a negligible effect on I_{ON}.

3.3.6 Impact of Drain Doping

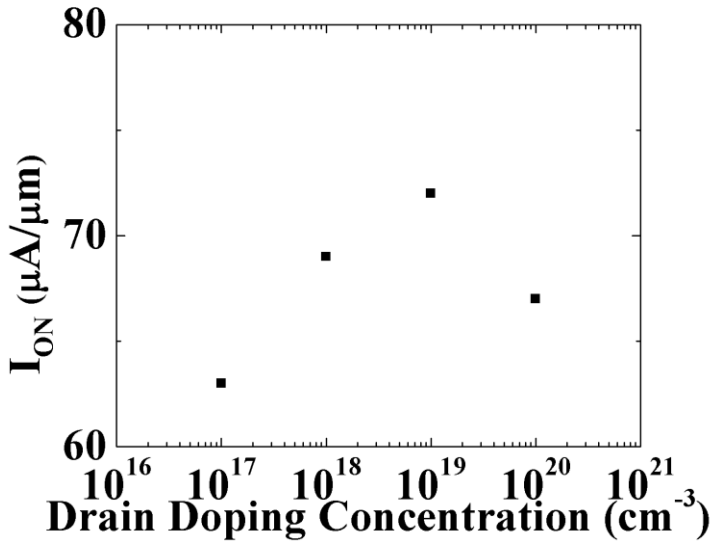
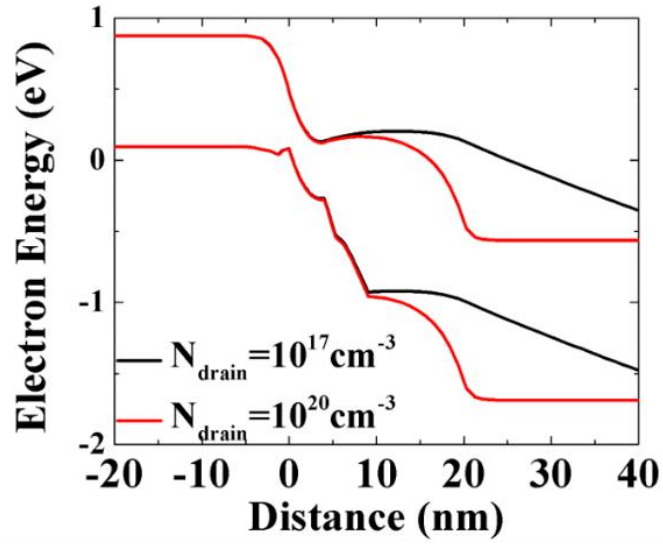


Fig. 3.10 I_{ON} of the Ge-pocket TFET as a function of the drain doping concentration.

Fig. 3.10 shows the impact of the drain doping concentration on I_{ON} of the Ge-pocket TFET. For a high drain doping concentration, the electric field from the drain penetrates to the channel region, and the conduction band in the channel is lowered, similar to the DIBL in conventional MOSFETs, as shown in Fig. 3.11(a). This leads to a reduction in the tunnel barrier height and the width in the channel, which increases the tunneling current at a low gate bias. This phenomenon is expected to become more severe for shorter L_{gate}. As the drain doping concentration is reduced, the electric field from the drain to the channel decreases. Therefore, the leakage current due to the conduction band lowering is reduced. However, the parasitic resistance of the drain becomes

significant as indicated by the electron quasi-Fermi level in the drain, as shown in Fig. 3.11(b). The parasitic voltage drop leads to a reduction in I_{DS}. The optimum drain doping concentration is found to be $10^{19}cm^{-3}$. Note that the impact of the drain doping on the contact resistivity is not considered, as the simulation is intended to emphasize the impact of the drain doping on the leakage current. The contact resistance can be reduced by adding a highly doped drain between the lightly doped drain and the metal contact, which resembles the concept of the sub-collector in BJT.



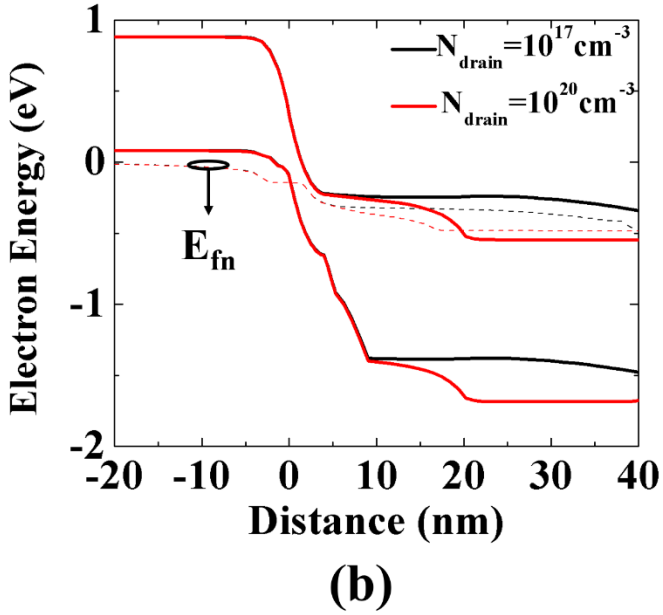


Fig. 3.11 The band diagram of the Ge-pocket TFET with different drain doping concentrations (a) low gate bias V_{GS}=0.1V and (b) high gate bias V_{GS}=0.5V. V_{DS} is set to 0.5V.

3.4 Scalability and Benchmark

The Ge-pocket TFET with an optimized doping concentration ($N_{source}=10^{20}cm^{-3}$, $N_{pocket}=5\times10^{19}cm^{-3}$, $N_{channel}=10^{16}cm^{-3}$, and $N_{drain}=10^{19}cm^{-3}$) has been benchmarked against 14nm node FinFETs (L_{gate}=20nm) in terms of I_{ON} [2],[73]. I_{ON} of the FinFETs is extracted from the experimental results and verified by calibrated simulations. Under V_{DD} of 0.5V, the Ge-pocket TFET exhibits an I_{ON} that is ~125% higher than the FinFETs, as shown in Fig. 3.12(a). Due to the steep *SS* at the low current regime, the advantage of the proposed structure over the FinFET technology becomes more significant as V_{DD} is further reduced. As V_{DD} is scaled down to 0.3V, the enhancement in I_{ON} increases to over 100×.

The performance of the Ge-pocket TFET for future technology nodes has been examined. The physical dimensions of the devices are adopted from ITRS (Table 3.2), and the optimized doping profile for 14nm node is used for all L_{gate}, as shown in Fig. 3.12(b). The proposed structure has demonstrated potential in both L_{gate} and V_{DD} scaling. Note that the scaling of channel thickness is less straightforward due to the strong QC. For a more rigorous treatment, NEGF is required.

Table 3.2 The physical dimensions of the Ge-pocket TFET for future nodes suggested by ITRS.

Tech. Node	**14nm**	**10nm**	**7nm**
L_{gate} (nm)	**20**	**16**	**14**
T_{ox} (nm)	**0.8**	**0.7**	**0.7**
T_{body} (nm)	**8**	**6**	**5**

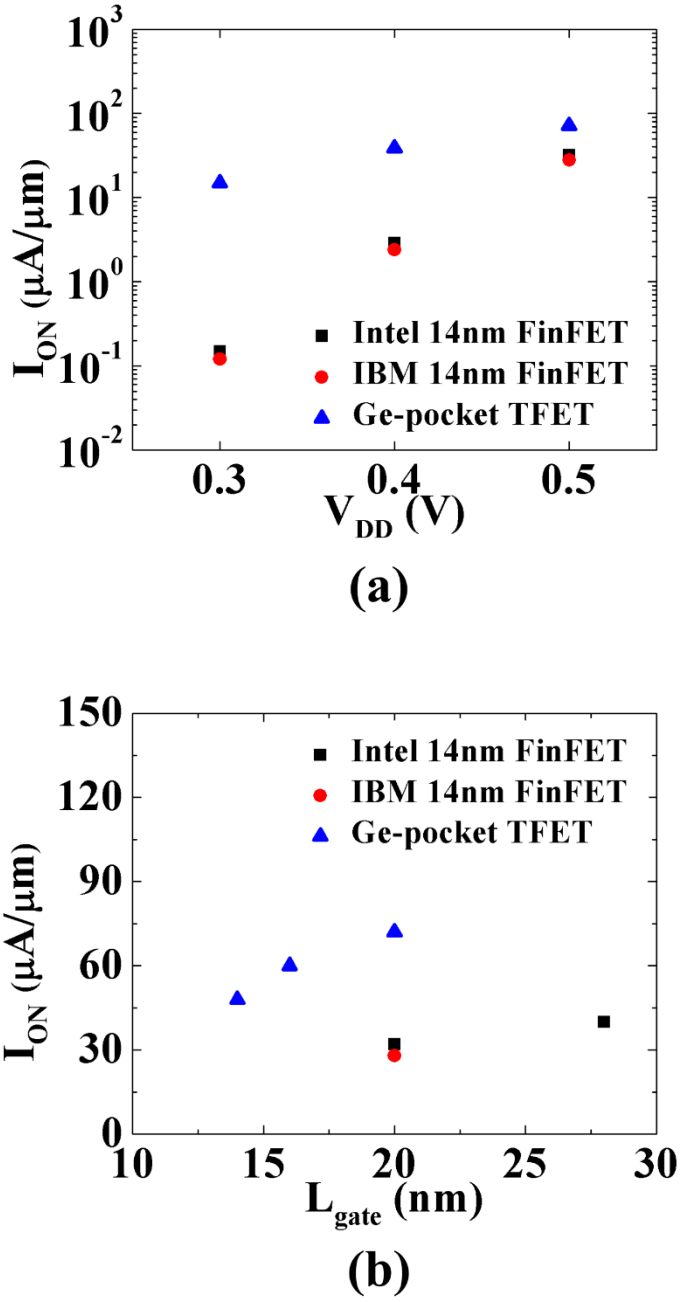


Fig. 3.12 Benchmark of the Ge-pocket TFET against 14nm FinFETs for (a) V_{DD} scaling and (b) L_{gate} scaling with V_{DD}=0.5V.

3.5 Impact of Pocket Doping Gradient

The tunneling process is sensitive to the electrostatic potential profile across the tunneling junction. To obtain a more realistic prediction of the device performance, the impact of doping gradients at the junction needs to be taken into consideration. The doping profile for a 14nm-node Ge-pocket TFET is shown in Fig. 3.13. The source doping gradient is set to be 3nm/dec, which is among the steepest slope achieved with CVD growth techniques. The pocket doping gradient varies from 2nm/dec to 6nm/dec. The I_{ON} as a function of the gradient is plotted in Fig. 3.14. For a pocket doping gradient of 2nm/dec, the reduced dose of p-type dopants results in a reduction in the lateral electric field across the junction, therefore a reduced I_{ON}. For a pocket doping gradient of 6nm/dec, the pocket comes out of full depletion due to the high dose of p-type dopants, and the device lost its steep switching characteristics. The optimum pocket gradient is around 3nm/dec for a peak pocket doping concentration of $5\times10^{19}cm^{-3}$. I_{ON} can be further enhanced by increasing the peak pocket doping concentration.

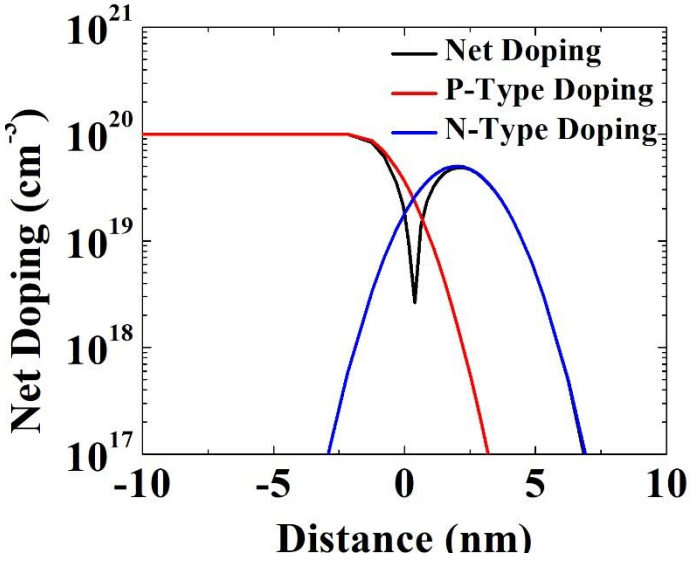


Fig. 3.13 The doping profile at the source/pocket junction.

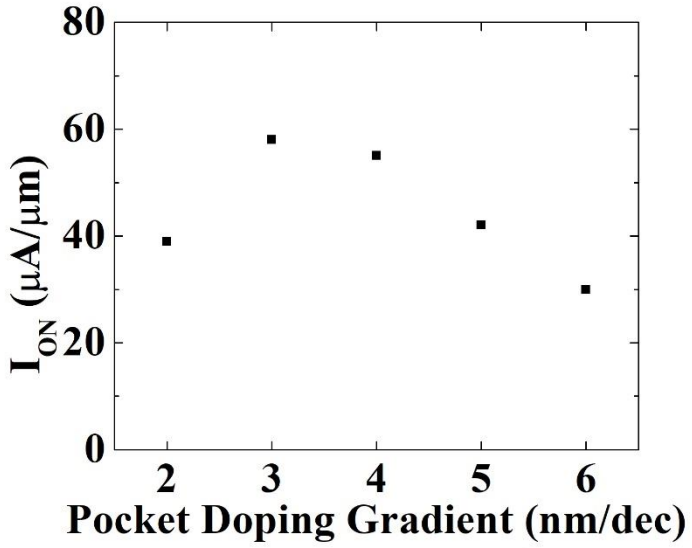


Fig. 3.14 I_{ON} as a function of pocket doping gradient with a peak pocket doping concentration of $5\times10^{19}cm^{-3}$.

3.6 Feasibility of P-type SiGe-Pocket TFET

For TFETs to be adopted by low power complementary logic applications, a well-balanced p-type TFET is needed. The concept of SiGe-pocket is also applicable to p-type devices. However, due to the large valence band offset between the pocket and the channel, the overlap between the conduction band of the source and the valence band of the channel even at off-state (Fig. 3.15). Therefore, the pocket width and the Ge composition need to be optimized to suppress the leakage current. An optimized Ge composition profile with a composition grading slope of 0.2/nm is shown in Fig. 3.16. The physical dimensions of the device are chosen to enable a fair performance comparison between the p-type $Si_{0.5}Ge_{0.5}$-pocket TFET and the 14nm FinFET. An abrupt doping profile is assumed for the simulation. By increasing the Ge composition and incorporating the counter-doping in the pocket region, p-type $Si_{0.5}Ge_{0.5}$-pocket TFET shows improvement in both I_{ON} and *SS* (Fig. 3.17). In addition, it has been benchmarked against 14nm FinFET in terms of I_{ON} and outperforms the FinFET for $V_{DD}\leq0.4V$ (Fig. 3.18).

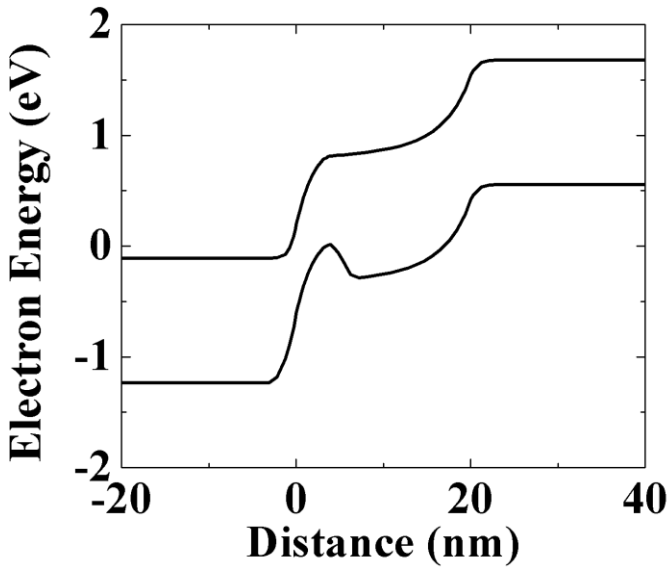


Fig. 3.15 The band diagram of the p-type $Si_{0.5}Ge_{0.5}$-pocket TFET with a 4nm p-type pocket at off-state.

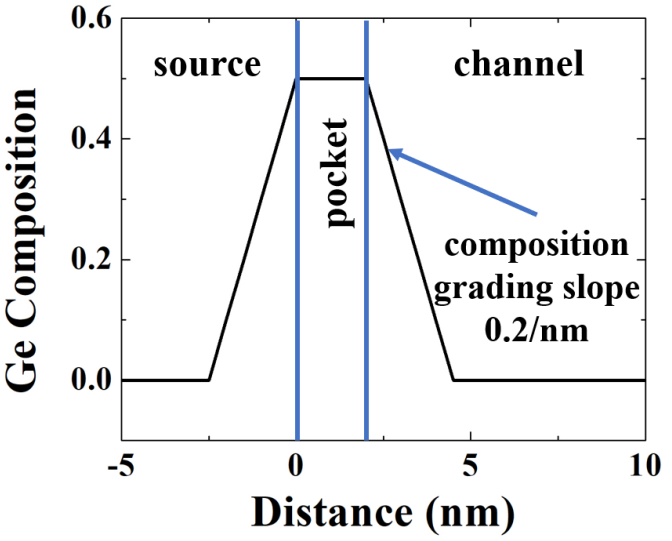


Fig. 3.16 The Ge composition profile along the channel direction for the optimized p-type $Si_{0.5}Ge_{0.5}$-pocket TFET.

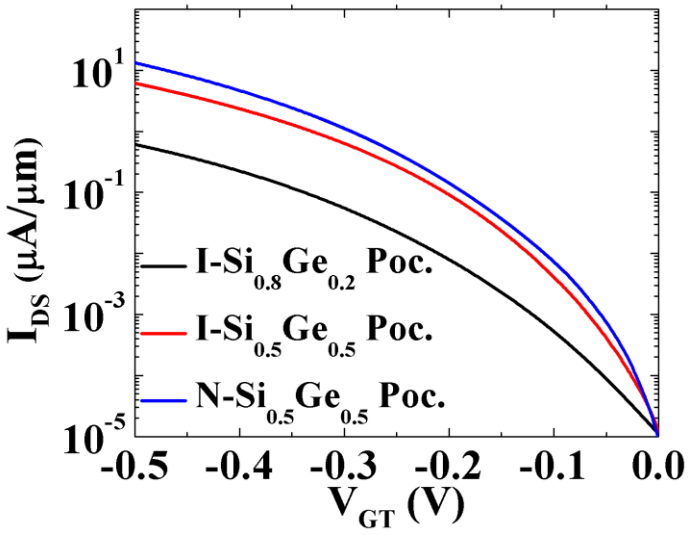


Fig. 3.17 The transfer characteristics of p-type SiGe-pocket TFETs with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket, an intrinsic $Si_{0.5}Ge_{0.5}$ pocket, and a p-type $Si_{0.5}Ge_{0.5}$ pocket.

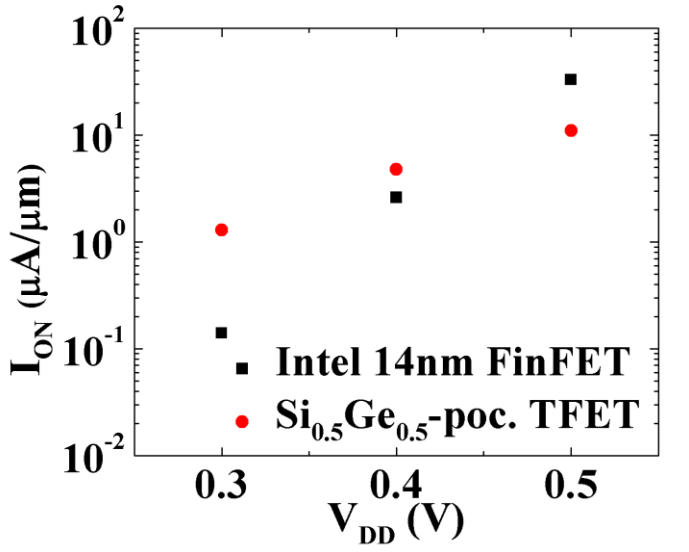


Fig. 3.18 The benchmark of the p-type TFET with a counter-doped $Si_{0.5}Ge_{0.5}$ pocket against 14nm FinFETs with reduced V_{DD}.

3.7 Summary

In this section, the concept of the Ge-pocket TFET is presented. SiGe is chosen over III-V materials because of its VLSI compatibility, mature material synthesis, and tunable bandgap.

Thanks to the reduced bandgap of the fully-strained Ge and the enhanced lateral electric field at the tunnel junction, the device performance is improved significantly. The ambipolar conduction at the drain side is suppressed by the large bandgap of Si. The proposed device structure shows performance superior to both $Si_{0.5}Ge_{0.5}$-source and Ge-source TFETs. The impact of doping concentrations at different regions on the device performance has been investigated. The optimized structure exhibits the potential to achieve steep *SS* and I_{ON} higher than 14nm FinFET technology under V_{DD} of 0.5V. The simulation results suggest that the proposed structure has excellent scalability in terms of L_{gate} and V_{DD}. Its performance advantage over the FinFETs increases significantly as V_{DD} is further reduced. A more rigorous examination of the device scalability will require NEGF due to the strong QC. The proposed structure provides a promising solution for low power logic applications for 14nm node and beyond. The feasibility of the p-type SiGe-pocket TFET has also been examined.

Chapter 4

Fabrication and Characterization of Vertical SiGe-Pocket TFETs

4.1 Introduction

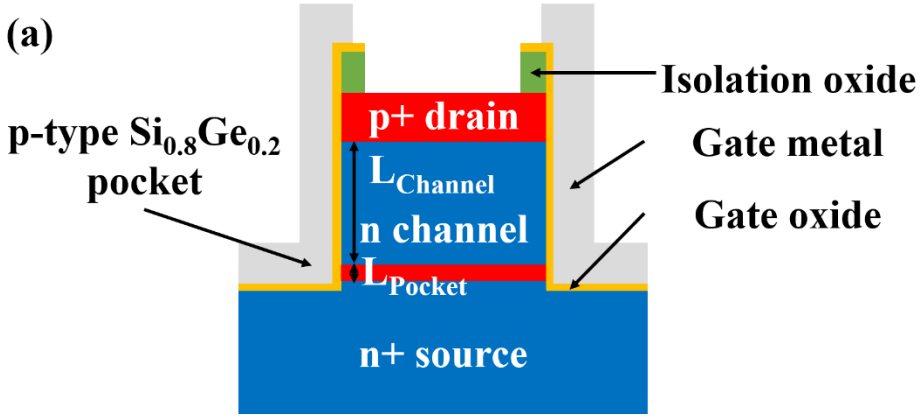


Fig. 4.1 The schematic of a vertical $Si_{0.8}Ge_{0.2}$-pocket TFET.

As discussed in the previous chapter, the device performance of TFETs improves significantly by adopting the countered-doped SiGe pocket due to the reduced tunnel barrier height and the enhanced lateral electric field. To experimentally demonstrate the advantages of SiGe-pocket TFET, vertical p-type TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket have been fabricated. The band alignment of Si/$Si_{0.8}Ge_{0.2}$ heterojunction is shown in Fig 4.2. Si homojunction TFETs and TFETs with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket have been fabricated in parallel. The rationales of adopting vertical structure are threefold: first, it is easier to realize the desired doping/composition profile vertically due to the growth technique; second, the channel length is independent of photolithography, and it is less susceptible to process variation; in addition, the vertical structure has great potential in 3D integration ICs. The Si/SiGe heterojunctions have been realized by reduced pressure chemical vapor deposition (RPCVD). All devices are fabricated with a low

thermal budget process to preserve the as-grown doping/composition profile. Compared with the other two types of devices, the TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket show significant improvements in I_{ON} and *SS* due to the enhanced transport across the tunnel junction.

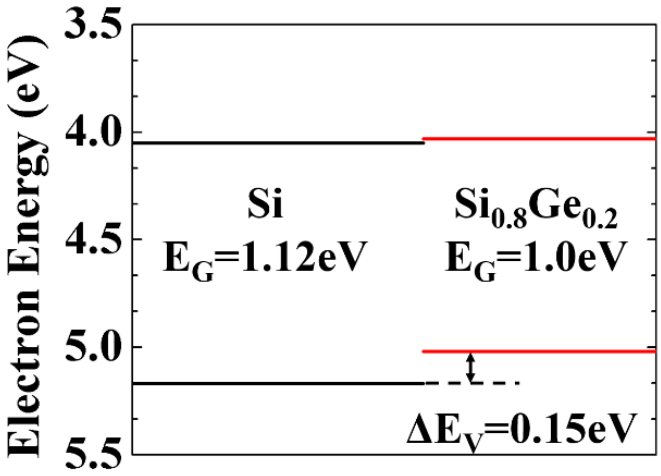


Fig. 4.2 The band alignment of Si/Si0.8Ge0.2 heterojunction.

4.2 Material Synthesis

The epitaxial growth of Si/SiGe heterojunctions is achieved by RPCVD, and the desired doping profiles are realized by in-situ doping. No dopant activation annealing is required in this case. Therefore, the thermal budget of the growth is significantly reduced, which is critical for preserving the desired doping/composition profile. RPCVD provides a few advantages over MBE: higher throughput, low background contamination, better deposition uniformity, and additional degrees of freedom to control material characteristics. The growth rate, Ge composition, and doping concentration of deposited film can be adjusted by tuning gases flow rate, pressure, and substrate temperature. In this section, RPCVD growth of in-situ doped $Si_{0.8}Ge_{0.2}$ has been

investigated in detail, and the growth conditions for all three types of the TFETs are discussed. In this study, the chamber pressure, the H_2 flow rate, and the $SiCl_2H_2$ flow rate are fixed at 20torr, 20slm, and 75sccm, respectively.

4.2.1 Growth of In-situ Doped SiGe

The growth of a high-quality SiGe layer with high active doping concentration is the most critical step in fabricating the TFETs with a SiGe pocket. During epitaxial growth, Ge atoms tend to segregate to the surface states and to minimize the surface free energy, which results in a smeared-out composition profile. To achieve a sharp composition profile, a reduced growth temperature is critical. Under low temperatures, the surface states are passivated by H atoms [70]. Thus, the surface segregation is suppressed. However, lowering the growth temperature leads to poor material quality. Therefore, the growth temperature needs to be properly optimized. The growth conditions for the SiGe pocket is discussed in detail.

Below 650°C, the growth rate of Si with $SiCl_2H_2$ is limited by the desorption of H and Cl atoms from the surface. However, the incorporation of Ge makes the surface desorption of H and Cl atoms more efficient. In addition, GeH_4 decomposes at a lower temperature than $SiCl_2H_2$. Thus, the epitaxial growth of SiGe can be done at a much low temperature. Intrinsic SiGe is first grown with GeH_4 as a precursor at different temperatures to identify the temperature window where a reasonable growth (~5nm/min) rate can be achieved with GeH_4 flow of 10sccm. Fig. 4.3 shows the growth rate and the Ge composition as a function of growth temperature, extracted from high-resolution x-ray diffraction (HRXRD) measurements. For a growth rate higher than 550°C, the growth rate is too high to have precise control of the pocket thickness. 24nm of $Si_{0.5}Ge_{0.5}$ has been

pseudomorphically grown on Si at 550°C, and the film remains fully strained as indicated by the interference fringes, as shown in Fig. 4.4. Atomic force microscopy (AFM) measurement shows that the RMS surface roughness of this sample is round 0.1nm (Fig. 4.5), which is similar to the value of the starting substrate. Both the HRXRD and the AFM results suggest the high-quality as-deposited $Si_{0.5}Ge_{0.5}$ epilayer.

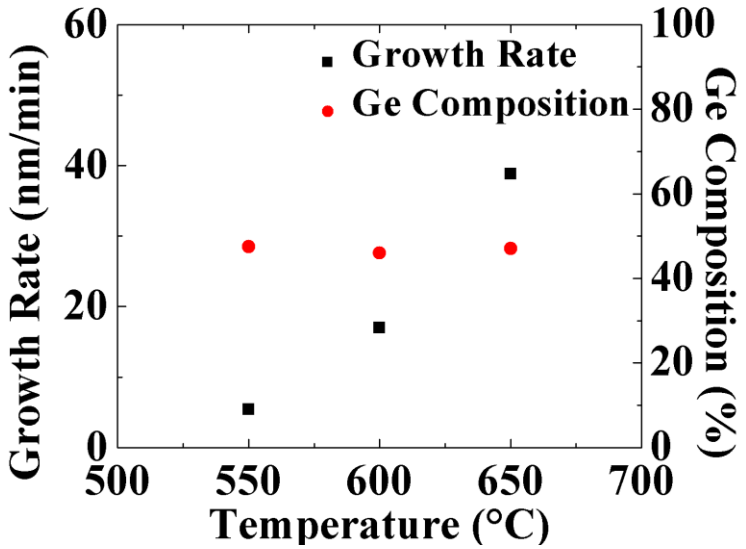


Fig. 4.3 The growth rate and the Ge composition of SiGe as a function of growth temperature.

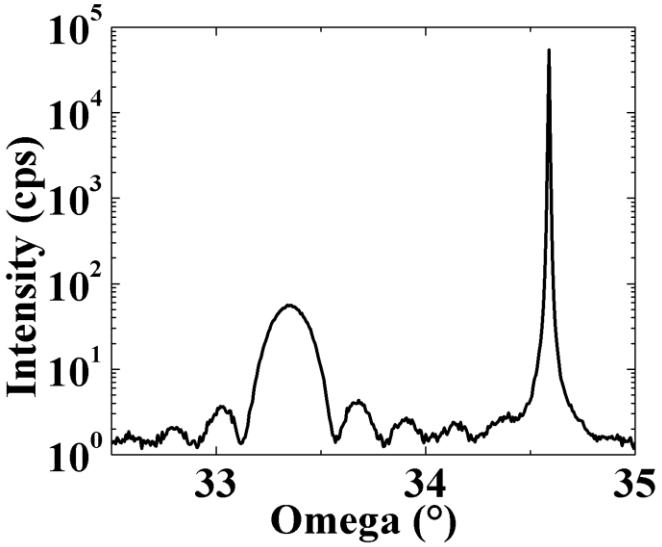


Fig. 4.4 The HRXRD of 24nm of $Si_{0.5}Ge_{0.5}$ on Si substrate.

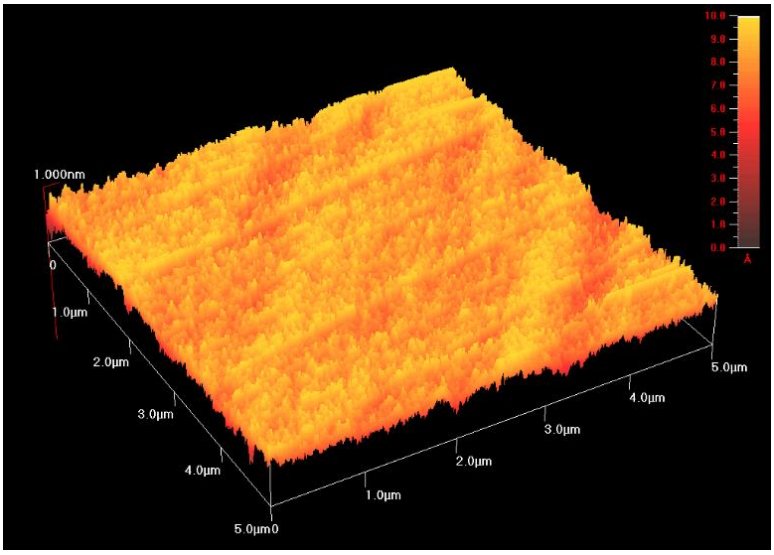


Fig. 4.5 The AFM measurement of $Si_{0.5}Ge_{0.5}$ sample grown at 550°C.

TFETs with a 5nm-intrinsic $Si_{0.5}Ge_{0.5}$ has been fabricated. The devices are unable to switch off, and the on/off current ratio is less than one order of magnitude. The excessive leakage current is likely due to the relaxation of the metastable $Si_{0.5}Ge_{0.5}$: the $Si_{0.5}Ge_{0.5}$ pocket thickness exceeds

its equilibrium thickness of 3.7nm [79], and the strained pocket layer relaxes during the subsequent Si channel and the Si source growth at elevated temperatures. The channel and the source are deposited at higher temperatures to achieve a reasonable growth rate and good material quality. Thus, reducing the growth temperature is not viable. In addition, SiGe films grown at low temperature are susceptible to contaminations, which lead to dislocations. Though the dislocation density is below the detection limit of HRXRD, it might still impact the electrical properties of the SiGe film. Consequently, the Ge composition of the pocket layer needs to be reduced, and the growth temperature needs to be increased. Fig 4.6 and Fig. 4.7 shows the Ge composition and growth rate of intrinsic SiGe as a function of mass flow ratio (MFR) between GeH_4 and $SiCl_2H_2$ at various growth temperatures. All things considered, a growth temperature of 650°C and an MFR of 0.02 is used for growing the intrinsic SiGe pocket.

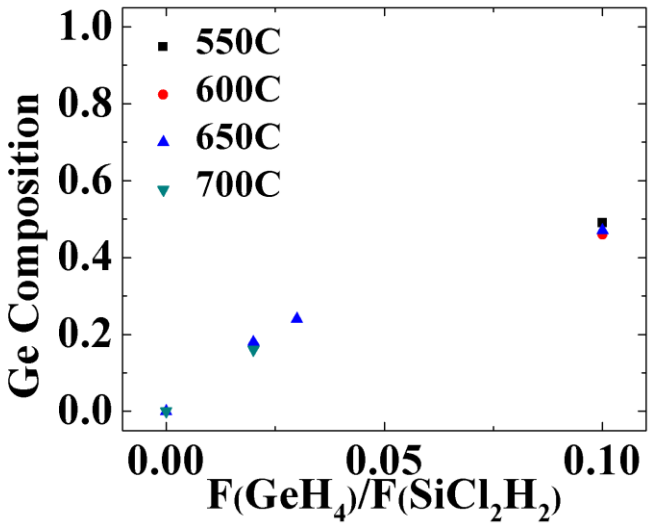


Fig. 4.6 The Ge composition of SiGe as a function of MFR at various growth temperatures.

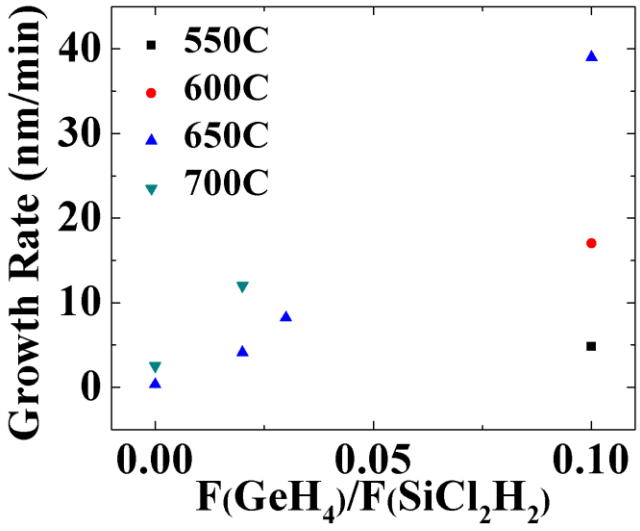


Fig. 4.7 The growth rate and the Ge composition of SiGe as a function of MFR at various growth temperatures.

By introducing the dopant gas, in this case, B_2H_6, into the chamber during the intrinsic SiGe pocket deposition, the SiGe layer can be in-situ doped. The dopant gas is mixed with H_2 by a mass flow controller before flowing into the chamber. Thus, a wide range of doping concentrations can be achieved. The incorporation of B has an unnoticeable impact on the Ge composition of the SiGe film, and the growth rate slightly increases with the B_2H_6, as shown in Fig. 4.8. The growth rate increases because the B atoms at the surface help the desorption of H and Cl atoms. The Ge composition and the growth rate of the deposited SiGe films are extracted from ellipsometry measurements. The active doping concentrations of the SiGe films are extracted from TLM measurements based on the assumption that heavily-doped SiGe and Si have the same mobility.

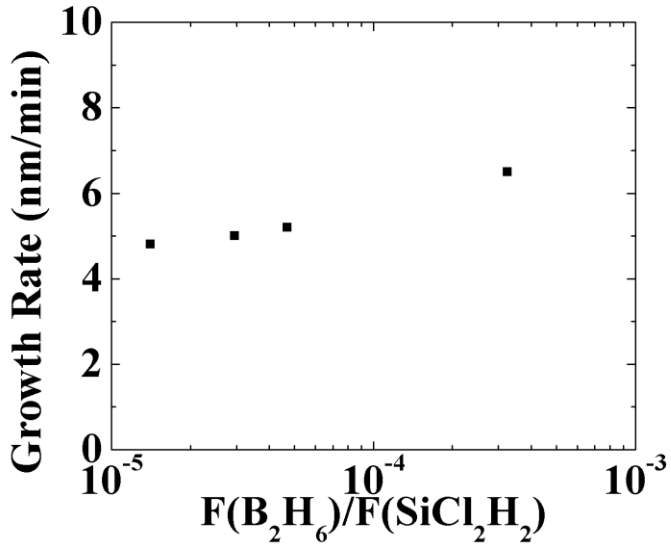


Fig. 4.8 The growth rate of B-doped $Si_{0.8}Ge_{0.2}$ films as a function of MFR.

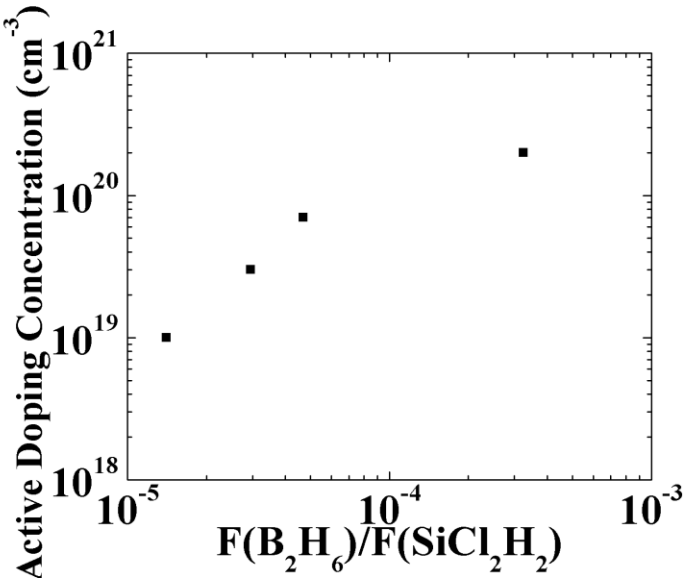


Fig. 4.9 The active doping concentration of $Si_{0.8}Ge_{0.2}$ films as a function of MFR.

4.2.2 Growth of Si/$Si_{0.8}Ge_{0.2}$ Heterojunctions for TFETs

All epitaxial growths are carried out on <100> degenerated P-doped 4-inch wafers with a doping concentration of $3\times10^{19}cm^{-3}$. The epitaxial growth flow of the p-type TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket is listed in Table 4.1. Wafers first go through RCA clean and followed by HF dip to clean the surfaces. The growth starts with hydrogen bake to remove surface native oxide. A clean, oxide-free surface is critical for achieving high-quality epitaxial film. All layers are then epitaxially grown in sequence. In between each deposition, a chamber etching/coating step is added. In this step, the chamber wall is first etched with HCl gas and then coated with a thin layer of Si. This helps to suppress the dopant absorption/emission by the chamber wall, which is critical for achieving a sharp doping profile. The growth recipe is modified for the p-type TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket and the Si homojunction p-type TFET. The dopant gas is turned off for the p-type TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket, and the pocket layer deposition step is removed for Si Homojunction p-type TFET. Note that the pocket thickness is increased from 4nm in the previous simulation study to 5nm due to the increased tunnel barrier of $Si_{0.8}Ge_{0.2}$ compared with Ge.

Table 4.1 Epitaxial growth flow for p-type TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket.

Epitaxial growth flow chart for p-type TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket		
1	RCA clean followed by HF dip	Surface cleaning
2	Hydrogen bake	Native oxide desorption at 1100°C for 10mins
3	n^+ source layer deposition	100nm $5\times10^{19}cm^{-3}$ P-doped Si at 1000°C
4	Chamber etching/coating	Minimizing P emission from chamber wall
5	p^+ pocket layer deposition	5nm $3\times10^{19}cm^{-3}$ B-doped $Si_{0.8}Ge_{0.2}$ at 650°C
6	Chamber etching/coating	Minimizing B emission from chamber wall
7	n channel layer deposition	150nm $5\times10^{17}cm^{-3}$ As-doped Si at 800°C
8	Chamber etching/coating	Minimizing As emission from chamber wall
9	p^+ drain layer deposition	120nm $6\times10^{19}cm^{-3}$ B-doped Si at 700°C

4.3 Process Flow

The process flow for all three devices is identical and outlined in Table 4.2 The key process steps of the TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket are illustrated in Fig. 4.10. After the epitaxial growth, SiO_2 is deposited on the samples by plasma-enhanced CVD (PECVD). It is used as an etch-stop layer for the later gate stack etching step. Mesa structures are defined by photolithography and then etched by CHF_3/CF_4-based chemistry (for SiO_2) and HBr/Cl_2-based chemistry (for Si/SiGe layers) sequentially. The channel length $L_{Channel}$ is 150nm, and the pocket length L_{Pocket} is to 5nm as defined during the growth.

After the definition of mesa structures, the samples are cleaned in diluted HF before the gate stack deposition. The gate stack consists of 4.4nm of Al_2O_3 (EOT~3.5nm including ~0.8nm of native oxide) and 10nm TiN deposited by atomic layer deposition (ALD), followed by sputtered Al-1%Si. A thin layer of TiN is incorporated as a barrier layer to prevent any damage from subsequent Al-1%Si sputtering or degradation due to Al_2O_3 and Al reaction. Previously, Al_2O_3-based MOS capacitors have been fabricated without a TiN barrier layer. An increase in EOT has been measured over time, and it saturates after two weeks. With the insertion of a thin TiN layer, no degradation has been observed over a month. For gate metal, Al-1%Si is used to suppress the Al spiking during subsequent annealing, which might penetrate the isolation oxide and cause a short circuit. The gate metal is then patterned and etched by Cl_2/BCl_3-based chemistry.

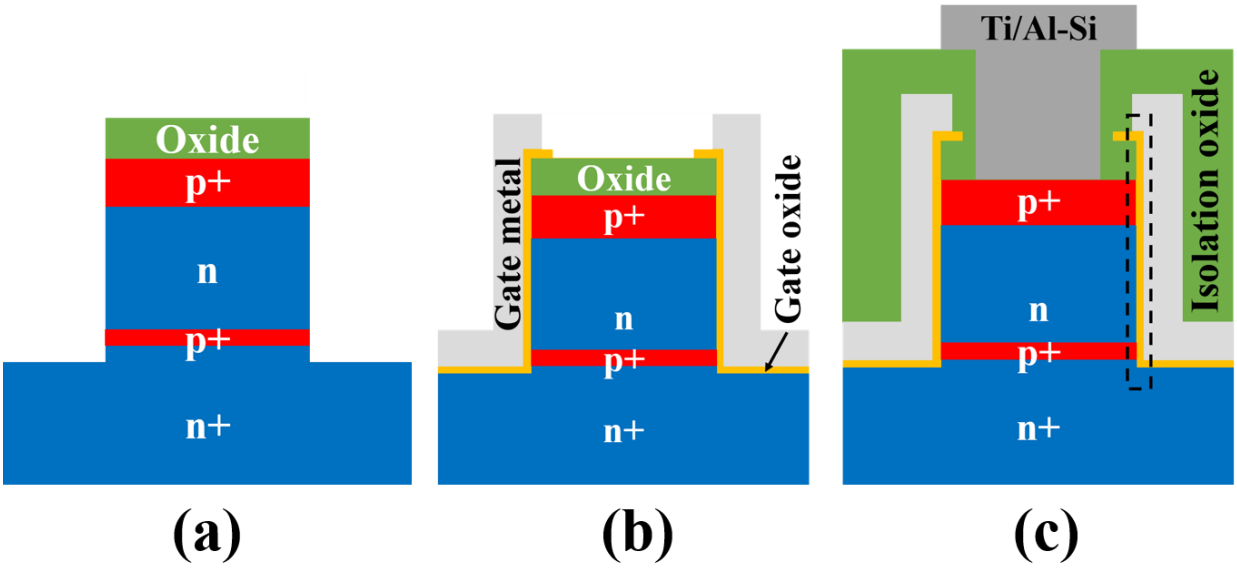


Fig. 4.10 Illustration of the vertical p-type TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket at different process steps: (a) after step 4, Si/SiGe layers etch, (b) after step 10, gate metal etch, and (c) after step 18, metal contact etch.

After the completion of the gate module, SiO_2 is deposited by PECVD as an isolation layer. Contact holes are patterned and etched to gain access to the source, the drain, and the gate. Ti/Al is sputtered, patterned, and etched to form contact pads. A pre-sputter etch step has been added before the metal deposition to clean the surface. Ti acts as a barrier layer to prevent spiking and other interaction between Al and Si. In addition, it dissolves residual native oxide and results in an oxygen-free interface for metal contact. The process is finished by forming gas anneal at 400°C for 1 hour. The cross-sectional SEM of the fabricated device is shown in Fig. 4.11. All process steps are carried out under 400°C to preserve the as-grown doping/composition profile.

Table 4.2 Detailed process flow of the vertical p-type TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$.

Process Flow of the Vertical P-type TFETs with a Counter-doped $Si_{0.8}Ge_{0.2}$		
1	Etch-stop layer deposition	220nm SiO_2 by PECVD
2	Mesa patterning	MLA150
3	Oxide etch	220nm dry etch with CHF_3/CF_4-based chemistry
4	Si/SiGe layers etch	290nm dry etch with HBr/Cl_2-based chemistry
5	Photoresist strip	Oxygen plasma
6	Residual oxide removal	30s 50:1 HF dip
7	Gate dielectric/barrier layer deposition	Al_2O_3 4.4nm/TiN 10nm by ALD

8	Gate metal deposition	200nm Al-1%Si by sputtering
9	Gate metal patterning	MLA150
10	Gate metal etch	210nm dry etch with Cl_2/BCl_3-based chemistry (200nm Al-1%Si + 10nm TiN)
11	Photoresist strip	Oxygen plasma
12	Isolation layer deposition	500nm SiO_2 by PECVD
13	Contact window patterning	MLA150
14	Oxide etch	500nm dry etch with CHF_3/CF_4-based chemistry
15	Photoresist strip	Oxygen plasma
16	Source/drain contact metal deposition	2mins pre-sputter etch followed by 10nm Ti/200nm Al via sputtering
17	Contact pad patterning	MLA150
18	Metal contact etch	210nm dry etch with Cl_2/BCl_3-based chemistry (10nm Ti + 200nm Al)
19	Photoresist strip	Oxygen plasma
20	Forming gas annealing	1hr at 400°C

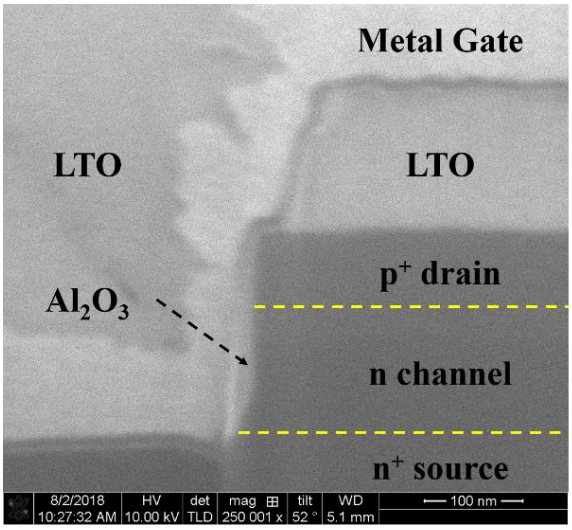


Fig. 4.11 The cross-sectional SEM picture of the fabricated vertical $Si_{0.8}Ge_{0.2}$-pocket TFET, as indicated by the black dash line box in Fig. 4.10(c).

4.4 Electrical Characterization

After the forming gas annealing step, the electrical performance of all three types of TFETs has been characterized. Their transfer and out characteristics are compared and discussed in detail. By incorporating the counter-doped $Si_{0.8}Ge_{0.2}$ pocket, improvements in both I_{ON} and *SS* have been observed. Output current saturation is observed for the TFETs with a $Si_{0.8}Ge_{0.2}$ pocket, under high

V_{DS} with no degradation in the linear region, which suggests good carrier transport across the tunnel junction. The threshold voltage, V_{TH} is defined as V_{GS} at which at I_{DS}=I_{OFF}=10pA/μm under V_{DS}=-0.5V, and I_{ON} is defined as I_{DS} at V_{GT}=V_{GS}-V_{TH}=-2V and V_{DS}=-0.5V.

4.4.1 Transfer Characteristics

Fig. 4.12 shows the transfer characteristics of all three devices at V_{DS}=-0.5V. By introducing an intrinsic $Si_{0.8}Ge_{0.2}$ pocket, the required surface band bending to achieve the same I_{DS} is reduced due to the smaller tunnel barrier height. Hence the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket has a reduced V_{TH}, as compared with the Si homojunction TFET. In addition, incorporating the p-type doping in the pocket increases the lateral electric field, in turn reducing the tunneling distance. Therefore, a smaller overlap is required to achieve the same I_{DS}, and a further decrease in V_{TH} is observed in the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket, as compared with the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket. No ambipolar conduction is observed.

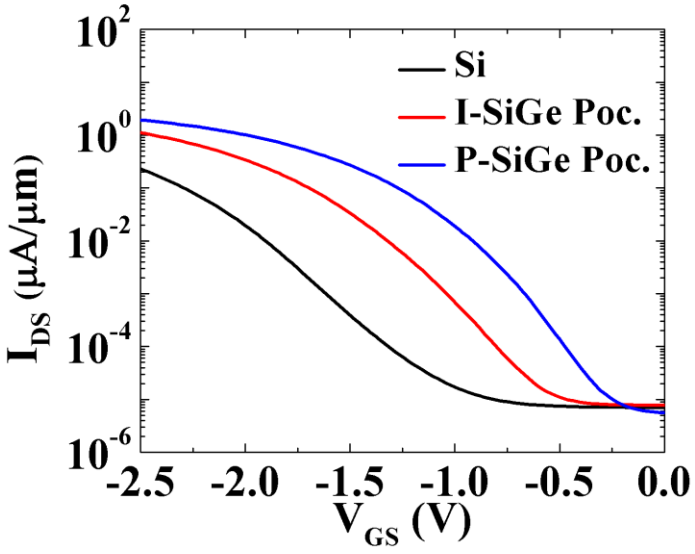


Fig. 4.12 The transfer characteristics of Si homojunction TFET (Si), the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket (I-SiGe Poc.), and the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket (P-SiGe Poc.) with V_{DS}=-0.5V.

The leakage current for all devices saturates around ~5pA/μm. This is dominated by the junction reverse leakage current, which is proportional to the dimensions of the mesa. After matching the off-state current, there are ~85% and ~160% improvement in I_{ON} in the TFETs with an intrinsic and a counter-doped $Si_{0.8}Ge_{0.2}$ pocket, respectively, as compared with the Si homojunction TFET. In addition, steeper turn-on has been observed for devices with a pocket Fig. 4.13. Both improvements are due to the incorporation of the $Si_{0.8}Ge_{0.2}$ pocket. Minimum drain influence on the subthreshold conduction on the TFETs with a $Si_{0.8}Ge_{0.2}$ pocket is observed, which indicates a good short-channel performance (Fig. 4.14).

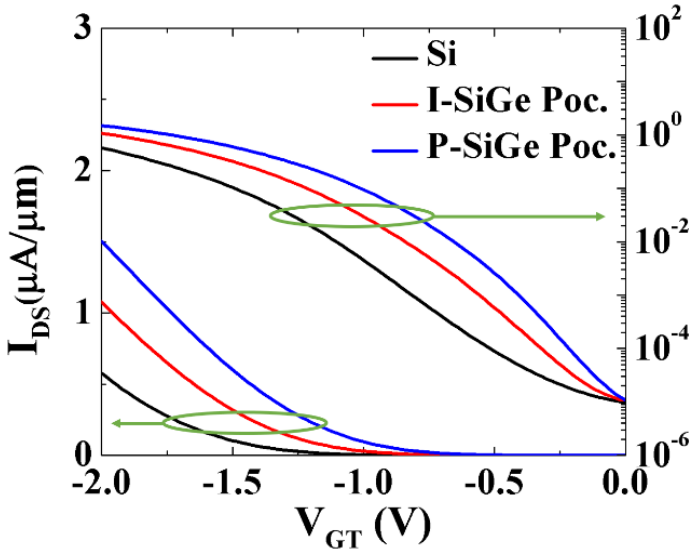
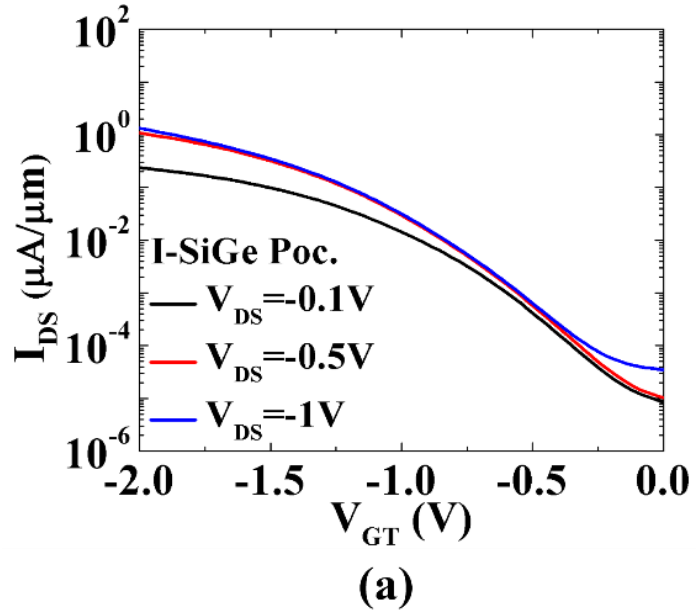


Fig. 4.13 The transfer characteristics of the Si homojunction TFET (Si), the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket (I-SiGe Poc.), and the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket (P-SiGe Poc.) after adjusting gate voltage to compensate for V_{TH} difference (i.e., $V_{GT}=V_{GS}-V_{TH}$) with V_{DS}=-0.5V.



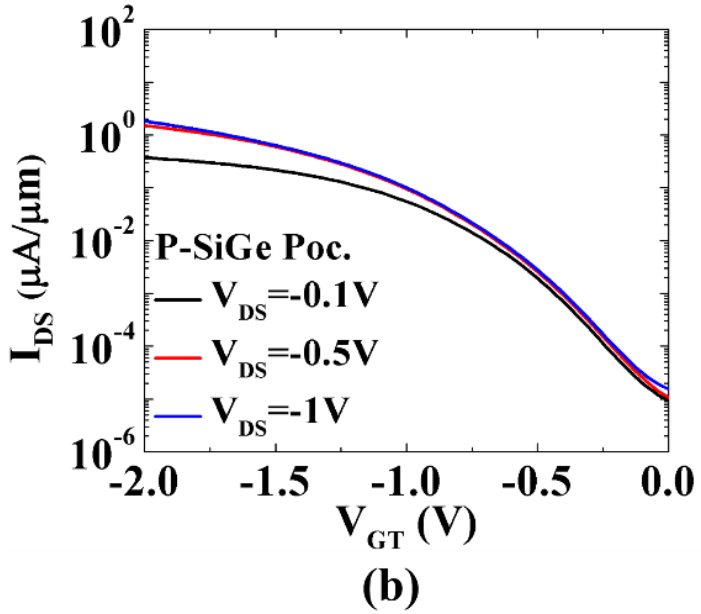


Fig. 4.14 The transfer characteristics of (a) the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket and (b) the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket with different V_{DS}. The drain bias has a minimum impact on the subthreshold conduction.

Fig. 4.15 shows the *SS* as a function of I_{DS}. Among all three devices, the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket shows the lowest *SS* for all current range. The improvements in minimum *SS* and *SS* at 1nA/μm are highlighted in Fig. 4.16. To reduce V_{DD}, steep *SS* needs to extend to a wide range of I_{DS}, namely from ~pA/μm to ~μA/μm. Therefore, it is instructive to look at the *SS* at 1nA/μm. The increasing *SS* in the low I_{DS} range (i.e., around leakage current level) is partially due to the reverse leakage current, which is not modulated by the gate voltage. Both leakage current and degraded *SS* in the low I_{DS} regime can be improved by reducing the channel thickness and making it fully depleted.

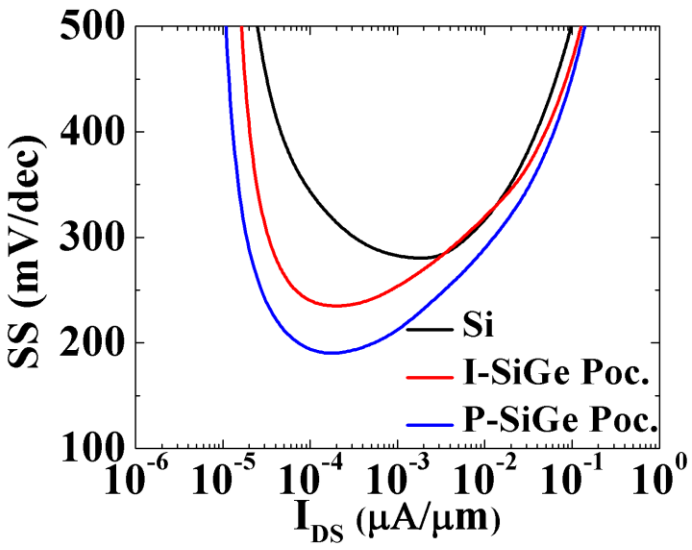


Fig. 4.15 *SS* as a function of I_{DS} for different devices with V_{DS}=-0.5V.

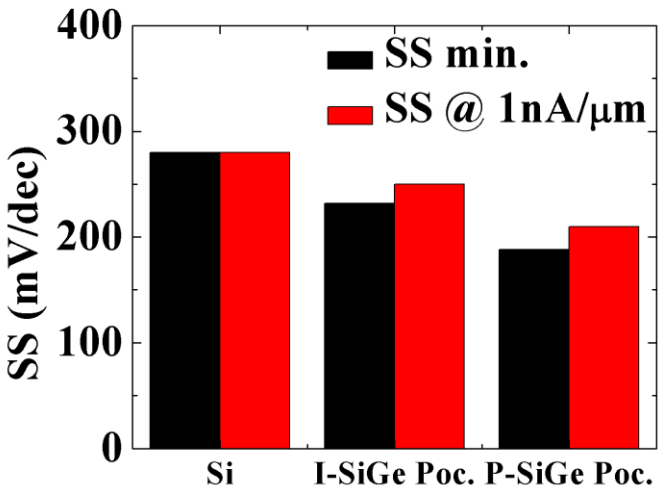
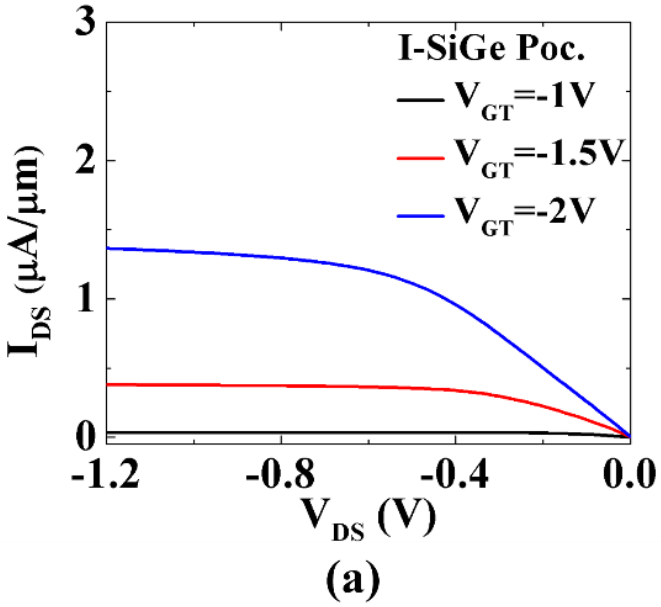


Fig. 4.16 Minimum *SS* and *SS* at 1nA/μm of all three TFETs. By incorporating the intrinsic and the counter-doped $Si_{0.8}Ge_{0.2}$ pocket, the tunneling is enhanced. Thus their switching behaviors become increasingly steeper.

4.4.2 Output Characteristics

Fig. 4.17 shows the output characteristics of the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket and the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket. Output current saturation is observed, and there is no diode-like behavior in the linear region. The diode-like behavior in the linear region [74],[75] indicates a high voltage drop across the tunnel junction due to the large tunneling resistance. Its absence confirms good carrier transport across the tunnel junction due to the reduced tunnel barrier height and the enhanced lateral electric field.



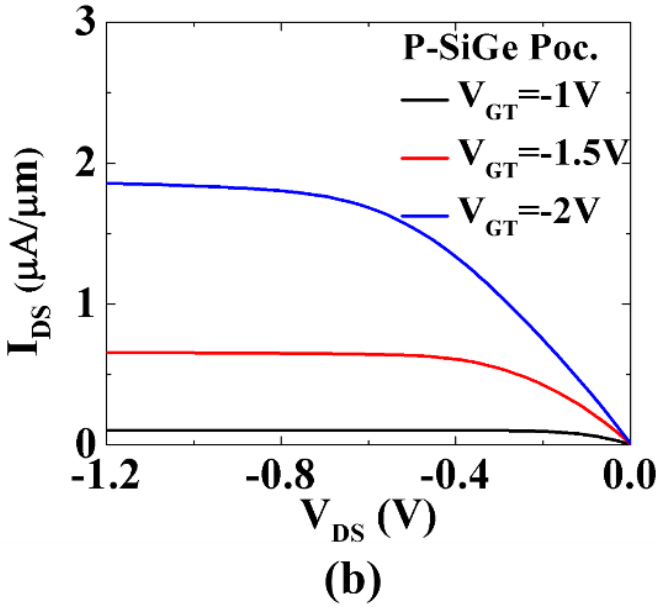


Fig. 4.17 The output characteristics of (a) the TFET with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket and (b) the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket.

4.5 TFETs Performance Analysis

Incorporating a p-type $Si_{0.8}Ge_{0.2}$ pocket into the device improves the device performance in terms of *SS* and I_{ON} significantly. However, the device fails to achieve sub-60mV/dec. By improving the material quality, the transfer characteristics of Si homojunction TFET show a steeper *SS* (min. *SS*~100mV/dec), a higher current drive, and a lower leakage current, as shown in Fig. 4.18, which suggests that the performance degradation is linked to the material quality. TCAD device simulation has been performed to investigate the impact of the material quality further.

The band-to-band tunneling model has been calibrated to achieve a reasonable agreement with Si homojunction TFET experiment data with the improved material quality (Fig. 4.19). The doping profile assumed in the simulation is shown in Fig. 4.20. A high phosphorus concentration is assumed at the source/channel due to dopant segregation. For Si homojunction TFET fabricated before the improvement of the material quality, a bandgap of 1.2eV is assumed. The value corresponds to the bandgap of polysilicon. The calibrated tunneling parameters have been adjusted to count for the change in the bandgap. The simulation agrees with the experimental data for I_{DS} above nA/μm (Fig. 4.21), where the band-to-band tunneling dominates the current conduction as suggested by pulsed IV measurement. Below nA/μm, the trap-assisted tunneling (TAT) takes over. Thus, a severe degradation in switching behavior is observed. The optimized p-type $Si_{0.5}Ge_{0.5}$-pocket TFET from the previous chapter has been re-benchmarked against 14nm FinFET using the new tunneling parameters, and the result is shown in Fig. 4.22

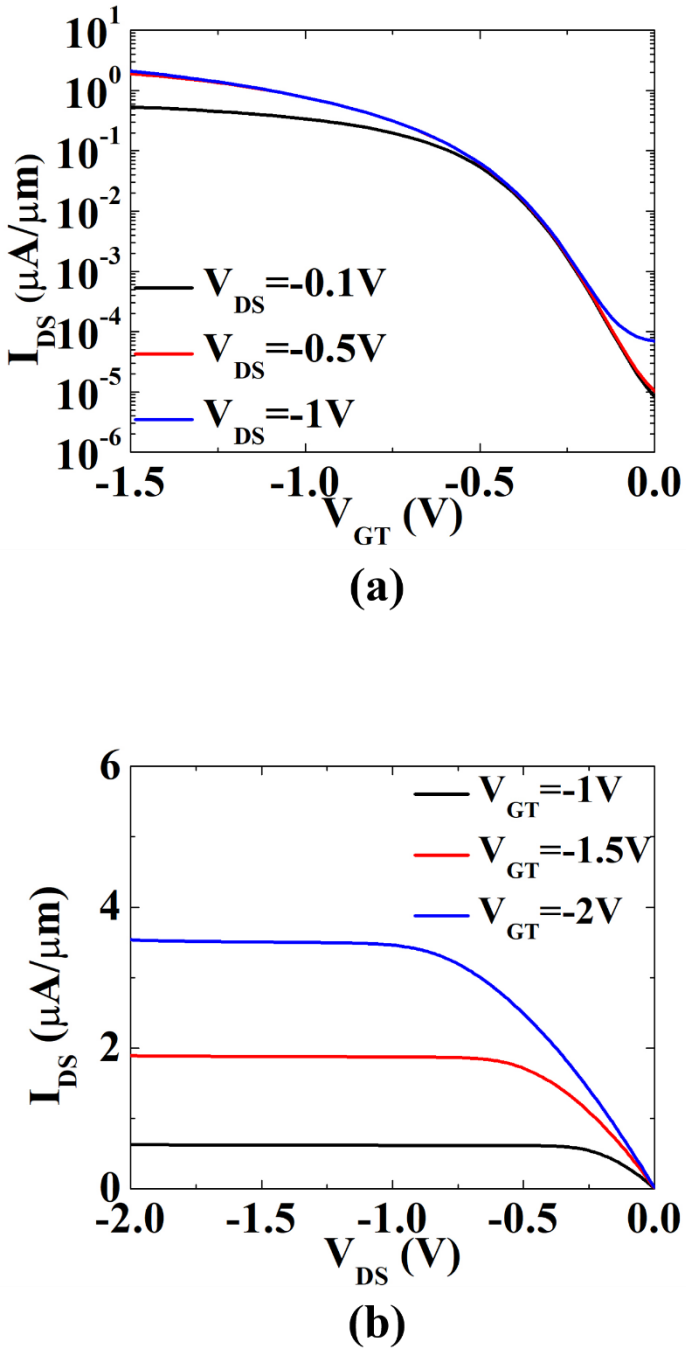


Fig. 4.18 The measured (a) transfer characteristics and (b) output characteristics of Si homojunction TFET with the improved growth condition.

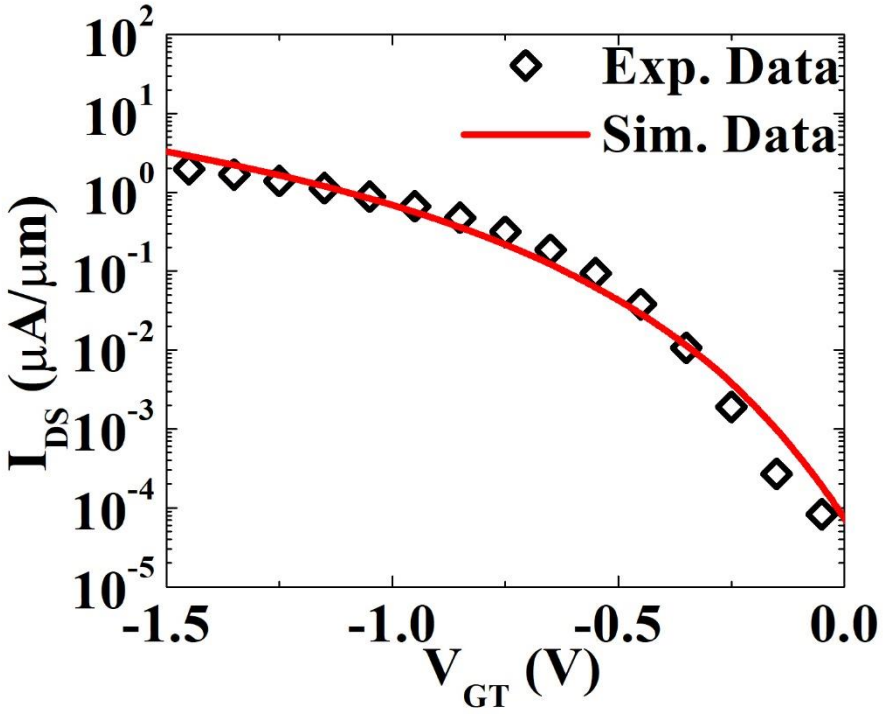


Fig. 4.19 The simulation has been calibrated to the Si homojunction TFET fabricated with an improved growth condition.

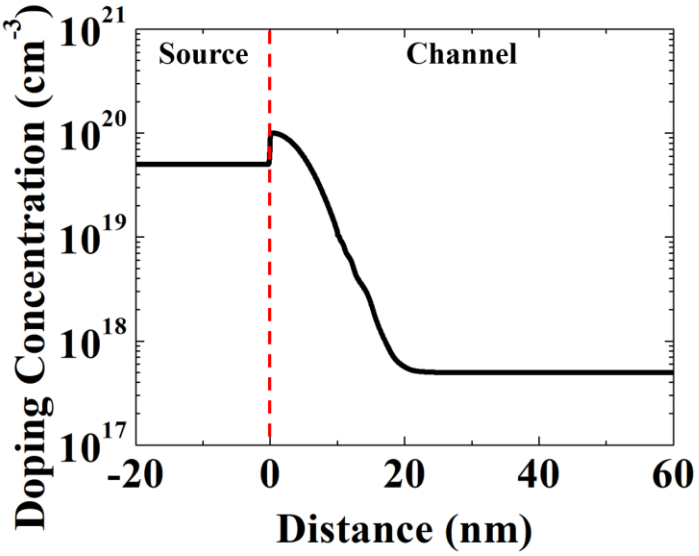


Fig. 4.20 The doping profile assumed for the simulation for Si homojunction TFET with the improved material quality. A 3nm/dec doping slope is assumed for the device with the improved material quality.

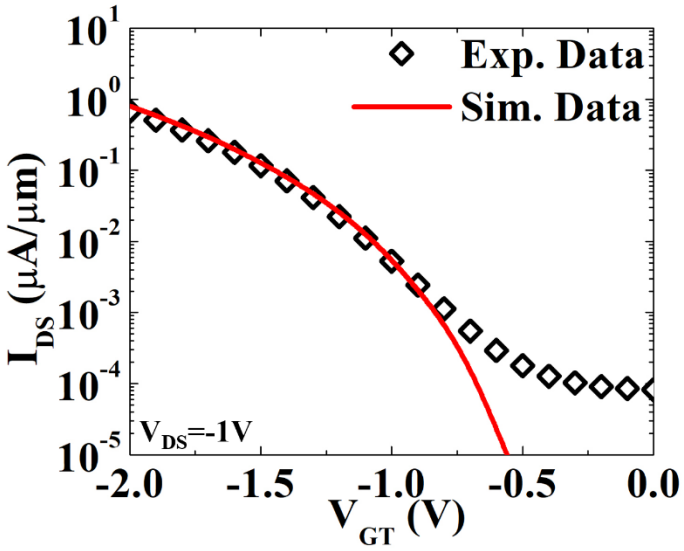


Fig. 4.21 The tunneling parameters have been adjusted to count for the bandgap shift. A good agreement has been achieved between the simulation and the experimental data for current higher than nA/μm range where the band-to-band tunneling dominates. The source doping gradient is assumed to be 10nm/dec.

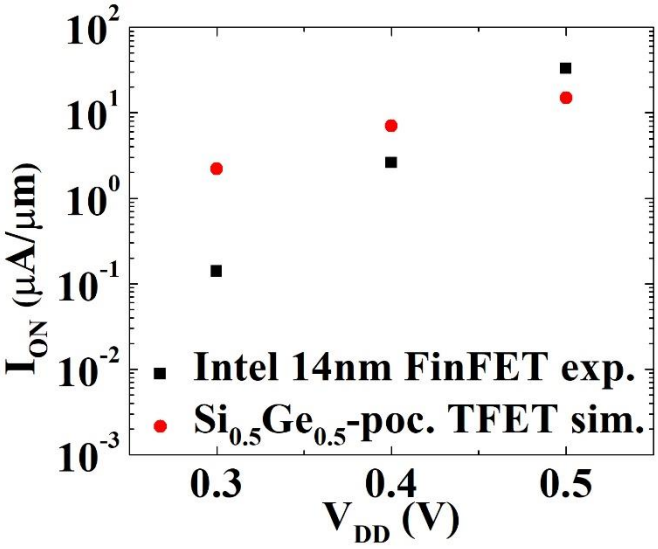


Fig. 4.22 The benchmark of the p-type $Si_{0.5}Ge_{0.5}$-pocket TFET against 14nm FinFETs with modified tunneling parameters for Si.

4.6 Summary

The Si homojunction TFETs, the TFETs with an intrinsic $Si_{0.8}Ge_{0.2}$ pocket, and the TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket have been fabricated. $Si/Si_{0.8}Ge_{0.2}$ heterostructure in the TFETs are deposited via RPCVD. A low-temperature process has been developed for fabricating the TFETs to preserve the as-deposited doping/composition profile. All three types of TFETs have been characterized and compared. Significant improvements in I_{ON} and *SS* have been observed for the TFETs with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket due to the reduced tunnel barrier height and the enhanced lateral electric field at the tunnel junction. The absence of the diode-like behavior in the output characteristics is an indicator of the good carrier transport across the tunnel junction. The impact of the material quality on the device performance has been discussed and analyzed.

Chapter 5

Conclusions

5.1 Summary

TFETs have been investigated extensively as one of the most promising steep slope devices. In this work, the experiment results of state-of-the-art TFETs have been examined thoroughly. Their successes and limitations have been identified to aid the design of new TFET structures. Although none of them has matched the performance of conventional MOSFETs, new device concepts that encompass the strong suits of previous TFETs have the potential to replace conventional CMOS for low power logic applications.

SiGe-pocket TFET is presented as a promising solution with VLSI-compatibility. Thanks to the reduction in the bandgap of strained SiGe, both tunneling barrier height and tunneling distance become smaller, which in turn promotes higher tunneling current. The optimization process of n-type Ge-pocket TFET for 14nm node has been discussed in detail with the aid of TCAD. The design is also applicable to p-type TFET. Vertical p-type $Si_{0.8}Ge_{0.2}$-pocket TFETs have been fabricated to demonstrate the device concept. Epitaxial growth of the tunneling junction is demonstrated by low-temperature RPCVD. Reduced SiGe growth temperature (650C°) suppresses the surface hydrogen desorption, which enables the formation of a sharp junction by minimizing Ge migration.

A detailed process flow of vertical p-type $Si_{0.8}Ge_{0.2}$-pocket TFET has been developed. The growth of SiGe heterojunction with RPCVD has been discussed in detail. Compared with MBE, RPCVD is a growth technique with higher throughput, which makes it more suitable for the manufacturing setting. Based on the experiment result, the enhancement in TFET performance due

to the insertion of a counter-doped $Si_{0.8}Ge_{0.2}$ pocket is significant. Compared with the fabricated Si-based homojunction TFET, approximately 160% improvement in I_{ON} and 30% reduction in minimum *SS* are observed in the TFET with a counter-doped $Si_{0.8}Ge_{0.2}$ pocket without the penalty of increasing leakage current. In addition, a current saturation region is observed in the output characteristics, which translates to suppress drain-to-channel coupling. The potential of SiGe-pocket TFET for low power logic application has been experimentally demonstrated.

Aside from the promising experimental results from SiGe-pocket TFET, there is still a gap between theoretical prediction and measured data. The impact of the material quality on the device performance has been investigated with TCAD. With the improved material quality, the simulation suggests that double gate SiGe-pocket TFET with a counter-doped pocket has the potential to outperform FinFET technology for 14nm technology node and beyond in terms of I_{ON}. And the performance disparity grows as V_{DD} further reduces.

5.2 Suggestions for Future Research

SiGe-pocket TFET has been demonstrated in this work. The improvements in I_{ON} and *SS* are observed compared with Si TFET. However, the experimental result still falls short of the theoretical projection. Further advancements in the processing are needed for the device to be competitive against state-of-the-art CMOS technology for low power logic applications. Potential solutions include:

- Improving the film quality: The tunneling process is sensitive to the quality of the deposited film. By improving Si quality, a significant improvement in the transfer characteristics has been observed in Si homojunction TFET: the trap-assisted tunneling in the subthreshold region

is suppressed, and current drive increases. Thus, it is critical to improving the film quality by reducing the contamination in the chamber.

- Increasing Ge composition: Both simulations and experiments have proven that increasing the Ge composition of SiGe is an effective approach to boost the performance of SiGe-based TFETs. The smaller bandgap results in the reduction in both the tunneling barrier height and the distance. Therefore, it can boost the tunneling probability. However, due to a 4.2% lattice mismatch between Si and Ge, the epitaxial growth of SiGe with high Ge composition (possibly pure Ge) is very challenging. The deposition process needs to be further optimized for metastable SiGe growth.
- Reducing growth temperature: High-quality as-deposited $Si_{0.5}Ge_{0.5}$ layer has been pseudomorphically grown on Si substrate in this study. But due to the elevated growth temperature of the subsequent layer, the metastable $Si_{0.5}Ge_{0.5}$ relaxes and leads to poor material quality. By adopting the new precursors such as Si_2H_6 and Si_3H_8, the growth temperature of Si can be reduced to sub-600°C. This helps to preserve the strain of the pseudomorphic SiGe layer and to suppress the dopant surface segregation.
- Enhancing electrostatic control: It has been experimentally demonstrated that good electrostatic control is essential for achieving steep *SS* and high I_{ON}. By improving the gate/channel coupling, the gate terminal modulates the channel potential more effectively, which results in steep switching characteristics and high current drive. For TFET with a thin-body multi-gate configuration, tunneling occurs across the body, which leads to an increased tunneling area. It is similar to the volume inversion in FinFET. To improve the electrostatic control of the SiGe-pocket TFET, it is beneficial to utilize the multi-gate structure with a high-k/metal gate.

- High doping concentration: In this experiment, the in-situ source doping concentration is ~$5\times10^{19}cm^{-3}$ based on the extraction from four-point measurements and TLM measurements. The low doping concentration in the source region results in a low electric field across the tunneling source/channel junction, which severely reduces the tunneling current. The low doping concentration is due to the incomplete ionization of dopant as well as the dopant surface segregation. The impact of the inactivated dopants in the source region is twofold: on the one hand, they act as defect centers and facilitate undesirable trap-assisted tunneling; on the other hand, the inactivated dopants become scattering centers and reduce the carrier mobility in the source. The former degrades the steep switch characteristics at the low current regime, and the later reduces the current drive due to higher parasitic source resistance. Both are detrimental to the TFET performance. Therefore, dopant activation with a low-thermal budget is essential because it minimizes the dopant diffusion and prevents the relaxation of the pseudomorphically grown SiGe layer. Pulsed laser annealing [x] and microwave annealing [x] are the potential solutions to this issue.
- Gas line purge and chamber etching/coating: seasoning the RPCVD chamber before each deposition step is critical for achieving a steep doping gradient. Increasing the dopant gas line purge time before deposition helps to flush out the residual dopant gas from the previous deposition. In addition, incorporating the etching/coating step helps to suppress the dopant absorption by and emission from the chamber wall.

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