Title
A LINEAR ELECTRONIC SWEEPING PULSE GENERATOR

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A LINEAR ELECTRONIC SWEEPING PULSE GENERATOR

Berkeley, California

DISCLAIMER

Research and Development

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Berkeley, California

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June 1, 1964

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ABSTRACT

An instrument is described which is useful for setting up and testing complex electronic pulse-handling systems. The instrument provides pulse up to ±10 V into a 125-ohm line at regular or random rates up to 10^6 pps. The pulse amplitude can be electronically swept through the whole amplitude range in a timewise linear fashion, with periods from 0.5 msec to 20 seconds.

Rise times from 0.05 to 1 μsec can be obtained. The pulses can either be flat-topped or have exponential tails from 5 to 100 μsec. A completely dc-coupled output is provided for reliable measurements of rate-sensitive effects in pulse amplifiers and analyzers.

The instrument can also be used as a time-to-amplitude converter for times greater than 5 μsec.

INTRODUCTION

Much time can be saved in setting up the electronic part of nuclear chemistry and physics experiments if suitable test equipment is available. Ideal test equipment would allow the simulation of experimental conditions without the use of expensive accelerator time. The tests must be fairly easy to perform, and it should be possible to quickly run through a large range of experimental conditions.

The pulse generator described in this report meets some of these requirements for tests of amplifier and pulse-height-analyzer stability and linearity, random-rate sensitivity, and pulse-shape sensitivity. In a typical experimental setup, the pulser feeds the preamplifier of a system with randomly spaced pulses having a fast rise time and a slow RC decay, to simulate the effect of particles detected by a counter. A wide range of input amplitudes is swept through repeatedly while the output amplitude distribution is stored by the same pulse-height analyzer that is to be used in the experiment. Most abnormalities in any part of the amplifying or analyzing equipment will be immediately obvious from the recorded distribution of output amplitude and from changes in the distribution as the average pulse rate is varied.

For linearity tests, a linear voltage ramp is sampled at regular intervals by triggering the start of this ramp with a "start" pulse and sampling it at a later time with a "stop" pulse.

DESCRIPTION OF INSTRUMENT

With the aid of Figs. 1 and 2, the main features of the instrument can be readily understood. A linear gate circuit samples a negative voltage supplied from

(a) an external source,
(b) a Zener-controlled voltage tapped by a helipot, or
(c) a very linear voltage-sweep generator.

The rate of sampling is determined by
an external pulse generator,
an internal variable-frequency oscillator,
a push-button, or
an internal source of randomly timed pulses.

Sampling rates greater than 100 pps are indicated on a front panel meter with an accuracy of about 10%. The output circuits are protected against short-circuit overload, and can drive any length of 125-ohm cable provided that it is properly terminated.

OUTPUT CHARACTERISTICS

Three simultaneous outputs plus a trigger are provided.
Pulse Width: 0 to 10 μsec, ac outputs (positive and negative),
0.5 to 40 μsec, dc output. (positive only)

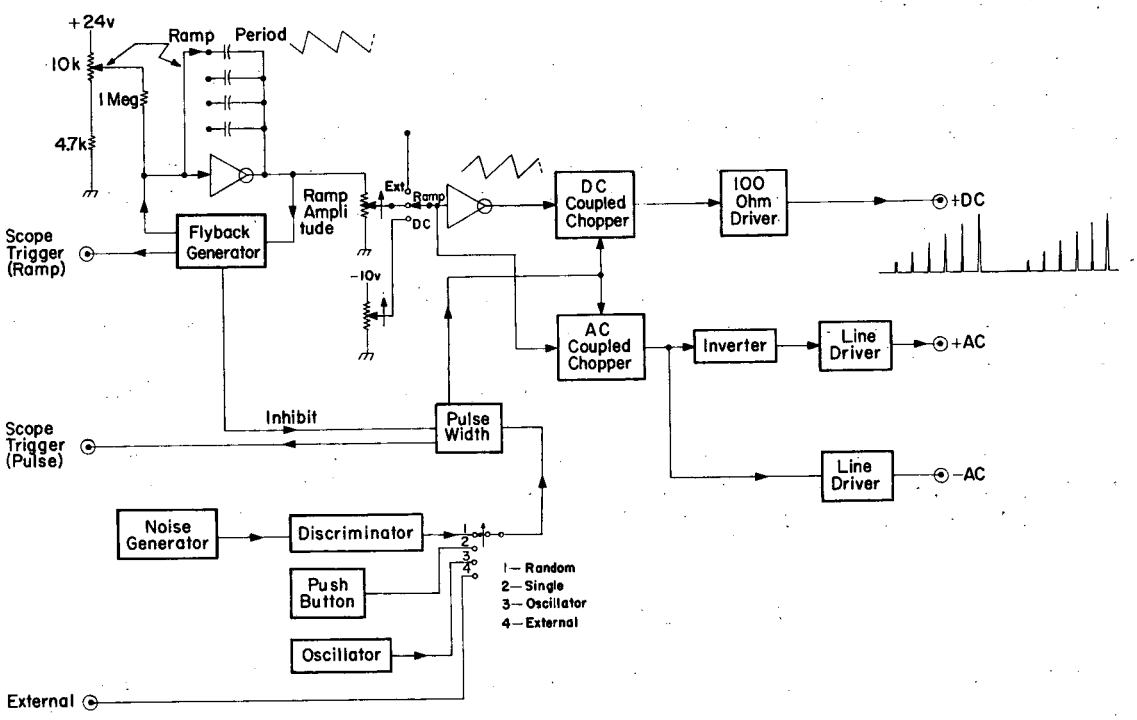

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Fig. 1. Ramp pulser block diagram.

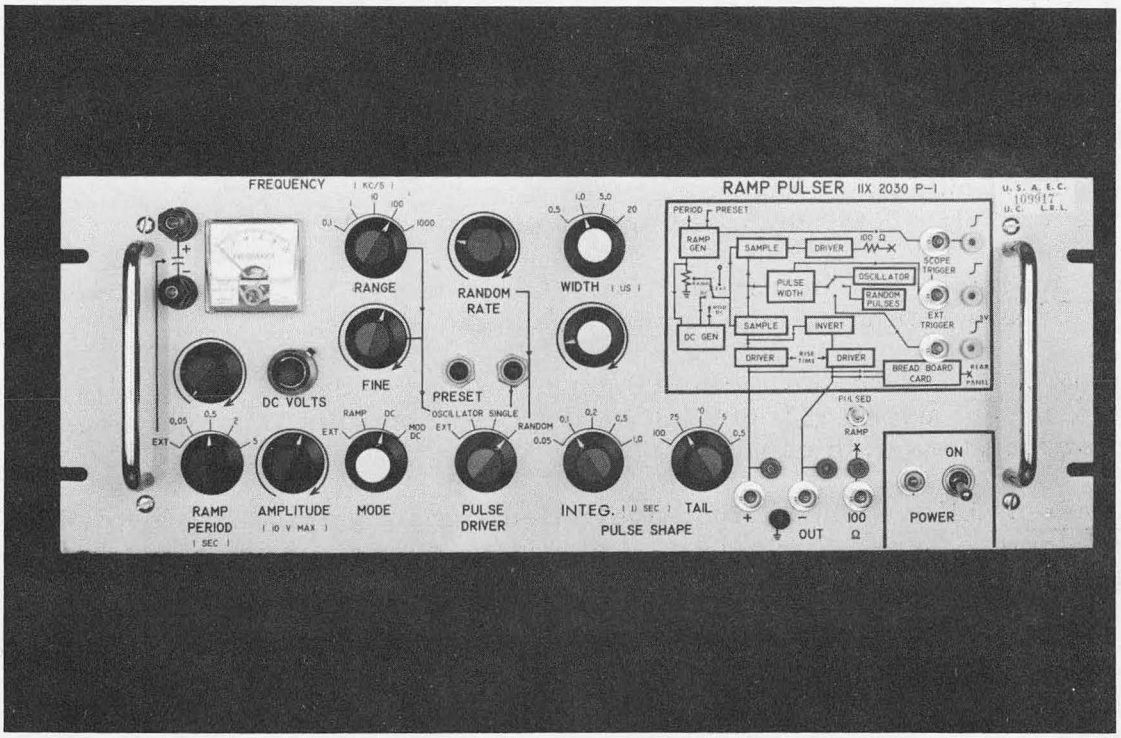

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Fig. 2. Front panel of ramp pulser.

(The use of dc coupling allows sample length to be extended indefinitely by use of an external signal.)

Pulse Rate: single (push-button) or from 10 pps to 10^6 pps; random rates can be controlled at any rate up to 8×10^5 pps.

Pulse Shape:

ac-Coupled outputs:
rise time: 0.05, 0.1, 0.2, 0.5, or 1.0 μsec;
fall time : 0.5 μsec;
tail pulse: 5, 10, 25, or 100 μsec.

dc-Coupled output:
rise and fall: 0.15, 0.25, 0.5 or 1.0 μsec.

Pulse Amplitude: Can be varied from ±0.05 V to ±10 V. Either a fixed dc voltage or a sweeping voltage can be selected.

Sweeping Voltage: Period from 500 μsec to 20 seconds. The slope is constant to ±0.1% for the upper 95% of each sweep (see Appendix A, regarding effects of dielectric storage in capacitors).

Amplitude Stability: The helipot-controlled sample voltage is provided by tapping off from a Zener-diode-regulated voltage supply. Typically, a 25°C change in temperature will produce a 15-mV zero drift in the sampling circuit (with flat-top pulses), and the Zener reference will shift as much as 10 mV. The tail pulse amplitude will show poorer stability owing to the higher impedances used. Line voltage changes of ±10% should produce no measurable effects.

The ac-coupled outputs reflect these stability figures, but considerably larger temperature effects appear on the dc-coupled output.

The amplitude of the ac-coupled outputs will show a slight rate sensitivity at duty cycles of 10% or higher, whereas the dc-coupled output is completely insensitive to rate effects.

SPECIAL FEATURES

Preset

The sweep period may be many seconds in duration. To avoid long waits before the start of a new period, a reset button initiates a new sweep cycle.

Modulated dc Supply

For stability tests with pulse-height analyzers, it is convenient to have counts fall in several channels. The amplitude of the helipot-controlled output level can be modulated by about 0.5% of full scale, with the modulation rate controlled by the ramp period.

Time-to-Pulse-Height Conversion

A rear panel switch allows a special "Time-to-Height" mode of operation to be used, where the linear sweep can be triggered by a "start" pulse. If a "stop" pulse is fed to the instrument after a time lapse (greater than 5 μsec) an output pulse is produced whose amplitude is proportional to the time lapse. Full-scale time may be selected as 0.25, 5, 50, or 500 msec. Longer or intermediate time scales may be obtained by use of an external capacitor. High duty cycles can be used, as the recovery time is only a small fraction of the time between start and stop pulses.

Breadboard Card

One card position has been left vacant in the unit. This location has connections to an inverting output driver, to the ramp voltage, to the "+" and "-" outputs, and to the power supply. The location is used by a special circuit for control of time-to-height operation, but for other applications, a special pulse shaper or generator may be built and plugged in at that card position. Output signals from circuits placed at the vacant position will reach a BNC connector on the rear panel via a linear inverting line driver.

APPLICATIONS

Often the sweeping pulser is used to feed a uniform pulse-height distribution to a pulse-height analyzer (PHA). It is of course important in interpreting the results, to take account of the variation of PHA dead time with pulse amplitude. With randomly spaced pulses, there will be fewer counts recorded at the higher PHA channel numbers. With regularly spaced pulses, the number of counts per channel will change abruptly if the pulse interval becomes shorter than the maximum dead time.

A more subtle problem arises when pulses are fed in with a slowly swept amplitude. Instead of a completely flat distribution of counts per channel, some statistical variation is observed. This can be understood, since most analyzers do not have completely sharp channel edges, so that for at least part of the time, random effects such as noise determine which of two adjacent channels receives counts. Even for absolutely sharp channel edges, there would be an uncertainty of one count per channel for each time the amplitude sweep crosses the channel edges, since the sweep does not cross each channel in an integral number of pulse periods. Statistical fluctuations can be reduced but not eliminated by using a sweep so slow that hundreds of counts are stored in each channel during each sweep.

Many pulse-height analyzers tend to favor certain channels; one speaks of an "odd-even" effect when, for example, more counts go into even-numbered than odd-numbered channels owing to faults in the address-register scaler. The sweeping pulser can produce a distribution that looks superficially similar to this fault, owing only to an unfortunate choice of test parameters. The reason is that some power-supply hum exists in any PHA, and a simple ratio may exist between the rate of crossing channels and the power hum period. Then nonrandom preference can be given to every other channel and an apparent odd-even effect is observed.

To see the magnitude of the effect consider the following example: Suppose in a 200-channel analyzer using 10 V input, there exists a peak-to-peak 120-cps hum voltage of 1 millivolt. This corresponds to 2% of one channel. Suppose that the sweep crosses one channel in one-half of a hum period (4.15 msec). Then the hum can increase the time to cross one channel by 2% and decrease the time in the adjacent channel by the same amount. This will cause a similar difference in the number of counts recorded by adjacent channels during that sweep. The problem can best be avoided by using a sweep rate so slow that many hum cycles occur while each channel is crossed. Successive sweeps also tend to average out the effect, so long as the sweep generator is not synchronized to power-line hum.

APPENDICES

INTRODUCTION

The following circuit diagrams and descriptions will be of value to those interested in using the instrument in special applications or in making modifications to it. Detailed printed card layouts, component lists, and wiring diagrams are available in addition to the schematics provided here.

Interconnections between cards of the pulser are given in Fig. 3.

The numbering system used on these circuits can be understood by means of an example: In 11X1942 S-1, 11X194 is the basic number of the card. The 2 refers to the size of the drawing, S-1 means schematic 1. In addition, a "Print List," 11X191 P-1, exists that lists all other drawings, such as the block diagram, 11X194_ B-1; the component list 11X194_ C-1; and so on.

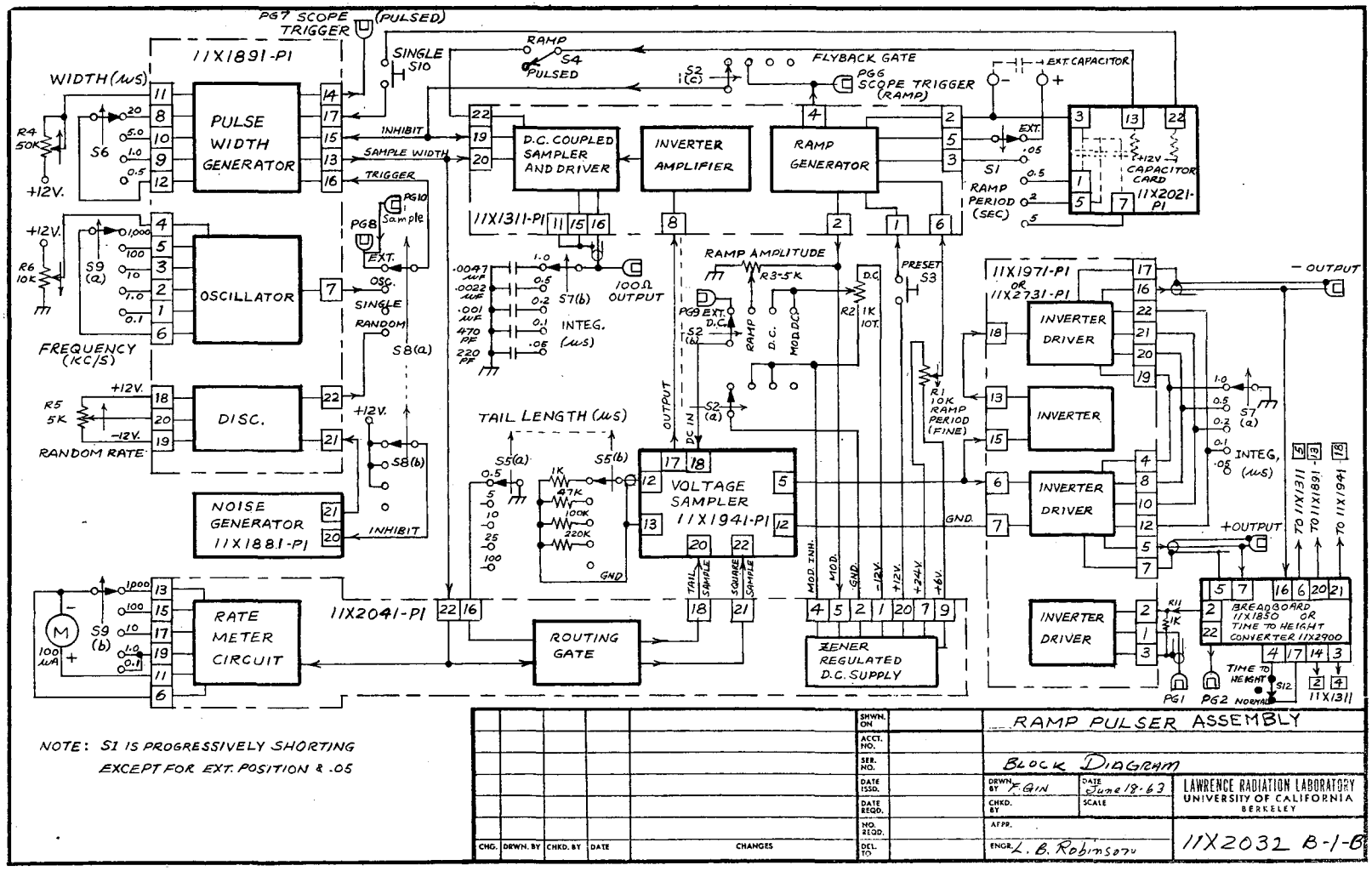

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Fig. 3. Ramp pulser assembly (11X2032 B-1B).

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A. DIELECTRIC STORAGE IN CAPACITORS

The effect of dielectric storage in capacitors places some limitations upon the sweep rates that can be used without sacrifice of linearity. Dielectric storage is small in the Mylar capacitors used, but can have an appreciable effect on the slope of the ramp at its beginning. Polystyrene capacitors show only 1/10 as much dielectric storage, but have not been used in the instrument because of their large size. For most applications, the results obtained using Mylar will be more than adequate, and in special critical applications, an external polystyrene capacitor can be connected to the binding posts provided. Tantalum electrolytic capacitors show much more dielectric storage than Mylar, but may be useful where extremely long ramp periods are desired.

Measurements of the time dependence of the dielectric relaxation current have been made. The current decays rapidly, with a time constant that increases with time. The decay is such that linearity of only the first part of the ramp is affected.

Assuming that the flyback period is 1% of the ramp period, the maximum effects on the slope during various parts of the ramp are given in the table below.

Ramp section	First 0–1%	First 1–5%	5–20%	Above 20%
Mylar	10%	5%	1%	0.2%
Polystyrene	1%	0.3%	—	—

The values given are outside limits, although a 2% change in slope has actually been observed over the bottom 5% of the range when Mylar capacitors were replaced by polystyrene. The effect has been practically eliminated in recent models of the ramp pulse generator by making the flyback time 10% of the ramp rise time.

B. CIRCUIT DESCRIPTIONS

1. Sampled Ramp Generator Card

11X1310 D-2

General

A Nuclear Instrumentation 4×8-in. 28-pin etched card produces both positive-going and negative-going ramps, 10 V in amplitude, with slope constant over most of the voltage range to better than 0.1%, if a polystyrene capacitor is used.

Ramp periods from 5 msec to 50 sec are easily obtained by selection of integrating capacitor and charging current.

The ramp can be sampled by a linear gate pulse of width, 0.3 μsec or longer.

Input Requirements

Voltage	Current (mA)
+24	80
+12	15
-12	6
-24	25

Note: The current requirement for +24 V assumes an output signal current of 50 mA. As output loading is reduced, power requirements drop correspondingly.

"Sample" instruction, Pin 20, 21, or 22.

+4 V to +12 V, any width greater than 0.3 μsec.

Integrating current.

Five to 500 μA supplied to Pin 5 determines the rate of rise of the ramp. The current is defined by a single resistor and voltage supply, as the base of Q5 remains steady at +0.8 V. Normally the current is determined by a fixed voltage at Pin 6.

Ramp rise time.

The ramp rise time is directly determined by the capacitors between Pins 2 and 5 in parallel with C5. Any value of capacitor may be used, care being taken that the capacitance is not a function of voltage. Polystyrene capacitors are preferable, Mylar capacitors are suitable; electrolytics give poor linearity. (See section on dielectric absorption, page 9.)

Preset.

The ramp voltage will reset to its zero level following the end of a +4 V signal to Pin 1. (This signal must last long enough--about 10% of the ramp period--to charge the ramp capacitor to its peak voltage.)

Output Signals

Negative ramp, Pin 2.

Voltage falls linearly from +0.1 to -14 V. The period is determined by the integrating capacitor and the current selected. The voltage then returns to +0.1 V as approximately 150 μA of recharge current is switched into the integrating capacitor.

Ramp sample, Pins 20, 21, and 22.

The negative ramp is inverted and fed out from the driver via Pin 16 during the length of a sample instruction pulse. (Connect Pins 8 and 2.)

Rise time.

By grounding Pin 11, 12, 13, or 14, the sampled pulse rise time may be made 0.1, 0.2, 0.5, or 1.0 μsec. The edge can also be controlled by an external capacitor from Pin 16 to ground.

Inhibit, Pin 4.

A positive pulse is generated during the ramp recharge or flyback time. If this signal is connected to the inhibit input (Pin 19) no sample outputs can occur during the flyback cycle.

Circuit Details

The block diagram of the circuit is shown by Fig. 4 and a schematic is given in Fig. 5. An operational amplifier (Q5 to Q9) with capacitor C5 acts as a linear integrating network to produce a negative-going linear ramp when a constant current is fed to the amplifier input. (Diode CR1 is normally nonconducting.) The Schmitt trigger circuit Q3 and Q4 triggers when the ramp voltage falls to about -14 V, causing the voltage of the collector of Q4 to drop and CR1 to conduct, thus recharging the integrator capacitor and causing the ramp voltage to rise towards zero volts, where the Schmitt circuit retriggers, allowing the ramp voltage to again fall in a linear fashion.

The circuitry is standard and need not be described in detail. Capacitor C4 is used to eliminate possible synchronizing of the start of the ramp with the sampling waveform (see below). Capacitor C3 and resistor R11 reduce the gain of the amplifier at high frequency to prevent possible oscillation.

Linearity

In operation, as the ramp voltage goes from 0 to -14 V the voltage at the base of Q5 does not change by more than a millivolt. A 1-megohm resistor is used to produce the charging current, so 1 mV will cause a variation in charging current of 1 nA. The base and emitter of Q6 move by less than 10 mV. This means that the emitter current of Q6 changes by less than 10 μA, and thus the base current of Q6 and collector current of Q5 change by less than 0.5 μA, so that the base current into Q5 should be constant to within 12.5×10^{-9} A. (This is assuming the manufacturer's guaranteed current gain of 40 for the 2N929 transistor at $I_C = 10$ μA and 20 for the 2N706.) Thus the charging current into the integrating capacitor does not change by more than 13.5 nA as the ramp output voltage changes, and so the slope of the ramp is constant to 0.1% or less, provided C5 is constant and the charging current is larger than 13.5 μA. Since the base of Q5 requires up to 2.5 μA, Pin 6 should be held above 17 V to guarantee 0.1% linearity.

When the ramp generator is used in the pulse generator, the ramp voltage is fed to the inverting amplifier, and thence to the output driver circuit. The switch transistor Q17 normally holds the output level within 100 mV of ground, and a "sample" instruction to Q16 cuts off Q17, allowing the ramp voltage to feed the driver for the duration of the sample instruction. The gain of these circuits is believed to be constant over the voltage range to within 0.1% for the short period involved in one sweep, so that the amplitude of the sample pulse increases at a rate that is constant within 0.1%.

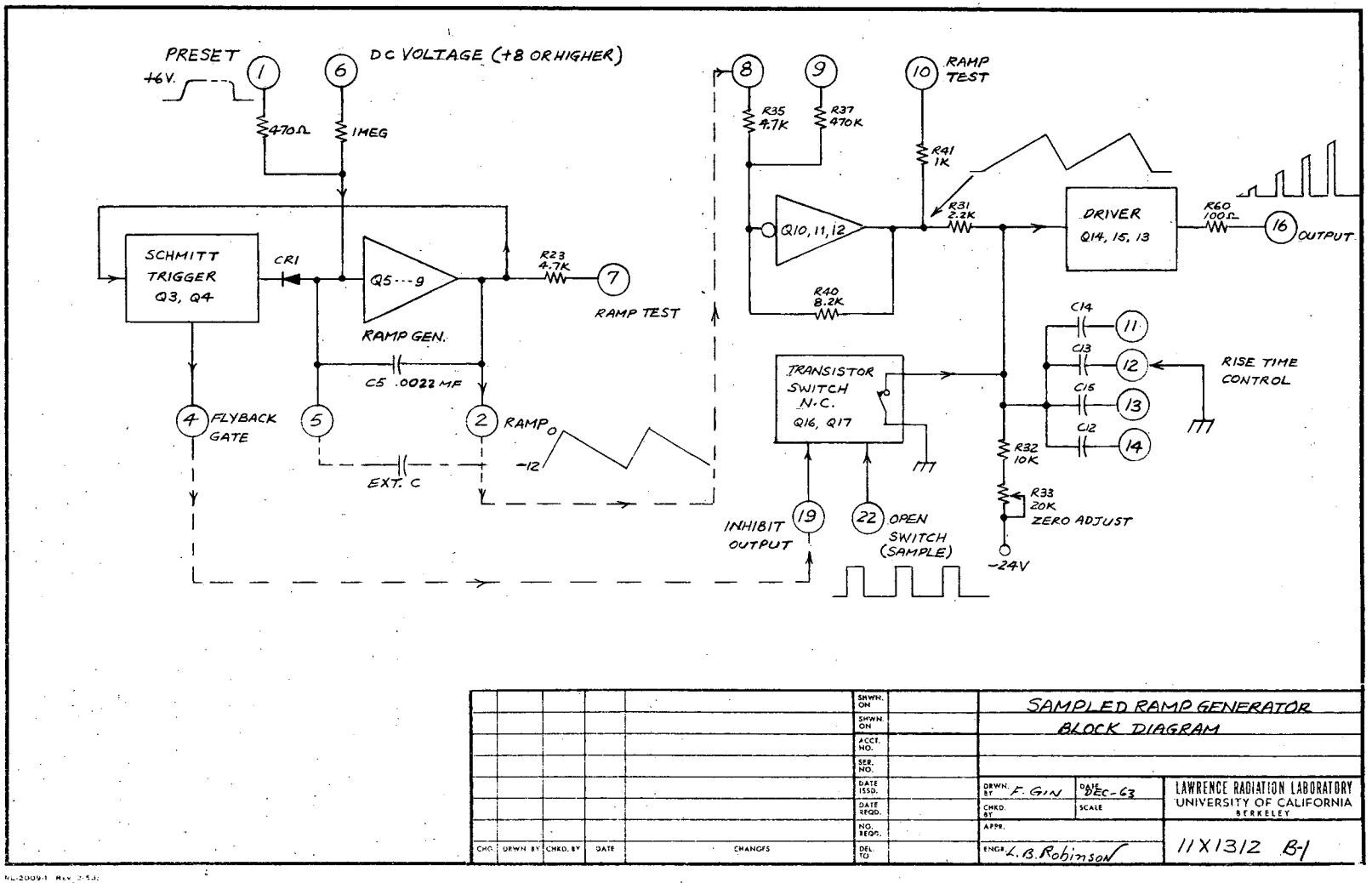

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Fig. 4. Sampled ramp generator block diagram (11X1312 B-1).

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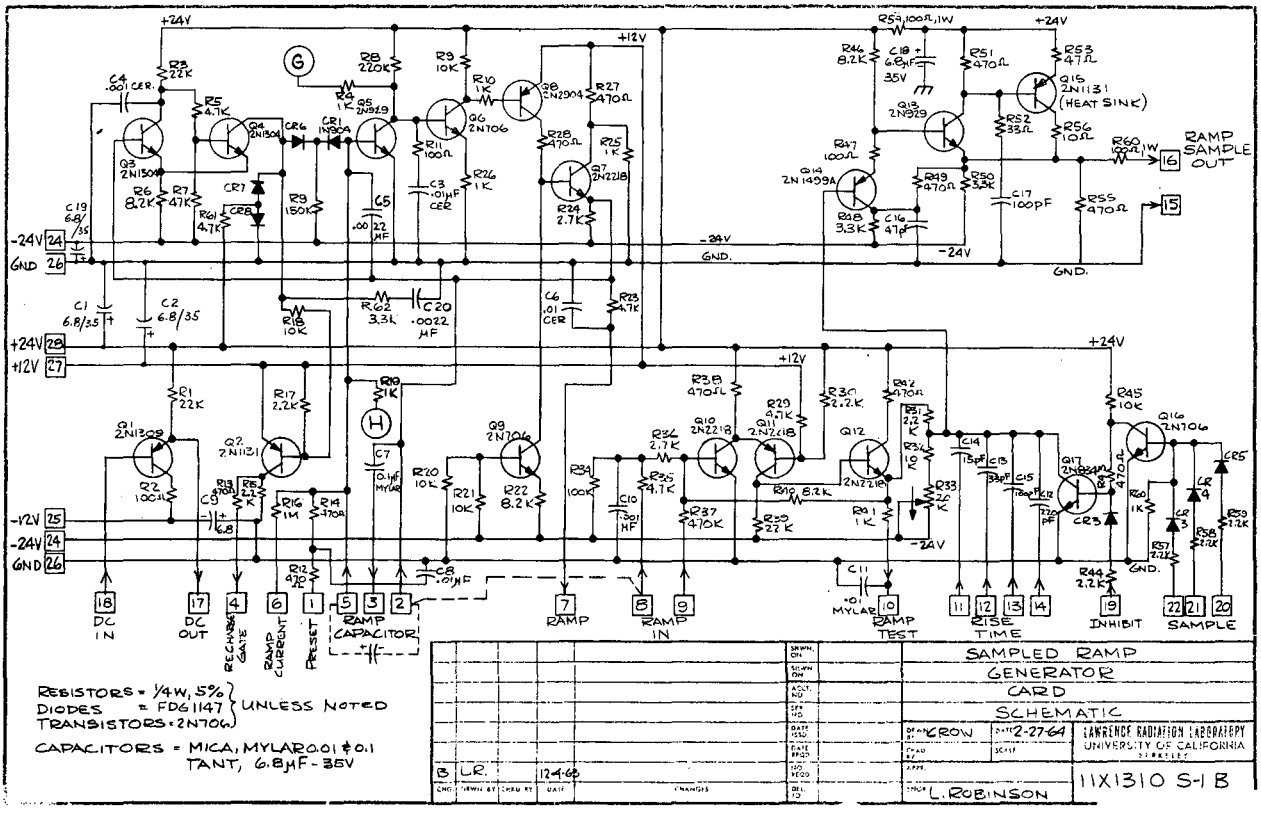

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Fig. 5. Sampled ramp generator card schematic (11X1310 S-1B).

The linearity of the output circuit Q10, Q11, Q12, Q13, Q14, and Q15 has been checked by connecting a voltage divider between Pins 16 and 8. It is possible to choose the midpoint of the divider so that it remains within 2 mV of ground for a 10-V ramp. Since input and output voltage levels are similar, this indicates that the output voltage does not deviate by more than ±4 mV from the ideal straight-line output that would be obtained if the output circuit gain were precisely constant.

2. One-Shot Module

11X1731 D-1

General

This module is a modified version of the "F-1" module described by J. H. McQuaid in LRL Engineering Note EE-862, August 1962. A standard printed wiring layout of the module has been used on several plug-in cards. The circuit is particularly useful for high duty cycles, as it recovers fully in 5 to 10% of its "on" time.

Input Requirements

Trigger signal.

A positive signal at Si must rise to 1.7 V and supply 0.5 mA over a 0.1-μsec interval for reliable triggering. It must fall and remain below +1 V before the end of the pulse period.

Marginal test.

The point M is normally held near ground potential. Variation of the marginal test voltage between ±5 V will affect the pulse width, but should not prevent operation of the circuit if components are within specifications.

Output Signals

Complementary outputs are produced at R0 and S0. The output at S0 is normally at about -0.5 V and rises to +4 V or above during the triggered period. It can supply 20 mA at +4 V or 1 mA at +10 V. The R0 output falls to -0.5 V during the triggered period. Rise times are less than 100 nsec.

Circuit Description

(See Fig. 6.)

This circuit is similar enough to the "F-1 module" to require little description. Capacitor Cd and resistor Rd determine the length of the triggered period. Resistor RS must be at least 20% smaller than Rd, so that the negative-going signal to the base of Q5 will be followed by the emitter of Q5 during triggering. Values of Rd between 4.7 K and 27 K can be safely used, and values of Cd as low as 47 pF give reliable operation.

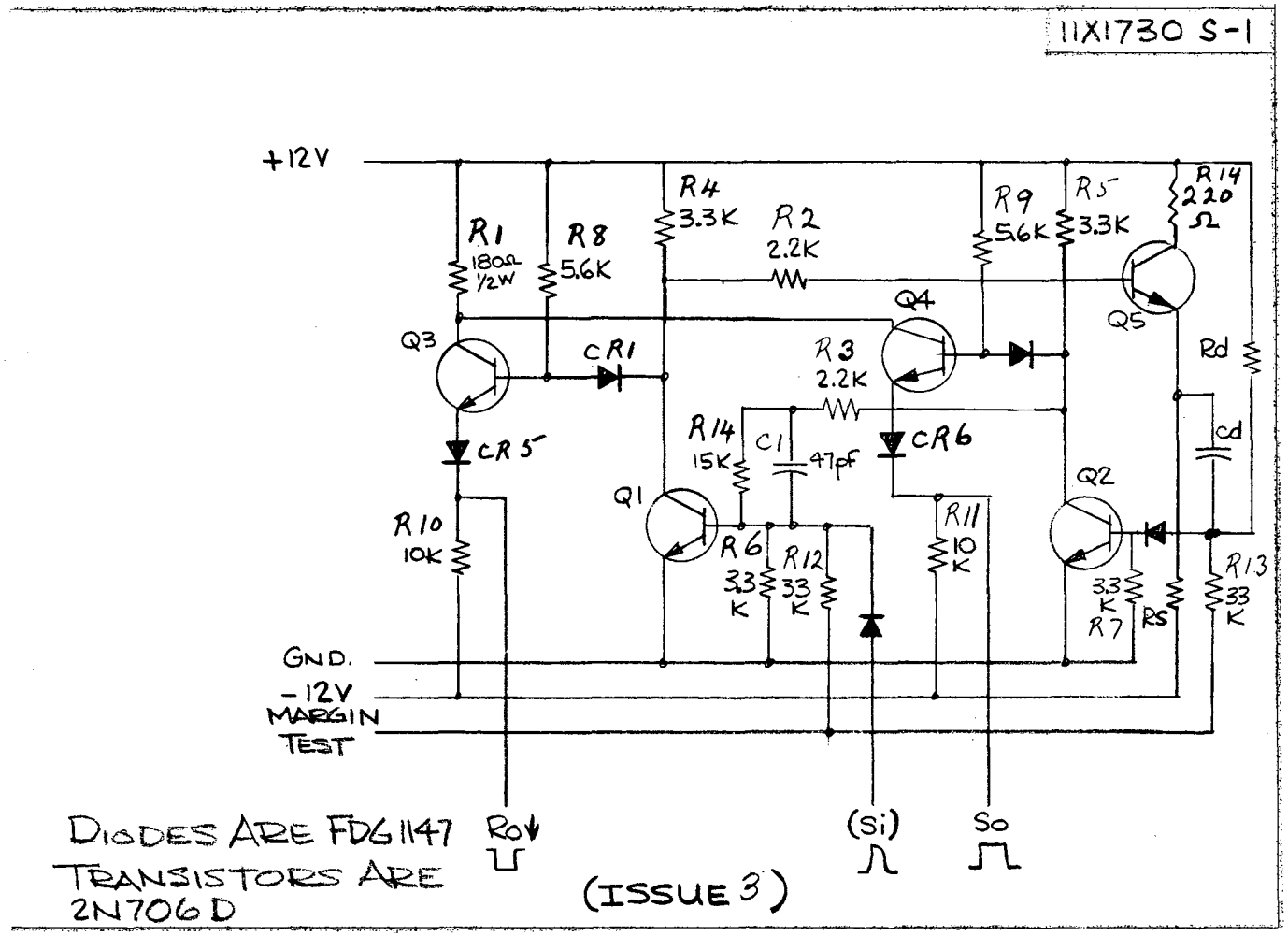

Fig. 6. One-shot module (fast recovery) schematic (11X1730 S-1).

3. Bistable Module

11X1750

General

(See Fig. 7.)

This circuit was designed as a standard building block for low-frequency circuitry (below 1 Mc/s). Detailed characteristics are given in LRL Engineering Note EE-862 by J. H. McQuaid.

The outputs of this circuit are completely isolated and protected. Either one can be shorted to ground or can drive high-capacity loads without affecting the state of the flip-flop. It drives at least 20-mA loads with +4 V signals. Output rise time is less than 0.1 μsec. Input signals below 1.2 V do not affect the flip-flop and for reliable triggering, a 0.5-μsec pulse should be able to supply 1 mA at a +2 V level.

4. Noise Generator Card (for Randon Pulse Generator)

11X1881 D-1

General

This 4×8-in. 28-pin etched card produces about 2 V rms of rf noise with frequency components up to several megacycles. It is used in conjunction with a discriminator circuit on another card (11X1891) to produce randomly spaced pulses at a controlled rate.

Input Requirements

Inhibit, Pin 20: 0 to allow output,
+4 V to inhibit output.

Output Signal

A noise spectrum with a high-frequency limit below 5 Mc/s is produced at Pin 21 as long as Pin 20 is disconnected or held below +1 V. It is important that the circuit card be shielded by a grounded box, otherwise the circuit can act as an amplifier for any nearby rf signal, destroying most of the desired random characteristics and possibly introducing low-frequency modulation.

The distribution of intervals (T) between pulses from the external discriminator has been measured. Using the logarithmic display of a pulse-height analyzer operated in the fixed dead-time mode, one finds that the distribution appears to follow the expected $N_T \propto e^{-NT}$ distribution, where N is proportional to the average output rate. At rates of more than a few tens of kc/sec, the finite dead time (≈ 0.5 μsec) introduces nonrandom effects.

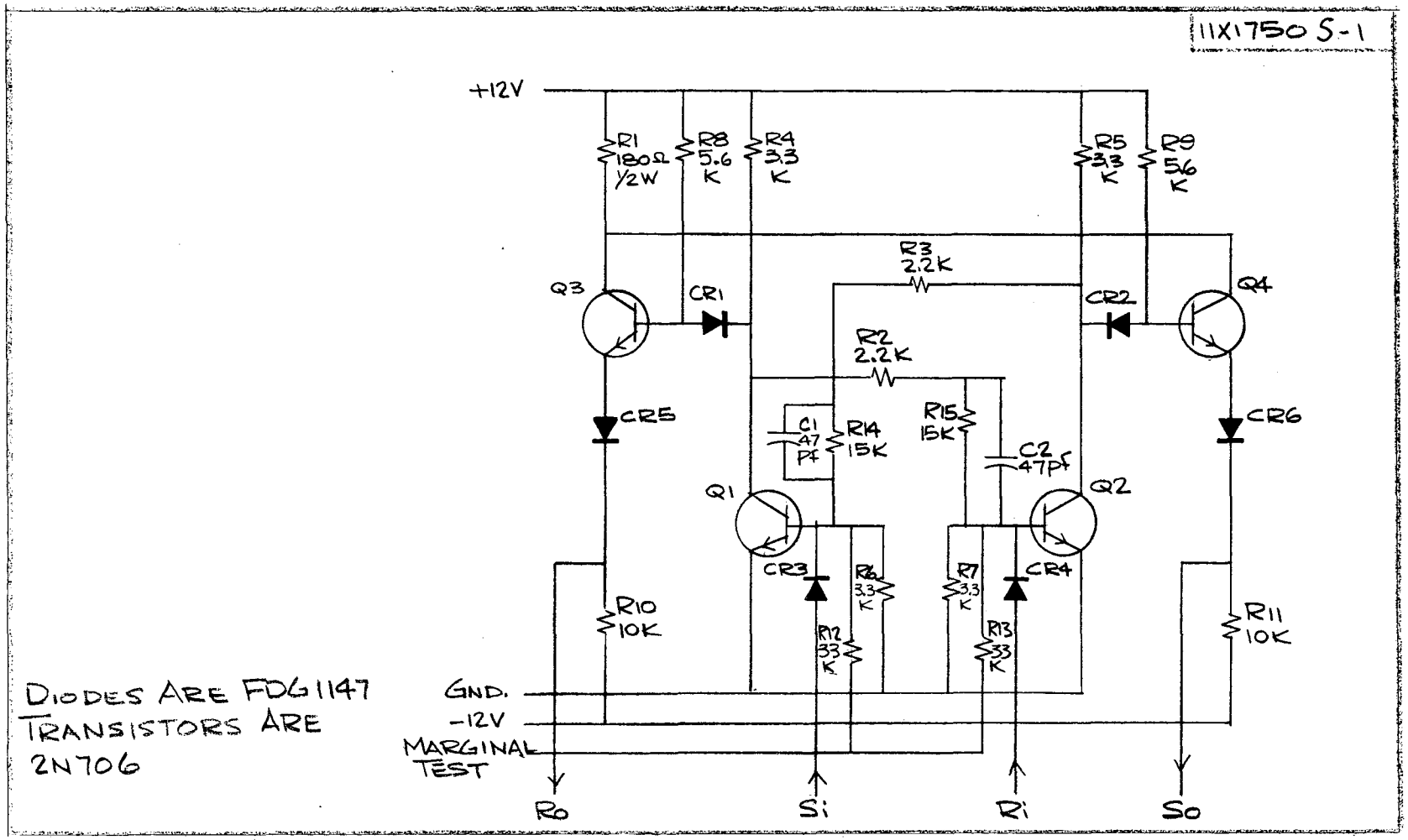

Fig. 7. Bi-stable module (2 Mc/s) schematic (11X1750 S-1).

Circuit Description

(See Fig. 8.)

The noise generator merely amplifies the noise produced in a planar silicon transistor operated at about 1 mA collector current. The frequency spectrum is limited on the low side by the coupling time constants of about 1 μsec. The time distribution of the random output from the external discriminator is of course determined by the time distribution of noise pulses above the discriminator level. This is not greatly affected by the frequency response of the noise generator so long as the rates are below about 100 kc/sec.

No indication of low-frequency modulation has been observed in the random output from the external discriminator.

5. Pulse Generator Card

11X1891 D-1

General

This 4×8-in 28-pin etched card contains three independent multivibrator-type modules: an oscillator with provision for continuous frequency variation, and two monostable circuits, one to provide gate pulses of varying width and one triggered by the noise generator (11X1881) to provide pulses at random intervals. Separate descriptions of the modules are provided.

Input Requirements

Oscillator-frequency control.

Pin 6 is either disconnected or shorted to Pin 5, 3, 2, or 1 for oscillator frequency ranges of 10^6, 10^5, 10^4, 10^3, or 10^2 pps. Pin 4 provides continuous frequency control with maximum frequency when grounded, with a reduction by a factor of 12 when Pin 4 is at +12 V.

Pulse width control.

Pin 12 is left unconnected or tied to Pin 9, 10, or 8 for a pulse width of the order of 0.5, 2, 5, or 20 μsec. Fine control is provided by adjusting the resistance between Pin 11 and +12 V. Maximum width occurs with 50 kΩ in series; and minimum width with Pin 11 shorted to +12 V.

Inhibit.

When the pulse-width circuit is to be triggered, Pin 15 is held below +0.2 V. To inhibit the circuit, Pin 15 must be at +4 V or above.

Trigger.

The one-shot circuit can be manually triggered at low rates by connecting Pin 17 to +12 V via 1 kΩ with a mechanical contact.

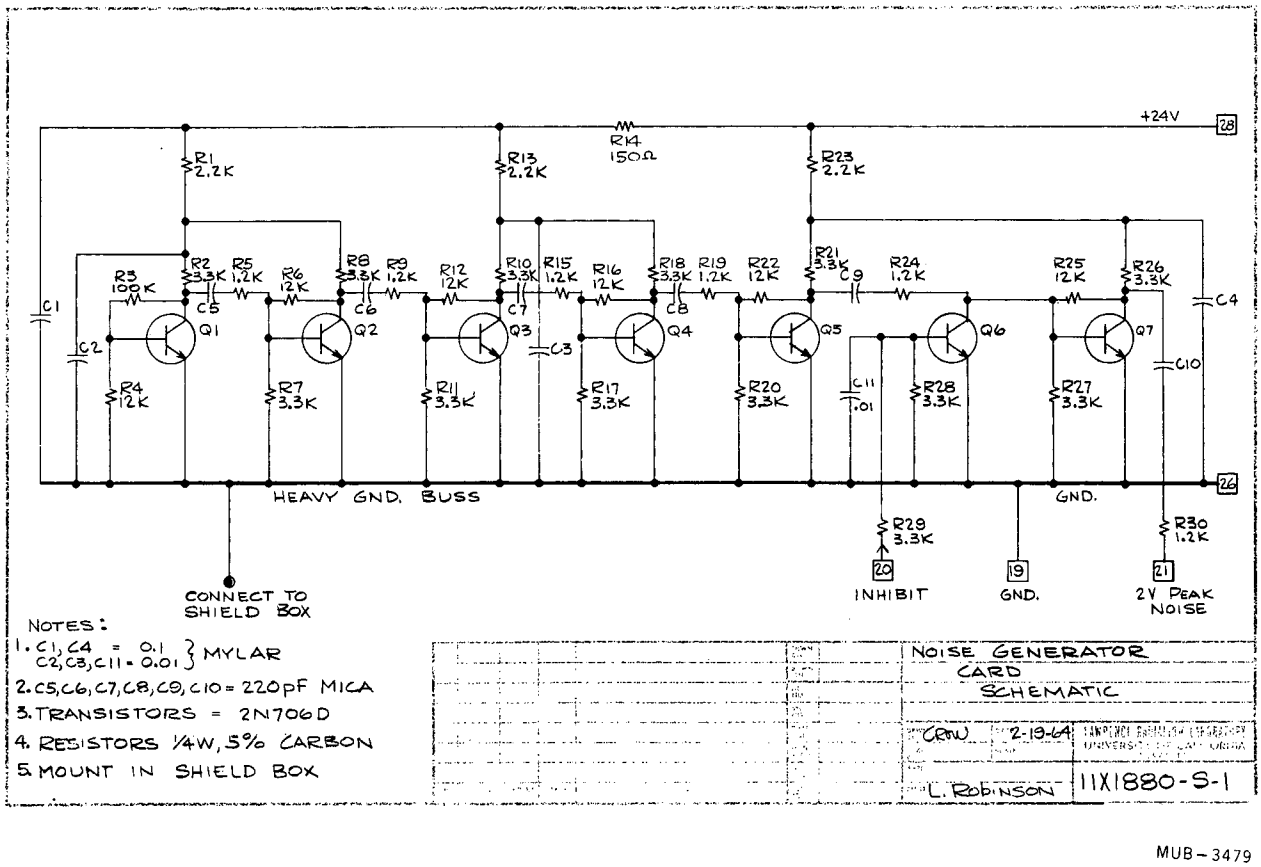

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Fig. 8. Noise generator card schematic (11X1880 S-1).

Electronic trigger signals of +4 V or larger may be fed in via Pin 16. A rise time of less than 0.2 μsec should be used.

Random-rate discriminator bias.

When 1 or 2 V of noise is fed to Pin 21, the trigger rate can be controlled by a potentiometer coupled between Pins 18 and 19, with the wiper connected to Pin 20. The discriminator does not trigger with the maximum negative voltage available applied to Pin 20.

Output Signals

Oscillator, Pin 7.

Pulses of width up to 3 μsec are produced for low oscillator rates. These approximate a square wave at 10^6 pps. Amplitude is at least 4 V with a 20-mA load. Rise time to +4 V is less than 0.1 μsec.

Pulse width, Pins 13 and 14.

Both pulses go to +4 V with a 20-mA load. Rise time should be less than 0.1 μsec. Loading on Pin 13 affects the signal at Pin 14 but loading Pin 14 cannot significantly affect the pulse on Pin 13.

Random rate, Pin 22.

0.5-μsec pulses occur at random intervals of greater than 0.8 μsec. The average rate is controlled by the voltage at Pin 20.

Circuit Details

(Refer to Fig. 9.)

Oscillator circuit.

The oscillator circuit is described in 11X2011 D-1.

One-shot module.

The one-shot module is described in 11X1731 D-1. It has a recovery time of about 10% of the "on" time. The external resistor to Pin 11 must not be larger than 50 kΩ for reliable operation. The input to Pin 17 is arranged so that a mechanical contact can produce single pulses, C9 feeding a fairly high impedance with CR1 reverse biased. When the circuit triggers, C9 is discharged rapidly via a negative pulse through R9 and CR1, so that retriggering is impossible for many milliseconds.

Random-rate generator.

The random-rate generator uses transistor Q3 as an amplifier for the 2 V input noise signal to Pin 21. The diode pump CR5, CR6, and C10 helps to stabilize the average triggering rate. Higher trigger rates charge C11 negatively, so that the negative bias at Si is increased, thus providing a form of negative feedback.

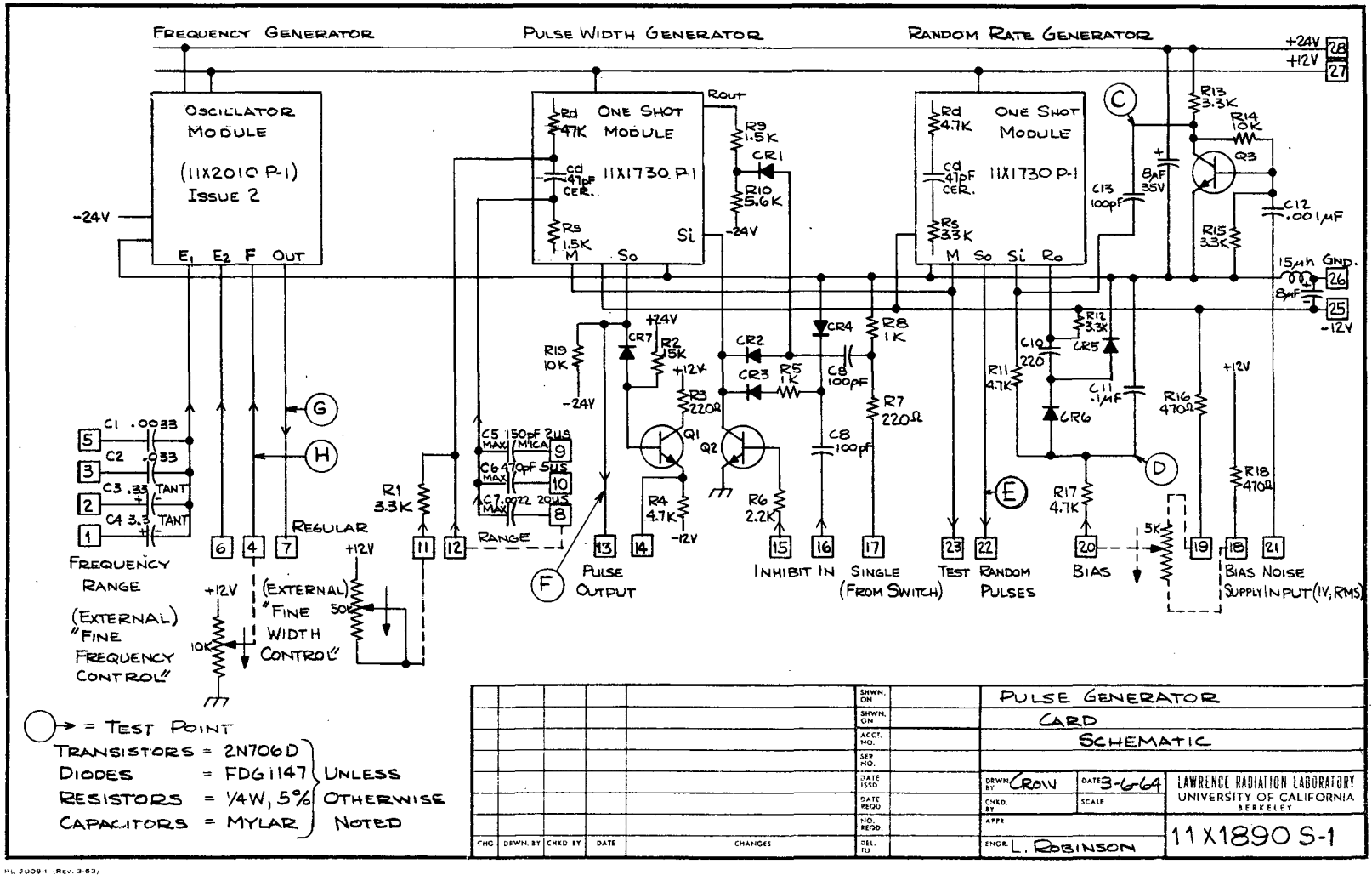

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Fig. 9. Pulse generator card schematic (11X1890 S-1).

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6. Tail-Pulse Generator Card

11X1941 D-1

General

This 4×8-in. 28-pin plug-in card contains two voltage sampling circuits having good temperature stability. Time constants are chosen so that one circuit produces fast rising pulses with long tails; the other can produce flat-top pulses up to 10 μsec wide.

Input Requirements

Drive pulses, Pins 20 and 22.

Pulses of +4 V are applied to one of the two inputs to produce either a tail pulse or a square pulse. The width of the square pulse is about 0.3 μsec greater than the width of signal applied at Pin 22. Input rise time should be less than 0.2 μsec.

Amplitude control, Pin 18.

A voltage between 0 and -10 V determines the amplitude of the output pulse. Input impedance is greater than 200 kΩ for fixed input voltage.

Tail-pulse time constant, Pin 13.

The tail-pulse output waveform is determined by the decay time constant of C12 (a 100-pF capacitor) across an external resistor connected between Pin 13 and ground. When a flat-top pulse is produced, a 1-kΩ shunt is used to give a fairly fast trailing edge.

Output Signals

Shaped Pulse, Pin 5.

Pulses are produced of -50 mV to -10 V from an impedance of a few ohms. This driver will drive -10 V into 100 ohms, although it normally drives an 825-ohm load. Pulses have rise times of less than 50 nsec. Decay time is determined by connections to Pin 13 and by which input, Pin 20 or 22, is used.

dc Output, Pin 17.

The input voltage to Pin 18 is reproduced at Pin 17 with stability of a few millivolts with 100-ohm output impedance.

Circuit Description

(See Fig. 10.)

The voltage sampling circuit has been used and described by several workers; its essential features for this application can be briefly noted, referring to Q10 and Q11.

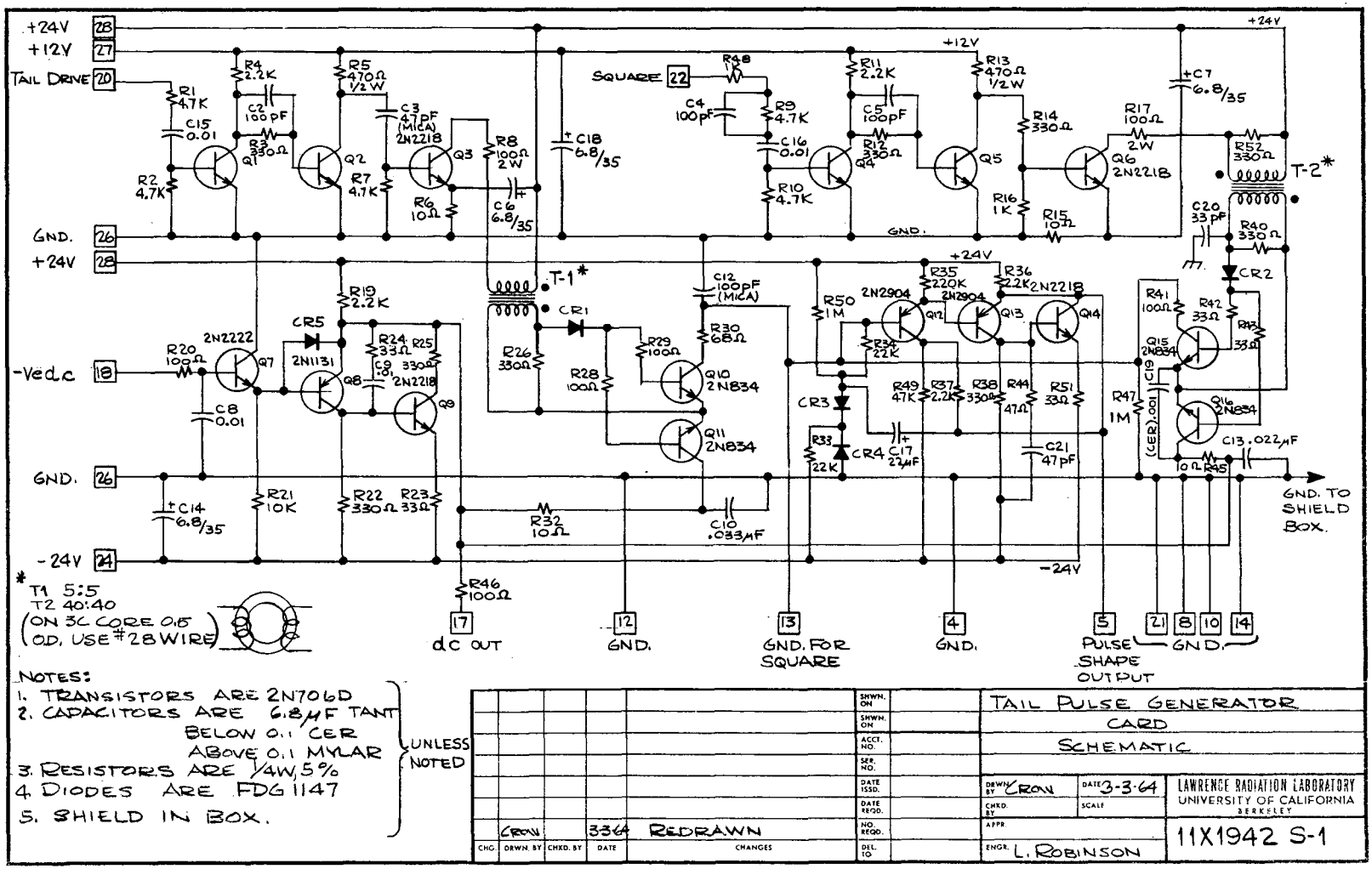

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Fig. 10. Tail pulse generator card schematic (11X1942 S-1).

A pulse, through transformer T1, brings Q10 and Q11 from their normal nonconducting state into saturated conduction, so that the voltage at the collector of Q10 falls to within a few millivolts of that at the collector of Q11. (The difference can be made very small by selection of matched transistors, but will generally by less than 50 mV if any two transistors of the same type are used.)

For the tail-pulse application, the drive pulse is made just wide enough to allow C12 to fully charge to the voltage at the collector of Q11. The values of T1 and the components associated with Q1, Q2, and Q3 were chosen to produce a suitably shaped charging pulse having a fast leading edge and a fairly slow trailing edge. Capacitive coupling across T1 is held as low as possible. Diode CR1 helps to prevent the negative-going signal that follows the charging pulse from affecting the output signal. Resistor R30 helps to hold worst-case overshoot signals to less than 50 mV at the output. Wiring layout is fairly critical here.

The square pulse produced by Q15 and Q16 can be up to 10 μsec wide, and time constants of T2 are chosen accordingly. Capacitors C20 and C19 improve the output waveforms (with the particular layout used).

The output circuit including Q12 through Q14 is a compromise between requirements of speed, duty cycle, and amplitude stability. The signal base line for tail pulses is determined by diodes CR3 and CR4 and is affected by the base current of Q12 through R34. The bootstrap capacitor C17 must be recharged even at high duty cycles, and for this reason the current in CR4 has been made much larger than that in CR3. When flat-top outputs pulses are produced, a 1-kΩ resistor shunts Pin 13 to ground, so that the base line is virtually unaffected by base current in Q12.

It should be clear that the voltage base line at Pin 5 does not affect pulse amplitude. However, any shift of voltage at the base of Q12 does change pulse amplitude, since the pulse amplitude depends on the difference in the quiescent voltage of the collectors of Q10 and Q11.

The dc-coupled amplifier Q7, Q8, and Q9 needs little explanation. Base emitter drops of Q7 and Q8 tend to compensate. Resistors R24, R32, and R45 and capacitors C9, C10, and C13 were added to reduce ringing in the circuit.

7. Linear Output Driver Card

11X1971 D-1

General

This 4×8-in. 28-pin plug-in card holds four co-ax cable-driver modules of the type used in the 11X1981 linear amplifier system. The circuit will drive ±10 V pulses into a terminated 125-ohm cable.

Circuitry has been included on the card to allow remote control of rise time for two of the modules.

Input Requirements

Input signals, Pins 2, 6, 15, and 18.

Pulses of either polarity with amplitude up to 10 V, with rise time no shorter than 50 nsec, are acceptable. Input impedance is fixed between 825 and 1500 ohms in series with 6.8 μF, depending on the rise time chosen.

Rise time control.

Integration time constants of 0.1, 0.2, 0.4, or 1.0 μsec can be selected for input signals on Pin 6 by grounding Pin 12, 10, 8, or 4 respectively. If those four pins are allowed to fall to -12 V, the input pulse is unaffected, with no integration. Lead length is not critical.

Similar results can be obtained for the input signal to Pin 18 by grounding Pin 22, 21, 20, or 19.

Output Signals, Pins 1, 5, 13, and 16

The circuit is designed to drive a 125-ohm terminated cable with pulses of either polarity and with amplitude up to 10 V. Output pulse width is limited by use of a 6.8-μF series output capacitor, which causes long pulses to droop.

Circuit Description

(See schematic diagrams, Figs. 11 and 12.)

Module.

The driver module has been used extensively in the 11X1981 amplifier system and is described here only briefly. Transistors Q2 and Q3 act as emitter followers for negative or positive pulses respectively. The output signal is fed back to the input of the inverting amplifier Q1 via resistor R3. The output voltage is slightly less than the input-signal current times resistor R3. Since the base line of the amplifier input is -12 V, this power supply line must be kept free from noise and ripple.

Capacitor C2 provides bootstrapping to give a high collector impedance to Q1. Transistor Q4 and resistor R9 limit the output current for positive output pulses, while R13 serves a similar function for negative output.

The emitter voltage of Q2 and Q3 is about +2 V and is affected by power supply voltages, so output signals are fed out via capacitor C4. This results in base line shift as a function of rate, but pulse amplitude is not affected by rate.

Plug-in card.

The plug-in card uses four modules. The input resistance of 825 ohms in series with 681 ohms gives an overall voltage gain slightly less than unity (R3 = 1.47 kΩ in the module).

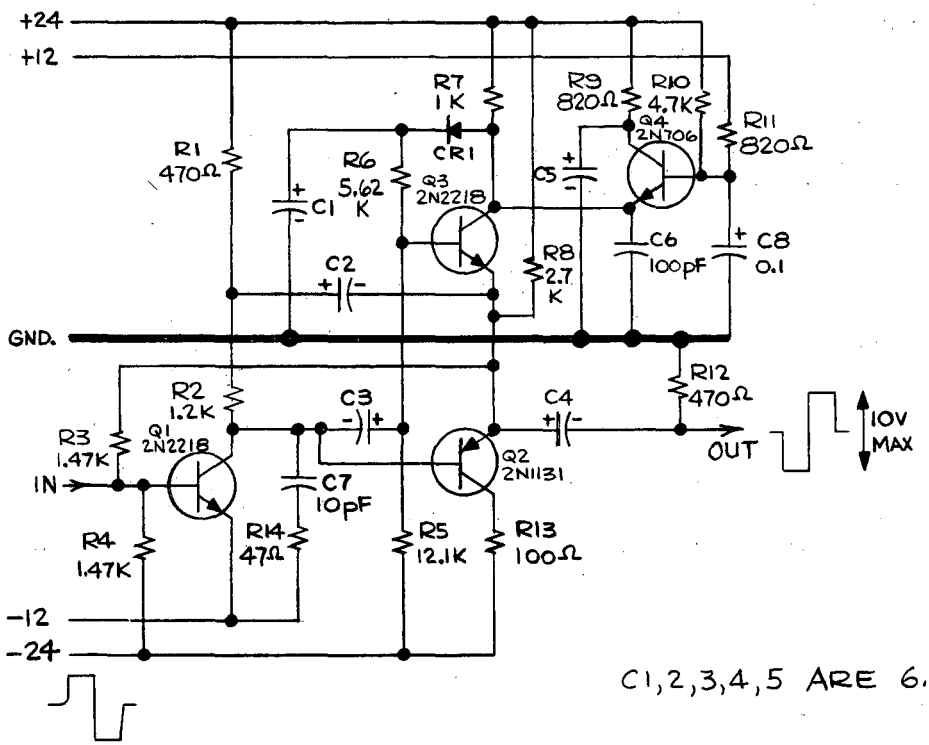
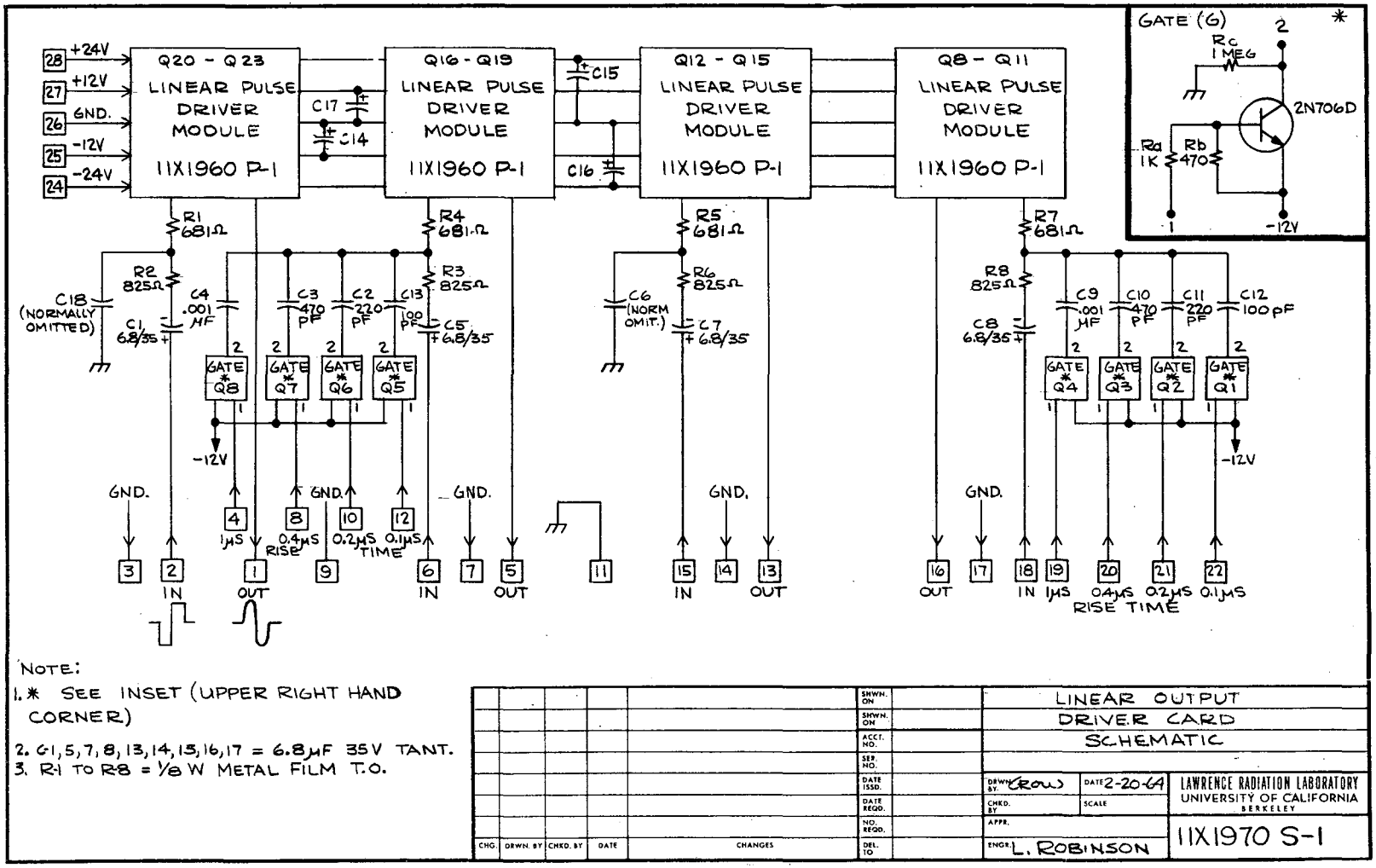


Fig. 11. ac-Coupled linear driver module schematic (11X1960 S-1).



NOTE:

1. * SEE INSET (UPPER RIGHT HAND CORNER)
2. C1, 5, 7, 8, 13, 14, 15, 16, 17 = 6.8μF 35V TANT.
3. R1 TO R8 = 1/8 W METAL FILM T.O.

					SHWN. ON	LINEAR OUTPUT DRIVER CARD SCHEMATIC	
					SHWN. ON		
					ACCT. NO.		
					SER. NO.		
					DATE ISSD.	DRWN. BY Crow	DATE 2-20-64
					DATE REQD.	CHKD. BY	SCALE
					NO. REQD.	APPR.	
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Fig. 12. Linear output driver card schematic (11X1970 S-1).

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The remotely controlled integrating time constants make use of the very low impedance of transistors Q1 through Q8 when current is applied to the base. When the transistors are nonconducting, they provide essentially an open circuit compared with R4 or R7.

The performance of this unit depends on careful grounding. Outputs should go directly to terminated 125-ohm cables, with the cable grounded at the card socket. Several grounded pins are provided for this purpose.

The circuit has been successfully used to drive 50-ohm cable, although the maximum output amplitude is slightly reduced and some overshoot appears on fast pulses.

8. Oscillator Module

11X2011 D-1

General

This four-transistor circuit is used with a standard printed wiring configuration, as part of several different plug-in cards. It is designed to allow remote selection of pulse repetition rates up to 10^6 pps.

Input Requirements

Frequency control.

The frequency range is determined by the capacity between points F1 and F2. Note that polarized capacitors should have the positive end connected to F1. The maximum period is increased by about 40 nsec per μF of capacity.

The frequency can be varied over a factor of about 12 by choice of the dc voltage fed to diode CR2. The dc source must be able to supply 1.5 mA. Maximum period occurs with voltage at +12 V.

Output Signal

Positive output pulses have a width close to 1 μsec at low repetitition rates. This width falls to about 0.5 μsec at 10^6 pps. Output current of 20 mA can be supplied at a pulse amplitude of +4 V. Pulse amplitudes up to 10 V can be produced into a high-impedance load.

Circuit Description

(See schematic diagram, Fig. 13.)

Transistors Q1 and Q2 form an emitter-coupled oscillator.

The period is determined by the capacity between the two emitters, by the amplitude of the voltage swing at the collector of Q2, and by the current in resistors R5 and R9. External fine control of the frequency is possible, since the voltage swing is determined by the voltage applied to CR2. Diodes CR3 and CR4 are used to keep reverse emitter leakage of transistors Q1 and Q2 from affecting the oscillator period.

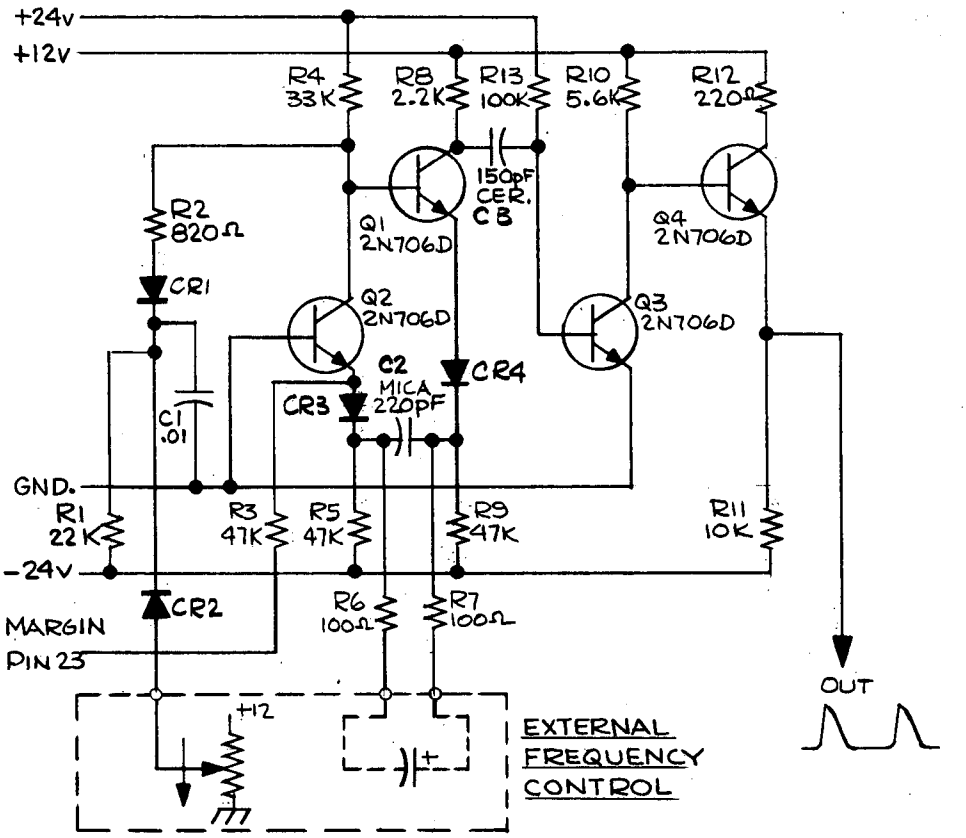

Fig. 13. Oscillator module schematic (11X2010 S-1).

Transistors Q3 and Q4 form an output amplifier. It is not feasible to derive output signals directly from the emitter of Q1, since the amplitude of signal at that point is a function of the frequency fine-control voltage.

Figure 14 is a schematic of the capacitor card used to determine the ramp period.

9. Rate Meter and Gate Card

11X2041 D-1

General

This 4×8-in. 28-pin plug-in card contains three independent circuits used in the ramp pulser assembly. One circuit has diode pumps to drive a linear rate meter at rates between 10^2 and 10^6 pps. A second circuit provides a dc Zener-regulated voltage that can be modulated. The third circuit routes pulses that determine which of two pulse-shaping circuits is energized in the tail-pulse generator card.

Input Requirements

Input signals.

Rate meter circuit: Pin 22 should be fed by +4 V, 0.5-μsec pulses. Longer pulses can be used at rates below 10^6 pps, but duty cycle should be below 50%.

Modulation circuit: Normally the 10-V ramp signal is fed to Pin 5. If no modulation is desired, Pin 4 and Pin 2 are connected.

Gate circuit: Pin 16 may be grounded, or allowed to float at +5 V. Input signals to be routed are fed to Pin 22. These signals must be able to drive 1 kΩ in parallel with the load at Pin 18.

Output signals.

Rate meter circuit: A 100-μA meter is connected from Pin 11 to Pin 13, 15, 17, or 19 for full-scale deflection with 10^6, 10^5, 10^4, or 10^3 pps respectively. The current is limited to slightly over 100 μA by R9.

Modulation and bias circuit: A -12 V Zener-controlled voltage between Pins 1 and 4 will drive a 1-kΩ load. If Pin 4 is not shorted to Pin 2, the voltage is modulated by 0.5% of the signal at Pin 5.

Gate circuit: Signals fed to Pin 22 are reproduced at Pin 18 if Pin 16 is allowed to float, or at Pin 21 if Pin 16 is grounded.

Circuit Description

Rate meter circuit.

(See Fig. 15.)

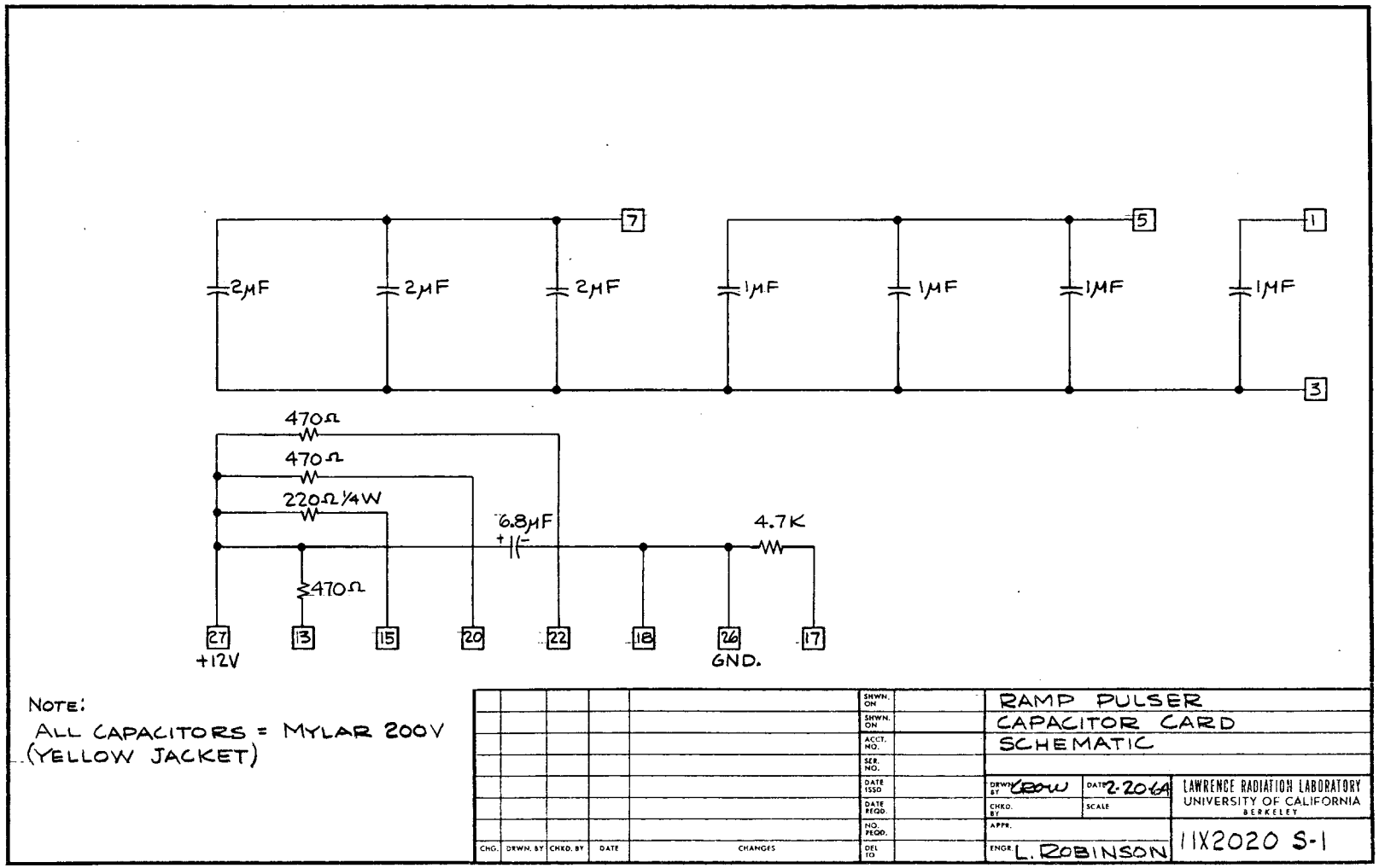

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Fig. 14. Ramp pulser capacitor card schematic (11X2020 S-1).

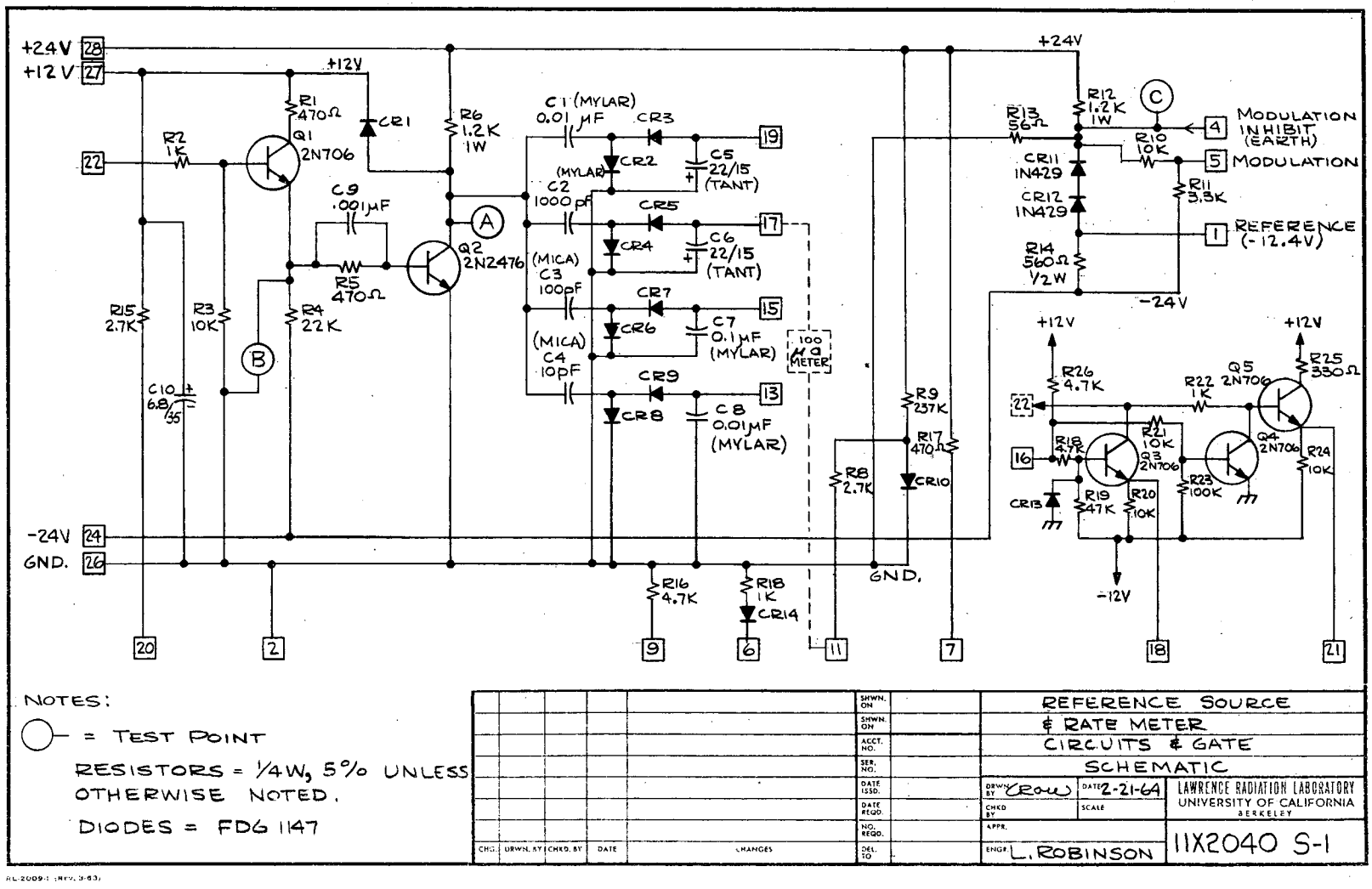

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Fig. 15. Reference source and rate meter circuits and gate schematic (11X2040 S-1).

Four diode pumps (for four frequency ranges) are driven by Q2. The power is adequate to drive only one of them at a time, so normally three outputs are allowed to float. Connecting one side of the external 100-μA meter to Pin 11 protects it against serious overload even when switching ranges. The 2N2476 is used for Q2 because of its rapid recovery from collector saturation. This circuit is somewhat sensitive to input pulse shape, and requires pulses of 0.5 μsec or longer for accuracy in the lowest ranges.

Gating circuit.

The operation of the gating circuit is straightforward. In one state, input signals to Pin 22 are coupled to Pin 18 with Q3 saturated, and Q4 clamping the base of Q5 to ground. In the other state, Q3 base remains at ground, while Q5 acts as an emitter follower.

Bias circuit.

The bias circuit can drive a 1 kΩ load. Two 6-volt Zener diodes are used for good temperature stability (±0.01% per °C).

10. dc-Coupled Linear Driver Card

11X2731 D-1

General

This card can be used as a direct replacement for the coaxial cable driver card 11X1971 P-1. It avoids most of the dc base-line shift that occurs with the 11X1971 driver, although its frequency response is slightly poorer.

Input Requirements

Ripple and noise on all lines can affect the output signal.

Input signals.

Input signals of either polarity and having a base line within 1 V of ground and with rise time longer than 50 nsec can be used. Pulse width should be less than 0.2 msec and duty cycles held below 30% to avoid base-line shift.

Output signals.

The output base line remains within 100 mV of ground level for duty cycles below 30% and is not affected by ±1 V shift in the input base line.

Terminated 125-ohm cables should be connected directly to the output pins of the card to obtain best frequency response, and to avoid possible oscillation.

Circuit Details

(See Figs. 16 through 18.)

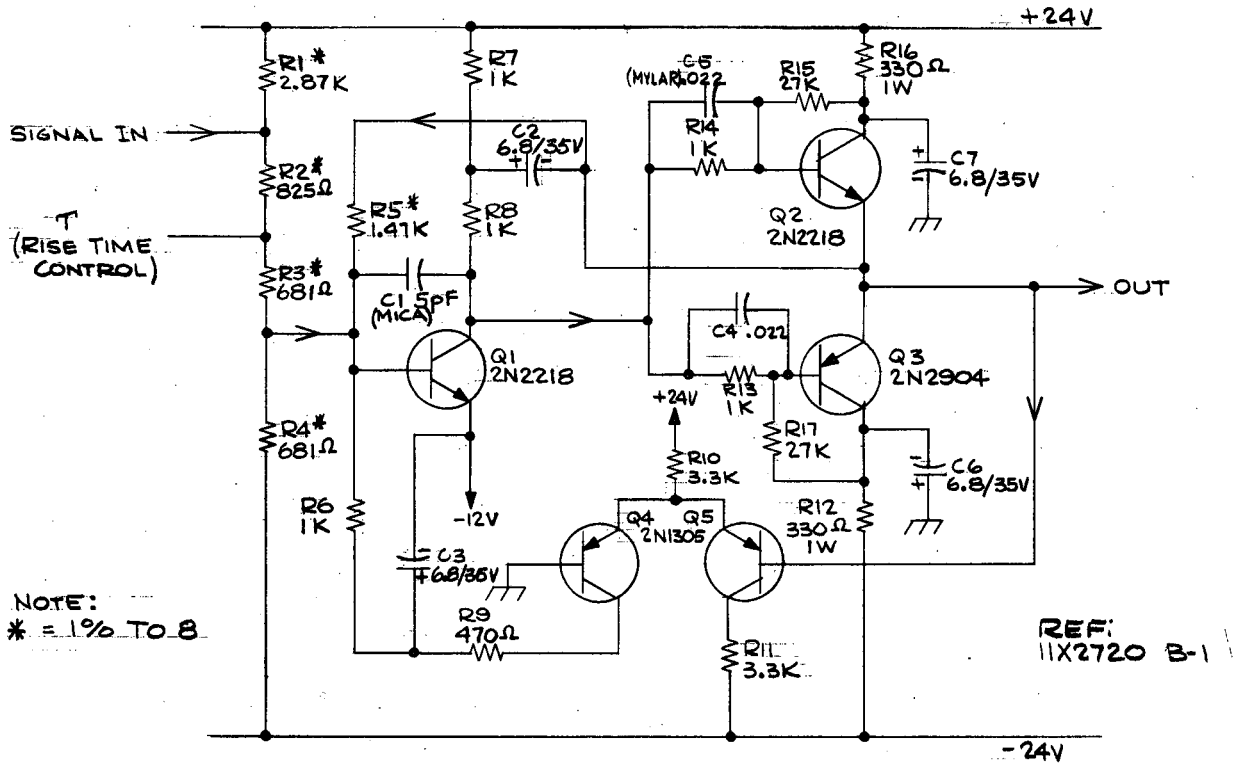


Fig. 16. dc-Restored linear driver module schematic (11X2720 S-1).

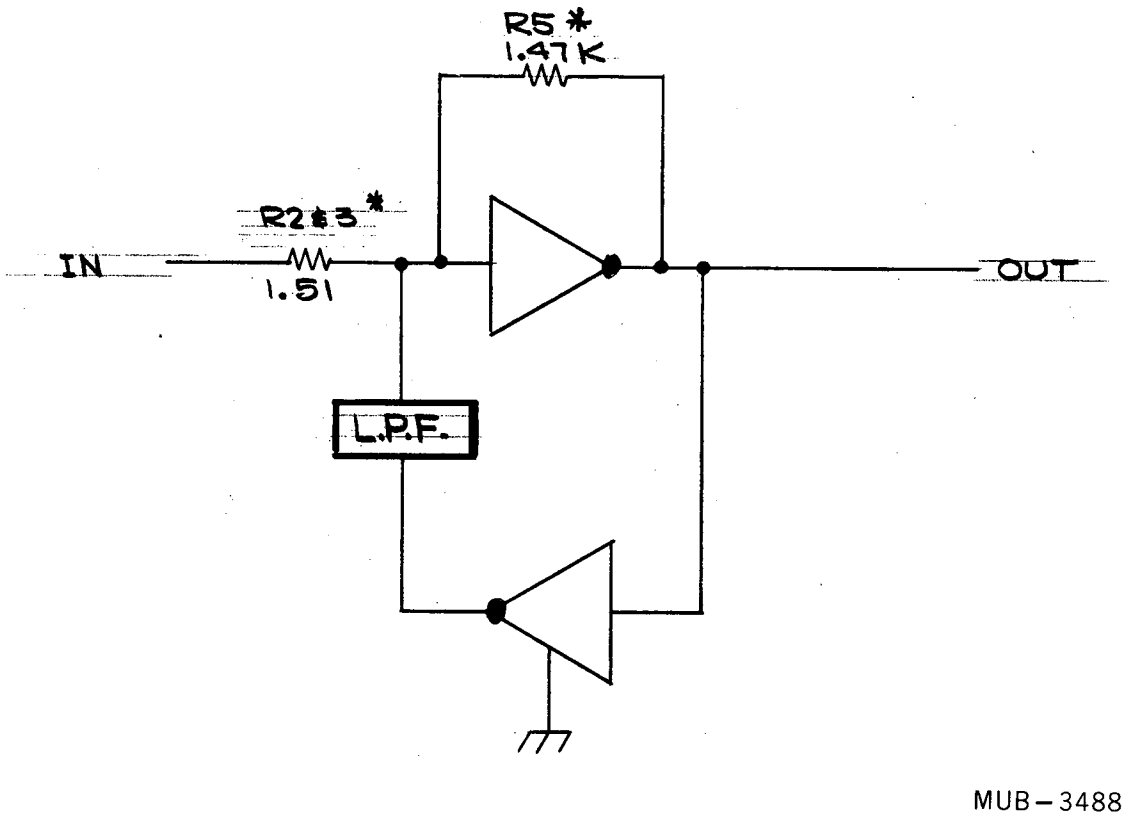
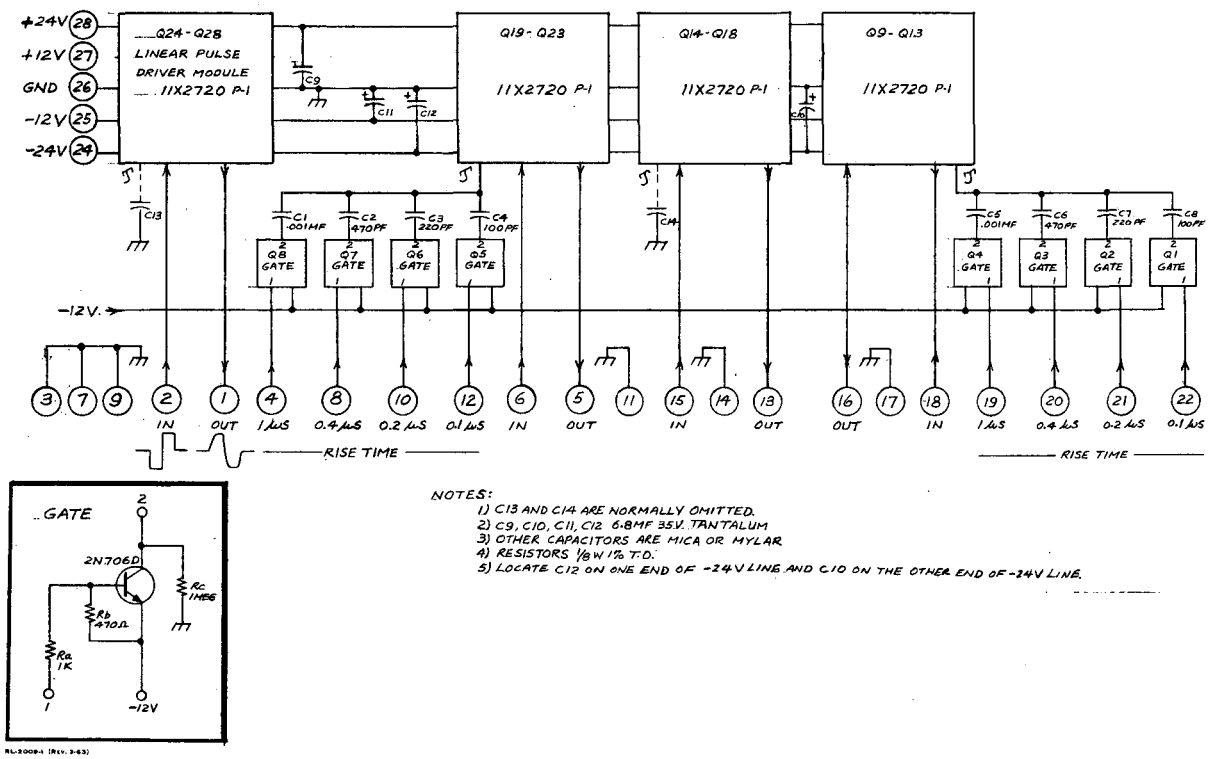


Fig. 17. dc-Restored linear driver module logic (11X2720 B-1).



NOTES:
1) C13 AND C14 ARE NORMALLY OMITTED.
2) C9, C10, C11, C12 6.8MF 35V. TANTALUM
3) OTHER CAPACITORS ARE MICA OR MYLAR
4) RESISTORS 1/8 W 1% T.D.
5) LOCATE C12 ON ONE END OF -24V LINE AND C10 ON THE OTHER END OF -24V LINE.

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Fig. 18. dc-Restored linear driver card (11X2730 S-1).

The circuit card contains four driver modules, with additional circuitry that allows remote selection of an integration time constant for two of the input signals.

The driver module (see schematic 11X2721 S-1) consists of an inverting amplifier Q1 with gain controlled by the ratio of resistors R5/(R2 + R3). Emitter follower transistors Q2 and Q3 provide bipolar drive power with power dissipation limited by R12 and R16.

Transistors Q4 and Q5 provide feedback to hold the quiescent output voltage within a few millivolts of ground potential. The integrating circuit R9, C3 prevents this feedback from affecting the voltage gain for short pulses. The maximum pulse width and maximum duty cycle are, however, limited by the time constant. No shift larger than 100 mV occurs for duty cycles less than 30%, and the feedback circuit causes a droop on pulses of only about 1 mV per μsec. Germanium 2N1305 transistors were used because of their good reverse base-emitter voltage characteristic.

This circuit is somewhat sensitive to capacitive loading on the output, and for good results, any cable driven by it should be terminated. Although 50-ohm cable can be used, better results are obtained with 125-ohm cable.

11. Time-to-Height Converter

11X2031 P-2

Purpose

A slightly modified version of the ramp pulser (11X2031 P-1) can be used for time-to-pulse-height conversion in the range from 5 μsec to 1 sec.

Circuit Description

(See Fig. 19.)

The time-to-height converter operates only when a switch on the rear panel is thrown to the appropriate position. Otherwise the unit acts as a standard ramp pulser, with the lock-off signal at Pin 4 causing diodes CR1 and CR2 to be reverse biased. (Pin 6 is connected to Pin 5 of 11X1310 S-1.)

In the time-to-height setting, the lock-off signal is removed, and the difference amplifier Q3 and Q4 feeds back to the ramp generator, holding its output at zero volts. (2N1304's are used because of the good reverse emitter characteristics.) When a time-to-height "start" pulse is received, the bistable circuit is set via R12, this decouples the difference amplifier from the ramp generator (CR1 is reverse biased), and the ramp goes in a negative direction until a "stop" pulse is received. The ramp amplitude is sampled at this point and the resulting pulse is fed to the output drivers. The bistable circuit is reset by the "stop" pulse feeding to Pin 20, allowing the difference amplifier to act again, since CR3 is now reverse biased. Resistor R7 provides about 1 mA of current to recharge the integrating capacitor of the ramp generator.

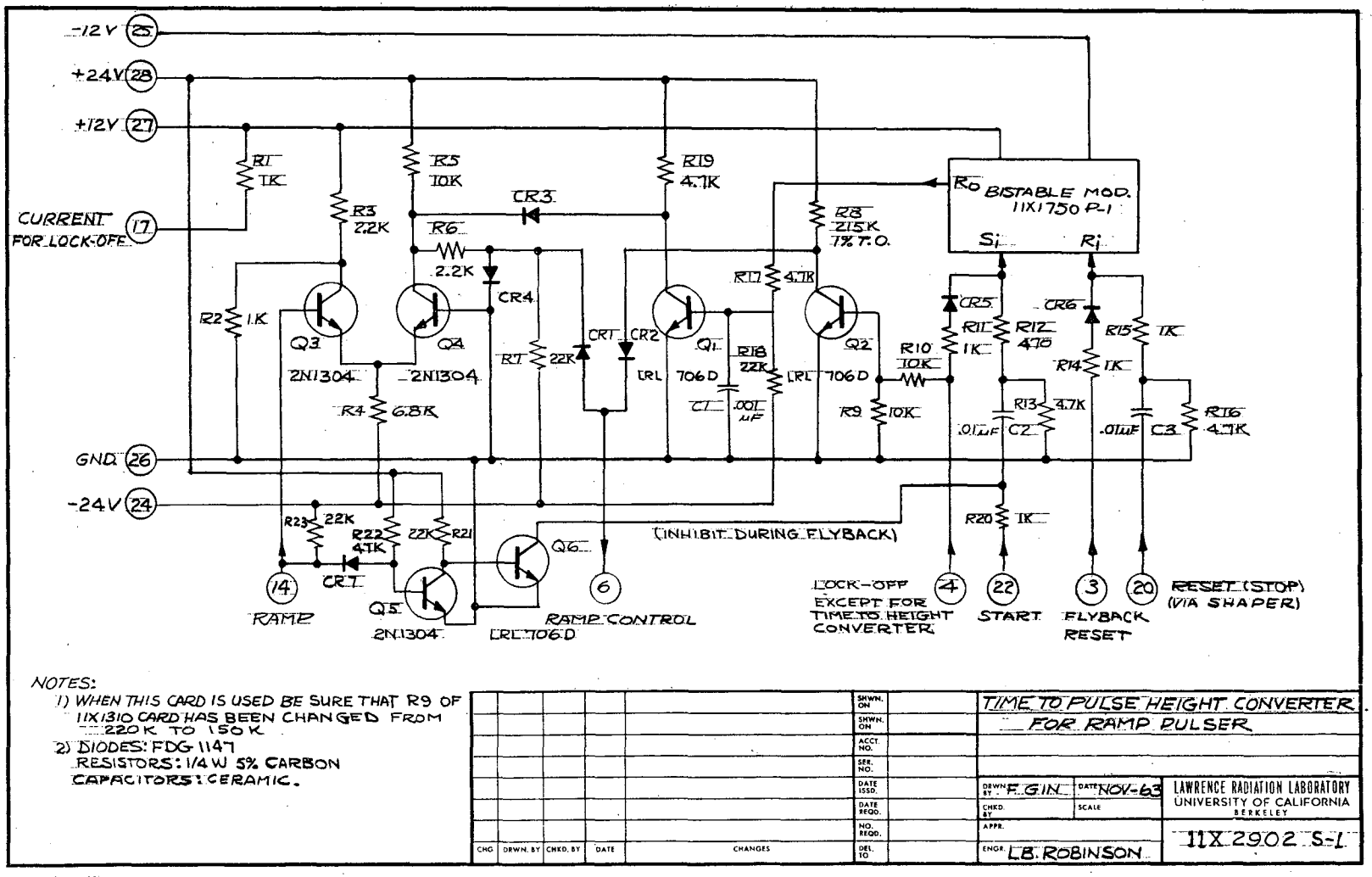

Fig. 19. Time-to-pulse-height converter for ramp pulser (11X2902 S-1).

If no stop pulse occurs, the bistable circuit is reset via Pin 3 during the normal flyback of the ramp.

Notes on Experimental Application

This unit is useful for high duty cycles, since the ramp resets in a fraction of the time to be measured. Some problems can arise at high rates, however.

The "+" and "-" "OUT" signals from the ramp pulser assembly are ac coupled, with a time constant less than 1 msec for a 125-ohm system. This could cause poor resolution in some cases; if so, the "dc" or "100 ohm" output pulse, which has no rate dependency, should be used.

If more than one time can be recorded during a single ramp cycle, e.g., when a high background is present, short times are favored, since the first pulse received cuts off the cycle, and a second pulse can never be recorded, even though the PHA dead time might allow several pulses per ramp cycle. In this case, the reset via Pin 20 and R15 on 11X2902 S-1 can be removed, and the ramp can then be sampled many times per cycle.

Modification to Standard Pulser for Time-to-Height Conversion

1. See drawing 11X2401 D-3 for chasis wiring.
2. Construct circuit shown in 11X2902 S-1, on a 28-pin plug on card, and insert in the miscellaneous card position of the assembly.
3. Mark front panel 11X2031 P-2.