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Fast startup RF blocks with Low Supply Noise Sensitivity for Internet of Things Applications

THESIS

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MASTER OF SCIENCE

In Electrical Engineering

by

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DEDICATION

To

My inspiring wife

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I would like to appreciate my advisor Prof. Michael Green for his invaluable guidance and discussions. Furthermore I would like to thank my family and friends for all their support and encouragement.

ABSTRACT OF THE THESIS

Fast startup RF blocks with Low Supply Noise Sensitivity for Internet of Things Applications

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Mohammad Radfar

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Professor Michael Green, Chair

In this thesis, mechanisms that cause LC Oscillator frequency sensitivity to supply noise is analyzed. It is proven that variations in both the common-mode and differential-mode components can increase the jitter in the presence of supply variations due to non-linearity of the capacitors that are in the oscillator. A novel compensation technique that reduces this sensitivity is presented. Simulations show that this technique can reduce the periodic jitter due to supply sensitivity by more than 80%.

CHAPTER 1

INTRODUCTION

Internet of Things (IoT) is the next generation of communications networks that is expected to dominate the hardware and software industry due to the very high number of devices that will be interconnected. As the IoT applications are growing at a very fast rate, the hardware requirements are becoming more complicated and hence, performance of RF/Analog blocks can be critical for optimizing the cost and efficiency of the performance for IoT systems. Therefore, new design techniques must be developed for low-power RF transceivers and local oscillators with low sensitivity to the external noise and fast startup. This includes the entire transmitter and receiver chain. One of the most sensitive blocks in a transceiver is the local oscillator whose performance can strongly affect both coherent and burst-mode transceivers. In coherent systems, the frequency accuracy can be corrupted by the internal or external noise; hence, the resulting jitter can increase the bit error rate. In burst-mode systems, the oscillator startup time is also important, in addition to the above-mentioned performance parameters.

One of the most common ways to reduce LC VCO sensitivity to supply noise is by making use of an on-chip low-dropout regulator. Although the power supply rejection can be as high as 60 dB in low frequencies, effects due to capacitive coupling, can reduce it to 20-30 dB at higher frequencies such as 10 MHz [1]. The additional power consumption can be from 2% to 20% of the total current consumption [2]. Recent work [3] focused on the supply sensitivity of a ring oscillator. In that paper it was shown that this sensitivity originates from modulation of the RC time constant of the output load of each delay cell. It was then shown

that the insertion of additional circuitry at the output of each delay cell could counteract this modulation and thereby reduce the supply sensitivity by nearly an order of magnitude. Developing a similar type of dynamic approach to LC oscillators was the motivation of this research.

In this thesis, an analysis of the effect of supply noise on LC oscillator performance is presented. It is shown that the jitter caused by the supply noise is due primarily to the nonlinearity of the capacitances – particularly the varactors. This behavior is shown by simulating the transient behavior of the VCO and generating both frequency vs. time and the eye diagrams. Then, a novel technique is introduced to compensate for the effect of supply noise on the output jitter. The compensation loop is designed and simulated to reduce the jitter by almost one order of magnitude [4].

CHAPTER 2

LC Oscillators Jitter and Supply Noise Sensitivity

The importance of reducing the jitter was explained in the previous chapter. In this chapter we will focus on the jitter caused by the supply noise. A simulation bench model is presented to quantify the effect of supply noise and how it can affect the frequency of oscillation and hence the jitter. In the next chapter, a compensation technique is developed to reduce the jitter and frequency variation caused by the supply noise.

2.1 LC Oscillation Supply Sensitivity Simulations

An LC oscillator topology with an NMOS cross-coupled pair is shown in Figure 2.1. It includes a pair of varactors C_{var} to control the oscillation frequency as a VCO; capacitance C_p that includes transistor drain-to-bulk capacitance C_{db}, gate capacitance C_g, and load capacitance of the following stage C_L as well as the fixed output capacitances adjust the frequency range; and an NMOS cross-coupled pair to provide the negative conductance needed to create positive feedback.

We assume for now that the bias current I_{ss} is designed to be independent of V_{DD}. The oscillation frequency is determined by the LC tank's resonant frequency, which is approximately given by:

$$\omega_r = \frac{1}{\sqrt{L(C_{var} + C_p)}}$$

With the exception of the fixed output capacitor, all of these capacitances exhibit nonlinearity -- i.e., they are all voltage dependent. It can be observed that for a fixed (i.e., supply independent) *ISS*, the voltage across level-shifting resistor *Rcm* will be constant, and thus any variation in V_{DD} will be seen directly at the output voltages *Vout+* and *Vout-*. Such a variation will modulate the voltages across the capacitances, thereby causing ω_r, and thus the oscillation frequency, to vary. It can be shown that the incremental sensitivity of the oscillation frequency with respect to VDD is given by:

$$\frac{1}{\omega_r}\frac{d\omega_r}{dV_{DD}} = -\frac{1}{2}\frac{1}{C_{var}+C_p}\left[\frac{dC_{var}}{dV_{DD}}+\frac{dC_p}{dV_{DD}}\right]$$

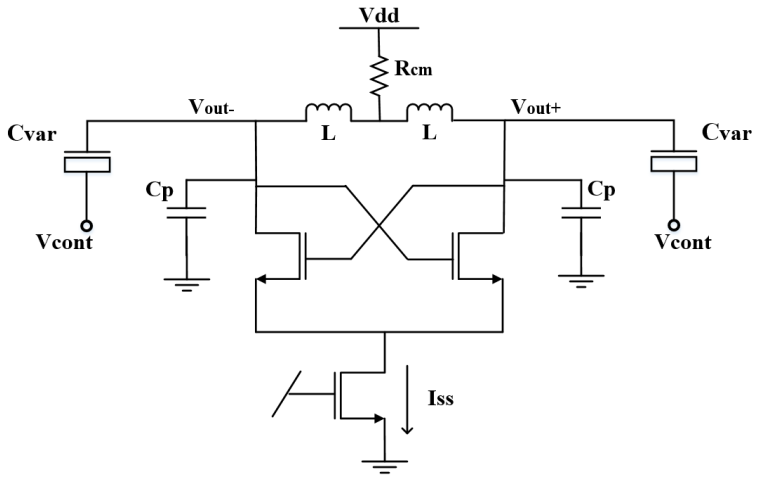

Figure 2.1: LC Oscillator Topology (NMOS cross-coupled pair)

In order to evaluate the amount of the oscillation frequency sensitivity to the supply noise, a transient simulation was run on the Fig. 2.1 circuit. The 5.7GHz oscillator is designed in Tower Jazz sbc18h BiCMOS Process with *L*=1nH; *Cvar*'s minimum and maximum capacitance are 50 fF and 130 fF respectively; *Cp* = 450 fF including all other parallel capacitance; *Iss* = 1 mA; and V_{DD} = 1.8 V. In order to determine the frequency sensitivity, a 10

MHz sinusoidal disturbance with 50 mVp-p amplitude at 10MHz is superimposed onto V_{DD}. Such a supply signal is shown in Figure 2.2.

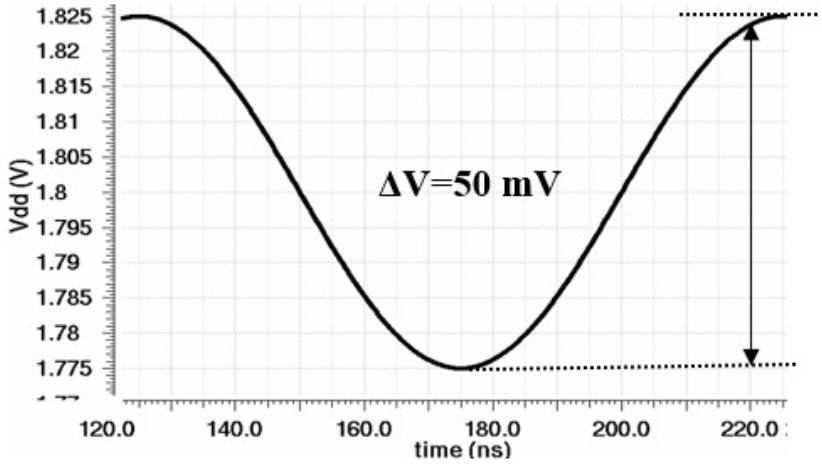

Figure 2.2: Supply with the 10 MHz disturbance

The 10 MHz frequency is chosen here because in a typical high-speed communication transceiver the PLL in which the VCO is embedded would typically have a jitter bandwidth on the order of 1 MHz. Frequency components of the disturbances below this bandwidth would naturally be attenuated by the action of the PLL. On the other hand, since the periodic jitter is inversely proportional to the disturbance frequency (as derived in Appendix 1 in [3], frequency components much higher than the jitter bandwidth would have little effect on the output periodic jitter. For this reason, 10 MHz was chosen as the disturbance frequency for the simulations presented here.

The sensitivity can be quantified using two different plots. Fig. 2.3 shows frequency vs. time over one cycle of the disturbance frequency. This method is specifically applicable for a single-frequency noise analysis. A more general simulation that can be also testable by

measurement is the eye diagram. As indicated in Figure 2.4 which is plotted in the same transient analysis as Figure 2.2 and 2.3, the supply noise causes variation in the zero-crossing times, thereby making the eye diagram more closed.

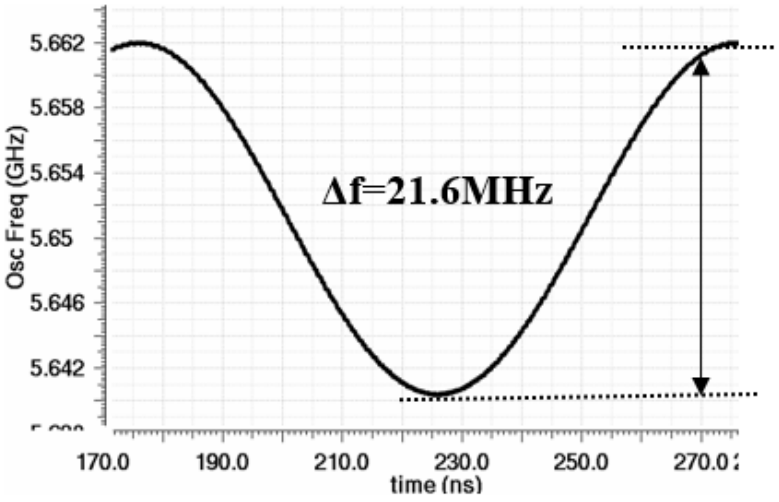

Figure 2.3: The frequency vs. Time plot for a single frequency noise

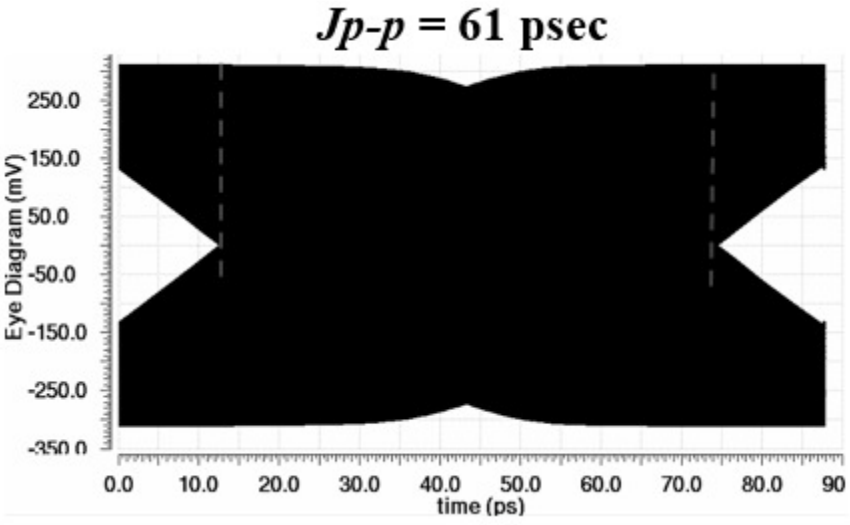

Figure 2.4: Jitter calculation by plotting the eye diagram

In order to characterize the independent mechanisms affecting the periodic jitter, we analyze and simulate the effects of variations in the common-mode output voltage tail current in the following sections.

2.2 Sensitivity Mechanisms

2.2.1. Sensitivity on Common Mode Voltage

Despite its fully differential structure, the Fig. 2.1 topology is sensitive to the supply noise even when like elements are perfectly matched. The frequency sensitivity is primarily due to the capacitance non-linearity at the oscillator's output nodes. The NMOS transistors and the load add nonlinear drain and gate capacitance, respectively, at the output nodes, but the most significant nonlinear capacitance in the VCO comes from the varactors. A typical varactor capacitance vs. gate-to-bulk voltage is shown in Figure 2.5.

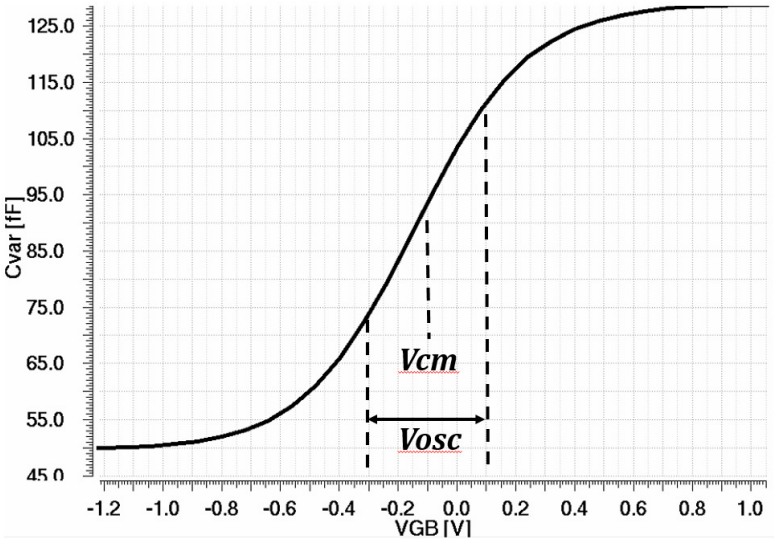

Figure 2.5: Varactor Capacitance vs Gate-Bulk Voltage

The varactor is used to provide a capacitance that depends on the applied control voltage V_{cont}. This is mainly used for fine-tuning the oscillation frequency. The slope of the capacitance vs. voltage of the designed varactor will determine the sensitivity of the oscillation frequency to the control voltage as indicated in Figure 2.6. This slope, known as *Kvco,* can be adjusted by setting the ratio of of varactor capacitance to the fixed capacitance at the oscillator outputs. This parameter should be high enough to provide the required frequency range of the oscillator. On the other hand, an excessively high *Kvco* leads to higher noise sensitivity and higher PLL loop gain, which can compromise stability. In GHz range oscillators, *Kvco* is normally adjusted to be a few hundreds of MHz. In the presented design, *Kvco* is 360MHz.

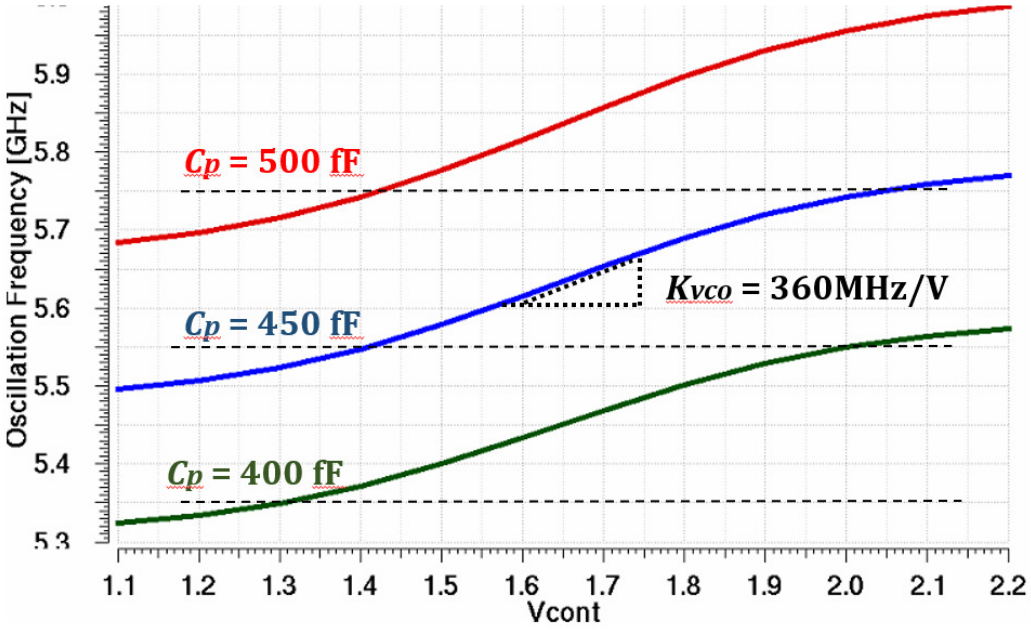

Figure 2.6: Fine Tuning by varactor design

The effect of varactor variation on the oscillation frequency has an important role in the noise sensitivity. Supply noise is directly applied to the common-mode voltage through the resistor biasing. This is illustrated in Figure 2.7 for the same simulation setup described earlier. In order to simulate only the effect of the common-mode voltage on the independent of other variation a 10MHz noise is applied to the supply with an ideal current source as indicated in Figure 2.8. This ideal current source is used to exclude the effect of tail current variations in this simulation setup.

The result indicates that as the common-mode voltage increases, the equivalent capacitance increases as well and hence the oscillation frequency decreases. This behavior is shown in the transient simulation waveform in Figure 2.9.

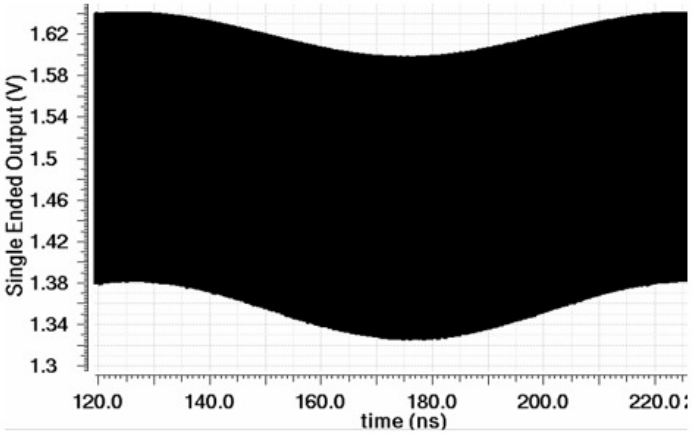

Figure 2.7: Single-ended output variation due to 10 MHz noise

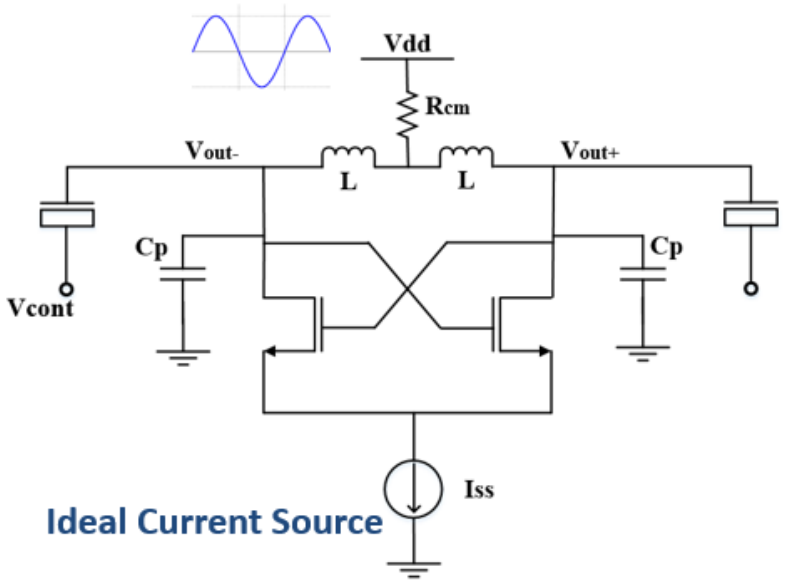

Figure 2.8: Common mode voltage variation effect on oscillation frequency

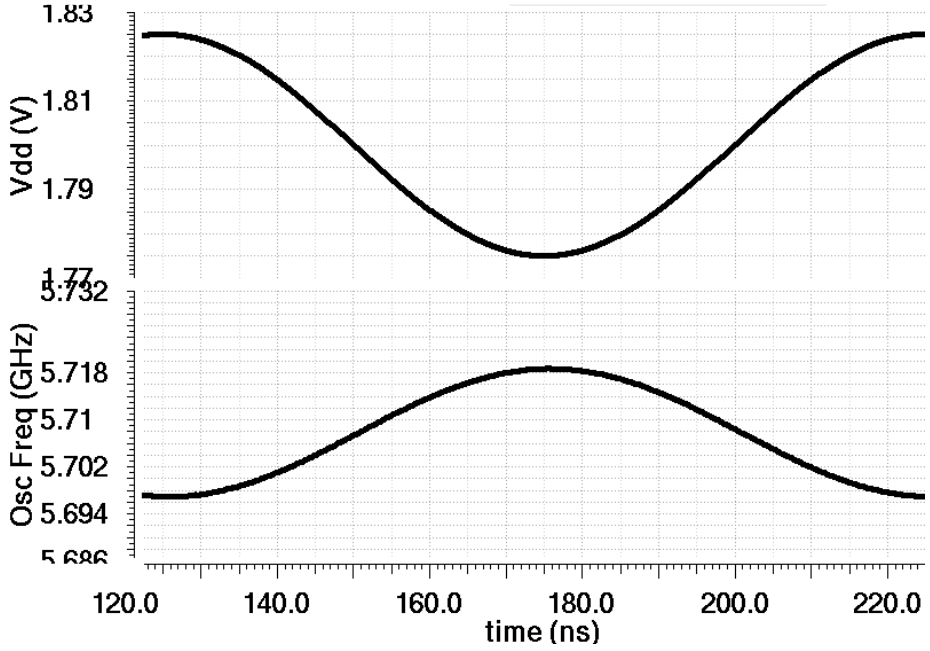

Figure 2.9: Oscillation frequency decrement as common mode voltage increases

2.2.2 Sensitivity to Oscillation Amplitude

The second parameter affecting the oscillation frequency is the oscillation amplitude. Due to the non-linearity of the capacitances, a change in the oscillation amplitude will vary the equivalent varactor capacitance and hence the oscillation amplitude. The equivalent capacitor can be considered as the value of a fixed-value capacitance that, if it replaced the nonlinear capacitors, would result in the oscillator exhibiting the same frequency; Fig. 2.10 illustrates this concept. Since the varactor C vs. V characteristics includes some non-linearity, even with the same common-mode voltage, the equivalent varactor capacitance will vary with the oscillation amplitude.

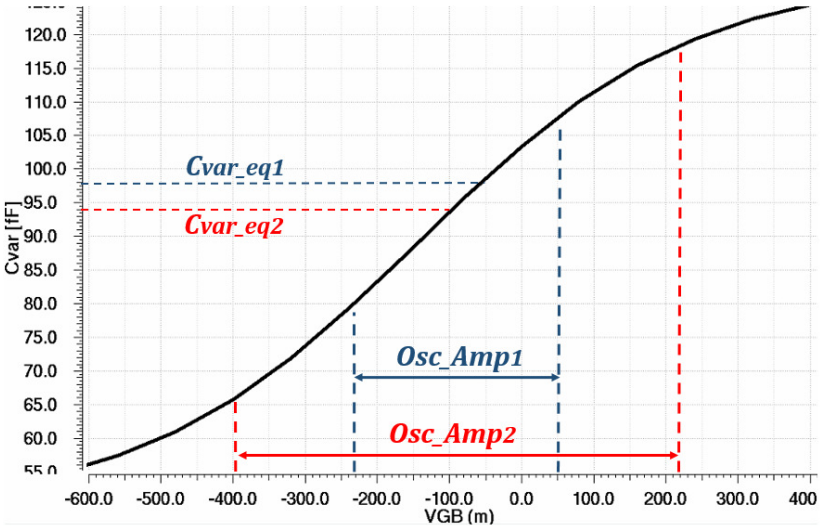

Figure 2.10: C vs V non-linearity and dependency of equivalent varactor capacitance on oscillation amplitude

2.2.3 Analysis of Sensitivity to Both Amplitude and Supply Variation

As shown in the previous sub-sections, the frequency of oscillation is sensitive to both the differential-mode amplitude and the DC common-mode voltage at the output nodes. Both of these effects can be observed from the family of curves in Fig. 2.11. These results confirm the effects described in the previous sub-sections indicating that the oscillation frequency decreases as the common-mode voltage increases for constant oscillation amplitude, while the frequency increases with oscillation amplitude when the common-mode voltage remains constant. In the next chapter, we will use these results to propose a technique, so that these effects compensate each other in order to reduce the sensitivity.

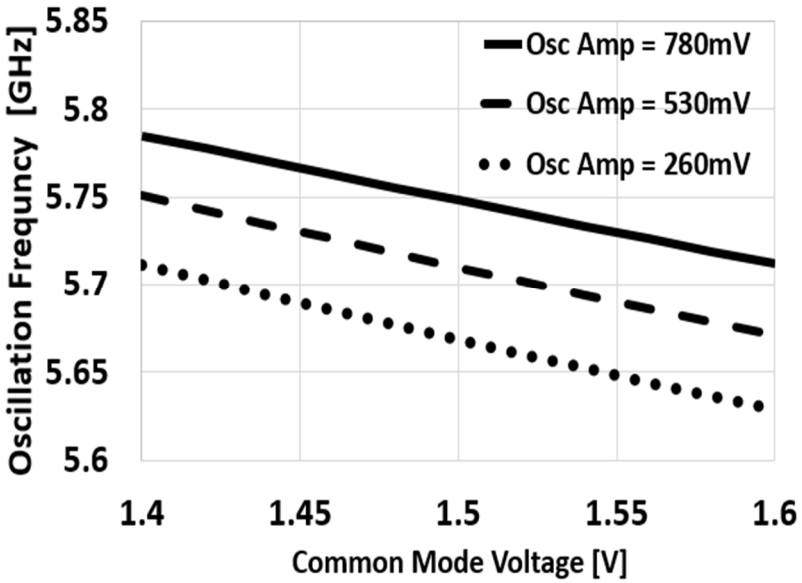

Figure 2.11: Oscillation frequency vs. common-mode voltage for three values of differential output amplitude

2.3 Supply Sensitivity for other LC Oscillator Architectures

LC oscillators are not limited to the topology shown in the Figure 2.1 circuit. Complimentary cross-coupled pair topologies such as the one shown in Fig. 2.12 [5] are widely used in the practical IC design industry due to their lower phase noise for the same current consumption. The architecture adds a PMOS cross-coupled pair in parallel with the LC tank. This leads to higher negative conductance, resulting in higher amplitude of oscillation and hence, lower phase noise.

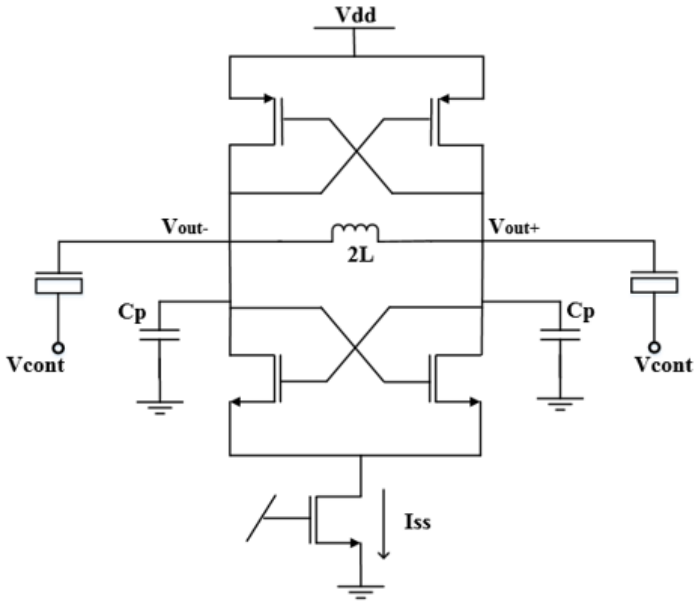

Figure 2.12: Complimentary Cross-Coupled LC Oscillator Architecture

Due to the same sensitivity mechanisms, complimentary CMOS cross-coupled pair structures have the same sensitivity as NMOS cross-coupled pair oscillators for the same design parameters such as varactor and output capacitances, supply voltage, and bias

current. A similar simulation bench as previous sections is set up to CMOS cross-coupled pair architecture. The frequency vs. time plot for the 50mVp-p supply noise at 10 MHz together with the eye diagram are shown in Figure 2.13. As can be seen in the plots, the supply noise results to 14.6MHz frequency variation which translates to 40 psec jitter at the output. Although the amount of CMOS cross-coupled sensitivity obtained in this case is smaller than NMOS cross-coupled pair, the mechanisms are the same, and as shown later, the same compensation technique shows the same improvement in both architectures.

2.4 Summary of Sensitivity Mechanisms Analysis

In this chapter, the problem of sensitivity to supply noise was discussed for two topologies of LC oscillators. The two mechanism of sensitivity were discussed and the way to calculate this parameter were presented. The next chapter uses the mentioned two mechanisms to cancel each other's effects in order to significantly reduce the oscillator's sensitivity to supply variations.

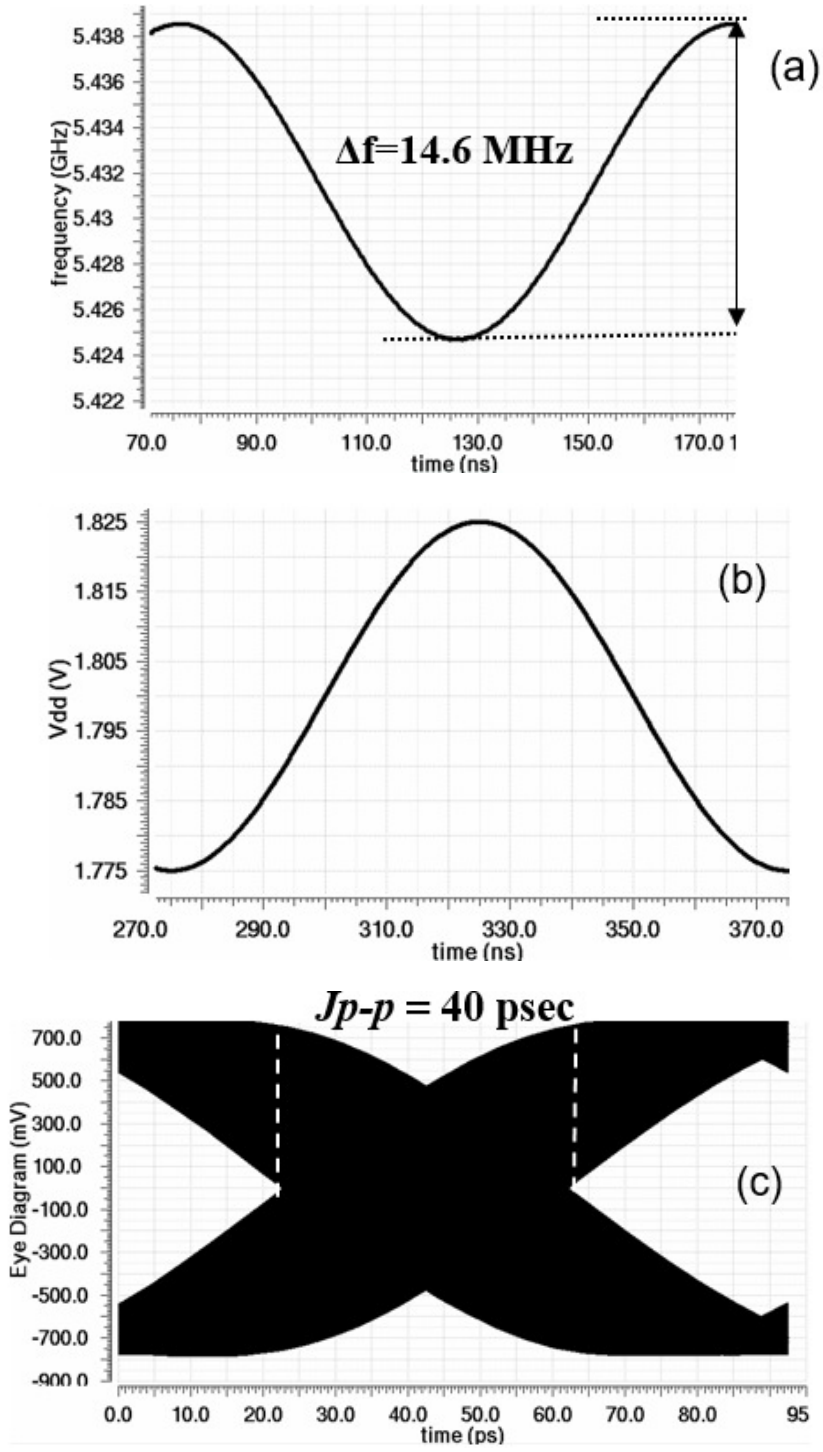

Figure 2.13: CMOS Cross Coupled LC Oscillator's Sensitivity to Supply Noise Simulations

(a) Frequency variation vs. time (b) The applied supply noise (c) Eye Diagram

CHAPTER 3

Developed Design Technique to Compensate LC Oscillator Supply Sensitivity

In the previous chapter, the effect of supply noise variations was analyzed in the LC oscillator topologies. The sensitivity was simulated through frequency vs. time plots and eye diagrams. In addition, two mechanisms affecting the supply sensitivity were introduced and studied, indicating the effect of common-mode voltage and oscillation amplitude (or tail current) on the oscillation frequency. In this chapter, a new design technique is developed to compensate the effect of the mentioned mechanism to achieve the minimum supply sensitivity [3].

3.1 LC Oscillator Compensation Loop

In order to minimize the supply noise sensitivity, we can start formulizing the sensitivity as:

$$\frac{\Delta f_{osc}}{\Delta V_{DD}} \rightarrow 0$$

Considering the two mechanisms of sensitivity we can break down the sensitivity as:

$$\frac{\Delta f_{osc}}{\Delta V_{CM}} \cdot \frac{\Delta V_{CM}}{\Delta V_{DD}} + \frac{\Delta f_{osc}}{\Delta A_{osc}} \cdot \frac{\Delta A_{osc}}{\Delta V_{DD}} \rightarrow 0$$

Where A_{osc} and V_{CM} are differential oscillation amplitude and common-mode voltage, respectively. We will assume that the bias current source is designed to be supply

independent so that $\frac{\Delta A_{osc}}{\Delta V_{DD}}$ is very small. Thus, with no compensation, the oscillation frequency variation will be mainly due to the dependency on V_{DD}. Since $\frac{\Delta V_{CM}}{\Delta V_{DD}} = 1$ in the Figure 2.1 Architecture, the sensitivity expression can be simplified as:

$$\frac{\Delta f_{osc}}{\Delta V_{DD}} \cong \frac{\Delta f_{osc}}{\Delta V_{CM}}$$

However, if we were to deliberately increase $\frac{\Delta A_{osc}}{\Delta V_{DD}}$ using a compensation loop, we could minimize the sensitivity, considering that the $\frac{\Delta f_{osc}}{\Delta V_{CM}}$ and $\frac{\Delta f_{osc}}{\Delta A_{osc}}$ have opposite signs as proved in the previous chapter. Such a dependence of the oscillation amplitude on V_{DD} could be set through the bias current:

$$\frac{\Delta A_{osc}}{\Delta V_{DD}} = \frac{\Delta A_{osc}}{\Delta I_{SS}} \cdot \frac{\Delta I_{SS}}{\Delta V_{DD}}$$

The term $\frac{\Delta A_{osc}}{\Delta I_{SS}}$ is determined by the equivalent parallel resistance of the LC tank which is highly dependent on Q of the inductor. But $\frac{\Delta I_{SS}}{\Delta V_{DD}}$ can be increased through a compensation loop that is developed as follows.

The compensation loop can be realized by modulating, with an appropriate gain, the tail current with the disturbance signal, so that oscillation frequency total variation is reduced. In order to implement this idea, the compensation loop is proposed as Fig 3.1. In the proposed architecture, the oscillator differential output is connected to a lowpass RC filter. The values of *Rfilt* and *Cfilt* are chosen to filter out the oscillation frequency component so that only the supply disturbance frequency and DC signal are passed to the non-inverting input of the op-amp. A reference voltage *Vref*, set to the desired output common-mode level, is applied to the inverting input of the op-amp. The output of the op-amp is applied to the

gate of M3; therefore, the supply noise modulates the VCO tail current and thus the amplitude of oscillation. The overall op-amp gain at the disturbance frequency should be determined such that the effect of common-mode variations can be canceled with the in-phase amplitude change. In order to accomplish this, the compensation loop gain is defined as follows.

$$\frac{\Delta I_{SS}}{\Delta V_{DD}} = \frac{\Delta I_{SS}}{\Delta V_{CM}} \cdot \frac{\Delta V_{CM}}{\Delta V_{DD}} = G_{COMP}$$

The gain can be written as:

$$G_{COMP} = g_{m3} \cdot A_v$$

where A_v is the op-amp voltage gain.

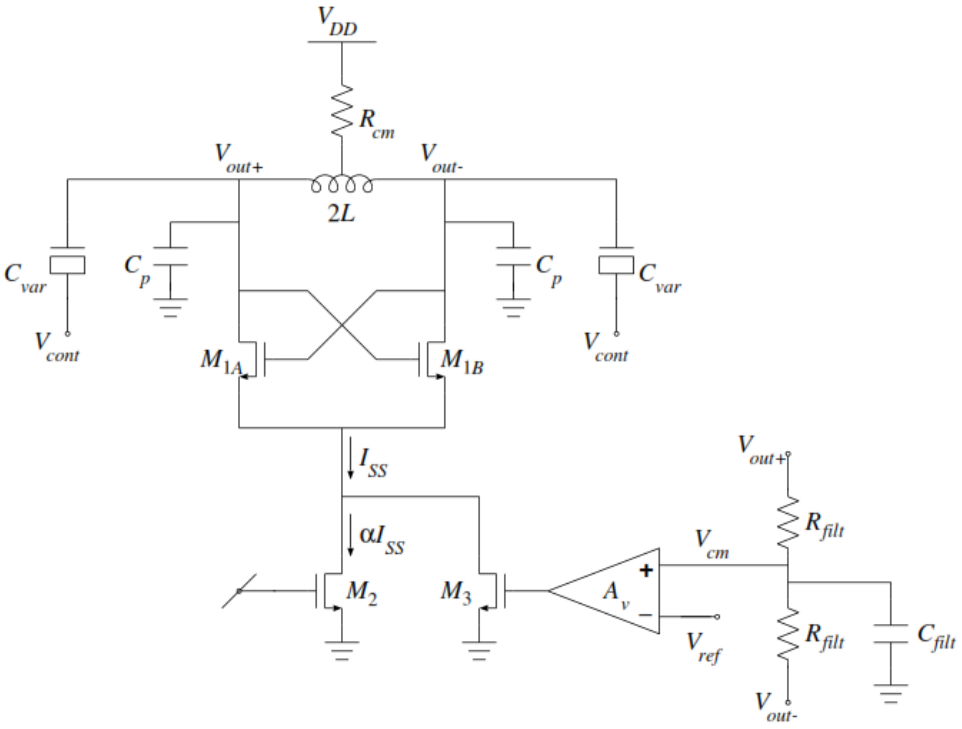

Fig 3.1 Compensation loop architecture

The op-amp is realized by a folded-cascode topology as shown in Fig 3.2 (a). In this case, the op-amp can provide high voltage gain in both DC and higher frequencies. The output common-mode level will be maintained close to *Vref* independent of any supply variations. However, the op-amp architecture needs to be modified in order to provide a high dc gain for stable biasing and a reduced gain in the noise frequency range in order to modulate the oscillation amplitude with the supply noise. This can be realized by adding a series RC at the op-amp output as Fig 3.2 (b). The capacitor in the series RC adds a low frequency pole near *1/(rout.C)* where *rout* is the folded-cascode amplifier output put resistance and a zero at *1/(R.C)*. This results in the op-amp frequency response shown in Fig 3.3. As expected, the DC gain is as high as *gm.rout* where *gm* is the amplifier's input differential pair transconductance. By setting the added pole frequency much lower than the supply noise frequency, we can achieve a fixed appropriate gain through the compensation loop. The op-amp gain in this case is $A_v = g_m R$.

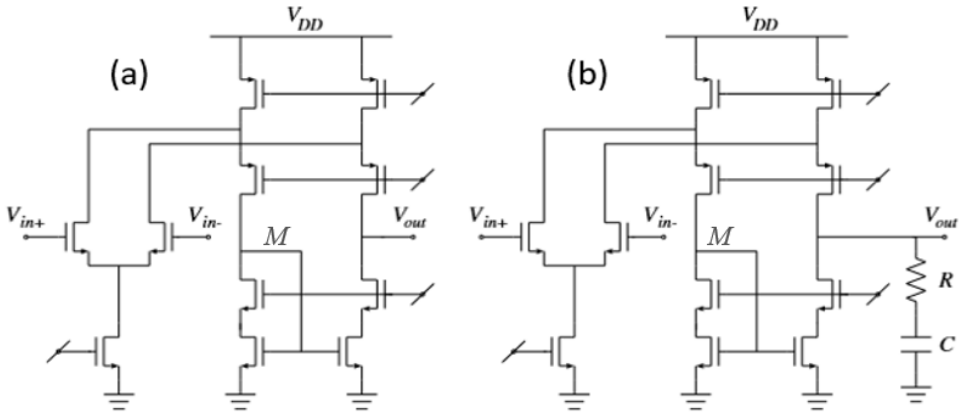

Fig 3.2 (a) Conventional folded-cascode amplifier (a) folded-cascode amplifier with low-frequency pole and zero

Referring to the previously derived formulations, in order to minimize the supply sensitivity we have the following condition:

$$\frac{\Delta f_{osc}}{\Delta V_{CM}} \cdot \frac{\Delta V_{CM}}{\Delta V_{DD}} = - \frac{\Delta f_{osc}}{\Delta A_{osc}} \cdot \frac{\Delta A_{osc}}{\Delta V_{DD}}$$

$$\rightarrow \frac{\Delta f_{osc}}{\Delta V_{CM}} = - \frac{\Delta f_{osc}}{\Delta A_{osc}} \cdot \frac{\Delta A_{osc}}{\Delta I_{SS}} \cdot G_{COMP}$$

where $G_{COMP} = g_{m3}.A_v$. The compensation circuit is designed in TowerJazz sbc18h BiCMOS process with Av = 3.3, g_{m3}=1 mA/V. These values were chosen in the way that the two side of the above mentioned equation cancel each other. Similar supply noise simulation is done with compensation loop. The frequency vs. time and the eye diagram is presented in Fig. 3.4. More than 80% sensitivity improvement is achieved in the eye diagram where the jitter is reduced from 61 psec to 13 psec together with the oscillation frequency variation reduced from 21.6MHz to 4.6MHz. In general, the required loop gain in the compensation circuit should be optimized depending on the details of the LC oscillator design.

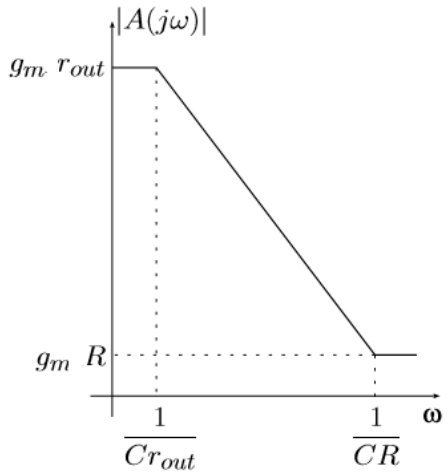

Fig 3.3 Compensation loop amplifier frequency response

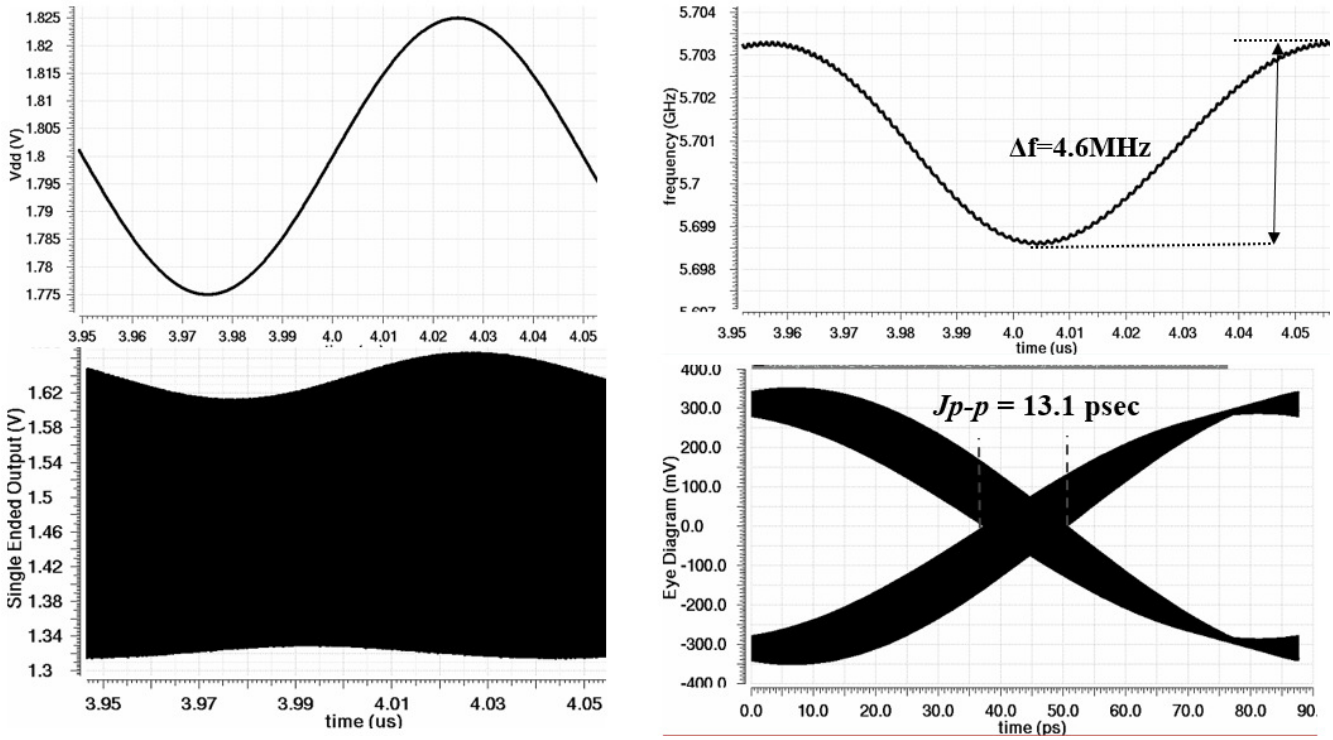

Fig 3.4: (a) Applied 10MHz 50mVp-p supply noise (b) Oscillation frequency vs. time

(c) Oscillator single-ended output waveform (d) Eye diagram

3.2 Compensation Technique Analysis

In the previous section, we proposed a new compensation loop technique that can significantly reduce LC oscillator supply noise sensitivity. In this section, other aspects of having this loop will be introduced.

3.2.1 Additional Power Consumption

While the oscillator total tail current remains constant after adding the compensation circuit, the amplifier will dissipate additional power. In this particular design, the op-amp

consumes 80 μA while the designed 5.7GHz oscillator current consumption is 1 mA from the tail current. Thus the compensation technique increases the current consumption only by 8%.

3.2.2 Phase Noise

Despite the fact that reducing the supply sensitivity can improve the external phase noise by around 14dB, the compensation loop circuit's elements contribute additional noise. This noise is applied to the tail current and thus will increase the phase noise generated by the oscillator. A simulation of the phase noise with and without the compensation is shown in Fig. 3.5 without any supply noise in the simulation. It can be observed that for the band of interest which is frequency range of higher than 1 MHz, the internal phase noise degradation is no more than 1-2 dB in the worst case compared to the 14 dB improvement in external phase noise. When the VCO is used in a PLL, the phase noise degradation for lower frequencies will be filtered in the PLL loop filter and thus will not affect the performance.

3.2.3 Loop Amplifier Frequency Response

As mentioned in the previous chapter, the amplifier needs to maintain a high dc gain and provide the optimum gain at the noise frequencies. The detail of this gain and corner frequency adjustment is shown in Fig. 3.6 where the frequency response is plotted for different values of series resistance and capacitance. The detail of the calibration will be discussed in the next subsection; however, maintaining constant gain in the band of interest,

which could be from the PLL loop bandwidth to 10 times the bandwidth has an important role to provide uniform compensation for the supply noise in different frequencies. This requires the non-dominant poles to occur at sufficiently high frequencies specially the mirror pole. In order to achieve this, the amount of parasitic capacitances within the signal path should be minimized. This can be interpreted as minimizing delay in the loop as the amplitude of oscillation needs to be modulated in-phase with the common-mode voltage. As indicated in the plot, the second pole is pushed to the frequencies more than 50MHz. This requires the capacitance at node M in Fig. 3.2 amplifier to be minimized.

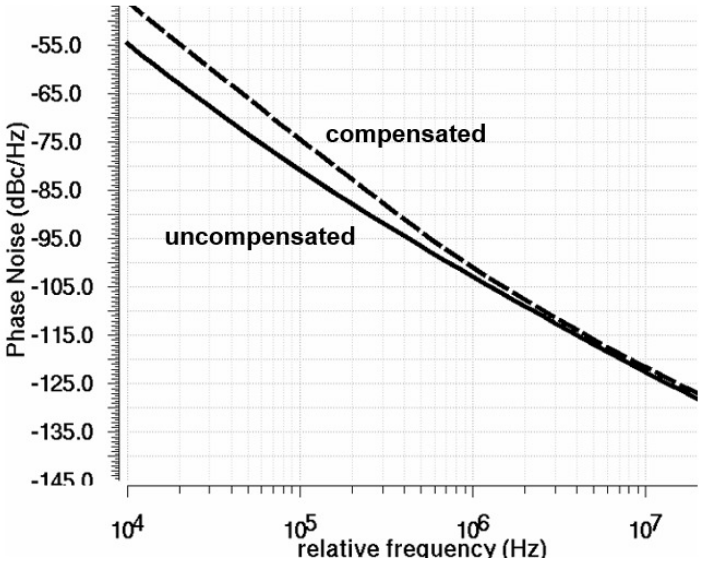

Fig 3.5: Phase noise comparison of compensated and uncompensated oscillator

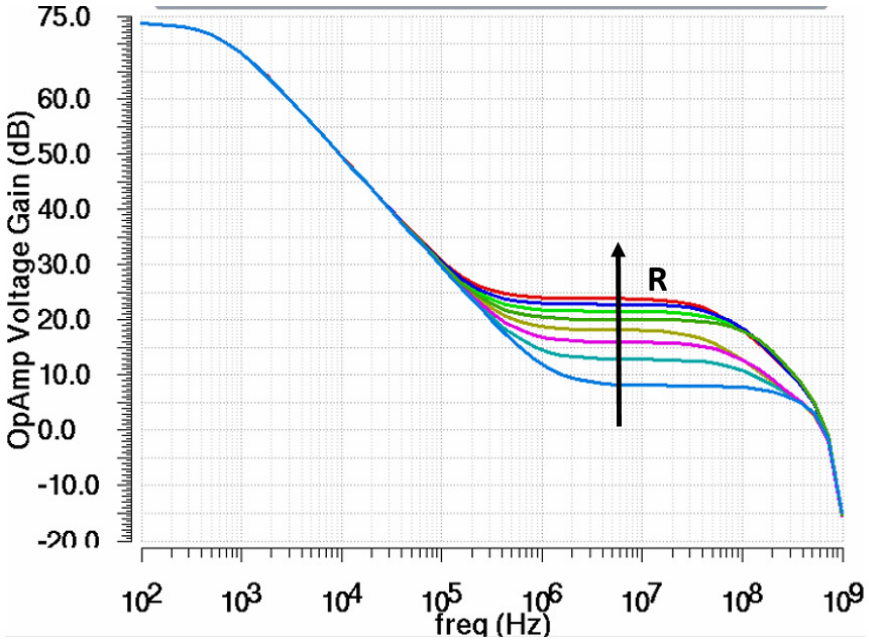

Fig 3.6: Loop amplifier frequency response

3.2.4 One-time Calibration against Process Variation

As the value of R and C in the series RC circuit might vary over the process, one-time calibration will be applicable in the practical implementation of the new compensation technique. Such calibration can be realized using programmable resistor ladders in series with the main *R* and the programmable capacitor bank in parallel with the main *C*. The calibration architecture is shown in Fig. 3.7.

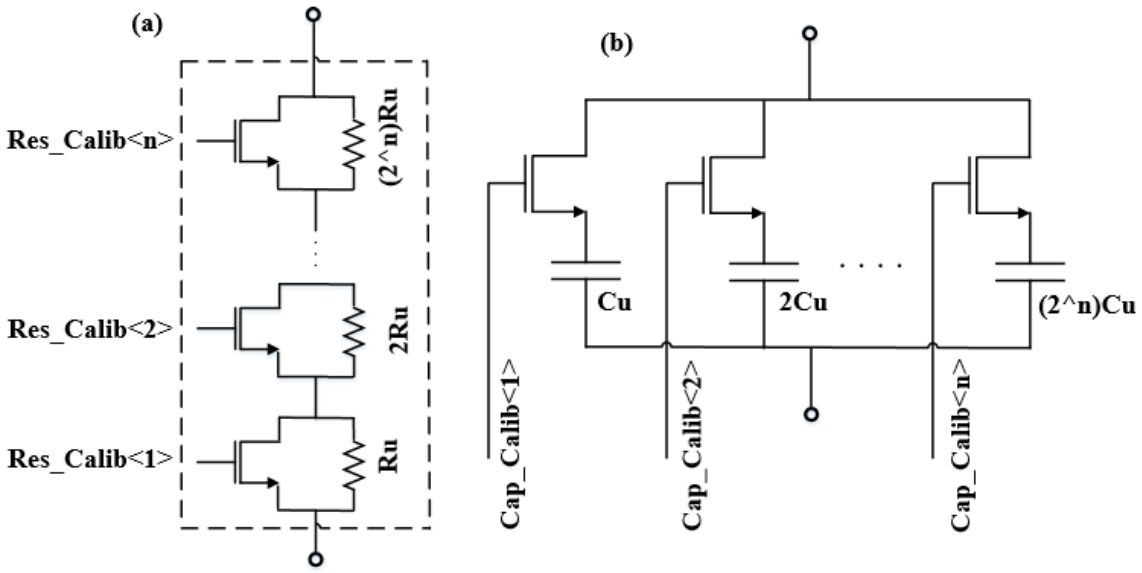

Fig 3.7: Programmable (a) Resistor ladder (b) Capacitor bank

3.3 Compensating the Complimentary (CMOS) Cross-Coupled Pair Architecture

In Chapter 2, we showed that the complementary (CMOS) cross-coupled pair architecture (Fig. 2.12) is also sensitive to the supply noise. This sensitivity was analyzed through a single-tone supply disturbance. In this section, we apply the compensation technique used in the VCO with NMOS cross-coupled transistors to reduce the supply sensitivity in this version of the VCO as well. The comparison of compensated and uncompensated CMOS cross-coupled oscillators to 10MHz 50mVp-p noise is presented in Fig 3.8. The results verify the efficiency of the technique in supply sensitivity reduction for the mentioned architecture as well. The oscillation frequency variation is decreased from 14.6 MHz to 2.9MHz. The eye diagram is also opened up showing jitter improvement from 40psec to 9.6psec, again introducing more than 80% sensitivity improvement.

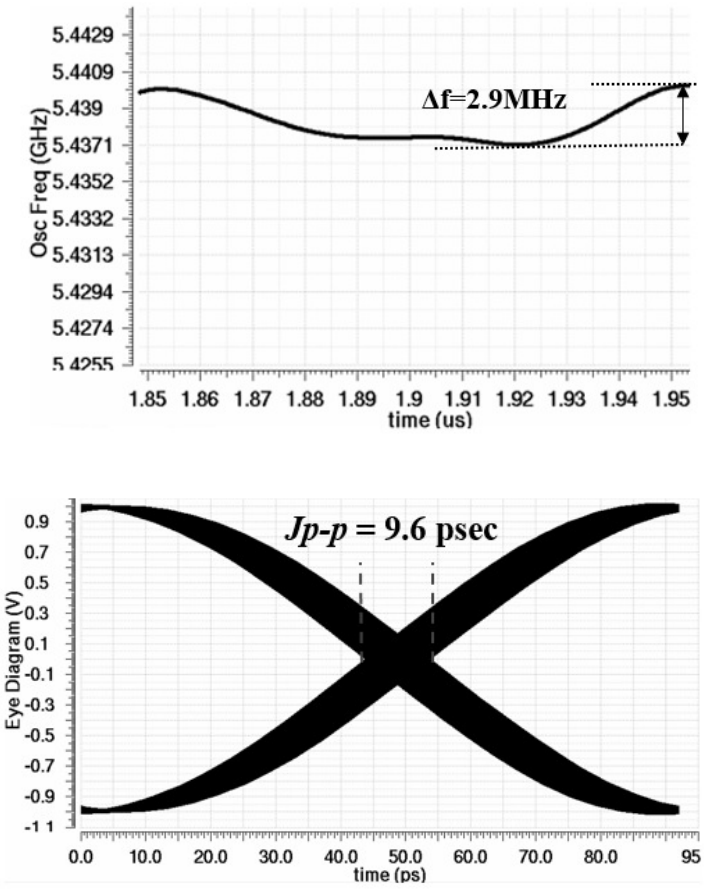

Fig 3.8: CMOS cross-coupled pair compensation for frequency variation and eye diagram

3.4 Summary of the Compensation Technique

In this chapter, a novel method is proposed using compensate sensitivity mechanisms through a compensation loop from the oscillation output to its tail current. The technique significantly improves oscillation frequency sensitivity to the supply noise by more than 80%. This improvement was achieved at the cost of 8% more current consumption and 1-2 dB additional phase noise. The efficiency of the method is examined for both NMOS and CMOS cross-coupled pair oscillator structure.

CHAPTER 4

Conclusions

In this thesis, the problem of sensitivity of LC oscillators with respect to the supply noise was studied and characterized for different architectures. The amount of sensitivity was quantified through the frequency vs. time variations and eye diagram. Then, the mechanisms causing the frequency variation were investigated. The common-mode voltage and the amplitude of the oscillation were shown to be two main parameters that can modulate the oscillation frequency through the operation.

Based on this analysis, a new technique was introduced to cancel out the effect of common-mode voltage and amplitude variation through an additional compensation circuit. The solution contains a compensation loop, modulating the tail current in-phase with the common-mode voltage variations. Using the optimized loop gain, the amount of supply noise sensitivity is efficiently reduced. The costs of applying this method on the internal phase noise and total power consumption were discussed. A one-time calibration method is presented to keep the sensitivity improvement over the process variations. The efficiency of the developed technique was also practiced for different LC oscillator architectures and also by post-layout verifications.

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