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# Integration of Active GaAs Based Optoelectronics onto Si Substrates

A dissertation submitted in partial satisfaction

of the requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Chia-Pu Chu

2014

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ABSTRACT OF THE DISSERTATION

Integration of Active GaAs Based Optoelectronics onto Si Substrates

by

Chia-Pu Chu

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2014

Professor Kang Lung Wang, Chair

Controlled heteroepitaxy and integration of arsenide based III-V compounds onto Si surfaces have been an important enabling technology for high efficiency solar cells and light emitters in satellite and optical interconnect applications. However, obtaining high crystal quality III-V compounds on Si, such as GaAs on Si is still challenging: (1) anti-phase domain (APD) boundary formation as the result of the polar GaAs growth on non-polar Si system, (2) a high density of threading dislocations generated by 4.1% lattice constant mismatch, and (3) the 62% thermal expansion coefficient mismatch leading to cracks during the cooling process.

The objective of this research is to obtain arsenide based III-V compounds monolithically integrated onto Si surfaces being APD-free with chemically abrupt GaAs/Si interfaces and possessing excellent optoelectronic properties. Patterned growth scheme by molecular beam epitaxy (MBE) is the approach I undertook to integrate GaAs based III-V compounds onto exactly oriented Si substrates. And the research consists of the following three stages to fulfill the objective.

**(1) Precise positioning and low defect density selective area epitaxy for self-assembled/catalyst-free GaAs nanodisks on $SiO_2$ masked exactly oriented Si(100) substrates:**

Pure zincblende GaAs nanodisks with precise positioning and low defect density are demonstrated by selective area epitaxy. Defects in the epilayers are reduced by strain relaxation through facets formation and by a lateral overgrowth scheme atop the SiO2 mask.

**(2) High-quality and defect-free GaAs thin film on $SiO_2$ masked exactly oriented Si(111) substrates by a two-step growth technique:**

Taking advantages of low energy for both Si(111) surface and GaAs/Si(111) interface, the two-step grown GaAs of total ~175 nm atop patterned Si(111) substrates exhibits atomically smooth surface morphology, single crystallinity and a remarkably low defect density.

**(3) Successful integration of InGaAs/GaAs double heterostrucure onto $SiO_2$ masked exactly oriented Si(111) substrates with remarkably reduced thermal stress:**

The atomically smooth and high crystalline quality InGaAs/GaAs DH is realized. The confined misfit dislocations at the nucleation layer and nearly threading dislocation-free buffer layer contribute to the atomically sharp GaAs/Si interface. The remarkable reduction in the thermally induced stress corroborates the effectiveness of the square shape pattern design. Optical properties and carrier dynamics are characterized by micro-photoluminescence (μ-PL) and time-resolved PL.

The dissertation of Chia-Pu Chu is approved.

Mark S. Goorsky

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Oscar M. Stafsudd

Kang Lung Wang, Committee Chair

University of California, Los Angeles

2014

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# Chapter 1

# Background and Introduction

## 1.1 Background

Controlled heteroepitaxy and integration of arsenide based III-V compounds onto Si surfaces has been an important enabling technology for high efficiency solar cells and light emitters in satellite and optical interconnect applications. Since the 1980s, III-V compounds epitaxially grown on Si substrates have attracted a great deal of interest due to the monolithic integration of optoelectronic devices with Si-based microelectronics[1-3]. In fact, successful heteroepitaxial growth will not only provide high carrier mobility and direct bandgap III-V materials, but also maintain the advantages of lightweight and low-cost Si substrates with high mechanical strength and excellent thermal management. Clearly, a number of advantages have been claimed for GaAs/Si technology. However, the drawback of the technology is that the GaAs layers monolithically grown on Si are much more defective than those on GaAs wafers, with the dislocation density of $10^7$ $cm^{-2}$ on Si wafers versus $10^3$ ~ $10^4$ $cm^{-2}$ typical for GaAs wafers. In addition, Si doesn't provide the semi-insulating property as GaAs does, which will make high speed device fabrication more difficult. Nevertheless, solar cells for satellites or light sources for optical interconnects would be durable applications because the lightweight, robust, higher thermally conductive are the driving forces.

On the other hand, the potential advantage is the capability to use the well-developed Si fabrication technology for high integration level, and to use GaAs based materials in local areas providing special functions. If the GaAs/Si layers can be seamlessly integrated with the Si devices, the combination would remarkably offer unique advantages. Optical interconnect technology would be the best example, and GaAs/Si technology could be used for optical interconnections

between silicon VLSI circuits. Current issues with optical interconnects are hybrid packaging, crosstalk, speed, and power consumption while signals traveling off chips[4]. An additional problem with optical interconnects is the loss associated with inefficiencies in converting the optical power to electrical power[5]. However, the direct combination of monolithically grown GaAs onto Si would solve these problems. To date, researchers have extensively focused on the growth of high quality III-V compounds on Si and accomplished the so-called bottom-up integration. However, obtaining high crystal quality III-V compounds, such as GaAs on Si is still challenging due to anti-phase domain (APD) boundary formation as the result of the polar GaAs growth on non-polar Si system; a high density of threading dislocations generated by 4.1% lattice mismatch along with 62% thermal expansion coefficient mismatch.

The objective of this dissertation is to obtain arsenide based III-V compounds monolithically integrated onto Si surfaces which are APD-free with chemically abrupt GaAs/Si interfaces and possess excellent optoelectronic properties. Because of the ultra−high vacuum nature of molecular beam epitaxy (MBE), we are capable of controlling the initial surface exposure, and apply in-situ high energy electron beam characterization technique to monitor the nucleation and growth process under various experimental conditions.

## 1.2 The role of MBE in III-V technology

Two epitaxial methods being successfully applied to the growth of high quality III-V compound semiconductors are MBE and metal organic chemical vapor deposition (MOCVD) as well as their variations. MBE and MOCVD are two fundamentally different crystal growth methods: MBE is primarily a non-equilibrium process while MOCVD is a quasi-equilibrium process. In comparison to MOCVD, MBE offers a superior capability in rendering highly complex compositional and

doping profiles required for high performance devices. This strength is the result of the conceptual simplicity of the MBE growth process, where doped layers are grown by depositing the constituent elements and dopants atom by atom. MBE growth can be understood without using either thermodynamics or crystalline physics. The composition of a layer and its doping level only rely on the arrival rate of their sources. The rate of production of the sources can be very easily and accurately controlled by effusion cell temperatures.

An MOCVD, however, is complicated by the need for chemical decomposition of the starting materials at elevated temperatures which introduces more remarkable diffusion and autodoping problems. Furthermore, fine control of atomic abruptness in MOCVD is severely affected by finite gas flow velocities and boundary layer effects. Ideally, MBE is a much simpler process for crystal growth compared to MOCVD, and all of the record-making microwave and optoelectronic devices are grown by MBE. Furthermore, since the performance is of paramount importance, MBE has an edge; there are several devices could only be successfully fulfilled from MBE growth procedures. One example related to the work here is the low-threshold continuous-wave (CW) GaAs-on-Si quantum well lasers. Additionally, MBE is a relatively low temperature, non-equilibrium growth process. The defects due to the lattice and thermal mismatch are more likely to be localized and usually will not affect the device operation a few hundreds nm away from the GaAs/Si heterointerface. Until MOCVD can really rival its performance, MBE along with its improved versions is here to stay although its role has been mostly continue to be restricted to research laboratories. For example, Chemical Beam Epitaxy (CBE) and Gas-Source MBE (GSMBE) combining the advantages of MBE and MOCVD can provide a long-term supply of source materials without breaking the vacuum which is very desirable in mass production[6-7], and they offer easy control of V/III ratio in growing quaternary materials like InGaAsP, which cannot

be easily done in conventional solid-source MBE. The only drawback has been the concerns over the use of highly toxic gases.

On the other hand, the combination of ion beam etching techniques and molecular beams in an MBE system offers an opportunity to complete the material growth, masking, etching, and metallization in a single MBE system without breaking the vacuum. With the help of such a technology is potentially more reliable and cost-effective. In the field of GaAs-on-Si, there have been numerous opportunities and challenges. Presently, almost all high-end microwave and optoelectronic devices have already been dominated by MBE, despite of the difficulty of GaAs-on-Si growth. The main problems within this field which remain are high defect density at the GaAs/Si interface, the control of interface defects and strain, the improvement of device performance. However, the development of the applications in GaAs-on-Si has been promising. The capability to produce device-quality heteroepitaxial growth for specific device purpose is a non-trivial challenge, and beginning with an issue of lattice constant mismatch, then thermal mismatch and bandgap alignment. The amount of lattice mismatch has the direct relevance to the success in epitaxial growth. Whereas, the mismatch in coefficient of thermal expansion can lead to severe growth/fabrication issues for the defect propagation into the active region of the devices. Last, the bandgap alignment evaluations determines suitability of the materials to fulfill a specific function within the devices. The monolithic integration of the III-V on Si holds a great promise for the future demonstration of the practical integrated III-V optoelectronics on a Si complementary metal oxide semiconductor (CMOS) platform such as the optical connects. Moreover, if successful, it will smoothly shift the optoelectronic market from using relatively expensive intrinsic substrates like GaAs or InP to Si substrates.

### 1.3 An overview of activities in electrical vs. optical interconnects

As aforementioned applications of III-V on Si integration indicate, optical interconnects could be the technology with the impactful importance. Future ultra-speed computers will process tremendous amount of data to meet the ever growing demand in science and technology. The throughput of a computer has to be increased dramatically from the current level. The researchers have predicted that the chip-to-chip bandwidth demand is likely to jump to 100 Gb/s or more in the near future[8], which could create enormous difficulties even for the latest VLSI microelectronic technology[9-10].The parasitic impedance of copper interconnects is starting to place restrictions on scaling for higher throughputs. Therefore, electrical interconnects and switching speed have been identified as the two major bottlenecks to throughput of computing systems. We cannot take full advantage of the development of high-speed Si and GaAs switching and parallel architecture, unless we can solve the interconnect problem. However, using photons rather than electrons to communicate between chips has the potential advantages of large bandwidth, low crosstalk, and low power consumption[5].

A modern computing system functions by bringing a large number of separate elements to bear on a common problem. Coordinated operations of the elements requires a large amount of communication among them through many long wires. Variability in manufacturing and fluctuation in a system causes the elements of a system to differ from one another in their response to signals. Therefore, signals must be large enough to be interpretable by any element of the system. This means high-power dissipation over a finite length of interconnections. Thus, fitting a complex interconnection pattern into a small space become the most limiting factor in a computer system and the other being the switching speed of an element. Currently, the study of communication and information is aimed at providing the largest bandwidth and lowest power dissipation in a system.

In general, we have been faced with a few fundamental limits unique to a computing system. First, the nature of a computing system which requires more than two streams of information to interact indicate that the times of arrival of information at a device are extremely important. Second, the coding of data streams that allows efficient use of a communication channel capacity cannot be applied to a computer because the methods of information processing through the interaction of two or more streams of coded data are not known yet. Experimentally, the packaging of microelectronics presents an enormous problem for a system designers.

However, deciding between electrical and optical interconnects is a complex task. Although fiber optic transmission techniques have some intrinsic merits, the existing computer architectures are based on electrical interconnects and can seriously limit the application of optical interconnects. In general, insertion of optical interconnects as a direct one-to-one replacement of point-to point electrical interconnects doesn't offer remarkable advantages for current computer systems. This is because: (1) overall system reliability would decrease because of the use of hybrid optical components, (2) overall system power consumption can increase because of the inefficiency of the optical-to-electrical conversion, and (3) increased costs due to the increase in packaging complexity. The cost factor can be offset by higher performance; the high-power consumption can be reduced with sub-milliampere threshold lasers and high quality photodetectors, but the system reliability issue cannot be solved easily. It's therefore desirable to use as few optical interconnects as possible, in the most necessary and effective places. One area where optical interconnects can improve system performance is where large signal fan-outs are required over long distance and at high speeds. High electrical fan-outs are common at the intra-chip and interboard level, including data bus, control lines, and clock lines. If the distance between two elements on a transmission line is much less than the wavelength of the signal, the entire fan-out

system can be viewed as a single transmission line with a load increasing with distance. The impedance of a transmission line is

$$Z = \sqrt{\frac{L}{C}}$$

Where L and C are the inductance and capacitance per unit length. Without fan-out, the unloaded line has an impedance of

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

With loading, the capacitance per unit length is changed to

$$C = \frac{C_0 C_l}{C_0 + C_l}$$

Where $C_0$ and $C_l$ are unloaded and distributed loading capacitance due to fan-outs. And we can get the impedance on the line a distance d away from the starting point

$$Z(d) = \frac{Z_0}{\sqrt{1 + C_{load}/C_0 d}}$$

Where $C_{load}$ is the total load capacitance, d is the transmission line length, $C_0$ is the intrinsic line capacitance. As a result, the driving power has to be increased to maintain a constant signal level. Another effect due to increased fan-out is the propagation delay. Since the velocity of propagation is given by

$$v = \frac{1}{\sqrt{LC}}$$

We have

$$t(d) = t_0 \sqrt{1 + \frac{C_{load}}{C_0 d}}$$

The increase in propagation delay is due to the charging-up of capacitive element at each fan-out. While the increase in driving power is not fundamentally limiting since the driver lines can be designed to carry enough power, the propagation delay decreases the critical line length $l_c$ which is the distance that an electrical signal can travel without causing any signal skew[5,8].

The fundamental difference between electrical and optical fan-outs is that in the case of electrical fan-outs, the signal travels in the media surrounding the transmission line usually made of the ceramic or polyimide circuit board. Whereas, for optical fan-outs, the signal travels in a guided media, the optical fiber or silica waveguide. In an optical fiber, the effect of capacitive loading doesn't exist since no conductor is used. The number of fan-outs for optical interconnects is limited by the available power to the detectors. The amount of power available to the detectors is determined from the source power and the distributed losses throughout the system. Optical fan-out is achieved by power splitting of a channel. The power should be split equally among n detectors. In addition to the distributed loss, there is an excess loss due to the imperfect coupling. Let the sensitivity of detectors used in the system be $P_{min}$, source power be $P_{source}$, the total power loss be; then the maximum number of optical fan-outs can be calculated from

$$P_{source} + \alpha = P_{min}$$

Accordingly, the optical fan-outs can offer a higher fan-out speed since there is no additional propagation delay, and they don't require increased driving power. However, unterminated electrical transmission lines are limited by the critical line length (given the total $C_{load}$ for the entire system, the line length dominates), while terminated transmission lines are limited by the density of fan-out (given the total line length, the per unit length capacitance dominates) along the line. Hence, it's clear from the analysis above that optical interconnects should be used to implement data buses and distribution structures within computing systems

which are currently limited by electrical interconnects.

### 1.4 Heteroepitaxial Growth of III-V compound semiconductors on Si

In order to realize the monolithic integration of III-V material on silicon substrate, high-quality III-V compound buffer layers must be grown on a Si substrate. However, heteroepitaxy between III-V thin films and silicon substrates induces a large strain energy in the thin films. Due to the large lattice and thermal mismatches, this large strain is released by the formation of structural defects and dislocations in the III-V material. Therefore, the density of structural dislocations should be reduced to an acceptable level or even defect-free structures as an ideal goal, since the performance of light emitting devices is deteriorated and is degraded due to the irradiative recombination processes occurring at defect centers. However, structural-defect-free III-V compounds have not been grown on Si substrates by lattice-mismatched heteroepitaxy regardless of a great deal of research.

The key challenges in the heteroepitaxy of semiconductors, relative to the development of useful optoelectronic devices, are the control of the growth morphology, stress and strain introduced by mismatched system and crystal defects. The purpose of this chapter is to review the properties and challenges of the epitaxial integration of III-V semiconductors on silicon substrates that bear on these aspects of heteroepitaxy, including crystallographic properties, elastic properties, surface properties as well as the different types of structural defects.

The term "epitaxial" is applied to a thin film grown atop the crystalline substrate in ordered fashion that atomic arrangement of the thin film accepts crystallographic structure of the substrate. Epitaxial growth is one of the most important techniques to fabricate various "state of the art" optoelectronic devices. Modern devices require very sophisticated structures, which are composed

of thin layers with various compositions. Quality, performance and lifetime of these devices are determined by the purity, structural perfection and homogeneity of the epitaxial layers[11]. Epitaxial crystal growth resulting in epitaxial layer perfection, surface flatness and interface abruptness depend on a number of factors like: the epitaxial layer growth method, the interfacial energy between substrate and epitaxial thin film, as well as the growth parameters - thermodynamic driving force, substrate and layer misfit, substrate misorientation, growth temperature, etc.

Regardless of the growth technique, atoms and molecules are delivered to the substrate surface, and a large fraction of these species adsorb on the surface. Once adsorbed, there are three things that can happen to an adatom. It can either form a strong chemical bond to the surface where it is trapped, diffuse onto the surface to find an energetically preferred location prior to strong chemical bonding or desorb. Once adsorbed chemically, the adatoms can diffuse on the surface and this diffusion can be highly anisotropic, depending on the symmetry and nature of the surface[12]. These adatoms diffuse on the surface till they either desorb from the surface, find another adatom or nucleate to an island, attach or aggregate to an existing island or step, dffuse onto the surface or react at a defect site. Diffusion onto the surface, or interdiffusion can be significant under certain growth conditions[12]. The main surface process that occur during epitaxy are schematically shown in Fig 1.1 with different atomistic processes. The extent of interdiffusion can be thought as solubility of one material into other and clearly has strong dependence on the material system. On the other hand, the reactions at defect site are often important. For example, reactions at step edges (a defect with respect to perfect surface) are the foundation of step-flow growth[11].

The formation of islands and the attachment of atoms to existing structures and clusters are important in the formation of self-assembled islands. When diffusing adatoms impinge on each other, they will nucleate and form an island. Adatoms that directly impinge to on an island can

either incorporate into the island or lead to the next layer growth, depending on the surface potential and energy. As the island continues to grow further and possibly migrate, they can find other islands and coalesce into larger islands[12-13].

Understanding kinetics, thermodynamics and how they interact and compete with each other would enables us to know how to control the growth of thin films. However, in MBE growth, the molecular beams from different sources intersect each other at the substrate surface, where the crystallization processes take place. A series of surface processes take place during MBE growth which are schematically summarized in figure 1.1. The surface processes occurring during MBE growth are characterized by a set of relevant kinetic parameters that describe them quantitatively.

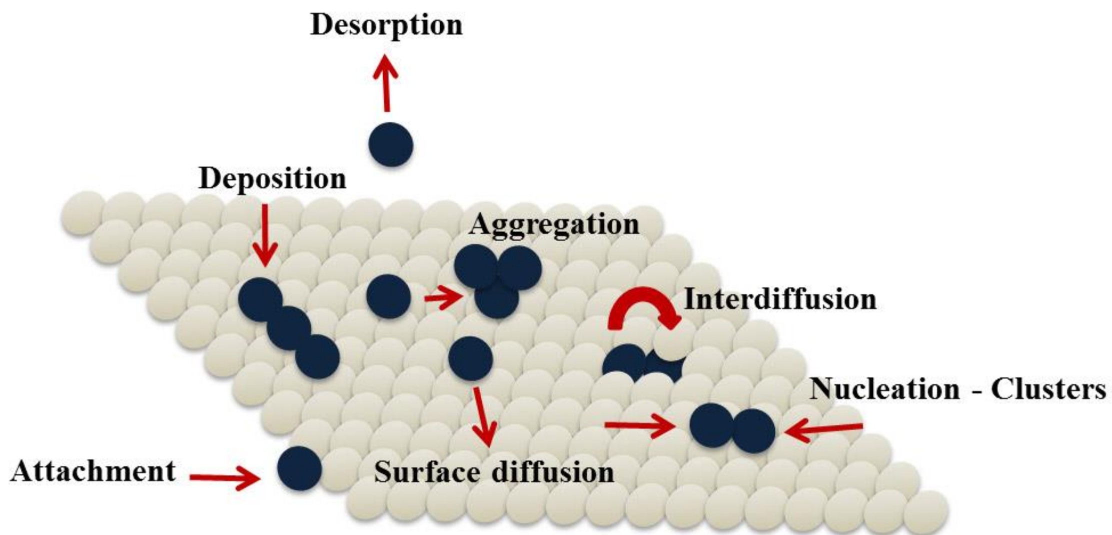



Figure 1.1: A schematic of basic possible processes during epitaxial growth.

The arrival rate is described by the flux of the arriving species and gives the number of atoms impinging on the unit area of the surface per second. Impinging atoms with temperature $T_i$ onto substrate surface, which has temperature $T_s$, usually lower than $T_i$ at different positions are with different kinetics energies. Depending on the atom energy and the position at which it hits the substrate surface, the impinging atom could re-evaporate immediately, carrying with it an energy corresponding to temperature $T_e$ (exchange energy) with atoms of the substrate at $T_s$. A

description of this process is possible by defining the thermal accommodation coefficient $(\alpha)$ as[14]:

$$\alpha = \frac{T_i - T_e}{T_i - T_s}$$

When $T_e$ equals $T_s$ , the accommodation coefficient is unity. Thus, it is a measure of the extent to which whether the adatoms reach the thermal equilibrium with the substrate. Furthermore, the sticking coefficient $(S_c)$is defined as the ratio of the number of atoms which adsorb $(N_{ads})$ or stick to the substrate surface, to the total number of atoms ($(N_{tot})$ that impinge upon substrate surface during the same period of time, and expressed as below[14]:

$$S_c = \frac{N_{ads}}{N_{tot}}$$

In many cases $S_c$ is less than unity and it may be a small fraction in cases when the adsorption energy of atoms on the substrate is low, or the substrate temperature is high. Assuming $\alpha$ is unity, all the impinging atoms are accommodated on the substrate surface and achieve thermodynamic equilibrium. However, this doesn't mean they will stay on the adsorbed sites permanently. The adatoms still have a finite probability related to the substrate temperature of acquiring sufficient energy to overcome the adhesive forces and leave the substrate[14-15]. If aggregation of adatoms doesn't occur, all the adatoms will eventually be re-evaporated. Thus, the $S_c$ could almost be zero even when $\alpha$ is unity. There are two main types of adsorption that can occur during MBE. The first is physical adsorption referring to the case where there is no electron transfer between adsorbate and adsorbent by forming a van der Waal's bond with a surface atom. This type is so-called "physisorption". The second type resulted from forming a covalent or ionic bond with a surface atom, referring to the case with electron transfer, i.e., chemical reaction, taking place between adsorbate and adsorbent. And this is so-called "chemisorption"[13-15].

In addition, the rate at which adatoms are adsorbed to the surface can be described by an

exponential law[15]:

$$R_{ads} \propto v_a e^{-E_{ads}/kT}$$

Where $v_a$ is the adsorption, $E_{ads}$ describes the necessary energy to overcome the electrostatics potential, $k$ is Boltzmann constant and $T$ is the substrate temperature[14-15]. However, most substrates have complicated reconstructions and the bonding is highly directional. Therefore, the probability of adsorption to some sites is higher than other. Assuming defect-free surfaces, a number of theoretical and experimental works has been carried out to find the most stable adsorption sites. Adsorbed atoms may diffuse from one site to another via thermally activated hopping, the diffusion rate which can also be expressed by:

$$D \propto a^2 K_s \propto a^2 e^{-E_d/kT}$$

Where $K_s$ is the site-to-site hoping rate, $K_s$ is the effective hopping distance between sites, $E_d$ is the diffusion energy, and $T$ is the substrate temperature[13, 15-16]. Because of the complicated nature of the most surfaces, diffusion is a complicated process. It should be pointed out that diffusion is the process responsible for the degree of smoothness of the grown film at a fixed growth rate. Furthermore, atoms meet and bond with each other after diffusion forming various size clusters are dependent on the deposition/growth rate.

Another crucial factor is the temperature of the substrate $T$. Increasing the temperature beyond the certain limits leads to desorption of the molecules back into the chamber vacuum. In thermodynamics, the desorption rate increases exponentially and the actual growth rate decreases accordingly.

$$R_{des} \propto f(\theta) e^{-E_{des}/kT}$$

The desorption rate $R_{des}$ is dependent on the degree of coverage $f(\theta)$ and the desorption energy $E_{des}$ [15]. However, the slow growth rates allow the adsorbed molecules to migrate on the substrate to a proper nucleation site for the growth. Notably, nucleation on smooth surfaces is not energetically favored. The most energetically favorable sites are those on terraces and step edges on the growing surface as more chemical bonds tend to bond to neighboring sites at these locations.

Growth parameters like substrate temperature T, growth rate, and the V/III ratio have to be chosen appropriately for the desired application. The V/III ratio has a similar impact on the layer growth as the substrate temperature does. High values shorten the migration length of the group III species because they can more easily find a nucleation sites and then incorporate into the crystals. However, this can also deteriorate the thin film quality due to the tendency of islands formation. On the other hand, the desorption of group III species is counteracted by the higher V/III ratio due to the lower sticking coefficient under the high V/III ratio. Low values, otherwise increase the migration length, but also enhance the probability of desorption. The growth rates are thereby determined by the group III fluxes and the desorption. In the MBE growth, the substrate surfaces are held in UHV chambers while being exposed to molecular beams of the growing material. Meanwhile, the thermodynamics and kinetic factors determine the growth mechanisms. The classical thermodynamic approach to epitaxial thin film growth leads to the definition of the so-called growth modes. This thermodynamics approach is used to determine growth modes of thin films close to equilibrium. The growth mode describes the nucleation and growth processes. Moreover, there is a direct correspondence between the growth mode and the film morphology, which gives the structural properties such as perfection, flatness and interface abruptness of the layers. The kinetic description of growth in which the film morphology is the result of the microscopic path taken by the system during growth. This path is determined by the displacement

rates of the single atom, cluster, or molecule as compared to the deposition, desorption, and dissociation rates. It is determined by the kinetics of the transport and diffusion processes on the surface[13, 16-17].

The competition between the film and substrate surface energies resulting from the growth dynamics and growth conditions determines the growth mode of the epitaxial growth process close to equilibrium. However, the MBE growth process is a kinetically dominated process and thermal equilibrium conditions are only partially fulfilled. Thin films grown by MBE technique are usually not in thermodynamic equilibrium, but kinetically. This is due to the limited surface diffusion, the deposited material cannot completely rearrange itself to minimize the surface energy. The supersaturation of the deposited species leads to a large nucleation rate, and kinetics will lead to the occurrence of different growth modes[15, 17]. Therefore, the behavior of deposited species will be determined by a number of kinetic parameters. Among them, the diffusion coefficient ($D_S$) is probably the most important parameters. It determines the average distance an atom can travel on flat surface before being trapped. This distance is the surface diffusion length ($l_D$) and can be defined by

$$l_D = \sqrt{D_S \tau}$$

Where $\tau$ is the dwelling time before re-evaporation. And the surface diffusion coefficient is generally expressed as[16]:

$$D_S = v a^2 e^{-E_A/kT}$$

Where $E_A$ is the activation energy for diffusion, $v$ is the frequency of diffusion, and $a$ is the characteristic diffusing distance. From the equation above, it is clear that deposition temperature is important because it controls the diffusivity of the adatoms. Therefore, the growth modes in real systems far from equilibrium will be controlled mostly by these kinetic factors and partially by the

thermodynamic factors.

Experimentally, the distinction between three classical growth modes is well known and classified into three growth regimes: Frank-van der Merwe (FM) (layers growth mode), Volmer-Weber (VW) (islands growth mode) and Stranski-Krastonov (SK) (mixed growth mode for layers and islands). The study of the thin film growth typically involves the deposition of a controlled amount of atoms onto a well characterized crystalline substrate at a prescribed set of growth conditions. In the case of Frank-van der Merwe (FM) (layer by layer growth mode): Layer growth is observed when the sum of the binding energy (as known as, the surface energy) for the deposited film/substrate interface and substrate itself is larger than that of the deposited film particles. In this sense, a uniform monolayer of deposited material can form a planar 2D sheet as long as the thin film surface energy is decreased toward the bulk crystal value. Then the layer growth is sustained. However, during FM growth mode, a new layer is nucleated only after the completion of the layer below.

On other hand, while there is no strong bonding between film and substrate, 3D-islands are being formed. The film dose not wet the substrate because this will lead to an increase in the total surface energy. This growth mode is referred to as Volmer-Weber (VW) growth mode. It occurs when the binding force between the particles of the deposited material stronger than the forces between the material and the substrate. In the heteroepitaxial growth, the so-called Stranski-Krastanov (SK) growth mode can also occur. SK mode is considered as the combination between the FM and VW growth modes, and the former growth modes are merged in this case. The layer-to-island growth more results from significant misfit dislocations between the thin film and the substrate. the growth mode changes from layer by layer to island growth. During heteroepitaxial growth, the lattice mismatch between the substrate and the deposited film gives rise to biaxial

strain, resulting in an elastic energy that grows with the increasing layer thickness. Misfit dislocations at or near the film/substrate interface will be formed if the layer thickness exceeds a critical thickness. At this thickness, it is thermodynamically favorable to introduce dislocations because the elastic energy released by the dislocations becomes comparable to the increase in the interfacial energy. In other words, misfit dislocations are necessarily to be introduced to release the strain through defects formation[17].

The concept of monolithically epitaxial integration of III-V compound semiconductors onto Si substrates is not straightforward but very challenging due to the significant differences in basic material and crystal properties that exist between elemental silicon and III-V compounds. Heteroepitaxy differs from homoepitaxy in that it requires the nucleation of a new phase on a foreign substrate. Because of this, the surface chemistry and physics play important roles in determining the properties of heteroepitaxial deposits, including structural and electrical characteristics, defect densities and structure, and the layer morphology[11,15]. However, the heteroepitaxy is classified for three main types based on the lattice constants of the two crystalline materials, lattice-matched heteroepitaxy for the same lattice constants and lattice-mismatched heteroepitaxy but elastically strained like InGaAs on GaAs for different lattice constants, and partially relaxed as in the case of the growth of GaAs on silicon with high misfit dislocation density. The heteroepitaxy process is widely used, not only for research but also for manufacturing semiconductor devices such as lasers, light emitting diodes (LEDs) and transistors.

### 1.5 Challenges of Heteroepitaxial Growth of GaAs on Si

Growing GaAs on Si presents a notable materials problem. There are essentially three difficulties for growing high quality bulk GaAs/Si films. First the 4% lattice mismatch between

GaAs and Si leads to a high dislocation density. While theoretically these dislocations could all be confined at the GaAs/Si interface, in actuality, $10^7 – 10^8$ $cm^{-2}$ dislocations would propagate to the GaAs surface. These dislocations can be modeled as lines of point defects (threading dislocations), and will thus lead to higher number of deep level traps, reduced carrier lifetime, and reduced carrier mobility. Various techniques have been examined to attempt to improve the quality of the GaAs/Si interface, each usually claiming to cause an order of magnitude reduction in dislocation density. These two techniques are universally accepted as useful. The first is increasing the thickness of the buffer layer deposited below the actual device layers. As the buffer GaAs/Si thickness is increased up to several μm thick[18-21], more defects have the chance to annihilate each other, leading to higher quality material and thus higher device performance. The second, and more successful technique to improve the GaAs layer is thermal annealing[22-24]. In-situ and ex-situ techniques have been demonstrated to be effective by a number of groups. The results demonstrated by the groups suggested that thermal cycling combined with in-situ annealing with AlGaAs caps are most effective in removing the dislocations[25-26]. While the literature is unanimous on the improvements produced in GaAs/Si by using thermal cyclic annealing, there is confusion regarding the effects of strained layer superlattices (SLS). SLS are designed to bend dislocations, either to leave the crystal or to react with nearby dislocations. And they are supposed to work better in cooperation with thermal cycling. However, these techniques are not cost-effective and would even complicate the growth procedures.

The second problem is the growth of polar GaAs on the non-polar Si substrates. This can potentially lead to growth of antiphase domain disorders (APDs). At the single-atom steps of the Si surface, antiphase domain boundaries consisting of As-As and Ga-Ga bonds are easily formed. However, misorienting the substrate from (001) axis by a few degrees (typically $2 – 4^o$) will

eliminate the antiphase domains from thick films. The standard model explain the elimination of these domains is the presence of the double-atom steps. However, it is clear from a number of reports[27-28] that the standard cleaning process may actually lead to man-atom supersteps rather than a uniform distribution of double-atom steps. Since GaAs/Si is grown free from antiphase domains using these techniques, it's probable that another mechanism is responsible for the reduction of antiphase domains. self-annihilation is one proposed model[29]. Although the antiphase domain problem has been solved through the use of off-axis substrates, the requirement of using these vicinal substrates may cause problems in the Si devices.

The final problem is the 62% thermal expansion coefficient mismatch between GaAs and Si. This limits the thickness for GaAs/Si lasers and durable LEDs. Since the quality of the GaAs/Si layers improves monotonically as thicker layers are grown, this limit is of more than research importance. It may be that InP and InGaAs layers, despite an even larger lattice mismatch than GaAs, are better suited to heteroepitaxial growth since their thermal expansion coefficients are better matched to Si's. Sapphire substrate on the other hand, are well matched in thermal expansion to GaAs, although GaAs/Si/sapphire material is of poorer quality than GaAs/Si because of the poorer Si on top of the sapphire. The other alternative would be the wafer bonding technique, however, this technique will lead to some mechanical defects at the interface and low-yield in productivity.

Recently, the patterned growth scheme has been demonstrated as an excellent alternative to obtain high quality GaAs and other materials on silicon dioxide ($SiO_2$) patterned Si substrates[30-33]. Most importantly, this growth scheme can effectively mitigate these three major mismatch problems[34-36]. Instead of misoriented (vicinal) Si substrates, this patterned growth approach using exactly Si substrates could also effectively reduce the probability of forming high-density APD

boundaries. Based on the finite size growth nature in the patterned growth scheme, the strain induced by the mismatches in lattice constants and coefficient of thermal expansion will be mitigated remarkably. Hence, the exactly oriented Si substrates was chosen as the starting material in my work to carry out the patterned growth scheme for the III-V to Si integration in the MBE chamber.

**1.6 Dissertation outline**

This dissertation will describe my work based on the patterned growth scheme by MBE to fulfill:

(1) Precise positioning and low defect density selective area epitaxy for self-assembled/catalyst-free GaAs nanodisks on $SiO_2$ masked exactly oriented Si substrates.

(2) High-quality and defect-free GaAs on $SiO_2$ masked exactly oriented Si(111) substrates by a two-step growth technique and its photovoltaic applications.

(3) Integration of InGaAs/GaAs double heterostrucure onto $SiO_2$ masked exactly oriented Si(111) substrates and its optical property characterizations.

# Chapter 2

# Experimental Techniques

## Introduction

This chapter discusses the major experimental techniques used in this study. They are molecular beam epitaxy (MBE), scanning electron microscopy (SEM) and energy dispersive spectrum (EDS), atomic force microscopy (AFM), transmission electron microscopy (TEM), X-ray diffractometry (XRD), photoluminescence (PL) and time-resolved photoluminescence (TRPL).

## 2.1 molecular beam epitaxy (MBE)

The critical experimental apparatus used in this study is the Perkin-Elmer MBE 430 system, as shown in figure 2.1.1. In addition to the main growth chamber with three ultra-high

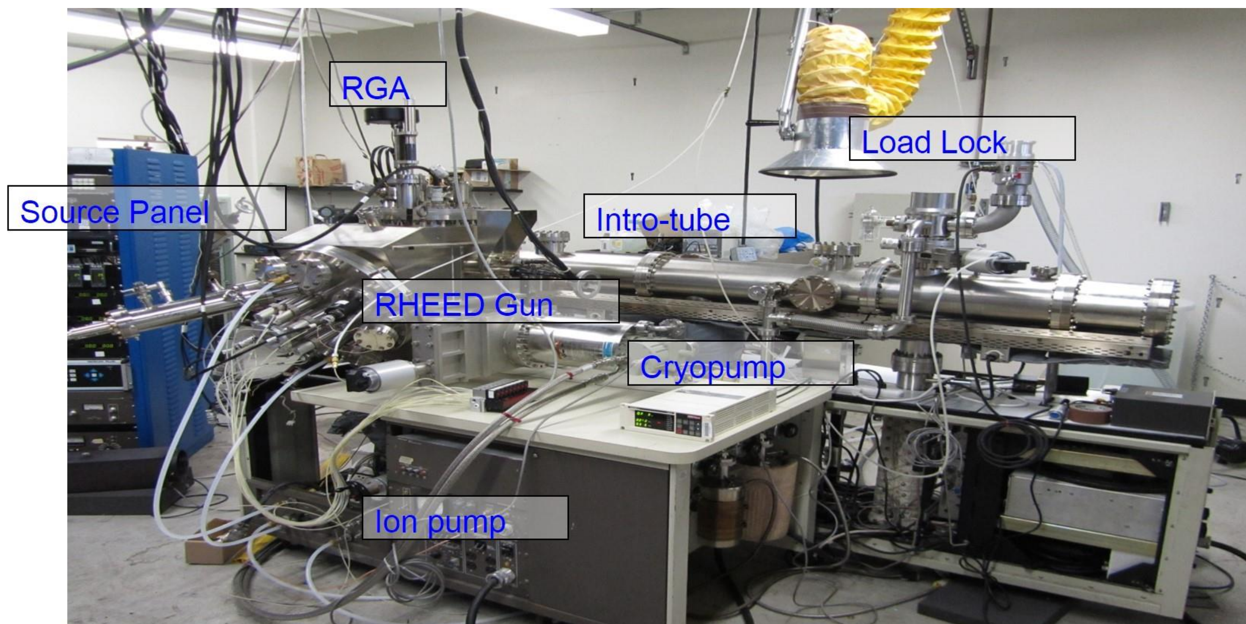



Figure 2.1.1: The picture of Perkin-Elmer MBE 430 system.

vacuum (UHV) pumps – ion pump, titanium sublimation pump and cryo-pump, the key system components include substrate manipulator holding the samples, and the source flange containing

various solid source elemental effusion cells (As, Ga, In, Al, Si and Be as n- and p-type dopants respectively).

The vacuum system consists in a stainless-steel growth chamber, UHV-connected to an intro-tube chamber as shown in the figure 2.1.1, where substrates are degassed prior to growth, and a load-lock chamber for transfer to and from air. All the components of the growth chamber must be able to resist bake-out temperatures of up to 200 ºC for extended periods of time, which are necessary to minimize outgassing from the internal walls. The pumping system must be able to efficiently reduce residual impurities to a minimum. Typical MBE growth rates for III-V type semiconductors are of the order of 1ML/sec, obtained for group III partial pressures of $\sim 10^{-6}$ torr. With atomic densities in the crystal of about $10^{22}$ $cm^{-3}$ meaning that to reduce the impurity concentrations below $10^{15}$ $cm^{-3}$, the impurity partial pressures must be reduced below $\sim 10^{-13}$ torr, assuming a unity sticking coefficient. In practice, base pressure is reduced to the $10^{-11} \sim 10^{-12}$ torr range, with the residual gas being essentially $H_2$. The pumping system usually consists of ion pumps, with auxiliary Ti-sublimation and cryogenic pumps, for the pumping of specific gas species. On the other hand, liquid $N_2$ cryoshroud surround internally both the main chamber wall and the source flange. Since MBE is a cold wall technique, cryoshroud prevent re-evaporation from parts other than the hot cells. Besides, they provide thermal isolation among the different cells, as well as additional pumping for the residual gas.

Effusion cells are the key components of an MBE system, because they must provide excellent flux stability and uniformity, and material purity. Furthermore, being the parts that must withstand the highest temperatures (up to 1400 ºC) for the longest periods, they are often responsible for machine downtime. Therefore a careful choice of elements, materials and geometry must be taken. The cells are placed on a source flange, and are co-focused on the substrate heater,

to optimize flux uniformity. There are four major parts of a cell: (1) The crucible is usually made of pyrolitic boron nitride, which can stand temperatures of up to ~1300ºC without appreciable degassing. Its shape can be cylindrical or conical with different tapering angles, depending on the material to be evaporated. Its size depends on the material to be evaporated as well, and has to be big enough to provide several months of operation before the depletion of the material. (2) Ta filament is in charge of heating, while (3) multiple Ta foils provide heat shielding. (4) A thermocouple is located in an appropriate position in order to measure the material temperature; temperature regulation is provided by high-precision PID regulators. A mechanical or pneumatic shutter, usually made of Ta or Mo, is placed in front of the cell to trigger the flux. The shutters must be operated much faster than the growth rate, and should be computer-controlled to provide reproducible growth cycles, especially for superlattices. Besides, they must be designed not to outgas when heated from the cells, and not to constitute an appreciable heat shield, giving rise to flux transients after opening. An important source type for evaporation of group-V elements is the so-called cracking cell. In this cell, the material is first thermally evaporated (in the form of tetramers) from a large-capacity reservoir; afterwards it passes through a hotter cracking zone in a tube, where molecules are dimerized ($As_4 \rightarrow As_2$).

Speaking of the growth of GaAs, the growth must be performed within a range of substrate temperatures and beam fluxes such that the surface chemistry favors stoichiometric growth. Fortunately, such conditions are well established. For a broad temperature band ranging from below 500 ºC up to ~ 680 ºC, the Ga atoms sticking coefficient onto GaAs is unity, that is, all the Ga atoms impinging upon the GaAs surface will stick). Whereas at these substrate temperatures, the As-As bond is unstable so that As will only bond to Ga. If the beam flux ratio is excessive such that As flux is much greater than Ga flux, stoichiometric GaAs is achieved, since the As flux in

excess of Ga flux will not stick. The growing crystal arranges itself into its lowest energy state which is the desired stoichiometric GaAs zincblende crystal structure. In practice, a flux ratio ~10:1 (As : Ga) is usually used for MBE growth. Much higher ratios lead to higher defect density, whereas lower flux ratios may lead to a Ga-rich film. As far as substrate temperature goes, the highest temperature feasible (limited by Ga desorption) is usually the best, as this limits the incorporation of impurity atoms into the film. The exception to these rules is in the case of heavy doping Be doping, where a lower temperature and higher As flux is usually used to combat the tendency of Be to diffuse rapidly in GaAs. Furthermore, since Ga atom has unity sticking coefficient, the growth rate can be directly calculated from the Ga flux and is directly proportional to the Ga flux.

MBE is as much a surface science technique as it is a growth technique. The UHV nature of MBE provides extremely clean, atomically abrupt surfaces which can be probed by a variety of electron beam techniques. Chief among these is reflection high energy electron diffraction (RHEED). RHEED is a glancing angle electron diffraction technique whose diffraction patterns reflect primarily the surface periodicity due to the shallow beam angle. If electrons interact only with the first atomic layer of a perfectly flat and ordered surface, the three-dimensional reciprocal lattice points degenerate into parallel infinite rods. In the resulting Ewald construction the intersection of the Ewald sphere (with a radius much larger than the inter-rod spacing for typical RHEED energies) consists therefore of a series of points placed on a half circle. In reality, thermal vibrations and lattice imperfections cause the reciprocal lattice rods to have a finite thickness, while the Ewald sphere itself has some finite thickness, due to divergence and dispersion of the electron beam. Therefore, even diffraction from a perfectly flat surface results in a diffraction pattern consisting in a series of streaks with modulated intensity, rather than points. If the surface is not flat, many electrons will be transmitted through surface asperities and scattered in different directions, resulting in a RHEED pattern

constituted by many spotty features. Therefore, a first important information provided by RHEED regards the flatness of a surface. Furthermore, it is evident that diffraction from an amorphous surface (such as an oxide on top of a semiconductor) gives no diffraction pattern at all, and only a diffuse background will result. This is important, for example, for evaluating oxide desorption when a new substrate is initially heated up prior to growth in the MBE chamber, exposing the underlying, crystalline semiconductor surface.

## 2.2 scanning electron microscope (SEM) and energy dispersive spectrum (EDS)

SEM is basically a mechanism for a scanning electron beam across a sample in a controlled manner (area, beam diameter, resolution). An electron beam incident on the sample produces an image while in the field emission microscope the specimen itself is the source of electrons. The interaction of an electron beam with a solid can lead to the ejection of loosely bound electrons from the conduction band. These are the secondary electrons with energies below around 50 eV. The standard SEM mode is imaging the secondary electron signal, since the secondary electron are largely emitted from a region relatively near the surface. An SEM consists of an electron gun, a lens system, scanning coils, and an electron collector. The electron energy is typically about 10-30 keV for most samples, but for insulating samples the energy can be as low as several hundred eV. The use of electrons has two advantages over optical microscopes: much larger magnifications are possible since electron wavelengths are much smaller than photon wavelengths and the depth of field is much higher.

Characteristic X-rays result from electron transitions between inner orbits, which are normally full. An electron must first be removed in order to create a vacancy into which another can 'fall' from an orbit further out. In electron probe analysis vacancies are produced by electron

bombardment, which also applies to X-ray analysis in the TEM. EDS makes use of the X-ray spectrum emitted by a solid sample bombarded with a focused beam of electrons to obtain a localized chemical analysis. All elements from atomic number 4 (Be) to 92 (U) can be detected in principle, though not all instruments are equipped for 'light' elements ($Z < 10$). Qualitative analysis involves the identification of the lines in the spectrum and is fairly straightforward owing to the simplicity of X-ray spectra. Quantitative analysis (determination of the concentrations of the elements present) entails measuring line intensities for each element in the sample and for the same elements in calibration Standards of known composition. By scanning the beam in a television-like raster and displaying the intensity of a selected X-ray line, element distribution images or 'maps' can be produced. Also, images produced by electrons collected from the sample reveal surface topography or mean atomic number differences according to the mode selected. The SEM which is closely related to the electron probe, is designed primarily for producing electron images, but can also be used for element mapping, and even point analysis, if an X-ray spectrometer is added. There is thus a considerable overlap in the functions of these instruments.

### 2.3 atomic force microscopy (AFM)

AFM is essentially ultra-sensitive surface profilometer. Using piezoelectric positioning gears and near-atomically sharp tips, AFM can provide vertical resolution of a few tens of angstroms and lateral resolution of fractions of micron. AFM has been used to identify characteristic surface morphology features as well as yielding root-mean-square (RMS) roughness values. With respect to RMS roughness, it should be noted that this value is somewhat area dependent (averaging over larger areas usually slightly increases the RMS roughness). Also, RMS roughness can be misleading if the surface contains, for example, a limited distribution of narrow

but deep pits. Nonetheless, RMS roughness provides a measure of the surface smoothness or roughness which allows sample-to-sample comparison. In these studies, AFM was also used to characterize antiphase domains and threading dislocations, both of which produce identifiable surface features.

## 2.4 transmission electron microscopy (TEM)

TEM is the electron beam analogous to optical microscopy of thin, transparent samples. Imaging may be done in either cross-section or plan-view modes, dependent on sample preparation. The electron beam transparency requirement demands sample thickness of order 200 nm or les, requiring a complex sample preparation process involving polishing, grinding, and ultimately ion milling to produce the final thinned sample. Cross-sectional TEM further requires gluing together a stack of wafers with the desired interface at the center, which is then processed similarly to plan-view samples. For cross-sectional samples it is essential to ion mill (mostly by focused ion beam) centered on the target interface in order to image it.

The tediousness of TEM sample preparation is offset by the wealth of information which can be obtained. TEM can image dislocations, antiphase domains, stacking faults, interface roughness, and other crystallographic defects, and provide extensive information about each, including dislocation burgers vectors, domain orientations, etc. TEM can provide statistically accurate threading dislocation densities for values above about $10^7$ $cm^{-2}$, where etch pit density measurements become inaccurate. Below this level, however, TEM becomes inaccurate due to the excessive number of imaging areas required to assess these low densities, for which typically less than one dislocation per field of view is observed. TEM can also distinguish individual layers in a multi-layer structure if there is sufficient electron scattering contrast. Practically, this usually

means that compositional differences are observable, but not doping differences. Noticeably both plan-view and cross-sectional imaging is necessary in order to unambiguously identify all defects. In particular, the misfit dislocations are only imaged in plan-view since they do not extend far beyond the interface between the epi-layers and the substrates.

### 2.5 X-ray diffractometry (XRD)

X-rays primarily interact with electrons in atoms. When x-ray photons collide with electrons, some photons from the incident beam will be deflected away from the direction where they original travel, much like billiard balls bouncing off one another. If the wavelength of these scattered x-rays did not change (meaning that x-ray photons did not lose any energy), the process is called elastic scattering (Thompson Scattering) in that only momentum has been transferred in the scattering process. These are the x-rays that we measure in diffraction experiments, as the scattered x-rays carry information about the electron distribution in materials. On the other hand, In the inelastic scattering process (Compton Scattering), x-rays transfer some of their energy to the electrons and the scattered x-rays will have different wavelength than the incident x-rays.

Diffracted waves from different atoms can interfere with each other and the resultant intensity distribution is strongly modulated by this interaction. If the atoms are arranged in a periodic fashion, as in crystals, the diffracted waves will consist of sharp interference maxima (peaks) with the same symmetry as in the distribution of atoms. Measuring the diffraction pattern therefore allows us to deduce the distribution of atoms in a material.

The peaks in a x-ray diffraction pattern are directly related to the atomic distances. Let us consider an incident x-ray beam interacting with the atoms arranged in a periodic manner as shown in 2 dimensions in the following illustrations. The atoms, represented as green spheres in the graph,

can be viewed as forming different sets of planes in the crystal. For a given set of lattice plane with an inter-plane distance of d, the condition for a diffraction (peak) to occur can be simply written as

$$2d \sin \theta = n\lambda$$

which is known as the Bragg's law, after W.L. Bragg, who first proposed it. In the equation, $\lambda$ is the wavelength of the x-ray, $\theta$ is the scattering angle, and n is an integer representing the order of the diffraction peak. The Bragg's Law is one of most important laws used for interpreting x-ray diffraction data. It is important to point out that although we have used atoms as scattering points in this example, Bragg's Law applies to scattering centers consisting of any periodic distribution of electron density.

Powder XRDis perhaps the most widely used x-ray diffraction technique for characterizing materials. As the name suggests, the sample is usually in a powdery form, consisting of fine grains of single crystalline material to be studied. The technique is used also widely for studying particles in liquid suspensions or polycrystalline solids (bulk or thin film materials). The term powder really means that the crytalline domains are randomly oriented in the sample. Therefore when the 2-D diffraction pattern is recorded, it shows concentric rings of scattering peaks corresponding to the various d spacings in the crystal lattice. The positions and the intensities of the peaks are used for identifying the underlying structure (or phase) of the material. Generally speaking thin film diffraction refers not to a specific technique but rather a collection of XRD techniques used to characterize thin film samples grown on substrates. These materials have important technological applications in microelectronic and optoelectronic devices, where high quality epitaxial films are critical for device performance. Thin film diffraction methods are used as important process development and control tools, as hard x-rays can penetrate through the epitaxial layers and

measure the properties of both the film and the substrate.

Basic XRD measurements made on thin film samples include:

- Precise lattice constants measurements derived from ω-2θ scans, which provide information about lattice mismatch between the film and the substrate and therefore is indicative of strain & stress
- Rocking curve measurements made by doing a ω scan at a fixed 2θ angle, the width of which is inversely proportionally to the dislocation density in the film and is therefore used as a gauge of the quality of the film.
- Superlattice measurements in multilayered heteroepitaxial structures, which manifest as satellite peaks surrounding the main diffraction peak from the film. Film thickness and quality can be deduced from the data.
- Glancing incidence x-ray reflectivity measurements, which can determine the thickness, roughness, and density of the film. This technique does not require crystalline film and works even with amorphous materials.

## 2.6 photoluminescence (PL) and time-resolved photoluminescence (TRPL)

The phenomena which involve absorption of energy and subsequent emission of light are classified generically under the term luminescence. Phosphors are luminescent materials that emit light when excited by radiation, and are usually microcrystalline powders or thin-films designed to provide visible color emission. Excitation by absorbance of a photon leads to a major class of technically important luminescent species which fluoresce or phosphoresce. In general, fluorescence is “fast” (ns time scale) while phosphorescence is “slow” (longer time scale, up to hours or even days). The absorption of energy, which is used to excite the luminescence, takes

place by either the host lattice or by intentionally doped impurities. In most cases, the emission takes place on the impurity ions, which, when they also generate the desired emission, are called activator ions. When the activator ions show too weak an absorption, a second kind of impurities can be added (sensitizers), which absorb the energy and subsequently transfer the energy to the activators. This process involves transport of energy through the luminescent materials. Quite frequently, the emission color can be adjusted by choosing the proper impurity ion, without changing the host lattice in which the impurity ions are incorporated. On the other hand, quite a few activator ions show emission spectra with emission at spectral positions which are hardly influenced by their chemical environment. This is especially true for many of the rare-earth ions. Generally, luminescence of phosphors involves two processes: excitation and emission. Many types of energy can excite the phosphors. Excitation by means of energetic electrons is cathodoluminescence (CL). PL occurs when excited by photons, electroluminescence (EL) is excited by an electric voltage, chemiluminescence is excited by the energy of a chemical reaction, and so on. The process of emission is a release of energy in the form of photon. In the host lattice with activator, the activator is directly excited by incoming energy; the electron on it absorbs energy and is raised to an excited state. The excited state returns to the ground state by emission of radiation.

PL is a basically a measurement in which electron-hole pairs are photogenerated, typically by a laser beam whose photo energy is well above bandgap, and the resultant luminescence produced by radiative decay is measured spectrographically. TRPL is a variant whereby only a single luminescence wavelength is temporally monitored after the photoexcitation source is abruptly cut off. The decay transient as the original equilibrium illuminated minority carrier concentration decays through recombination is measured. The TRPL transient thus will be a

measure of those material or heterostructure parameters which control the rate of recombination. For a very thick film under low-level injection where photogeneration is deep (i.e. far from the surface or epi-layer/substrate interface) the TRPL decay will simply reflect the bulk lifetime. Such measurement is often impractical, however, since the above-bandgap excitation will be absorbed near the sample surface, so that the decay rate will be dominated by recombination at the typically very high density of surface states. TRPL dacay lifetime can be related to the bulk minority carrier lifetime as[37]:

$$\frac{1}{\tau_{TRPL}} = \frac{1}{\tau_P} + \frac{2S}{d}$$

Where $\tau_{TRPL}$ is the TRPL decay lifetime, $\tau_P$ is the bulk minority lifetime, $S$ is the interface recombination velocity, and $d$ is the epi-layer thickness. TRPL provides a simple, non-destructive means of evaluating the minority carrier recombination velocity and the interface recombination velocity, both of which are critical parameters for designing lasers, LEDs, and solar cells such minority carrier devices.

# Chapter 3

# Experimental Results

## 3.1 Precise positioning and low defect density selective area epitaxy for self-assembled/catalyst-free GaAs nanodisks on $SiO_2$ masked exactly oriented Si substrates.

This section is focused on the structural and optical characterizations of self-assembled/catalyst-free GaAs nanodisks on $SiO_2$ masked Si(100) patterned substrates by molecular beam epitaxial growth. Pure zincblende GaAs nanodisks with precise positioning and low defect density are demonstrated by selective area epitaxy. The influence of the growth temperature and deposition duration is investigated. Excellent morphological and structural properties are characterized by scanning electron microscopy and cross-sectional transmission electron microscopy. Defects in the epilayers are reduced by strain relaxation through facets formation and by a lateral overgrowth scheme atop the $SiO_2$ mask which is corroborated by micro-Raman spectroscopy. In particular, I show how the material quality contributes to excellent optical properties observed by micro-photoluminescence spectroscopy from 77 K to room temperature.

### 3.1.1 INTRODUCTION

III-V nanostrcutures including nanowires, quantum dots, etc. are key enablers for nanotechnologies and some achievements have already been demonstrated in nanoelectronics[38], nanophotonics[39], biosensors[40-41], and so on. The inherent merits of III-V nanostructures in high electron mobilities, direct bandgaps, and vast possibilities of bandgap engineering are the main reasons to make the III-V nanostructures sought-after. Such high quality III-V epitaxial

nanostructures can be easily obtained through homoepitaxy by molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD), or chemical beam epitaxy (CBE). However, it's desirable to have such high quality III-V nanostructures integrated to the cost-effective and complementary metal oxide semiconductor (CMOS) compatible Si platform. In fact, successful heteroepitaxial growth will not only provide high carrier mobility and direct bandgap III-V materials, but also maintain the advantages of lightweight and low-cost Si substrates with high mechanical strength and excellent thermal management. To date, researchers have extensively focused on the growth of high quality III-V compounds on Si and tried to accomplish the so-called bottom-up integration. Due to the mismatches in lattice constants, thermal expansion coefficients, and polar/nonpolar nature, the misfit dislocations, threading dislocations, and antipase domain boundaries (APB) are generated which results in tremendous degradation of the device electrical and optical properties. Although various growth schemes such as complex thermal cycle annealing process [42-44], strained layer superlattice (SLS) buffer layers[45], micron-thick graded buffer layers[46], microchannel epitaxy[47] (MCE), flow-rate modulation epitaxy (FME), and migration-enhanced epitaxy[48-49] have been developed, they still haven't efficiently elimintated the aforementioned defects. More remarkably, these defects play key roles to hinder the possibility to realize the high-efficieny minority carrier devices like light emitting diodes (LEDs), laser diodes (LDs), and avalanche photodiodes (APD) on Si.

In this context, I investigate our growth of self-assembled/catalyst-free GaAs nanodisks on top of $SiO_2$ masked Si(100) patterned substrates by molecular beam epitaxy. With the assist of the selective area epitaxy (SAE) on patterned substrates, the stress is laterally relaxed through the top facet and side wall formation, leading to nearly defect-free GaAs nanodisks. Most importantly, this growth scheme can effectively mitigate the major mismatch problems based on the finite size

growth condition. The finite size growth leads to the reduction in the thermal stress at GaAs/Si interface, therefore minimizing the formation of threading dislocations and stacking faults penetrating into the epilayers. Furthermore, instead of using misoriented Si substrates, this SAE approach using nominal Si(100) substrates could also effectively reduce the probability of forming high-density APBs. On top of that, (100) oriented substrate is compatible with the mainstream CMOS technology which enables us to fulfill the genuine III-V to Si platform integration. In addition to all these obvious advantages, the SAE growth technique eliminates the need for patterning post-growth mesas, while the $SiO_2$ sidewalls can automatically serve as a lateral electrical isolation. As for the catalyst-free growth mechanism for our GaAs nanodisks, the lack of seed particles avoids the diffusion of the seed on/into Si and forbids the creation of detrimental deep level traps or scattering centers in GaAs and Si. In this way, the merit enables the viable pathway to integrate three dimensional based GaAs nanostructure devices to Si-based processes and electronics. I hereby report the selectively grown GaAs nanodisks on Si(100) substrates with a substantially reduced number of defects. The key influences of the growth temperature and deposition duration are investigated. The precise positioning process were defined using hole arrays with thermally grown $SiO_2$ on Si(100) substrates. Rectangular GaAs nanodisks with superior material quality were formed due to the strain relaxation through facets and lateral overgrowth. Cross-sectional transmission electron microscopy investigation reveals the single crystalline zincblende structure and the reduced number of stacking faults and dislocations. Micro-Raman spectroscopy indicates the GaAs nanodisks crystallinity changes from polycrystal-dominant to single crystal-dominant structure from the growth temperature at 550 °C to 630 °C. Besides, the strong direct band-to-band transition in optical properties from micro-photoluminescence spectroscopy measurements demonstrates the catalyst-free growth mechanism

successfully circumvent the incorporation of such mid-gap trap centers.

### 3.1.2 EXPERIMENTAL DETAILS

Firstly, a 60-nm-thick $SiO_2$ was thermally grown on Si(100) substrates. Arrays of circular holes with a diameter of 1 μm were defined by stepper lithography followed by the subsequent inductive coupled plasma reactive ion etching (ICP-RIE) of the top $SiO_2$ layer. Prior to the growth, the patterned substrates are chemically cleaned. They were degreased sequentially in acetone, isopropyl alcohol with ultrasonic agitation, and treated in 30% KOH for 20 seconds at room temperature to remove the RIE damaged Si surface and expose a fresh Si surface in the patterned holes. Then, the patterned substrates were cleaned by piranha solution ($H_2SO_4$:$H_2O_2$=1:3) for 3 minutes at room temperature. Immediately prior to loading the patterned substrates to the MBE loadlock, a 30-seconds dip in 5% diluted HF solution was done to remove the native oxide on the exposed silicon surface and achieve hydrogen passivation, then rinsed in deionized water for 1 minute and blown dry with nitrogen. The cleaned samples were further degassed at 400 °C for 10 minutes in the buffer tube of our Perkin-Elmer 430 MBE system prior to loading into the growth chamber. Afterwards, the thermal treatment was applied at 900 °C for 10 minutes in the MBE growth chamber to desorb residual native oxides, which might have formed during the loading, and to make the surface hydrogen-free. In order to enable growth runs start with the most stable growth condition, all of the growth runs were initiated exposing the patterned substrates under the $As_2$ overpressure for 5 minutes to turn the exposed Si surface inside the patterned circular holes into the As-terminated one. Subsequently, the growth of high quality GaAs layers on Si was performed under an $As_2$ beam equivalent pressure (BEP) around $2 \times 10^{-6}$ torr. Thermocouple and pyrometer were simultaneously used to measure the growth temperature. The two-dimensional

(2D) equivalent growth rates and V/III ratios were calculated and calibrated by reflection high energy electron diffraction (RHEED) similar to GaAs homoepitaxy.

I initiated the growth by depositing a low temperature grown 25 nm-thick GaAs layer at 400 °C to reduce the unintentional doping effect from the Si atoms in the substrates. Followed by this stage, the growth of self-assembled/catalyst-free GaAs nanodisks then thereby started. The growth temperature dependent experiments were carried out from 550 °C to 630 °C with the V/III ratio at 10 to investigate the optimal growth temperature for SAE to take place. The As and Ga shutters were then simultaneously opened to initiate growth. The growth condition is similar to that of GaAs homoepitaxy with a Ga flux planar growth rate of 1 Å/s. After deposition of nominal 1 μm-thick GaAs, the growth was terminated. It was found that a growth temperature of 630 °C yields the best selectivity and crystal quality. Therefore, the time evolution study was also performed at this growth temperature to investigate the morphology change in each stage from the growth duration of 30 minutes to 120 minutes.

The morphology of as-grown GaAs nanodisks was evaluated by scanning electron microscopy (SEM, JEOL, JSM-6700F, operated at 10 KV). The structural and crystalline quality were further investigated by cross-sectional transmission electron microscopy (XTEM, JEOL, JEM-3000F, operated at 300 KV). In addition, the micro-Raman spectroscopy (Renishaw Raman microscope) was performed at room temperature by using a 532 nm excitation laser. Finally, the temperature dependent micro-photoluminescence (PL) spectroscopy was performed under the excitation of 488 nm line Ar-ion laser at the power density of 6 W/cm$^2$, and the PL signal were detected by liquid-nitrogen cooled InGaAs detector.

### 3.1.3. RESULTS AND DISCUSSION

*A. Catalyst-Free and Selective Area Epitaxy Growth Mechanisms*

In the GaAs/Si low-dimensional nanostructures heteroexpitaxy, one should consider not only the conventional problems relating to the major mismatches mentioned earlier, but also the following two questions: unintentional doping from the Si substrate, and misfit dislocation at the heterointerface. In the traditional vapor-liquid-solid (VLS) growth of nanostructures, the seed catalysts usually corrosively etch the Si surface and release Si atoms which can diffuse into the epilayers[50]. For the catalyst-free growth, Si can also diffuse into GaAs epilayers because of the high growth temperatures required for the growth. This unintentional doping from the Si substrate is viewed to form a gradual carrier distribution layer inside the GaAs epilayers. In such a case, highly doped *n*-type layers may form close to the heterointerface resulting from the unintentional doping degrading the performance in GaAs nanostructures. Therefore, it is significant to suppress the unintentional doping. Although there have not been found the most effective and guaranteed way to suppress this kind of doping. It is believed a low-temperature grown buffer layer could probably suppress the unintentional doping. Therefore, the growth was initiated by depositing a 25 nm-thick GaAs layer at 400 °C prior to the self-assembled/catalyst-free GaAs nanodisks. On the other hand, the intrinsically lattice-mismatched system usually introduces misfit dislocations at the heterointerface. However, these misfit dislocations could be effectively reduced by shrinking the contact area of the GaAs epilayer to the Si surface. Obviously, this is the advantage of the finite size SAE applying to this study. In SAE, the growth is constrained in certain areas of a substrate, i.e. the one-dimensional (1D) growth is enhanced by suppressing the 2D growth.

The growth mechanism is schematically drawn in figure 3.1.1. Basically, a Si substrate is covered by an amorphous $SiO_2$ thin film patterned with micro- or nano-scale windows. Then, the growth conditions are chosen such that the sticking coefficients of the As and Ga adatoms are zero

on $SiO_2$ and nonzero in the hole arrays, i.e. the exposed Si surface[51]. The purpose of SAE is to constrain the incorporation of group-III adatoms to certain areas on a patterned substrate. In fact, there are mainly two contributions that influence this growth mechanism: (1) diffusion of adatoms from $SiO_2$ to the exposed Si surface, and (2) preferential desorption of adatoms on $SiO_2$ relative to the Si surface.

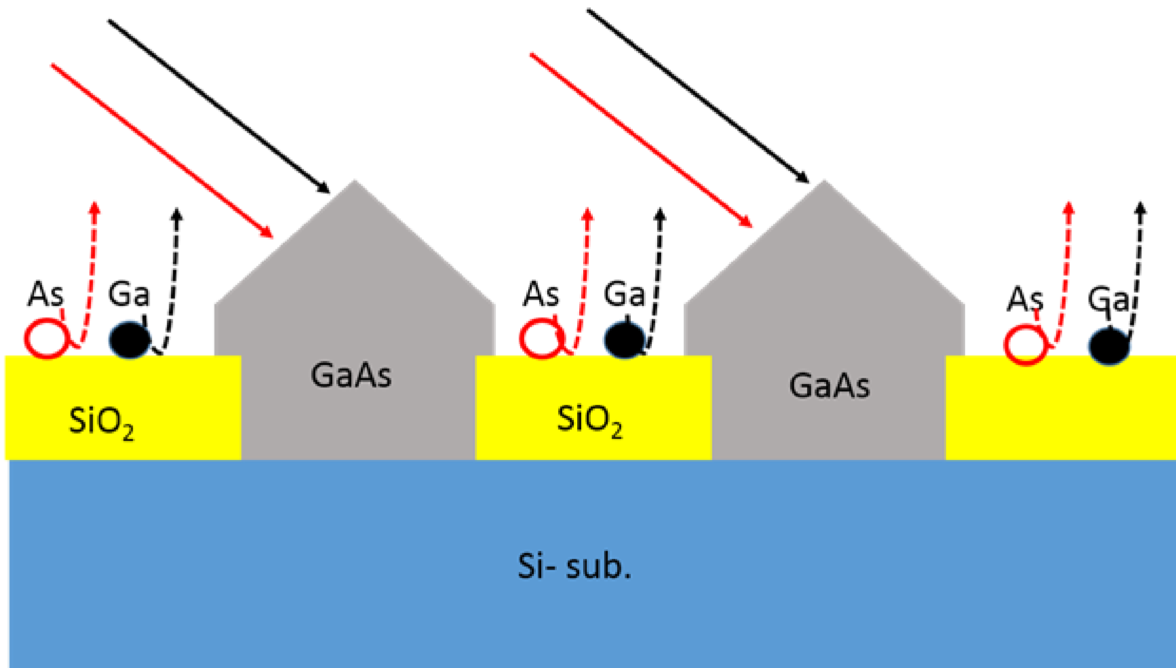


Figure 3.1.1: The schematic of growth mechanism for selective area epitaxy (SAE) displaying the diffusion and desorption of Ga/As adatoms atop the $SiO_2$ mask.

These two contributions to SAE are discussed theoretically as follows:

***1. Diffusion of adatoms from the oxide***

Based on the different lifetimes of adatoms before incorporation in a film or desorption from the substrate, there exists a concentration gradient over the edge between exposed Si surface and $SiO_2$. This gradient results in a net diffusion of Ga from $SiO_2$ to the exposed Si surface. Invoking the second Fick's law, we can describe the surface diffusion in the following differential equation[52]:

$$\frac{d\sigma}{dt} = D\left(\frac{d^2\sigma}{dx^2} + \frac{d^2\sigma}{dy^2}\right) - \frac{\sigma}{\tau} + R$$

with $\sigma(x,y)$ being the surface density of adsorbed Ga atoms at a point on the 2D surface, $D(x,y)$ the coefficient of surface diffusion, $\tau(x,y)$ the lifetime of Ga adatoms on the surface and $R$ the incoming beam flux. This equation is now solved using necessary boundary conditions for periodic hole arrays in a $SiO_2$ layer with a hole pitch $d$. Then the resulting $\sigma$ is averaged over a hole which would be proportional to the average nanostructure height. Unfortunately solving this approach would most likely require numerical methods. The surface lifetime $\tau$ of Ga adatoms is determined by the lifetime $\tau_i$ for incorporation into the surface and $\tau_d$ for desorption from the substrate. $\tau$ can be calculated from $\tau_i$ and $\tau_d$ according to Matthiessen's rule[53]:

$$\frac{1}{\tau(x,y)} = \frac{1}{\tau_i(x,y)} + \frac{1}{\tau_d(x,y)}$$

Therefore, we now consider some approximations to get an analytical solution. Due to the radial symmetry of the holes, the concentration gradient at a position is assumed to be a point towards the center of the nearest neighboring Si hole. The diffusive transport on the oxide is characterized by a diffusion length $L_D$ which is the scale where only a $1/e$ fraction of the diffusive particles remain as the rest have desorbed from or incorporated to the substrate after this distance. Incorporation of Ga onto the oxide is neglected as this is not a significant effect in the selective growth regime. Meanwhile, the incorporation of atoms into the GaAs layer is considered to happen homogeneously over the exposed Si surface and at a high efficiency.

***2. Desorption of adatoms on the oxide***

The second contribution to selective growth results from a higher volatility of Ga and As

adatoms on $SiO_2$ with respect to Si surfaces. The reason of this volatility is that the sticking coefficient of Ga and As adatoms on the $SiO_2$ surface is reduced with respect to the sticking probability on the GaAs surface because of less favorable binding sites. In particular, this also means that the growth of GaAs on the surface of the oxide also depends strongly on the existence of nucleation centers where diffusing Ga atoms become attached. In experimental situations the sticking coefficient on $SiO_2$ is not completely zero eventually leading to the growth of polycrystalline GaAs on the oxide. Assuming quasi-equilibrium conditions, the equation describing the maximum critical flux of impinging atoms leading to zero-deposition of GaAs on the $SiO_2$ surface is[54]:

$$J_c \propto \frac{v_0^2}{4D_0} e^{-(2E_{Des} - E_{Diff})/k_B T}$$

with $v_0$ being the desorption rate constant, $D_0$ the diffusion constant, $E_{\text{Diff}}$ the activation energy for diffusion and $E_{\text{Des}}$ the activation energy for desorption, $J_{\text{C}}$ is the critical flux for a given temperature $T$, below which zero-deposition occurs. As commonly $2E_{\text{Des}} - E_{\text{diff}} > 0$ in thin film growth, zero-deposition on the oxide is available by either increasing the growth temperature $T$ at a given Ga-flux $J_{\text{Ga}}$ or by decreasing the Ga-flux (deposition rate) $J_{\text{Ga}}$ at a given temperature $T$[55].

### *B. Experimental Results*

In order to investigate the mechanism of SAE, the growth-temperature dependent study were carried out to understand the process of diffusion and desorption of Ga and As adatoms with respect to the exposed Si surface. Figure 3.1.2 shows three SEM micrographs of GaAs grown on patterned Si(100) substrates at growth temperatures ranging from 550 °C to 630 °C. The nominal deposition thickness is fixed at 1 μm for all of the growth runs. When the temperature is set at 550

°C as shown in Figure 3.1.2 (a), almost no selectivity is observed and the deposited GaAs exhibits amorphous or polycrystalline crystallites. As the temperature is increased to 600 °C as displayed in figure 3.1.2 (b), rectangular crystals are formed at the patterned hole arrays sites, showing enhanced material quality with some top facets. Nevertheless, the selectivity is not as perfect as GaAs can still be seen on the $SiO_2$ surface and some agglomeration of GaAs crystallites between different pattern holes.

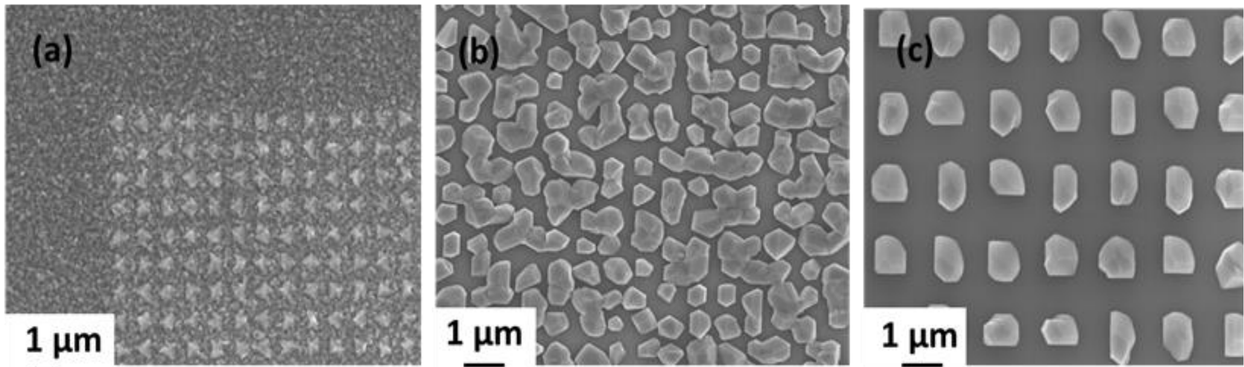


Figure 3.1.2: SEM images of growth temperature dependent study for SAE grown GaAs nanodisks on Si(100) patterned substrates at (a) 550 °C, (b) 600 °C, and (c) 630 °C.

The complete selective growth is achieved at 630 °C as can be seen in figure 3.1.2 (c). GaAs nanodisks preferentially fill the patterned holes to form the nanodisk arrays. Each individual nanodisk, as shown in figure 3.1.2 (c), has lateral dimensions of ~1 µm as it fully covers the exposed Si surface. Faceting is very evident at this temperature, indicating single crystalline growth, although defects can still be observed on some of the crystals. It is noticeable that growth temperature significantly affects selectivity and material quality through adatom kinetics. A proper growth temperature of 630 °C is crucial to achieve the high material quality and the selective growth. However, when the substrate temperature is above 650°C, the strong desorption of the selectively grown nanodisks predominates and no material is seen on either the exposed silicon

surface or $SiO_2$. Otherwise, at low temperatures, selectivity becomes poor as polycrystalline GaAs crystallites were deposited both in the holes and on the mask surface as displayed in Figure 3.1.2 (a). The reason for the poor selectivity is because the diffusion length of Ga as well as the decomposition rate of GaAs on $SiO_2$ becomes much less than the higher temperature cases. Consequently, nucleation occurs on both of the patterned hole arrays and the mask. Furthermore, inside the patterned holes, the density of GaAs nucleation sites increases as a result of the decreased Ga diffusion length on Si surface. Coalescence of these nucleated crystals then results in a high density of defects. Therefore, the growth temperature of 630 °C is the optimized growth temperature.

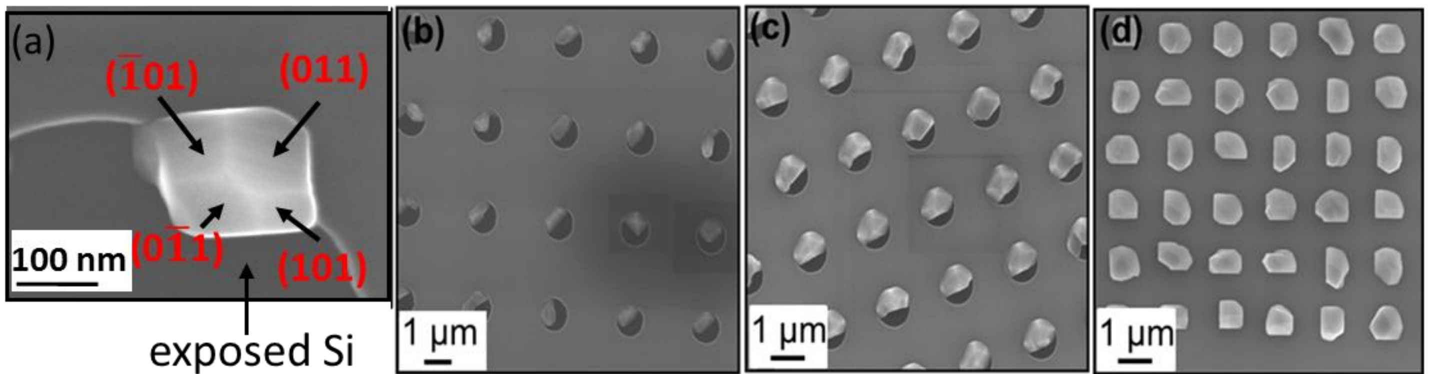



Figure 3.1.3: SEM images of time evolution study for SAE grown GaAs nanodisks on Si(100) patterned substrates for (a) 30 mins, (b) 60 mins, (c) 90 mins, and (d) 120 mins.

On the other hand, in order to understand the morphological change in each growth stage, the time evolution growth study was also performed at 630 °C from the deposition duration of 30 minutes to 120 minutes as displayed in figure 3.1.3. As can be seen in figure 3.1.3 (a), the growth initiated from one particular nucleation site, i.e. mostly on the edge of $SiO_2$, and then in the following stages to expand to fill the complete hole region to form the nanodisk arrays. As

deposition proceeds, these nucleated GaAs crystals incorporate more material and expand both vertically and laterally to fill the patterned holes as can be seen in figure 3.1.3 (b) and (c). Up to 120 minutes as shown in figure 3.1.3 3(d), each individual nanodisk has lateral dimensions of ~1 μm and it fully covers the patterned area. It is also identified from the SEM image that these disks have evident facets even at the very beginning, i.e. after 30 minutes of the growth duration stage as shown in figure 3.1.3 (a). The vertical side walls (four edges of the rectangle from top view) are four {011} planes. The top four facets are other {011} planes. These facets indicate single crystalline nature of the growth and they are associated with the lowest total surface energy in equilibrium.

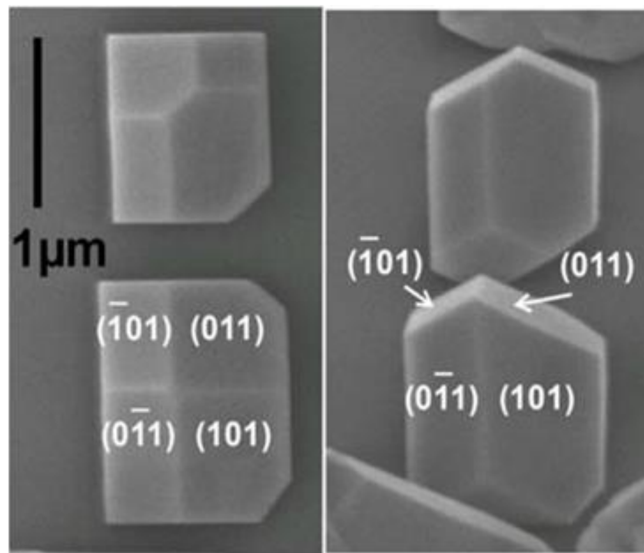



Figure 3.1.4: The SEM images of two adjacent GaAs nanodisks grown at 630 °C showing {110} side walls and top facets. Left: top view; right: 45° tilted view.

The growth mechanism of the nanodisk is studied by its morphology at the beginning stage and the final stage of the deposition as shown in figure 3.1.3 (a) and 3(d). When the growth temperature reaches as high as 630°C, Ga adatoms either desorb on $SiO_2$ surface or migrate to the

nearby opening of silicon surface. These Ga adatoms are then incorporated with As and nucleate in the Volmer-Weber (VW) growth mode[56]. Due to the large diffusion length of Ga at this temperature, these nucleations occur at the edges of the circular openings, where Ga atoms migrate to and then stop at the boundary. In addition, it can be clearly seen that the same set of {011} facets present not only in these nucleated crystals at the beginning stage but also in the final stage of the growth as displayed in figure 3.1.4, which is the magnified view of figure 3.1.3 (d). Such facets formation on the top surface as well as the sidewall indicates the minimization of the total surface energy by strain relaxation in the very beginning stage. Following the idea, as the deposition proceeds, the deposited GaAs crystals retain the strain relaxed nature but expand their size vertically and laterally to form the nanodisks.

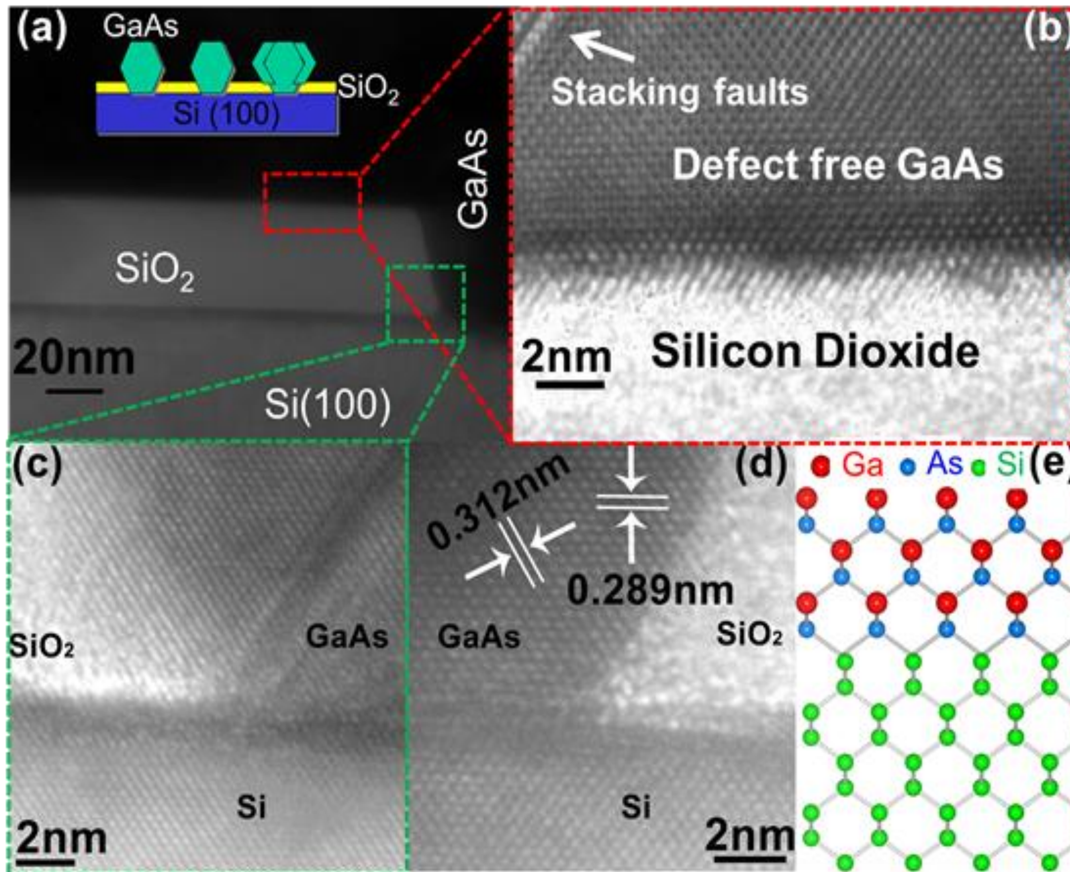


Figure 3.1.5: The XTEM images of (a) GaAs/Si interface; (b) GaAs laterally overgrown on top of $SiO_2$ showing very few stacking faults (c) left edge, (d) right edge of GaAs/$SiO_2$ interface showing defect free nature beyond the edge, and (e) GaAs-Si covalent bond diagram.

GaAs nanodisks grown at 630 °C were further investigated by high resolution XTEM. Figure 3.1.5 (a) exhibits the relative location of GaAs-Si-$SiO_2$ interfaces, whereas figure 3.1.5 (b) shows the GaAs laterally overgrown on top of $SiO_2$ with very few stacking faults and superior crystal quality in this region. The good crystal quality in the overgrown region is possibly due to the complete strain relaxation in the GaAs epilayers within the patterned hole region, so that the extended growth on the $SiO_2$ can retain the almost defect-free nature. Furthermore, figure 3.1.5 (c) the left edge and (d) the right edge of GaAs/$SiO_2$ interface also show threading dislocation and stacking fault free nature beyond the edges. With no observed rotational twin defects and threading dislocations, the good quality of the material corroborates the efficacy of SAE scheme. Although some low-density stacking faults are observed as shown in figure 3.1.5 (c), they are mostly constrained at the edge of the patterned hole. These stacking faults occur when the nucleated GaAs crystal expands to reach the $SiO_2$ mask as they are possibly one way to release the strain energy. With the reduced defect density and the very constrained surface misfit dislocations (only ~ 2 nm at GaAs/Si interface) achieved by nanoscale patterning and lateral overgrowth on top of the $SiO_2$ mask, these GaAs nanodisk arrays may have a potential for optoelectronic device applications.

Moreover, micro-Raman spectroscopy was employed as a means to nondestructively characterize the GaAs nanodisks crystallinity change and the strain relaxation conditions as the growth temperature varies from 550 °C to 630 °C as shown in figure 3.1.6. Previous investigations[57-58] have shown the Raman signals from highly perfect single-crystal GaAs consists

primarily of the contributions from the longitudinal optical (LO) phonon mode at 292 $cm^{-1}$. On the other hand, the addition of defects into the structure results in the contributions from the otherwise transverse optical phonon (TO) mode at 268 $cm^{-1}$. Therefore, the ratio of LO to TO relative intensities in the Raman spectra could be used as the qualitative assessment to understand the crystalline quality of the GaAs nanodisks. Figure 3.1.6 exhibits the comparison of the Raman spectra obtained from GaAs nanodisks at different growth temperatures. The figure demonstrates the remarkable increase of LO mode intensities as the growth increases from 550 °C to 630 °C, indicating the single-crsytal dominant structure is formed as the process goes toward the complete SAE. At 630 °C, the largest LO/TO ratio compared to the other two growth temperatures suggests the much fewer defects and grain boundaries are incorporated into the epitaxially grown structure. However, there are no peak shifts in the LO and TO modes corroborating the complete strain relaxation in the structures grown at these three growth temperatures due to the merit of the SAE.

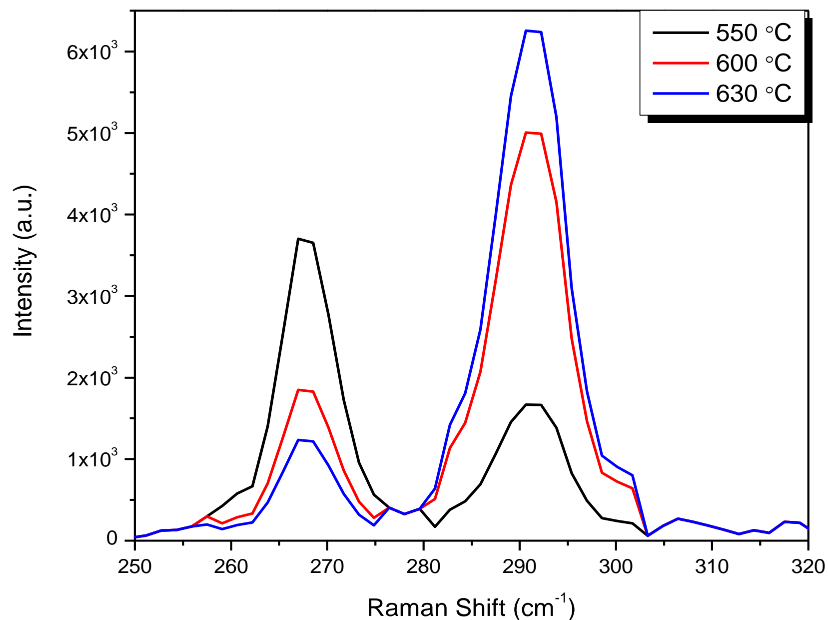



Figure 3.1.6: The micro-Raman spectra for GaAs nanodisks grown at different growth

temperatures showing the trend of increasing LO/TO intensity ratios with the increasing temperature.

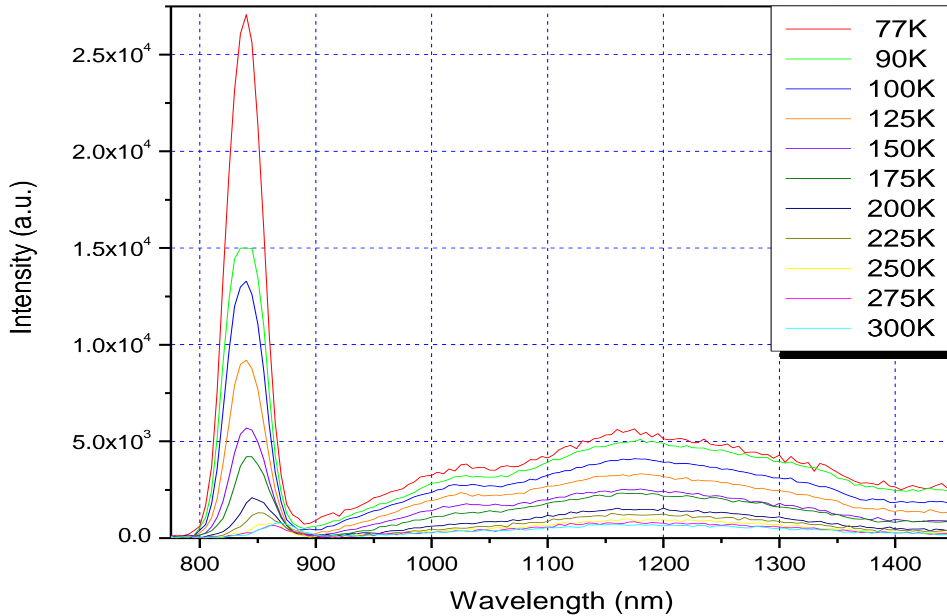



Figure 3.1.7: The temperature dependent μ-PL spectra in the temperature range from 77 K to 300 K for GaAs nanodisks grown at 630 °C.

Figure 3.1.7 shows the temperature dependent μ-PL spectra for GaAs nanodisks grown at 630 °C within the hole arrays. The strong direct band-to-band as well as the relatively inhibited defect-induced optical transitions are exhibited in the temperature range from 77 K to 300 K. As expected, the PL peaks redshift and broaden with increasing temperature corroborating the luminescence mainly from the direct band-to-band transition. We can hereby attribute the excellent optical property to the tremendously reduced defects and stacking faults at the GaAs/Si interface. Moreover, the contributions from catalyst-free growth mechanism along with the initial low temperature grown GaAs layer effectively suppress the formation of mid-gap trap centers and

unintentional doping from the Si substrate.

### 3.1.4 SUMMARY AND CONCLUSIONS

The demonstration of the SAE growth of high-quality GaAs nanodisks on patterned Si(100) substrate is reported. SEM and XTEM reveal excellent material quality, which is attributed to relaxation of strain energy by forming facets and the lateral overgrowth scheme. The reduced defect density and the very constrained surface misfit dislocations (only ~ 2 nm at GaAs/Si interface) are achieved. The strain relaxation and the change in crystallinity from polycrystal-dominant to single crystal-dominant structure with the increasing growth temperature are verified by the micro-Raman spectroscopy. In addition, the excellent material quality contributes to excellent optical properties observed by micro-PL from 77 K to room temperature with luminescence mainly from direct band-to-band transition.

## 3.2 High-quality and defect-free GaAs on $SiO_2$ masked exactly oriented Si(111) substrates by a two-step growth technique and its photovoltaic applications.

High-quality and defect-free GaAs were successfully grown via molecular beam epitaxy on silicon dioxide patterned Si(111) substrates by a two-step growth technique. Compared with the one-step approach, the two-step growth scheme has been found to be a better pathway to obtain a superior-quality GaAs on Si. Taking advantages of low energy for both Si(111) surface and GaAs/Si(111) interface, the two-step grown GaAs of total ~175 nm atop patterned Si(111) substrates exhibits atomically smooth surface morphology, single crystallinity and a remarkably low defect density. A low-temperature GaAs nucleation layer of the two-step growth helps relieve the misfit stress by accommodating the misfit dislocations at the very adjacent GaAs/Si interface. The excellent properties of the two-step grown GaAs were investigated and verified by field-emission scanning electron microscopy, atomic force microscopy, x-ray diffraction, transmission electron microscopy, and Raman spectroscopy. Finally there is a demonstration of a GaAs on Si solar cell which could represent an important milestone for future applications in light emitting diodes, lasers and photodetectors on Si.

### 3.2.1 INTRODUCTION

Since the 1980s, III-V compounds epitaxially grown on Si substrates have attracted a great deal of interest due to the monolithic integration of optoelectronic devices with Si-based microelectronics. In fact, successful heteroepitaxial growth will not only provide high carrier mobility and direct bandgap III-V materials, but also maintain the advantages of lightweight and low-cost Si substrates with high mechanical strength and excellent thermal management. To date, researchers have extensively focused on the growth of high quality III-V compounds on Si and

accomplished the so-called bottom-up integration. However, obtaining high crystal quality III-V compounds, such as GaAs on Si is still challenging due to anti-phase domain (APD) boundary formation as the result of the polar GaAs growth on non-polar Si system; a high density of threading dislocations generated by 4.1% lattice mismatch along with 62% thermal expansion coefficient mismatch.

To circumvent such intrinsic mismatch problems, several approaches, such as time-consuming and complex thermal cycling process, quantum dots dislocation filters, strained layer superlattice (SLS) buffer layers and micron-thick graded buffer layers, have been employed for the epitaxial growth. However, these techniques are not cost-effective and would even complicate the growth procedures. Recently, the patterned growth scheme has been demonstrated as an excellent alternative to obtain high quality GaAs and other materials on silicon dioxide ($SiO_2$) patterned Si substrates[59-61]. Most importantly, this growth scheme can effectively mitigate these three major mismatch problems[62]. Instead of misoriented (vicinal) Si substrates, this patterned growth approach using nominal Si substrates could also effectively reduce the probability of forming high-density APD boundaries. Hence, the nominal Si substrates could be chosen as starting material in our work. However, the surface energy for different planes must be carefully considered in order to achieve the high-quality GaAs atop Si. As opposed to Si(100) plane, Si(111) plane has a lower surface energy[63]. In addition, the lower GaAs/Si(111) interface energy would further facilitate Frank-van-der-Merwe (FM) layer-by-layer growth mode. Meanwhile, we can also benefit from the use of $SiO_2$ sidewalls in stopping and hindering the propagation of the threading dislocations. Consequently, a much thinner GaAs epilayer with a substantially reduced *number of* defects *is e*xpected to be grown on patterned Si(111) substrates. In addition to these obvious advantages, the patterned growth technique eliminates the need for patterning post-growth mesas,

while the $SiO_2$ sidewalls can automatically serve as a lateral electrical isolation.

Recently, such patterned growth approach for GaAs/Si has been demonstrated by numerous research groups[63, 64-67]. Furthermore, a nanopatterned growth approach was used to obtain continuous and large-scale μm-thick GaAs films on Si(001) substrates by metal-organic vapor-phase epitaxy (MOVPE)[68-69]. However, the growth process reported here utilized a growth temperature as high as 650°C and the μm-thick overgrown GaAs epilayers which are incompatible for the back end of line (BEOL) Si technology and unfavorable for GaAs to Si integration. In particular, a growth temperature more than 600°C is not suitable for the metallization in Si devices. Also, due to a lower thermal conductivity of GaAs compared to Si, the thick GaAs buffer layer is inappropriate for an efficient thermal management in these devices.

In this section, I demonstrate such GaAs to Si integration at a growth temperature of 600°C utilizing the two-step scheme on Si(111) patterned substrates. In doing so, the large misfit stress between GaAs and Si is relieved by misfit dislocations at GaAs/Si interface which are introduced by low-temperature (400~450°C) grown GaAs nucleation layer in the first step. The nucleation layer was relaxed to a nearly stress free state, and therefore a thick GaAs could be readily grown at a higher temperature (550~600°C) by homoepitaxy. Furthermore, I demonstrate that the two-step conformal epitaxy could successfully not only generate high-quality and ultra-thin GaAs layer atop Si substrates, but also make the GaAs surface facet-free beneficial for planar optoelectronic devices. Through comprehensive morphological, structural and crystallinity characterizations, I conclude that the two-step growth scheme is a viable approach to achieve ultra-thin, atomically-smooth, single-crystalline GaAs epilayer grown in the patterned holes. Finally, a *p-i-n* heterojunction was fabricated based on the *i*-GaAs buffer layer capped with a $n^+$-GaAs atop the *p*-Si substrate. Thus, photovoltaic devices were realized to illustrate the utility of such buffer layer.

### 3.2.2 EXPERIMENTAL DETAILS

First, a 200-nm-thick thermal $SiO_2$ was grown on Si(111) substrates. Arrays of circular holes with a diameter of 1 μm were defined by stepper lithography followed by the subsequent inductive coupled plasma reactive ion etching (ICP-RIE) of the top $SiO_2$ layer. Representative scanning electron microscopy (SEM) images of patterned circular holes and the corresponding schematics are shown in figures 3.2.1 (a) and (b).

Prior to the epitaxial growth, the patterned substrates were chemically cleaned by the standard RCA process. Next, the substrates were immersed in a 2.5% diluted hydrofluoric acid (HF) for 30 s at room-temperature (RT) to strip the thin oxide layer and some traces of ionic contaminants. The cleaned samples were degassed at 400°C for 10 mins in the buffer tube of our Perkin-Elmer 430 MBE system prior to loading into the growth chamber. Afterwards, the thermal treatment was applied at 900°C for 10 mins in the growth chamber to remove residual native oxides, which might have formed during loading, and to make the surface hydrogen-free. Subsequently, the growth of high quality GaAs layers on Si was performed under an As beam equivalent pressure of around $2 \times 10^{-6}$ torr. In order to ascertain a high quality epilayer through the two-step process, I also grew GaAs atop Si(111) patterned substrates via one-step, i.e. a self-assembled growth approach as the control samples for comparison. Both of one-step and two-step growth schemes were initiated after turning the exposed Si surface inside the patterned circular holes into the As-terminated one. This was done by exposing the patterned substrates under the As overpressure for 5 mins. The surface morphology of as-grown GaAs structures was characterized by SEM (JEOL, JSM-6700F) and atomic force microscopy (AFM, VEECO Nanoscope IIIa Multimode SPM) in the tapping mode. To determine the crystalline quality, the as-grown patterned structures were studied using a high resolution x-ray diffractometer (HRXRD, Bruker D8 Discover) with a

monochromatic CuKα (λ = 1.5405 Å) radiation source operated at 45 kV and 40 mA. The structural and crystalline quality of GaAs were further investigated by cross-sectional transmission electron microscopy (XTEM, JEOL, JEM-3000F) with the specimens prepared by gallium focused ion beam (Ga-FIB) milling with pre-coated chromium, gold, and platinum films as protective layers. Furthermore, the micro-Raman spectra on the as-grown patterned structures were obtained at RT by using a Raman spectrometer (Reinshaw Raman microscope) with a 532 nm excitation

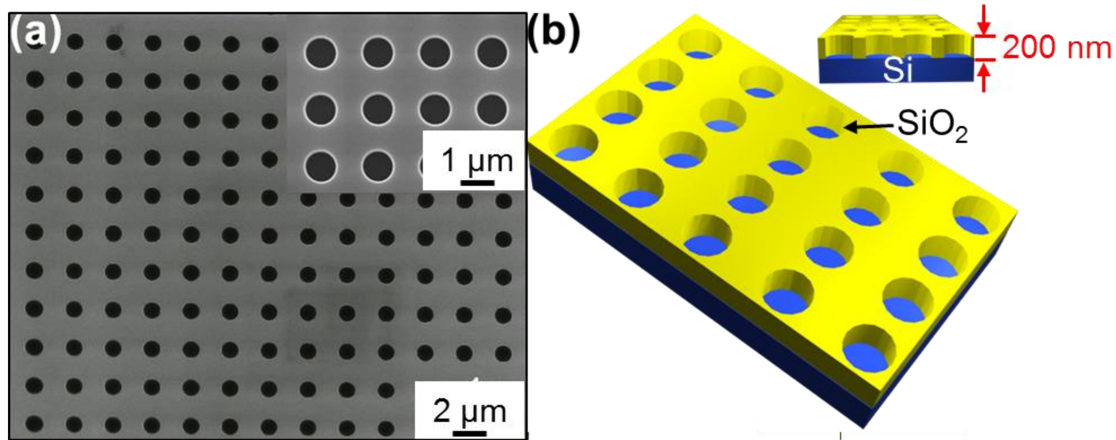



Figure 3.2.1: (a) SEM images for arrays of patterned holes with 1 μm diameter formed by stepper lithography, where the dark circular holes are exposed Si surface. (b) Schematics of tilted and cross-section views for patterned Si substrates with a 200-nm-thick $SiO_2$ mask.

laser.

### 3.2.3 RESULTS AND DISCUSSION

Prior to discussing the experimental results, at first the models of both one- and two-step growth initiation and continuation processes on Si(111) substrate are schematically shown in figure 3.2.2. For the one-step growth, GaAs is grown directly at a substrate temperature as high as 630°C with a V/III ratio of 10. The faceted GaAs was grown for 1 μm in thickness at the nominal growth rate of 1 Å/s. In this growth method, both nucleation and growth occur at a high

temperature so that the nuclei can easily have different orientations with respect to the substrates. Accordingly, the misoriented nuclei are easily formed and the nucleation occurs predominantly at heterogeneous sites as schematically illustrated in figure 3.2.2 (a)-(i). Because of the high substrate temperature in this growth process, both the nucleation rate and the density of nuclei on the substrate surface remain low. Furthermore, since the free energy barrier for heterogeneous nucleation is also low compared to that of homogeneous nucleation, the growth rate is high and the misoriented nuclei grow and coalesce rapidly to form polycrystalline structures. Consequently, continuation of the growth at this high temperature results in thickening of this polycrystalline

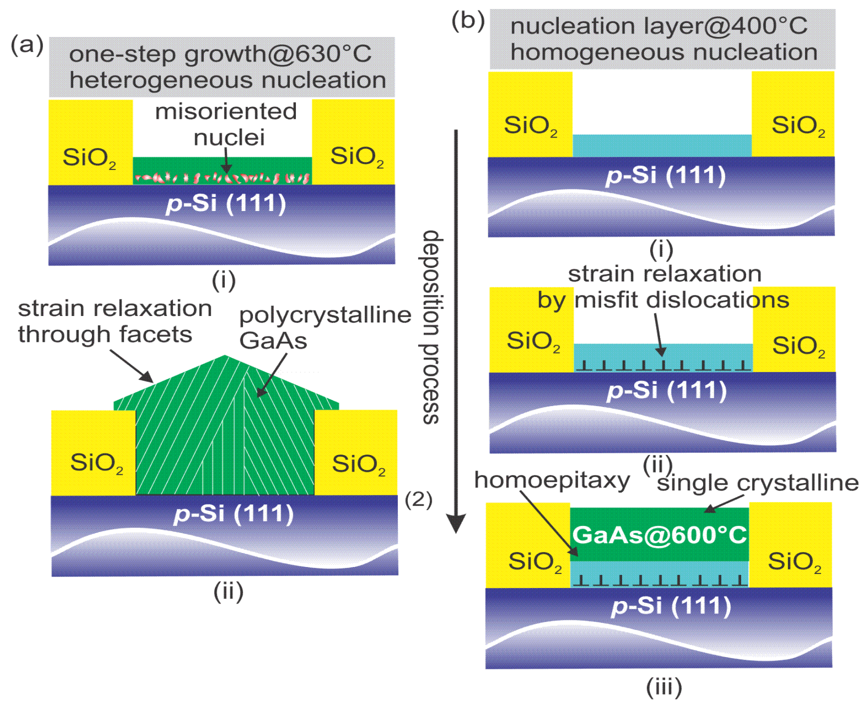



Figure 3.2.2: Schematic illustrations of two different growth schemes at different stages (a) one-step growth model: (i) growth initialization at 630°C through the formation of misoriented nuclei without misfit dislocations, (ii) polycrystallinity of GaAs and the facet formation as the growth continues, (b) two-step growth model: (i) deposition of nucleation layer at 400°C, (ii) introduction of misfit stress and its relaxation through misfit dislocation, (iii) deposition of high quality GaAs at 600°C.

layer[70], which are corroborated with our experimental data described later.

In contrast, for the two-step growth, a 25-nm-thin GaAs nucleation layer at 400°C was initiated with a V/III ratio of 25 and a slow growth rate at 0.25 Å/s. Then without any interruption, a subsequent thicker GaAs layer of 150 nm was grown at 600°C with a V/III ratio as high as 100 and a growth rate of 1 Å/s. For each temperature ramping stage, a low ramp rate at around 0.1°C/s was used to mitigate the influence of the thermal expansion coefficient mismatch issue. In this process, the low-temperature GaAs nucleation layer regrows epitaxially in the so-called solid phase epitaxial (SPE) growth mode during the heating process before the subsequent high temperature (600°C) step. Since the low-temperature (400°C) grown nucleation layer consists of mostly homogeneous small nuclei in parallel epitaxy with the substrate, this layer is not under misfit stress (figure 3.2.2 (b)-(i)). Hence the film resulting from coalescence of growing nuclei is essentially single-crystalline with only few misoriented grains embedded in it[71]. However, as the temperature increases, the misfit stress is induced at the regrown GaAs/Si interface due to the inherent thermal expansion coefficients mismatch induced lattice constants change. To accommodate the misfit stress, the misfit dislocations are formed at the interface as schematically shown in figure 3.2.2 (b)-(ii). At the higher growth temperature step, the lattice constant of the nucleation layer recovers to the bulk lattice constant of GaAs. Thus, a thick subsequent layer can be readily grown since growth mode is turned into homoepitaxy and the mode changes from a 3D to a 2D layer-by-layer FM mode.

Now the experimental results of both growth methods will be described in details. For the one-step growth scheme, hexagonally faceted GaAs epitaxial films were obtained as shown in figures 3.2.3 (a) and (b). The results achieved by this growth process are similar to what have been

reported elsewhere[72]. The selectivity of this self-assembled growth scheme is achieved due to the

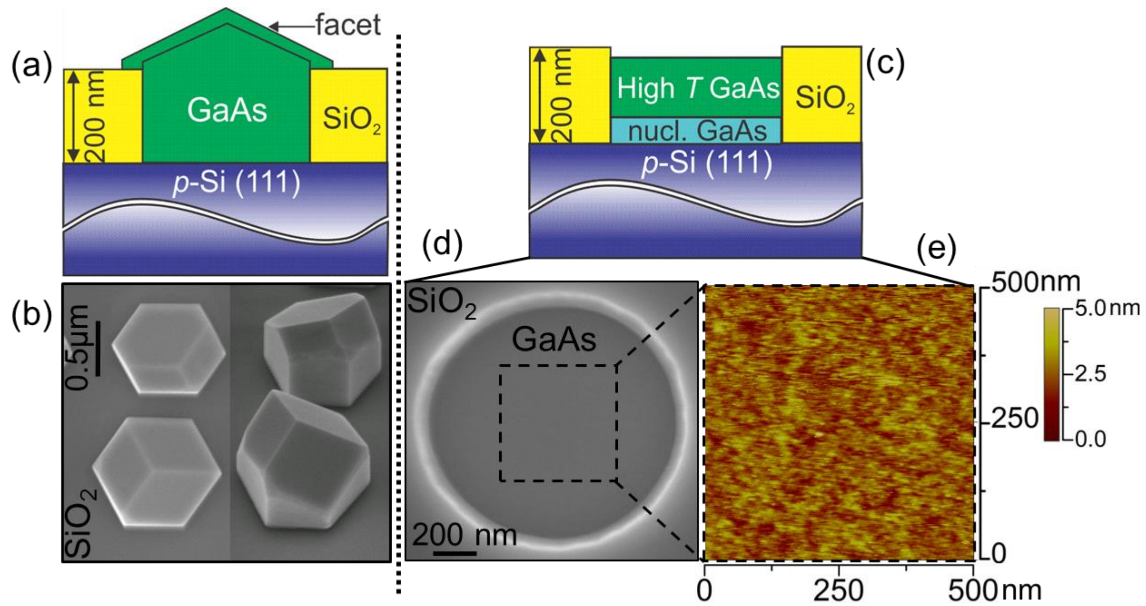



Figure 3.2.3: Schematic cross-sectional views of GaAs via (a) one-step and (c) two-step growth scheme. (b) SEM plan-view and 45° tilt-view images for self-assembled GaAs crystals. (d) SEM plan-view image of GaAs within the patterned circular hole. (e) Corresponding 0.5 μm × 0.5 μm AFM image for the selected region in (d) showing the ultra-smooth surface morphology of GaAs.

long migration length of Ga adatoms and their remarkable desorption from the $SiO_2$ mask at this high temperature. These Ga adatoms are rapidly incorporated with As, yielding self-assembled islands on the nucleation layer through the Volmer-Weber (VW) growth mode. The faceted nature of the as-grown crystals, showing the lower surface energy planes, lead to three (011) facets on the sidewalls and the other three (011) for the top facets. The stress is laterally relaxed through the formation of top facets and sidewalls in this structure. Moreover, we observed the lateral overgrowth of the crystals protruding from the patterned holes toward the $SiO_2$ masks, indicating the minimization of total surface energy in the lateral direction by forming energetically favorable surfaces. However, the strain relaxation in the self-assembled growth through this faceting

formation manner is not preferred for realistic planar optoelectronic device applications due to the uneven surfaces and faceted textures. Alternatively, the two-step based layer-by-layer growth is desirable for planar optoelectronics technology.

For the two-step growth scheme, the grown structures as schematically illustrated in figure 3.2.3 (c) were subjected to different characterization studies. Figures 3.2.3 (d) and (e) show the close-up SEM plan-view and the AFM image, respectively for such as-grown GaAs. The film exhibits atomically smooth surface morphology and high selectivity on the patterned substrates. The ultra-smooth GaAs possess a peak-to-peak variation of only 2 nm and root-mean-square (RMS) roughness value of 0.4 nm which are lower than the lowest-ever reported values obtained on nominal Si substrates[73-74].

The crystalline quality was further characterized by XRD omega-2 theta scans and omega rocking curve scans as displayed in figure 3.2.4. The patterned grown GaAs through the two-step growth exhibits superior single-crystalline characteristic as illustrated in figure 3.2.4 (a). The rocking curve FWHM value for the GaAs(111) plane is as low as 205 arcsec. The superior surface morphology and crystalline quality from the two-step grown samples could be attributed to the effective reduction of threading dislocations and anti-phase domain boundaries. These were achieved by the strain relaxation from the low-temperature to high-temperature transition and the constrained finite size growth from the patterned substrates. Since the nucleation for the two-step growth was carried out at a low temperature, the nucleation was predominantly homogeneous and these nuclei were with a parallel orientation with respect to the substrates. In this case, the lateral growth rate of the homogeneously formed nuclei is much faster than those heterogeneously formed nuclei misoriented with respect to the substrates[75]. Moreover, this parallel epitaxy may even consume the non-parallel clusters by grain boundary migration[75]. Consequently, the density of the

nuclei is so high that they only need to grow by a very small amount before they coalesce. Meanwhile, the chance for any inclusion of misoriented nuclei which could lead to polycrystalline

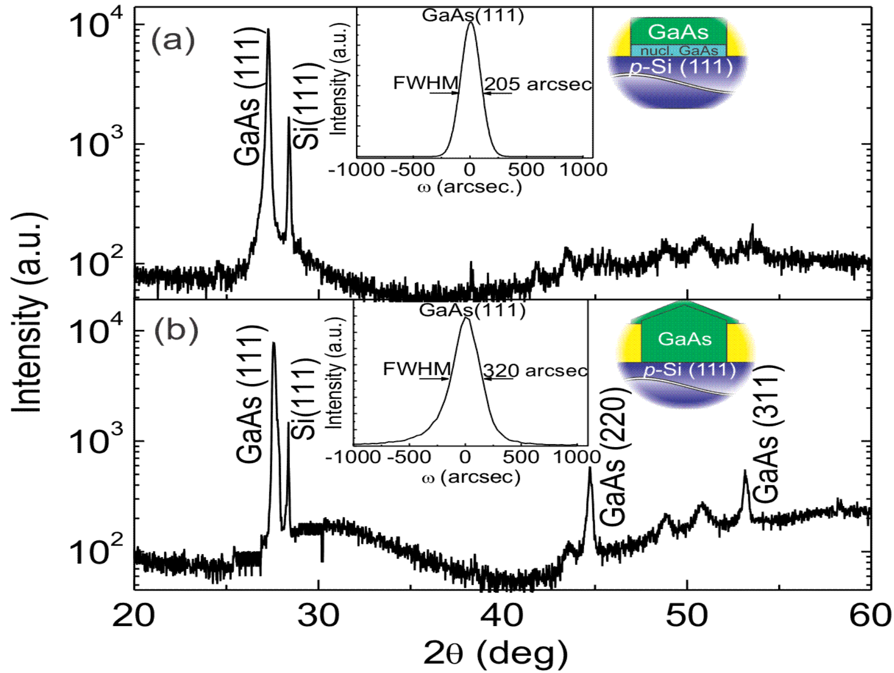



Figure 3.2.4: (a) The XRD omega-2 theta scan for structures grown by (a) two-step growth scheme showing nearly single-crystallinity and (b) one-step (self-assembled) growth scheme showing poly-crystallinity with the presence of GaAs(220) and (311). Two insets show their corresponding rocking curves of GaAs(111) peaks.

nature is further reduced. Accordingly, the high nucleation rate and the high-density of nuclei contribute to their quick coalescence to form a continuous thin and single-crystalline layer on the substrates. On the other hand, the one-step grown GaAs structures exhibit polycrystalline nature, which is confirmed from many diffraction peaks from (111), (220) and (311) crystal planes as shown in figure 3.2.4 (b). In addition, a larger FWHM value of 320 arcsec is also seen. This worse crystalline quality obtained from the one-step growth could be ascribed to a larger amount of defect formation along both $SiO_2$ sidewalls and GaAs/Si interfaces caused by the higher growth rate

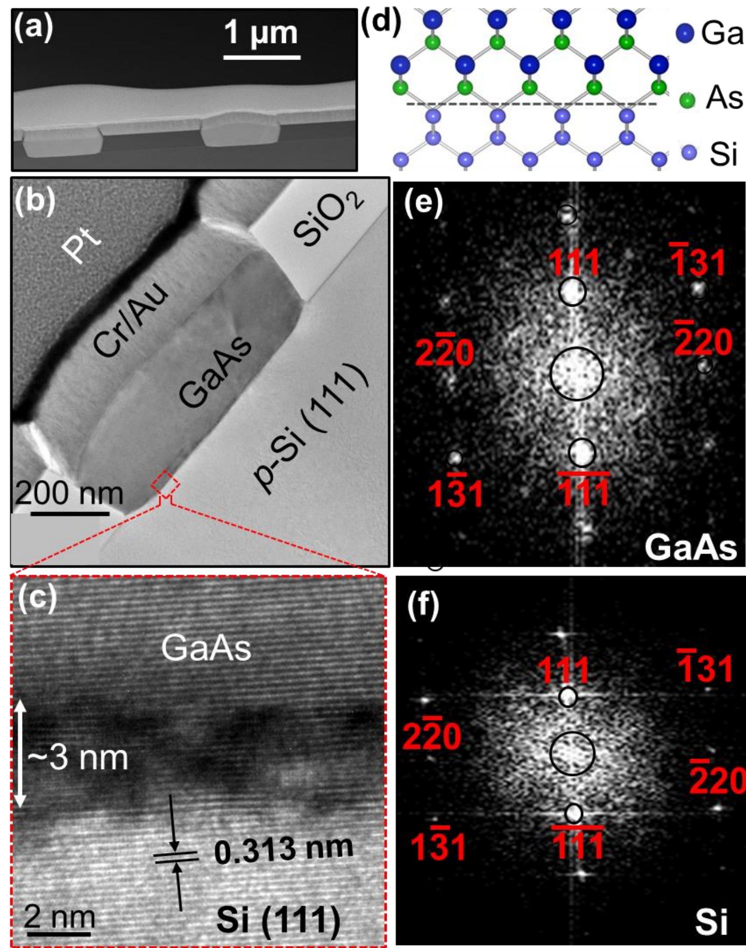



Figure 3.2.5: (a) HAADF XTEM image of GaAs/Si(111) grown by the two-step growth scheme. (b) close-up view of BF XTEM image of GaAs/Si(111), demonstrating the confinement of the defects at the GaAs/Si interface and threading-dislocation-free GaAs beyond the interfacing layer. (c) HRTEM image of GaAs/Si(111), indicating that the misfit dislocations are confined within a few nm region near the GaAs/Si interface. (d) GaAs/Si covalent bond diagram. (e) and (f) SAED patterns taken for GaAs epilayer and Si, respectively, indicating the GaAs layers were epitaxially grown on Si(111) substrates following the same single-crystalline orientation.

sample was immersed in a molten KOH at 350°C for 30 s. Selected Area Electron Diffraction

(SAED) patterns for such two-step grown GaAs epilayer and substrate are also shown in figures 3.2.5(e) and (f), respectively, further affirming the high quality of the GaAs epilayer on Si. Both of the SAED patterns in the $[11\bar{2}]$ zone axis exhibit single-crystalline characteristics, indicating that single crystalline GaAs on Si(111) substrate. Furthermore, the diffraction spots shown in figure 3.2.5 (e) with the Miller indices indicate that the layer is twin- and dislocation-free. Hence, from the above analyses, we may conclude that the structural quality of our GaAs grown through two-step growth scheme is better than those reported, where nominally the high density of rotational twin defects and threading dislocations usually occurred.

The next is to demonstrate the utility of such two-step grown reliable buffer layer for subsequent multilayer growth. For this purpose, a 150-nm thick GaAs layer was grown at 580°C on top of a buffer layer. The schematic cross-sectional view of such structure is shown in figure 3.2.6 (a). Followed by an in-situ post growth annealing at 680°C under As overpressure, the film properties were investigated by both XRD and micro-Raman spectroscopy. The structure still exhibits single crystallinity confirmed by the XRD pattern which is same as figure 3.2.4 (a). Figure 3.2.6 (b) displays the micro-Raman spectrum in which two GaAs Raman signature peaks corresponding to the transverse optical (TO) and longitudinal optical (LO) vibrational bands are located at 267 and 291 $cm^{-1}$, respectively.

These strong LO and weak TO bands of GaAs, are slightly red shifted by 1 $cm^{-1}$ compared to those of bulk GaAs indicating that there are a few defects generated within the GaAs films during the growth process[76]. In spite of being comparable or even better than some of the previous reported results[76-78], the LO-band FWHM for such as-grown GaAs to be ~5.8 $cm^{-1}$ is higher than the bulk GaAs which could be attributed to disorder-induced strain relaxation, perhaps arising from point defects formed during the growth[77].

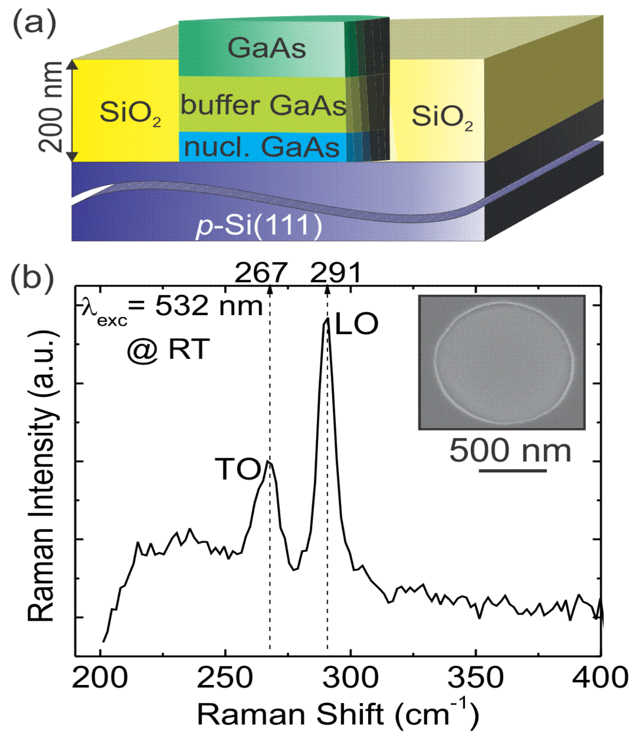



Figure 3.2.6 (a) Schematic cross-sectional view for a structure consisting of a 150-nm GaAs on top of a high quality GaAs buffer layer. (b) Micro-Raman spectrum for the as-grown structure at RT. The inset shows an SEM image of the as-grown structure.

A prototype *p-i-n* solar-cell structure was fabricated using the two-step grown GaAs buffer layer array as schematically illustrated in figure 3.2.7(a). The structure, shown in figure 3.2.2 (b), was modified by adding a 50 nm $n^+$-type heavily doped ($2 \times 10^{18}$ cm$^{-3}$) GaAs on top of the undoped GaAs buffer layer. Si was used for *n*-doping. The top contact was realized by depositing an indium-tin-oxide (ITO) layer on $n^+$ GaAs, whereas indium was used for the bottom contact. The current density-voltage (*J*-*V*) characteristic of the solar-cell is shown in Figure 7(b). In dark, the device exhibits a good rectification characteristic with a current ratio greater than $10^2$ measured at

±1V bias. The fitted $J$–$V$ curve gives the ideality factor ($\eta$) to be 1.6 at RT. Such low ideality factor could be attributed to high minority carrier recombination at the interface of GaAs and *p*-Si substrate as well as a large series resistance of the top contact. The photovoltaic behavior under solar simulator of one sun AM 1.5G illumination shows $J_{sc}$=18.4 mA/cm$^2$ and $V_{oc}$= 0.18 V. The calculated energy conversion efficiency (ECE) and fill factor (FF) are 0.9% and 28%, respectively. The ECE of this GaAs/Si *p-i-n* based device is comparable or better than the reported values for nanostructured solar cells[79-80]. We can attribute this fairly good performance to the high quality buffer layer, which has a very low surface misfit and carrier-trapping threading dislocations. The low FF resulting from a high ideality factor and the low $V_{oc}$ could also be due to the presence of a high density of GaAs surface states adjacent to $SiO_2$ sidewalls and less efficient hole transport across the GaAs/Si heterointerface. It is expected that through proper passivation and improved contact design[81], the energy conversion efficiency may improve significantly.

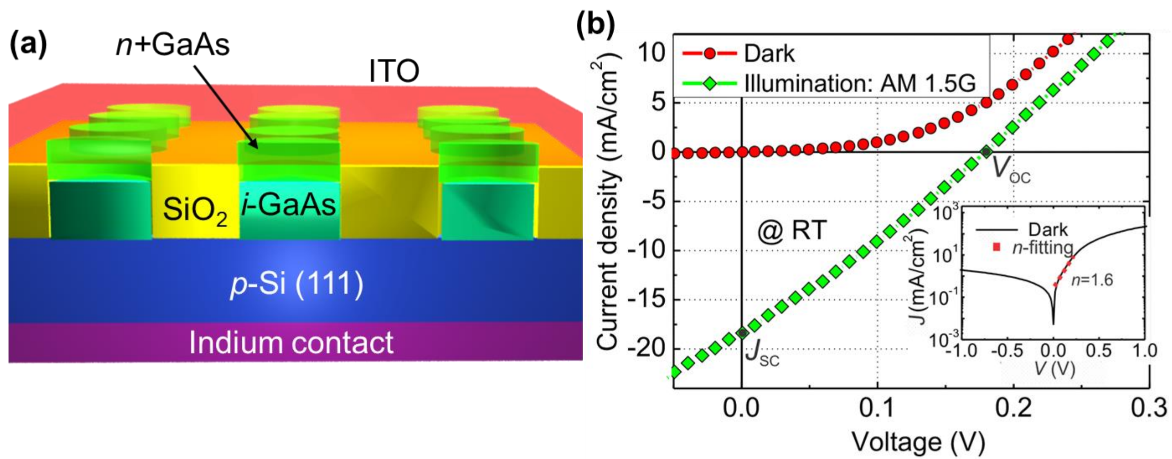



Figure 3.2.7 (a) Schematic cross-sectional view of the fabricated *p-i-n* solar cell (b) *J-V* characteristics of the device under dark and illumination of one sun AM1.5G; the semilogarithmic plot of dark *J-V* is shown as inset.

### 3.2.4 SUMARY AND CONCLUSIONS

The high structural and crystalline quality GaAs on patterned Si(111) substrates was successfully grown through our two-step growth scheme. Utilizing the finite size growth and lower surface energy of Si(111), the high quality GaAs atop Si with ultra-thin (~175 nm) and ultra-smooth epilayers was obtained. The defect-free GaAs epilayer is a potential candidate substrate for planar optoelectronic devices, which shows a pathway to create III-V on Si for many different applications. The fabricated basic *p-i-n* solar cell shows fairly good ECE and FF, and hence can be viewed as an important step toward the broad applications of the III-V compounds to Si integration.

### 3.3 Integration of InGaAs/GaAs double heterostrucure (DH) onto $SiO_2$ masked exactly oriented Si(111) substrates and its optical property characterizations

The study is focused on the realization of InGaAs/GaAs DH on $SiO_2$ masked exactly oriented Si(111) substrates. Through the patterned growth scheme and the optimized nucleation layer as the foundation, the atomically smooth and high crystalline quality InGaAs/GaAs DH is realized. Furthermore, as evidenced by the TEM images, the confined misfit dislocations at the nucleation layer and nearly threading dislocation-free buffer layer contribute to the atomically sharp GaAs/Si interface. The remarkable reduction of two orders of magnitude in the thermally induced stress in COMSOL simulation further corroborates the effectiveness of the square shape pattern design leading to the excellent structural quality and surface morphology. Micro-photoluminescence (μ-PL) and time-resolved photoluminescence (TRPL) data further corroborate the decent optical properties at low temperature of 77 K.

#### 3.3.1 INTRODUCTION

Over the past few decades, there has been an intense research interest in heteroepitaxial growth of GaAs on Si substrates due to a wide range of emerging applications, such as optoelectronics integrated circuits, high-efficiency light-emitting or detecting devices, and low cost solar-cells with increased mechanical strength. High-quality heteroepitaxial growth of GaAs/Si is highly demanded, because it allows to combine the advantges of silicon technology with the optical and high-speed capabilities of GaAs and its alloys. However, direct planar epitaxial growth GaAs on Si for a successful heterogeneous integration is challenging due to lattice

mismatch and significant differences in coefficient of thermal expansion as well as anti-phase domain (APD) boundary formation as the result of the polar GaAs growth on non-polar silicon.

To overcome such intrinsic material-related problems, several time-consuming, cost-ineffective and complex ways including micron-thick buffer layer, in-situ or ex-situ thermal annealing, quantum dots dislocation filters, and strained layer superlattice (SLS) buffer layershave already been employed during the epitaxial growth of GaAs on silicon. A simple and cost-effective way of eliminating, or reducing lattice and thermal mismatches is to employ the concept of the patterned growth. Due to the size effect resulting in a localized growth, such concept also reduces the probability of forming APD defects in the epilayers. Therefore, the patterned growth using especially $SiO_2$ masked Si substrates have been demonstrated to be an effective way for obtaining high-quality GaAs on Si. This should also offer the possibility of using a very thin buffer layer for achieving defect-free GaAs epifilms. In addition to these obvious advantages, the patterned growth technique eliminates the need for patterning post-growth mesas, while the $SiO_2$ sidewalls can automatically serve as a lateral electrical isolation.

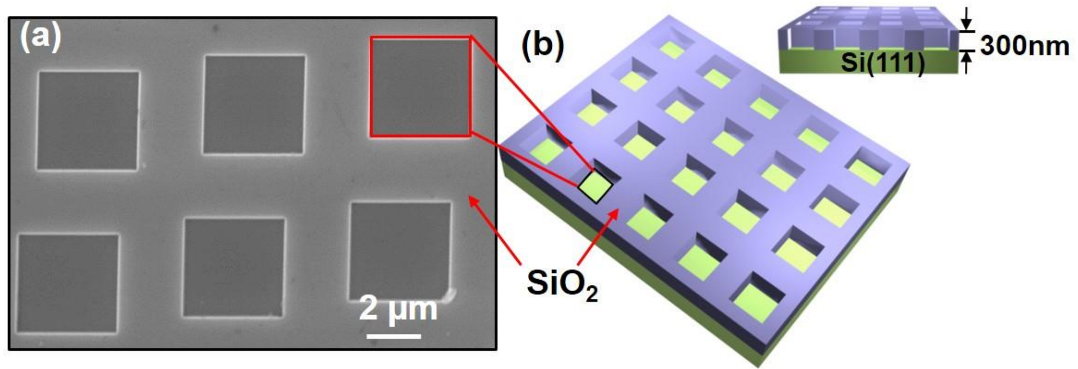
The high-quality epitaxial growth of GaAs on Si using patterned substrates has been widely reported in a broad number of journals[82-85]. However, the growth process reported in most of these studies utilized either a high growth temperature or the micron-thick overgrown GaAs epilayers which are incompatible for the back end of line (BEOL) Si technology and unfavorable for GaAs to silicon integration. Besides, the as-grown samples reported in these studies[86-88] lack double heterostructures, serving as an active region, which essentially limits their applicability in realizing high-efficient light sources. In this paper, we demonstrate high-quality InGaAs/GaAs multilayer heterostructures on patterned silicon substrates utilizing ultra-thin buffer layer, being suitable for targeted applications. In spite of the growth of GaAs on Si(100) is more desirable for device

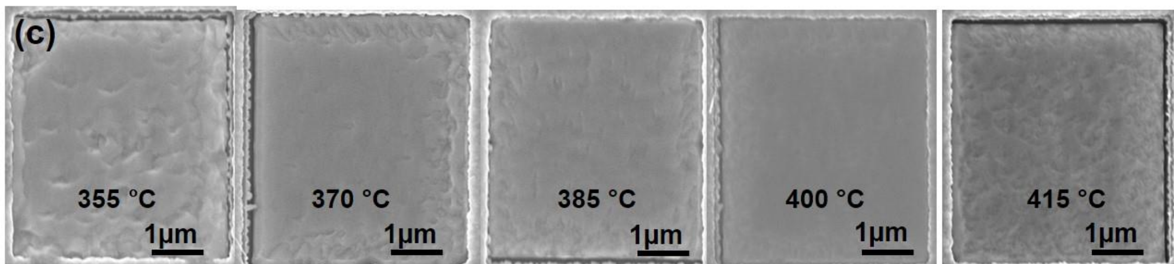
applications, Si(111) is used in the present experiments because a (111)-oriented substrate has lower surface energy as well as lower surface energy at the interface and it prevents the formation of antiphase domains in the relation to the bond matching at the interface.

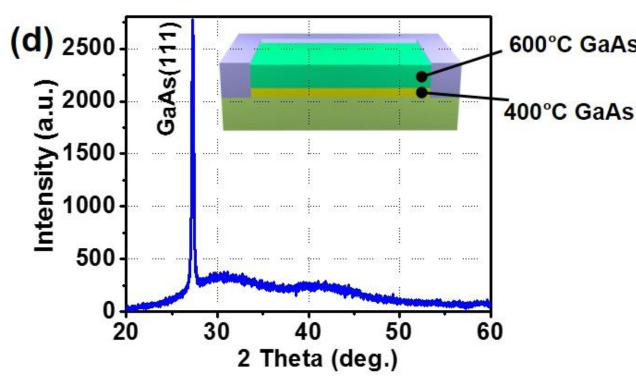
### 3.3.3 EXPERIMENTAL DETAILS

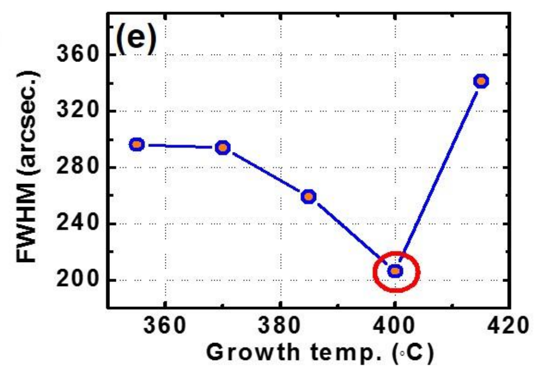
The patterned substrates were fabricated on 280-nm-thick thermal $SiO_2$ masked Si(111) substrates. The stepper lithography combined with inductive coupled plasma reactive ion etching (ICP-RIE) techniques were used to define square arrays of holes with 4 μm side length in such patterned substrates. Representative scanning electron microscopy (SEM) images of patterned square holes and the corresponding schematics are shown in figures 3.3.1 (a) and (b). Prior to the epitaxial growth by our Perkin-Elmer 430 MBE system, the required preparation steps during pre- and post-loading the sample into the reactor for the patterned substrates are discussed in the publushed results[89]. Under an As beam equivalent pressure of around $2 \times 10^{-6}$ torr, the growth was inititaed by employing two-step growth process that has been proven to be a successful approach to deposit GaAs on Si[90]. In this growth method, a good-quality nucleation layer is formed at a low temperature of 400° C before high-temperature deposition of thicker crystalline films. Details of such growth process and how it was employed at the early stage of the growth on top of Si(111) substrate are also described in the formerly published results[89]. And the process to obtain the optimal nucleation layer growth temperature is shown in figures 3.3.1 (c), (d), and (e). After achieving a smooth nucleation layer of GaAs on Si(111), the substrate temperature was raised to 600 °C, the growth temperature of crystalline GaAs, required for a second step growth on top of the nucleation layer. The second step growth was performed at 1 Å/s and V/III ratio of 100, resulting in 150 nm thick GaAs buffer layer. The growth was then interrupted. The samples were

in-situ annealed at 700 °C for 15 min under As overpressure to annihilate the defects introduced during the nucleation process. Followed by the two-step grown GaAs buffer layer is the growth of bottom GaAs barrier layer at 580 °C for the InGaAs DH. The growth temperature was ramped down to 500 °C in order to deposit InGaAs layer with a nominal thickness of 10 nm. The nominal indium molar composition, in this study, was 0.15, and the As fiux during growth was increased to make the V/III ratio of 150 in order to deal with the In segregation problem. It has been demonstrated that indium segregates towards the growth front during the MBE growth of InGaAs[91]. Therefore, the growth temperature as low as 500 °C and high As flux were used for the deposition of InGaAs well and immediate overlaying GaAs layer as the capping layer. Hence, the In segregation and evaporation at growth temperature above congruent sublimation can be prevented. More importantly, utilizing the double GaAs capping layers at 500 °C and 550 °C is believed to further reduce the In segregation issue while increasing the growth temperature to grow the topmost GaAs layer. Finally, the growth was terminated with the deposition of top GaAs barrier layer grown at 580 °C followed by in-situ annealing under As overpressure at 700 °C.


(a)
2 μm
(b)
300nm
Si(111)
SiO2


(c)
355 °C
1μm
370 °C
1μm
385 °C
1μm
400 °C
1μm
415 °C
1μm


(d)
GaAs(111)
600°C GaAs
400°C GaAs
Intensity (a.u.)
2 Theta (deg.)


(e)
FWHM (arcsec.)
Growth temp. (°C)

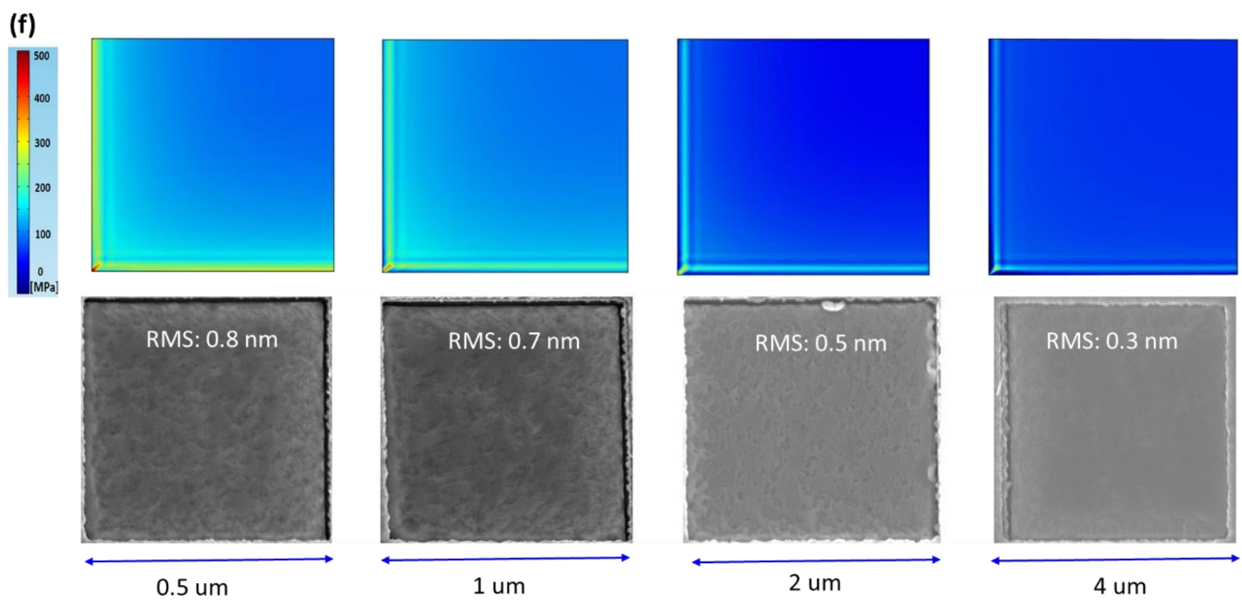

(f)
[MPa]
RMS: 0.8 nm
RMS: 0.7 nm
RMS: 0.5 nm
RMS: 0.3 nm
0.5 um
1 um
2 um
4 um

Figure 3.3.1: (a) A plan-view SEM image of $SiO_2$ masked Si(111) patterned substrate and (b) its schematic. (c) SEM images for the growth temperature dependent GaAs nucleation layer (d) XRD ω - 2θ scan for the structure in the inset based on the 400 °C grown nucleation layer. (e) FWHM for XRD ω –scan on the samples with various growth temperature nucleation layers. (f) quarterly-symmetric geometry COMSOL thermal stress simulation results versus SEM images for GaAs thin films on Si on size dependent patterned windows.

The surface morphology of as-grown InGaAs/GaAs heterostructures was characterized by SEM (JEOL, JSM-6700F) and atomic force microscopy (AFM, VEECO Nanoscope IIIa Multimode SPM) in the tapping mode. The crystalline quality were determined using a high resolution x-ray diffractometer (XRD, Bruker D8 Discover) with a monochromatic CuKα ($\lambda$ = 1.5405 Å) radiation source operated at 45 kV and 40 mA. The cross-sectional specimen was prepared by hand polishing using a tripod technique and final thinning using a Gatan precision ion polishing system (PIPS). The structural characteristics of the InGaAs/GaAs multilayer structure were then investigated by cross-sectional transmission electron microscopy (TEM, Tecnai F20, operated at 200 keV). In addition, a finite element model in COMSOL was developed to predict and analyze the internal stresses of the patterned InGaAs/GaAs DH due to their deposition parameters. Of specific interest were the thermally induced stress distributions and potential edge concentrations as a result of disparities in thermal expansion properties. Photoluminescence spectra from InGaAs/GaAs DH on the as-grown patterned structures were collected using frequency-doubled diode pumped Nd:YAG laser ($\lambda$ = 532 nm). The micro-photoluminescence (μ-PL) was collected by a 50× objective lens, and recorded by a CCD camera. Time-resolved photoluminescence (TRPL) measurements were performed using a mode-locked Ti:sapphire laser

operated at a wavelength of 635 nm with a pulse width of 2.7 ps and a repetition rate of 80 MHz. The TRPL signal was collected by a Hamamatsu C5680 Streak Camera system.

### 3.3.3 RESULTS AND DISCUSSION

Since the quality of the nucleation layer will directly influence the quality of the whole structure due to any propagation of dislocations into the upper layers or in-plane cumulative strain, it's worth studying the optimization of nucleation layer growth condition as the starting point toward the realization of InGaAs/GaAs double heterostructure. In order to optimize the nucleation layer growth temperature, the growth temperature dependent experiments were utilized to grow various temperature 25 nm GaAs nucleation layer followed by the 600 °C 150 nm GaAs buffer layer (600 °C is the well known growth temperature for a crystalized GaAs thin film). As can be seen in figure 3.3.1 (c), the 25 nm nucleation layer grown at 400 °C exhibits the smoothest and the most uniform coverage in the patterned sites. However, the further crystalline quality characterization is necessary to be carried out to corroborate the surface morphology characterization. Hence, XRD $\omega$ - 2$\theta$ scans were firstly performed on each sample to identify the crystalline phase as shown in the representative plot figure 3.3.1 (d) for the 400 °C nucleation layer case. The GaAs(111) is the only crystalline phase observed in the four grown samples although the linewidth of the GaAs(111) differs from one another representing crystalline quality varies from the different nucleation growth temperature. Hence, the $\omega$ –scans at each GaAs(111) for the five samples shown in figure 3.3.1 (c) were carried out. As shown in figure 3.3.1 (d), the $\omega$-scans on the samples with various growth temperature dependent nucleation layers with the GaAs(111) peaks full width at half maximum (FWHM) ranging from 205 arcsec. to 342 arcsec.. The lowest value of 205 arcsec. from the sample grown based on 25 nm 400 °C nucleastion layer represents

the best crystalline quality with a remarkably reduced defect density, which corroborates the best surface morphology for this sample. Therefore, the GaAs thin films grown based on the 25 nm 400 °C nucleation layer and 150 nm 600 °C will hereafter serve as the base for the further InGaAs/GaAs DH growth. However, we can exam from the other angle with the help of COMSOL thermal stress build up simulation based on the growth procedure as aforementioned. As shown in figure 3.3.1 (f), we could reason the optimal patterned window size as being used in the growth. The COMSOL thermal stress simulation was done in the quarterly-symmetric geometry manner for GaAs thin films being deposited onto various patterned windows ranging from 0.5 µm to 4 µm. The simulation was set up to emulate the cooling process after the growth is finished. For the substrate temperature being cooled down from 600 °C to 20 °C. The mismatches in coefficients of thermal expansion and temperature difference during the cooling process leads to the tensile stress throughout the GaAs thin films. However, the more concentrated and reduced tensile stress is only found for the 4 µm window meaning reduced and more localized thermal stress of GaAs thin films appear on the 4 µm window. As can be further substantiated by SEM and AFM roughness analysis, the GaAs thin films possess the atomically smooth nature with the roughness RMS value down to 0.3 nm meaning the very good quality as a buffer layer grown on the 4 µm window. However, COMSOL simulation cannot demonstrate those atomic level mismatches in APD and lattice constants. Hence, I hereby resort to some literature which did size dependent GaAs[92-94] and SiGe[95] epitaxy onto $SiO_2$ masked patterned Si. As indicated in references, the authors demonstrated the remarkable reduction in defect density as the window size was shrunk down below 10 µm, and further showing the optimal patterned window size corresponds to 4 µm. Thus combining the COMSOL results with SEM/AFM analyses and literature references, we can have a good intersection point of window size of 4 um between the increasing and decreasing window sizes.

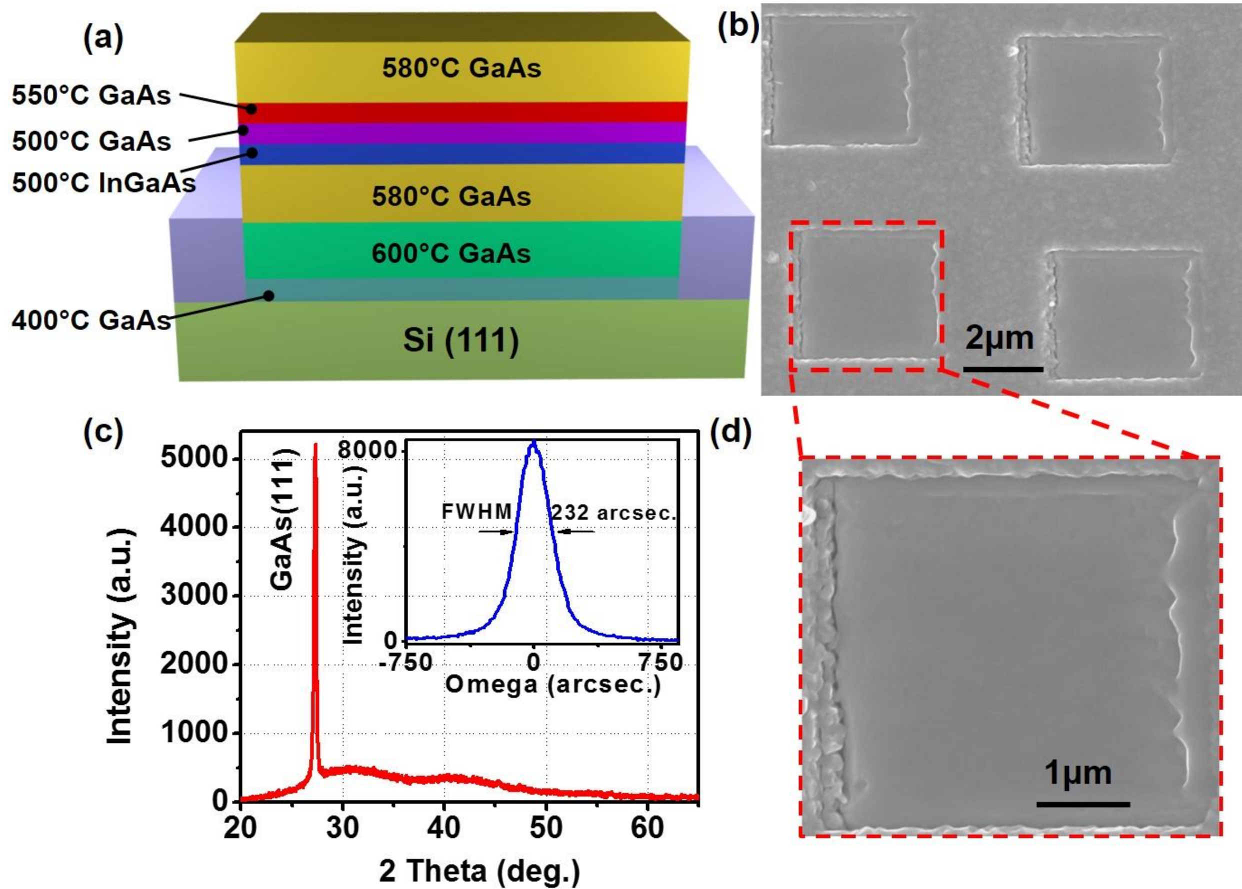



Figure 3.3.2: (a) The schematic cross-section view of the InGaAs/GaAs DH grown based on a Si(111) patterned substrate. (b) A plan-view SEM image of the as-grown InGaAs/GaAs DH. (c) The XRD ω-2θ scan for the as-grown InGaAs/GaAs DH exhibits the single crystalline nature, and the corresponding ω-scan at the GaAs(111) peak is shown in the inset. (d) The close-up view for a single InGaAs/GaAs DH at a patterned window.

Following the growth procedure indicated in the section of experimental details, the schematic cross-section view of the InGaAs/GaAs DH in figure 3.3.2 (a) displays the relative location and growth temperatures for each epilayer. The successful results are presented in a plan-view SEM image shown in figure 3.3.2 (b) for an array for the patterned grown InGaAs/GaAs DH

with the close-up view in figure 3.3.2 (d) for a single structure at a patterned window. During the patterned growth, adatoms far from the oxide sidewall can easily migrate into the patterned windows and bond to the underlying substrate atoms. However, the growth is interrupted by the amorphous $SiO_2$ layer at the sidewall. The facet formation during the patterned growth is mainly governed by the orientation of the $SiO_2$ sidewall with respect to the underlying substrate. In other words, the growth rates or the nucleation process of different growth planes near oxide sidewall are not same, yielding faceted-surface morphology. In my case, taking advantage of using Si(111) substrates instead of Si(100) ones, I could remarkably reduce the GaAs/Si interface energy as well as the epitaxially grown GaAs buffer layer surface energy . In this way, the facet formation won't be an issue. On the other hand, Pratt *et al.*[100] reported that the In migration process is extremely sensitive to the group V flux during growth of InGaAs/GaAs quantum wells on patterned GaAs substrates. Using this concept, we have used the arsenic flux in a controlled way so that the migration of adatoms during the growth can be suppressed, leading to smooth and facet-free surface. It is believed that high As flux (i.e. high V/III ratio, with the ratio approximately equal to 150 in our experiments) reduces the In adatoms migration by limiting migration length, hence minimizing the coalescence of the adatoms, and yielding planar growth. In spite of high V/III ratio employed in our two-step growth, GaAs are deposited on both oxide and exposed Si surfaces as can be seen in figure 3.3.2 (b). This is because of the fact that the growth temperature ranging from 400 °C to 600 °C was used in this study which results in inducing nucleation for GaAs on a $SiO_2$ surface. Due to such nonselective growth, GaAs deposited at the pattern edges is in intimate contact with the ploycrystalline GaAs with columnar grains that grows on top of the amorphous oxide mask layer. Although fully selective GaAs/InGaAs heterostructure growth could be achieved at a temperature over 630 °C[101], a low growth temperature range below 600 °C was

utilized in this study, making the growth process more compatible to standard Si complimentary metal-oxide-semioconductor (CMOS) technology.

The crystalline quality was further characterized by XRD ω-2θ and ω rocking-curve scans The patterned InGaAs/GaAs DH through the two-step growth exhibits superior single-crystalline characteristic as shown in figure 3.3.2 (c). The broad shoulder over the 2θ range of interest in the XRD pattern is attributed to the presence of the amorphous $SiO_2$ on the samples since the X-ray spot size is around 1 cm × 1 cm, the inclusion of amorphous $SiO_2$ signals is normal. The diffraction peak for the 10 nm thin InGaAs layer with indium content as low as 15% cannot be resolved at around GaAs(111) peak. This could be most probably due to such broad shoulder which buried low-intensity InGaAs peak as well as the low thickness of this InGaAs layer. The rocking curve full-width at half-maximum (FWHM) value for the GaAs(111) plane is as low as 232 arcsec as shown in the inset. The superior surface morphology and crystalline quality from the two-step grown samples could be attributed to the effective reduction of threading dislocations and anti-phase domain boundaries. These were achieved by the strain relaxation from the low-temperature to high-temperature transition and the constrained finite size growth from the patterned substrates. The details of the nucleation and growth processes in the two-step growth and the description how these processes lead to high-quality single-crystalline layer on the patterned substrates can be found in the published results[89]. It should be noted that such two-step grown InGaAs/GaAs heterostructure possesses only ~ 350 nm GaAs layer, exhibiting the FWHM of 232 arcsec. Given the prior reports of the x-ray rocking curves for GaAs on Si, a FWHM value of 232 arcsec was only attained with GaAs films that are on the order of microns thickness. This amounts to approximately two orders of magnitude improvement in the quality of our two-step grown square-patterned GaAs thin films. This investigation is ongoing and clearly more work is

needed to optimize growth conditions by which the quality of such epilayers could be further improved. The crystalline quality is further evidenced by the average crystallite size, which is calculated from the FWHM of the XRD omega-scan peaks based on Debye–Scherrer formula[98]

$$D = \frac{1.2\lambda}{\mathrm{FWHM}(2\theta) \times \cos\theta}$$

where FWHM is for the most prominent XRD $2\theta$ peak, and $D$ is the crystallite size. In our case, the dominating peak is GaAs(111) at around $2\theta = 27.3°$. Thus the crystallite size obtained is 170 nm. For this crystallite size approximation, we exclude the peak broadening contributed from the instrument and the strain from the epilayers because of the appropriate use of the optics in the measurements and the strain relaxation in the epilayers.

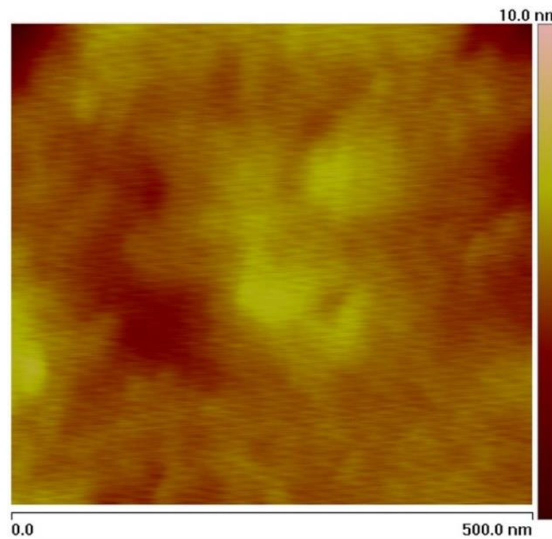



Figure 3.3.3: The AFM image of scanned 0.5 µm × 0.5 µm area from a single patterned window showing the ultra-smooth surface morphology with a RMS roughness of 0.25 nm for as-grown InGaAs/GaAs DH surface.

Furthermore, the AFM image shown in figure 3.3.3 shows the surface morphology of as-grown InGaAs/GaAs DH within scanned 0.5 μm × 0.5 μm area. Several were done. The grown film exhibits atomically smooth surface morphology, yielding a peak-to-peak variation of only 1.8 nm and root-mean-square (RMS) roughness value of 0.25 nm which are lower than the lowest-ever reported values obtained on exactly oriented Si substrates as well as the atomically smooth GaAs(111) epilayer.

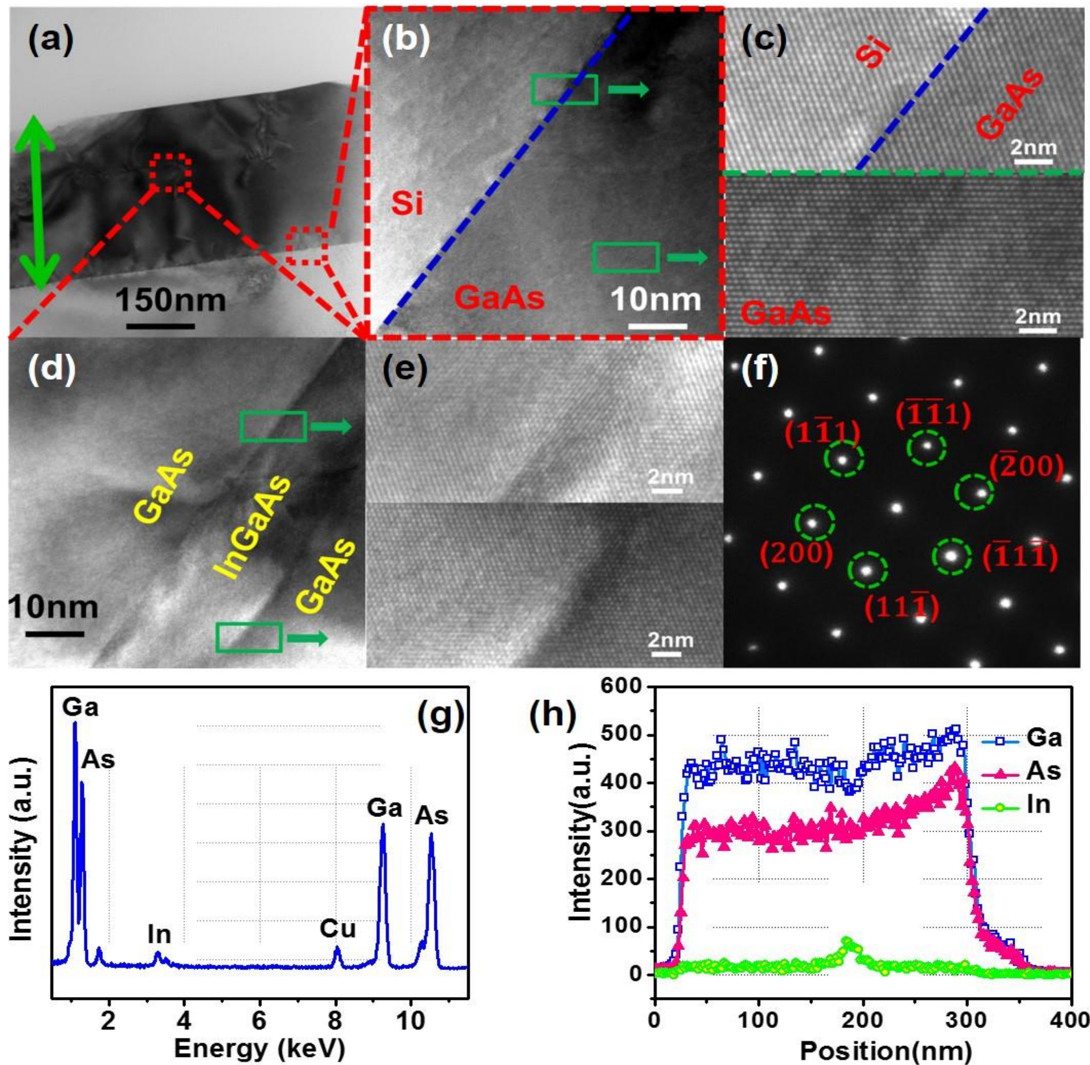



Figure 3.3.4: (a) The cross-sectional TEM (XTEM) image of the InGaAs/GaAs DH grown on patterned Si(111). The green arrows indicates the vertical range of the whole structure. (b) The XTEM image at GaAs/Si heterointerface showing nonobservable threading dislocations. (c) The

high resolution TEM (HRTEM) images shows the abrupt and defect-free GaAs/Si interface (Top), and stacking fault free GaAs epilayer right above the Si (Bottom). (d) Magnified TEM image of the InGaAs/GaAs DH. Although the defects are visible at the GaAs/InGaAs interface, while no threading-dislocation are observed beyond the DH. (The lefthand side of the image is toward the Si surface) (e) The XTEM image for the interface between GaAs barrier layers and the InGaAs layer: Bottom GaAs barrier layer /InGaAs interface (Top), and top GaAs barrier layer/InGaAs interface (Bottom). (The green arrows also indicate the relative locations.)(f) Selective Area Electron Diffraction (SAED) patterns taken for GaAs epilayer, indicating the GaAs layers were epitaxially grown on Si(111) following the exactly single-crystalline orientation. (g) The energy dispersive spectrscopy (EDS) of the whole InGaAs/GaAs DH. (h) The position dependent EDS line-scan for the whole DH. (The plot starts from the GaAs/Si interface).

The local material quality of the as-grown GaAs/InGaAs/GaAs heterostructure was further examined by TEM. Figure 3.3.4 (a) shows the cross-sectional TEM (XTEM) image of the whole structure on patterned Si(111) substrate. In figure 3.3.4 (b) and (c), there is a sharp and abrupt transition between the Si substrate and the GaAs nucleation layer showing very good heterointerfacial quality. Furthermore, there is neither observable threading dislocations penetrating into the GaAs epilayer nor stacking defaults in the nucleation layer region adjacent to the Si interface as can be justified from figure 3.3.4 (c). Misfit dislocations and threading dislocations are the two most common types of dislocations appeared in the zinc blende or diamond crystal structure of a cubic system. During the early stage growth of the GaAs nucleation layer on Si, the lattice-mismatch induced interfacial misfit dislocations appear and they are mainly confined within ~3 nm from the GaAs/Si heterointerface. However, in this InGaAs/GaAs DH study, the

misfist dislocations could be claimed too confined within narrower range to be observed. This means the effectiveness of the patterned growth scheme via the 4 μm × 4 μm square patterns has been proved. Moreover, based on the etch pit density (EPD) study on the as-grown heterostructure, the threading dislocation density is measured to be ~$5 \times 10^6$ $cm^{-2}$ obtained by counting the etch pits after the sample was immersed in a molten KOH at 350 °C for 30 s. Figure 3.3.4 (d) and (e) show XTEM and high resolution TEM (HRTEM) images of the well/barriers region with GaAs/InGaAs/GaAs layers, exhibiting a few defects at well-to-barrier interfaces. The GaAs bottom barrier layer located below the InGaAs well layer and on top of the Si substrate as indicated in the upper portion of the figure 3.3.4 (e) is observed to be nearly defect-free. Likewise, the nearly defect-free GaAs top barrier layer above the InGaAs well layer is also displayed in the lower portion of the figure 3.3.4 (e). In the adjacent well-to-barriers regions, the visible misfit dislocations are generated mainly due to the lattice mismatch between GaAs barrier layers and the InGaAs well layer, and the thermally induced stress during growth temperature change from the low-temperature grown well layer to the high-temperature grown GaAs top barrier layer. The selective area electron diffraction (SAED) pattern shown in figure 3.3.4 (f) further justifies the high quality InGaAs/GaAs DH on Si. The SAED pattern in the $[11\bar{2}]$ zone axis exhibits simply spotty pattern, indicating the single crystalline InGaAs/GaAs DH on Si(111) substrate. Furthermore, the spotty diffraction pattern indexed in Miller indices indicates no twin spots, hinting that the as-grown layer is microtwin- and dislocation-free. Moreover, the energy dispersive spectrscopy (EDS) of the whole InGaAs/GaAs DH displayed in figure 3.3.4 (g) qualitatively present the elemental composition within the whole DH, showing the approximately stoichiometric Ga and As elements as well as the small fraction of In. More specifically, the EDS line-scan profile in the vertical direction (starting from GaAs/Si interface toward the top GaAs

barrier layer) as displayed in figure 3.3.4 (h) provides the information of the relative elemental composition throughout the entire structure. The strong and nearly stoichiometric Ga and As elements throughout the entire structure are observed. In addition, a weak but distinguishable signal from In at the well region with its composition of 15% can also be seen in this profile corroborating the correct location of this layer as indicated in the growth procedure.

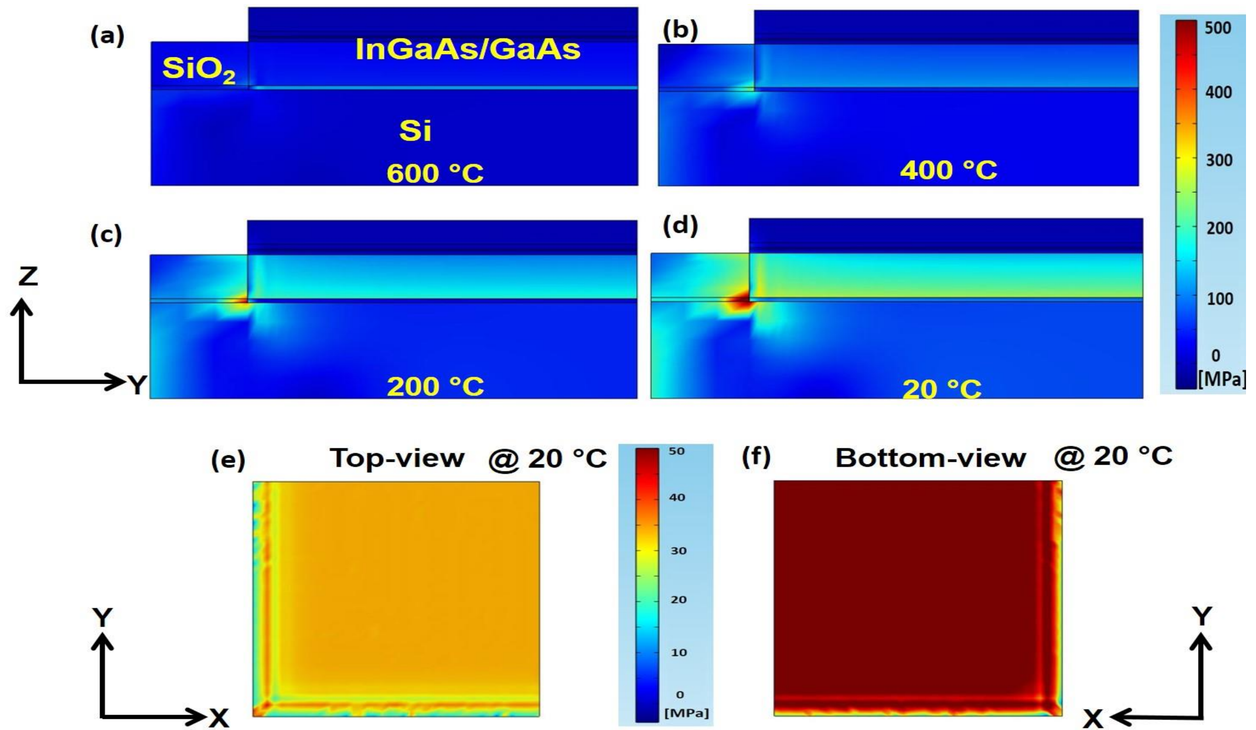



Figure 3.3.5: (a) to (d) The thermally induced stress profile was simulated in COMSOL to display the stress build-up profile during the cooling process (from 600 °C to 20 °C) after the post growth in-situ annealing was finished. The DH simulated in COMSOL was built in the geometrically quarter-symmetric manner for the InGaAs/GaAs DH at a single 4 μm × 4 μm patterned window. (e) The thermally induced stress profile for the InGaAs layer (seen from the top). (f) The thermally induced stress profile for the InGaAs layer (seen from the bottom).

A finite element model was developed in COMSOL to predict and analyze the internal stresses of the patterned InGaAs/GaAs DH due to their deposition parameters. Of specific interest were the thermally induced stress distributions and potential edge concentrations as a result of disparities in thermal expansion properties among the dissimilar materials. It was assumed that each material's mechanical properties behaved linearly, experiencing no hysteresis or creep effects, with thermal contributions expressed quazi-statically as a function temperature only. Of the four materials present in the system referenced by figure 3.3.2 (a): GaAs, InGaAs and the Si substrate were treated with full orthotropic elasticity tensors to best represent the heteroepitaxial deposition process, while the $SiO_2$ template was considered to be fully isotropic. All four materials were considered to maintain constant densities, thermal expansion coefficients, heat capacities and thermal conductivities.

A unit cell, representative of a single InGaAs/GaAs element encapsulated in two dimensions by the $SiO_2$ template, was defined with quarter symmetry. The boundary conditions of the model were dictated by approximating the thermomechanical properties experienced during the deposition in the MBE chamber. Depicted in figure 3.3.2 (a), each layer was specified with a reference temperature, corresponding to the temperature with which it was deposited, from which a thermal strain was calculated by taking its difference relative to the temperature of interest. The substrate was approximated by its first 700 nm with a roller condition on its bottom surface preventing Z-axis translation. A convergence study, not shown, confirmed negligible (< 1%) variation down to this thickness. All external surfaces were treated as perfectly insulated except where temperature was specified at the bottom surface of the substrate and swept from 600 °C to 20 °C. The thermal stresses of interest were computed using linear-elastic constitutive relations and Navier's equation at quadratic gauss points from the calculated thermal strains.

Figure 3.3.5 (a) - (d) illustrate the temperature evolution of the stresses seen in a cross-section of the entire geometry as it is cooled from 600 °C to 20 °C. As the stack is cooled to 400 °C, stress concentrations evolve from the intersection of the Si substrate, $SiO_2$ mask and GaAs nucleation layer. This is primarily attributed to significant variation in thermal expansion coefficient and stiffness between the three materials, but there is also a geometric contribution due to the corner. Further reduction in temperature to 200 °C provides additional stress build-up at the patterned substrate vertex as well as shear-lag effects which can be seen be propagating through the lower GaAs layers (the buffer layer and the nucleation layer) from both the template and, to a lesser effect, the substrate. Upon reaching the final temperature of 20 °C the largest stress concentrations are observed between the template and the substrate with moderate stress propagation into lower GaAs regions at a tensile magnitude of approximately 200 MPa.

An evaluation of this stress transmission into the InGaAs layer is provided in figure 3.3.5 (e) and (f) for the temperature of interest. As expected, the largest stresses are propagated from the corner of the layers beneath while the majority of the volume experiences a uniform tensile stress. Once fully cooled to 20 °C, the stress magnitude is approximately 40 MPa throughout the area with a variation of 15 MPa through its thickness. Additional variation at the edges is observed in the form of rippling and is due to the shear lag and pinning effects of the lower layers (the nucleation layer, buffer layer, and the bottom barrier layer).

Compared to conventional $10^1 – 10^2$ GPa thermally induced stress build-up for the directly deposited GaAs on Si, the simulation results indicates the great amount of reduction of it. Evidenced further by the line-scan profile in the diagonal direction (from the edge to the center) on the InGaAs layer shown in figure 3.3.6, we can notice that the thermal stress is mainly concentrated at the corner vertexes of the square pattern leading to less cracking and smoother

surface morphology throughout the most grown area as we obtained from SEM and AFM characterizations. By means of the patterned growth scheme in this study, we could hereby obtain the InGaAs/GaAs DH with reduced defect density and the improved crystallinity/interface conditions.

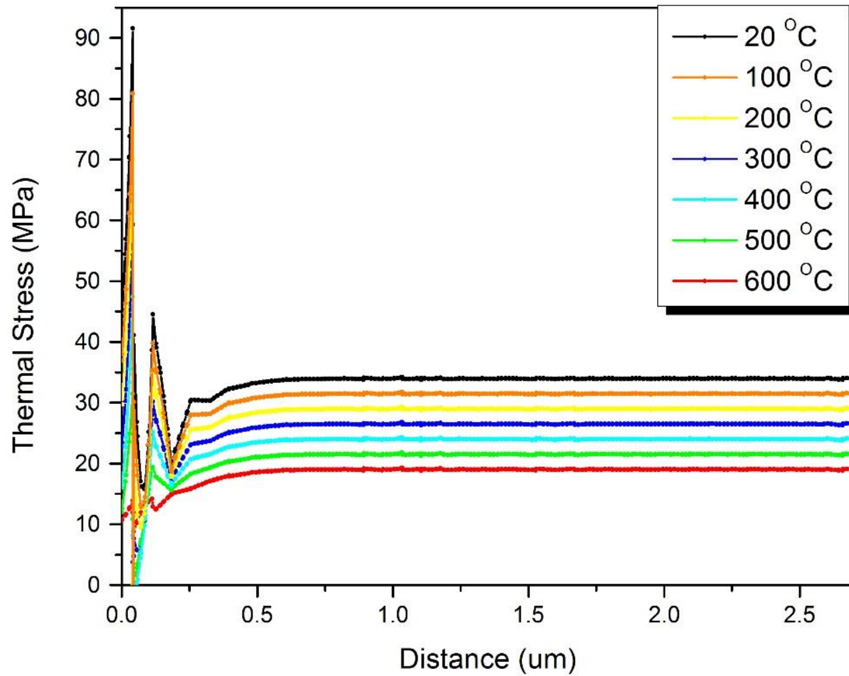



Figure 3.3.6: Thermally induced stress line-scan profile in the diagonal direction (from the edge to the center) on the InGaAs layer for all the temperature steps during the cooling process.

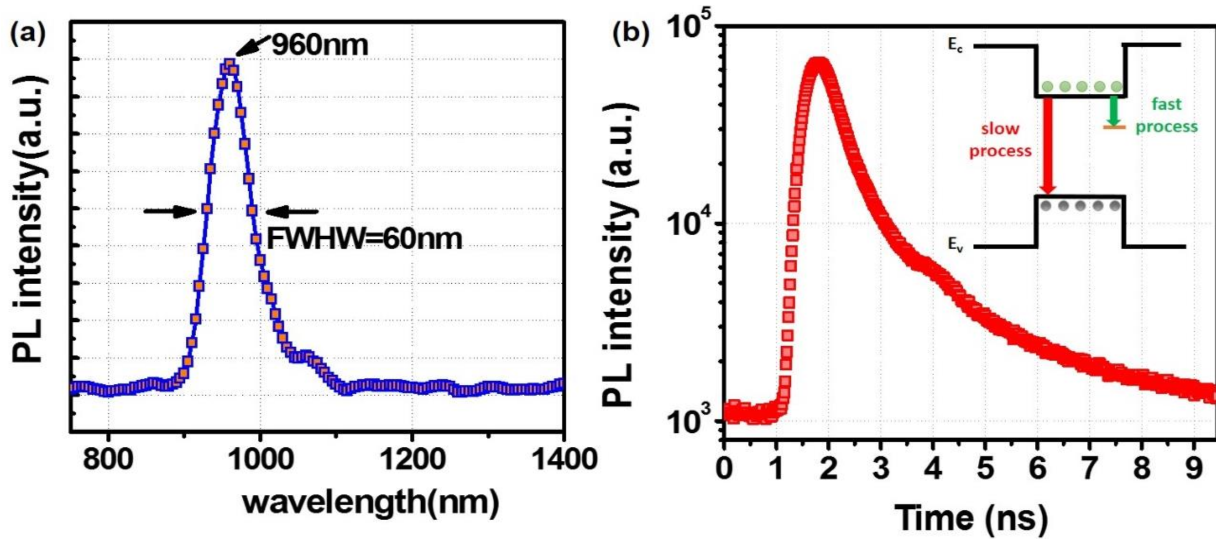



Figure 3.3.7: (a) Low temperature (77 K) μ-PL spectrum from InGaAs/GaAs DH on a patterned Si substrate, and (b) The semilogarithmic plot of the TRPL intensity for the ground state emission. Inset: schematic illustration of the carrier dynamics in the DH (the brown horizontal line indicates any types of trap center in the forbidden gap).

Figure 3.3.7 (a) shows the μ-PL spectrum at 77K for InGaAs/GaAs heterostructures within the hole arrays. We observed the only peak at about 960 nm representing the strong direct band-to-band ground state optical transitions in InGaAs/GaAs DH with indium compositions of about 15%. The full-width-half-maximum (FWHM) of the emission spectra is measured to be 60 nm which is close to or even better than some of the previous reported results[99]. This indicates an excellent optical property of the light-emitting medium with reduced defects and stacking faults at the GaAs/Si interface. Figure 3.3.7 (b) shows the measured TRPL data for the ground state PL emission at 77 K. The pump energy is 1.95 eV which is above the GaAs bandgap and the average pump intensity incident on the sample is as low as 100 W/cm$^2$. At this excitation level, only the ground state in the InGaAs well layer is filled out with the carriers. Hence, the rise dynamics of

the corresponding emission is analyzed. The PL signals first rise with a measured time constant of 140-180 ps which is extracted by fitting the PL data with monoexonential fits. It should be noted that the rise time is the time required for the carriers to be captured and relaxed into the ground state of the DH. Since the rise time is much shorter than the measured carrier lifetime as mentioned later on, there is no relaxation bottleneck in these DHs, i.e., all carriers relax to the ground state before recombining.

The decaying part of the TRPL relative intensity can be described by a biexponential decay function[100]: $A_1$ exp(-$t/t_1$) + $A_2$ exp(-$t/t_2$), where $A_1$ and $A_2$ are the amplitude ratios and $t_1$, $t_1$ decay time constants. The fast decaying lifetime $t_1 = 0.45$ ns, the slow decaying lifetime $t_2 = 3.7$ ns and the amplitude constants $A_1 = 3 \times 10^6$, $A_2 = 9 \times 10^4$ are obtained from the fitting using the Levenberg-Marquardt algorithm[100]. Biexponential decays may here be interpreted as the fast and slow processes relating to the nonradiative recombination through carriers capture/trap into the defects either in the bulk or the DH and the radiative recombination, respectively. Thus, the slow decaying time constant $t_2 = 3.7$ ns could be attributed to the radiative lifetime of the carriers which is in a reasonable agreement with values met in the literature[101-102] for InGaAs/GaAs DHs. A good figure of merit of evaluating the radiative recombination efficiency in such DHs is the relative magnitude of the slow decaying component to fast decaying component $A_2/A_1$[103-105]. This ratio is measured to be as low as 0.03 in the InGaAs/GaAs DHs, indicating that the nonradiative processes are dominant. These nonradiative processes are mainly governed by the defects, dislocations in the bulk or DHs introduced during the epitaxial growth. Through a further optimization of the epitaxial growth and reduction of the defects in the as-grown samples, it is expected that the radiative lifetime will increase along with the enhancing decaying component, i.e., $A_2/A_1 > 0.5$[106]. The growth optimization process for the defect-free epilayers is in progress and will be reported.

### 3.3.4 SUMMARY AND CONCLUSIONS

The successful demonstration of InGaAs/GaAs DH grown on the exactly oriented Si patterned substrates is reported. The patterned growth scheme along with the two-step growth technique help realize the high quality GaAs buffer layer leading to the atomically sharp and nearly defect-free interface. As evidenced by XRD and TEM study, the single crystalline and epitaxially grown nature are the major factors contributing to the high yield PL. The remarkable reduction of the thermally induced stress during the cooling process through the square pattern design also plays a very important role for good material structural quality. However, there is still much room to further improve the misfit dislocation density as to make the room temperature luminescence possible.

# Chapter 4

## Future Work

Following the successful monolithic integration of InGaAs/GaAs onto square-shape Si(111) patterned substrates, it comes to the point to think about the improvement. Since it's been proved thermally induced stress has played an important role in the epilayer quality, it's worth thinking about the dominant factors in addition to the pattern window shape. The most noticeable factor would be the material property of the dielectric mask material itself. As listed in the table 4.1 below, the coefficient of thermal expansion of $Al_2O_3$ is quite similar to that of GaAs as well as the much larger Young's modulus of $Al_2O_3$ mask. In this way, we should expect to have more synchronous expansion/contraction activity between the dielectric mask and the epilayer in the cooling and heating processes. In addition, the stiffer $Al_2O_3$ could provide a counter stress to ease the strong tensile stress build-up during the cooling process at three dissimilar materials junction corner. In the following figure 4.2 and 4.3, the simulation results in COMSOL display the justification.

| | $Al_2O_3$ | SiO2 | GaAs | Si |
|---|---|---|---|---|
| **Young's modulus [GPa]** | **400** | **70** | **75.3** | **185** |
| **Thermal conductivity [W/m·K]** | **35** | **1.4** | **46** | **130** |
| **Coefficient of thermal expansion x $10^{-6}$ [1/K]** | **6.5** | **0.5** | **6** | **2.6** |

Table 4.1: Material stiffness and thermal properties concerned in the patterned growth scheme[103].

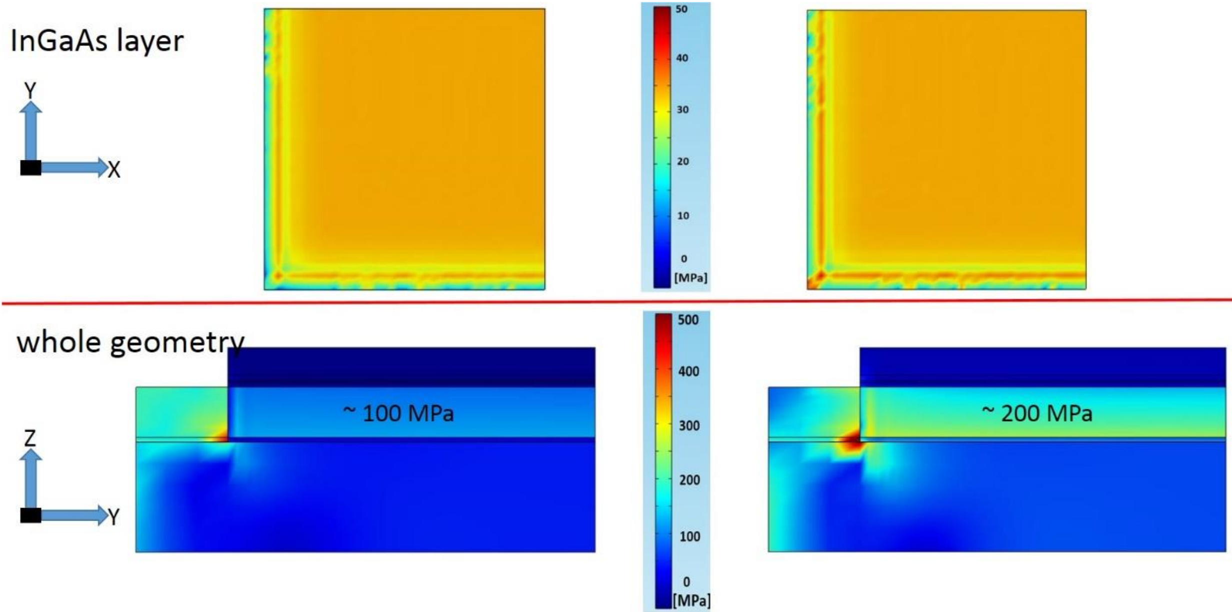



Figure 4.2: Thermal stress distribution in the InGaAs layer (top row) for the $Al_2O_3$ masked template (Left column), $SiO_2$ masked template (Right column); and the cross-section views of whole quarter geometry (bottom row) for the $Al_2O_3$ masked template (Left column), $SiO_2$ masked template (Right column). The thermal stress distribution displays the $Al_2O_3$ masked template is a promising choice to further relax the thermal stress by confining the stress at the corner and dielectric.

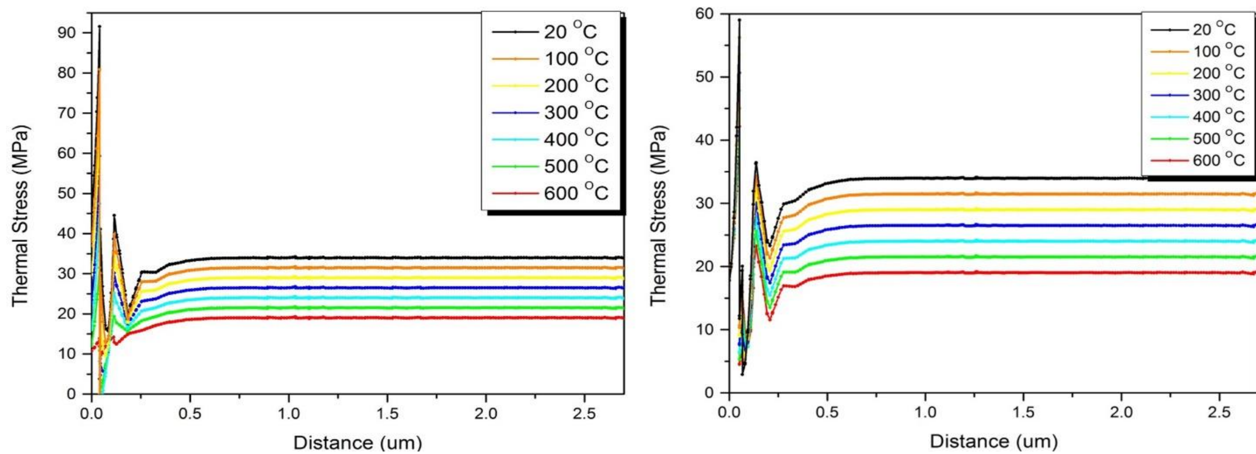



Figure 4.3: Thermal stress magnitude line scan from the edge to the center (in the diagonal drection) in the 4 um windows for the $SiO_2$ masked template (Left), $Al_2O_3$ masked template (Right).

From the COMSOL simulation results based on the same model built up in Chapter 3, we could find the $Al_2O_3$ masked template could offer even better thermal stress relaxation through the comparable coefficient of thermal expansion to GaAs and the stiffer characteristic of this material itself. The tensile stress from the cross-section view shown in figure 4.2 is only concentrated at the corner and not even propagating into the GaAs nucleation/buffer layer. Figure 4.2 also displays the factor of 2 stress magnitude reduction in the nucleation and buffer layer when the InGaAs/GaAs grown on $Al_2O_3$ masked template as compared with $SiO_2$ masked template. Additional thermal stress variation at the edges is observed in the form of rippling and is due to the shear lag and pinning effects. Through the stress magnitude line scan of the InGaAs layer (in the diagonal direction: starting from the edge to the center) as shown in figure 4.3, $Al_2O_3$ masked template also helps reduce the stress magnitude by a factor of 1.5 at the edge of the template when compared with the $SiO_2$ counterpart. Hence, I could conclude $Al_2O_3$ masked template could be a very promising replacement for the originally used $SiO_2$ one to offer even better epitaxial thin films.

Overall, the patterned growth scheme of active GaAs based optoelectornics is still a very promising research topic. Through the controlled heteroepitaxy by MBE, it’s expected to really fulfill the efficient and durable GaAs based lasers on exactly oriented Si substrates.

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