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High Speed DSP Circuits and Systems for 60 GHz Wireless Communication

A dissertation submitted in partial satisfaction  
of the requirements for the degree Doctor of Philosophy  
in Electrical Engineering

by

Frank Hsiao

2013

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## ABSTRACT OF THE DISSERTATION

High Speed DSP Circuits and Systems for 60 GHz Wireless Communication

by

Frank Hsiao

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor M. –C. Frank Chang, Chair

The unlicensed 60 GHz band provides new opportunities for short ranged indoor Gb/s wireless communication applications. Compared with III-V semiconductor process technologies, nanometer CMOS based 60 GHz transceivers are attractive from the manufacturing cost and low power consumption point of view but these sensitive mm-Wave transceivers are highly susceptible to process variations thus they face a big challenge in achieving high

yield performance. This suggests DSP based calibration circuits and algorithms to compensate for the performance loss due to process variations. In the first part of the dissertation, DSP based “Self-Healing” circuits and systems are presented to perform concurrent calibration on multiple RF transceiver parameters such as noise figure, image, transmitter IQ mismatch, and DC offset to optimize the 60 GHz CMOS transceiver performance. Digital baseband circuits applied to probe and measure the RF parameters such as direct digital frequency synthesizer, FFT based spectrum analyzer, and self-healing calibration controller will be discussed for a 4 Gb/s 60 GHz self-healing transceiver SOC in 65nm CMOS process.

In the second part of the dissertation, the focus will be on the implementation aspects of a digital modem for a multi-Gb/s 60 GHz SOC radio. A 7 Gb/s OFDM/Single-Carrier frequency domain equalizer in 65 nm will be presented as an example. 4-parallel signal processing architecture allows this equalizer chip to achieve a symbol sampling rate of 1.76 GS/s while the core DSP circuits are clocked at 1/4 the input symbol rate. This equalizer chip is equipped with a 512pt FFT processor and a 512pt IFFT processor to demodulate the received OFDM and single-carrier signals. It includes a time domain Golay correlator based channel estimator to obtain the multipath channel impulse response, and it also includes a MMSE equalizer for channel correction in frequency domain.

The dissertation of Frank Hsiao is approved.

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Sudhakar Pamarti

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Kung Yao

---

Lixia Zhang

---

M.C. Frank Chang, Committee Chair

University of California, Los Angeles

2013

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## VITA

- 2002                      B.S., Applied Mathematics  
National Chiao Tung University,  
Hsinchu ,Taiwan
- 2005                      M.S., Computer Science  
National Chiao Tung University,  
Hsinchu, Taiwan
- 2007                      M.S., Electrical Engineering  
University of Southern California,  
Los Angeles
- 2009                      Research Assistant and Teaching Assistant  
University of California, Los Angeles

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Sandeep D'Souza, **Frank Hsiao**, Adrian Tang, Sai-Wang Tam, Roc Berenguer, and M. F. Frank Chang, "A 10-bit, 2GS/s, DAC-DDFS-IQ-Controller Baseband enabling a Self-Healing 60GHz Radio-on-Chip" IEEE Transactions Circuits and Systems II, 2013

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## Chapter 1 Introduction

The unlicensed 7 GHz of bandwidth at 60 GHz have brought a lot of opportunities for short ranged multi-Gb/s wireless communication systems. Standards like IEEE 802.15.3c and 802.11ad have been established to promote wireless LAN or WPAN communication applications in the 60 GHz band [1],[2]. In these applications, it is highly desirable to reduce the power consumption and manufacturing cost so as to have an economically viable product. CMOS process technologies then becomes an evident solution for implementing the circuits for these 60 GHz communication applications. However, in ultra-deep-sub-micron CMOS process technologies, to maintain low cost and high manufacturing yield of the integrated circuits is often a very challenging task when the process statistical variations are high. Sensitive mm-Wave circuits will suffer a significant loss in yield due to the variations in linearity of the RF amplifiers. This implies some sort of circuit calibration or compensation to compensate the transceiver circuit parameters to improve the yield performance. These calibration mechanisms are usually DSP based digital circuits estimating some analog circuit impairment parameters and then performing compensation in either digital domain or analog domain. In this work, collective digital calibration or “Self-

Healing” of multiple circuit parameters on a RF transceiver is presented. On-chip Calibration or Self-Healing 60GHz circuits poses several additional challenges. At the system level, wide bandwidth and linear ‘sensors’ and circuit control ‘knobs’ are required to sense and tune or ‘heal’ the transceiver impairments. Digital Self- Healing algorithms must be able to correctly capture the characteristics of the transceiver and the digital circuits applied for Self-Healing algorithms must also be high-speed and wide bandwidth in order to accommodate the 60 GHz transceiver system. At the same time, the power consumption of these Self-Healing digital circuits and processors must be minimized so the extra overhead of installing the Self-Healing processing functions would be minimal and be suited for on-chip integration.

In the first part of the dissertation, 60 GHz communication and the radio impairments of a 60 GHz transceiver will be introduced. These RF circuit impairments along with nano-scale CMOS process variations causing the manufacturing yield loss will provide strong motivation for a Self-Healing based 60GHz transceiver. In this first part of the dissertation, the DSP Self-Healing algorithm will be presented and the details on the digital circuit implementations will be discussed.

In the second part of the dissertation, digital baseband signal processing for 60 GHz wireless communication will be presented. For standards such as IEEE 802.15.3c and IEEE 802.11ad, they both adopt Single-Carrier and OFDM modulation methods. For high throughput multi-Gb/s 60 GHz wireless systems, multipath channel equalization is one of the most challenging and area/power

consuming functions in the digital baseband modem. To compensate the channel induced ISI effects for these systems, OFDM modulation or time domain channel equalizers are widely applied. Single-Carrier modulation techniques usually apply time domain channel equalizer like DFE (Decision-Feedback Equalizers) and OFDM modulation typically apply a 1-tap channel frequency response inversion in the frequency domain. An equalizer applying OFDM-like 1-tap channel frequency response inversion process is preferred over time domain DFEs when transmitting in a 60GHz non-line-of-sight (NLOS) multipath channel environment where the root-mean-square (RMS) channel delay spread may exceed over 10ns or over 100 symbols when the transmission symbol rate is at 1GS/s. In this kind of a multipath channel environment, designing DFEs for single-carrier transmission systems requires a large number of feedback filter taps to compensate the multipath fading. The number of filter taps for these kind of DFEs used in wireless channel environment are usually proportional to the number of complex multipliers necessary to implement them since the wireless channel impulse response will change over time. In addition, the extra loop unrolling and the parallel look-ahead symbol decision hardware necessary to support multi-Gb/s throughput with complex modulations, e.g., 8PSK and 16QAM, makes DFEs impractical to apply in terms of area and power consumption. As a result, most previously reported Gb/s baseband DFEs for wireless baseband modems support only simple modulation methods like QPSK or MSK.

From the baseband system integration point of view, when implementing a combo OFDM and single-carrier modulation modem, it is highly desirable to have

an equalization hardware architecture that would fully utilize the FFT processor already required in the OFDM receiver to perform channel estimation, equalization, and other modem signal processing functions for the demodulation of single-carrier signals. Single-carrier frequency domain equalization (SC-FDE) then becomes an attractive and feasible low-cost implementation solution as its concepts and datapath are similar to those of an OFDM modem receiver.

In this dissertation, a 7Gb/s frequency domain minimum mean squared error (MMSE) equalizer chip for 60 GHz wireless communication system is demonstrated. 4-parallel signal processing architecture allows this equalizer chip to achieve a symbol sampling rate of 1.76 GS/s while the core DSP circuits are clocked at  $\frac{1}{4}$  (1.76 GHz/4=440 MHz) the input symbol rate. This 1.76 GS/s symbol sampling rate achieves the sampling rate required by IEEE 802.15.3c and IEEE 802.11ad standard and it is the first implemented equalizer to achieve this target symbol rate specification in 65nm technology node. This equalizer chip is equipped with a 512pt FFT processor and a 512pt IFFT processor to demodulate the received OFDM and single-carrier symbols. It also includes a time-domain Golay correlator based channel frequency response (CFR), and it also includes a MMSE equalizer for channel multipath compensation in the frequency domain. To verify the proposed equalizer chip at Gb/s throughput, differential input clock driver and low voltage differential signaling (LVDS) output drivers are also implemented in this chip.

The content of this dissertation is as follows. Different aspects of radio system design for 60 GHz radios are addressed in Chapter 2. In Chapter 2, a

baseline 60 GHz radio system is also addressed and it will be used as a comparison with the Self-Healing 60 GHz radio SOC presented later. In Chapter 3, RF impairments of the 60 GHz radios will be introduced and the concepts including the high level Self-Healing algorithms and architectures will be discussed. Chapter 4 will discuss the details on the DSP circuits applied for Self-Healing 60 GHz radio. The circuit specifications, design considerations, and architectures will be discussed. Also in Chapter 4, the Self-Healing 60 GHz radio SOC implementation results will also be presented. Chapter 5 focuses on the baseband modem implementation aspects of 60 GHz radio. The frequency domain equalizer will be applied as the main example on the data-path of a 60 GHz baseband modem. The performance and implementation results of the frequency domain equalizer will also be presented in Chapter 5. Finally, Chapter 6 summarizes the results and main conclusions of the dissertation and provides some thoughts for future research topics.

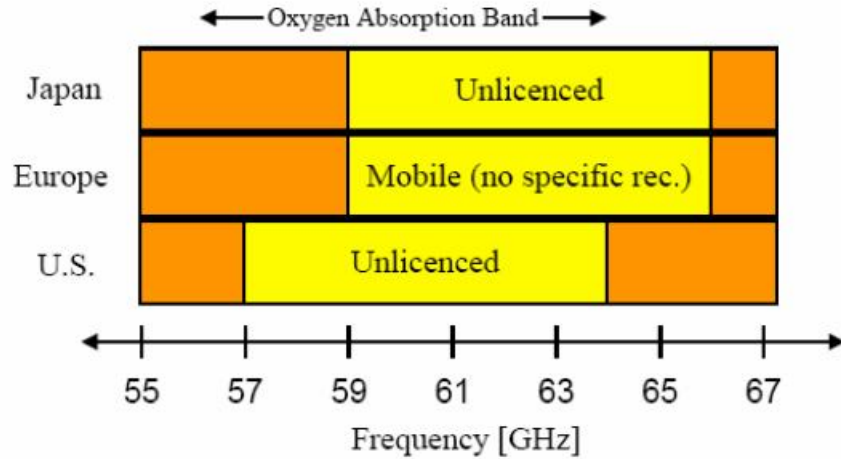
## **Chapter 2: 60 GHz Wireless Communication and 60 GHz Transceiver**

This chapter introduces 60GHz wireless communication and the motivation for high short ranged data rate wireless communication is first addressed. This is then followed by an introduction of 60GHz transceivers. Different architectures and major transceiver circuit blocks will be briefly discussed. The challenges of the transceiver operation at 60GHz are then highlighted. This is followed by a discussion on the design challenges of nanometer CMOS mm-Wave RF circuits due to process variations. The analog RF impairments are then summarized. Finally, a baseline 60GHz transceiver will be introduced this baseline transceiver will be used as a comparison with the Self-Healing 60GHz transceiver.

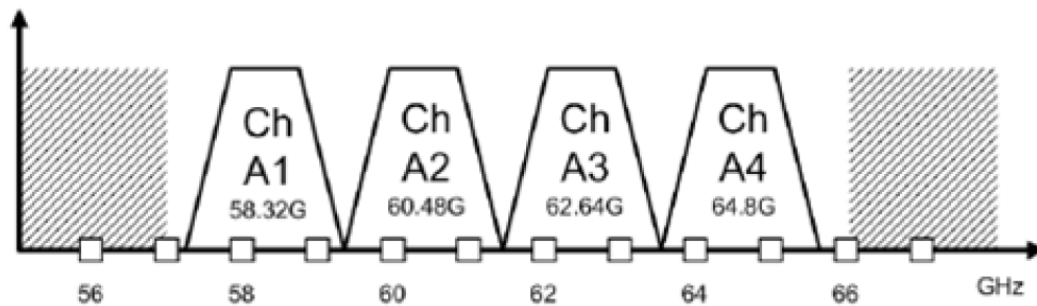
### **2.1 60 GHz Wireless Communication**

Over the past few years, advances in CMOS process technology and the need for wide bandwidth high-data rate wireless transmission have made mm-Wave technologies to attract a great deal of interest from university research groups and industry. 60 GHz mm-Wave technology offers several advantages over the current communications systems for high data rate wireless transfer. One of the main reasons is the 7 GHz of unlicensed bandwidth centered around 60GHz. This large unlicensed bandwidth brings potentials for Gb/s wireless applications like wireless uncompressed high-definition video transfer or high-speed wireless

data docking stations that allow multiple electronic devices to be connected without the actual need for the physical cable wires. Fig. 2.1 shows the unlicensed 60 GHz band in different regions of the world and the channelization of the 60 GHz for IEEE 802.15.3c standard.



(a)



(b)

Fig. 2.1 (a) Unlicensed 60 GHz band around the world and (b) Channelization of IEEE 802.15.3c

From the US Federal Communications Commission (FCC) regulations, 60 GHz communications are allowed with a much higher transmit power. The

equivalent isotropic radiated power (EIRP) for 60GHz communications are higher compared with 2.4GHz WLAN or 3.1 GHz UWB systems. This higher transmit power allows 60GHz wireless communication to overcome the higher path loss at 60GHz and confines the transmission environment to an indoor environment limiting a transmission link distance to around 10 meters or so. This also means that the effective interference levels for 60GHz are less than the WLAN systems located around 2.4 GHz and 5.2 GHz.

With this huge 7 GHz bandwidth available for 60 GHz communication applications, it makes system modulation design simpler. Low spectral efficiency modulation methods like BPSK, QPSK, or 16 QAM can be applied and making these systems easily achieve over 1 Gb/s. This makes a 60 GHz system an ideal candidate to support Gb/s wireless data transfer applying digital modulation. In standards like IEEE 802.15.3 or IEEE 802.11ad the total bandwidth at 60 GHz are further channelized into channels of around 2 GHz. Since 60 GHz operates at such a high RF carrier frequency, this allows multiple-antenna solutions to be implemented on-chip easily compared with the lower frequency WLAN systems. This will enable multi-antenna beamforming solutions to be implemented on CMOS offering higher integrated system at lower costs.

Of course, with all these benefits and advantages, short ranged communication at 60 GHz does not come without price and challenges. First of all, the design and modeling of 60 GHz building blocks of a transceiver becomes much more complex and delicate compared with lower frequency systems. At 60 GHz, small deviation in local oscillator (LO) frequency offset means a huge



timing and phase offset for the baseband modulation symbols and more effort is necessary for the baseband timing/frequency recovery algorithms. Also at 60 GHz or other mm-Wave frequencies, the design of active and passive devices in CMOS becomes more complicated [3]. The effects of layout parasitic must be carefully modeled or else a frequency down-shift between simulation and measurement results would occur decreasing the performance of the circuits.

One other major reason that is challenging for the 60 GHz wireless applications to become widely adopted in commercial mobile electronics is the power consumption. Since 60 GHz communication aims to target Gb/s throughput with simple low spectral efficiency modulation, this means that the mixed-signal circuit blocks like ADC (analog-to-digital converters) or DAC (digital-to-analog converters) will be power hungry running at an order of GS/s. For the digital baseband modem, even at advanced CMOS technology nodes like 65nm or 40nm, 4-parallel DSP processing or 8-parallel DSP processing must be implemented to meet the symbol sampling rate requirements of 1.76 GS/s defined by IEEE 802.15.3c or IEEE 802.11ad. Parallel processing means multiplication of datapath hardware by 4 or by 8; this implies the increase of power and area consumption to accommodate the Gb/s transmission link. How to effectively come up with datapath architectures with low power consumption will be a major challenge before 60 GHz wireless applications can be widely adopted in the indoor mobile electronic devices.

## 2.2 60 GHz Wireless Transceiver

In this subsection, the 60 GHz transceiver designed at UCLA HSEL and its major circuit block will be briefly described. This transceiver will be used as the baseline transceiver and be later on compared with the Self-Healing 60 GHz transceiver to demonstrate the effectiveness and the necessity of Self-Healing on mm-Wave 60 GHz circuit blocks to increase the effective yield.

The baseline 60 GHz transceiver designed by various members of UCLA HSEL is shown in Fig. 2.2. [4], [5], [6], [7]. At the baseband transmitter side, the input digital data bits are first modulated and then converted to analog voltage signals by driving the I/Q quadrature DACs. Following the DACs are the 3<sup>rd</sup> order inverse Chebyshev antialiasing filters with 1GHz cut off frequency. This means that the DACs has to operate at 2GHz and the symbol signaling at the digital baseband modulator also has to transmit at 2GHz clock frequency to avoid signal aliasing. At the baseband receiver side, to cope with the transmitted signal, the baseband analog signal is converted to digital by applying a 4-parallel time-interleave 7b ADC also clocked at 2GHz. The baseline 60 GHz transmitter and receiver have been designed using a 2-stage heterodyne architecture. Although direct conversion (DC) based architecture would greatly reduce the system hardware complexity by removing the IF (intermediate frequency) stage and image reject filters. However, the stringent amplitude and phase mismatch requirements on the I and Q channels makes it very hard to achieve the targeted 0.1 dB gain mismatch and 10° degree phase mismatch at 60 GHz in the implemented design considering layout and circuit matching. Therefore the

traditional 2-stage heterodyne transceiver architecture is adopted in the baseline 60 GHz transceiver. In the baseline 60 GHz transceiver the intermediate frequency (IF) stage is at 12 GHz followed by RF mixers to convert the signals up and down from 12 GHz to 60 GHz carrier frequency. On the transmitter side, the I/Q DAC outputs are first converted to 12 GHz by applying quadrature up-conversion mixers. In the second stage, a single mixer up converts the 12 GHz IF signal to 60 GHz. Then, the 60 GHz up converted signal is amplified by a 3-stage fully differential transformer based power amplifier (PA) with a saturated output power (PSAT) of 14.85dBm and power-added-efficiency (PAE) of 16%. On the receiver side, the LNA is followed by an single-side-band RF-mixer converting the signal from 60GHz to 12GHz IF, followed by quadrature IF mixers that further mix down the 12 GHz signals to baseband. The 60 GHz RF synthesizer that generates the 12 GHz and the 48 GHz LO signals are generated by a wideband and low phase noise integer-N PLL. In the baseline 60 GHz transceiver, two identical PLLs are included on the transmitter and the receiver to support the frequency duplex division (FDD) operation which is defined by the 802.15.3c standard. The block diagram of the baseline 60 GHz transceiver is shown in Fig.

2.2

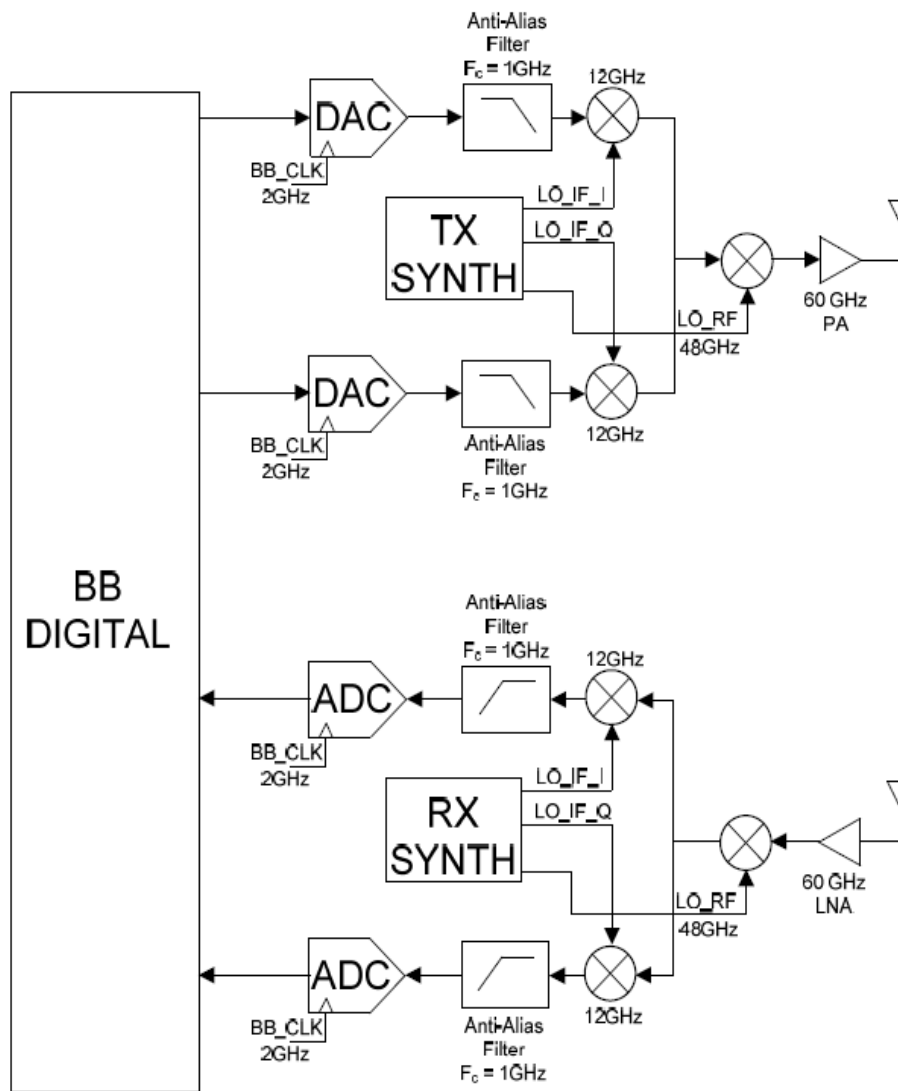


Fig. 2.2 Baseline 60 GHz transceiver

## **2.3 Nanometer CMOS Process Variations Effects and 60 GHz RF Circuit Impairments**

This section will discuss the CMOS process variation effects and its impact to 60 GHz circuits design followed by the discussion of 60 GHz RF circuit impairments. This will bring out the motivation of digital calibration to aid the analog circuits to overcome the process variation and inherent circuit impairments.

With the advances of CMOS transistor scaling, integrated SOC systems have become more and more popular. However, with the performance increase of the transistors at the nanometer process technology, it also brings increased statistical process variations in and decreased their yield performance. One common example would be the drift of transistor threshold voltage ( $V_t$ ). These process variations across the wafer will lead to die- to -die performance differences which increases the circuit design efforts to cope with these process variations. Fig.2.3 shows the performance lost due to scaling variability [9]. This scaling variability caused from process variations resulted from the manufacturing variations such as threshold voltage, gate length of transistors, and wiring interconnect process variations will lower the yield performance of the integrated circuits as CMOS process scales.

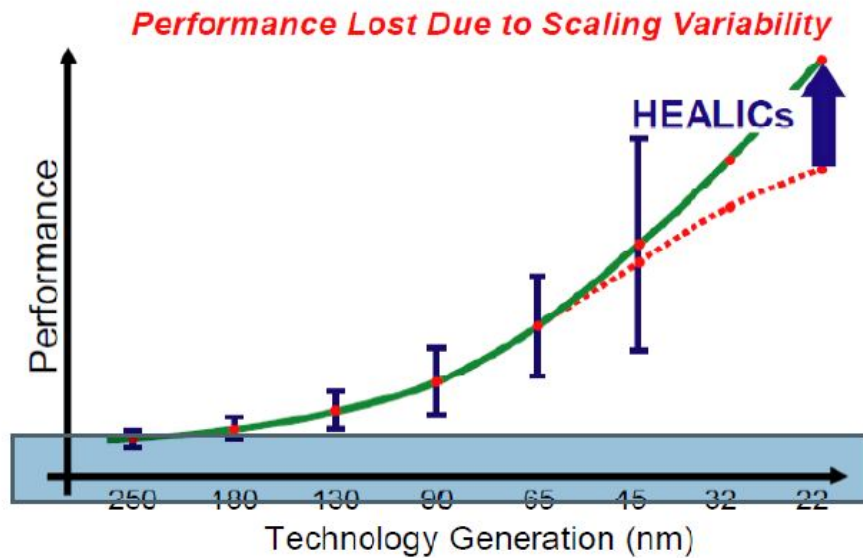


Fig. 2.3 Performance lost due to scaling variability

The performance loss due to scaling variability for nanometer high-performance circuits has resulted Defense Advanced Research Projects Agency (DARPA) to formulate a research program on ‘Self-Healing of RF/Mixed-Signal Integrated Circuits’ or the ‘Healics’ program. The main motivation for this Healics program is to introduce the process invariant digital circuits and systems to correctly calibrate or ‘heal’ the analog impairments caused by the process variations. Therefore, in a Self-Healing transceiver, it would include some digital and analog circuits that could sense or measure the circuit impairments, and these undesired circuit impairments can be corrected or healed by the self-healing circuits in presence of process variations and different operating environments. With self-healing functions included in a 60 GHz transceiver, the effective manufacturing yield would increase compared with a baseline 60 GHz transceiver

and in result the approach of adding self-healing functions to the baseline transceiver would lower the overall manufacturing cost.

Recently, the self-healing or autonomous calibration concepts have been applied in smaller scaled circuit blocks like PLL or in a power amplifier [10]. They do not optimize the various analog circuit impairments concurrently, and tradeoffs of calibrating each circuit parameters are not well considered as a system. Therefore, as the major part of the dissertation and also the research work of various UCLA HSEL members, the research of a self-healing transceiver that considers the analog RF transceiver impairments concurrently which is suitable for calibrating a complete transceiver is investigated.

To summarize Chapter 2, the radio impairments generated by non-ideal circuits in a 60 GHz radio are discussed and they serve as the main parameters the self-healing 60 GHz radio is trying to correctly calibrate. In here, we begin with the system link budget and discuss the impacts of radio impairments on the system link budget. In the system link budget, one of the final performance factors we care in the system is the bit error rate (BER) or the packet error rate (PER). With the targeted BER, one can determine the required  $E_b/N_0$  for this system. This  $E_b/N_0$  is defined as the energy per bit normalized against noise. With the information about the data rate  $R$  and the transmission bandwidth  $B_T$  the link signal-to-noise ratio (SNR) as:

$$\frac{S}{N} = \frac{E_b}{N_0} \left( \frac{R}{B_T} \right) \quad (2.1)$$

This SNR is required for a given modulation to achieve the targeted BER. By accounting the circuit impairments into the SNR the signal-to-noise-and-distortion (SNDR) ratio can be defined. And SNDR is defined as:

$$SNDR = \frac{S^2}{N_0 + \sum_{k=1}^M D_k^2} \quad (2.2)$$

Where in (2.2),  $S^2$  is the signal power,  $M$  is the number of different impairments,  $N_0$  is the thermal noise power, and  $D_k^2$  is the distortion power contributed from various different impairments. From (2.2), it can be seen that with more impairment distortion power it will result in lower SNDR making the system harder to achieve the targeted BER.

In the following, some of the circuit impairments the Self-Healing transceiver targets to correct or heal on will be discussed [11], [12], [13].

### **Thermal Noise:**

Thermal noise can be found in all physical electronic devices. The power spectral density can be represented by  $kT$ , where  $k$  is the Boltzmann's constant  $k = 1.38 \times 10^{-23} \text{ W}_s/\text{K}$  and  $T$  is the temperature in Kelvin ( $K$ ). Thermal noise is the main limitation on the RF receiver's sensitivity, and the receiver sensitivity is defined as:

$$\begin{aligned} \text{Receiver sensitivity} &= \text{Receiver Noise Floor} + \text{SNR} \\ &= \text{Thermal Noise} + \text{Receiver Noise Figure} + \text{SNR} \end{aligned} \quad (2.3)$$

In (2.3), the receiver noise figure  $NF = \text{SNR}_{\text{in}}/\text{SNR}_{\text{out}}$  is defined as the ratio of the output SNR to the input SNR for a functional block in the receiver. Lowering the



receiver noise figure is one of the key factors in lowering the SNDR. By tuning the gain stages of the receiver low noise amplifier (LNA), the receiver noise figure (NF) can be adjusted at the cost of receiver gain and linearity performance which also impacts on the overall SNDR. Fig.2.4 shows the effect of the thermal noise on the signal degrading the overall SNDR.

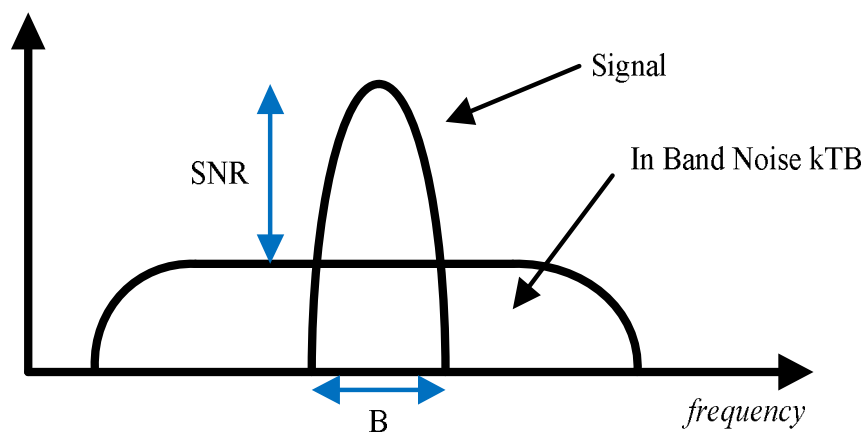


Fig. 2.4. Thermal noise contributing to SNDR degradation

### **IQ mismatch:**

IQ mismatch is a circuit impairment that happens during the up conversion or down conversion of the baseband or IF signals to the RF band. The conversion process shifts the local oscillator (LO) by 90 degrees to produce the quadrature sinusoidal components. It is impossible to achieve a perfect matching in layout or devices on both the I-branch and Q-branch of the LO and this gain and phase imbalance is the source to IQ mismatch. IQ mismatch is much more severe for direct-conversion (DC) receiver architectures since the conversion process

happens at 60GHz. Although, in the baseline 60 GHz transceiver the conversion is done at IF 12 GHz, the effects of IQ mismatch cannot be neglected and must be compensated for in the self healing transceiver. Assuming that the gain mismatch error is defined as  $20 \log \frac{1+\alpha}{1-\alpha}$  dB and the phase error is  $\phi$  degrees. Then the IQ imbalance of the mismatched LO output signals can be represented as

$$\begin{aligned} &2(1+\alpha)\cos(2\pi f_c t - \phi / 2) \\ &-2(1-\alpha)\sin(2\pi f_c t + \phi / 2) \end{aligned} \tag{2.4}$$

where in (2.4)  $f_c$  is the carrier frequency. IQ mismatch will cause the modulation symbol constellation to expand or compress in amplitude due to gain error and the constellation to rotate due to the phase error. The implications to self-heal this IQ mismatch would be some sort of gain adjustment at either transmitter side or receiver side to correct the gain mismatch. For 60 GHz systems, to correct the phase mismatch, rotating the initial signal constellation in the digital baseband transmitter side, or rotating the constellation in the baseband modem side would be the solution. Trying to correct the gain or phase mismatch in the analog domain and at 60 GHz would be very difficult. Designing high resolution and high frequency phase shifters themselves would face the problem of insufficient granularity. Also, the analog phase shifter themselves also suffer from process variations making the calibration at 60 GHz RF domain more difficult compared with digital baseband calibration. To measure the IQ mismatch, the image-reject ratio (IRR) is measured. A tone can be sent through the transceiver chain and based on the magnitude of the image signal the IQ mismatch of the transceiver

can be estimated. Fig. 2.5 shows the spectrum of the fundamental signal and the IRR that depicts the IQ mismatch.

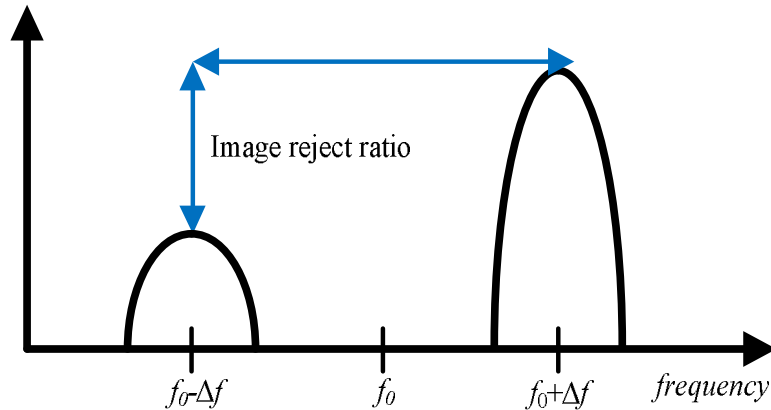


Fig. 2.5. Measuring IQ mismatch by measuring the IRR

### **Nonlinearity and Intermodulation distortion**

The RF amplifiers exhibit nonlinear behavior and saturating gain at large input levels. The nonlinearity of a RF amplifier is characterized by P1dB and 3rd-order-input-intercept (IIP3). When the RF transmitter or RF receiver amplifies different signals with different frequencies, intermodulation products raised from circuit nonlinearity lead to in-band distortion. This intermodulation effect must be decreased to an acceptable level to meet the required SNDR and BER specification. Other undesirable effects of intermodulation include spectral regrowth at the transmitter causing the spectral mask regulations to fail or large unwanted energy leakage at adjacent channels or interference to other electronics device occupying in the nearby spectrum. Fig. 2.6 shows the spectrum of the 2nd

order intermodulation (IM2) and 3rd order intermodulation (IM3) with input frequencies of  $f_0 + \Delta f_1 + \Delta f_2$  and  $f_0 + \Delta f_1 + \Delta f_2$ . To self-heal the intermodulation distortion, the self-healing transceiver must be able to first estimate the OIM2 and OIM3 and then be able to control the RF transceiver's bias, or amplifier gain to get a good tradeoff between non-linearity, noise, and gain performances.

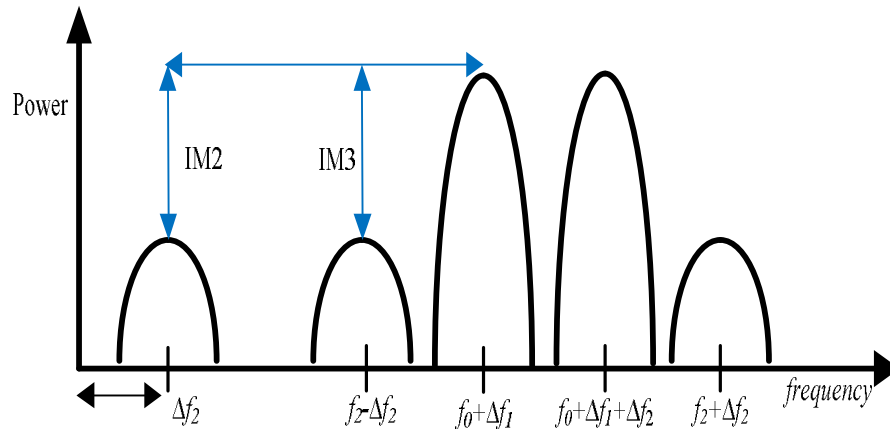


Fig. 2.6. Intermodulation impairments contributing to SNDR degradation

### DC Offset

The origin of DC offset comes from nonlinearity and self-mixing of the LO and RF input ports of a mixer. The leakage from LO can come back to the mixer input ports and mix with the LO itself. When the circuits have even-order nonlinearity, large DC offsets can arise. DC offset will saturate the different stages of the receiver, lowering the receiver dynamic range and eventually make the receiver fail. To heal the DC offset, the self-healing transceiver can first measure its nonlinearity by applying 1-tone or 2-tone test and then by applying

some offset cancelling technique by adding additional offset at the digital transmitter side

## **Chapter 3 Self-Healing 60 GHz Transceiver**

In this chapter the self-healing 60 GHz transceiver is discussed and the circuits necessary for self-healing functions as well as the algorithms to perform self-healing will be introduced.

### **3. 1 Top Level View of the Self-Healing Controller**

From Chapter 2, the concepts and motivations of self-healing for a RF transceiver to perform multiple parameter calibration were discussed. In this chapter, the architecture and the circuits for the self-healing transceiver will be introduced. From a top-level view, to calibrate multiple transceiver circuit parameters and monitor its performance and address statistical process variations, it would require some sort of a digital signal processor or ‘controller’ that acquires transceiver parameter information [11]. And based on the signal processor’s distortion analysis, the self-healing controller would be able to take actions and control the RF transceiver to impair with the impairment effects and perform transceiver optimization. The whole self-healing optimization loop would involve in digital, mixed-signal, and analog RF circuits to achieve these tasks. The self-healing controller itself would be in a form of a finite-state-machine equipped with different circuit calibration algorithms.

In summary, the basic flow of the circuit self-healing process is as follows:

- (1) Send out some probe testing signals through the transceiver chain.
- (2) RF Sensors to sense the environmental changes and be able to accurately respond to these environmental changes for the self-healing controller to monitor after the probe signals have been excited.
- (3) The transceiver circuit blocks have control ‘knobs’ for the self-healing controller to compensate for the process and environment variations. These knobs can be used to adjust various transceiver circuit parameters like bias, gain, capacitance, or current.
- (4) The self-healing controller continues on monitoring the transceiver and tune the circuit control knobs until the targeted circuit or microsystem achieve the final performance specification.

The whole self-healing optimization loop in the higher level can be summarized into 4 steps: (1) probe testing signal (2) sensors sense environmental changes (3) self-healing controller monitor the sensor changes (4) adjusting the circuit control knobs to optimize transceiver performance. A block diagram of the self-healing optimization loop is shown in Fig.3.1.

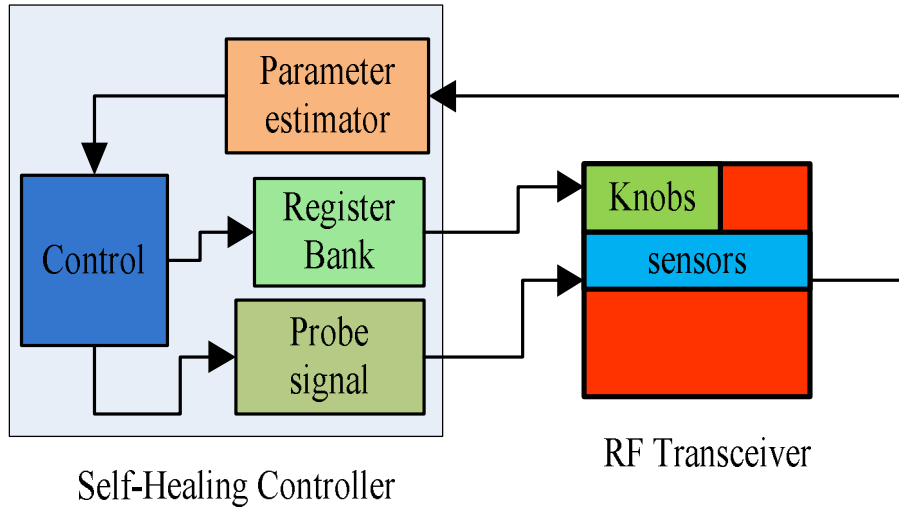


Fig. 3.1. High-level block diagram of the self-healing transceiver system

The goal of the self-healing system targeted by UCLA HSEL's Healics project is shown in Fig. 3.2. Prior to the self-healing, less than 75% of the transceiver dies would meet the target performance. After applying self-healing and calibrating for the process and environmental variations, more than 7% % of the dies would meet the target performance. By applying self-healing, the total effective yield of the dies would increase thereby reducing the total fabrication costs.



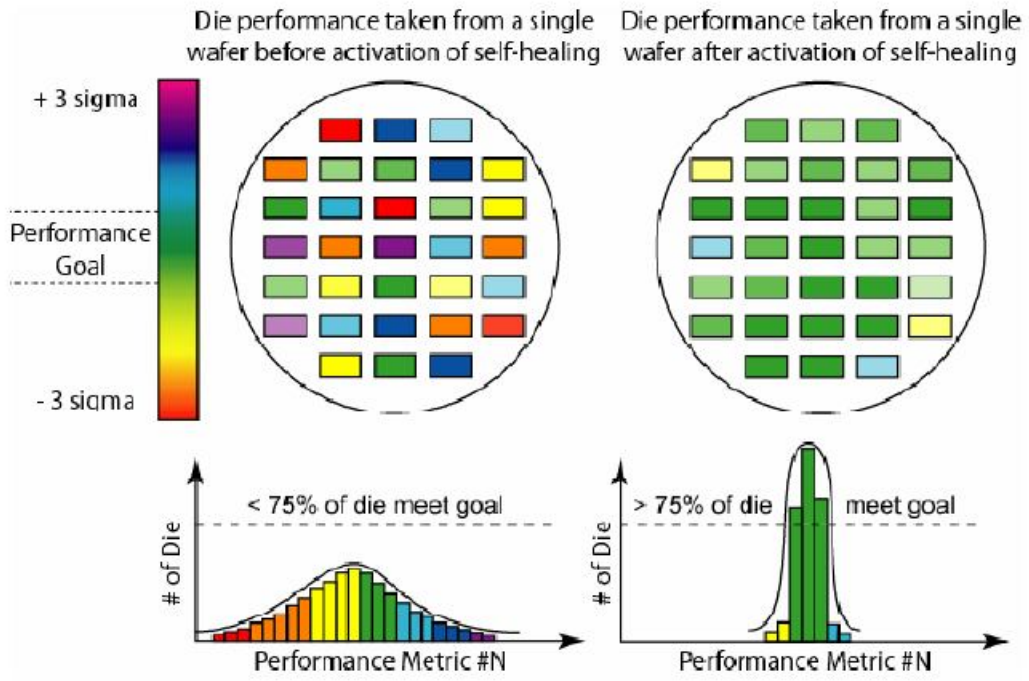


Fig. 3.2. Yield increase by applying self-healing

Now that the optimization flow of the self-healing controller has been introduced the circuits and datapath necessary for the self-healing controller can be investigated.

### 3.2 Circuits and Sensors for Self-Healing

#### Test tone generator

The self-healing controller needs to probe the mm-Wave 60 GHz transceiver before the transceiver status can be monitored [14]. This would mean some sort of a signal generator to send out test signals and excite the transceiver. Since the monitoring of the 60 GHz RF transceiver would involve in intermodulation and harmonics, a signal generator suited for this purpose would be one that can generate arbitrary 1-tone or 2-tone sinusoidal waveforms. Direct digital frequency synthesizer (DDFS) would serve this purpose of 1-tone/2-tone generation. One DDFS unit can generate a single tone. By combining the outputs of two DDFS together, two tone probe signals can be generated. Fig. 3.3 shows schematic of DDFS two tone generation.

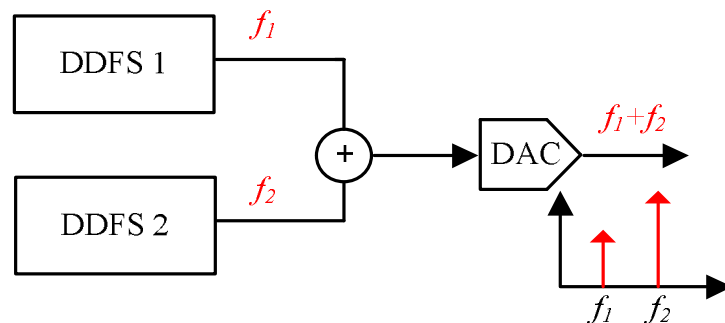


Fig. 3.3. DDFS two tone generation

## **Parameter estimator**

To monitor and the environmental changes and the spectrum of image or intermodulation signals, parameter estimator is needed in the self-healing controller. This parameter estimator is a FFT based spectrum analyzer that can estimate the output spectrum of the transmitter or receiver or various different RF sensors on the transceiver. To combat thermal noise, this parameter estimator can average over multiple FFT processing's to achieve the targeted SNR requirements. The design of the parameter estimator is further discussed in Chapter 4.

## **Auxiliary Mixed-Signal Data Converters**

To convert the digital outputs of the DDFS based signal probe generator to analog waveform, a digital-to-analog (DAC) is necessary. Initially an auxiliary high resolution but low speed and low powered DAC is desired to drive the probe signals. Having an auxiliary DAC has several benefits. First, the probe signal generator and the auxiliary DAC can be clocked at low frequency to save the power for self-healing. Second, at low frequency, it makes the DDFS probe signal generator design much easier. Third, high SFDR and effective number of bits (ENOB) on the auxiliary DAC can be easily achieved at low clock frequency thereby improving the overall sensing resolution of the self-healing controller. However, with the auxiliary DAC and the wide bandwidth signaling DAC both present on the integrated SOC, it makes the antialiasing filter solution complicated. Two sets of passive filters are necessary on the self-healing transceiver SOC, one for low frequency but high linearity 7 bit auxiliary DAC.

And one 5b DAC for high frequency 16-QAM complex modulation, but the linearity requirements are more relaxed for the signaling DAC. Also, a high linearity analog multiplexer is necessary to switch between the high resolution and the low resolution DACs making the dual DAC implementation impractical. Instead, the auxiliary DAC and the signaling DAC are combined together and replaced with a high speed 10b (7b ENOB) DAC to save power/area and the implementation efforts of the analog multiplexer and extra anti-aliasing filters. Fig. 3.4 shows block diagram of the two implementation strategies and (a) is chosen over (b).

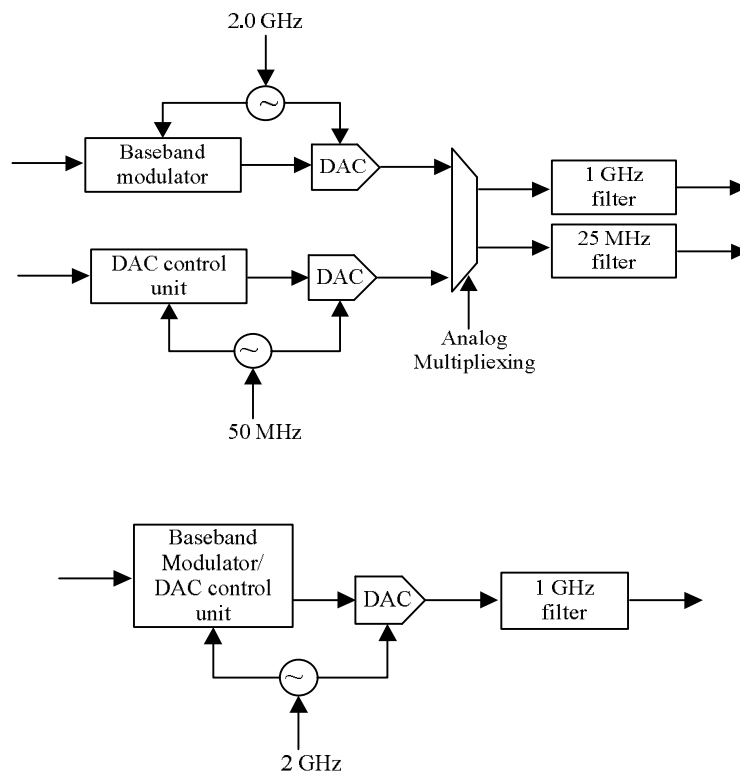


Fig. 3.4. (a) Dual DAC implementation strategy (b) Combined signal and auxiliary DAC

On the receiver side there are both a 10 bit 10 MHz auxiliary ADC for monitoring the changes of the RF sensors for self-healing purposes, and a 7b 2 GHz signaling ADC for 16 QAM signal demodulation. Trying to merge the auxiliary ADC and the signaling ADC together to a 10b 2 GHz ADC is much harder and the power consumption is much higher than keeping them separate. So for the 60 GHz self-healing transceiver, there are two sets of ADCs, the auxiliary ADC for self-healing and the signal ADC for demodulation.

### **Sensors and Tuning Knobs for Self-Healing**

Different RF sensors are placed at the 60 GHz self-healing transceiver for monitoring the system and environmental changes [15]. Temperature sensors are placed near the temperature sensitive circuits like the power amplifier (PA) or the receiver low noise amplifier (LNA). PA consumes a major portion of the transmitter power, overheating the PA will degrade the performance of the PA and the circuits close to PA. The temperature sensor on the receiver side is used to measure the noise power or  $kTB$  and this noise power can be applied to measure the noise figure (NF) thereby healing the receiver noise figure by tuning the gain stages of the LNA. To account for the temperature sensor's resolution fluctuation, the temperature sensor resolution is set to less than  $1^\circ\text{C}$  in order to be applied as noise reference. The analog outputs of temperature sensors are quantized by the auxiliary ADC to static digital codes and can be read directly by the self-healing controller.

To sense the intermodulation and nonlinearity behavior at the transmitter side, an envelope detector sensor is applied. The envelope detector is a squaring device which can down-convert the intermodulation distortion and the images to the baseband. With envelope detector, the transmitter IQ mismatch can be measured independent of the receiver chain. It's worth noting that the envelope detector's dynamic range must be larger than the intermodulation and IQ mismatch specifications which was defined at 40 dB and - 40dB. Once the probe signal is sent through the transmitter chain, the envelope detector output with the intermodulation can be digitized by the auxiliary ADC and its spectrum can be analyzed by the FFT based spectrum analyzer on the self-healing controller. By analyzing the intermodulation spectrum, the gain or the bias on the transmitter PA stages can be adjusted until it meets the targeted specification.

Power detector sensor is applied on the transmitter and coupled to PA output to measure the PA output gain and measure the P1dB. Again, the output of the power detector is digitized by the auxiliary ADC and the gain stages of the PA and can be adjusted until the transmitter meets the output P1dB requirements. The dynamic range of the power detector need not to be very strict in design, it only needs to detect  $\pm 5$  dB of the power centered on the output P1 dB.

The design of the tuning knobs on the transceiver circuit blocks like transmitter, PA, LNA, receiver programmable gain amplifier are critical to effectively heal the circuit parameters. Tuning knobs can be either analog or digital control knobs. For analog control knobs, based on the monitored results

like intermodulation spectrum or temperature output code, the self-healing controller can adjust the tuning knobs to change the settings of the analog RF transceiver circuits. These knobs include fine-grained biasing, capacitor bank tuning and varactors in an LC tank. These tuning knobs are present at the input of LNA and are adjusted to heal the noise figure or tune the frequency of the VCO on the PLL to optimize the phase noise performance. Digital control knobs can be regarded as the digital tuning of the DC offset, gain tuning, IQ phase rotation on the digital probe signals that drive the DAC. This predistortion or initial digital signal tuning can be applied to heal the intermodulation and the IQ mismatch effects of the 60 GHz self-healing transceiver.

### **3.3 Self-Healing Algorithms**

In this section we go into the algorithm and sequencing flow to heal each circuit or microsystem performance parameter of the self-healing 60 GHz transceiver [11].

#### **Transmitter Image Healing**

Transmitter image healing is the first step of the self-healing process. Once the image signal is suppressed it will make the transmitter output power measurement much straightforward. If the image issue is not resolved, the image signal cannot be distinguished from the actual signal. Transmitter image healing is accomplished by sending single-tone testing signals through the probe signal generator. The transmitter envelope detector is applied to capture the image signal

power. Since the envelope detector is connected to the auxiliary ADC, the spectrum of the transmitter and image signal information is captured by running FFT analysis on the on-chip PSD processor. The transmitter image is healed by adjusting the amplitude and phase control knobs on the DAC input or the DDFS IQ unit.

### **Transmitter Local Oscillator Leakage Healing**

To heal the local oscillator (LO) leakage, a single-tone probe signal is applied through the transmitter to the envelope detector. By measuring the spectrum of the envelope detector output, the LO leakage can be calculated by summing out the energy leakage on the FFT bins. To heal for the LO leakage, the IQ unit on the digital probe is adjusted until the LO leakage is below the required specification.

### **Transmitter P1dB Healing**

To heal the transmitter P1dB, a ramping signal with increasing power is sent from the DDFS probe signal generator. The increasing signal power level of the test tone is accomplished by tuning the digital gain control codes on the DDFS IQ unit. The output power information is captured through the power detector which is coupled with the PA. The transmitter gain can then be measured by computing the ratio between transmitter input power to the transmitter output power. The P1dB is the point where the output gain drops by 1dB.

### **Transmitter and Receiver OIM3 Healing**



To heal the transmitter or receiver's output third order intermodulation is to apply two tone signal generation on the DDFS probe to the transmitter or to the receiver. For transmitter OIM3 healing, once the two-tone signals are sent, the self-healing FFT PSD processor measures the spectrum on the output of the transmitter envelop detector. By tuning the control knobs of the PA bias and output gain stages, the OIM3 level can be adjusted. For the receiver OIM3, two-tone testing signals are generated from the DDFS and to the transmitter chain and sent to the receiver. The transmitter and the receiver are connected using a fixed power attenuator and the receiver OIM3 can be measured. Once the transmitter OIM3 is measured, the receiver OIM3 can be calculated. To heal the OIM3 on the receiver, the LNA knobs are adjusted to achieve the specification requirements.

### **Receiver Noise Figure Healing**

The receiver noise figure (NF) is defined as:

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{N_{in}}{A_{RX}/N_{out}} \quad (3.1)$$

Where in (3.1)  $A_{RX}$  is the gain of the receiver,  $N_{in}$  is the noise at the receiver input, and  $N_{out}$  is the noise at the receiver output. The input noise is equal to  $kTB$ , where  $k$  is Boltzmann's constant,  $T$  is the temperature, and  $B$  is the bandwidth. The temperature sensor on the transceiver can provide the value of  $T$ , and the bandwidth of the receiver is determined by the RX filter which is 1.2GHz. To calculate the receiver noise figure, only the output noise is left to be measured. To measure the output noise, the configuration shown in Fig. 3.5 is applied. When

no signal is present at the receiver, the output noise of the receiver can be measured by summing all values of the FFT bins on the parameter estimator. With this information, the noise figure of the receiver can be calculated, and then used to perform the NF healing. And to heal the receiver noise figure, the LNA input and output stage knobs are adjusted.

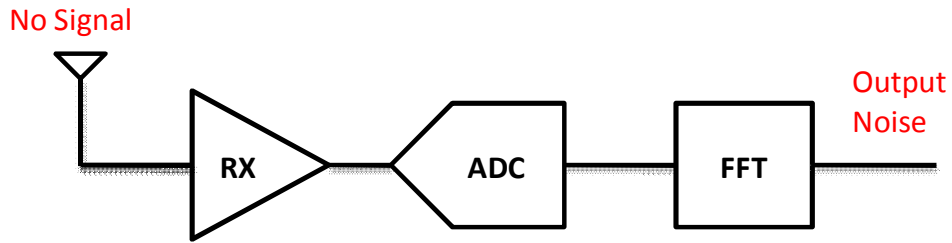


Fig.3.5. Measuring the receiver output noise



The signaling rate on this transceiver is designed at 1 GS/s. The DAC and the signaling ADC are both clocked at 2GHz. The modulation formats supported by this transceiver are BPSK, QPSK, and 16QAM. This translates to 4 Gb/s throughput. The digital circuits and systems collectively called as the self-healing controller on the self-healing 60 GHz transceiver are implemented in application specific integrated circuit (ASIC) style and this self-healing ASIC includes:

**ADC CTRL unit:** The ADC control unit is used to acquire the cyclic 10 MS/s auxiliary ADC digital outputs, and the digital outputs can provide the parameter estimator to perform spectral analysis or statistical averaging to aid on the monitoring of the RF transceiver sensors.

**Parameter estimator unit:** The parameter estimator unit is a 128pt FFT processor based spectrum analyzer. The bandwidth of this FFT processor is determined by the sampling rate of the auxiliary ADC which is 10 MS/s and this translates to a Nyquist frequency of 5 MHz. The frequency resolution of each FFT bin is  $10\text{MHz}/128 = 0.78 \text{ kHz}$ . Besides performing FFT analysis, the parameter estimator also computes the periodogram which is the estimated spectrum of the RF sensor outputs. The FFT processing within the parameter estimator unit can be configured to perform averages in any 2's power number from 32~1024. The outputs of the estimated spectrum are saved in the on-chip registers for read out.

**DAC CTRL unit:** The DAC control unit is a multimode signal function generator to drive the mixed-signal DAC. The DAC control unit throughput is at 2 GHz which is the same as the auxiliary/signaling DAC. The DAC control unit can

generate 1-tone or 2-tone sinusoidal signals for self-healing purposes or on-chip pseudo-random-bit-sequence (PRBS) based BPSK, QPSK, or 16 QAM modulation signals for transceiver loop back testing. Although the overall throughput of the DAC control unit is at 2 GHz, the internal architecture of the DAC control unit is running at 500 MHz and then time interleaved to 2 GHz to meet the timing requirements of the 65nm process.

**IQ unit:** The IQ unit is the digital predistortion and phase rotation unit of the DAC control unit. The IQ unit can add additional DC offset, gain control, and lookup table mapping for the digital outputs from the DAC control unit. By applying digital predistortion or phase rotation, it aids the self-healing controller in RF parameter monitoring and IQ mismatch correction.

**RF REG unit:** The RF register unit is a 256 register bank that stores the transceiver knob values in digital codes. It works with the self-healing controller as a storage unit that saves the current settings of the RF circuit control knobs. And by assigning different digital codes through the USART unit, the RF register unit can be reprogrammed into different knob settings.

**USART unit:** The universal serial asynchronous receiver transfer (USART) unit is the serial interface in which through the PC the self-healing transceiver can be configured and the self-healing algorithms can be initiated and sequenced. Also, all the control knob digital codes are written through USART, and the parameter estimator values can be read through USART to the PC for further post processing. The USART is clocked by a low frequency digital clock (<1 MHz)

provided by the PC to save the area and power for on-chip clock sources. Basically through USART all the complex self-healing algorithms can be initiated, reconfigured, and transceiver parameter values can be read out. The USART is the main platform for the self-healing transceiver testing and functional verification.

#### **4.1 DAC Control and IQ Unit**

The DAC control unit is a direct digital frequency synthesizer (DDFS) based 1-tone or 2-tone generator that can be used to generate probe signals for the 60 GHz self-healing transceiver and also provide modulation signals for transceiver loop-back tests. The high speed 2.0 GHz DAC can achieve 43 dB SFDR at Nyquist (1 GHz), this sets the limit on the SFDR performance of the DAC and DDFS combined chain. Therefore, the SFDR of the DDFS in this DAC control has to be kept larger than 50 dB SFDR to avoid signal degradation over the whole transmitter chain. Since this DAC control unit has to be clocked at 2.0 GHz using the CMOS 65nm process, the DDFS design is mainly challenged by the area available on chip and the strict timing constraint requirements [16],[17]. Therefore, the DDFS requires an architecture that applies simple and fast logics while maintaining SFDR above 50 dB.

The presented DDFS is a 2.0 GHz DDFS with I/Q quadrature output control. This DDFS design is able to generate quadrature signals with one-tone or two-

tones. These two quadrature carriers are out of phase with each other by  $90^\circ$ , and it is extremely useful in nonlinearity performance verification of wireless communication applications. Not only the frequency of the output waveforms is configurable, the amplitude scaling of the waveform amplitude can also be modified, and an offset to the amplitude can be added to either output by the IQ unit. These features are added to reduce the LO leakage for the RF transceiver. In addition, phase rotation can be added to the quadrature component. The I/Q rotation is implemented to compensate or predistort the I/Q mismatch effects in the transceiver.

The basic concepts for a DDFS are as follows [18]. Assuming that an  $N$ -bit frequency control word goes into the input of the phase accumulator and the output of the phase accumulator is an  $L$ -bit number where  $L$  is smaller than  $N$ . The  $L$ -bit code is used to select an entry in the ROM look up table. This means that the look up table will have  $2^L$  entries. The block diagram of the DDFS with uncompressed ROM is shown in Figure 4.2. The frequency tuning resolution and the SFDR of the DDFS can be increased by increasing  $L$ , but the number of entries in the look up table will increase exponentially consuming more area and power. If each entry in the look up table has a length of  $K$  bits, then the ROM has a size of  $2^L \times K$  bits. The higher the number of  $K$  is, the higher the SFDR the DDFS achieves.

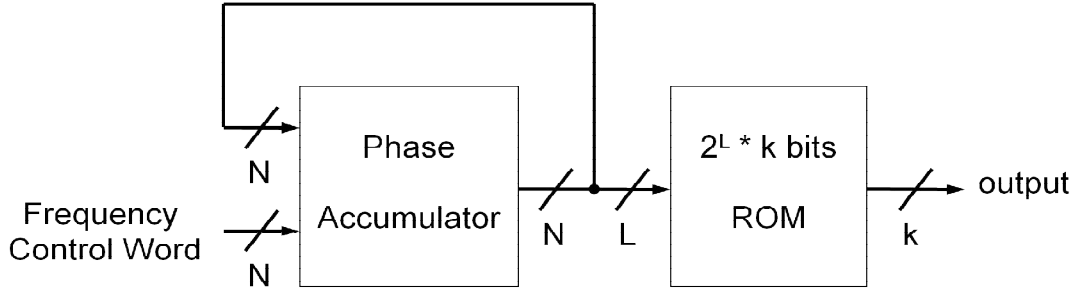


Figure 4.2. Block diagram of the DDFS with uncompressed ROM

In order to implement a DDFS with a fine resolution and high SFDR, a very large ROM size is required when the brute force look up approach is applied. A large ROM would imply a circuit with large area, large power, and computation delay. Therefore, aggressive compression and interpolation algorithms are desired in a DDFS design to reduce the size of the ROM look up table [19], [20].

### Taylor Series Approximation

In the proposed DDFS, Taylor series approximation based look up table is applied. The Taylor series is a representation of any function as the sum of infinite amount of terms calculated from the derivatives of this function at a given point [21]. If  $f(x)$  is the function, and point “ $a$ ” is the given point that the Taylor series is expanding from, then the Taylor series representation of this function is:

$$f(x) = \sum_{n=1}^{\infty} \frac{f^{(n)}(a)}{n!} (x - a)^n \quad (4.1)$$

where in (4.1)  $f^{(n)}$  denotes the n-th derivative of the function  $f$ .



Assuming that the DDFS generates a  $k$ -bit phase input  $\theta$ , the  $n$  MSB's of the phase input is denoted as  $\varphi$ , and the  $m$  LSB's of the phase input is denoted as  $(\theta-\varphi)$ . Then the sine and cosine values with the input phase  $\theta$  can be represented with the Taylor series expanding at point  $\varphi$

The first two terms in the Taylor series provides a very accurate approximation of the sine and cosine function. Instead of using a full sized ROM with  $2^k$  entries, only two ROM's are needed to store the values of  $\sin(\varphi)$  and  $\cos(\varphi)$  with size  $2^m$  and  $2^n$  respectively. The only drawback for this approach is that extra adder and multiplier are needed to implement this technique, and conventional multipliers are slow and area consuming. The block diagram of the Taylor series approximation based phase-to-sine converter on the DDFS is shown in Fig. 4.3.

The cosine wave is also generated with a similar architecture.

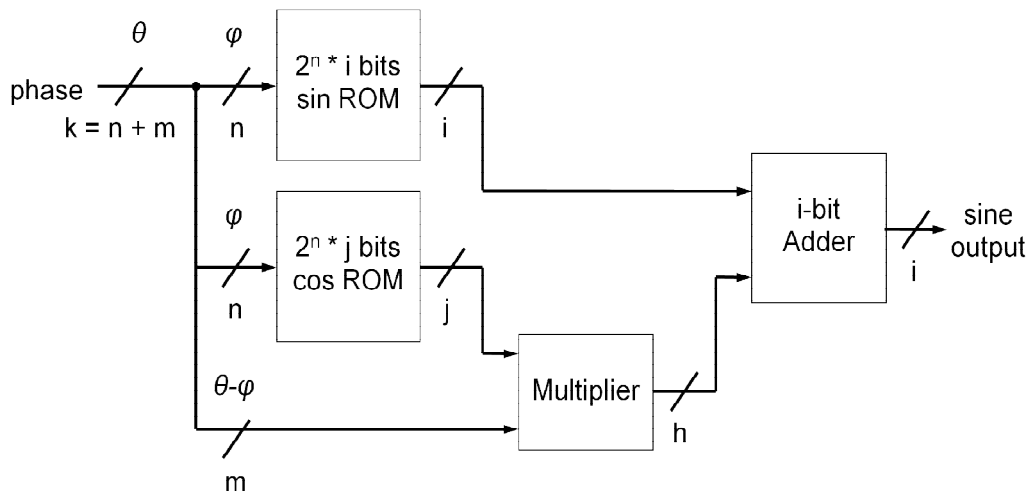


Figure 4.3. Block diagram of Taylor series approximation for sine wave output

Different ROM compression methods have been proposed in the literatures in the past and their compression ratio and SFDR performance are summarized in Table 4.1.

Table 4.1 SFDR performance of various compression techniques

References	Compression	SFDR
Ballaouar [22]	21:1	65 dBc
Conventional Taylor Series	64:1	97.04 dBc
Essenwanger [23]	67:1	97.23dBc
Eltawil [24]	157:1	64.6dBc

In the proposed DDFS architecture, the proposed ROM compression approach is modified from the Taylor series approximation and similar to the Taylor series linear interpolation technique referenced from [21]. With a phase input  $\theta$ , the sine and cosine values can be calculated as follows:

$$\begin{aligned}\sin(\theta) &= \sin(\theta_i) \pm \alpha(\theta - \theta_i) + \delta_{\sin} \\ \cos(\theta) &= \cos(\theta_i) \mp \beta(\theta - \theta_i) + \delta_{\cos}\end{aligned}\quad (4.2)$$

where  $\theta_i$  is the MSB of the phase input  $\theta$ , and  $(\theta - \theta_i)$  represents the LSB of the phase input  $\theta$ . The phase input  $\theta$  is a value between  $\theta_i$  and  $\theta_{i+1}$ , which are the two consecutive phase address used for the coarse ROM's that store the pre-determined sine and cosine values.  $\alpha$  and  $\beta$  are the pre-determined interpolation coefficients used to generate the fine correction to the sine and cosine values.  $\delta_{\sin}$  and  $\delta_{\cos}$  are the small errors introduced in the Taylor series linear interpolation method. Two coarse ROM's are used to store the sine and cosine values from 0 to

$\pi/4$ . The sine and cosine values were previously determined and translated into binary codes. 5 bits are used to access the coarse ROM and each ROM has  $2^5 = 32$  entries. With a 10b DDFS output, each entry in the ROM have a length of 9b because the MSB is the sign bit of the output, which can be determined by the MSB of the phase bits. Each ROM has a size of  $2^5 \times 9 = 288$  bits, and a total of 576 bits are used for the coarse ROM in the DDFS design, which leads to a compression ratio 142:1.

The pre-determined interpolation coefficients  $\alpha$  and  $\beta$  need to be multiplied by  $(\theta - \theta_i)$  to obtain the fine correction to the sine and cosine values generated by the coarse ROM's. The complex multiplier and the ROM required are replaced by hardwired shift-and-add based constant multiplier to reduce the circuit complexity and operating frequency. Since only the first two terms in (4.2) are implemented to approximate the sine and cosine values, the Taylor series linear interpolation error  $\delta_{sin}$  and  $\delta_{cos}$  are introduced. These two values are closely approximated by the third term in (4.2)

$$\delta_{cos} \approx -(\theta - \theta_i)^2 \frac{\cos(\theta_i)}{2} \quad (4.3)$$

Since the maximum values of  $\sin(\theta_i)$  and  $\cos(\theta_i)$  are 1, the terms  $\delta_{sin}$  and  $\delta_{cos}$  have the following upper limit:

$$\begin{aligned} |\delta_{sin \max}| &= \frac{(\theta - \theta_i)^2}{2} \\ |\delta_{cos \max}| &= \frac{(\theta - \theta_i)^2}{2} \end{aligned} \quad (4.4)$$

The maximum value of  $(\theta - \theta_i)$  is equal to the difference between two of the consecutive phase addresses used for the coarse ROMs. With  $m=5$  bits, the interpolation error for phases between 0 to  $\pi/4$  is  $(\theta - \theta_i) = \pi/4/2^5 = 0.02454$ . Then  $|\delta_{sinmax}| = |\delta_{cosmax}| = 3.012 \times 10^{-4}$ , which translates to an achievable SFDR of 70.4 dBc theoretically.

### **DDFS Core Unit Architecture**

The DDFS core unit architecture that is shown in Figure 4.4. The input to the DDFS is a 14-bits frequency control word, which goes into the 14-bit phase accumulator. 13 bits of the phase accumulator are used for the phase-to-amplitude conversion. The 3 MSB of the phase accumulator output are feed into a control logic, which is used to generate the full sine and cosine function from the ROM's that only store 0 to  $\pi/4$  of the sine and cosine values. The middle  $m=5$  bits are used to address the coarse ROM, and the  $n=5$  LSB are used to generate the fine correction values. The outputs of the adder/subtractor go through the second one's complement logic block, and the MSB of the output of the phase accumulator are added in the beginning to generate the final DDFS sine and cosine output.



the input samples of the last adders/subtractors arrive at the same clock cycle. Extra pipeline registers are added within the control logic to ensure that the logic signals are synchronized with the data signals. The drawbacks of adding pipeline registers are the area/power consumed by the pipeline registers and the additional signal delays in the system [25].

The 3 MSB of the phase bits determines which quadrant the phase is located in, and the control logic block takes the 3 MSB and distributes control signals to all the blocks in the system. The 1<sup>st</sup> MSB is used to control the one's complement block at the sine output, and the 1<sup>st</sup> MSB XOR 2<sup>nd</sup> MSB is used to control the one's complement block at the cosine output. The 3<sup>rd</sup> MSB is used to control the one's complement block after the phase accumulator, then it is XOR with 2<sup>nd</sup> MSB to control the outputs of the MUX's after the ROM's. Table 3.1 summarizes the output signals generated by the control logic block. These control signals provide this DDFS architecture to generate the full sine and cosine quadrature waveforms with only storing phase address of 0 to  $\pi/4$  in the ROM's.

Table 4.2. Summary of DDFS control signals

3 MSB	0	0	0	0	1	1	1	1
one's	0	1	0	1	0	1	0	1
one's	0	0	0	0	1	1	1	1
one's	0	0	1	1	1	1	0	0
MUX 1	0	1	1	0	0	1	1	0
MUX 2	0	1	1	0	0	1	1	0
sine add/sub	0	1	1	0	0	1	1	0
cosine	1	0	0	1	1	0	0	1

The phase accumulator in the proposed DDFS is a 14-bit phase accumulator with no pipeline stages added. This phase accumulator is the circuit with the longest signal path in this architecture, and it should be optimized in logic synthesis and place and route to meet the timing requirements of the overall system.

The sine and cosine functions from phase 0 to  $\pi/4$  are broken into 32 intervals and stored in one physical ROM. These 32 sine and cosine values are analyzed in MATLAB and converted into binary representations for Verilog RTL coding. The coarse ROM has a total of 32 entries with 5-bit access address, and each entry is a 9-bit data. The total size of the DDFS ROM is 576 bits.

## DDFS with I/Q Output Control

The I/Q unit is a block that can change the gain, DC offset, and phase output of the DAC control core unit, and this is added between the DDFS core unit and the DAC. I/Q unit block can adjust the magnitude and the scaling of the waveform, and it can be used to fix the LO leakage in the RF transceiver [11],[4]. In addition, the I/Q unit can add a phase offset to compensate the I/Q mismatch effects of the transceiver. Figure 4.5 shows the block diagram of the I/Q unit. It consists of two adders and two real multipliers for both quadrature real and imaginary branch, and one complex multiplier for the imaginary signal branch. Pipelines stages are added between each operation to accommodate the required timing constraints.

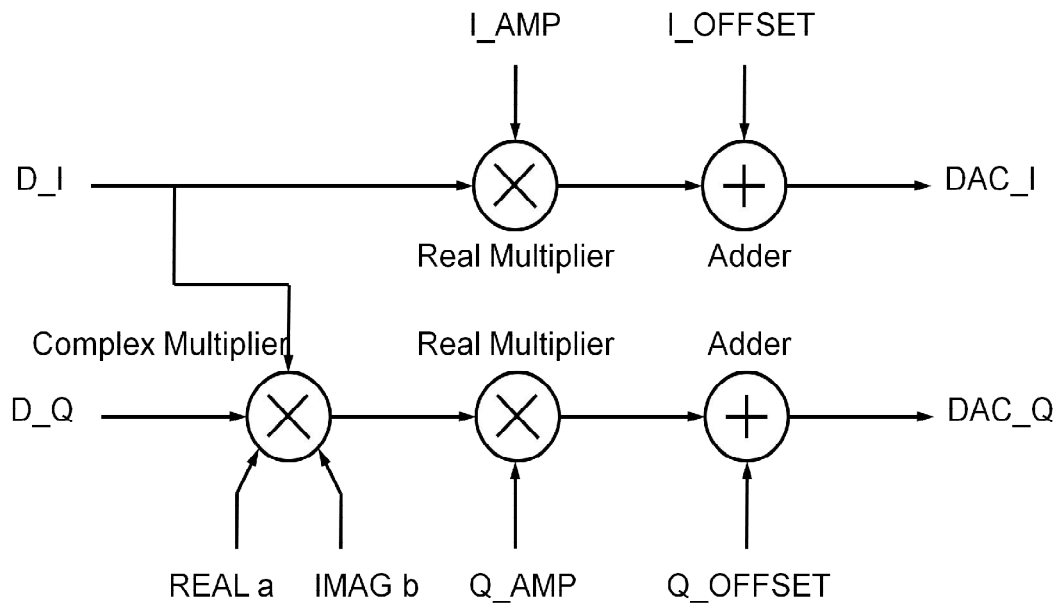


Figure 4.5. Block diagram of the I/Q unit



$D_I$  and  $D_Q$  are the quadrature cosine and sine outputs from the DAC control core unit. The signal  $D_Q$  (sine output) then goes through a complex multiplier that rotates the phase of the  $D_Q$  waveform by a specified degrees, which is controlled by the variables  $a$  and  $b$ . The phase rotated output  $D_{Q_{rotated}}$  value can be calculated with the following equation:

$$D_{Q_{rotated}} = D_Q \times a + D_I \times b \quad (4.5)$$

Where the  $D_{Q_{rotated}}$  is the output of the complex multiplier. Assuming that the signal  $D_Q$  is rotated by a phase  $\theta$ , the inputs  $a$  and  $b$  is determined by  $a = \cos(\theta)$  and  $b = \sin(\theta)$ . The values of  $a$  and  $b$  can be calculated on the PC side and assigned through the USART interface and stored in the on-chip control registers.

Even with interpolation optimization techniques to reduce the ROM size and pipelining to reduce the computation critical path, it's still not enough to meet the timing constraints of 2.0 GHz clock frequency. Parallel interleaving technique is applied to increase the processing throughput of the DDFS to 2.0 GHz by multiplexing 4 paths of sub-DDFS each operating at 500 MHz [25]. The block diagram of the 4-parallel time interleaved DDFS is shown in Fig. 4.6. For a frequency control word of  $\Delta f$ , a shift operation is applied to generate  $4 * \Delta f$  signal, which is then feed to the inputs of four identical DDFS core units that are each clocked by 500 MHz. Each sub-DDFS unit has a different starting phase in the phase accumulator. The I/Q unit following the DDFS core are also 4-parallel interleaved and each clocked at 500MHz. The outputs signals of these four I/Q units are finally feed into a high speed multiplexer clocked at 2 GHz. The 2 GHz

digital output of this multiplexer (MUX) then drives the DAC that converts the digital waveforms into analog ones.

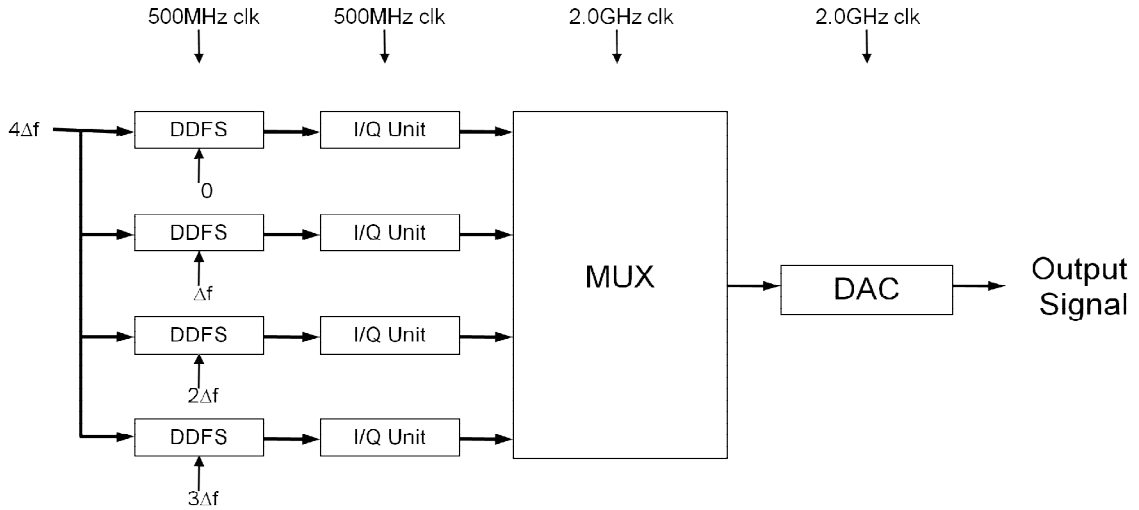


Figure 4.6. Block diagram of the 2.0 GHz DDFS with I/Q output control

The system is provided with a 2.0 GHz master clock from external signal generator instrument, and a divided-by-4 clock divider is required to generate the 500MHz clock for the DDFS core units and the sub-I/Q units. The divide-by-4 clock divider is implemented by a 2-bit synchronous counter. Fig. 4.7 shows the circuit schematic of the clock divider. In Fig.4.7, CLK\_DIV\_4 and CLK\_DIV\_2 are respectively the divided by 2 and divided by 4 clock signals.

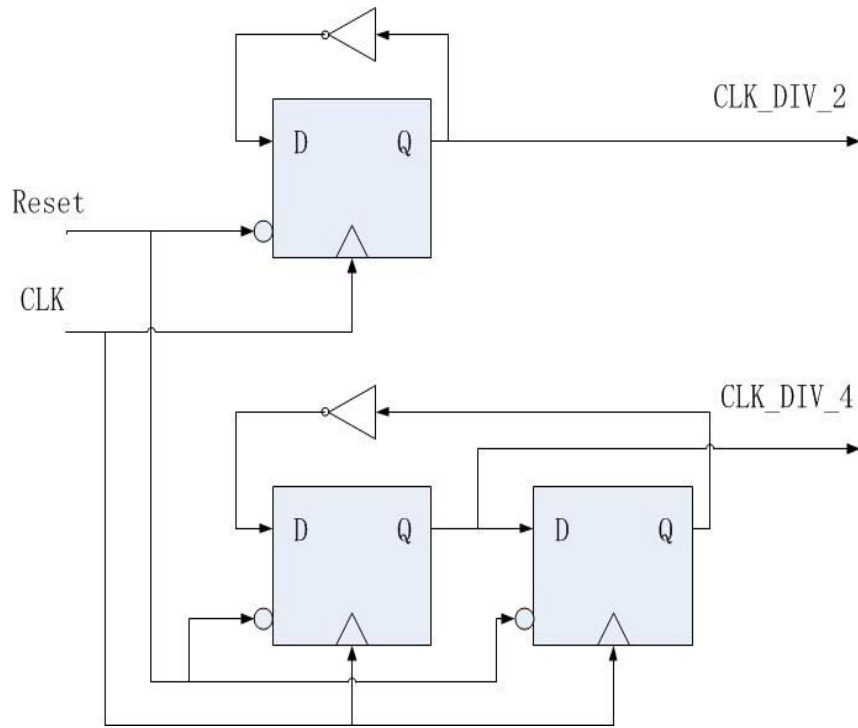


Fig. 4.7. Schematic of the clock divider

At every clock cycle of the 500MHz clock, the four interleaved sub-DDFS cores generate four outputs from four consecutive phases. Then the MUX takes in these four samples and outputs them one at a time at frequency of 2.0 GHz. So even though the DDS unit core is only running at a lower clock frequency of 500MHz, the DAC control unit can operate at 2 GHz and generate signals up to 1 GHz with this time interleaved technique. The disadvantage of applying the time interleaved parallel technique is that four different DDS core units are needed to achieve the speed of 2 GHz. Now with this technique applied, four ROMs are needed to implement the proposed architecture and the total ROM size has now increased to 2,304 bits.

## **Design Verification and Implementation Results of DAC Controller**

Matlab was first applied for the high level modeling and evaluation of the DDFS interpolation algorithm and architecture. It models the exact bit true and cycle accurate behavior of the DDFS core unit. SFDR performance simulations in Matlab were performed to ensure that this architecture indeed generates quadrature sine and cosine waveforms meeting the self-healing requirements. After Matlab high level modeling, Verilog RTL codes were written to implement the DAC controller discussed in the previous section. At the RTL implementation top level, the DDFS is separated into four blocks: DDFS core unit, IQ unit, MUX, and the clock divider. Different combinations of inputs are included in the Verilog test bench code to ensure the DAC controller functions.

After Verilog RTL implementation, the DDFS core units, IQ unit, MUX, and clock divider were synthesized. Cadence Encounter RTL Compiler was applied to synthesize and generate the gate level netlist while applying TSMC's 65nm CMOS standard cell library. For 2.0 GHz high frequency designs like the clock divider and MUX, low  $V_T$  threshold voltage technology library was applied. For the 500 MHz sub-DDFS and IQ units, standard  $V_T$  threshold voltage standard cells were applied to save power. After the synthesized netlists were generated, these netlists files were used to perform gate level simulation of the design. The results from the gate level simulations were compared with the results from the Matlab to verify that the synthesized gatelevel netlist matches with the initial high level Matlab design.

The place and route (P&R) process was performed in the Cadence SoC Encounter after synthesis. In the P&R layout process, power and ground metal wires were applied with layer 5 and above to reduce the resistance and IR drops. Fig. 4.8. shows the finished P&R layout for the DAC control unit in the Cadence SoC Encounter. After P&R, a final gds layout is generated for top level integration of the self-healing transceiver.

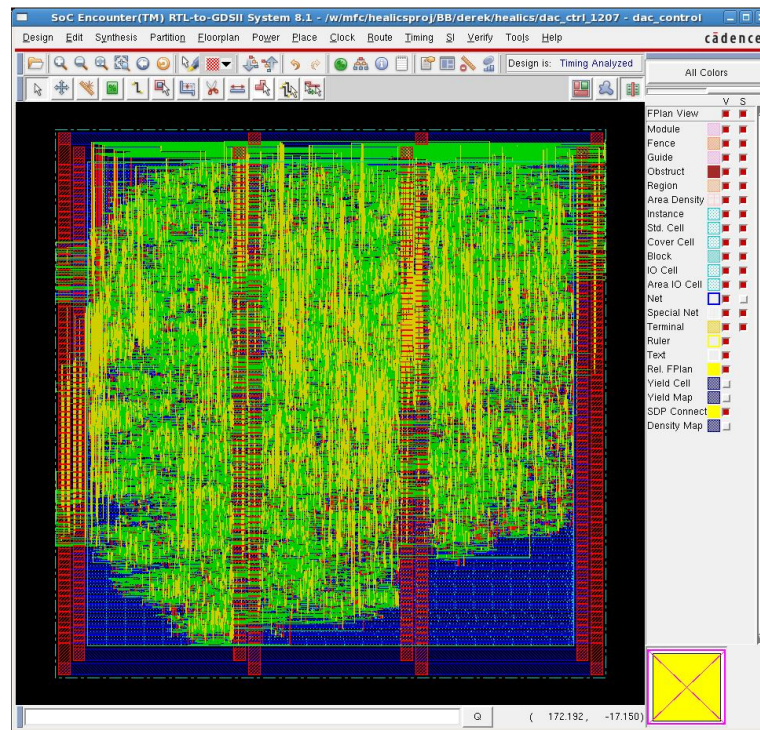


Fig. 4.8. DAC control unit layout in Cadence SoC Encounter

The generated gds layouts from Cadence SOC encounter were then imported into the Cadence Design System for physical verifications and post-layout simulations. DRC (design rule checking) was first conducted on the layout then LVS (layout vs. schematic) was performed to check if the generated layout matches with the system described by the Verilog code. To conduct transistor level post-layout simulation, resistance and capacitance (RC) extraction of the DAC control unit was performed. The schematics of each layout can then be created to run accurate post-layout simulation with other mixed-signal or analog circuits in the self-healing transceiver. Figure 4.9 shows the layout of the DAC controller integrated in the self-healing transceiver. The DAC control unit occupies an area of 363  $\mu\text{m}$  by 393  $\mu\text{m}$ . The layout is placed on the right side of the transceiver, and the outputs of the DAC control drive the two multiplexers left of the DDFS. The high speed clock divider is placed in between the multiplexers to minimize the clock skew.

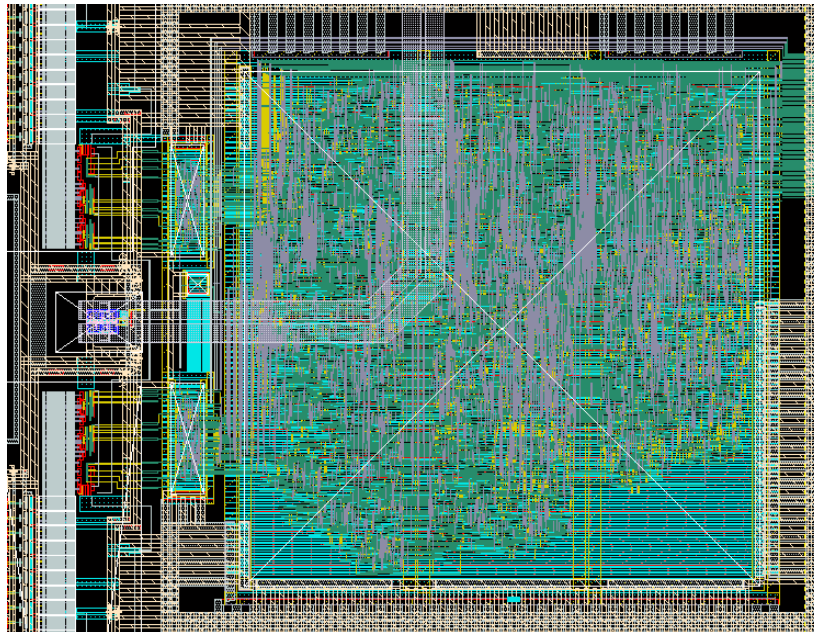


Fig.4.9. Layout of DDFS with I/Q output control

RC extracted post-layout simulations were further performed to ensure that the mixed signal microsystem DAC control and the DAC would function at 2.0 GHz clock frequency. In postlayout simulation, loading capacitors were added at the output of the DAC control to accurately model the loading capacitance from the DAC and inductors were added to simulate the bondwire effects. A large number of transient simulations under different process corners were performed to verify the functionality of the DAC control and DAC combined system. The following figures show some of the postsimulation outputs generated by the DAC control.

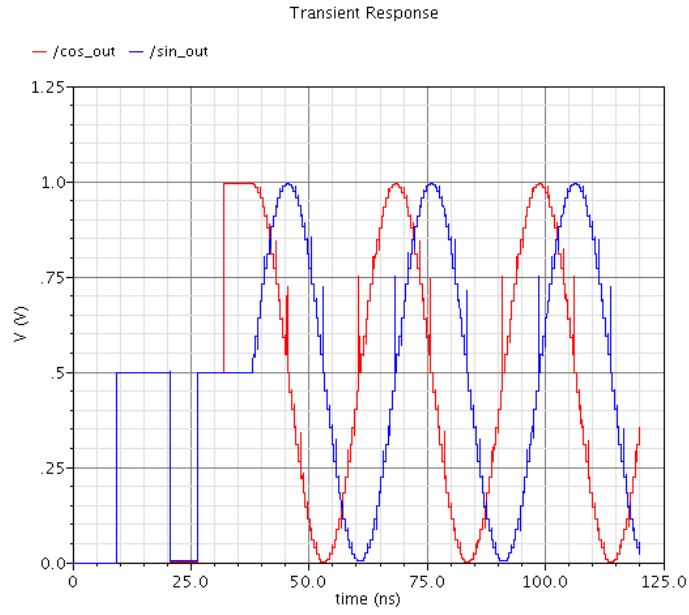


Fig. 4.10. DAC control with single-tone output

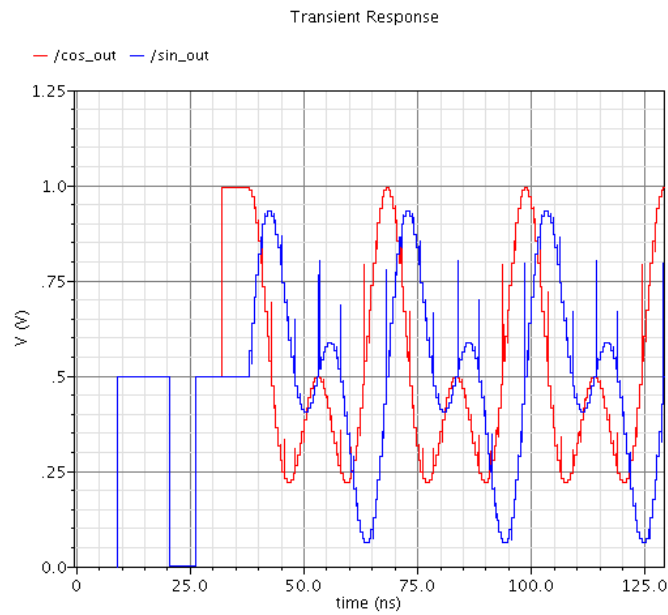


Fig. 4.11. DAC control with two-tone output



Fig. 4.12 shows the SFDR performance of the DAC control at single tone mode when applied with 10b an ideal DAC. FFT processing was applied to calculate the spurs and the SFDR of the DAC control at single tone mode was measured to be 58.41dB.

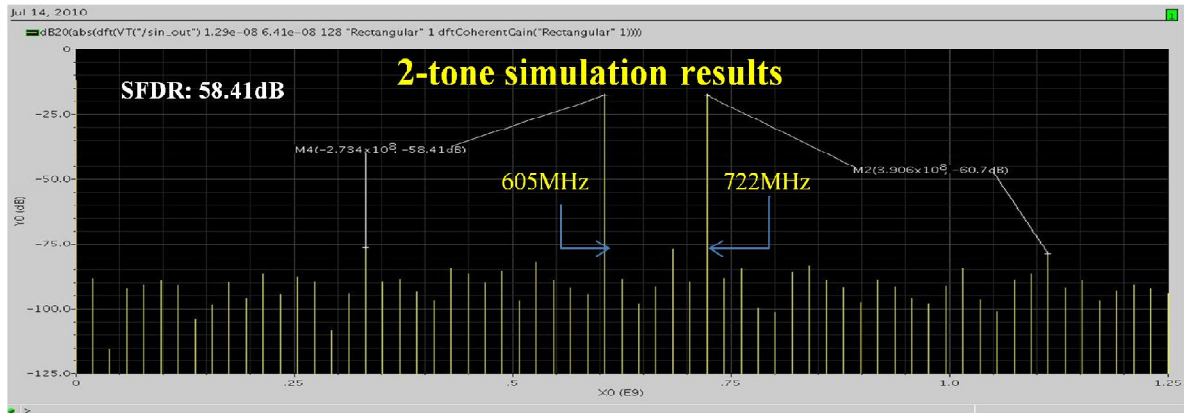


Fig. 4.12. SFDR simulation of the DAC control unit

Table 4.3 shows the performance summary of the 2.0 GHz time interleaved DAC control unit. This DAC control unit is both a two-tone DDFS with IQ output control designed for self healing and a BPSK, QPSK, and 16 QAM modulator designed for transceiver loop-back test. The DDFS has 14b frequency control, when closed at 2.0 GHz the frequency tuning resolution is 122KHz and the maximum output frequency is 1 GHz. The IQ unit following the DDFS can generate 10b amplitude scaling, 10b DC offset and 10b phase rotation on the DDFS quadrature outputs.

Table 4.3 DAC control unit design summary

	DAC control unit
Technology	TSMC 65 nm CMOS
Quadrature Output	Yes
Output Range	0 ~ 1.0 GHz
Frequency Resolution	122 KHz
Clock Frequency	2.0 GHz
Core $V_{DD}$	1.0 V
Power Consumption	10mW @ 2GHz clock
SFDR	58.41 dB
Area	0.143 mm <sup>2</sup>

## **Performance Comparison and Conclusion of the DAC control unit**

In here, we present the comparison of the proposed DAC control unit with other existing DDFS architectures and provide conclusion to the DAC control design. Most existing DDFS designs focus on fine frequency tuning resolution and high SFDR, but the proposed DDFS design focuses on high operating clock frequency, low area and power consumption, and multi-mode functioning for transceiver calibration purposes. As shown in Table 4.4, the proposed DDFS for the DAC control achieves the highest clock frequency at smallest area and power consumption.

The DDFS core within the DAC control unit applies modified Taylor series linear interpolation technique to reduce the ROM size while maintaining a SFDR of 58dB to support the 10b 40dB 2.0 GHz DAC in the self-healing transceiver. The total ROM size in the DDFS design is 2,304 bits, which translates to a ROM compression ratio of 36:1 at 2 GHz clock frequency. The high clock frequency operating capability of the DAC control unit is achieved by both careful consideration of the DDFS interpolation algorithm, optimization of the pipelined architecture, replacing the fine interpolation lookup table and general multiplier with hardwired shift-and-add based constant multiplier, and 4-parallel time interleaved architecture.

Table 4.4 Comparison of DAC control unit with other DDFS designs

Design	Process	Max. Freq.	Area	SFDR	Power
[16]	90nm CMOS	1.3 GHz	2.0 mm <sup>2</sup>	52.0 dBc	269 μW/MHz
[19]	350nm CMOS	2.0 GHz	3.99 mm <sup>2</sup>	50 dBc	410 μW/MHz
[20]	350nm CMOS	0.3 GHz	14.44 mm <sup>2</sup>	78.56 dBc	900 μW/MHz
[21]	180nm CMOS	0.5 GHz	0.095 mm <sup>2</sup>	95 dBc	160 μW/MHz
[22]	130nm CMOS	1 GHz	0.010 mm <sup>2</sup>	63.2 dBc	8.2 μW/MHz
The proposed DAC control unit	65nm CMOS	2.0 GHz	0.143 mm <sup>2</sup>	58.41 dBc	5.89 μW/MHz

## 4.2 Parameter Estimator

The bandwidth of the self-healing FFT spectrum analyzer is 10 MHz, which is determined by the 10 MS/s sample rate of the 10b (8.7 ENOB) auxiliary ADC. This block is therefore a low-speed unit, and does not require complex parallel processing or pipelining techniques in order to meet timing requirements. The length of the FFT is chosen to be 128. This allows the resolution of the FFT bins to properly detect the OIM3 harmonics from the transmitter envelope sensor [11].

The FFT's quantization noise performance is designed to have an SQNR of at least 50 dB in order to preserve the SNDR of the auxiliary ADC and prevent signal quantization noise degradation through the digital signal processing datapaths. To further increase the SNR, the FFT spectrum analyzer can perform different number of averages by taking averages of 32, 64, 128, 256, 512, or 1024.

The block diagram of the proposed FFT spectral analyzer microsystem is shown in Fig. 4.13 (a). The FFT unit takes two 10b inputs, each from a separate auxiliary ADC unit. A 128-point FFT is performed through the block shown in Figure 4.13 (b). The FFT processor contains seven butterfly stages, each with a corresponding shift register, complex multiplier, and a ROM lookup table. Figure 4.13 (c) shows the FFT averaging operation, where each de-multiplex block is connected to a controller. There are a total of 128 registers for storing the 128 FFT bin. Each of the registers is multiplexed to an accumulator for summation of the number of averages. The actual division operation of the averaging is accomplished by shifting operation since the number of averaging is fixed to a

power of 2 within 1024. From the averaged outputs, the estimated spectrum is calculated and then readout through the USART interface [31].

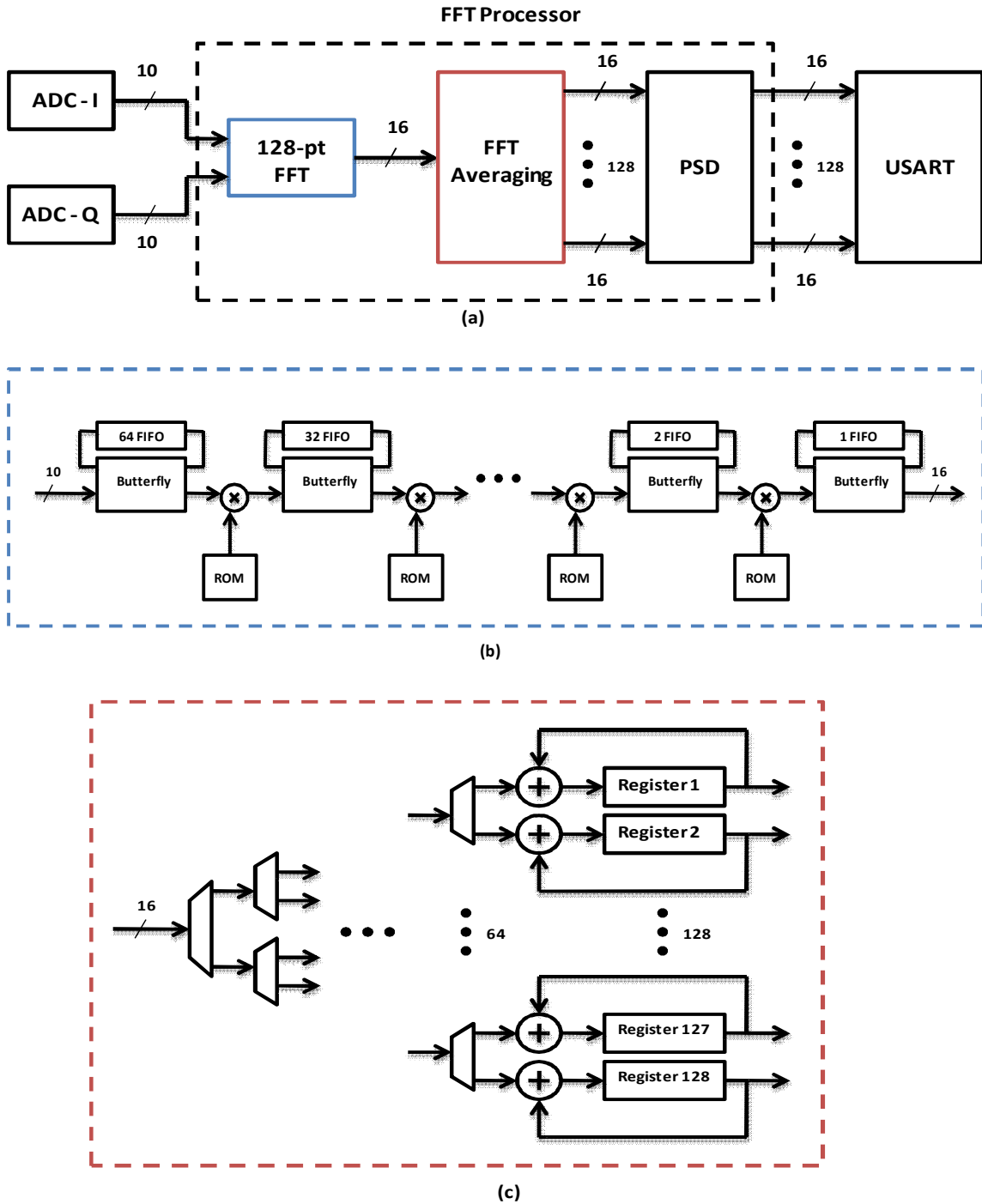


Fig. 4.13. (a) Parameter estimator (b) 128pt FFT processor (c) FFT Averaging

One desired feature for the self-healing mode FFT is flexibility, since its specification is one of the last circuits to be finalized within the self-healing transceiver design process. To support different noise parameter requirements, the FFT architecture was selected to be as flexible as possible. Therefore, a radix-2 FFT algorithm was chosen, so that the parameter estimator can be easily adjusted to any FFT lengths. Radix-2 FFT has a relatively simple architecture and it can be applied for signal demodulation for the baseband modem [32]. Although high speed throughput is not a requirement for this FFT processor, the pipeline architecture is still applied. It is chosen because beside self-healing purposes it can also be applied for OFDM/Single-Carrier modem demodulation. By using a pipeline design for the 10MS/s FFT, the same hardware can be applied for the high-speed equalization FFT as long as multi-mode clocking support for the FFT processor is provided.

This dissertation focuses on the radix-2 decimation in frequency (DIF) FFT algorithm. This algorithm is easy to implement in hardware due to its simplicity, and regularity. In radix-2 FFT algorithms, the N-point DFT is continuously divide and conquered into N/2 DFTs. For radix-2 algorithms, we have the following relation from the symmetry of the twiddle factor  $W_N^{nk}$ .

$$W_N^{nk} = -W_N^{nk + \frac{N}{2}} \quad (4.6)$$

where  $W_N^{nk} = e^{-j2\pi\frac{nk}{N}}$ . To implement the radix-2 DIF FFT algorithm, equation (4.6) can be used to apply the twiddle factor symmetry to obtain equation as follows

$$\begin{aligned}
X_k &= \sum_{n=0}^{N/2-1} x(n)W_N^{nk} + \sum_{n=N/2}^{N-1} x(n)W_N^{nk} \\
X_k &= \sum_{n=0}^{N/2-1} [x(n) + x(n + N/2)e^{-j\pi k}]W_N^{nk} \\
X_k &= \sum_{n=0}^{N/2-1} [x(n) + x(n + N/2)(-1)^k]W_N^{nk} \tag{4.7}
\end{aligned}$$

(4.7) is then split into even and odd parts and by using a change of variables, we let  $k=2r$  for the even frequency samples, and  $k=2r+1$  for the odd frequency samples. And analyzing the even frequency samples, we have

$$X(2r) = \sum_{n=0}^{N/2-1} [x(n) + x(n + N/2)]W_N^{2rn} \tag{4.8}$$

Putting into the DFT form, this equation can be rewritten as

$$X(2r) = \sum_{n=0}^{N/2-1} [x(n) + x(n + N/2)]W_{N/2}^{2rn}, \quad r = 0, \dots, \frac{N}{2} - 1 \tag{4.9}$$

From (4.9), the  $N/2$ -point DFT can be obtained from the  $N$ -point DFT. These constitute the even portion of the  $N$ -point DFT. To calculate the other half, the odd frequency samples are analyzed.

$$X(2r+1) = \sum_{n=0}^{N/2-1} [x(n) - x(n + N/2)]W_N^n W_{N/2}^{rn}, \quad r = 0, \dots, \frac{N}{2} - 1 \tag{4.10}$$

(4.10) provides the second half of the  $N/2$ -point DFT. Therefore, this decomposition can be repeated until the complete FFT algorithm is completed. This decomposition operation is known as a butterfly operation. For a 128pt FFT processor, in single path feedback delay pipeline architecture, there are a total of seven radix-2 butterfly stages [31].



From equations (4.9) and (4.10), it can be seen that each butterfly operation requires two complex additions/subtractions and one complex multiplier. For two complex numbers  $x = x_{re} + jx_{im}$  and  $W = W_{re} + jW_{im}$  here  $x$  is the input and  $W$  is the twiddle factor. When complex addition is performed the following is obtained,

$$x + W = (x_{re} + W_{re}) + j(x_{im} + W_{im}) \quad (4.11)$$

One complex addition consists of two real additions. Now if complex multiplication is performed, the following is obtained:

$$x \times W = (x_{re}W_{re} - x_{im}W_{im}) + j(x_{im}W_{re} + x_{re}W_{im}) \quad (4.12)$$

One complex multiplication is expanded into three real additions and four real multiplications. However, this operation can be simplified by exploiting the fact that the twiddle factor is a constant. Rewriting (4.12), we obtain the following

$$x \times W = [(x_{re} + x_{im})W_{re} - (W_{re} + W_{im})x_{im}] + j[(x_{re} + x_{im})W_{re} - (W_{re} - W_{im})x_{re}] \quad (4.13)$$

Since the twiddle factor  $W$  is a constant, then  $W_{re} + W_{im}$  and  $W_{re} - W_{im}$  can be pre-computed, and its results written in a ROM lookup table. Therefore, one complex multiplication can be reduced into three real multiplications and five real additions. Since multiplications are more computationally expensive than additions, the area is reduced by applying three multipliers and five adders over four multipliers and three adders.

Due to finite bit representation in digital arithmetic, the quantization effects can degrade the SQNR. The word length applied in the DSP circuits, play a large

role in the tradeoff between precision and area. The word length of a butterfly stage determines the number of bits used to store the numerical values for that stage. Applying a larger word length not only consumes more area and but also affects the maximum throughput of the system.

The word length for each butterfly stage is chosen such that the SQNR still meets the 50 dB SQNR specification, while still meeting the 10 MHz sampling rate requirements so it won't saturate the signal performance of the auxiliary ADC. Care on the quantization and wordlength truncation must be taken such that overflow or underflow effects does not occur. The first stage of the FFT processor begins with a 10 bit input with word length. Since each successive butterfly operation performs additions. This 128-point FFT contains seven stages. After the final stage, the output is 16 bits.

The twiddle factor  $W_N^{nk} = e^{-j2\pi\frac{nk}{N}}$  applied in FFT processing is a constant, where the real part is represented by a cosine function, and the imaginary part is represented as a sine function. Once the number of points the FFT is determined, a ROM table can be used to store the pre-computed values of all the necessary twiddle factors. The size of the ROM table can be reduced by exploiting the symmetry between the sine and cosine functions. The sine values on the interval  $[0, \pi]$  is the negative of the sine values on the interval  $[\pi, 2\pi]$ . This symmetry can be reduced even further since there is even function symmetry between the two intervals  $[0, \pi/2]$  and  $[\pi/2, \pi]$ . This similar symmetry argument can be applied to the cosine function. Therefore, the ROM lookup table only needs to contain sine

and cosine values between 0 and  $\pi/2$ . The sine values on the interval  $[0, \pi/4]$  are equal to the cosine values on the interval  $[\pi/4, \pi/2]$ , and vice versa. Therefore, the ROM table only needs to store sine and cosine values between 0 and  $\pi/4$ .

In order to properly detect the OIM3 harmonics or the image spectrum from the transmitter, the resolution bandwidth of the FFT bins must provide a noise floor lower than the harmonics. The SNR can be improved by taking the average over many FFT samples of the same frequency bin.

The averaging operation is designed to average FFT processing for up to 1024 times. For each instance, the 16-bit FFT output is stored in a register with a feedback loop, where the output can be accumulated to up to 1024 times before the average is calculated. Following the averaging process, the absolute value is taken and the result squared to obtain the estimated power spectral density (PSD) or pseudo PSD since the absolute value is calculated instead of the actual square root of the  $I^2 + Q^2$ . To correctly re-order the data from the butterfly operations, the 128 output samples are connected to 128 registers, whose addresses correspond to reverse binary. Fig. 4.14 shows the block diagram for the FFT averaging process and PSD estimation computation.

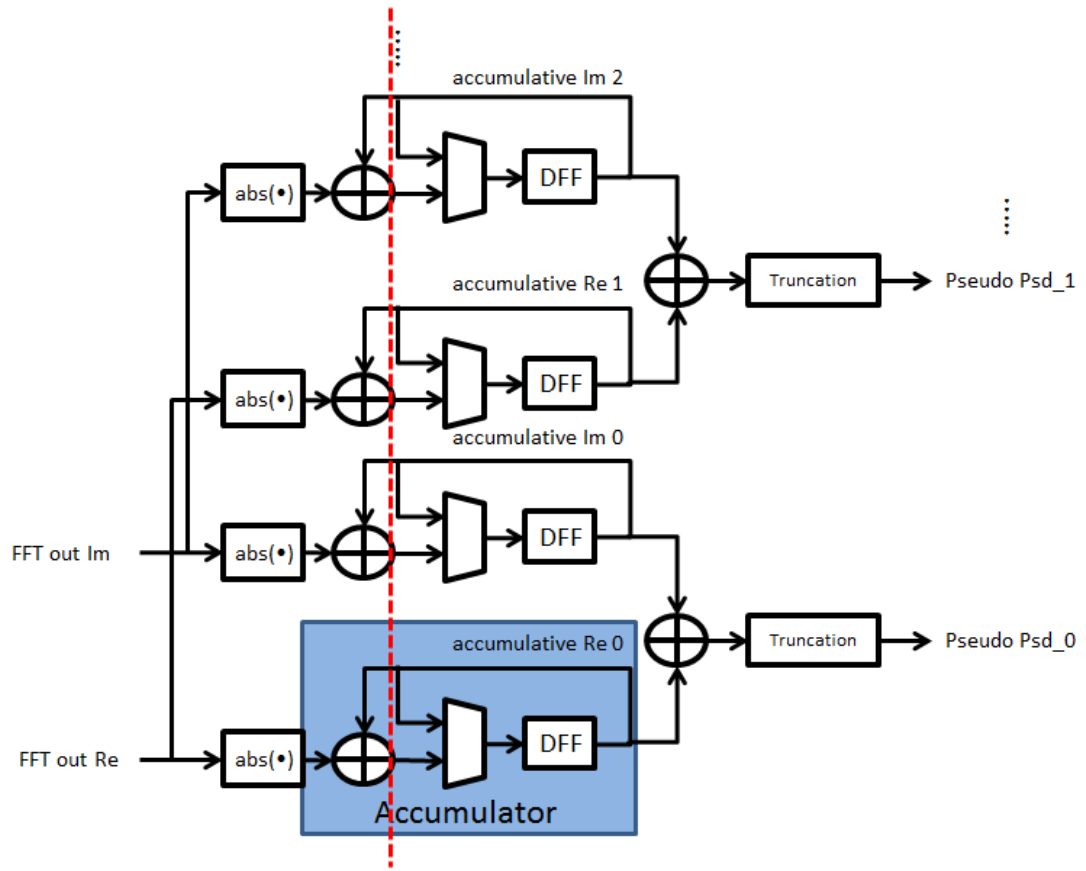


Fig. 4.14. The block diagram of the estimated PSD processing

The self-healing FFT based parameter estimator in the self-healing controller is designed in verilog code and synthesized using Cadence RTL Compiler using TSMC 65nm 6M process. Following synthesis, the parameter estimator is placed and routed using Cadence SOC Encounter. The layout applies 65% core utilization, and a clock tree is inserted in order to minimize clock skew effects.

Including the power rings, this parameter estimator layout occupies an area of  $580 \mu\text{m} \times 963 \mu\text{m}$ . Fig. 4.15 shows the layout of the parameter estimator.

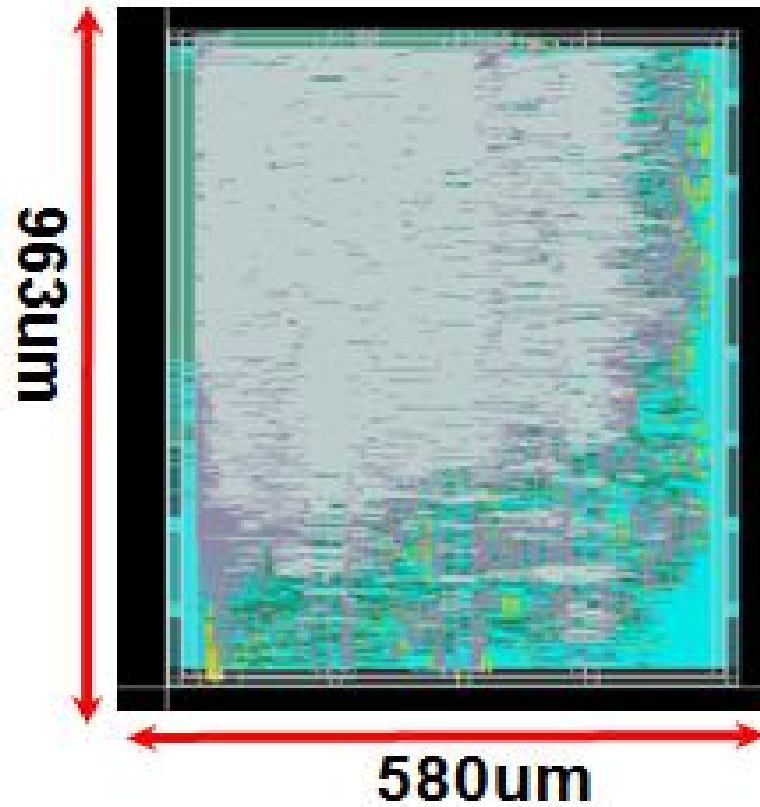


Fig. 4.15 Layout of the parameter estimator

A 128-point FFT processor based parameter estimator clocked at 10MHz is designed to aid in the self-healing operation of a 60GHz transceiver. The FFT processor is designed using radix-2 decimation-in-frequency algorithm and implemented with pipelined single delay feedback architecture. The complex FFT processor has 10b input and 16b output with a SQNR of 60dB. The estimated spectrum is calculated by summing the absolute values of the real and complex

components. Different FFT averages can be applied on the parameter estimator to achieve a higher SNR. This estimated spectrum output is stored in the registers of the USART unit, where data can be readout by a PC to be further analyzed. Table 4.5. presents the summary of the parameter estimator in the self-healing controller.

Table 4.5 Summary of the parameter estimator

	Parameter estimator
Technology	TSMC 65 nm CMOS
Quadrature Output	IQ 128pt FFT
Frequency Resolution	0.78 KHz
Clock Frequency	10 MHz
Core $V_{DD}$	1.0 V
Power Consumption	1mW @ 10 MHz clock
SQNR	50dB
Area	0.558mm <sup>2</sup>

### 4.3 Self-Healing Transceiver Implementation Results

In this section, the 4 Gb/s self-healing transceiver and the self-healing controller implementation results and measurements are presented. The 4 Gb/s self-healing transceiver was implemented with TSMC 65nm general purpose with six metal layer process. The overall transceiver architecture is shown in Fig. 4.16 and a summary of the transceiver features is shown in Table 4.6 [33],[11].

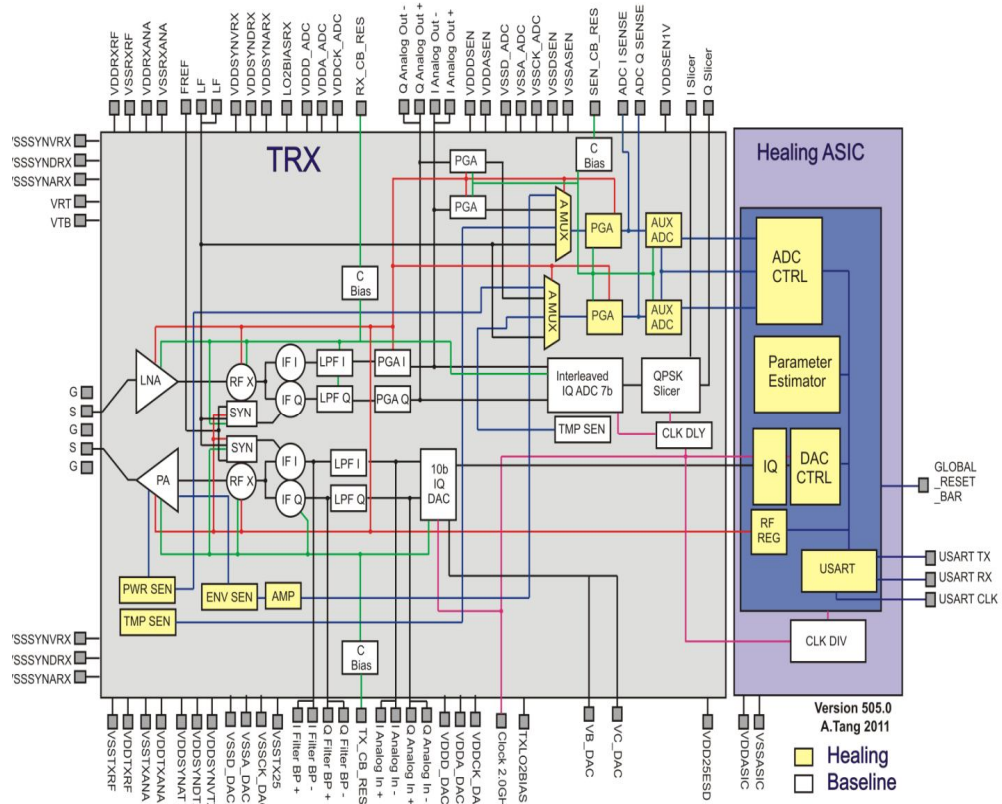


Fig. 4.16. 4 Gb/s 60 GHz Self-Healing transceiver architecture

Table 4.6. Self-Healing transceiver features

Feature	Value
Size	4.0 x 4.0 mm
Pads	145
On-Chip Cap	285 pF
Power Domains	44
RF Control	255
RF Frequency	57-65 GHz
BB Clock	2.0 GHz

The layout and the die photo of the self-healing transceiver are shown respectively at Fig. 4.17 and Fig. 4.18. The self-healing controller and other digital circuits are located at the bottom right hand corner of the chip. There are a total of 3 clock domains supplying the digital circuits of the self-healing transceiver. There is a 2.0 GHz clock supplying the DAC controller and the digital demodulator, a 10 MHz clock supplying the parameter estimator and the auxiliary ADC sampler, and a less than 1 MHz clock for the USART communication. The 10 MHz clock for the parameter estimator is divided down by the 2.0 GHz clock, where the 2.0 GHz clock is supplied from an external low jitter signal generator instrument. The USART clock is provided by the PC and is asynchronous with the clocks applied by the DAC control and parameter estimator, therefore issues such as cross clock domain communications to avoid the loss of data or setup/hold time error issues were carefully implemented during the chip integration process.



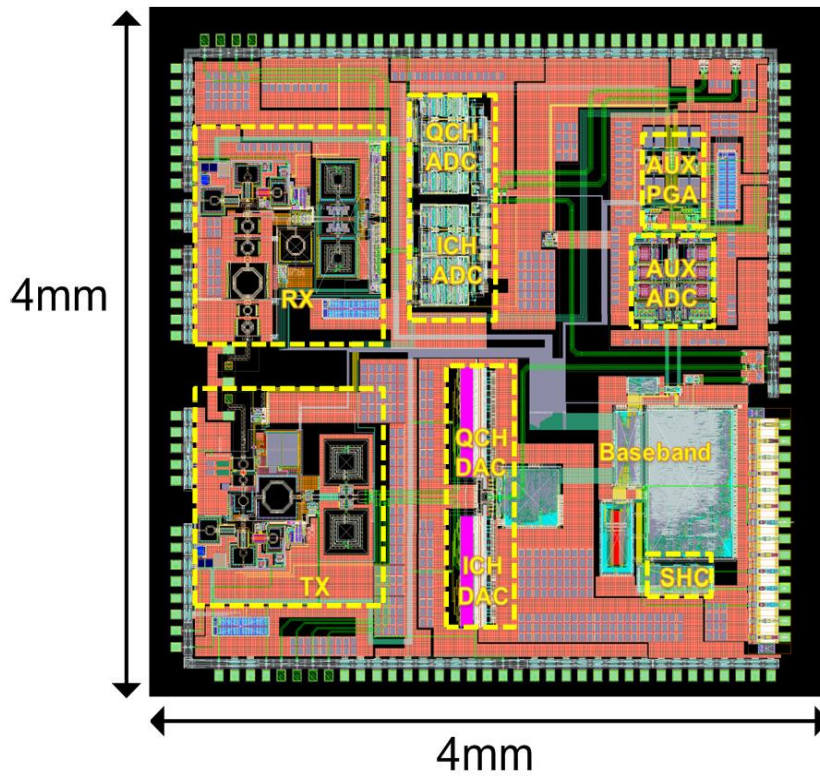


Fig. 4.17. Self-Healing transceiver layout

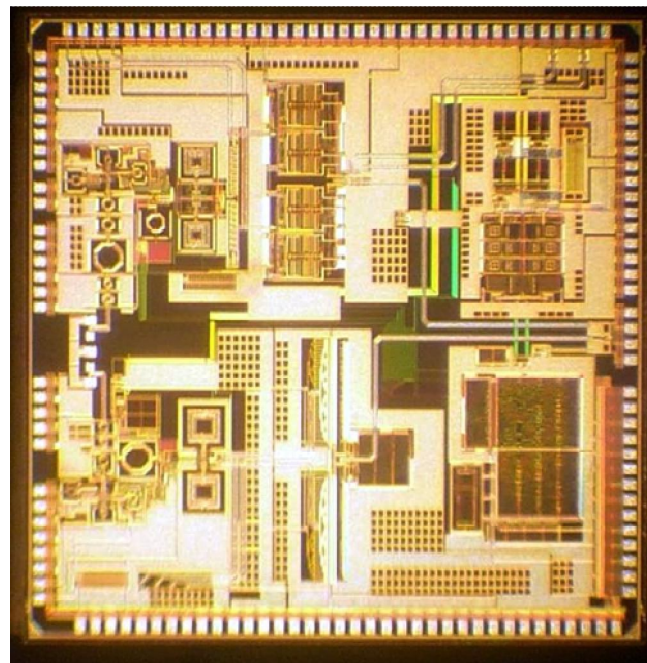


Fig. 4.18. Self-Healing transceiver die photo

Since this self-healing chip spans 4mm-by-4mm, and there were no on-chip automatic clock recovery circuits like delay-lock-loops, buffer based tunable clock phase adjustment circuits were placed on the demodulator side to keep the clock phase of the receiver synchronized with the transmitter.

To prevent circuit performance loss due to ground bounce and IR drop, there were a total of 44 power domains on the transceiver. The DAC control unit shares the ground and supply power plane with the DAC, the demodulator shares its power domain with the ADC, the parameter estimator and USART and other low clock frequency digital circuits occupies a dedicated digital core power domain.

Fig.4.19 and Fig.4.20 show the test setup for the combined DAC control and DAC and the system level testing of the self-healing transceiver. The main control of the transceiver is achieved through the PC and the USART link. The monitoring of the parameter estimator on the self-healing controller and the RF register knob settings are all read and written through the USART. The self-healing algorithms finite state machine can be hardwired on the USART or be written on the firmware on the PC side. In this self-healing transceiver, to make the testing and monitoring more flexible and reduce the risk of hardwiring finite machines to decrease the self-healing algorithm performance, most of the self-healing algorithms are implemented on the PC firmware.

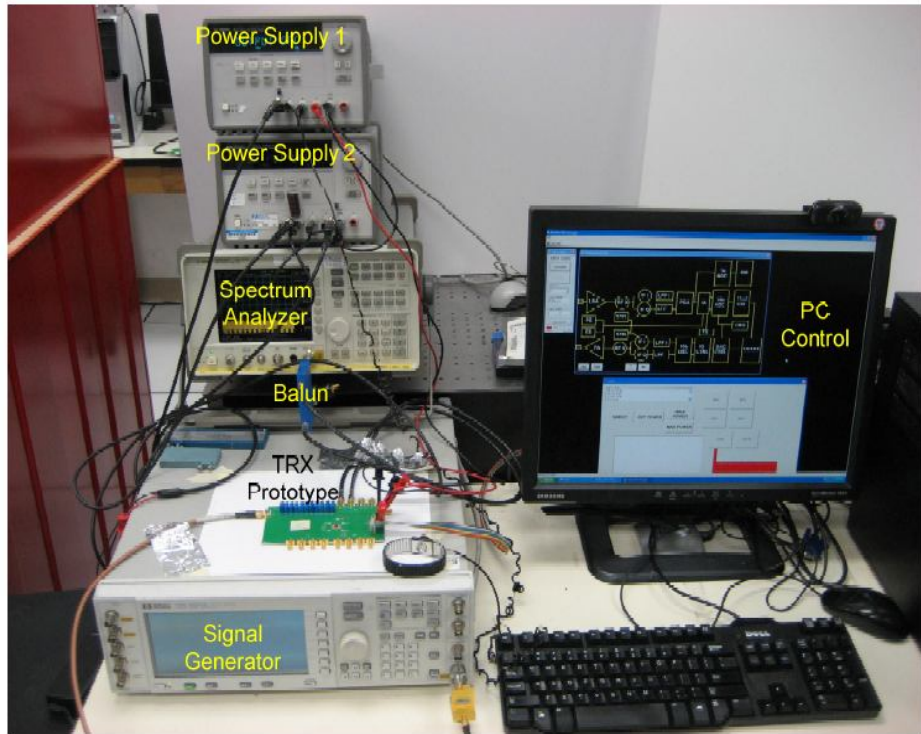


Fig. 4.19. DAC controller unit and DAC test setup

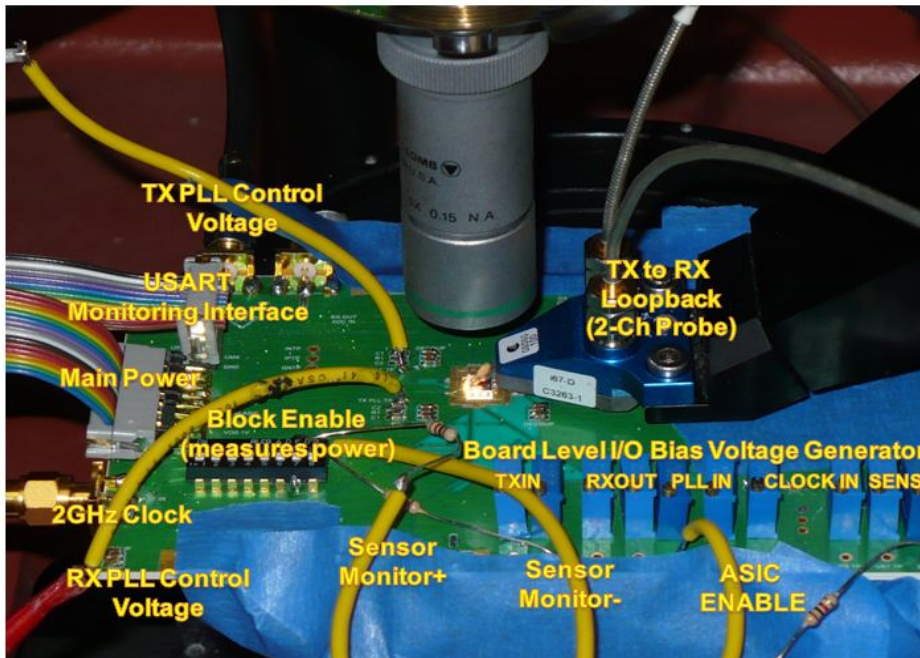


Fig.4.20. Self-Healing Testing probe setup with the PCB board

The performance results of the DAC controller providing test tones to the DAC is shown in Fig. 4.21. It shows that at the Nyquist frequency of 1 GHz, the SFDR performance of the combined DAC control unit and the DAC can achieve 40 dB which is sufficient for the self-healing requirements as well as the signal modulation.

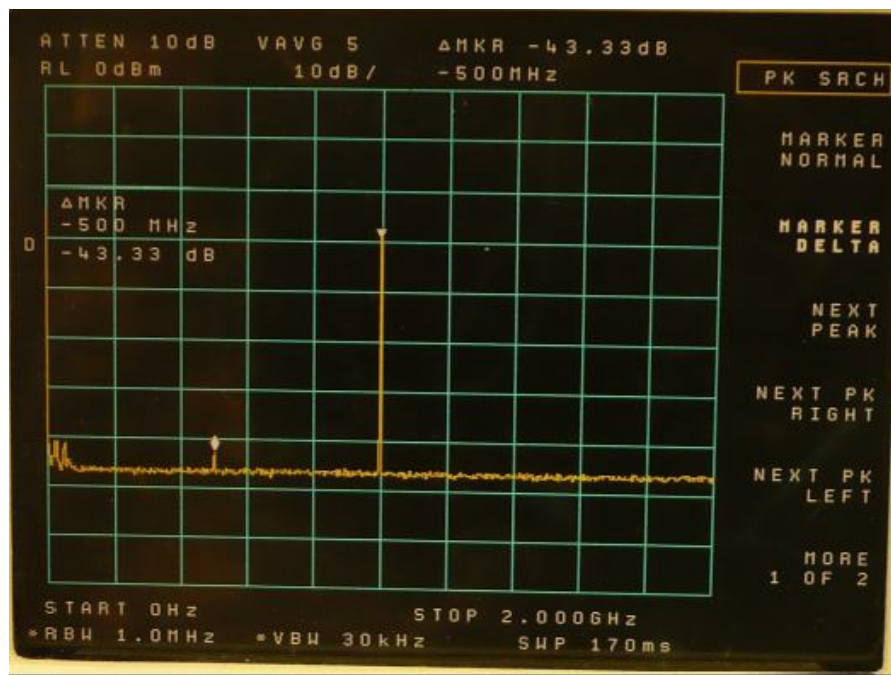


Fig. 4.21 SFDR performance of the DAC control and the DAC, achieving 40dB SFDR at 1 GHz

Fig. 4.22 shows the SFDR performance of the DAC control and the DAC at at low frequency of 60 MHz.

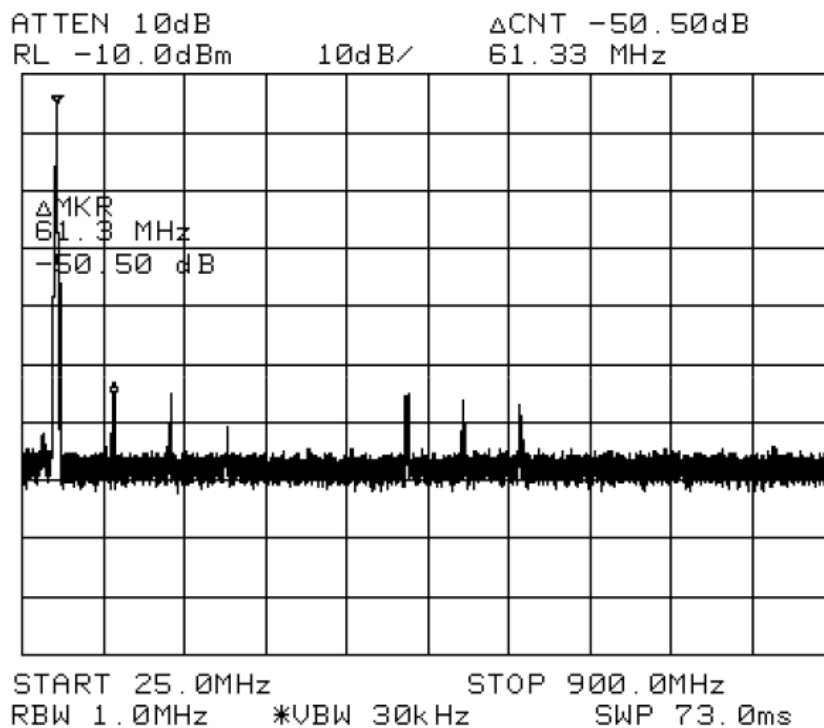


Fig. 4.22 SFDR performance of the DAC control and the DAC, achieving 50dB SFDR at 60 GHz

To perform self-healing algorithm for the IQ mismatch, the IQ unit on the DAC controller is applied to adjust the DC offset, gain control, and phase rotation on the quadrature signal. Fig. 4.23 shows the measured results on the IQ unit functions. From Fig. 4.23, by adjusting the gain, DC offset, and phase rotation through the USART controller, the quadrature DAC control signal outputs can adjusted accordingly.

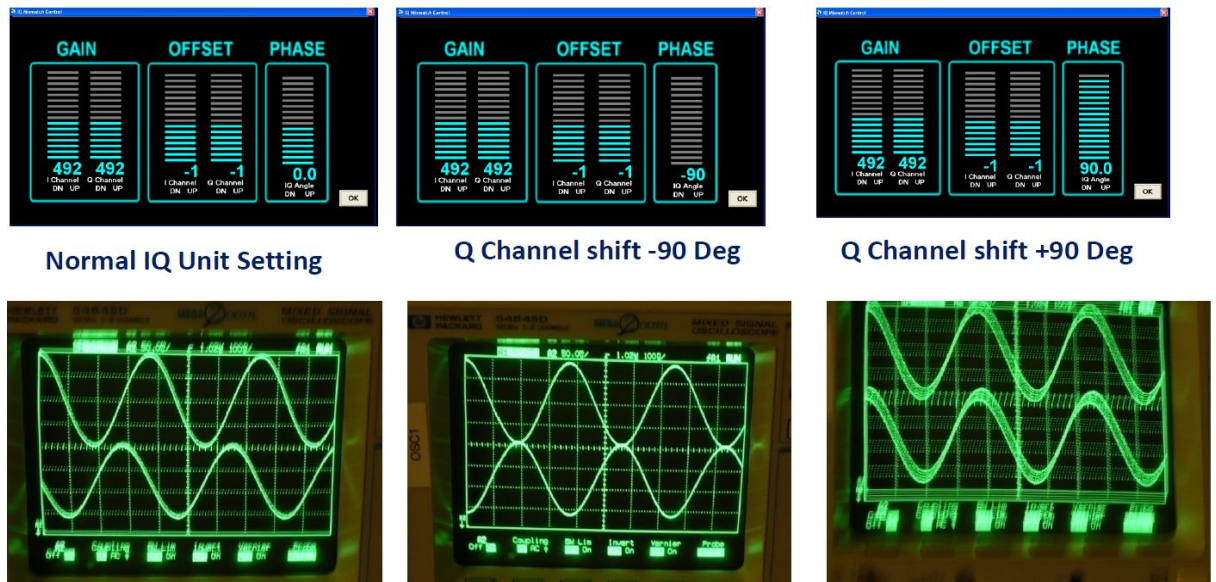


Fig. 4.23. The DAC control output with 0 degree, -90 degree, and 90 degree phase rotation on the Q channel

### 4.3.2 Nonlinearity Self-Healing Results

The healing of the transmitter image OIM3 is as follows, the DAC controller first provides a two-tone signal to the transmitter. The envelope sensor then measure the beat frequencies of the intermodulation tones and the fundamental tones and the spectrum estimation is captured through the FFT processor on the parameter estimaotr. Then three different RF control knobs are applied to adjust the transmitter OIM3, which is the mixer adjustable bias current, bias on the first stage of the power amplifier, and the gain adjustment on the output stage of the amplifier.

Different priorities were chosen on the three different control knobs to search for the most optimal healing configuration. Fig. 4.24 shows the convergence of the OIM3

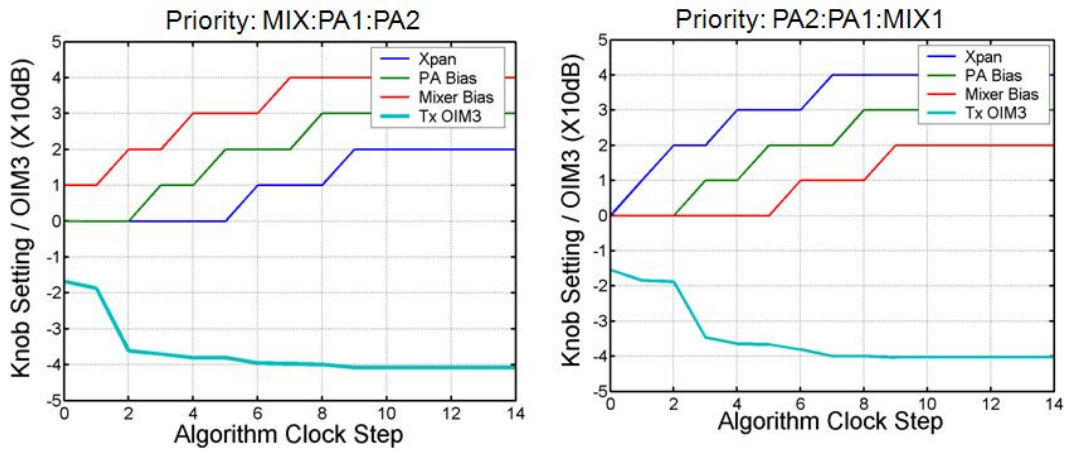


Fig.4.24. Convergence of the OIM3

From the left side of Fig. 4.24, it shows that by placing the priority in the order of mixer, PA bias, and PA expansion bias results the same in image performance as the right side where the priority is PA expansion bias, PA bias, and mixer bias. The priority ordering on the right hand side of Fig. 4.24 is preferred over the left hand side because when PA bias is converged at a lower setting the power consumption is lower. The yield result is shown in Fig. 4.25., this shows the effectiveness of self-healing over ten different chips. Before healing none of the chips satisfy the OIM3 requirements and after healing all ten chips satisfy the OIM3 requirements of less than -40dBc.

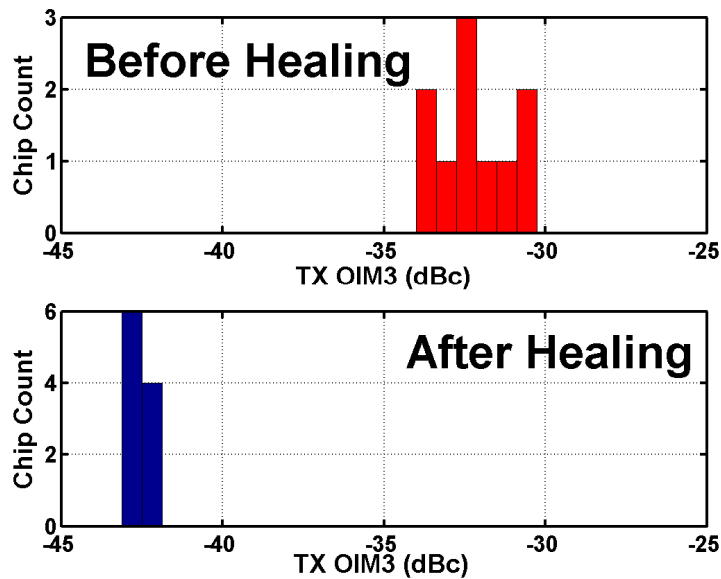


Fig. 4.25. Yield performance after OIM3 self-healing for 10 chips

The self-healing procedure for IQ mismatch is done by first generating a single-tone through the DAC control unit to the transmitter. Then the envelope sensor generates the fundamental frequency and the undesirable LO leakage tone and the image tone. The cause for LO leakage tone is due to the DC offset between the I and Q signal paths. To heal the for the IQ mismatch is to adjust the gain, offset, and phase rotation control knobs on the DAC unit until the image tone is suppressed. The FFT parameter estimator will monitor the spectrum on the output of the envelope detector. The priority for tuning to heal for IQ mismatch is to first do a sweep on the amplitude control to find the code with the lowest image. Then fix the amplitude control code and sweep over different phase to find the phase adjust that will result in the lowest image. Fig. 4.26 shows the spectrum for IQ mismatch healing when a single-tone is applied through the DAC control unit.





Fig. 4.26. The transmitter output spectrum of a single-tone test, this shows the carrier signal, the image tone, and the LO leakage tone.

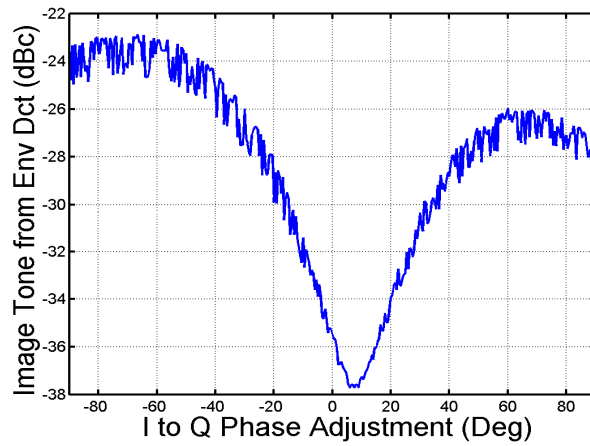
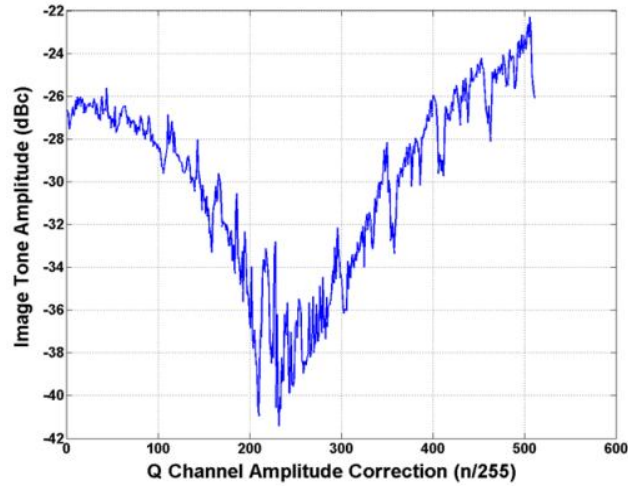


Fig. 4.27. Code sweep on the amplitude and phase for IQ mismatch self-healing

Fig. 4.28 shows the results after IQ mismatch before and after self-healing is applied. It achieves an image rejection of -40 dBc required by the targetted system specifications. Yield results are shown in Fig. 4.29, it shows when self-healing is applied the 10 different chips all have their image tones suppressed.

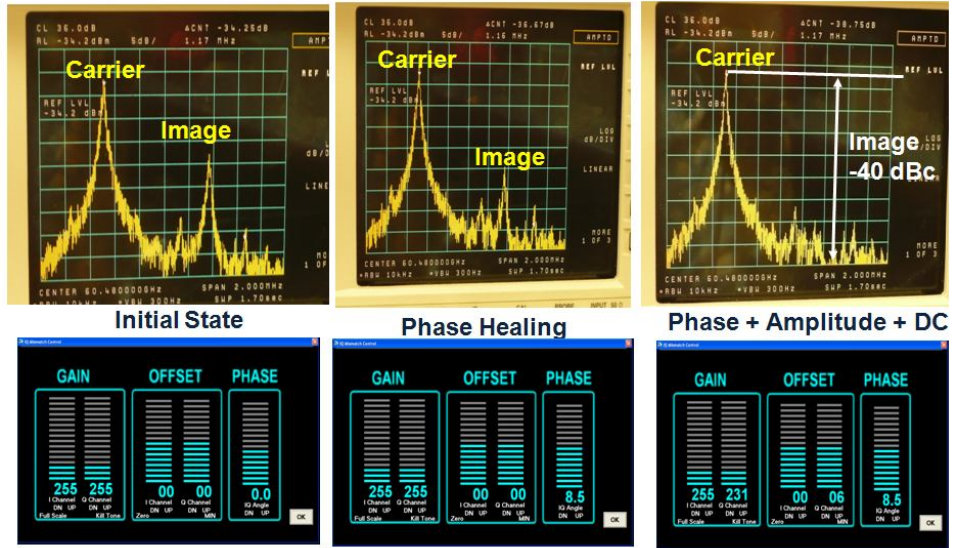


Fig.4.28. The transmitter spectrum output before and after IQ and image healing

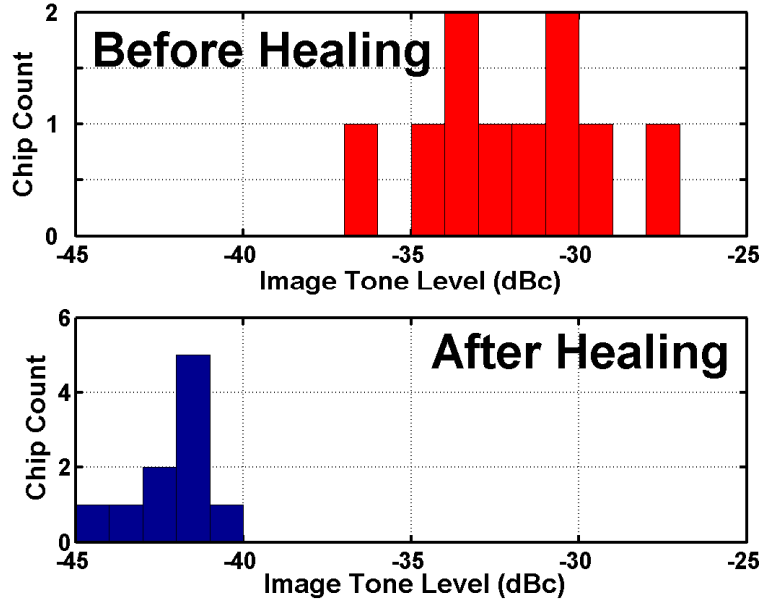


Fig. 4.29. Yield performance before and after IQ self-healing

On the receiver side, the noise figure of the receiver is healed. The noise figure of the receiver must be first estimated before noise figure healing is performed. The temperature sensor near the receiver first measure the temperature and the noise floor and  $kT$  can be computed. The bandwidth of the receiver is determined by the passive receiver filter so the bandwidth is pretty stable across different environmental corners and the noise power  $kTB$  can then be obtained. To obtain the output noise of the receiver, the spectrum of the receiver is first obtained and the FFT is computed. By integrating over the FFT bandwidth, the output noise power information is gathered. To measure the gain of the receiver, a tone can be injected by the DAC control unit through the transmitter to the receiver, then the gain of the receiver can be obtained. The noise figure  $NF = No/(A_{RX}Ni)$  where  $No$  is the output noise power,  $A_{RX}$  is the receiver gain, and  $Ni$  is the input noise  $KTB$ .

Once the noise figure (NF) is measured, the control knobs on the receiver can be tuned to heal for the noise figure. The contro knobs used for tuning the receiver noise figure are the 3 stage bias control knobs on the LNA. Fig. 4.30 show the results of noise figure self-tuning by tuning the three different stages of the bias on the LNA.

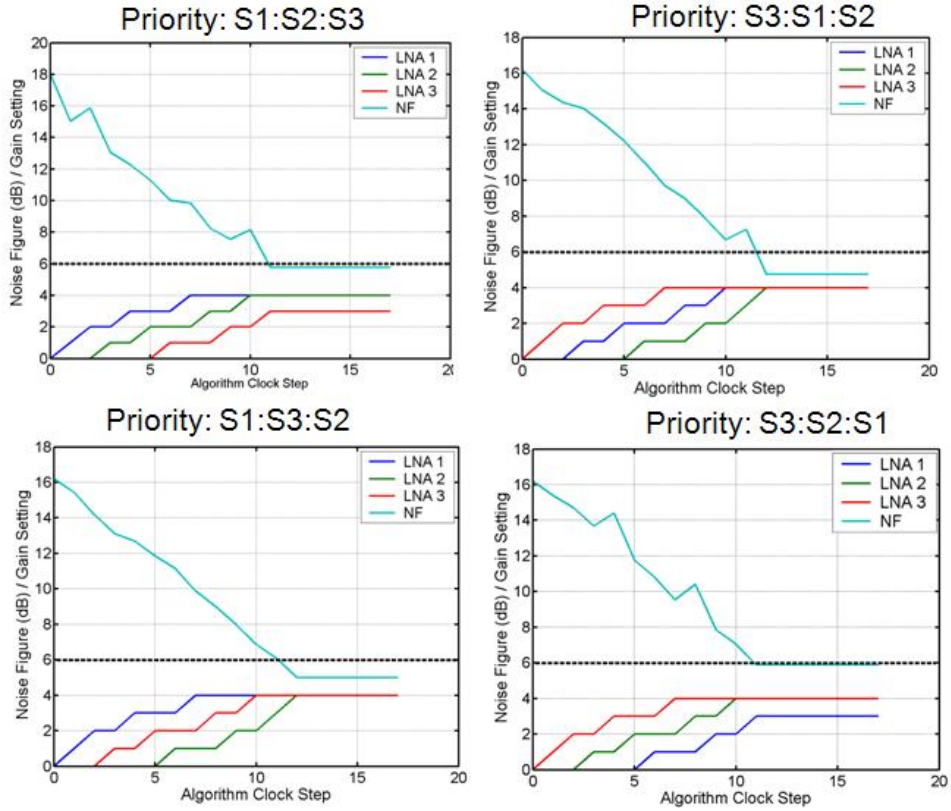


Fig. 4.30 Noise figure self-healing results

From Fig. 4.30, it can be seen that different priorities result in the decrease of the noise figure showing the effectiveness of noise figure healing. Again, in these situations, the solution in which gives the minimum power consumption and best linearity is favored. From measurement results, tuning the control knobs from out-to-input which is stage3 to stage2 to stage1 is the most optimal choice. Fig. 4.31 shows the yield performance for noise figure self-healing. The targetted noise figure after healing is 6 dB, and after self-healing all 10 chips have successfully achieved the targetted system specification.

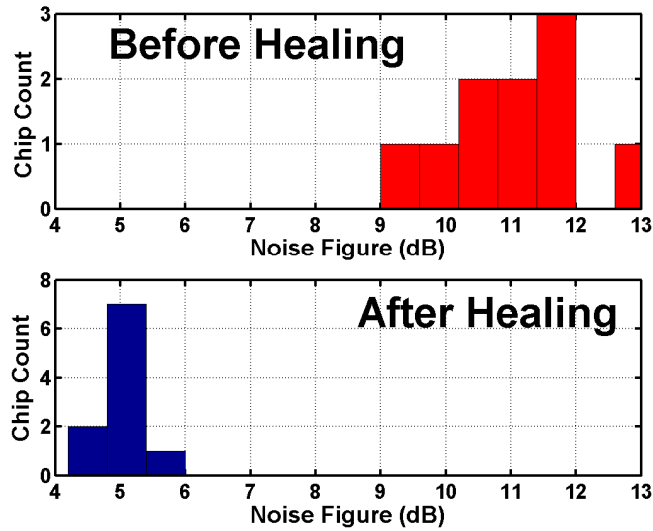
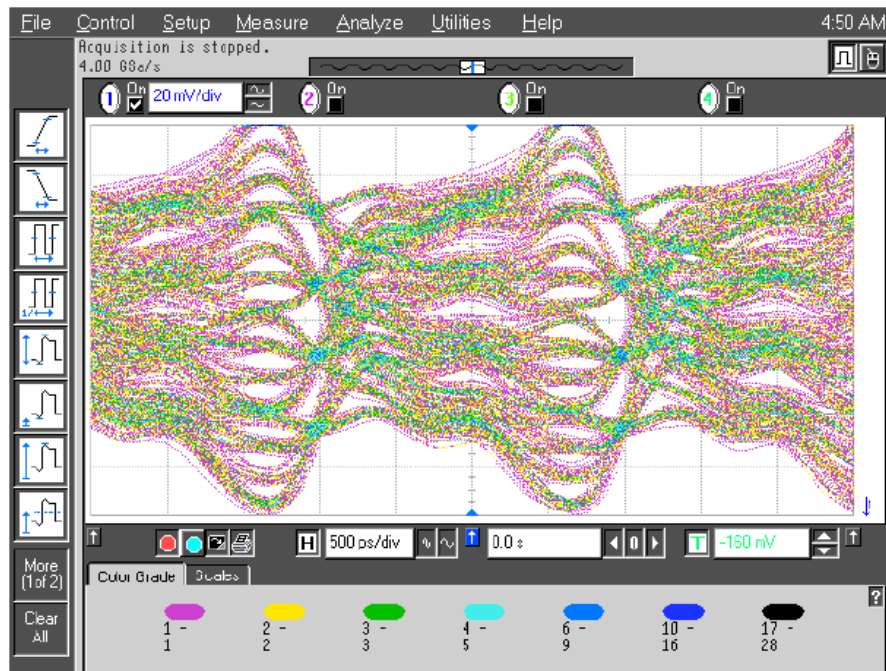
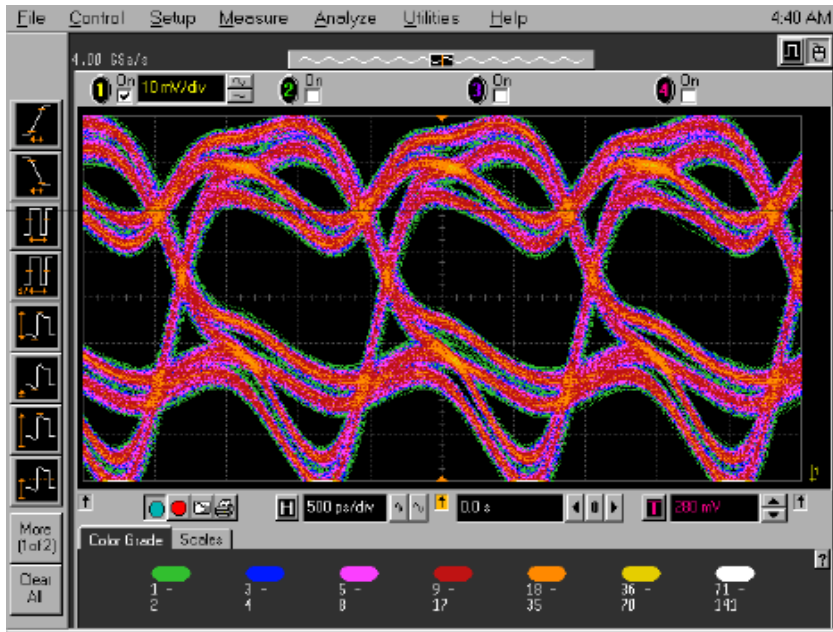


Fig. 4.31. Yield result before and after receiver noise figure self-healing

Besides self-healing functions, transceiver loopback testing are also conducted to verify the throughput performance of the self-healing transceiver. Fig. 4.32 shows the eye diagram with QPSK modulation by applying the PRBS generated bits from DAC controller. And Fig. 4.33 shows the eye diagram when 16-QAM modulation is applied. With a 1 GHz signal bandwidth, the maximum throughput that the self-healing transceiver can achieve is 4 Gb/s.

The entire 60 GHz self-healing radio occupies an area of 4mm-by-4mm. The total power consumption when running is 667 mW. This includes 198 mW for the transmitter, 177 mW for the receiver, 176 mW for the transmitter and receiver synthesizer, and 116 mW for both the ADC and the DAC mixed-signal converters.



## 4.4 Conclusion

In this chapter, the architecture and implementation results of the DAC control unit, parameter estimator, and the integrated self-healing transceiver is presented. The DAC control unit provides single-tone, two-tone, and modulation signals to drive the DAC. These generated tones can be adjusted in amplitude, DC offset, and phase rotation by the IQ unit following the DDFS. The DAC control unit operates at a clock frequency of 2.0 GHz, it is achieved by 4-parallel time interleaved processing architecture where each of the sub-DDFS are clocked at 500 MHz. The combined DAC control unit and DAC achieves a SFDR performance of 40dB at 1 GHz signal output which is enough to support the self-healing requirements as well as complex signal modulation up to 16-QAM.

The parameter discussed in 4.2 is a FFT processor based spectrum analyzer. The parameter estimator takes the digital samples from the auxiliary ADC and estimates the spectrum with the 128pt FFT processor. With a 5 MHz bandwidth, the spectral resolution is 0.78kHz to support self-healing monitoring. The parameter estimator can also perform different number of averaging to reduce the noise, the computed averaged spectrum information is stored in the on-chip registers and then readout to the PC for further analysis. The parameter estimator is the key circuit to the monitoring of the RF impariments in the self-healing transceiver.

In the last part of the chapter, the results of 4 Gb/s 60 GHz self-healing transceiver implementation results are presented. For all the self-healing algorithms, the DAC controller is applied to generate stimulus tones. The



parameter estimator is applied to estimate the spectrum from the envelope detector, power detector, and receiver to heal for nonlinearity, IQ mismatch, and the noise figure of the receiver. With the on-chip signal generator and spectrum analyzer, it also saves a lot of effort to setup the probes and instrumentation for mm-Wave transceiver testing before production to characterize the transceiver performance. The Self-healing approach with low power and area overhead make it an attractive approach to increase the effective yield for CMOS based transceiver to combat process variations at nanometer. The self-healing transceiver occupies an area of 4mmx4mm and a total power consumption of 667mW when operating.

## **Chapter 5 Baseband Modem Design for 60 GHz System**

In this chapter the baseband modem design for a multi-Gb/s 60 GHz system will be discussed. The baseband modem's main purpose in a transceiver is to modulate the data into digital symbols, perform pulse shape filtering, synchronization, equalization, and demodulation. At 60 GHz, since the available bandwidth per-channel is at least 2 GHz, low spectral efficiency modulation methods are preferred. In IEEE 802.15.3c and IEEE 802.11ad, the most spectral efficient modulation format applied is 16-QAM, higher order modulation like 32-QAM or 64-QAM is not preferred since this will add additional SNR and linearity requirements on the already power hungry GS/s ADC and DAC [1],[2],[34].

To achieve GS/s symbol processing on the 60 GHz baseband modem, parallel signal processing must be applied. For the IEEE 802.15.3c standard where the required symbol sampling rate is 1.76 GS/s, 4-parallel or 8-parallel signal processing datapath architecture must be adopted in order to meet the timing constraints of a 65nm or 40nm digital standard cell library.

In this chapter we will present with the design of a channel equalizer targeted for 60 GHz communication link.

## 5.1 Dual Mode OFDM/Single-Carrier Frequency Domain Equalizer

For high throughput wireless systems, multipath channel equalization is one of the most challenging functions in the design of a digital baseband modem. If the forward error control (FEC) decoder is not considered, the equalizer hardware itself is generally the most power/area consuming block in the baseband modem [35]. The hardware complexity of the equalizer is proportional to the multipath channel inter-symbol-interference (ISI) delay spread. To compensate for these channel induced ISI effects, baseband modems apply OFDM modulation techniques or time domain equalizers. An EQ applying OFDM-like 1-tap channel frequency response inversion process is preferred over time domain decision-feedback equalizers (DFEs) when communicating in a 60 GHz non-line-of-sight (NLOS) multipath channel environment where the RMS channel delay spread may exceed over 10 ns. In this kind of a channel environment, designing DFEs for single-carrier transmission systems requires a large number of feedback filter taps to compensate the multipath fading. For an addition of each filter tap, a complex multiplier is required. If 4-parallel signal processing is applied, this means 4 complex multiplier for each increase of symbol delay spread. In addition, the extra loop unrolling and the parallel look-ahead symbol decision hardware necessary to support multi-Gb/s throughput with complex modulations like 8PSK or 16QAM makes DFEs impractical to apply in terms of area and power consumption. As a result, most previously reported Gb/s baseband DFEs for wireless baseband modems support only simple modulation methods like QPSK or MSK [36],[37].

From the baseband system integration point of view, when the wireless system integrates several wireless connectivity solutions with different modulation methods, hardware sharing to reduce system power/area cost is highly desired. For example, 60 GHz systems like IEEE 802.15.3c or IEEE 802.11ad will most likely be integrated with legacy indoor wireless connectivity systems like IEEE 802.11a, 802.11n, and 802.11ac. Currently, most wireless connectivity systems at 60 GHz supports both OFDM and single-carrier modulation. An equalization hardware architecture that would be able to fully utilize the FFT processor which is required by the OFDM receiver to perform channel estimation, equalization, and other signal processing functions for the demodulation of single-carrier signals is a preferable way to save the extra hardware dedicated for single-carrier signal processing. Single-carrier frequency domain equalization (SC-FDE) then becomes an attractive solution as its concepts and datapath are similar to those of an OFDM receiver [38].

In this dissertation, we present a 7 Gb/s frequency domain minimum mean squared error (MMSE) equalizer chip for 60GHz wireless communication system. To achieve Gb/s throughput, parallel processing architecture must be applied when the circuit is implemented in CMOS 65nm or 40nm standard cell libraries. In the IEEE 802.15.3c or IEEE 802.11ad standard, the required symbol sampling rate is 1.76 GS/s, and to achieve this targeted sampling rate, the proposed equalizer applies 4-parallel signal processing with CMOS TSMC 65nm GP standard cell library. 4-parallel signal processing architecture allows this equalizer chip to achieve an overall symbol sampling rate of required by the IEEE

802.15.3c standard while the core DSP circuits are clocked at  $1/4$  ( $1.76\text{GHz}/4=440\text{MHz}$ ) the input symbol rate. This equalizer chip is equipped with a 512pt FFT processor and a 512pt IFFT processor to demodulate the received OFDM and single-carrier signals. The 512pt FFT processor is used by both OFDM and single-carrier modulation to transform symbols to frequency domain for equalization or synchronization while the 512pt IFFT processor is used by single-carrier modulation to convert the frequency domain symbols back to time domain for demodulation.

The equalizer also includes a time-domain Golay correlator based channel estimator to obtain the multipath channel frequency response (CFR), and it also includes a MMSE EQ for multipath channel correction in the frequency domain. To verify the proposed equalizer at Gb/s throughput during chip testing, differential input clock driver and low voltage differential signaling (LVDS) output drivers are also implemented in this chip for high speed chip loop back test.

### **Frequency Domain Equalizer System Block Diagram**

Fig. 5.1 shows the block diagram for 16QAM symbol equalization and the packet format of the proposed equalizer system. A transmission packet starts out with Golay sequence based preambles for receiver synchronization (SYNC) followed by two 256 symbol Golay channel estimation sequences “CES a” and “CES b”. Each Golay channel estimation sequence is appended with a postfix of 128 symbols. Following the Golay sequences is the block based packet payload

with cyclic prefixes (CP) in between. The length of the CP can be configured at 1/8, or 1/4 the length of a payload block and each payload block consisting of 512 samples can be demodulated with the 512pt FFT/IFFT processors. The proposed packet format is referenced from the IEEE 802.15.3c standard preserving the key characteristics of the Golay channel estimation sequences.

In this proposed equalizer, to process the GS/s input symbols while meeting the timing constraints of 65nm CMOS digital circuits, 4-parallel signal processing architecture is adopted since the targeted symbol rate 1.76 GS/s is too high to achieve in a single stream architecture when implemented with 65nm standard cells. The applied hardware parallelism allows the core computation circuits to be clocked at 1/4 the input symbol rate which is 440 MHz.

In the SC-FDE mode, after ADC processing and initial receiver synchronization processing, the SC-FDE takes in the 4-parallel channel distorted symbol streams and performs equalization before symbol demodulation. The equalization process is basically divided into two stages: channel estimation and channel equalization. The signal “CES\_on” in Fig.5.1 sets the EQ in channel estimation or equalization mode. The channel estimator first applies the received Golay channel sequence correlation values to estimate the multipath channel impulse response (CIR) information. Next, by taking the FFT of the CIR and storing it to the SRAM, the CFR needed for frequency domain equalization can be obtained. After channel estimation, the multipath distorted symbols in the packet payload are sent to the FFT processor for equalization. In the frequency domain,

these symbols are equalized based upon MMSE criterion. After channel correction, the equalized symbols are then sent to the IFFT processor for demodulation in time domain. In the OFDM modulation mode, since the modulation symbols are generated in frequency domain on the transmitter side and through IFFT these OFDM symbols are converted to time domain. Through the initial receiver processing and channel estimation, the received time domain channel distorted OFDM symbols are sent to the frequency domain by the FFT processor for channel equalization. After MMSE channel equalization, the channel corrected OFDM symbols are demodulated in the frequency domain.

The final 4-parallel demodulated output bit streams for both the OFDM and the SC-FDE modes are multiplexed out for post processing through the 2 on-chip LVDS output drivers. Although in Fig.5.1, the demodulation is shown for 16-QAM, the situation is similar for BPSK or QPSK modulation methods. The only difference is at how the LVDS output drivers multiplex the output bit streams.

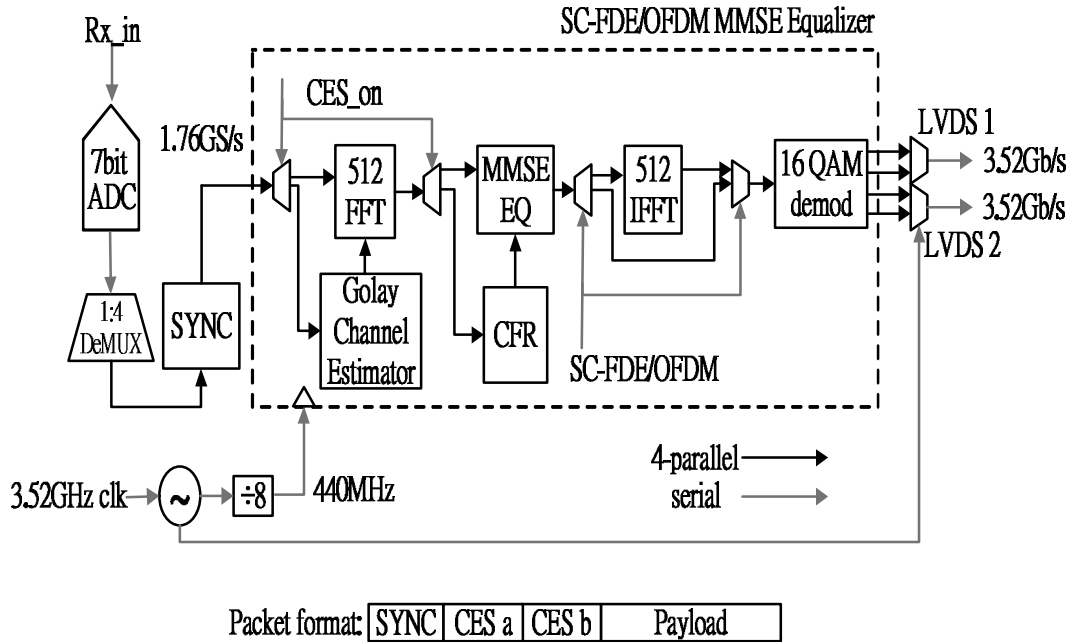


Fig.5.1. Frequency domain equalizer system

Fig. 5.2 shows the architecture of the 4-parallel 512pt FFT processor. It is composed of 4x time interleaved 128pt FFTs combined together through 3 complex multipliers, twiddle factor lookup tables (LUT), and a radix-4 4pt FFT unit. Each 128pt FFT processor is implemented with 7-stage pipelined radix-2 single-path delay feedback architecture. This is chosen for the 128pt FFT/IFFT processors as it has the simplest control and it can be easily extended to variable-length FFT processing for power saving purposes. With considerations of a more flexible layout floorplan to meet the circuit timing requirements, the FIFO memories used in the FFT processors are implemented with standard cell registers.



The complex multipliers (CM) in the first 3 stages of the 128pt FFT/IFFT processors are implemented with general multipliers, while in the final 4 stages, the CM are implemented with Canonical Signed Digit (CSD) multipliers composed of hardwired shifters and adders to save area and power [39]. The 512pt FFT processor has an input of 7b and output of 11b while the 512pt IFFT processor has an input of 11b and output of 8b. The 7b input is to cope with a 7b ADC that supports modulation formats up to 16-QAM. Through combinations of bit truncation and numerical scaling at every stage, the 512pt FFT and 512pt IFFT processors both provide a SQNR of at least 31dB to support complex modulation methods up to 16QAM in a non-line-of-sight indoor wireless channel environment.

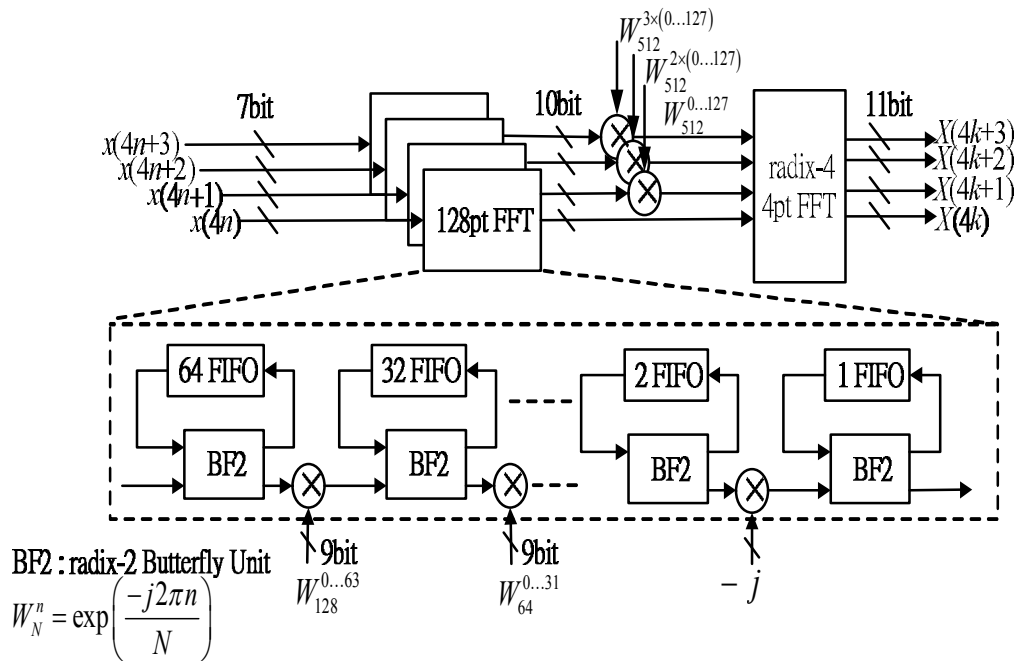


Fig.5.2. 512pt FFT processor architecture

## 5.2 Channel Estimator and MMSE Equalizer

The channel estimation method of the proposed equalizer is based on utilizing the complementary Golay sequences to obtain the channel frequency response. Golay sequences are also applied in IEEE 802.15.3c and IEEE 802.11ad standards for channel estimation [1],[2],[40]. Complementary Golay sequences ‘‘CES a’’ and ‘‘CES b’’ with a length of  $L=2^N$  have the property that the sum of their autocorrelation is a delta function [41]. The property is as follows:

$$R_a[i] + R_b[i] = 2N\delta[i] \quad (5.1)$$

where

$$\begin{aligned} R_a[i] &= \sum_{n=0}^{N-i-1} a_N[n+i]a_N^*[n] \\ R_b[i] &= \sum_{n=0}^{N-i-1} b_N[n+i]b_N^*[n] \end{aligned} \quad (5.2)$$

and  $R_a[i]$  and  $R_b[i]$  are the autocorrelation of the sequences CES a and CES b. This property can be applied to obtain the channel impulse response (CIR), the sum of the cross-correlation values between the received Golay sequences and the sequences themselves is the CIR. Benefits of applying Golay sequences for channel estimation are a multiplier free correlator, and a lower estimation error compared with the frequency domain based zero-forcing (ZF) method applied in [6]. In the ZF method, estimation accuracy is lost through the quantization error resulted from the estimation computation in the frequency domain where all the preamble symbols have to be first sent to the FFT processor before estimation.

Another way of viewing the benefits of time domain Golay channel estimation over frequency domain channel estimation is that by estimating the channel impulse response in the time domain, all the signal energy used in the estimation process is allocated to the first few main multi-path channel taps with large energy; as opposed to channel estimation in the frequency domain where all the signal energy is allocated to the frequency bins from FFT processing. Considering the finite quantization effects for high-speed VLSI systems applied by 60 GHz systems, it would be a better strategy to estimate the channel impulse response in the time domain and not suffer from the SNR loss due to FFT processor quantization effects when frequency domain channel estimation is applied.

Fig.5.3 shows the serial Golay correlator. It is very suitable for high-speed VLSI implementations since for a length  $L=2^N$  Golay sequence the correlator consists of only  $N$  registers,  $N$  inverters, and  $2N$  adders. However even with this simple architecture, it is impossible to achieve the timing requirements of the 1.76 GS/s. If the serial Golay correlator is applied using the serial architecture, the channel estimator have to be clocked at 1.76 GHz. This is not possible for a 65nm standard cell library considering the adders applied in the Golay correlator would easily reach 13b~15b, the critical path is too long. In this equalizer, a 4-parallel Golay correlator based channel estimator is proposed to achieve the GS/s input sampling rate. By applying a loop unrolling of 4 and architecture transformation, the functionality and the total number of delay registers in the parallel correlator remain the same compared with the serial correlator while the extra hardware for implementing the parallel correlator are the adders in each stage.

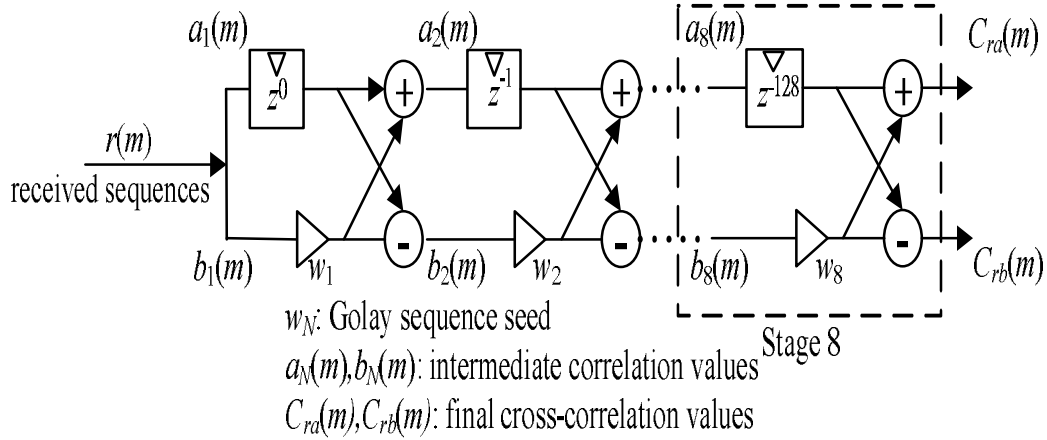


Fig. 5.3. Serial Golay correlator

Fig. 5.4 shows the 8-stage parallel Golay correlator based channel estimator. It first calculates the parallel scaled cross-correlation values  $C'_{ra}(4n+j)$  and  $C'_{rb}(4n+j)$ ,  $j=0\sim3$ , from the received Golay sequences. At each stage, the intermediate output correlation values are scaled down by dividing by 2 using 1b shifters to avoid wordlength inflation in the later stages and to satisfy the Golay sequence properties. As the wordlength increases, it would be harder to meet the timing requirements. Then after scaled correlation computation is done,  $C'_{ra}(4n+j)$  and  $C'_{rb}(4n+j)$  are sent to the FFT processor to generate frequency domain  $FC_{ra}(4k+j)$  and  $FC_{rb}(4k+j)$  cross-correlation samples to obtain the channel frequency response. The  $FC_{ra}(4k+j)$  samples are first stored in the SRAM while  $FC_{rb}(4k+j)$  are being computed. Once  $FC_{rb}(4k+j)$  are available, each  $FC_{ra}(4k+j)$  sample is read from the SRAM and the CFR is obtained by taking the average of the two at each frequency index. By applying this approach, it saves the power and the computation time of storing just the channel impulse response and having

to transform the channel impulse response to the frequency domain each time equalization is performed. The final computed CFR is then written to SRAM for channel equalization. (5.3) shows the averaging of the cross-correlation of the CES a and CES b in the frequency domain which results in the channel frequency response.

$$\text{CFR: } H(4k+j) = (1/2) (FC_{ra}(4k+j) + FC_{rb}(4k+j)) \quad (5.3)$$

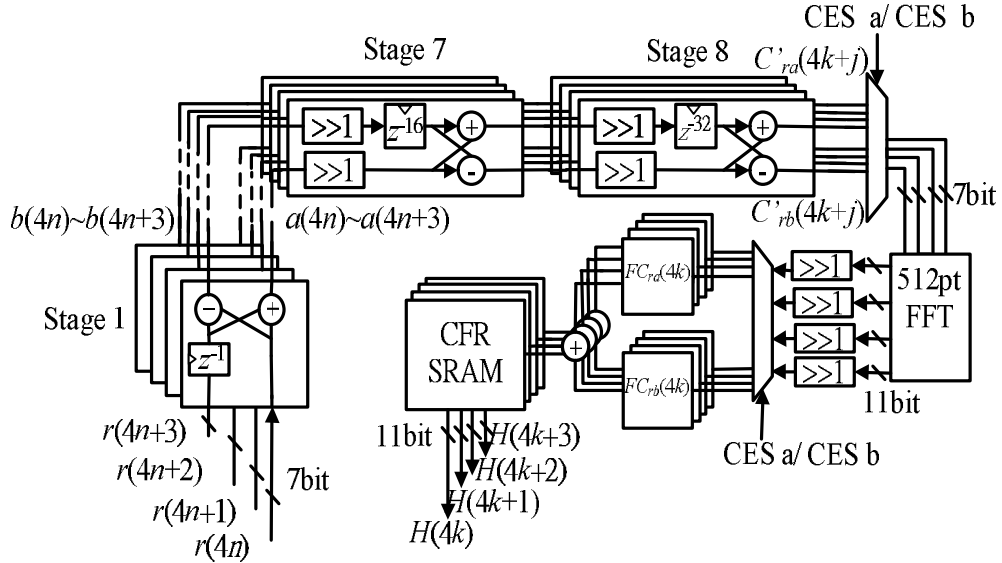


Fig. 5.4. Parallel Golay correlator based channel estimator

Fig.5.5 shows the architecture of the frequency domain minimum mean squared error (MMSE) equalizer. The characteristics of MMSE equalization is that the

received channel distorted symbols are corrected by multiplying with the noise normalized inverse CFR coefficients [43]. In Fig. 5.5,  $SNR^{-1}$  is the inverse signal-to-noise ratio. To minimize the computation latency of the MMSE equalizer, the divider in the equalizer is implemented with a 10bit interpolated inverse value LUT and a multiplier resulting in a total latency of 2 clock cycles. LUT based divider is preferred over long division based dividers as the computation latency is much lower, and for the 16-QAM modulation purposes a LUT based solution is enough in resolution.

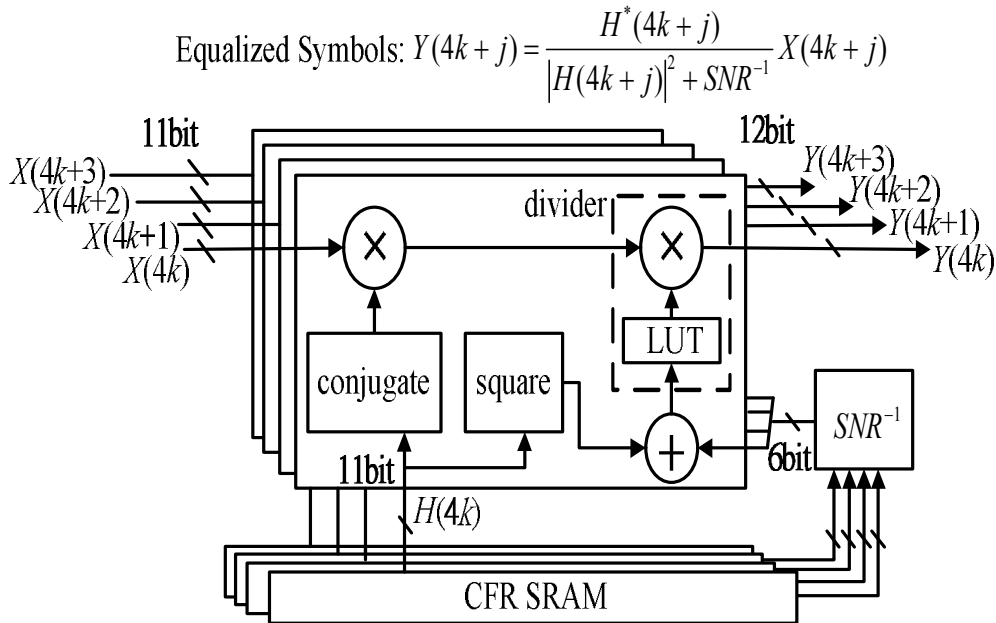


Fig. 5.5. MMSE equalizer architecture

To achieve MMSE equalization, the inverse SNR value has to be estimated. One simple way to obtain the signal power estimation is to accumulate the absolute value of the estimated CFR.

$$S = (1/512) \sum_{j=0}^3 \sum_{k=0}^{127} |H(4k+j)|^2. \quad (5.4)$$

The noise variance can be approximated as the accumulated squared absolute differences between the CFR and the frequency domain cross-correlation samples.

$$N = (1/2)(1/512) \left[ \sum_{x=a}^b \sum_{j=0}^3 \sum_{k=0}^{127} |H(4k+j) - FC_{Rx}(4k+j)|^2 \right]. \quad (5.5)$$

In (5.5), there are two different estimation which are respectively CES a and CES b. The hardware necessary to compute the signal power and the noise power are basically the squaring circuits, the adders, the accumulators, and the registers. To simplify the divider to calculate the inverse of the SNR, it is implemented with LUT and a multiplier.

Fig.5.6 shows the uncoded BER performance curves from bit-true RTL simulation using a NLOS residential channel model with RMS delay spread of 10ns. We can see that MMSE EQs outperforms ZF EQs due to their capability of noise suppression at channel nulls. Note that in Fig.6 OFDM BER performance is more inferior compared with the performance of SC-FDE due to uncoded system assumption.

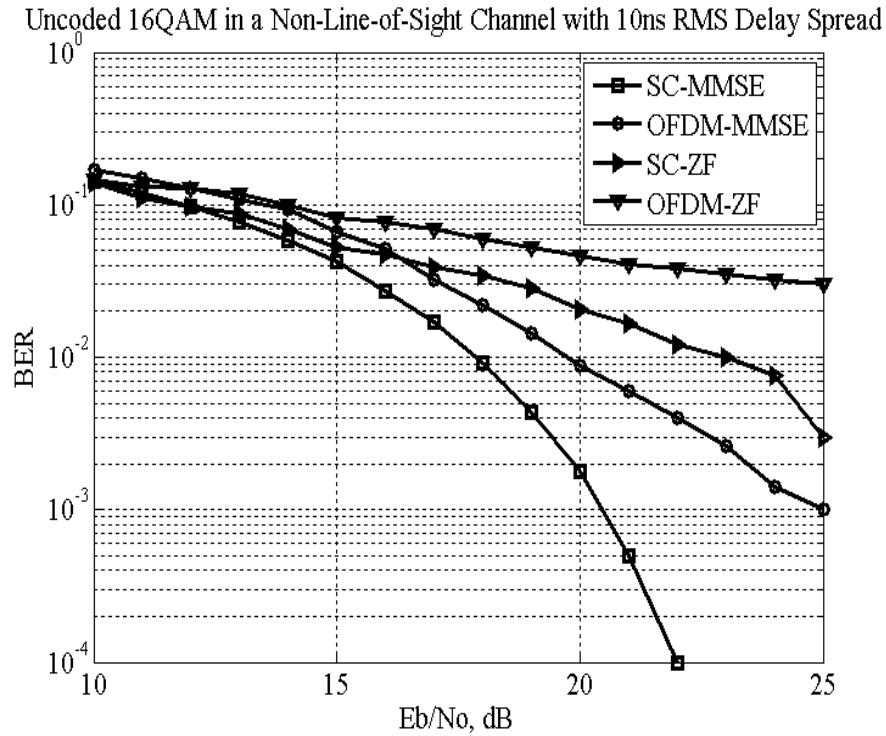


Fig. 5.6. BER performance plot

### 5.3 Equalizer Implementation and Measurement Results

The SC-FDE/OFDM dual-mode baseband equalizer is fabricated in TSMC 1P6M 65nm CMOS process with a core area of  $1.12\text{mm}^2$  and a die area of  $3.22\text{mm}^2$ . The total gate count of the equalizer chip including the test circuitry is 640K gates. On-chip BPSK, QPSK, and 16QAM (de-)modulators with 4-parallel PRBS generators and checkers are implemented to verify the equalizer's functionalities. A 3-wire serial interface is installed on-chip to test different operating configurations of the equalizer. Also through the 3-wire interface, test data samples can be written to the registers or the SRAM to perform EQ



functional checks and the computed output samples can be read asynchronously by the PC while the equalizer itself is clocked at full speed. Fig.5.7 shows the equalizer testing setup, it includes power supplies for the equalizer's digital core, analog IO drivers. The test setup includes a high speed signal generator for clock source, oscilloscope for IO bit stream capturing, and a PC for USART control to configure the equalizer chip.

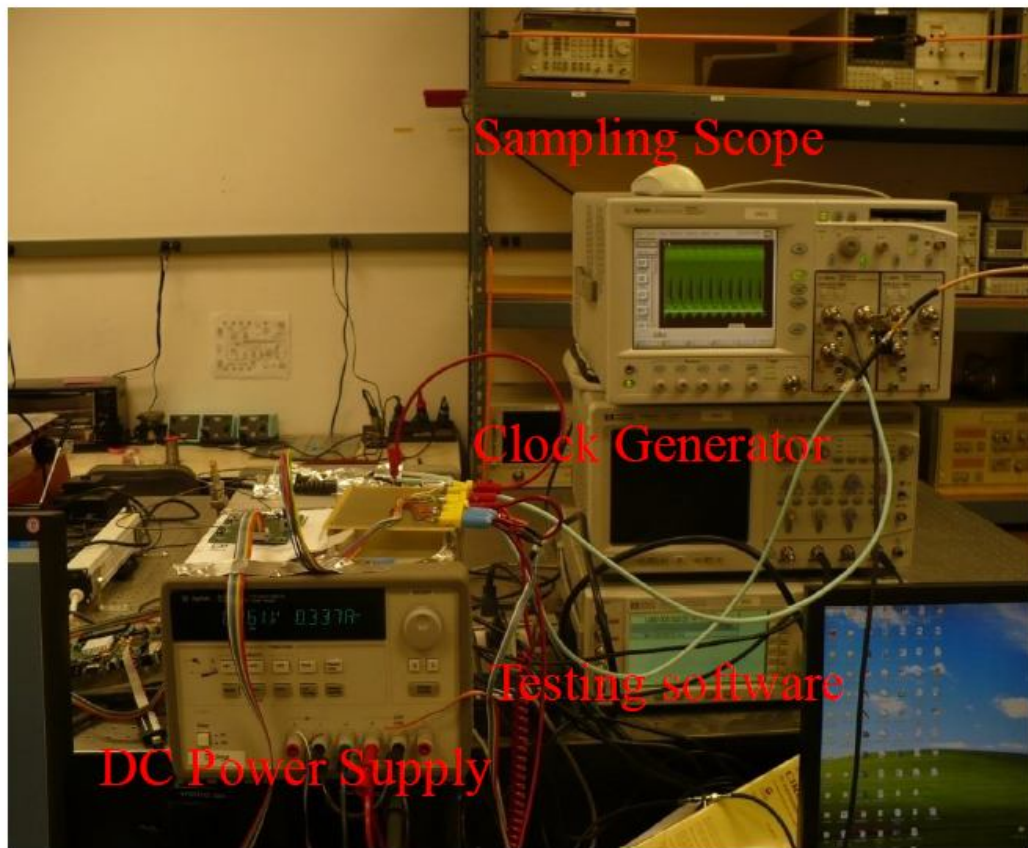


Fig.5.7 Equalizer testing setup

A total of 4 clock domains are contained in this equalizer chip: the high speed differential input clock, the equalizer core which is clocked at 1/8 the input clock, the output multiplexers and the LVDS output drivers which can be clocked at either the input clock or 1/2 of it depending on symbol modulation scheme, and the 3-wire interface whose sub-MHz clock is supplied from the PC. Fig. 5.8 shows the chip micrograph. In this chip, while all the DSP circuits are designed by digital standard cells approach, the high speed input clock driver and the LVDS output drivers are designed by an analog full custom approach.

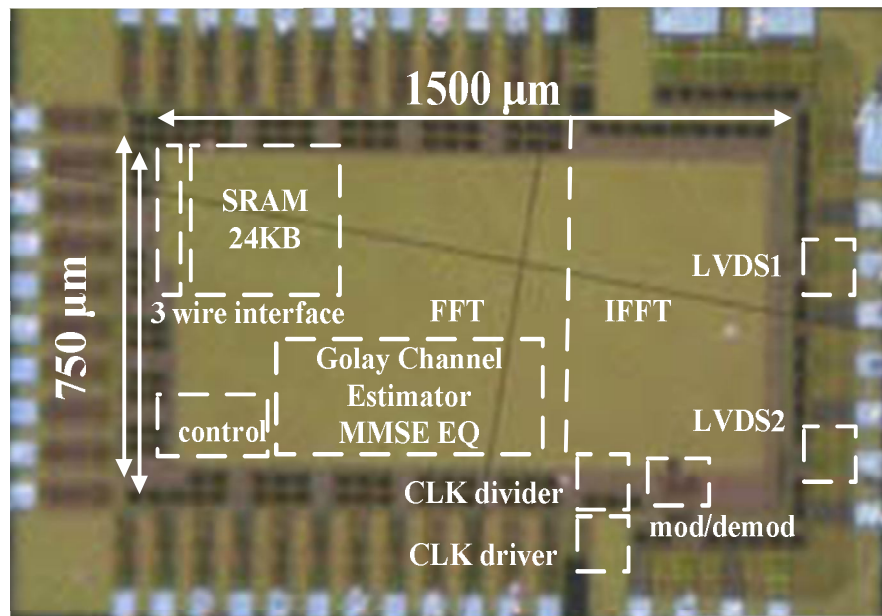


Fig. 5.8 Equalizer chip die-photo

This EQ chip has been successfully tested with a supply voltage ranging from 0.9V to 1.2V. The maximum measured symbol sampling rate at 1V supply is 1.46 GS/s with 5.84 Gb/s throughput when 16-QAM modulation is applied. The power consumption at this configuration is 124 mW for the SC-FDE mode and 88mW for the OFDM mode. The main power difference is that the 512pt IFFT processor is turned off in the OFDM mode. When the supply voltage is increased to 1.2V, the symbol sampling rate reaches 1.76 GS/s providing a throughput of 7 Gb/s at a power consumption of 208 mW for the SC-FDE mode and 148 mW for the OFDM mode. This supports the 1.76GHz chip rate defined in the IEEE 802.15.3c standard [1]. The first part of Fig. 5.9 shows the measured eye diagram from one of the two LVDS output drivers when a 2.92 GHz input clock is applied with 1V supply voltage in SC-FDE mode with 16-QAM modulation. The second part of Fig. 5.9 shows the measured eye diagram when the supply voltage is increased to 1.2V and the input clock is set at 3.52GHz. The chip summary is shown in Table 5.1. Comparison with previously reported chips having similar functions is shown in Table 5.2.

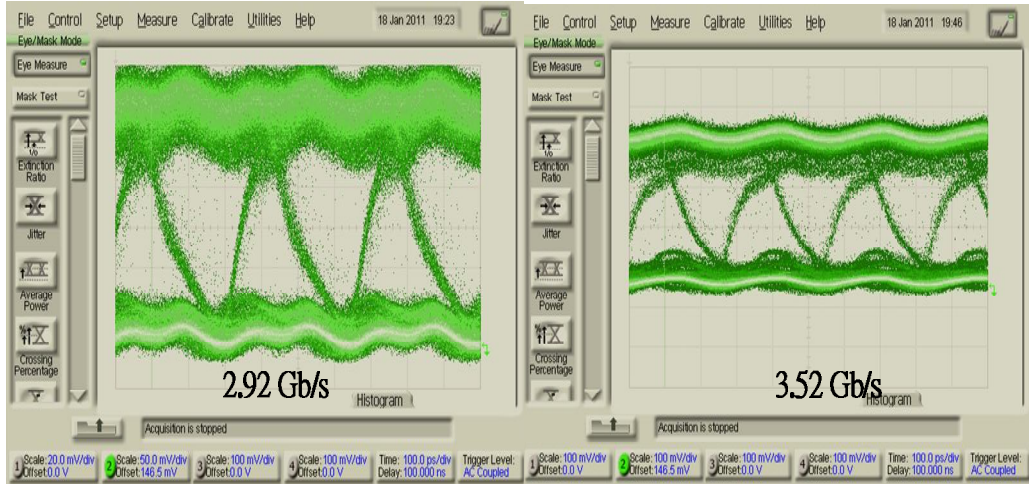


Fig. 5.9. Measured Eye Diagrams with 16-QAM modulation

Table 5.1 Equalizer chip summary

Technology	TSMC 65nm CMOS
Supply	0.9V~1.2V(core), 2.5V (I/O)
Area	1.12mm <sup>2</sup> (core), 3.22mm <sup>2</sup> (die)
Gate Count	Total: 640K 512pt FFT: 216K 512pt IFFT: 255K Golay Channel Estimator: 76K MMSE EQ: 51k 3-Wire Serial Interface: 0.4K Others (control, testing, (de-)modulator clocking, and etc.): 42k
SRAM	24KB
Throughput	5.84Gb/s(@1.0V,365MHz) 7Gb/s(@1.2V,440MHz)
Power	SC-FDE: 124mW(@1.0V,365MHz) 208mW(@1.2V,440MHz) OFDM: 88mW(@1.0V,365MHz) 148mW(@1.2V,440MHz)

Table 5.2 Equalizer chip comparison

	This Work	[37]	[45]	[46]
Process	65nm	90nm	90nm	130nm
Functions	4-parallel 512- FFT/IFFT Golay MMSE EQ	DFE with 4bit-ADC	8-parallel 256 FFT	4-parallel 1024-FFT ZF EQ LDPC- OFDM
Core Area	1.12mm <sup>2</sup>	1mm <sup>2</sup>	3.53mm <sup>2</sup>	17.80mm <sup>2</sup>
Clock/Core Freq.	3.52GHz/ 440MHz	1GHz/ 1GHz	N.A./ 447MHz	N.A./ 147MHz
Gate Count	640k	N.A.	583k	1.58m
Throughput	7Gb/s (16QAM)	1Gb/s (MSK)	N.A.	820Mb/s (QPSK)
Power	208/148mW	55mW	145.5mW	391mW
Energy	29.5/21pJ/b	55pJ/b	N.A.	476pJ/b

## **Conclusions**

This Chapter presents a frequency domain SC-FDE/OFDM MMSE equalizer chip targeted for indoor 60GHz NLOS wireless communications.

By applying 4-parallel signal processing architecture, the 640K gates chip provides a 7 Gb/s throughput with 16-QAM modulation at 1.2V supply. This is the first design in CMOS 65nm process to demonstrate multi-Gb/s throughput combined single-carrier and OFDM MMSE equalizer with 512pt FFT and IFFT processing.

## Chapter 6 Conclusion

In this dissertation, the DSP circuits and systems for a 4 Gb/s self-healing 60 GHz transceiver is presented. The self-healing controller is applied to perform concurrent calibration on multiple RF transceiver parameters to optimize the 60 GHz CMOS transceiver performance under nanometer CMOS process variations to optimize the transceiver performance. The digital baseband circuits applied to generate probe testing signals like the 2.0 GHz DAC controller is presented. 4-parallel time interleaved architecture is applied to achieve this operating frequency. 128pt FFT based spectrum analyzer serving as the parameter estimator is applied as the environmental monitoring processor in the self-healing controller. The self-healing algorithms and system level testing results are also presented in the dissertation. The whole self-healing chip occupies an area of 4mmx4mm and a total power consumption of 667mW when operating.

In the second part of the dissertation, implementation aspects of a digital modem for a multi-Gb/s 60 GHz SOC radio are discussed. A 7 Gb/s OFDM/Single-Carrier frequency domain equalizer in 65 nm is presented as an example as one of the key processing functions in a Gb/s wireless modem for 60 GHz applications. 4-parallel signal processing architecture allows this equalizer chip to achieve a symbol sampling rate of 1.76 GS/s while the core DSP circuits



are clocked at 1/4 the input symbol rate. This equalizer chip is equipped with a 512pt FFT processor and a 512pt IFFT processor to demodulate the received OFDM and single-carrier signals. It includes a time domain Golay correlator based channel estimator to obtain the multipath channel impulse response, and it also includes a MMSE equalizer for channel correction in frequency domain. The total gate count for the equalizer chip is 640K and the throughput of the chip reaches 7 Gb/s with 16-QAM modulation at 1.2V supply. This is the first design in CMOS 65nm process to demonstrate mult-Gb/s throughput combined single-carrier and OFDM MMSE equalizer with 512pt FFT and IFFT processing.

Looking ahead to the future, the self-healing radio design can be improved by decreasing the healing time. In the presented 4 Gb/s self-healing transceiver, most of the self-healing sequencings are initiated by the USART interface. The communication link between the USART and the PC is slow compared with the symbol operating frequency on the self-healing transceiver. By implementing most of the self-healing algorithms on-chip will greatly decrease the healing time and make the self-healing system more efficient. Of course, implementing all the functions on-chip, the system and circuit designers must consider tradeoffs of the system's verification flexibility, and the extra power/area overhead of implementing everything on-chip. The performance of the self-healing radio can also be greatly improved when the design of the baseband modem is considered in the early stages of the self-healing architecture planning. In the presented chip, self-healing and baseband modem were designed separately and not much considerations were put on how they interact with each other. By design them as a

whole and optimizing them together as an integrated digital radio processor that performs as a self-healing controller and modem, a lot of the hardware resources can be shared and reused thereby lowering the total SOC power/area consumption.

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