UNIVERSITY OF CALIFORNIA,
IRVINE

# A Glitch-Less Serializer and a MedRadio-Band Oscillator for Brain-Computer Interfaces

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical and Computer Engineering

by

Omid Malekzadeh Arasteh

Thesis Committee:
Professor Payam Heydari, Chair
Professor Zoran Nenadic
Assistant Professor An H. Do

# DEDICATION

*To my family*

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# ACKNOWLEDGMENTS

I would like to thank my advisor, Professor Payam Heydari for providing me with the opportunity to work on a number of exacting projects, none of which would have been completed without his persistent guidance and support. I am also grateful to my committee members, Professor Zoran Nenadic and Dr. An H. Do for their advice and insightful discussions.

I would like to thank all my colleagues at Nanoscale Communication IC (NCIC) Lab, in particular, Dr. Alireza Karimi Bidhendi and Mao-Cheng Lee for their mentorship and friendship.

I would like to acknowledge Tower Semiconductor, MOSIS and TSMC for facilitating the chip fabrication. I also thank Institute of Electrical and Electronics Engineers (IEEE) for giving me permission to include parts of my previously published papers in this thesis.

# ABSTRACT OF THE THESIS

A Glitch-Less Serializer and a MedRadio-Band Oscillator for Brain-Computer Interfaces

By

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Master of Science in Electrical and Computer Engineering

University of California, Irvine,

Professor Payam Heydari, Chair

This thesis presents the design and implementation of a glitch-less serializer and a MedRadio-band oscillator, required for neural recording and wireless communication in brain-computer interfaces. The state-of-the-art multi-channel brain signal acquisition relies on analog serialization which suffers from a number of non-idealities such as crosstalk and glitches. To minimize the latter effect, a non-overlapping clock generator logic is employed, which uses a gray-code scheme in the binary counter to avoid race conditions. This approach ensures that bit toggling during the channel sequencing does not cause unintended switching which would have introduced glitches in the serializer. A 4-channel brain signal acquisition prototype is fabricated in a 180nm CMOS process, exhibiting negligible crosstalk and no glitches. For the wireless link, most implantable systems further necessitate an inductorless transceiver design to account for the magnetic resonance imaging compatibility. An ultra-low power MedRadio-band (401-406 MHz) oscillator is demonstrated, which employs a 7-stage current-starved ring oscillator to meet this requirement. Fabricated in a 28nm CMOS process, the digitally controlled oscillator utilizes a coarse- and fine-tuning mechanism to compensate for process, voltage and temperature variations. The oscillator dissipates 114.8 $\mu$W at 1V supply and achieves a wide frequency tuning range ($\sim$96 MHz) with $<$60 nS of settling time.

# Chapter 1

# Introduction

There are approximately 250,000 to 368,000 people living with chronic spinal cord injury (SCI) in the U.S. alone [5], and most of them are affected by impairment or complete loss of gait function. To restore walking, there is an eminent need to realize a fully implantable brain-computer interface (BCI), capable of bypassing the damaged spinal cord. Fig. 1.1 depicts the grand vision for such fully-implantable BCI. The system consists of a skull unit (SU), a chest-wall unit (CWU) and an exoskeleton. The SU acquires the brain signals which are then transferred via a tunneling cable to the CWU that handles the data processing and transmits the control commands wirelessly to a robotic exoskeleton. Given that the SU is placed in the proximity of the brain tissue, it becomes crucial to reduce power and heat dissipation. Furthermore, the overall power consumption limits the longevity of a fully implantable BCI and needs to be minimized as it is powered by a rechargeable battery.

The next two sections provide a brief overview of the fundamentals of biopotential signals and brain electrophysiology, followed by a review of design challenges in neural recording and wireless communication for BCI applications.

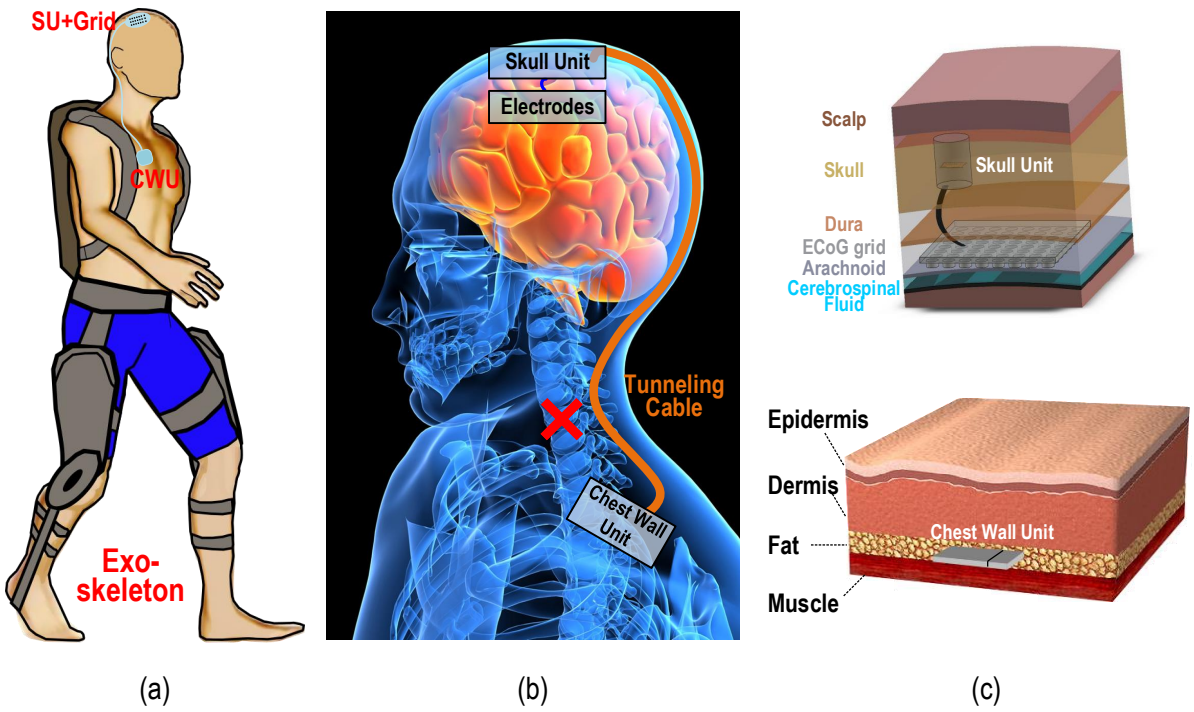



Figure 1.1: Proposed brain-computer interface: (a) system overview (b) implanted sub-modules (c) cross-section view of the implant sites.

## 1.1 Background

### 1.1.1 Biopotential Signals

Bioelectric potentials are produced as a result of electrochemical activity of a certain class of cells, known as excitable cells in the tissue [6]. The excitable cells exhibit two states: rest and active. At the rest state, the cell membrane is more permeable to K+ ions than Na+ ions and thus the internal medium builds a potential difference (-40 to -90 mV) relative to the exterior, to counteract the K+ ions diffusion gradient and reach an equilibrium. Once the excitable cell undergoes electrical stimulation either artificially or by the central nervous system, its membrane's permeability to Na+ ions increases such that its potential difference reaches +40 mV. However, this will be followed by a sharp decrease in the potential difference as the membrane returns to its resting state. This cycle of cellular potential is

referred to as the action potentials (AP) which is fundamental in generation of different biopotential signals such as electrocardiography (ECG), electromyography (EMG), electroencephalography (EEG), electrocorticography (ECoG) and local field potentials (LFP). In BCI applications, EEG, ECoG, AP and LFP are commonly used to observe neural activity.

### 1.1.2 Brain Electrophysiology

There is little known about how the human brain controls the limbs movement. Although, event-related synchronization of ECoG signals has been observed in response to lower and upper extremity movements, this relationship still remains to be explicitly characterized. It can be argued that the central and peripheral nervous systems are responsible for the generation of repeating temporal patterns to coordinate the muscle activity during human gait [7, 8, 9]. In fact, electrophysiological studies have shown that the sensorimotor cortex exhibits desynchronization in $\mu$ (8–13 Hz) and $\beta$ (14–40 Hz) bands during walking tasks [10, 11] as well as cyclic $\mu$-, $\beta$-, and $\gamma$-band modulation throughout the gait cycle [12, 13]. However, these studies were done using EEG which suffers from limited spatiotemporal resolution and motion artifacts. McCrimmon et al. [14] reported the first invasive electroneurophysiological characterization of the human leg (primary motor cortex, M1) during walking. ECoG signals were recorded from M1 area of human subjects as they performed various gait-related tasks. According to the findings, M1 is mostly responsible for the encoding of high-level gait control (i.e. walking duration and speed) instead of low-level patterns of leg muscle activation or movement trajectories. Hence, it is inferred that M1 interacts with subcortical/spinal networks, which are responsible for low-level motor control, to produce normal human walking. Based on this observation, a fully implantable BCI is envisioned to restore walking in SCI patients, which records neural activity, performs the required signal processing and transmits low-bandwidth control commands to a robotic exoskeleton.

## 1.2 Neural Recording

Although the input impedance of integrated circuits in CMOS technology is typically very high, a non-zero current would still flow from the brain to the input amplifiers [15]. This necessitates a transducer interface which converts the ionic current to electrical current, often called the biopotential electrode. Depending on the neural signal of interest, different electrode types with distinct impedances can be utilized. For ECoG, the electrode impedance typically varies between 1 to 5 k$\Omega$ and for EEG, the electrode impedance is about a few M$\Omega$ which can be reduced to a few k$\Omega$ by applying a gel between the scalp and the electrode.

The principal operation of this interface is based on the electrode-electrolyte interaction which governs the current flow. The electrolyte (i.e. brain tissue) contains no free electrons and the electrode contains no free cations or anions, thus a chemical reaction (oxidation/reduction) is necessary to allow the current flow. However, this will disturb the neutrality of the solution and creates a charge gradient at the electrode-electrolyte interface, causing a potential difference referred to as *half-cell potential*. Since the biopotential electrodes exhibit mismatches in reality, the half-cell potentials give rise to a differential DC electrode voltage offset (DEO) which can be quite large ($\sim$50 mV) and must be removed to avoid saturating the neural recording front-end.

To allow amplification of ECoG signals with amplitude <1 mV in the presence of the DEO, the neural amplifier should exhibit a high-pass filter (HPF) characteristics with very small corner frequency. Furthermore, it needs to provide low-noise amplification, reject common-mode aggressors such as the 50/60 Hz power-line interference and draw as little current as possible from the supply to reduce the power burden in a multi-channel acquisition system. Following the amplification, the neural signals must be serialized with minimum crosstalk and glitches, which facilitates the digitization by a single analog-to-digital converter (ADC) that helps to further reduce the power and area consumption.

## 1.3 Wireless Communication

Once the brain signals are digitized and processed by a digital signal processor (DSP), a control command is issued after decoding each walking intention. While the acquisition and processing units (i.e. the SU and CWU) are connected via a subcutaneous tunneling cable, the robotic exoskeleton relies on a wireless link which present a number of design issues. For instance, wireless communication between the implantable devices and external computers is typically a power-hungry process. In addition, limited enclosure area requires small form factor for all wireless unit's constituent components including the antenna.

To meet the most stringent field conditions (i.e., static magnetic field strength, specific absorption rate, etc.) due to the interactions with the magnetic field of magnetic resonance imaging (MRI) system, the proposed CWU shown in Fig. 1.1 relies on an inductorless TRX with no off-chip component except an antenna. Commercially available MRI-conditional devices use customized structures to enclose antenna to further reduce magnetic interaction and, hence, satisfy the MRI requirements for implantable systems (e.g., Medtronic W1DR01/W1SR01 [16]).

Multiple telemetry methods such as near-field magnetic coupling, conduction through the body, and short-range RF communication exist that establishes the link between the implanted device and external units or actuators. Although a number of IEEE standards have been introduced for such methods, the radios based on these standards still do not satisfy the severe power budget, heat dissipation, low emission power, and small area constraints required for an implantable BCI system. Nevertheless, MedRadio band (401–406 MHz) was dedicated by the Federal Communications Commission (FCC) for implantable and wearable devices, which has been expanded recently by allocating four 6-MHz bands at 413-419 MHz, 426-432 MHz, 438-444 MHz, and 451-457 MHz.

# Chapter 2

# A Glitch-Less Serializer for Multi-Channel Brain Signal Acquisition

## 2.1 Overview

Fig. 2.1 depicts the proposed brain signal acquisition (BSA) module consisting of an electrode array, differential amplifiers (Amps), a serializer and an output buffer [17]. As shown, the neural signals are recorded differentially with respect to each channel electrode and the shared reference electrode. The outputs of amplifier array are then time-multiplexed to better facilitate input-output cable management by reducing the number of wires. The non-overlapping clock generator within the serializer generates $N$-phase clock signals, each with 1/N duty cycle. Non-overlapping clock signals ensure that only one amplifier is connected to the output buffer at a time during the channel switchover. Finally, the serialized output is buffered prior to digitization and further processing by the DSP.

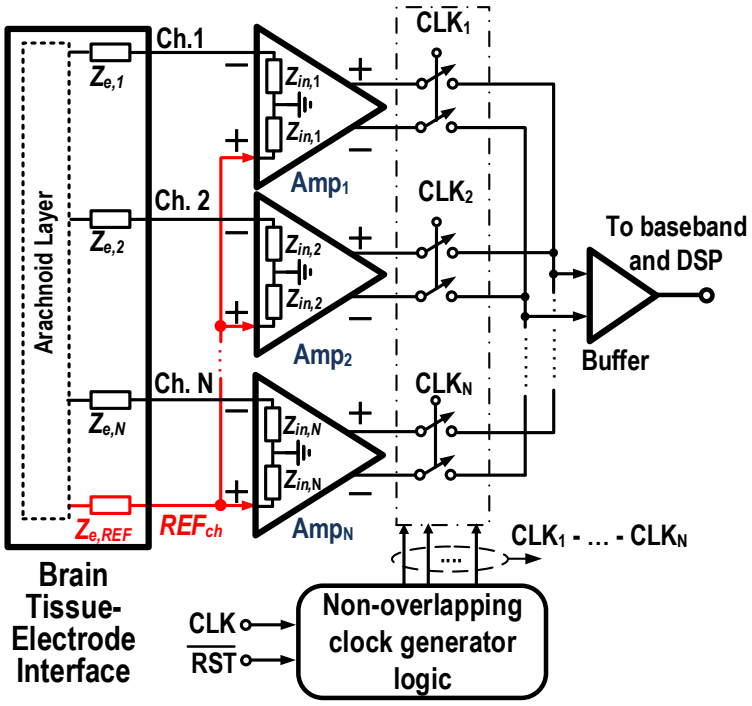



Figure 2.1: Architecture of the proposed multi-channel BSA

The subsequent sections of this chapter present the serializer design in the BSA, followed by the simulation and measurement results from a fabricated prototype.

## 2.2 Serializer Design

### 2.2.1 Topologies

Broadly speaking, data acquisitions rely on either analog or digital serialization of the recorded signals. Shown in Fig. 2.2(a), the BSA architecture based on analog serialization consists of $N$-number of Amps, a $N$:1 multiplexer, an output buffer and an ADC. While this approach allows sharing a single ADC which is advantageous in terms of power and area savings, it is prone to channel corsstalk, glitches and ghosting effect due to analog multiplexing. On the other hand, digital serialization, as depicted in Fig. 2.2(b), provides a robust

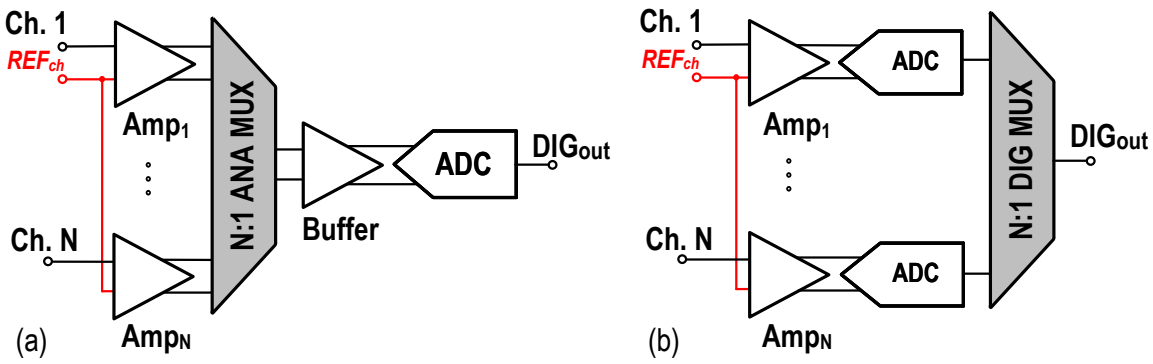



Figure 2.2: Multi-channel BSA architectures based on (a) analog and (b) digital serialization

method for aggregating digitized neural signals but suffers from increased power and area consumption which limits its scalability to smaller channel counts in implantable BCIs.

Analog multiplexing can be achieved in either voltage or current domain. Shown in Fig. 2.3(a), the analog multiplexer consist of four source-followers ($M_1$, $M_{1b}$ ... , $M_4$, $M_{4,b}$) and a switching network ($S_1$, $S_{1b}$ ... , $S_4$, $S_{4,b}$), which performs DC level shifting and buffering of each amplifier's output to the input of ADC, in addition to the serialization [1]. To allow further power saving in the channel buffers and ADC driver, a current-mode multiplexer is introduced in [2]. As depicted in Fig. 2.3(b), the current-mode multiplexed buffer employs a folded-cascode amplifier with complementary inputs to accommodate the wide voltage swing of the amplified signals. Transistors $P_1$ and $N_1$ convert each channel's output voltage signal to current which is then multiplexed at the low-impedance node in the folded-cascode stage by $P_{SW}$ and $N_{SW}$ transistors.

### 2.2.2 Digital Logic

The circuitry for the serializer logic used in BSA is presented in Fig. 2.4. It consists of a 2-bit counter, a 2-to-4 decoder and several logic gates which contrives i) non-overlapping clock signals for time-multiplexing, and ii) a gray-coding scheme for a 2-bit binary counter to eliminate race conditions. The serializer clock signal's duty-cycle produces temporal spacing

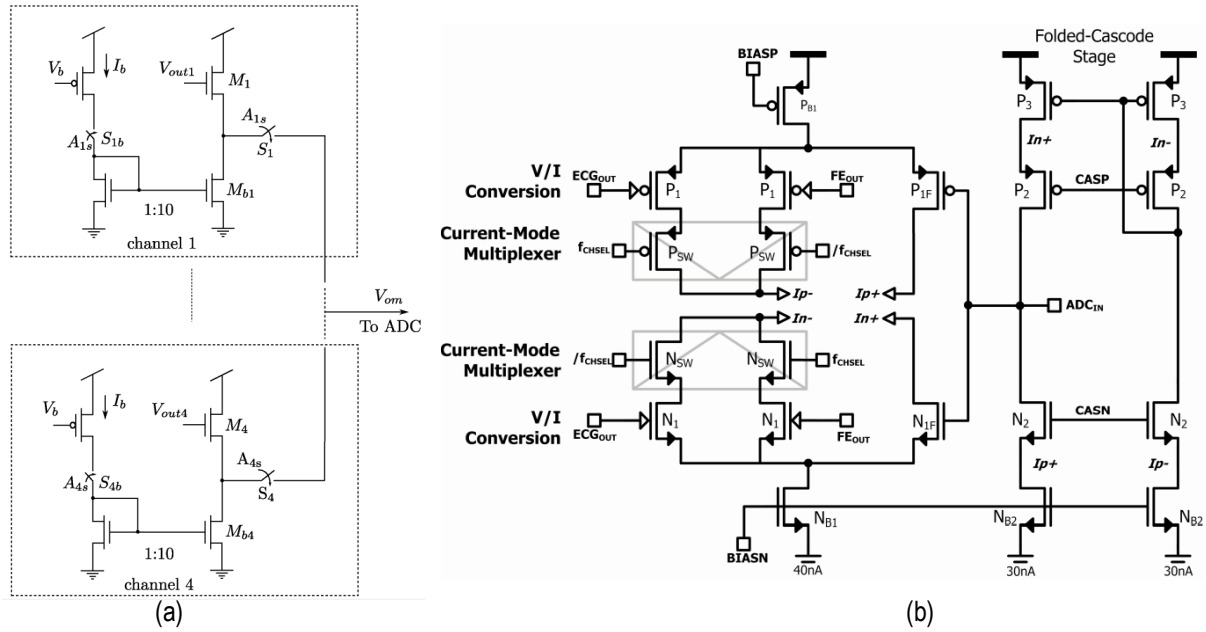



Figure 2.3: Analog multiplexer implemented in (a) voltage [1] and (b) current [2] domain

between clocks applied to the serializer switches (Fig. 2.4). A Gray-code converter (i.e. XOR logic gate) is used to convert binary code to Gray code such that the counter exhibits no race condition, which could otherwise result in sparks in the 2-to-4 decoder in Fig. 2.4.

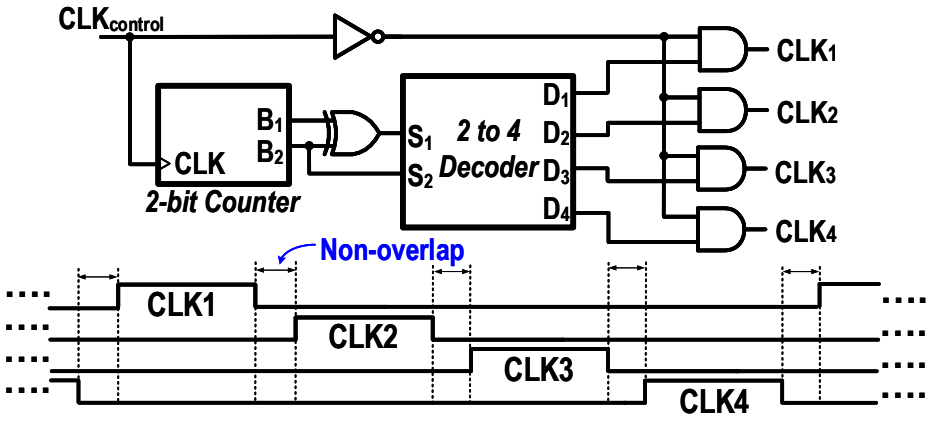



Figure 2.4: Digital logic top-level schematic and output waveforms

### 2.2.3 Analog Switches

Based on the analog multiplexing in voltage domain, a T-network switch, as depicted in Fig. 2.5(a), is used for channel selection in the serializer to provide large input-output isolation. Shown in Fig. 2.5(b), each switch in the T-network consists of a complementary pair of MOS transistors to achieve better on-resistance and minimize the effects of charge-injection and clock-feedthrough.

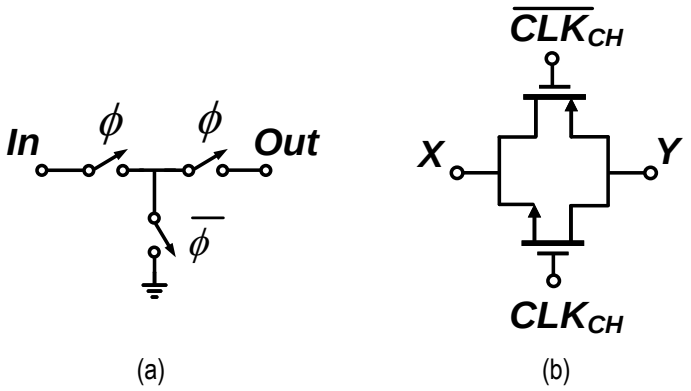



Figure 2.5: T-network switch (a) topology and (b) individual component

## 2.3 Simulations and Measurements

A 4-channel BSA is designed and fabricated in a 180nm CMOS process. It consists of an operational transconductance amplifier (OTA) array, a glitch-less serializer and an instrumentional amplifier (InAmp), as depicted in Fig. 2.6(a). The non-overlapping clock generator includes the digital logic that was discussed earlier. Both $CLK$ and $\overline{RST}$ signals are generated off-chip by the function generator and in case of signal acquisition from channel 0, they are set to ground. As illustrated in Fig. 2.6(b), InAmp comprises of two operational amplifiers (OpAmps) with resistive feedback that provides further amplification of the serialized output before digitization.

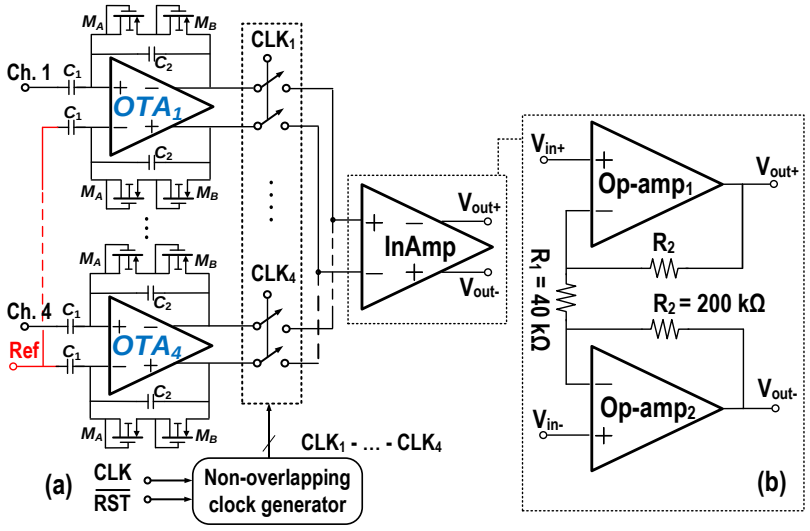



Figure 2.6: 4-channel BSA: (a) top-level diagram (b) InAmp implementation

This BSA prototype operates at 0.6 V supply voltage and occupies 0.352 mm$^2$ of die area (excluding pad ring), as shown in Fig. 2.7.

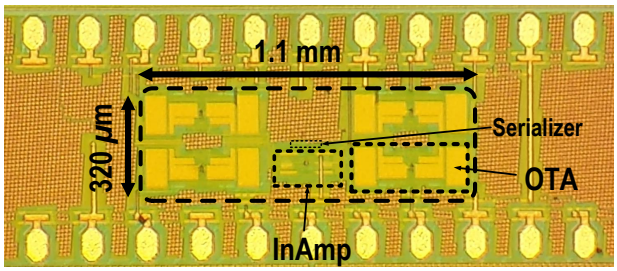



Figure 2.7: BSA die microphotograph

The functionality of serializer is verified by both simulation and measurements. Applying a 20 Hz sine-wave to all the channels, Fig. 2.8 shows the simulated output waveforms from the four channels after de-serialization (250 Hz/channel). Furthermore, a similar setup is reproduced in the measurement, which considers two signal sources with different frequencies: a 20 Hz and a 100 Hz sine-wave applied to channel 0 and 1, respectively while the other input channels are grounded. Fig. 2.9 depicts the measured output waveforms from each channel after de-serialization (1.5 kHz/channel), demonstrating no glitches and negligible crosstalk.

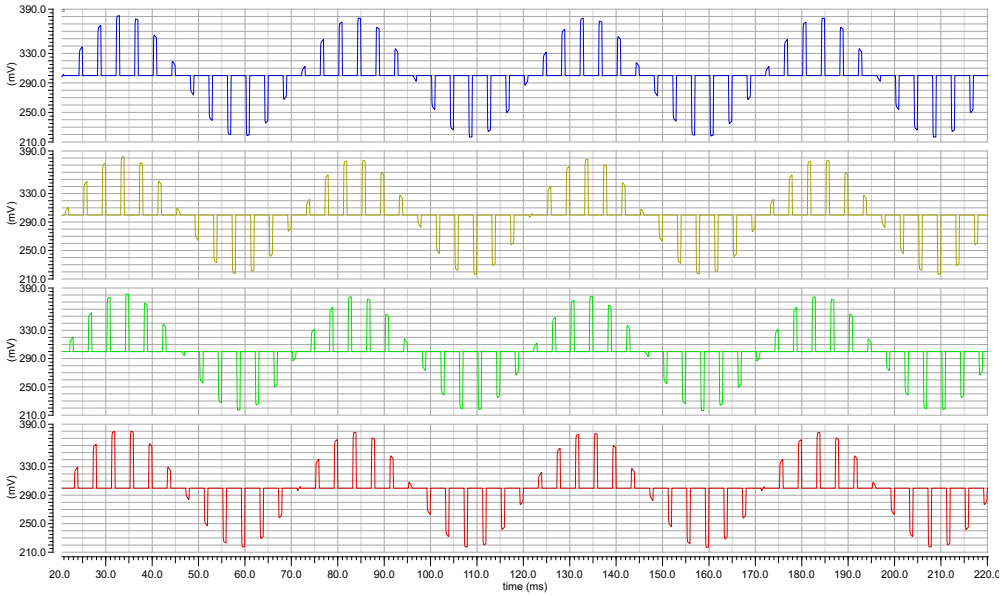



Figure 2.8: Simulated channel output waveforms after de-serialization

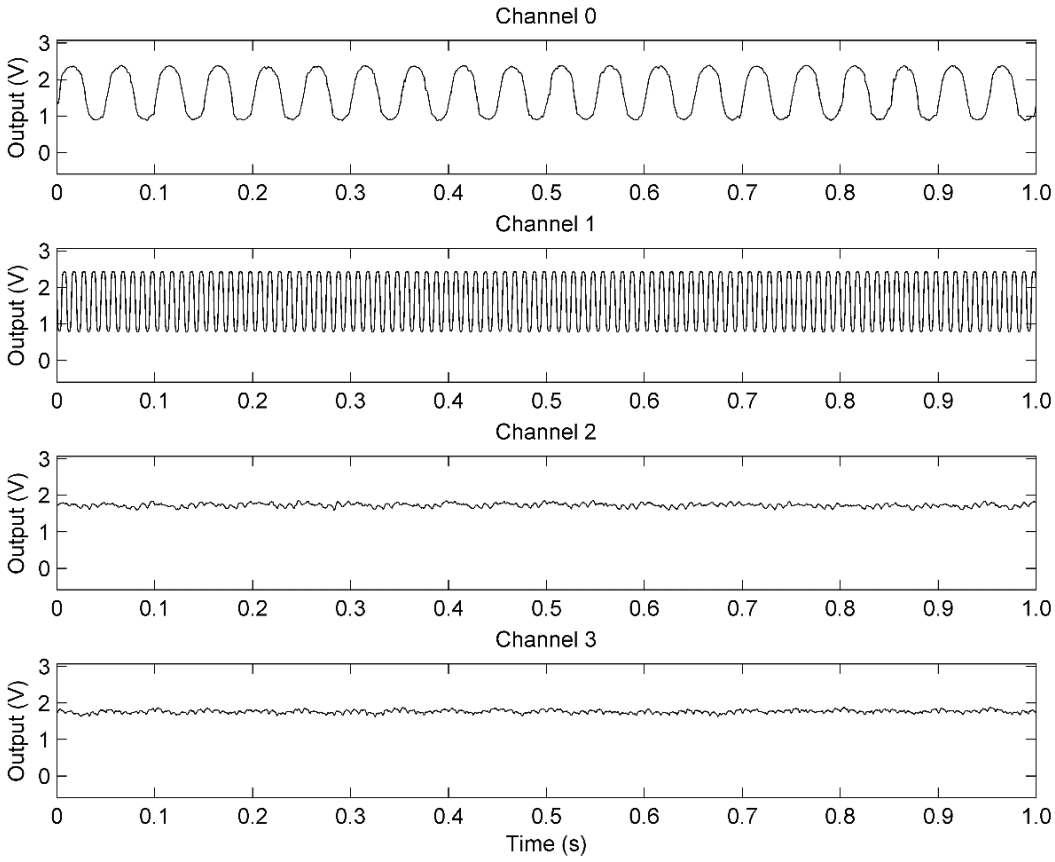



Figure 2.9: Measured crosstalk and glitches after de-serialization

To evaluate the performance under *in vivo* conditions, multiplexed EEG from electrodes AFz, Cz, Pz, and Oz (all referenced to AFz) are acquired while a subject is instructed to alternate between eyes-open and eyes-closed tasks. Shown in Fig. 2.10, the de-serialized EEG signals from electrodes Oz and Pz (2 kHz/channel) exhibit larger amplitudes of the occipital posterior dominant $\alpha$ rhythm during the eyes-closed state, as physiologically expected. These recordings further demonstrate that the serialization of the neural signals is executed reliably.

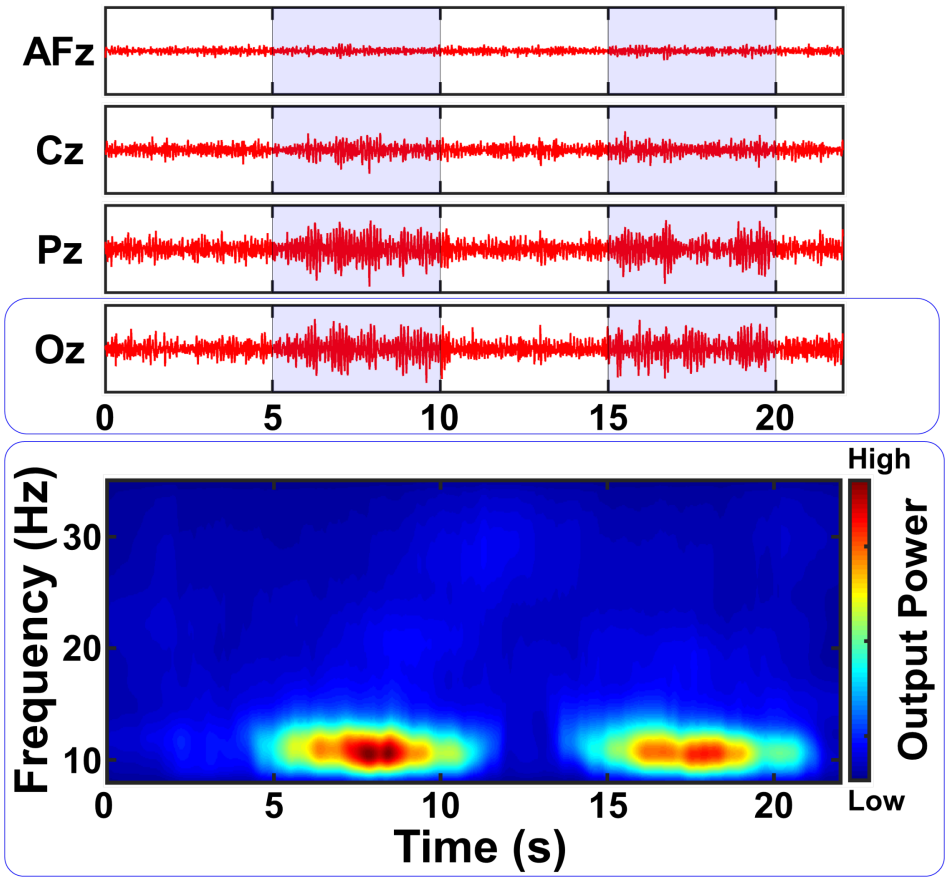



Figure 2.10: De-serialized EEG recordings from an *in vivo* experiment

# Chapter 3

# An Ultra-Low Power MedRadio-Band Oscillator for Implantable BCI

## 3.1 Overview

Fig. 3.1 depicts the proposed inductorless transceiver (TRX) comprising a supply-modulated non-coherent direct-detection receiver (RX) and a direct-modulation on-off keying (OOK) transmitter (TX) [18]. On the RX side, the incoming signal is strobed by a periodically activated noise-canceling low-noise amplifier (LNA) above the Nyquist rate of the baseband (BB) signal representing the BCI control commands. The BB signal is then recovered after passing through an envelope detector (ED) and a dynamic latched comparator, as a decision circuitry. A feedback control circuit turns off the RX amplifiers as soon as the current bit is resolved, effectively duty-cycling the RX. On the TX side, the BB data modulates the free-running digitally controlled oscillator (DCO) incorporating a fast frequency calibration loop, which allows the entire TX to be power-cycled. The OOK modulated signal is amplified by a self-biased, inverter-based power amplifier (PA) prior to transmission by an off-chip antenna.

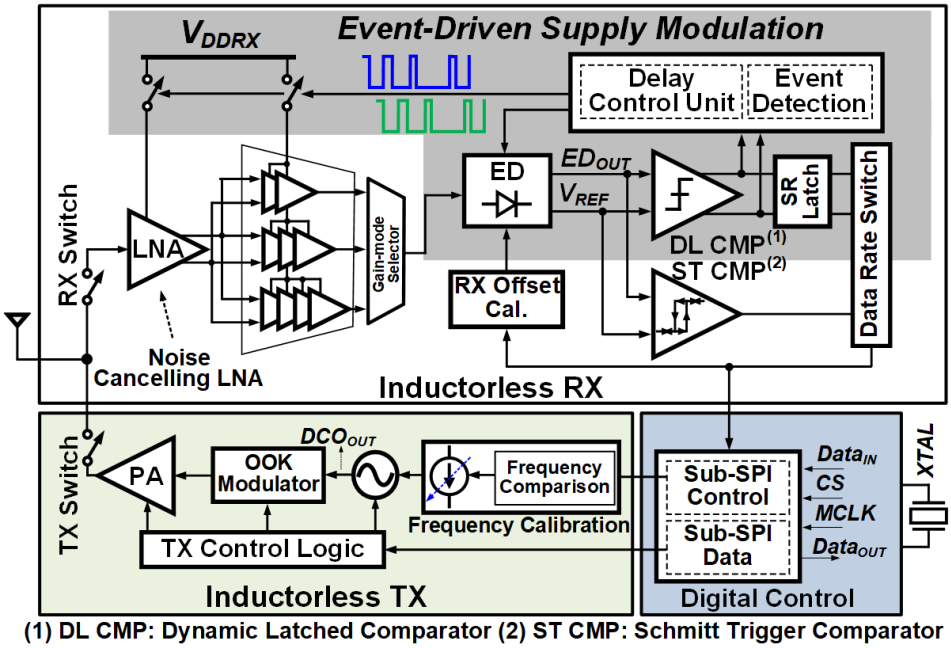



Figure 3.1: Architecture of the proposed low-power OOK TRX

The subsequent sections of this chapter present the oscillator design in the TRX, followed by the simulation and measurement results from a fabricated prototype.

## 3.2 Oscillator Design

### 3.2.1 Topologies

To facilitate the inductorless TX implementation, two main topologies are considered for the oscillator design. Depicted in Fig. 3.2(a), the relaxation oscillator at the top-level consists of an integrator, typically realized by an inverting active RC filter, and a Schmitt trigger. Given that Schmitt trigger exhibits two output states (i.e. high or low), the current flowing through the integrator creates a voltage ramp. Once the integrator's output voltage crosses certain threshold level, it forces the Schmitt trigger to toggle its output state and reverse the current flow. This leads to an opposite voltage ramp at the output of the integrator until the

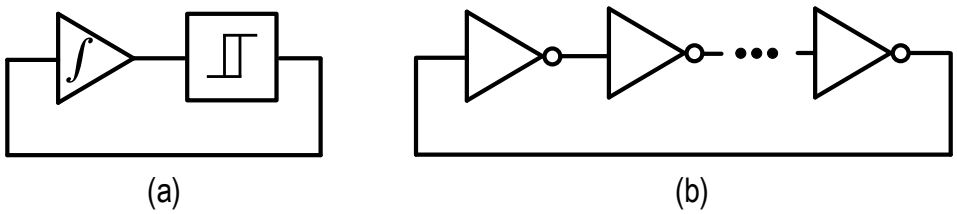



Figure 3.2: Inductorless oscillator topologies: (a) RC relaxation (b) Ring-based

threshold level is reached again. This repetitive cycle gives rise to an oscillatory waveform. On the other hand, ring-based oscillators place an odd number of inverters in cascade and forms a loop by connecting the output of the last stage to the input of the first stage, as shown in Fig. 3.2(b). This ensures that the loop phase is -180° to sustain oscillation and prevent latch-up.

An example of RC relaxation oscillator is depicted in Fig. 3.3(a) which uses pulse self-biasing to reduce power consumption as well as harmonic filtering and resistor feedback to achieve better phase-noise performance [3]. Since conventional relaxation oscillators depend on two current sources to charge and discharge the capacitor, it is possible to employ a differential pair, controlled by the outputs of the oscillator, with a single current source instead to reduce the power consumption, referred to as pulse self-biasing. Similar to LC oscillators, a shunt capacitor is placed in parallel with the current source to suppress the even harmonics and minimize the noise contributions. To speed-up the switching, a local resistor feedback is introduced, which modifies the equivalent resistance during the transitions and further reduces the phase-noise. Meanwhile, a three-stage ring oscillator is shown in Fig. 3.3(b) wherein both the signal and control paths are differential to achieve high common-mode rejection [4]. At high frequencies, ring oscillators are preferred to relaxation oscillators due to equal or better phase noise and the frequency stability that is easily achieved by additional digital calibration circuitry.

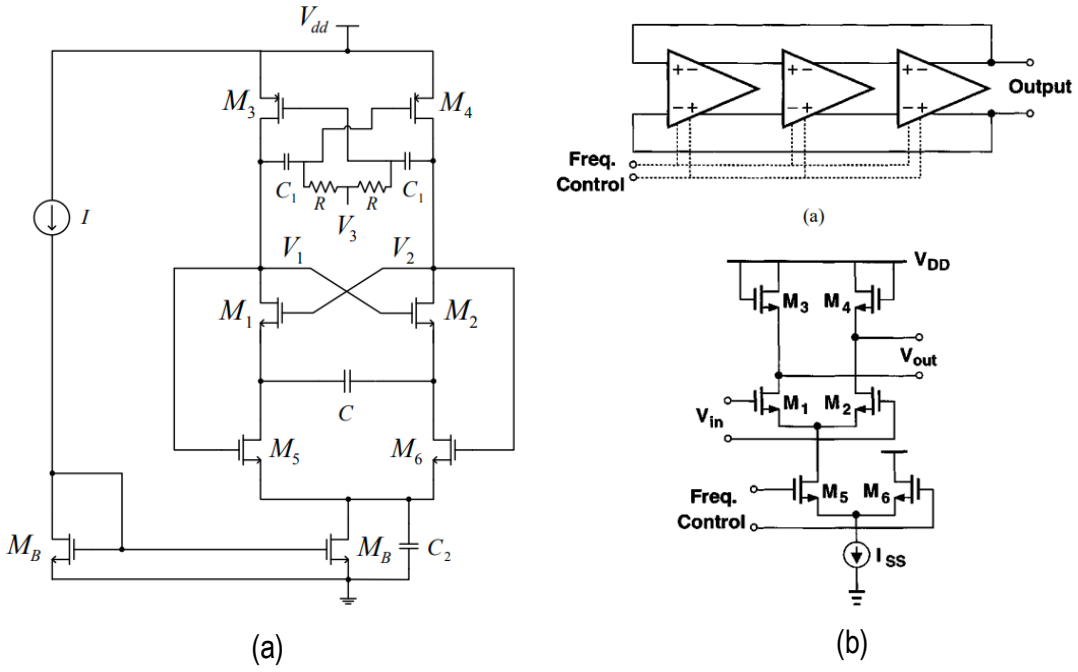



Figure 3.3: Circuit implementations of (a) RC relaxation [3] and (b) Ring-based [4] oscillators

### 3.2.2 Current-Starved Ring Oscillator

Fig. 3.4 depicts the 7-stage current-starved ring oscillator with an additional buffer. Each stage consists of a single-ended inverter which is assumed to have a delay of $\tau$. Thus, the large-signal oscillation frequency ($f_{\text{osc}}$) is readily calculated, as follows:

$$f_{osc} = \frac{1}{2n \times \tau} \text{ , where } n \text{ represents the number of stages} \tag{3.1}$$

As the stage delay decreases in more advanced technology nodes, achieving lower $f_{\text{osc}}$ requires additional number of stages (i.e. $n = 7$). To allow tunability of $f_{\text{osc}}$ in the presence of process, voltage and temperature (PVT) variations, a coarse- and a fine-tuning mechanism is introduced. Coarse-tuning is used to compensate for the process variations in a one-time calibration by employing a 3-bit current digital-to-analog converter (DAC) with a reference current, generated by an off-chip potentiometer. As depicted in Fig. 3.5(a), each coarse-

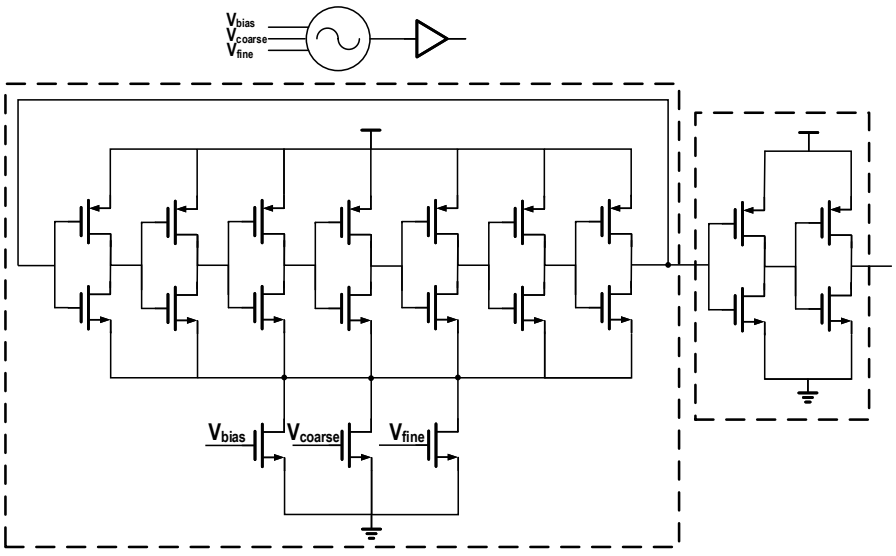



Figure 3.4: Current-starved ring oscillator

tuning bit of the current DAC ($B_{C,2}$,$B_{C,1}$,$B_{C,0}$) is controlled by a serial peripheral interface (SPI). To compensate for the temperature and supply voltage variations, fine-tuning of $f_{osc}$ is achieved by employing a 4-bit current DAC, as shown in Fig. 3.5(b). The control signals ($B_{F,3}$,$B_{F,2}$,$B_{F,1}$,$B_{F,0}$) are generated by the automatic frequency calibration (AFC) block, as will be discussed in the next sub-section.

### 3.2.3 Automatic Frequency Calibration

Within the AFC block, as depicted in Fig. 3.6, a 13-bit counter computes the binary representation of divide-by-two oscillation frequency by counting its cycles over the 32.768-kHz reference clock period from a Pierce XTAL (shared by the RX). The result is compared with the target cycle count $N_{CYC}$, where $N_{CYC} = f_{osc}/(2f_{XTAL})$, and fed to an SAR logic to adjust the oscillator current. The tuning range is $\Delta f = 2^{B}$ LSB, where LSB is the fine-tuning resolution and B is the number of control bits in SAR algorithm (4 bits). The calibration algorithm allocates one clock period for cycle counting, one for comparison, and one for internal reset. Therefore, the total calibration time $T_{cal}$ is derived as $T_{cal} = 3 \times B/\ f_{XTAL}$.

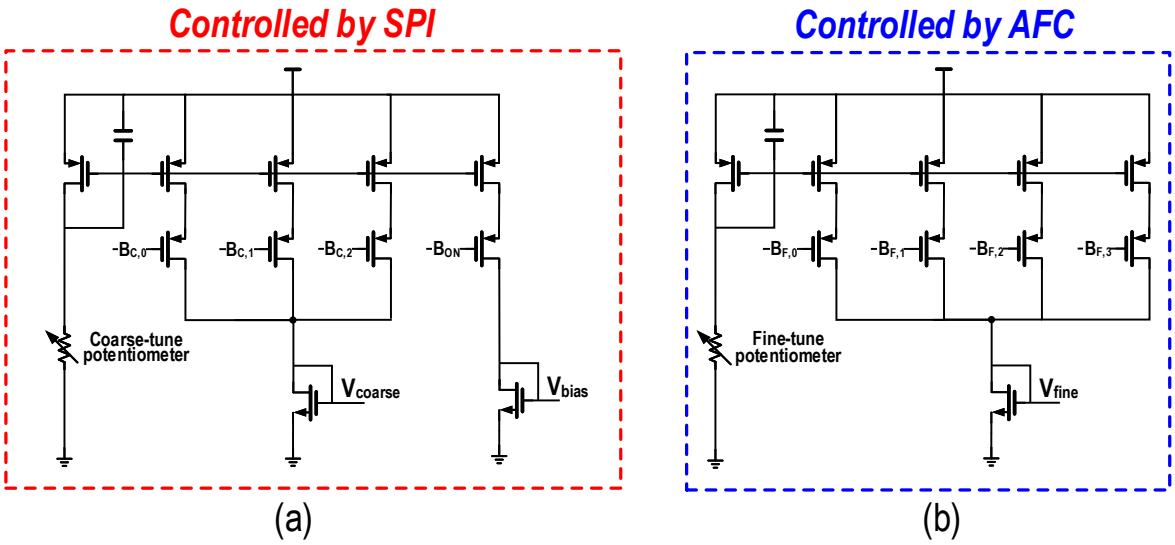



Figure 3.5: Current DACs for (a) coarse-tuning and (b) fine-tuning

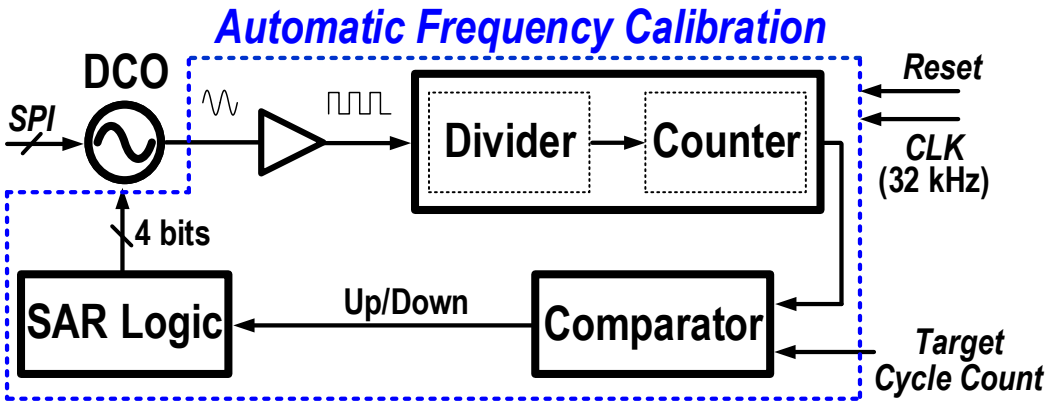



Figure 3.6: AFC block diagram

## 3.3 Simulations and Measurements

Designed and fabricated in a 28nm CMOS technology, the complete TRX prototype occupies $1.5 \times 1.5$ mm$^2$ of die area including pads, as depicted in Fig. 3.7.

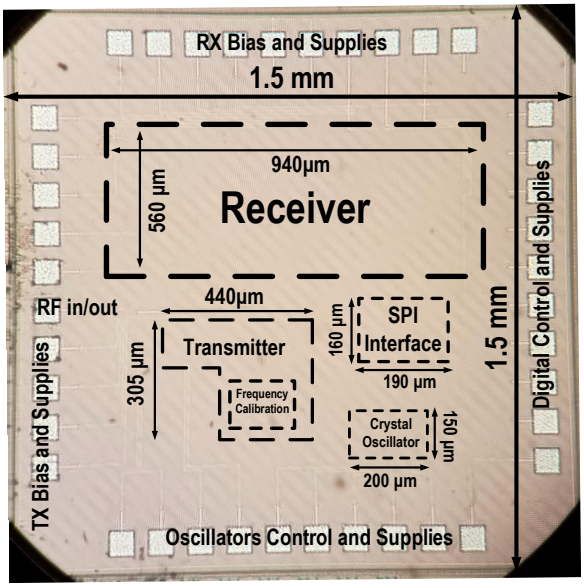
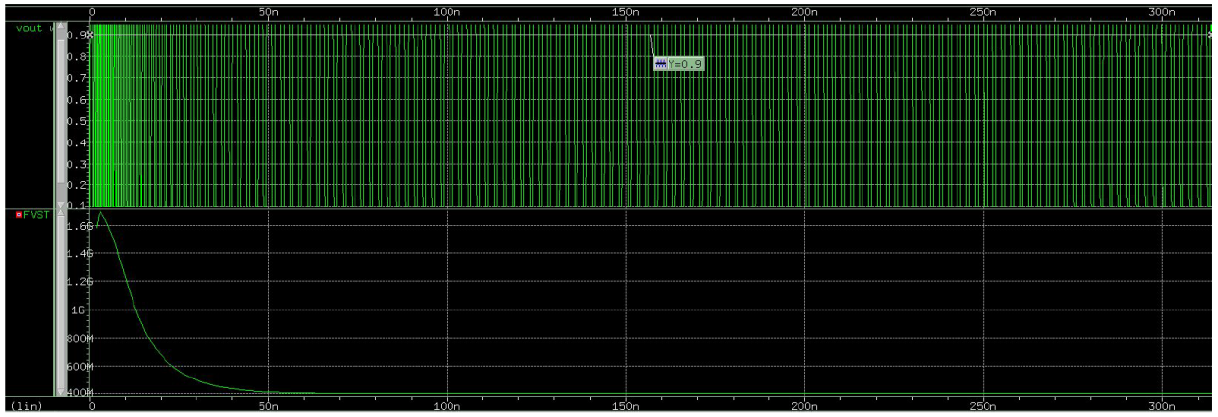


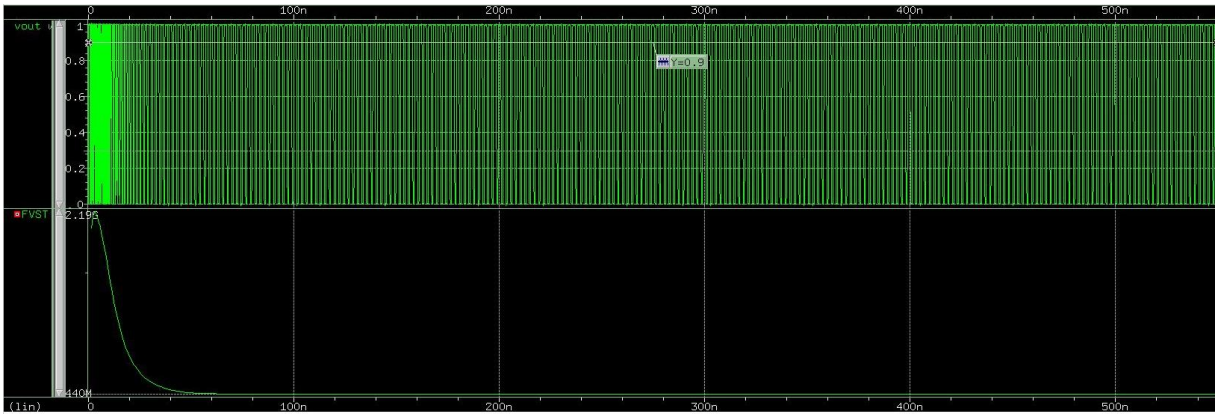

Figure 3.7: TRX die microphotograph

The functionality of ring oscillator and AFC block are verified by both simulation and measurements. The 7-stage current-starved ring oscillator and AFC module operates at 1V supply voltage. The nominal $f_{\text{osc}}$ is set to 403 MHz, to coincide with the center frequency of the lower MedRadio band. The tuning range of ring oscillator is approximately 344 to 440 MHz and can be acquired in <60 nS of settling time, as seen in Fig. 3.8. Coarse- and fine-tuning reference currents are set to 3.2 and 1.8 $\mu$A, respectively. The nominal power consumption of free-running ring oscillator is simulated to be 114.8 $\mu$W.

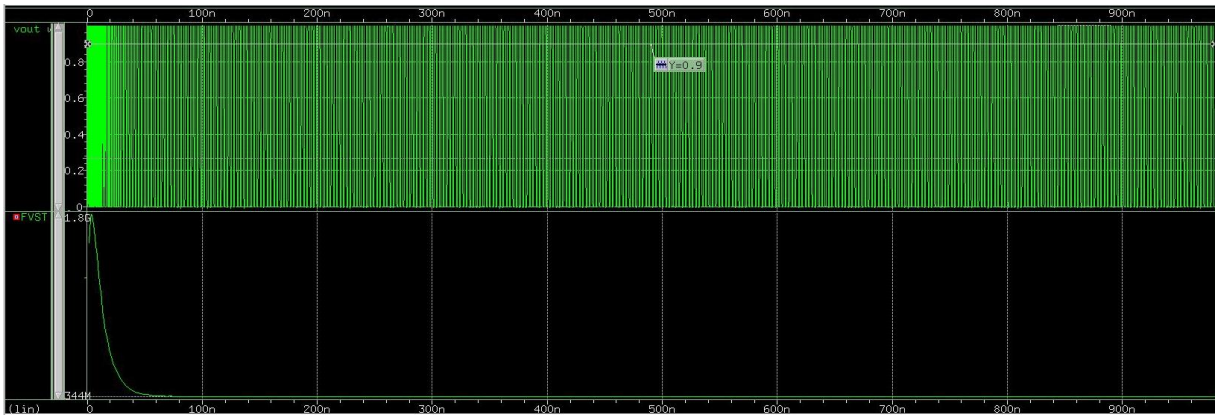
To characterize $f_{\text{osc}}$ across different corners including fast-fast (FF), typical-typical (TT) and slow-slow (SS), a Monte Carlo simulation with 100 number of samples is performed, as shown in Fig. 3.9. The results are summarized in Table 3.1.




(a)




(b)




(c)

Figure 3.8: Simulated settling behavior for (a) default (b) maximum and (c) minimum $f_{\text{osc}}$

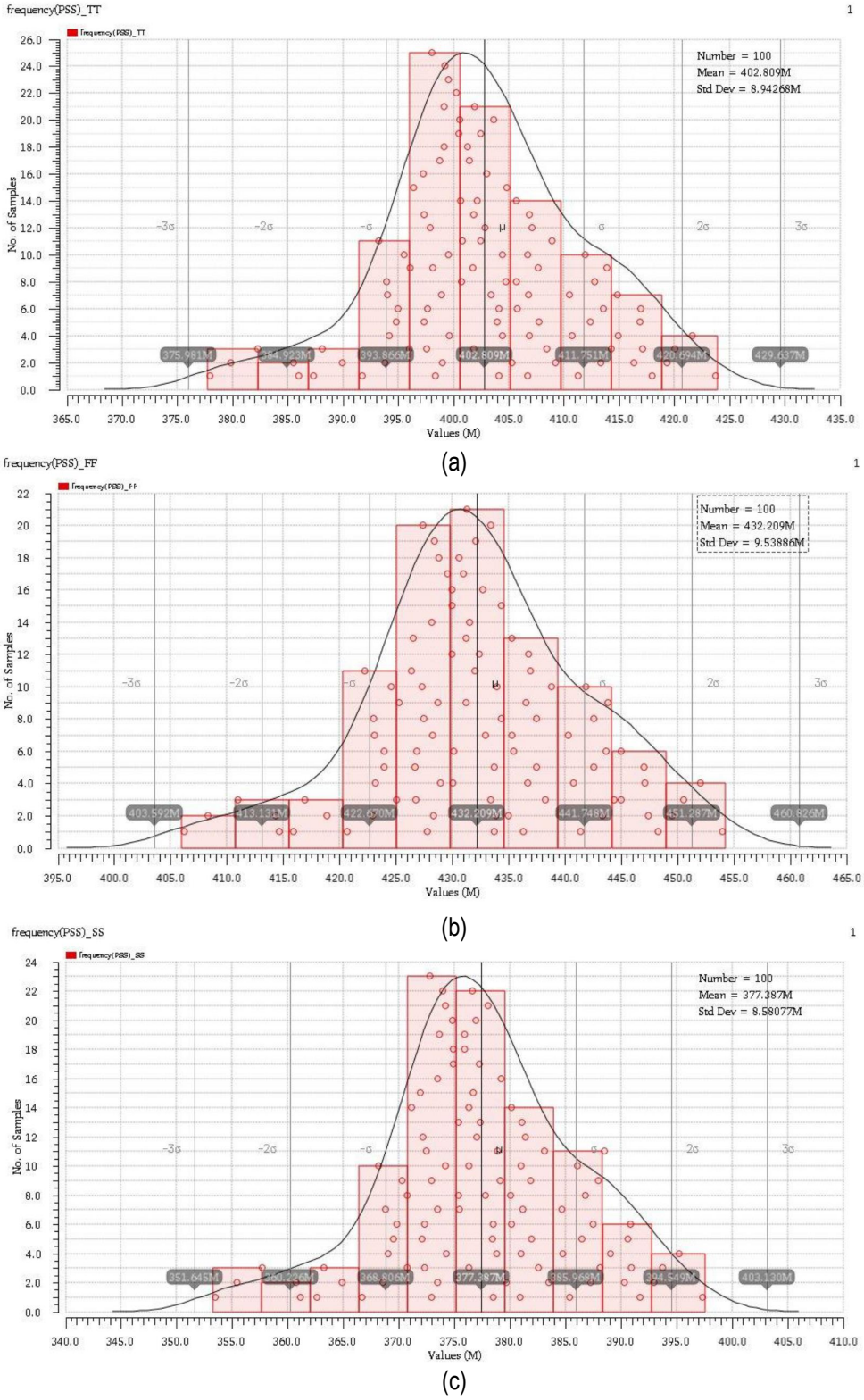



Figure 3.9: Monte-Carlo results of $f_{\text{osc}}$ across (a) FF (b) TT and (c) SS corners

| | FF | TT | SS |
|---|---|---|---|
| Avg. $f_{\text{osc}}$ (MHz) | 432.3 | 402.9 | 377.4 |
| Max. $f_{\text{osc}}$ (MHz) | 454 | 423.7 | 397.3 |
| Min. $f_{\text{osc}}$ (MHz) | 406.2 | 378 | 353.5 |
| Avg. $P_{\text{dis.}}$ ($\mu$W) | 116.5 | 122.5 | 160.8 |

Table 3.1: Summary of oscillator performance based on Monte-Carlo simulations

The ring oscillator single-tone output spectrum measured wirelessly is shown in Fig. 3.10. The fundamental frequency output power is 19.5 dBm. To reduce the sensitivity of the $f_{\text{osc}}$ to supply voltage variations, the AFC is enabled. Fig. 3.11 depicts the measured $f_{\text{osc}}$ versus supply voltage variations before and after calibration. As demonstrated, the AFC can compensate for approximately $\pm 2\%$ of changes in supply voltage.

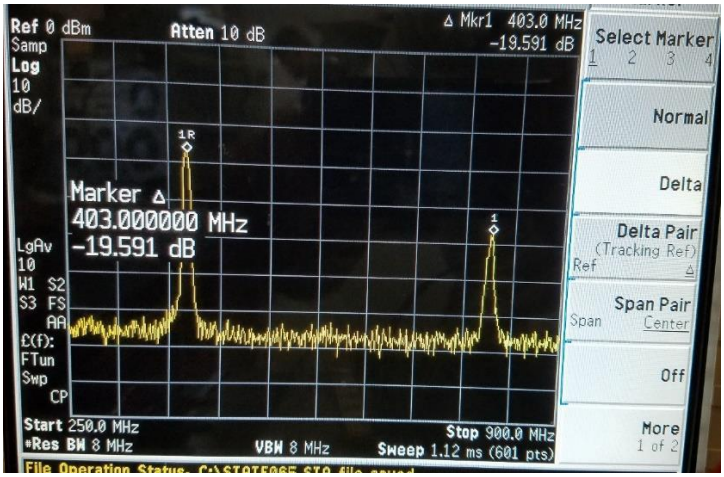



Figure 3.10: Measured output spectrum of $f_{\text{osc}}$

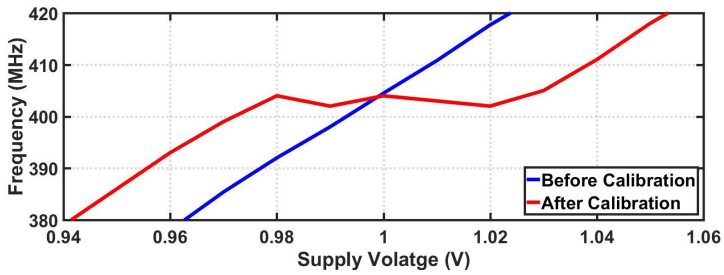



Figure 3.11: Measured $f_{\text{osc}}$ versus supply voltage variations

# Chapter 4

# Conclusion

In this thesis, a brief overview of the proposed fully implantable BCI system to restore walking in SCI patients is presented. The design and implementation of a glitch-less serializer and a MedRadio-band oscillator as part of the BSA and TRX sub-systems are discussed.

To address the limitations of analog serialization in the multi-channel BSA, a non-overlapping clock generator is employed, which uses a gray-code scheme in the binary counter to avoid race conditions. This approach ensures that bit toggling during the channel sequencing does not cause unintended switching which would have introduced glitches in the serializer. Designed and fabricated in a 180nm process, the 4-channel BSA exhibits negligible crosstalk and no glitches, as demonstrated by the electrical and biomedical measurement results.

To satisfy the MRI requirements for implantable systems, TRX is designed without the need for an on-chip or off-chip inductor. Based on this approach, the low-power MedRadio-band (401-406 MHz) TX uses a 7-stage current-starved ring oscillator with a coarse- and fine-tuning mechanism to compensate for PVT variations. Designed and fabricated in a 28nm CMOS process, the DCO operate at a nominal supply voltage of 1V, achieving a frequency tuning range of $\sim$96 MHz with a settling time of $<$60 nS and power dissipation of 114.8 $\mu$W.

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