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A Lightweight Multilevel Power Converter for Electric Aircraft Drivetrain

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Abstract: Next generation hybrid electric aircrafts rely on improvements in electric drivetrains. This work explores the advantages of incorporating high-density, high-efficiency dc-dc converters to enable flexible battery configurations, as well as increased dc bus voltages for reduced cable weight. A dc-dc front-end stage with wide operating range also enables a constant (and optimum) inverter input voltage, irrespective of battery state-of-charge, enabling increased inverter efficiency. Practical challenges such as gate drive power delivery, level shifting, commutation loop and converter start-up are addressed in this work to increase overall performance and reduce weight. Finally, this work demonstrates a high-voltage hardware prototype capable of achieving 99.3% peak efficiency and 28.2 kW/kg specific power density.

I. Introduction

Increased innovation within electric drivetrains is necessary to meet efficiency and weight requirements, enabling the next generation of hybrid, and eventually fully electric aircrafts. To fully enable more-electric aircraft, roadmaps indicate that future power conversion systems need to operate with minimum efficiency and power densities of 98% and 10 kW/kg respectively [1]. Previous work, such as [2], [3] and [4] have achieved these targets through the careful design of inverters, with a high input voltage (800 V-1 kV). Specifically, [2] demonstrates that higher input voltages result in higher operating power for a fixed output voltage, due to decreases in conduction losses. Moreover, work in [5] indicates that a higher dc bus voltage yields lower losses in transmission, increasing the overall power density of the on-board power system. This indicates that a higher dc voltage (800 V - 1 kV) will increase overall system efficiency in hybrid electric aircrafts. However; many current commercial hybrid electric aircrafts have battery voltages ranging from 270 V to 600 V, highlighting the necessity for high efficiency, light-weight dc-dc power conversion [6]. This work is targeted at smaller aircrafts with power levels in the tens to hundreds of kW wherein several batteries, and their associated power management, are to be connected in parallel for modularity. The approaches and techniques presented here are also suitable for larger aircraft, with appropriate scaling of power and voltage.

By inserting a regulation dc-dc boost stage into the standard hybrid electric power train [7], the battery architecture can remain at a lower voltage and vary in configuration while still operating the inverter at its peak dc voltage. Lower battery voltages also simplify the battery pack construction, where isolation and voltage clearances at altitudes can be challenging, Moreover, the wide voltage operating range dc-dc converter can tolerate changes in battery voltage during flight or lifetime allowing for a more robust system. Fig. 1 depicts an example drivetrain architecture with intermediary boost stages that provide a well regulated high voltage dc bus, while allowing for a very large input voltage range.

To take full advantage of this architecture, the bi-directional boost stage must be efficient and light-weight such that once coupled with the inverter the overall system still reaches the targets mentioned above. Hybrid-switched capacitor power converters have been shown to have high efficiency and power density, due to their high active and passive device utilization [8] [9]. In particular, the high energy density of Class II dielectric ceramic capacitors enable dramatic size/weight reductions com-

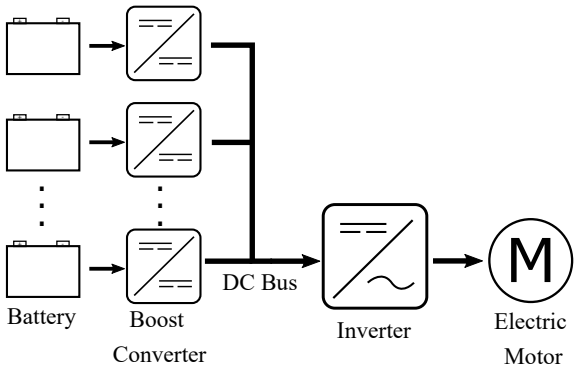

Fig. 1: Electric aircraft system architecture. This work focuses on the design and implementation of the dc-dc boost converter.

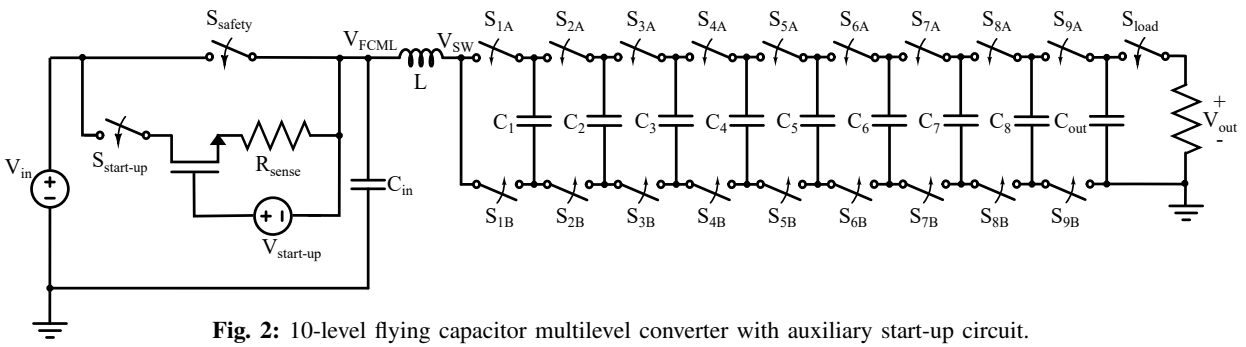

Fig. 2: 10-level flying capacitor multilevel converter with auxiliary start-up circuit.

pared to conventional converters [10], but care must be taken in the capacitor selection and converter design owing to non-linear capacitor losses under large dc bias and ripple operation [11] [12]. The flying capacitor multilevel converter (FCML) topology is of particular interest as it allows for the use of lower voltage switches and smaller inductance making it a suitable choice in applications demanding light-weight designs [13]. This work addresses the practical challenges of designing a light-weight and efficient dc-dc FCML bi-directional boost converter for electric aircraft applications.

The remainder of this paper is organized as follows: Section II provides design details of the gate drive and the commutation loop. Following this, Section III describes the start-up procedure required for practical implementation. Section IV provides experimental validation of the proposed techniques. Finally, Section V concludes the paper.

II. Design Considerations

For the FCML boost converter, the steady-state (ignoring capacitor voltage ripple) drain-source voltage (V_{ds}) is given by $\frac{V_{out}}{N-1}$, where N is the number of levels. For the 10-level design chosen in this work, the 1 kV maximum output voltage yields an average maximum voltage stress of approximately 110 V. Due to the increased performance of gallium nitride (GaN) switches, this work implements EPC2034C GaN devices taking advantage of their low on-resistance and small footprint. Since the EPC2034C parts are rated for 200 V, the devices operate at approximately 60% of their maximum, increasing the system reliability and allowing significant margin for flying capacitor voltage ripple at heavier loads. Fig. 2 shows a schematic diagram of the converter, including start-up circuitry. A key advantage of the FCML converter is its decreased inductor requirements: The PWM signal experienced by the inductor, and that present on V_{SW}, operates at an effective switching frequency that is (N-1) times higher than each device's switching frequency with phase shifted operation producing a frequency multiplication effect [14]. Moreover, rather than being equal to dc bus voltage, the ac amplitude of V_{SW} experiences the same voltage reduction as the switch voltage mentioned above which greatly reduces inductor volt-seconds. As such, a lower Henry inductor may be used to reduce size and weight without incurring excessive inductor current ripple.

A. Gate Drive

Owing to the large number of non-ground-referenced power switches, gate drive power delivery is a challenge in the FCML converter. A number of gate drive power delivery techniques are presented and analyzed in [15], and more recent techniques with improved performance are presented in [16]. A limitation of the cascaded bootstrap technique is the accumulating voltage drops of the bootstrap diodes. In this work, diodes with minimal forward voltage drop were chosen to reduce this effect while local linear regulators provide a stable 5V supply to each gate driver. Nevertheless, at extreme duty ratios the gate drive power supply voltage may fall below the 5 V limit of the devices employed here. To ensure sufficient headroom and reliable operation, the duty cycle range for this work is limited to 0.07-0.93.

B. Flying Capacitor Selection

To maximize specific power density targets for this high-voltage design, careful capacitor sizing, selection, and implementation are all critical design aspects. In an FCML converter, the average voltage across a flying capacitor is determined by $V_{k,fly} = k * \frac{V_{out}}{(N-1)}$, where k is the number of the corresponding level (numbered as shown in Fig. 2 for the boost topology). The dc voltages for each flying capacitor are calculated in Table I. Class II MLCCs (C5750X6S2W225K) were utilized due to their high energy density and low losses [17] [18]. However, the highest density devices are only rated for 450 V, requiring that flying capacitors C_5-C_8 are stacked in series to adhere to component voltage ratings. Additional balancing resistors of 2 MΩ, are added to ensure even voltage division between series stacked capacitors. The corresponding schematic for the capacitor and balancing resistor implementation is shown

Flying Capacitor	Nominal DC Voltage	Capacitor Configuration	Total No. Capacitors	Nominal Capacitance	De-rated Capacitance
C_1	111 V	3 in parallel	3	6.6 μF	3.96 μF
C_2	222 V	3 in parallel	3	6.6 μF	2.64 μF
C_3	333 V	3 in parallel	3	6.6 μF	1.98 μF
C_4	444 V	3 in parallel	3	6.6 μF	1.32 μF
C_5	555 V	2 in series + 5 in parallel	10	5.5 μF	1.65 μF
C_6	666 V	2 in series + 5 in parallel	10	5.5 μF	1.38 μF
C_7	777 V	2 in series + 5 in parallel	10	5.5 μF	1.20 μF
C_8	888 V	2 in series + 5 in parallel	10	5.5 μF	1.10 μF

TABLE I: Flying capacitor design specifications.

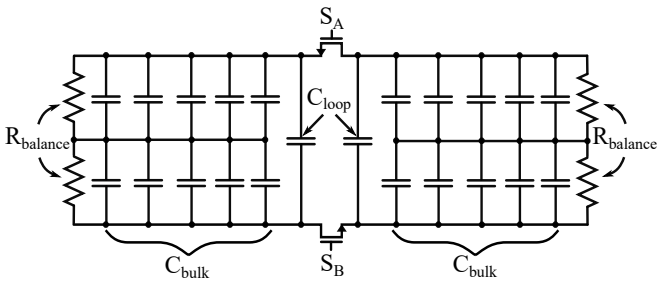

Fig. 3: High voltage switching cell depicting large bulk capacitance and associated biasing resistors in addition to small high-frequency capacitors, C_{loop}, placed close to the switching devices.

in Fig. 3. Since minimizing weight was a priority in this design, the minimum number of capacitors per level was determined such that the full-load peak-to-peak capacitor voltage ripple was ∼5% of the dc bus, with the adjacent switches needing to tolerate the same increase to their voltage rating. The resulting flying capacitor design is summarized in Table I, which also includes the capacitor de-rating due to dc bias at peak output voltage.

C. Commutation Loop Design

In considering board layout, it is necessary to minimize commutation loops to decrease overshoot and increase switch transition speeds [19]. In this work, a vertical switching cell design was implemented to allow for a small commutation loop and increased voltage clearance. With the increased number of necessary capacitors, due to the high power and voltage rating, the commutation loop design becomes more challenging. Therefore dedicated commutation loop decoupling capacitors (C_{loop}) are employed, immediately adjacent to the complementary power switches to reduce the loop area, as shown in Fig. 6. These capacitors use small form factor, low-inductance packages, with correspondingly low capacitance value. The commutation loop is further decreased by implementing a modified version of the electrically thin design as proposed in [18].

III. START-UP

For a practical implementation of the FCML converter, the input voltage cannot be applied instantaneously, since the voltage stress of the switches would exceed their rating as the flying capacitors take a finite amount of time to charge up to their respective voltages [2]. Past solutions to the start-up problem approached this challenge with a high impedance path which allows the input voltage to ramp with an RC time constant [20]. However, in this work's implementation the quiescent current draw while the converter is switching with no load, is approximately 10 mA. Once the capacitors are charged, this small amount of current will result in a non-negligible voltage drop across the high impedance path, and thus the input voltage to the FCML is not equal to the full input voltage of the system. Therefore, when the low impedance path is engaged the FCML sees a large input voltage step. At high input voltages this voltage step is greater than 50 V and therefore can cause imbalance and damage the devices. To solve this problem this work instead implements a constant current source in the auxiliary start-up branch as shown in Fig. 2. Here, a small isolated 5 V supply, $V_{start-up}$, drives a source follower whose current is defined by R_{sense}. The resistor R_{sense} was sized such that the constant current draw is barely higher than the observed quiescent current draw of the converter. This allows the input to reach much closer to its target value, thereby incurring a greatly reduced voltage step in practice. Another advantage of a constant start-up current is increased start-up speed and

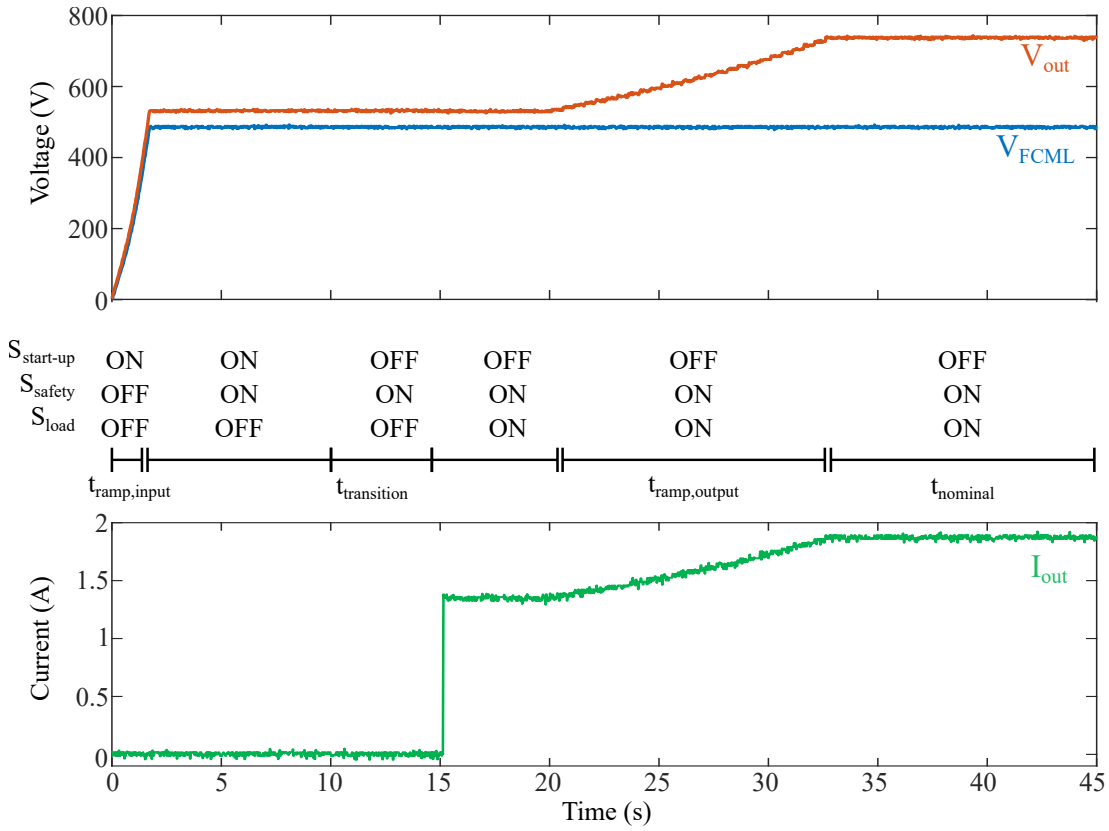

Fig. 4: Experimental waveforms showing start-up procedure with an input voltage of 500 V. The output voltage is controlled to be a constant 750 V at the end of the start-up routine.

lower peak current values, compared to RC time constant approaches.

The auxiliary start-up circuit is implemented using the components in Table II. For this prototype, the input and output switches (labelled $S_{start-up}$, S_{safety} and S_{load} in Fig. 2), are implemented as relays to simplify the gate drive. However, these devices add additional losses and could be implemented with solid state solutions to improve future system performance.

The start-up sequence is detailed below and shown with experimental results in Fig. 4:

- Initial Conditions: $S_{start-up}$, S_{safety} and S_{load} are all open. It is necessary during the input voltage ramp to disconnect the load so there is no in-rush current at the inductor. The converter begins switching at a duty ratio of 0.07, described above to be the minimum operational duty ratio.
- $t_{ramp,input}$: $S_{start-up}$ closes and the input voltage ramps linearly, as controlled by the aforementioned constant current source. The flying capacitors charge during this time, which can be seen in Fig. 5.
- $t_{transition}$: Once the flying capacitors are charged to their expected voltages, the low impedance input path is engaged by closing S_{safety}. After a short delay, to ensure the relay has closed, the start-up circuit is disengaged, by opening $S_{start-up}$. Finally, the load is connected by closing S_{load}. When the

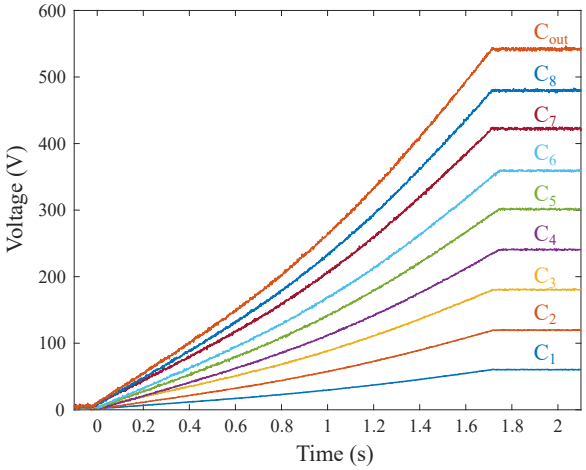

Fig. 5: Flying capacitor voltages during start-up ramp, $t_{ramp,input}$. Measured at 500 V input.

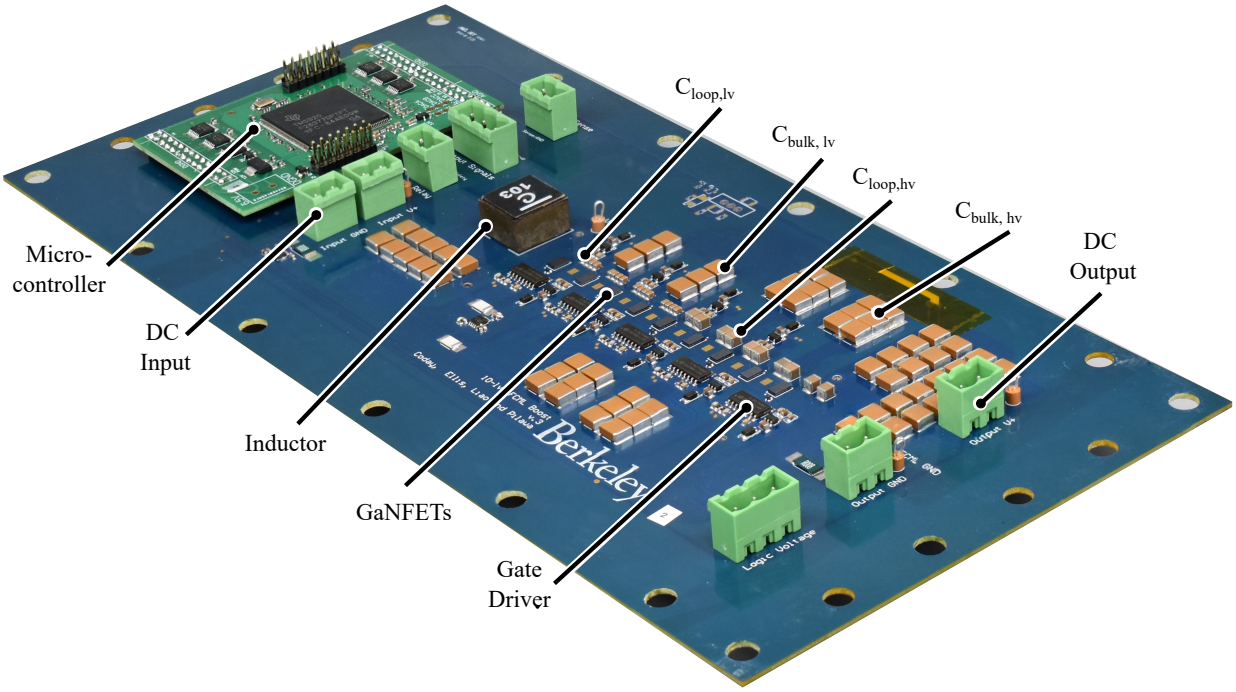

Fig. 6: Top view of the hardware prototype.

load is connected there is a corresponding current step, as seen in Fig. 4.

- $t_{ramp,output}$: As the initial duty ratio was fixed during the input voltage ramp, the closed loop control must be engaged to ramp the output voltage to the set value (750 V in the example shown in Fig. 4).
- $t_{nominal}$: Once the output voltage is set to the desired value, the converter enters nominal operation with full closed loop voltage control engaged.

Component	Part Number	Parameters
Switches	EPC 2034C	200 V
$C_{loop,LV}$	TDK C0G	47 nF, 450 V
$C_{loop,HV}$	KEMET C0G	22 nF, 1 kV
C_{bulk}	TDK X6S	2.2 μF, 450 V
Inductor	Coilcraft XAL1513	10μH
Gate Driver	Si8275	Dual-sided
LDO	LP2985IM5	5 V Output
$S_{start-up}$	G7L-2A-X-L	20 A, 1 kV

TABLE II: Component list for 10-level FCML boost design.

IV. Experimental Prototype and Measurements

The proposed concept was validated with a hardware prototype, as shown in the annotated photograph of Fig. 6. The component selection is detailed in Table II.

As can be observed from the measured switch-node voltage (V_{SW}) of Fig. 7, the flying capacitor voltages are well balanced, indicated by the even amplitude of the pulse-train. The measured inductor current of Fig. 7 also indicates well balanced behavior that is below saturation.

The converter performance is shown in Fig. 8, where the efficiency was measured up to 2.5 kW with 300 V input and 600 V output. Efficiency measurements were taken with a Keysight PA2201A Power Analyzer. The converter reached peak efficiency at 1.6 kW and 99.3% efficiency, including gate drive losses.

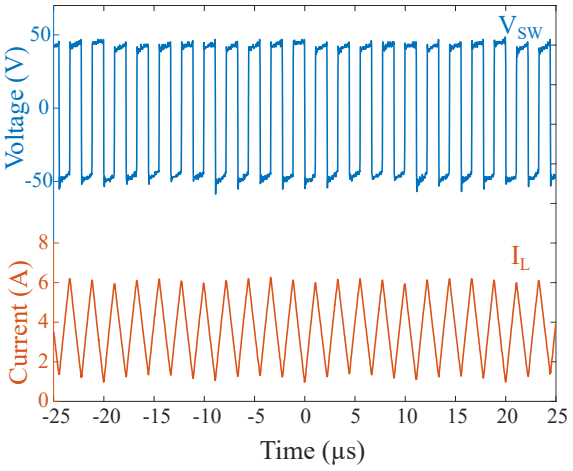

Fig. 7: Operating waveforms, measured at 400 V input, 800 V output. The switch node measurement is ac coupled.

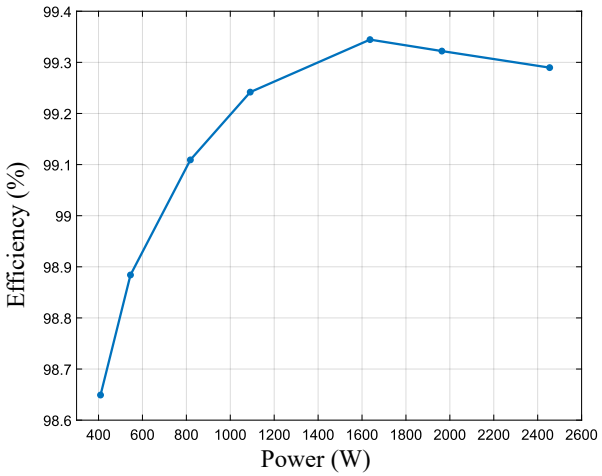

Fig. 8: Measured efficiency of 10-level FCML with fixed 300 V input and 600 V output.

Description	Value
Input Voltage	100 V - 600 V
Output Voltage	600 V - 1 kV
f_{SW}	50 kHz
Effective frequency	450 kHz
Peak Efficiency	99.3 %
Peak Output Power	2.5 kW
Specific Power Density	28.2 kW/kg
Volumetric Power Density	16.6 W/cm^3 (247 W/in^3)

TABLE III: Performance summary.

Using a FLIR thermal camera, a peak board temperature of 67 °C was recorded at 2.5 kW.

V. Conclusion

This work has presented a 10-level FCML converter capable of achieving efficiencies over 99% through implementation of; a cascaded bootstrap technique for gate drive, optimized device selection and a low commutation loop layout. Moreover, with an auxiliary start-up circuit, the converter is shown to safely start-up at high input voltages. With a power stage measured specific power density of 28.2 kW/kg, this hardware demonstration is indicative of significant future improvements to the performance of electric drivetrains in next generation hybrid electric aircraft.

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