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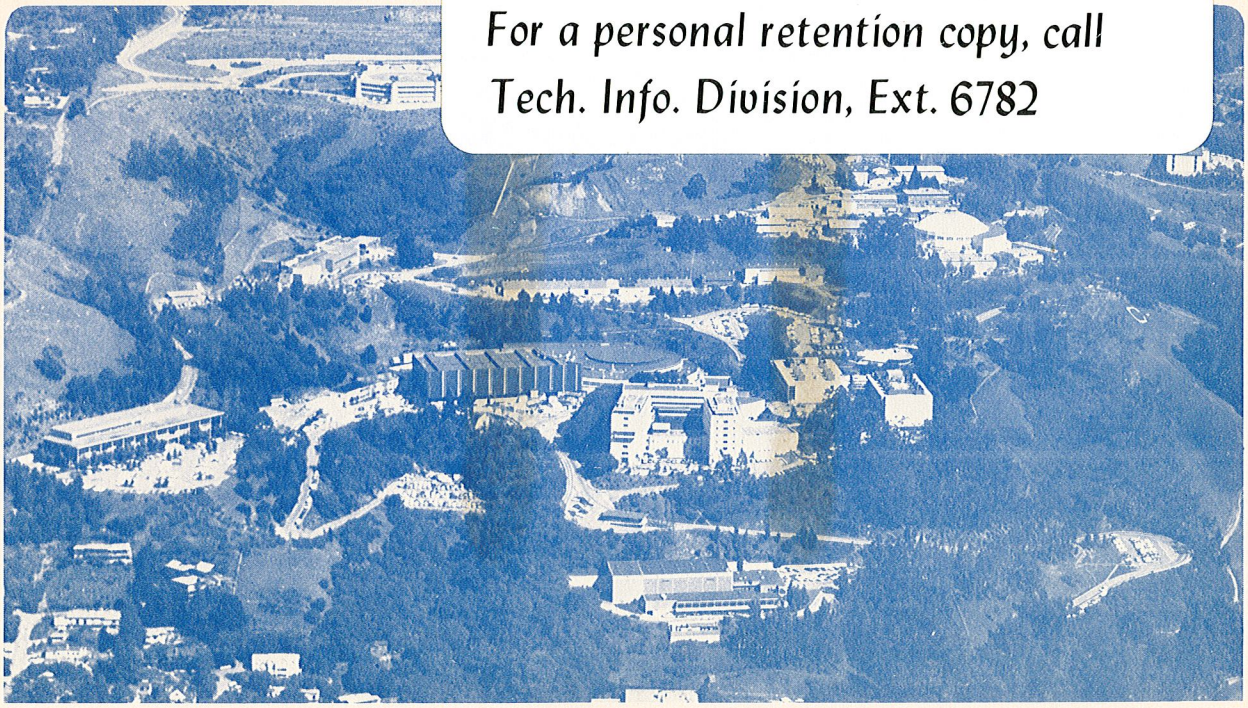

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USE OF CCDs IN THE TIME PROJECTION CHAMBER

LBL-13184

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Abstract

The Time Projection Chamber produces 3-dimensional information about the multiple tracks of reaction products produced by e^+e^- collisions at the center of the chamber. Two dimensions (r,ϕ) result from processing signals from proportional wires and induction pads (a total of 17,000 signals) mounted at the end planes. The third (axial) dimension is obtained by measuring the drift time of ionization from the particle tracks to the end planes. To achieve this, all wire and pad signals (suitably shaped to about 500 ns width) are stored in Charge Coupled Devices (CCDs) which, at any moment, hold 45.5 μs of signal history clocked in at a sampling rate of 10 MHz. About 40 μs after a master trigger, the history is frozen by stopping the clocking action, and a slow clock mode (20 kHz) is initiated to read out the stored samples which are then digitized (9 bits) and processed by an on-line computer. A total of 17,000 channels x 455 samples (each digitized to 9 bit accuracy) is stored in the CCDs (i.e., about 70M bits) for each event. This paper describes the pulse shaping philosophy, the design of the CCD units, the drivers and the testing procedures.

Introduction

The input to the CCD from the Time Projection Chamber[1] (TPC) amplifier is a psuedo-Gaussian pulse with approximately 250 ns peaking time. These signals appear in bursts ranging from 1 to as many as 20 pulses in 15 μs (the drift time of the chamber). Hence, a short amplifier shaping time must be used to achieve the required pulse pair resolution. The fact that the arrival of input charge from a track may spread over a large fraction of the shaping time results in ballistic deficiencies that make the signal amplitude a poor representation of the input charge. Therefore, CCD representation of the signal must allow for reconstruction of the input signal area. It must also allow for the determination of timing information.

The operation of the TPC is predicated on the use of a Charge Coupled Device for each signal channel which samples the analog input at fixed intervals and stores a sampled version of the signal in its cells. The sampled image shifts along the CCD as it is clocked. After 455 clock pulses, the initial sample appears at the output. Data is clocked in at a sample rate of 10 MHz (45.5 μs of analog history) while, for read out, the clock frequency is changed to 20 kHz and the output appears at 50 μs per sample. During the 50 μs periods the data is digitized, zero suppressed, and transferred to buffer memories. In the early phases of the development program various CCD's were tested to determine their capabilities for this system. The Fairchid 321A* units were selected on the basis of these tests.

Pulse Sampling

Sampling theory shows that a bandwidth limited signal sampled by delta functions with a frequency greater than two times the bandwidth can be reconstructed in the time domain by using sinc functions. For the TPC psuedo-Gaussian pulse the minimum sampling frequency would be about 6 MHz.

A computer model was used to evaluate the sampling and later reconstruction. The model sampled the amplifier pulse at a sample frequency and then used the samples to calculate the area and timing (centroid of the sample). The effect of varying the phase of the clock on the area and timing determinations was evaluated. The results are plotted in Fig. 1. as a function of the ratio of sample period to signal rise time (defined as 5% of the amplitude to the peak). The error bars in Fig. 1 show the uncertainty due to phase variations and the line following the envelope is used to guide. On the basis of these results the frequency chosen for the TPC was 10 MHz. Due to the effect of threshold (zero suppression) in the digitizers, detailed elsewhere[2], somewhat larger errors occur in real operation.

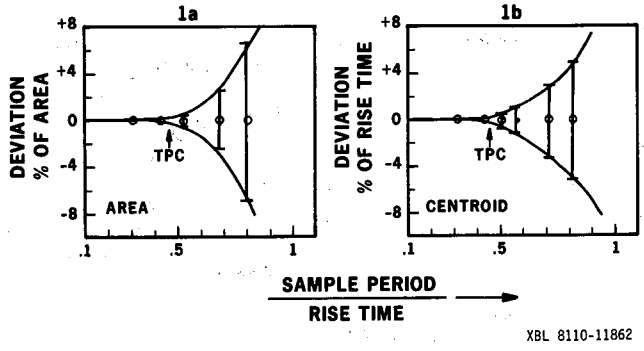


Fig. 1. Deviations of pulse area and timing after reconstruction of the CCD output as a function of sample period divided by pulse risetime.

Charge Coupled Devices

Charge Coupled Devices are relatively new and may not be familiar to all. A reasonable representation of the 321A is shown in Fig. 2. Below the gate structure is a diagram showing the electron potential wells existing during operation. The input pulse (V_{in}) is applied to a reverse biased diode that sets the potential of a large source of electrons (dashed area under the diode). The sample gate (ϕ_S) is then raised to 14V, and charge now flows to the right and accumulates under the reference gate (V_{REF}). The number of electrons stored under the reference gate is approximately determined by the difference in potetial between the input and reference gate, and by the capacitance of the oxide layer under the gate. The sample clock is then turned off trapping the electrons in the well under the reference gate.

While the sample clock is off, the transport gate (ϕ_t) is turned on. The trapped electrons then flow by diffusion into the dotted well under the first transport gate. The stair steps are the result of barrier implants and give the CCD its directional characteristics The transport clock is then turned off, and a new sample is initiated by the sample clock. While that is taking place the charge under the first transport clock flows to the well under the first DC transport gate (V_2). After the completion of the second sampling, the transport clock is turned on. The first sample is moved under the second transport gate; and the second sample is moved under the first transport gate. The device continues to sample and transport the charge along the structure preserving the identity of the individual samples. A reversed biased diode follows the last CCD cell. The potential well under the diode is determined by a reset transistor (Q_1). When the transport clock is turned off, charge is stored on the capacitance of the output diode and output transistor. A voltage approximately proportional to the input sample is thus detected at the gate of Q_2. When ϕ_{out} is on, this voltage will appear at the output of the device (V_{out}).

During the transfer of electrons from cell to cell some electrons are lost resulting in the ratio of output to input electrons being less than one (transfer efficiency of the device). For the 321A the overall efficiency, from input to output, is ≈0.96 at 10 MHz and ≈0.92 at 20 MHz clocking rates. These numbers were obtained with a "fat zero". (The fat zero corresponds to the device operating with about 5% of the maximum number of electrons in each cell. This minimizes trapping of electrons and places the signal in a more linear portion of the transfer function.) Figure 3 is typical of the input-output voltage transfer function. Unfortunately there is no simple way to linearize the curve with external components. The nonlinearity which arises in the input and output circuits of the CCD is compensated for by the computer for each individual channel.

As previously mentioned the CCD's are normally run at 10 MHz for data acquisition and then changed to 20 kHz for read out. During the readout period two undesirable effects are detected. One is dark current, the other will be called "glitches".

The dark current is due to thermally generated hole-electron pairs in the channel of the CCD. Because of the high frequency in the acquisition mode, the leakage current is effectively swept out. However, in readout, each succeeding bucket read out spends one more slow clock period in the device. This results in the output voltage having a ramp structure superimposed on the signal image. For the 321A/SL92102 the maximum slope is 0.05% per millisecond, or 0.5% of full scale in the normal complete readout time of the TPC at room temperature. The TPC specifications require a maximum slope of 0.2% of full scale. To achieve the desired slope the ambient temperature of the CCD's was reduced to about 12°C. Reducing the power consumption on the CCD board to a low value is essential in order for the cooling system to maintain the low temperature.

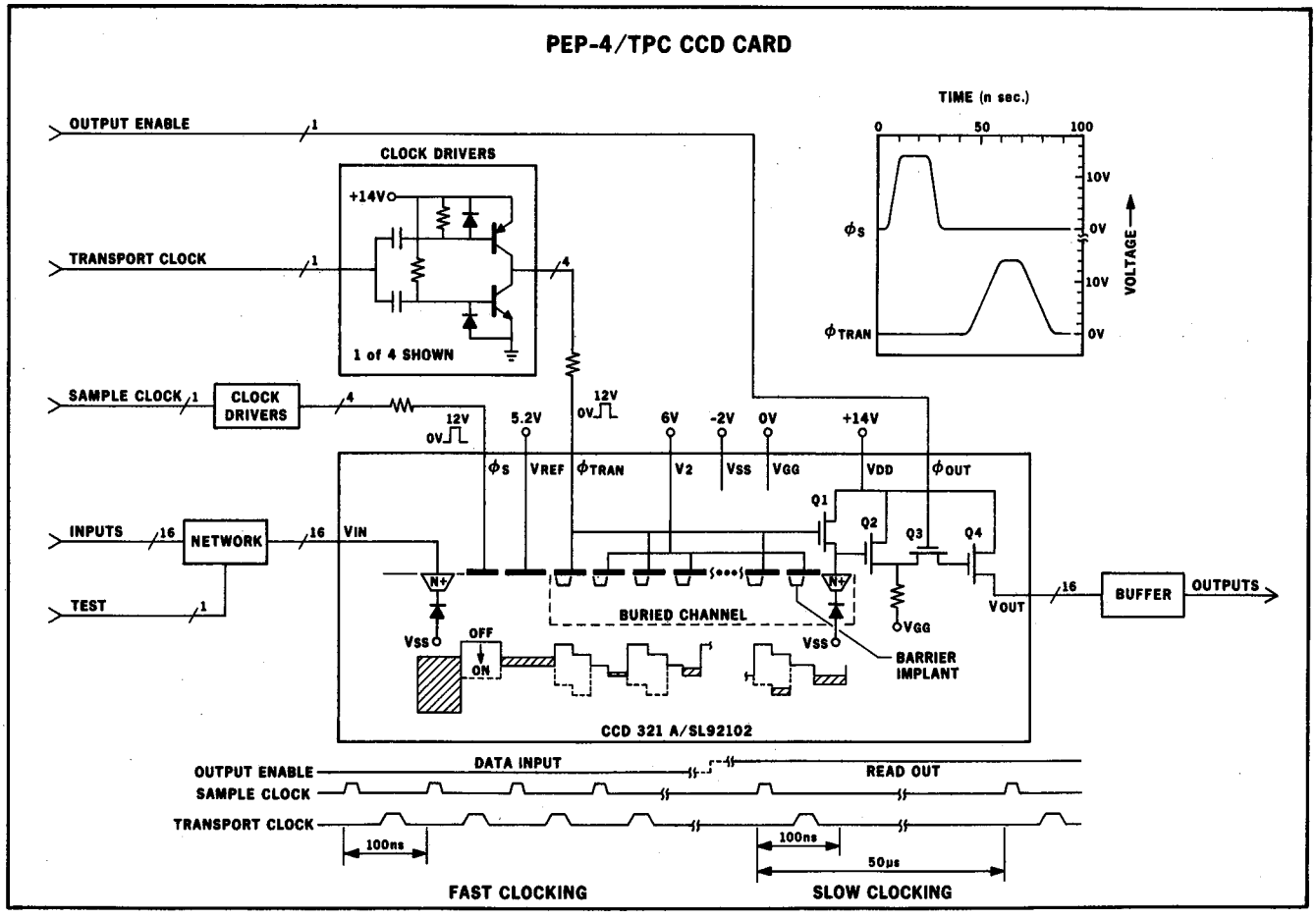


Fig. 2. Block diagram of the TPC CCD driver card.

Glitches are defined for this purpose to be transient deviations from the straight line of the output voltage ramp of more than one part in 500 of the dynamic range. Two identifiable classes of glitches have been observed. The first, though seldom seen, is from a local area of the CCD with high leakage current. This shows up as a step in the slow output ramp. The second type is a few buckets that deviate from the base line and are typically located at specific locations in the CCD.

Physically the CCD is divided into a few long rows of identical cells joined at alternate ends by a few trapezoidal cells to make the CCD continuous. There are seven corners of trapezoidal cells in the 321A structure. The glitches usually appear at locations corresponding to these corners and again, appear to be of two types. The first is associated with the difference in transfer efficiency for the fast and slow clocks. With a fat zero, some cells will have more or less electrons because of variations from the average transfer efficiency. When the clocks are changed to slow, the transfer efficiency tends to become ≈1.0 for all cells and the excess or deficiency of charge shows up as a glitch at the output. In the design of the CCD boards the clock waveform edges are made the same independent of frequency to minimize this effect. This, plus high transfer efficiency has reduced this problem to a negligible amount for the TPC. The second type of glitch is associated with charge injection (forward bias of the channel) into the cells when the clock frequency is changed. The latter two effects can usually be isolated from each other by running the device with and without a fat zero. The nature of the charge injection, usually at the corners, has not been determined. The defective devices are rejected.

CCD Driver Card

The CCD driver card shown in Fig. 2 has eight clock drivers to handle 16 channels of CCD's. Four of the drivers are for the sample clock. The other four are for the transport clock. Hence, two dual CCD chips or four channels are driven by each driver. As mentioned earlier the CCD must be operated at low temperature to reduce dark current. This places a severe constraint on the total power dissipation on a board.

The AC power associated with charging and discharging the clock gate capacitance of a CCD is $P=fCV^2$ (≈120 mW at 10 MHz with C equal to 60 pF and a clock amplitude of 14V). Additional power dissipated on the board should be minimized. This led to the selection of a drive circuit that dissipates no power in the rest state. The push-pull configuration is shown in Fig. 2. In the rest state one transistor is biased lightly on and the other off. A TTL input is applied to the driver. It is differentiated by the capacitor to supply the necessary charge to place the transistor in the appropriate state to charge or discharge the load capacitance by by 14V.

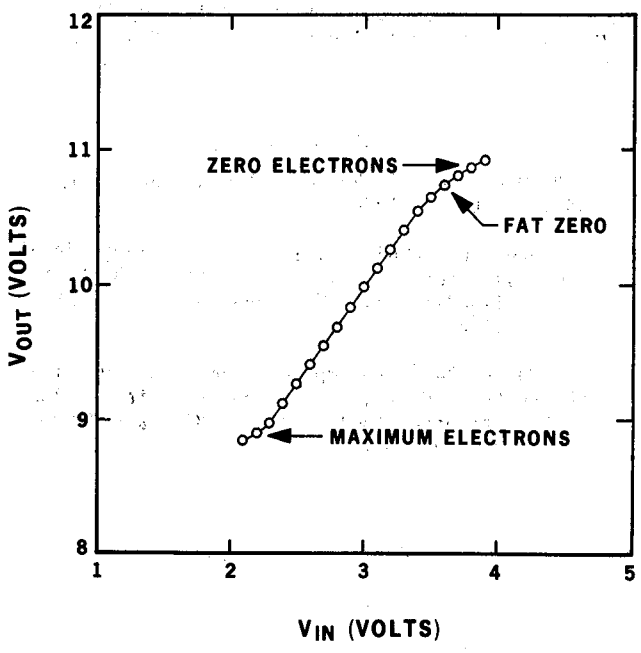
The charge to drive the transistors on the leading and trailing edge of the TTL input is derived as $\Delta Q \approx I_C/2\pi f_T$ (base charge) + 14 C_{OB} (Miller capacitance) + $14C_L/\beta_F$ (load charging). The collector current (I_C) is selected to obtain the required rise and fall times of the clocks (5–15 ns.)

Charge injection in the CCD can take place if the clocks go negative with respect to V_{SS}. Therefore, it is necessary to generate the clocks with no undershoot. This was accomplished by adding a series resistor to the clock lines that critically damps the LC circuit composed of the clock line inductance and device capacitance. Included in Fig. 1 are the clock waveforms as presented to the CCD's. Using these drivers and associated circuits the power dissipation per channel is ~390 mW at 10 MHz.

The output source-follower (Q_4) of the CCD is disabled during fast clocking so that it will not consume energy charging and discharging stray capacitance. It is enabled during the slow clocking mode (timing diagram portion of Fig. 2). The on time of the clocks is the same during the slow and fast mode to minimize changes in transfer efficiency. The buffer at the output compensates for the DC output level of 9 V ± 2 V (4 V input) and normalizes the gain (CCD gain ≈0.9).

Testing of Devices and Boards

The CCD's are first batched for placement on boards of 8 devices (16 channels) per board by the device tester. This automatic tester[3] first determines that the devices meet LBL's specifications for transfer efficiency, dark current, dynamic range, noise, and output offset voltage for two channels on one chip (<300 mV) with the same input. The input-output transfer function is then determined with a reference gate of 5.2 V (V_{REF}). Figure 3 shows a typical transfer function. Linearity is checked and a point corresponding to ≈5% of the dynamic range is located.



CCD TRANSFER FUNCTION

XBL 8110-11845

Fig. 3. Input/output transfer function of a 321A CCD.

This point is used for batching. Batching is used to minimize the number of potentiometers on the CCD board. There are two adjustments per board; one for input bias, the other for output offset. The input bias points typically fall in three bins (3.9, 4.0 or 4.1V). For a given input voltage there is a

spread of the CCD output voltage of 4 V. The devices are batched in 40 bins each of 100 mV. After loading the batched devices on a board, an input bias and coarse output level adjustment is made.

An automatic board tester then scans the boards and determines if some channels need fine tuning. Usually a few trim resistors, mounted on stand-offs, are changed. The computer then directs the operator to adjust the average buffer output level to 300 mV and performs a transfer efficiency test. Boards are then installed in the TPC system. Devices and boards have been retested over long periods of time (≈ six months). No changes exceeeding our measurement error of 1% have been detected.

Conclusion

The operation of CCD's, which is a key to the TPC concept, has been achieved and has met the required specifications of dark current, cross talk, transfer efficiency and noise (glitches) of one part in 500.

Acknowledgemensts

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*Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy.

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