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Wideband Reconfigurable Blocker Tolerant Receiver for Cognitive Radio Applications

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Wideband Reconfigurable Blocker Tolerant Receiver for Cognitive Radio Applications

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical Engineering

by

Qaiser Nehal

2018

ABSTRACT OF THE DISSERTATION

Wideband Reconfigurable Blocker Tolerant
Receiver for Cognitive Radio Applications

by

Qaiser Nehal
Doctor of Philosophy in Electrical Engineering
University of California, Los Angeles, 2018
Professor Asad A. Abidi, Chair

Cognitive radios (CRs) use “white spaces” in spectrum for communication. This requires front-end circuits that are highly linear when the white space is adjacent to a strong blocker. For example, in the TV spectrum (54 MHz-862 MHz) broadcast transmissions are the blockers.

This work describes the design of a wideband blocker tolerant receiver. First EKV based MOSFET model is used to analyze RF transconductor distortion. Expressions for its IIP3 and P_{1dB} are also given. Derivative superposition based linearization scheme for the RF transconductor is also explained.

Second mixer switch nonlinearity is analyzed using EKV. Simple expressions for receiver IIP3 and P_{1dB} are given that provide design insights for linearity optimization. Low phase noise LO design is also described to lower receiver noise figure in the presence of large blockers.

Finally, transimpedance amplifier (TIA) large-signal operation is studied using EKV. It is shown that source follower inverter-based TIA transconductor results in higher receiver P_{1dB}.

A prototype receiver based on these ideas was designed in 16nm FinFET CMOS. Measured results show that receiver can operate from 100 MHz to 6 GHz and can tolerate up to +12 dBm blockers. Furthermore, its noise figure is only 8.9 dB in the presence of +10 dBm

blocker located at 80 MHz offset.

The dissertation of Qaiser Nehal is approved.

Subramanian Srikantes Iyer

Danijela Cabric

Sudhakar Pamarti

Asad A. Abidi, Committee Chair

University of California, Los Angeles

2018

To my parents...

for their unending love and unwavering support

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At the end I would like to thank my parents for their support and sacrifices they have made over the years to turn my dreams in to reality. I would not be where I am today without their love and encouragement.

VITA

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CHAPTER 1

Introduction

The idea of Cognitive Radios (CR) was first proposed in [1]. Cognitive radios can be used to alleviate spectral scarcity issue by using "white spaces" in the frequency spectrum for communication. This requires front-end circuits for CR to be tunable over a wide frequency range. They must also be highly reconfigurable to operate under varying operating conditions while at the same time have high linearity to tolerate strong interferers [2].

1.1 Cognitive Radio receiver performance metrics

This section looks at CR receiver sensitivity and linearity requirements based on examples from the literature and existing standards related to CRs.

1.1.1 Receiver Sensitivity and Bandwidth

IEEE 802.22 standard [3] regulates the use of cognitive radios in the TV spectrum (54MHz to 862 MHz) for wireless regional area networks. This standard assumes coverage areas as far as 100 km and is therefore a good candidate to study sensitivity specification for cognitive radios.

Receiver sensitivity P_{Rx} is given as

$$P_{Rx} = -174\, dBm/Hz \,+\, NF_{Rx} \,+\, 10logB \,+\, SNR_{min}\,, \tag{1.1}$$

where NF_{Rx} is receiver noise figure (assumed to be about 6 dB for customer premise equipment (CPE)), B is the signal bandwidth (6MHz in the TV spectrum), and SNR_{min} is the minimum acceptable signal-to-noise ratio at the receiver output. According to the standard, for the case of QPSK modulation (rate: (1/2) at BER=2×10^{-4}) in multipath channel, the required SNR_{min} is 8.1 dB. This leads to P_{Rx} of about -92.1 dBm.

Therefore cognitive radios meant for operation in the TV spectrum should have sensitivity of about -92 dBm.

1.1.2 Blocker Tolerance

Cognitive radios operating in the TV spectrum will share the spectrum with other broadcast transmitters. Examples of these transmitters are VHF radios (used by police nd emergency services), FM broadcast and TV broadcast etc. Table 1.1 (from [2]) provides power levels of different types of blockers operating in the TV spectrum.

Table 1.1: Table from [2], blockers in TV spectrum

	f_c **[MHz]**	P_B **[dBm]**
VHF Radios	70	25
TETRA	400	14
FM Broadcast	90	-2
TV Broadcast	400	-15
GSM Basestation	900	-29
GSM Terminal	900	-3.5
WLAN	2400	-12

Table 1.1 shows that cognitive radios should be able to withstand very large blockers in the TV spectrum (up to several tens of dBm). However for carrier frequency $f_c \geq 1000MHz$, the blocker level is around 0 dBm.

1.1.3 Intermodulation Distortion

So far only a single strong blocker case has been considered. In practice, there may be several blockers present together, and they can interfere with the wanted signal through intermodulation distortion. Intermodulation distortion in the receiver is characterized by its input-referred intercept point. Lets calculate the intercept point required for a cognitive receiver that supports IEEE 802.22 standard. This will give an idea about the linearity requirement for front-end circuits intended for CR applications.

According to the IEEE 802.22 standard, receiver sensitivity can degrade by 1 dB in the presence of interferers. Therefore,

$$P_{IM}\,[mW] \;=\; 10^{(-91.1/10)}\,[mW] \;-\; 10^{(-92.1/10)}\,[mW]\,, \tag{1.2}$$

where P_{IM} represents the power (in mW) of the intermodulation term. From (1.2) P_{IM} is about -98 dBm. The receiver second-order intercept point can be found using

$$IIP2\,[dBm] \;\geq 2P_B\,[dBm] \;-\, P_{IM}\,[dBm]\,, \tag{1.3}$$

where P_B represents the interferer power in dBm. In the IEEE standard 802.22, $P_B = -8\,dBm$, and hence the required receiver IIP2 is about +82 dBm.

Similarly, the receiver third-order intercept point can be found using

$$IIP3\,[dBm] \;\geq \frac{3P_B}{2}\,[dBm] \;-\, \frac{P_{IM}}{2}\,[dBm]\,, \tag{1.4}$$

which leads to the required receiver IIP3 of +37 dBm for interferer level $P_B = -8\,dBm$. Similar values for receiver intercept points have been calculated in [4]. Clearly these IIP2 and IIP3 requirements for receiver are very stringent, and only a handful of receivers have been shown to reach this level of linearity performance in modern CMOS processes [5, 6, 7].

1.2 Baseline Receiver Architecture

The last section provided sensitivity and linearity targets for cognitive radio front-end circuits. This section gives a brief introduction about the baseline receiver architecture used to achieve those targets.

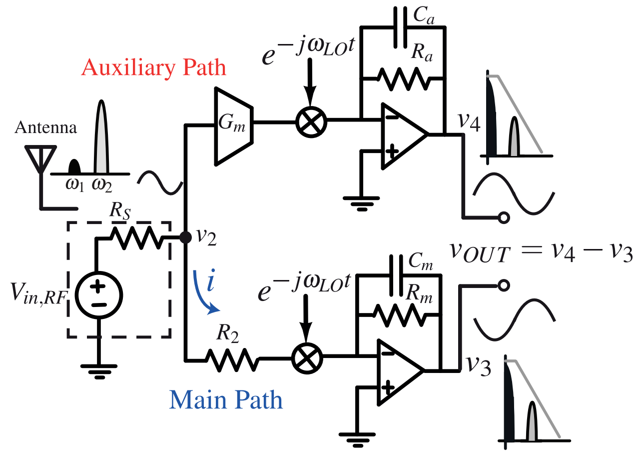


Figure 1.1: Baseline Receiver architecture.

Fig. 1.1 shows the block diagram representation of the receiver architecture from [8]. It consists of two separate downconversion paths: main path that provides 50Ω impedance match to the antenna, and auxiliary path that is used to sense node voltage v_2. An RF transconductor G_m converts v_2 to current. Notice that both these paths do not provide any voltage gain at RF to avoid compression from blockers. Passive mixers are used in both paths to downconvert RF current directly to baseband. In the baseband, trans-impedance amplifiers (TIAs) convert the current to voltage and also provide filtering for the unwanted signals. The final output v_{OUT} is the difference of the outputs v_4 and v_3.

To understand the fundamental operation of the network, mixers in Fig. 1.1 can be ignored giving rise to the linear time invariant (LTI) version of this receiver in Fig. 1.2. Receiver gain is

$$\frac{v_{OUT}}{V_{in,RF}} = \frac{G_m R_a R_2 + R_m}{R_s + R_2} \,. \tag{1.5}$$

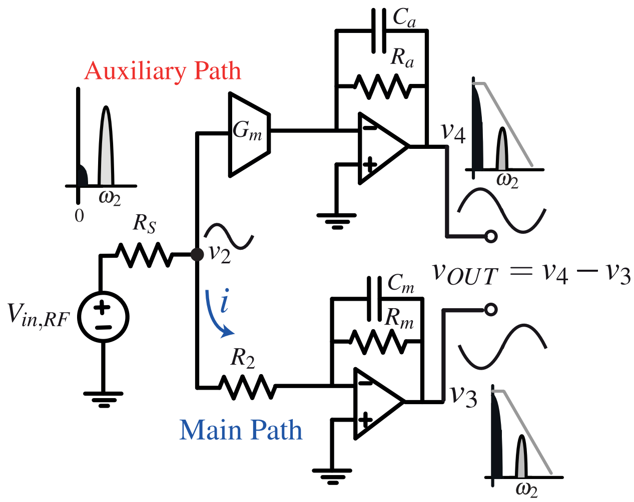


Figure 1.2: Simplified Receiver architecture.

1.2.1 Noise Cancellation Property

It has been shown in [8, 9] that the network of Fig. 1.1 can cancel the noise of R_2 (the 50Ω matching resistor), and that eventually leads to a receiver with very low noise figure. This is important because cognitive radios require low receiver sensitivity. To understand this better, let's model the noise of R_2 as an independent voltage source $v_{n,R2}$ in series with the resistor (see Fig. 1.3). The transfer function from $v_{n,R2}$ to the final output v_{OUT} is

$$\frac{v_{OUT}}{v_{n,R2}} = \frac{G_m R_a R_2 - R_m}{R_s + R_2} \ . \tag{1.6}$$

From (1.6), if $G_m R_a R_2 = R_m$, then $\frac{v_{OUT}}{v_{n,R2}} = 0$, and hence R_2 does not contribute to receiver noise figure and this helps to improve its sensitivity.

1.2.2 Receiver Linearity

The linearity of the baseline receiver from [8] is not sufficient to satisfy blocker tolerance and intermodulation specifications for cognitive radio operation. Therefore analysis of different nonlinearity mechanisms in the baseline receiver is a big part of this work and later chapters in this dissertation describe in detail methods to improve receiver linearity.

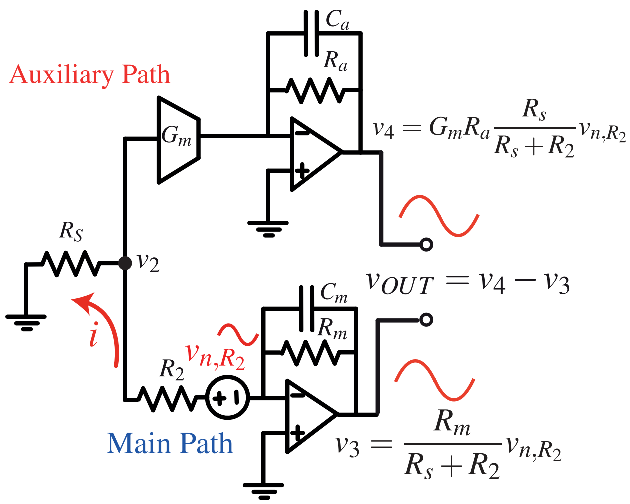


Figure 1.3: Noise cancellation in the baseline receiver.

1.3 Organization of the Dissertation

Chapter 2 deals with the modeling and linearity analysis of RF transconductor G_m. Simple expressions to compute IIP3 and compression point (P_{1dB}) of RF G_m are derived using EKV [10] and compared against simulations done using BSIM4. Chapter 2 also explains a wideband scheme to improve the linearity of RF transconductor G_m.

Chapter 3 deals with linearity analysis of passive mixer switches using EKV model. Simple expressions to calculate IIP3 and P_{1dB} of the main path are given. The analysis also gives design insight to create highly-linear main path to satisfy tough linearity specifications for cognitive radios. In addition to switch distortion, this chapter also looks at the design of local oscillator (LO) path driving mixer switches. A simple method that doubles receiver operating frequency is also shown.

Chapter 4 deals with the design of transimpedance amplifier (TIA) used in baseband to filter out unwanted signals. It provides EKV model to find the compression profile of the TIA as a function of blocker offset frequency. Based on this analysis, source-follower based inverters are used as active elements in the TIA. This helps to improve P_{1dB} of the main path.

Chapter 5 describes receiver architecture based on the building blocks analyzed in previous chapters. It also shows different operating modes of the receiver. Measurement results from the test chip are also included.

At the very end **Chapter 6** includes summary of this dissertation and discussion about future work.

CHAPTER 2

RF Transconductor

RF transconductor (G_m) is an important building block for high-linearity front-end circuits [8, 11, 12]. This chapter uses EKV model [10] to analyze distortion in inverter based RF G_m and also includes a linearization scheme to boost its linearity.

2.1 Inverter

Inverter based G_m is a commonly used implementation of transconductor in blocker-tolerant receivers [8, 11, 12]. Fig. 2.1a shows schematic of inverter based G_m biased at a DC voltage $V_{dd}/2$. It is driven by sinusoidal source v_{in} at its input. The output of inverter is current i_{out} flowing in to a virtual ground represented in Fig. 2.1a by an ideal DC voltage source $V_{dd}/2$.

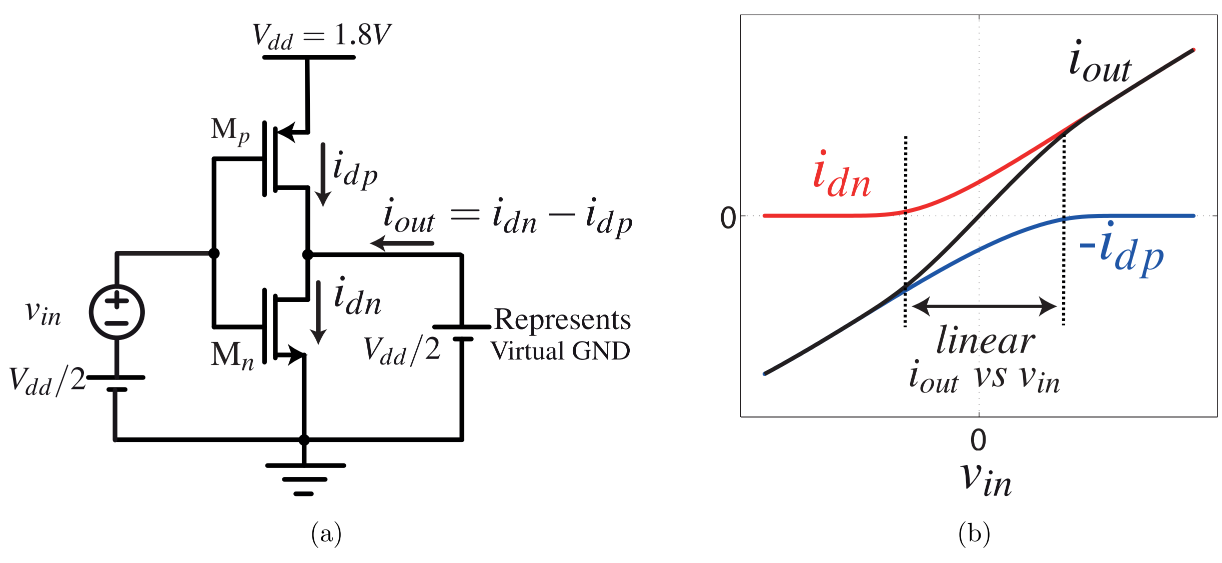


Figure 2.1: Inverter based G_m (a) Schematic. (b) DC Transfer characteristics of Inverter

DC Transfer characteristics of the inverter are shown in Fig. 2.1b. Note that i_{out} varies linearly with v_{in} as long as M_n and M_p stay in saturation. Mathematically this can be shown using EKV MOS transistor model [10].

$$\begin{aligned} i_{out} &= i_{dn} + i_{dp} \\ i_{out} &= \frac{\beta_n}{2n}\left(\frac{V_{dd}}{2} + v_{in} - V_{t0}\right)^2 - \frac{\beta_p}{2n}\left(\frac{V_{dd}}{2} - v_{in} - V_{t0}\right)^2 , \end{aligned} \tag{2.1}$$

where $\beta_n = \mu_n C_{OX}\left(\frac{W}{L}\right)_n$, $\beta_p = \mu_p C_{OX}\left(\frac{W}{L}\right)_p$ and V_{t0} is their threshold voltage (same value for both NMOS and PMOS). Assuming that $\beta_n = \beta_p = \beta$, simplifying (2.1) leads to

$$\begin{aligned} i_{out} &= 2\frac{\beta}{n}\left(\frac{V_{dd}}{2} - V_{t0}\right) v_{in} \\ i_{out} &= 2 g_{mg} v_{in} , \end{aligned} \tag{2.2}$$

where $g_{mg} = \frac{\beta}{n}\left(\frac{V_{dd}}{2} - V_{t0}\right)$ is the small-signal gate transconductance of M_n. Key point here is that even though i_{dn} and i_{dp} are square-law functions of v_{in}, i_{out} is a linear function of v_{in} due to the push-pull operation of an inverter.

2.1.1 Modeling field dependent mobility in EKV

The square-law behavior of M_n and M_p in saturation yields a linear i_{out} vs v_{in} characteristics and as a result IIP3 will be infinite as there is no third-order nonlinearity. A more realistic number for IIP3 is obtained if mobility degradation due to vertical field is taken in to account [10]. Mathematically, lets define effective β_n as

$$\beta_{effn} \triangleq \frac{\beta}{1 + \theta V_P} , \tag{2.3}$$

where V_P is the pinch-off voltage of M_n. It is defined as the channel potential at which the inversion layer charge is zero for a given gate voltage and is given by [10]

$$V_P = \frac{V_{Gn} - V_{t0}}{n} = \frac{V_{dd}/2 + v_{in} - V_{t0}}{n} .$$

Using V_P in (2.3) gives effective β_n for M_n

$$\beta_{effn} \triangleq \frac{\beta}{1 + \theta\left(\frac{V_{dd}/2 + v_{in} - V_{t0}}{n}\right)} , \tag{2.4}$$

Similarly effective β_p for M$_p$ can be defined as

$$\beta_{effp} \triangleq \frac{\beta}{1+\theta\left(\frac{V_{dd}/2-v_{in}-V_{t0}}{n}\right)} \; , \tag{2.5}$$

where $\theta L = \frac{1}{E_c} \approx 0.2\mu m/V$ (assuming same value for M$_n$ and M$_p$) and $L = 0.15\mu m$. Using β_{effn} and β_{effp} in (2.1) and performing Taylor series expansion on it gives

$$i_{out} = g_{mg}v_{in} + g_{mg2}v_{in}^2 + g_{mg3}v_{in}^3 + \cdots \; , \tag{2.6}$$

where

$$g_{mg} = \left.\frac{\partial i_{out}}{\partial v_{in}}\right|_{v_{in}=0} = \frac{2\beta\left(V_{dd}/2 - V_{t0}\right)\left(2\theta\left(V_{dd}/2 - V_{t0}\right) + 4n\right)}{4\left(\theta\left(V_{dd}/2 - V_{t0}\right) + n\right)^2} \; , \tag{2.7}$$

$$g_{mg2} = \left.\frac{1}{2}\frac{\partial^2 i_{out}}{\partial v_{in}^2}\right|_{v_{in}=0} = 0 \; , \tag{2.8}$$

$$g_{mg3} = \left.\frac{1}{6}\frac{\partial^3 i_{out}}{\partial v_{in}^3}\right|_{v_{in}=0} = \frac{-\beta\theta n^2}{\left(\theta\left(V_{dd}/2 - V_{t0}\right) + n\right)^4} \; . \tag{2.9}$$

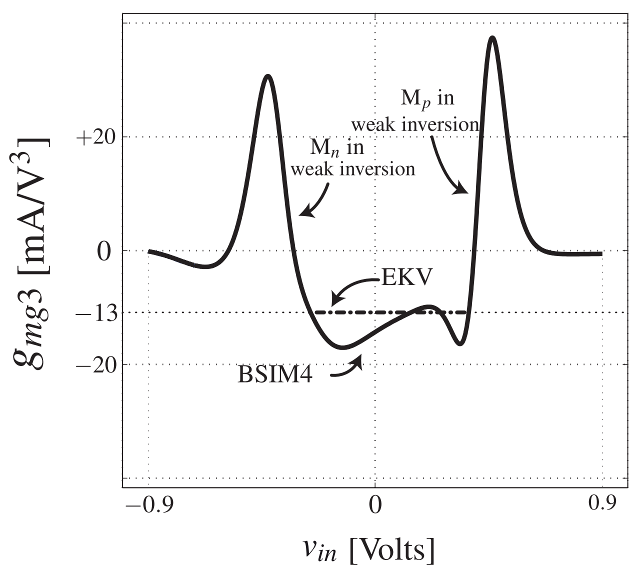
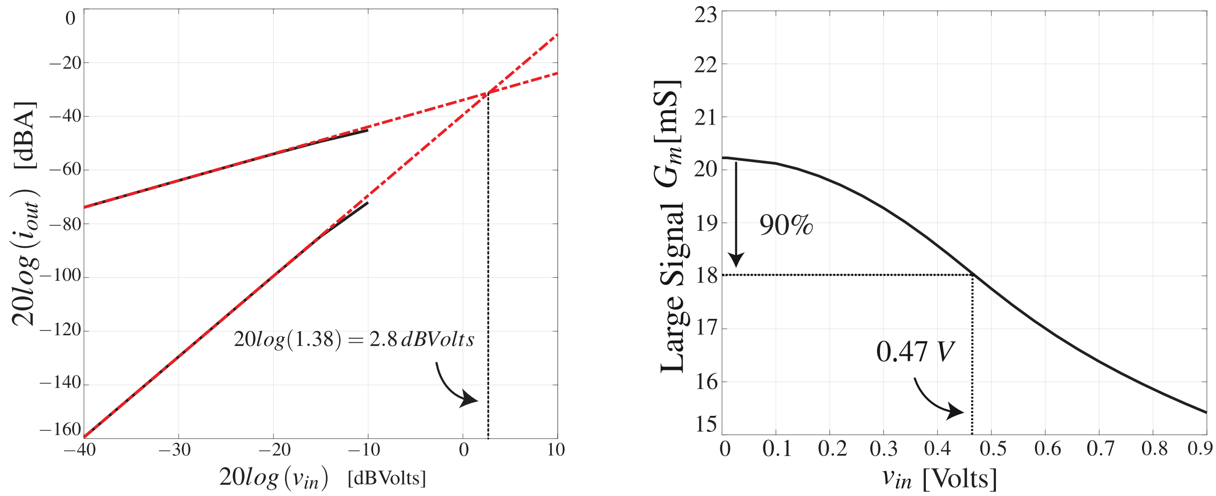


Figure 2.2: Inverter g_{mg3} plot: 28nm BSIM4 vs EKV model.

Note that g_{mg3} hase opposite sign compared to g_{mg}, and this results in compressive i_{out} vs v_{in} characteristics. Fig. 2.2 shows g_{mg3} of an inverter using CMOS 28nm BSIM4 model and compares it with the value obtained using (2.9). Note that (2.7,2.9) hold true only in



(a) (b)

Figure 2.3: SPECTRE simulation of inverter based G_m using 28nm BSIM4 model (a) IIP3 (b) 1 dB compression point (P_{1dB}).

the vicinity of $v_{in} = 0$. If v_{in} swing is large enough that it causes M_n (or M_p) to enter weak inversion (or in to triode region), then (2.7,2.9) do not apply.

The input-referred third-order intercept point (IIP3) of inverter based G_m can be calculated using (2.7) and (2.9) as

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{mg}}{g_{mg3}}\right|},$$

$$IIP3 = \left(1 + \frac{\theta}{n}\left(\frac{V_{dd}}{2} - V_{t0}\right)\right)\sqrt{\frac{4}{3}\left(\frac{V_{dd}}{2} - V_{t0}\right)\left(\frac{V_{dd}}{2} - V_{t0} + \frac{2n}{\theta}\right)}. \tag{2.10}$$

$\left(\frac{V_{dd}}{2} - V_{t0}\right)$ is equal to the quiescent value of the inverter pinch-off voltage V_P. Therefore according to (2.10) IIP3 of an inverter biased at $\frac{V_{dd}}{2}$ can be increased by raising V_{dd} itself. Fig.2.3a shows the SPECTRE simulation of IIP3 of inverter based G_m using 28nm BSIM4 model (two tones at 2 GHz and 2.02 GHz). The simulated IIP3 is in close agreement with the IIP3 value obtained using EKV model as shown in Table 2.1.

(2.7) and (2.9) can also be used to calculate input-referred 1 dB compression point (P_{1dB})

Table 2.1: Parameter values used in EKV model for RF G_m and the resulting IIP3 and P_{1dB}

Parameter	**Value**
θ	$1.5\,V^{-1}$
n	1.4
β	$69\,mA/V^2$
V_{dd}	$1.8\,V$
V_{t0}	$0.5\,V$
IIP3	$4.1\,dBV$
P_{1dB}	$0.5\,V$

of inverter based G_m.

$$\begin{aligned} P_{1dB} &= \sqrt{0.145\left|\frac{g_{mg}}{g_{mg3}}\right|}\,, \\ P_{1dB} &= \left(1+\frac{\theta}{n}\left(\frac{V_{dd}}{2}-V_{t0}\right)\right)\sqrt{0.145\left(\frac{V_{dd}}{2}-V_{t0}\right)\left(\frac{V_{dd}}{2}-V_{t0}+\frac{2n}{\theta}\right)}\,. \end{aligned} \tag{2.11}$$

Fig.2.3b shows the SPECTRE simulation of P_{1dB} of inverter based G_m using 28nm BSIM4 model (tone at 2 GHz). Large signal G_m is defined as

$$\begin{aligned} v_{in} &= A_{in} cos\left(\omega_{RF} t\right)\ , \\ i_{out}\left(t\right) &= \sum_{k=1}^{\infty} I_{out}\left[k\right] cos\left(k\omega_{RF} t\right)\ , \\ G_m &= \frac{I_{out}\left[1\right]}{A_{in}}. \end{aligned} \tag{2.12}$$

Simulated P_{1dB} (0.47 V) using BSIM4 model is in close agreement with P_{1dB} (0.5 V) obtained using EKV model.

2.2 Using Auxiliary Inverters for Linearization

In the last section it has been shown that g_{mg3} (third-order coefficient of the Taylor expansion of i_{out}) has opposite sign to that of g_{mg} (transconductance of inverter and the first-order coefficient of the Taylor expansion of i_{out}). This results in compressive i_{out} vs v_{in} characteristics of the inverter based transconductor. However if a positive g_{mg3} of an auxiliary FET is used to nullify the negative g_{mg3} of an inverter, then the resulting composite g_{mg3} will be zero and IIP3 of the composite will be greatly improved. This idea has been used in [13, 14, 15, 16, 17, 18], sometimes referred to as the Derivative Superposition Linearization method.

Let's consider an inverter based G_m and its corresponding g_{mg3} as a function of v_{in} (in Fig. 2.4a and Fig. 2.4b). Let's add an auxiliary FET M_{a1} in Fig. 2.4a. Its $g_{mg3,a1}$ is shown as the solid blue line in Fig. 2.4b. $g_{mg3,a1}$ curve can be shifted to the right by biasing M_{a1} gate at a different potential relative to that of M_n (by inserting a series voltage source V_{b1} as shown in Fig. 2.4c). Note that the size of M_{a1} can be adjusted such that the positive peak of $g_{mg3,a1}$ approximately cancels out g_{mg3}. The same process can be repeated to introduce another auxiliary FET M_{a3} (with offset voltage V_{b3}) such that $g_{mg3,a3}$ cancels out g_{mg3} across a wide range of v_{in}. Cancellation of g_{mg3} over an even wider range of v_{in} is possible by adding more auxiliary FETs (Fig. 2.5a). The end result is that $G_{mg3,composite}$ stays zero over approximately the full range of v_{in}. This boosts IIP3 and P_{1dB} of the composite transconductor.

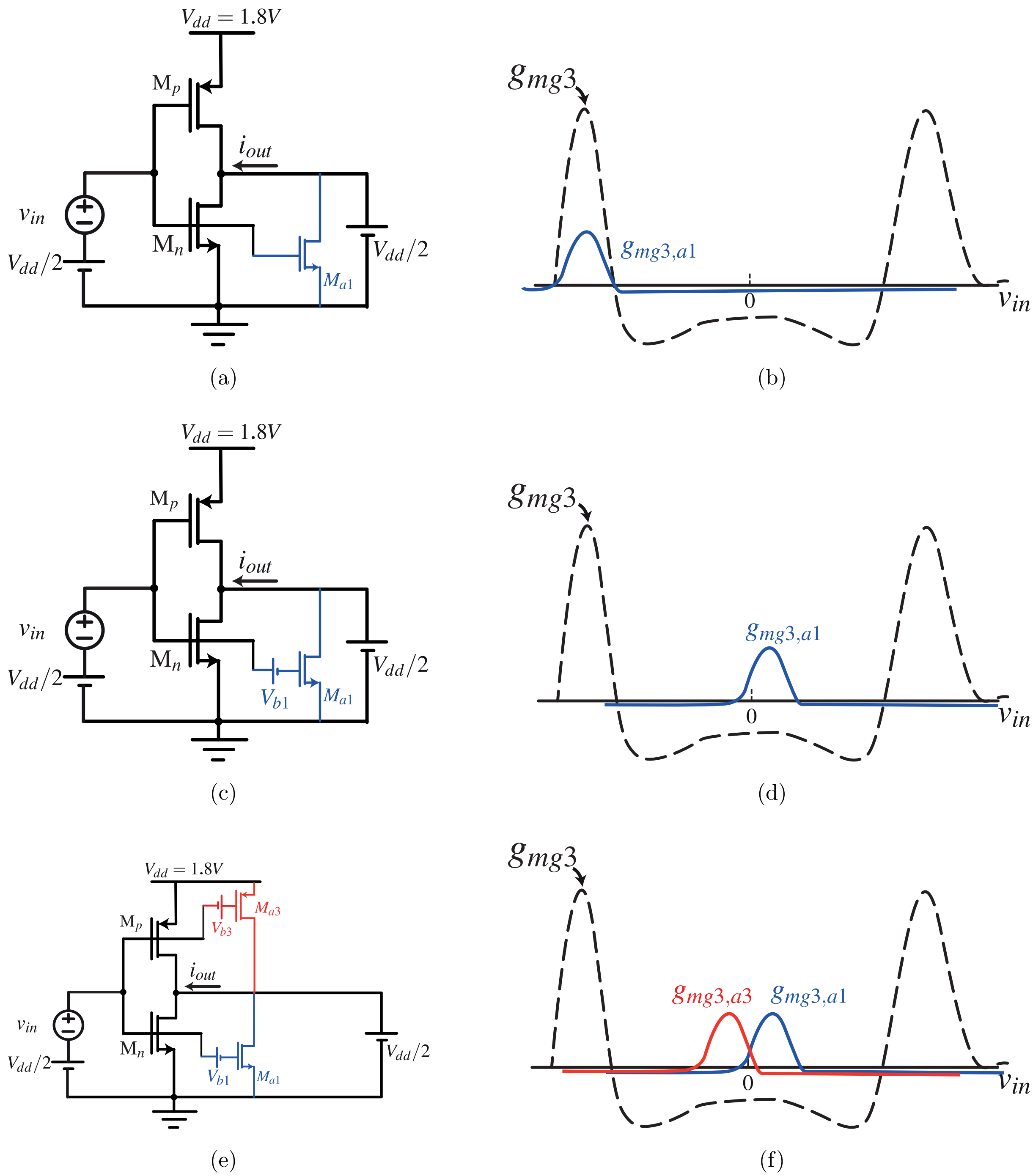


Figure 2.4: SPECTRE simulation of inverter based G_m using 28nm BSIM4 model (a) IIP3 (b) 1 dB compression point (P_{1dB}).

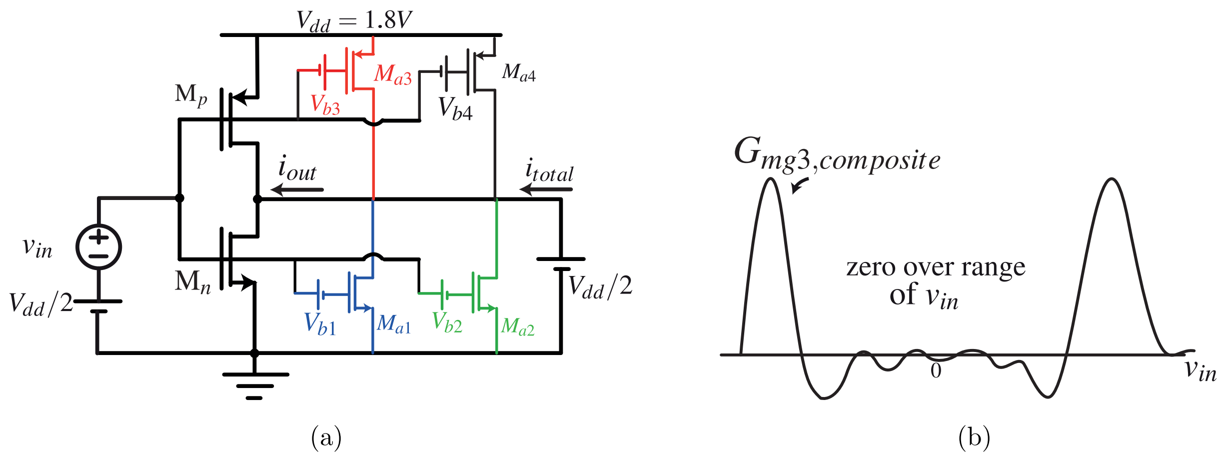


Figure 2.5: Composite G_m using main inverter (M$_n$, M$_p$) and auxiliary inverters (M$_{a1}$, M$_{a2}$, M$_{a3}$, M$_{a4}$) (a) Schematic (b) Third-order coefficient of Taylor expansion of i_{total}.

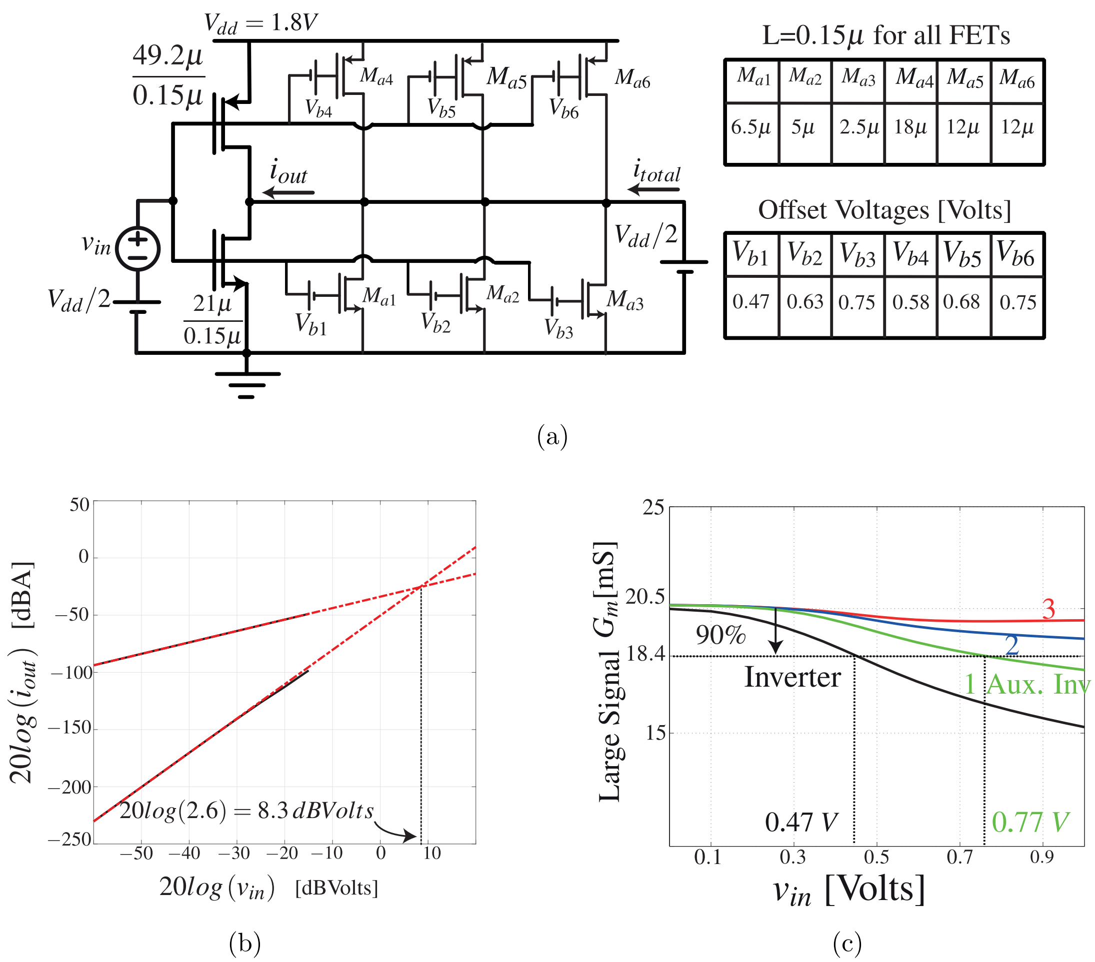


Figure 2.6: Composite G_m simulation results using 28nm BSIM4 models (a) Simulation setup (b) IIP3 (c) P$_{1dB}$

Fig. 2.6b shows simulated IIP3 of the composite G_m and it is approximately 6 dB higher than the IIP3 of a simple inverter. Fig. 2.6c shows that by using 3 auxiliary inverters (or 6 auxiliary FETs) it is possible to obtain a very linear large signal transconductance that can withstand 0.9 V amplitude v_{in} at its input.

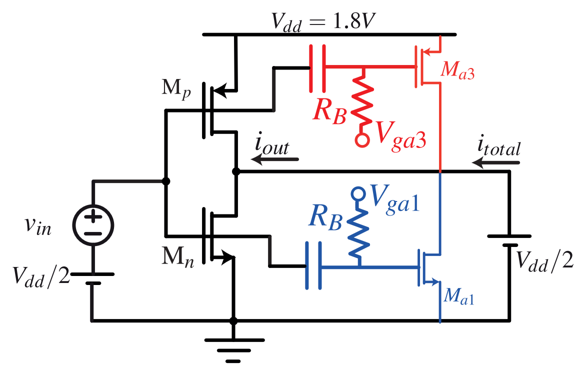
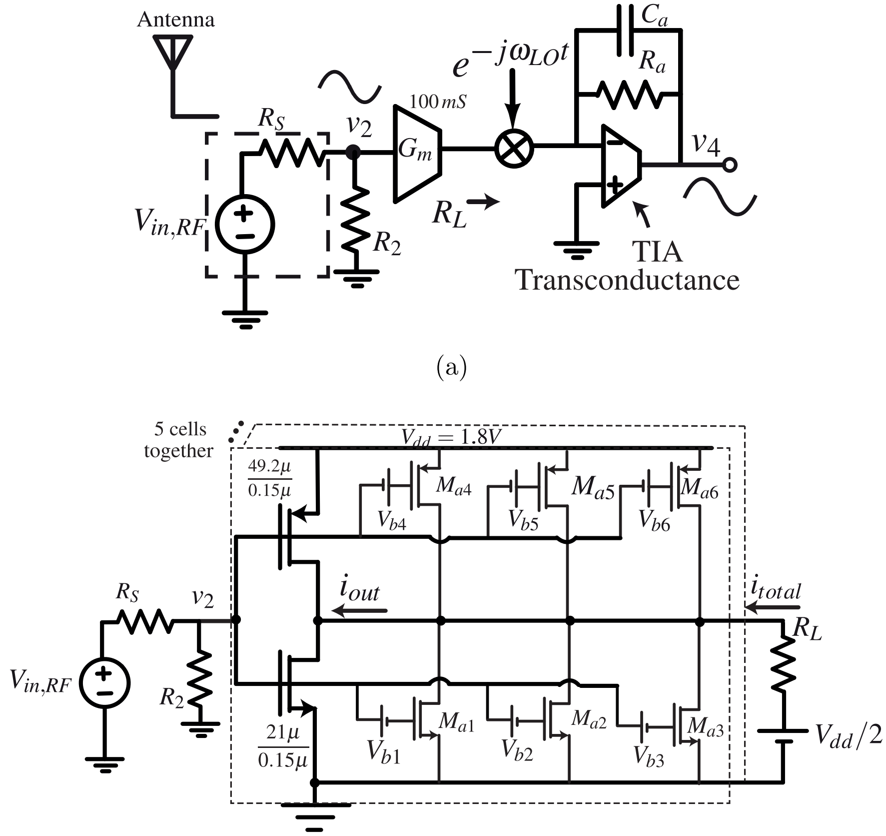


Figure 2.7: Implementation of offset voltages

In practice v_{in} is ac coupled to the gate of auxiliary FETs and offset voltages (V_{b1} and V_{b2}) are connected to their gate by large resistors R_B as shown in Fig. 2.7 ([17, 18]).

2.2.1 Impact of Imperfect Virtual Ground

Composite G_m is embedded in a complete receiver (Fig. 2.8a) to get a sense of its realistic performance. Fig. 2.8b is a simplified version of Fig. 2.8a where R_L represents the mixer switch resistance and the upconverted TIA impedance. Fig. 2.9 plots the 1dB small-signal gain compression of the composite G_m ($100\,mS$) against the size of R_L using 28nm BSIM4. It shows that in order to tolerate a $+8\,dBm$ blocker ($1.6\,V_{pp}$ swing at v_2) virtual ground resistance has to be kept less than $2.2\,\Omega$. This value of R_L in turn dictates the size of mixer switches and the size of TIA transconductance. Larger size mixer switches result in higher LO power consumption, and a larger size of TIA transconductance result in higher power consumption in baseband part of receiver.



(b)

Figure 2.8: Composite G_m (a) Embedded in receiver (b) Testbench for Blocker P_{1dB}

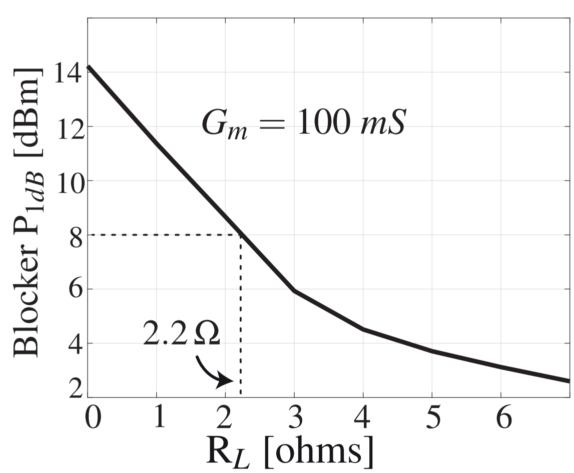
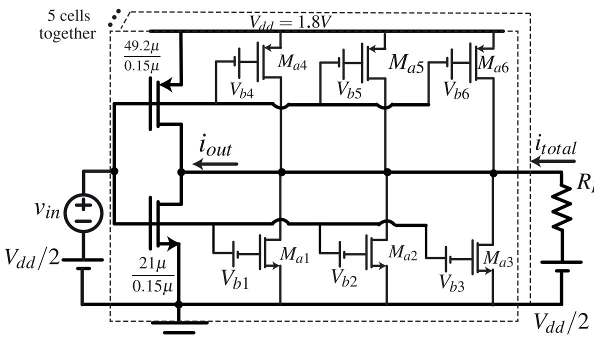


Figure 2.9: Blocker P_{1dB} of composite G_m vs R_L

2.2.2 Impact of Offset Voltage variation on compression point

Fig. 2.10a V_{b2}, V_{b4} and V_{b5} were changed from their nominal value to either $0.47\,V$ or $0.75\,V$. Fig. 2.10b shows gain compression of the composite G_m ($100\,mS$) with these new offset voltages. Clearly P_{1dB} of the composite G_m is somewhat lowered for the same R_L.



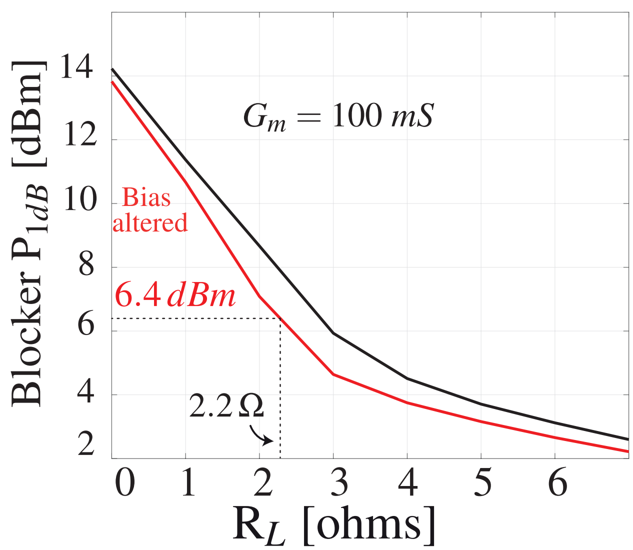
L=0.15μ for all FETs

M_{a1}	M_{a2}	M_{a3}	M_{a4}	M_{a5}	M_{a6}
6.5μ	5μ	2.5μ	18μ	12μ	12μ

Offset Voltages [Volts]

V_{b1}	V_{b2}	V_{b3}	V_{b4}	V_{b5}	V_{b6}
0.47	0.75	0.75	0.47	0.75	0.75

(a)



(b)

Figure 2.10: Composite G_m (a) Changing gate offset voltages (b) Impact on Blocker P_{1dB} of the composite G_m due to bias voltage variation.

2.3 Noise Figure of Inverter G_m vs Composite G_m

It has been shown in the last section that composite G_m has better linearity than that of a simple inverter based G_m. To get a complete picture, noise figure of the two architectures should also be taken in to consideration. Fig. 2.11a shows the network under consideration. G_m can be realized as a simple inverter or by the composite architecture. Small signal noise factor will be the same in both cases because auxiliary FETs in composite G_m are OFF under small-signal operation. Noise Factor (F) of the network in Fig. 2.11a is

$$F = 1 + \frac{\gamma}{G_m R_s} \tag{2.13}$$

where $\gamma = 1$ is the noise coefficient, and $G_m = 100\,mS$ is the small-signal transconductance. $R_s = 50\Omega$ is the source resistance. Fig. 2.11b compares the simulated noise figure $(10log(F))$ of simple inverter based G_m vs the composite G_m.

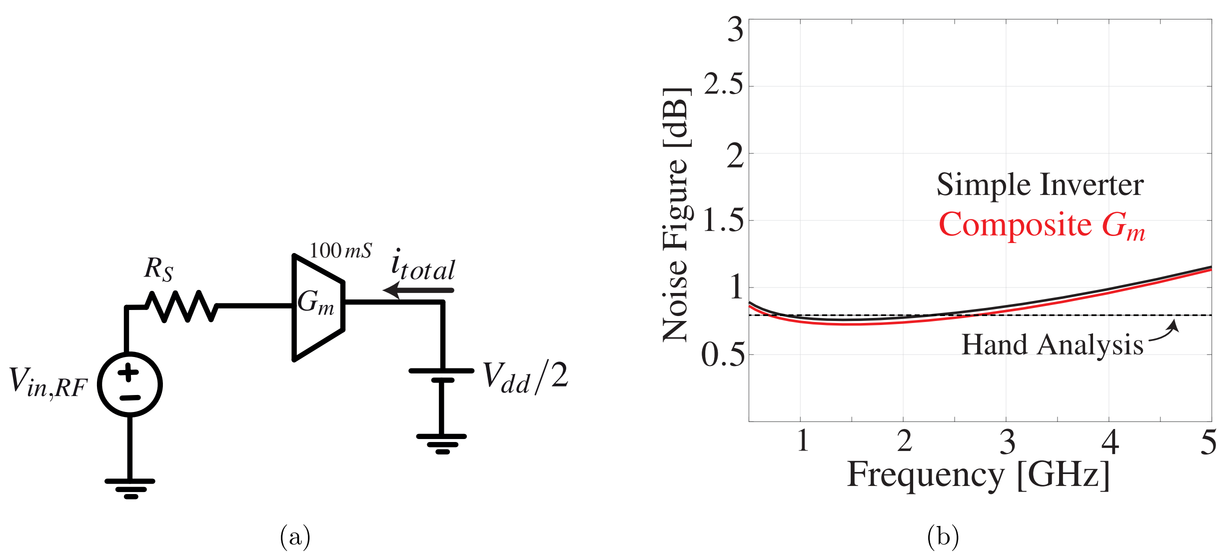


Figure 2.11: Noise Figure comparison (a) Schematic (b) Noise Figure comparison of simple inverter vs composite G_m

2.4 Conclusion

In this chapter, EKV based FET model was used to analyze RF G_m nonlinearity. Expressions for IIP3 and P_{1dB} were found, which showed that raising supply voltage V_{dd} increases the linearity of inverter based G_m. Derivative superposition method was shown to boost inverter linearity by making G_{m3} zero over wide range of input amplitude without compromising its noise figure. As a result composite G_m is selected for use in the prototype receiver.

CHAPTER 3

Passive Mixer and LO Design

3.1 Passive Mixer Nonlinearity

Mixers form a crucial part of all receivers. Mixers are the first circuit block in case of mixer-1^{st} receivers and their distortion can limit receiver linearity. [19, 20, 21, 6] are examples of prior work done to analyze mixer nonlinearity. The biggest contribution to mixer nonlinearity comes from the nonlinear i_D vs v_{DS} relationship of mixer switch. The goal here is to quantify mixer switch nonlinearity using simple yet effective methods, and to come up with design strategies that enable a highly-linear mixer-1^{st} receiver.

3.1.1 NMOS Passive Mixer

Fig. 3.1a shows a mixer-first receiver using 25% duty cycled non-overlapping clocks to drive mixer switches. To simplify mixer nonlinearity analysis, baseband TIA is assumed to be perfectly linear and have zero input impedance. DC voltage V_{dc} represents virtual ground at the baseband TIA input. Furthermore each one of the mixer switches can be replaced by as series combination of an *always-ON NMOS* and an *ideal switch*. The always-ON NMOS gate is tied to high logic value of the clock $V_{g,ON}$ and the ideal switches are driven by non-overlapping clocks. In this way mixer operation is divided in to two halves: always-ON NMOS models i_D vs v_{DS} nonlinearity while the ideal switch models the switching action.

Since ideal-switches are driven by non-overlapping clocks and at any given time only one of the switches is closed. This allows always-ON NMOS to be slided to the left resulting in the circuit shown in Fig 3.1c. Since the drain terminal of the always-ON NMOS is connected to V_{dc} at any given time, the circuit is in Fig. 3.1c can be simplified further, giving rise to the network in Fig 3.1d.

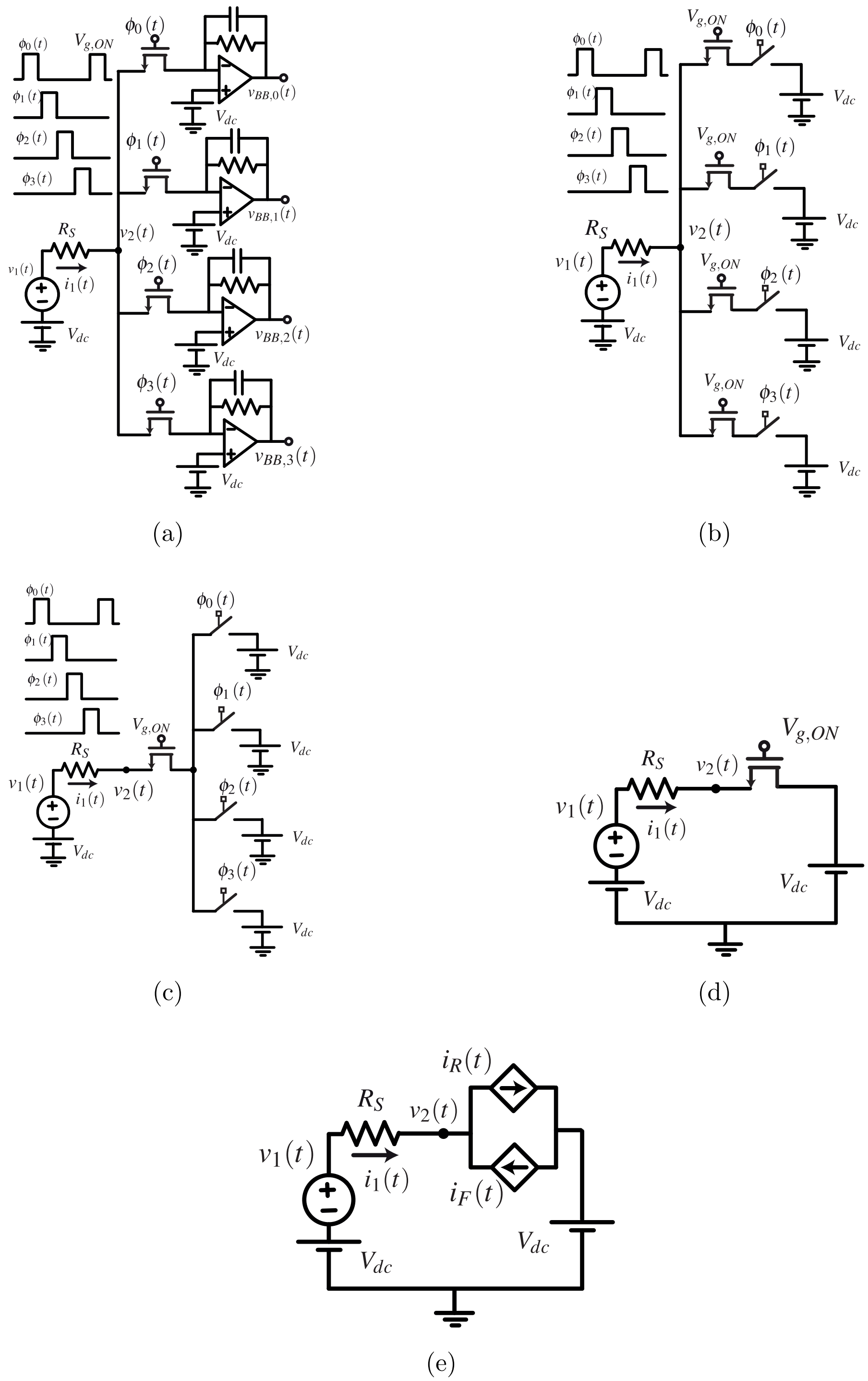


Figure 3.1: Mixer-first Receiver G_m (a) Schematic. (b), (c), (d), (e) Circuit Simplifications

Always-ON NMOS can be modeled using EKV [10]. $i_F(t)$ represents the forward-current and $i_R(t)$ represents the reverse current source.

$$i_F = \frac{n\beta}{2}\left(V_P - V_{dc} - v_2(t)\right)^2 \ , \tag{3.1a}$$

$$i_R = \frac{n\beta}{2}\left(V_P - V_{dc}\right)^2 \ , \tag{3.2a}$$

where $\beta = \mu_n C_{OX}\left(\frac{W}{L}\right)_n$ and $V_P = \frac{V_{g,ON} - V_{t0}}{n}$ (pinch-off voltage) are the parameters of the always-ON NMOS. RF current $i_1(t)$ that flows in the loop is given by,

$$i_1(t) = i_R(t) - i_F(t) = \frac{n\beta}{2}\left[2\left(V_P - V_{dc}\right)v_2(t) - v_2^2(t)\right] \ . \tag{3.3}$$

For a sinusoidal signal applied to the network of Fig. 3.1e ($v_1(t) = V_1 cos(\omega t)$), current $i_1(t)$ will have a fundamental component and harmonics. $i_1(t)$ can be represented using Fourier series as

$$i_1(t) = I_{1,1}cos(\omega t) + I_{1,2}cos(2\omega t) + I_{1,3}cos(3\omega t) \ , \tag{3.4}$$

where $I_{1,1}$ is the amplitude of the fundamental and $I_{1,2}$, $I_{1,3}$ are the amplitudes of the second and third harmonics. It is assumed that $i_1(t)$ can be adequately represented using only the first three terms of the Fourier series because the network is weakly nonlinear. $v_2(t)$ can be represented as

$$v_2(t) = V_{2,1}cos(\omega t) + V_{2,2}cos(2\omega t) + V_{2,3}cos(3\omega t) \ , \tag{3.5}$$

where $V_{2,1}$ is the amplitude of the fundamental and $V_{2,2}$, $V_{2,3}$ are the amplitudes of the second and third harmonics.

Fundamental Frequency Terms

Substituting (3.4) and (3.5) in (3.3), and equating coefficients of $cos(\omega t)$ from both sides of the resulting equation gives

$$I_{1,1} = \frac{n\beta}{2}\left[2\left(V_P - V_{dc}\right)V_{2,1} - V_{2,2}\left(V_{2,1} + V_{2,3}\right)\right] \tag{3.6}$$

Since the network is weakly nonlinear, for small amplitude of applied voltage V_1 $V_{2,2}(V_{2,1}+V_{2,3})$ is much smaller than $2(V_P - V_{dc})V_{2,1}$ in (3.6) and $I_{1,1}$ can be approximated as

$$I_{1,1} \approx n\beta\,(V_P - V_{dc})\,V_{2,1}\ , \tag{3.7}$$

$$I_{1,1} \approx \frac{V_{2,1}}{R_{on}}\ . \tag{3.8}$$

where on-resistance of NMOS is $R_{on}^{-1} = n\beta\,(V_P - V_{dc})$. Applying KVL to the network of Fig. 3.1e, amplitudes of the fundamental components of voltages are given by

$$V_1 = I_{1,1}R_s + V_{2,1}\ ,$$

$$V_1 = I_{1,1}R_s + I_{1,1}R_{on}\ ,$$

$$I_{1,1} = \frac{V_1}{R_s + R_{on}}\ , \tag{3.9a}$$

$$V_{2,1} = \frac{R_{on}}{R_s + R_{on}}V_1\ . \tag{3.9b}$$

Second Harmonic Terms

Substituting (3.4) and (3.5) in (3.3), and equating coefficients of $cos(2\omega t)$ from both sides of the resulting equation gives

$$I_{1,2} = \frac{n\beta}{2}\left[2\,(V_P - V_{dc})\,V_{2,2} - V_{2,3}V_{2,1} - \frac{V_{2,1}^2}{2}\right] \tag{3.10}$$

Ignoring $V_{2,3}V_{2,1}$ (3.10) gives

$$I_{1,2} \approx \frac{V_{2,2}}{R_{on}} - \frac{V_{2,1}^2}{2}\ . \tag{3.11}$$

Applying KVL to the network of Fig. 3.1e, amplitudes of second harmonic terms are

$$0 = I_{1,2}R_s + V_{2,2}\ . \tag{3.12}$$

Substituting $V_{2,1}$ from (3.9b) in (3.12) and simplifying the resulting expression gives

$$I_{1,2} = -\frac{n\beta}{4}\left(\frac{R_{on}}{R_{on}+R_s}\right)^3 V_1^2\ , \tag{3.13a}$$

$$V_{2,2} = \frac{n\beta}{4}R_s\left(\frac{R_{on}}{R_{on}+R_s}\right)^3 V_1^2\ . \tag{3.13b}$$

Third Harmonic Terms

Substituting (3.4) and (3.5) in (3.3), and equating coefficients of $cos(3\omega t)$ from both sides of the resulting equation gives

$$I_{1,3} = \frac{n\beta}{2}\left[2\left(V_P - V_{dc}\right)V_{2,3} - V_{2,2}V_{2,1}\right] \tag{3.14}$$

Simplifying (3.14) by substituting values of $V_{2,1}$ from (3.9b) and $V_{2,2}$ from (3.13b) gives

$$I_{1,3} = \frac{V_{2,3}}{R_{on}} - \frac{n^2\beta^2}{8}R_s\left(\frac{R_{on}}{R_{on}+R_s}\right)^4 V_1^3 \,. \tag{3.15}$$

Applying KVL to the network of Fig. 3.1e, amplitudes of third harmonic terms are

$$0 = I_{1,3}R_s + V_{2,3} \,. \tag{3.16}$$

Substituting $V_{2,3}$ from (3.15) in (3.16) and simplifying the resulting expression gives

$$I_{1,3} = -\frac{n^2\beta^2}{8}R_s\left(\frac{R_{on}}{R_{on}+R_s}\right)^5 V_1^3 \,, \tag{3.17a}$$

$$V_{2,3} = \frac{n^2\beta^2}{8}R_s^2\left(\frac{R_{on}}{R_{on}+R_s}\right)^5 V_1^3 \,. \tag{3.17b}$$

IIP3

In terms of Taylor series $i_1(t)$ can be written as

$$i_1(t) = \alpha_1 v_1(t) + \alpha_2 v_1^2(t) + \alpha_3 v_1^3(t) \,. \tag{3.18}$$

If $v_1(t) = V_1 cos(\omega t)$, then (3.18) becomes

$$i_1(t) \approx \alpha_1 V_1 cos(\omega t) + \frac{\alpha_2}{2}V_1^2 cos(2\omega t) + \frac{\alpha_3}{4}V_1^3 cos(3\omega t) \,, \tag{3.19}$$

$$i_1(t) \approx I_{1,1}cos(\omega t) + I_{1,2}cos(2\omega t) + I_{1,3}cos(3\omega t) \,. \tag{3.20}$$

Thus

$$\alpha_1 = \frac{1}{R_{on}+R_s} \,, \tag{3.21a}$$

$$\alpha_3 = -\frac{n^2\beta^2}{4}R_s\left(\frac{R_{on}}{R_{on}+R_s}\right)^5 \,. \tag{3.21b}$$

Therefore IIP3 of mixer-first receiver is

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|},$$
$$IIP3 = \frac{2}{n\beta}\left(\frac{R_{on}+R_s}{R_{on}}\right)^2 \sqrt{\frac{2}{3}\frac{1}{R_s R_{on}}} \qquad [Volts]\,. \tag{3.22}$$

From (3.22), IIP3 of mixer-1^{st} receiver can be improved by increasing $\frac{R_s}{R_{on}}$. Intuitively this makes sense also because as $\frac{R_s}{R_{on}}$ increases, voltage swing $v_2(t)$ across the mixer RF input reduces, suppressing i_D vs v_{DS} nonlinearity. Fig. 3.2 shows the simulated IIP3 of mixer-first receiver using 16nm BSIM-CMG models. Table 3.1 gives the value of EKV parameters and IIP3 calculated using (3.22).

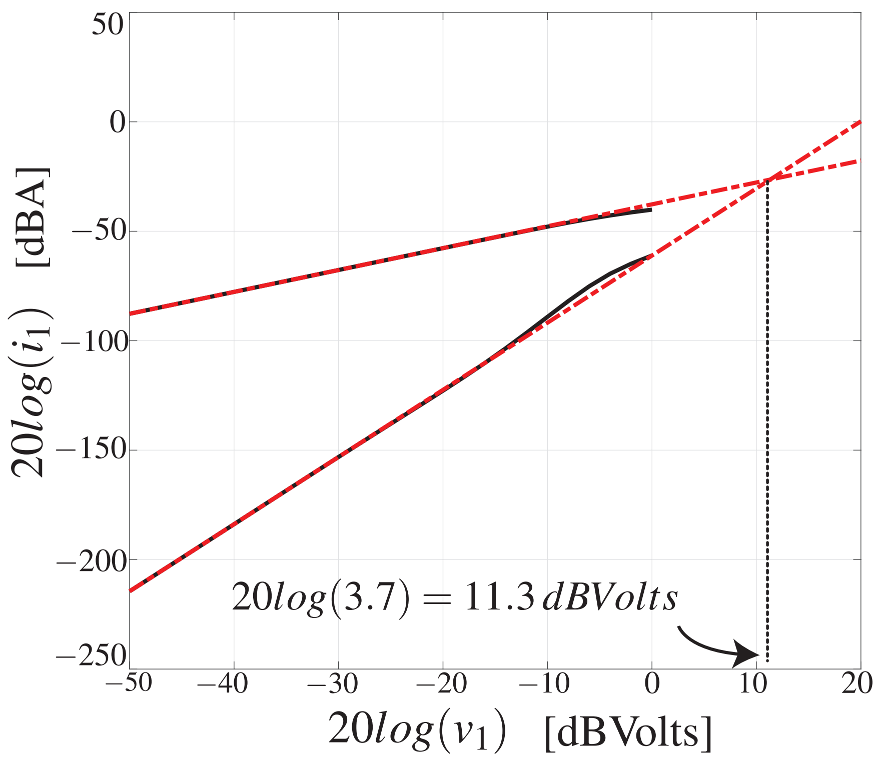


Figure 3.2: IIP3 of mixer-first receiver using NMOS mixer switches and ideal baseband TIA using 16nm BSIM-CMG model

Table 3.1: Parameter values used in EKV model of mixer switch nonlinearity and the resulting IIP3 and P_{1dB}

Parameter	**Value**
R_s	$50\,\Omega$
n	1.1
β	$50\,mA/V^2$
$V_{g,on}$	$1.8\,V$
V_{t0}	$0.17\,V$
V_{dc}	$0.9\,V$
IIP3	$14.3\,dBV$
P_{1dB}	$4.7\,dBV$

The same analysis can be used to compute P_{1dB} of the receiver and is given as

$$\begin{aligned} P_{1dB} &= \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}, \\ P_{1dB} &\approx \frac{2}{3n\beta}\left(\frac{R_{on}+R_s}{R_{on}}\right)^2\sqrt{\frac{2}{3}\frac{1}{R_sR_{on}}} \qquad [Volts]\,. \end{aligned} \tag{3.23}$$

Simulated P_{1dB} (1.0 dBV) of mixer-first receiver (see Fig. 3.3) using 16nm BSIM-CMG models is comparable to P_{1dB} (4.7 dBV) calculated from (3.23).

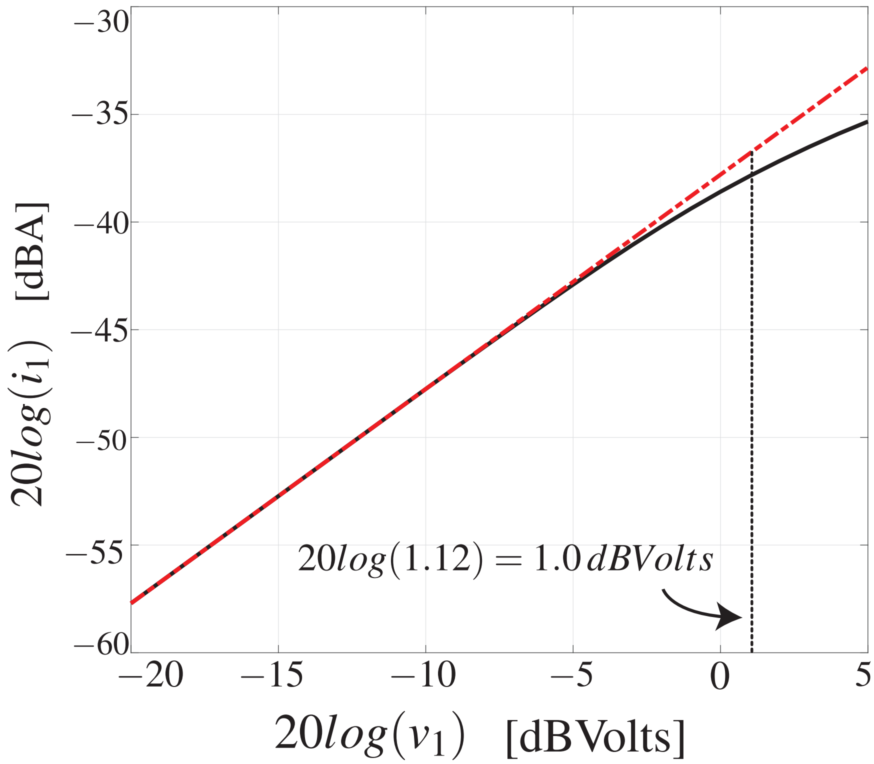


Figure 3.3: P_{1dB} of mixer-first receiver using NMOS mixer switches and ideal baseband TIA using 16nm BSIM-CMG model

3.1.2 CMOS Passive Mixer

Fig. 3.4a shows a mixer-first receiver using CMOS mixer switches. Similar to NMOS mixer switch nonlinearity analysis, baseband TIA can be assumed to be perfectly linear with zero input impedance and the network can be simplified in to the form shown in Fig. 3.4b. Using EKV models for the NMOS and PMOS FETs in triode region,

$$i_{FN}(t) = \frac{n\beta_n}{2}\left(V_{Pn} - V_{dc} - v_2(t)\right)^2 \ , \tag{3.24a}$$

$$i_{RN}(t) = \frac{n\beta_n}{2}\left(V_{Pn} - V_{dc}\right)^2 \ , \tag{3.24b}$$

$$i_{FP}(t) = \frac{n\beta_p}{2}\left(V_{Pp} - V_B + V_{dc} + v_2(t)\right)^2 \ , \tag{3.25a}$$

$$i_{RP}(t) = \frac{n\beta_p}{2}\left(V_{Pp} - V_B + V_{dc}\right)^2 \ . \tag{3.25b}$$

where $\beta_n = \mu_n C_{OX}\left(\frac{W}{L}\right)_n$, $\beta_p = \mu_p C_{OX}\left(\frac{W}{L}\right)_p$ and V_{t0} is their threshold voltage (same value for both NMOS and PMOS). V_B is the body bias voltage of the PMOS. $V_{Pn} =$

$(V_{gn,ON} - V_{t0})/n$ is the pinch-off voltage for NMOS, and $V_{Pp} = (V_B - V_{gp,ON} - V_{t0})/n$ is the pinch-off voltage for PMOS. Assuming the sizes of NMOS and PMOS are chosen such that $\beta_n = \beta_p = \beta$, and the logic high values of the clocks are such that $V_{Pn} = V_{Pp} = V_P$ then $i_1(t)$ can be expressed as

$$i_1(t) = (i_{RN} - i_{FN}) + (i_{FP} - i_{RP}) \, ,$$
$$i_1(t) = n\beta v_2 (2V_P - V_B) \, . \tag{3.26}$$

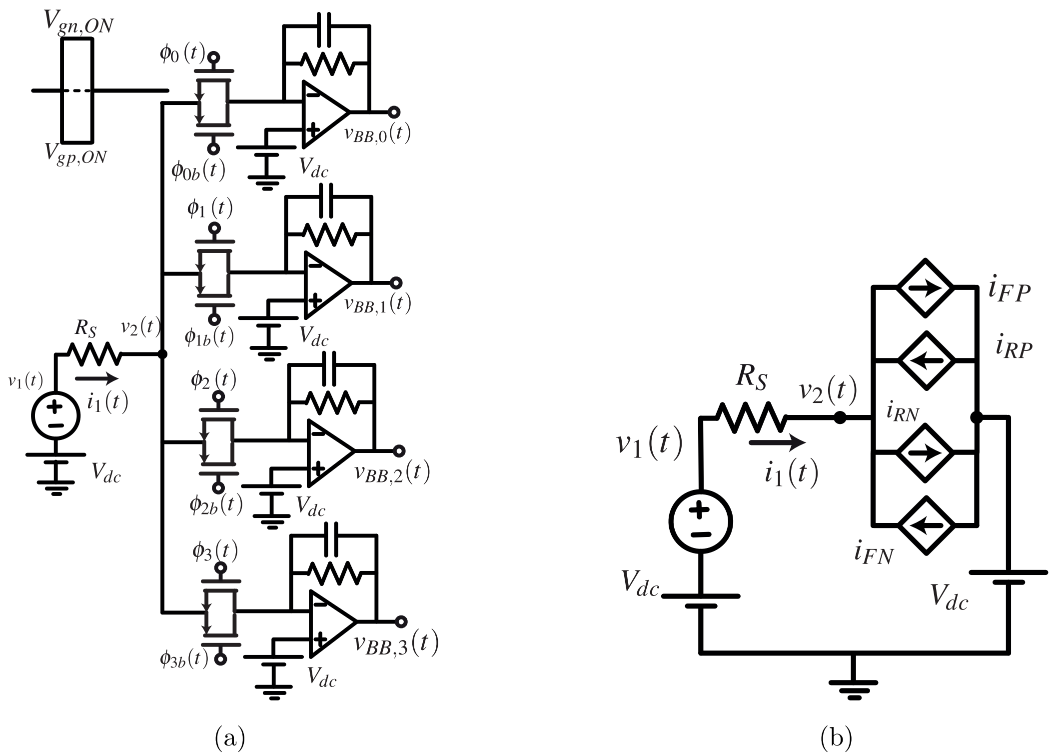


Figure 3.4: Mixer-first Receiver using CMOS mixer switches (a) Schematic. (b) Circuit Simplification

(3.26) implies that NMOS and PMOS cancel out each other i_D vs v_{DS} nonlinearity in a CMOS mixer switch. In practice, it is not possible to precisely match NMOS and PMOS and completely eliminate i_D vs v_{DS} nonlinearity. Nonetheless CMOS mixer switch achieves a higher IIP3 as compared to similarly sized NMOS switch. Fig. 3.5 shows the simulated IIP3 for a mixer-first receiver that uses CMOS switches and it is about 8 dB higher than that of a NMOS switch.

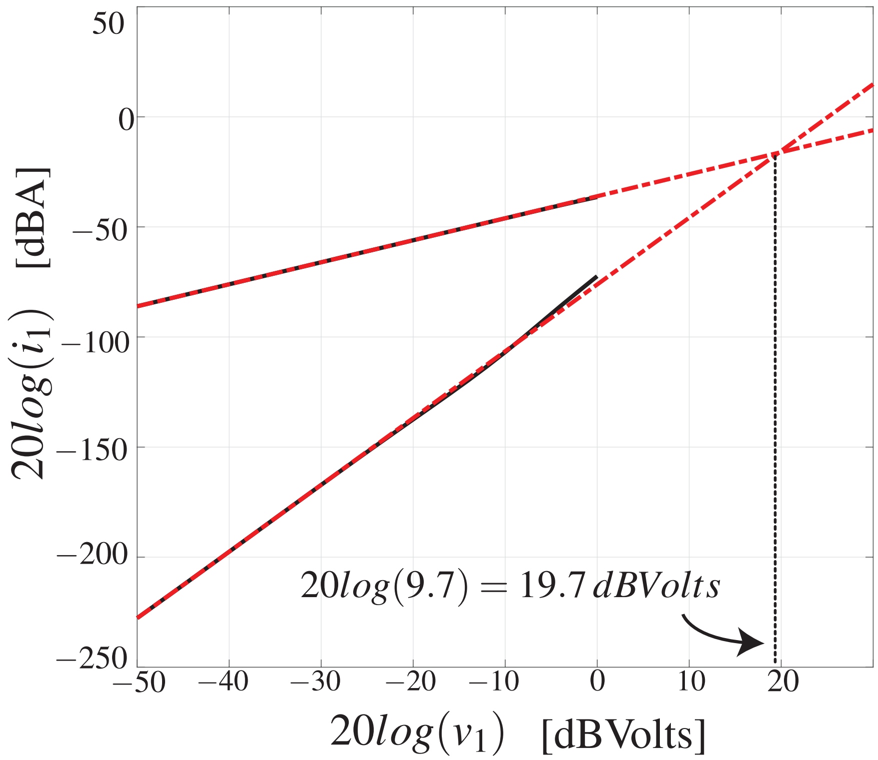


Figure 3.5: IIP3 of mixer-first receiver using CMOS mixer switches and ideal baseband TIA using 16nm BSIM-CMG model

Simulated P_{1dB} of mixer-first receiver using CMOS switches is shown in Fig. 3.6and it is approzimately $7\,dB$ higher than that of NMOS mixer switches.

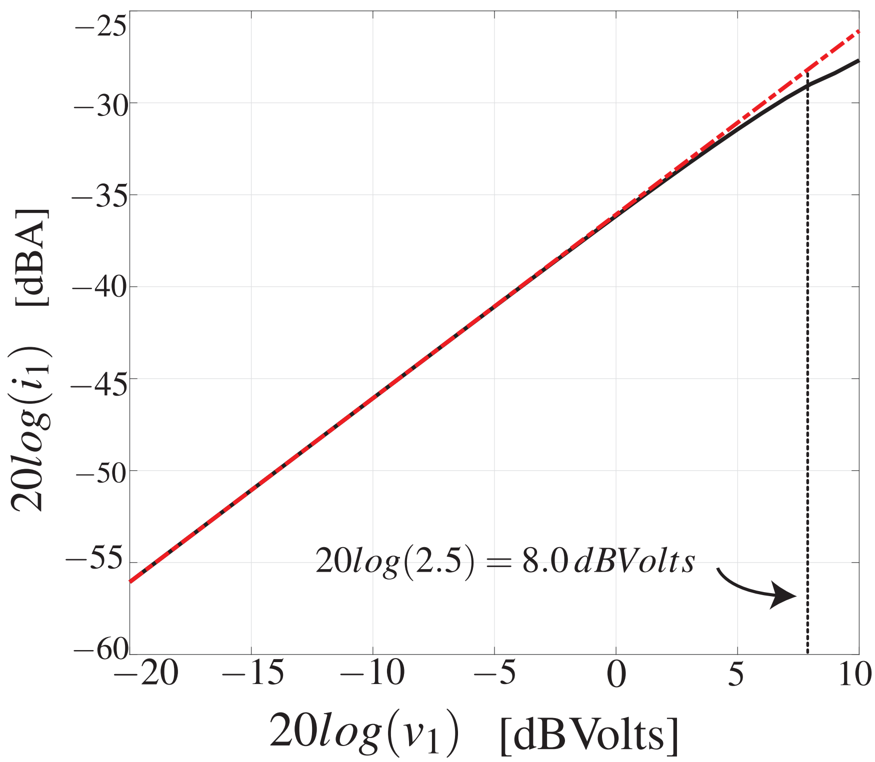


Figure 3.6: P_{1dB} of mixer-first receiver using CMOS mixer switches and ideal baseband TIA using 16nm BSIM-CMG model

3.2 Downconversion using 8-phase mixing

In this work RF signal is down-converted by 8 passive mixer switches driven by 1/8 duty cycle non-overlapping clocks as shown in Fig. 3.7a. The down-converted current is transformed to voltage by transimpedance amplifiers (TIA). The final output is the weighted summation of the TIA outputs. $(K_0, K_1, ..., K_7)$ are the baseband weighting coefficients whose values are chosen such that the RF signal is multiplied effectively by a complex sine wave that is sampled-and-held 8 times per cycle (see Fig. 3.7b). As a result the first alias term is moved to -7th harmonic and is 16.9 dB lower relative to the fundamental (see Fig. 3.7c). A complete mathematical analysis of this approach is given in [9].

A shift register based divide-by-4 circuit is used to generate these 8 non-overlapping clocks. The divider circuit works reliably up to $f_{LO} = 3GHz$. This limits the max operating

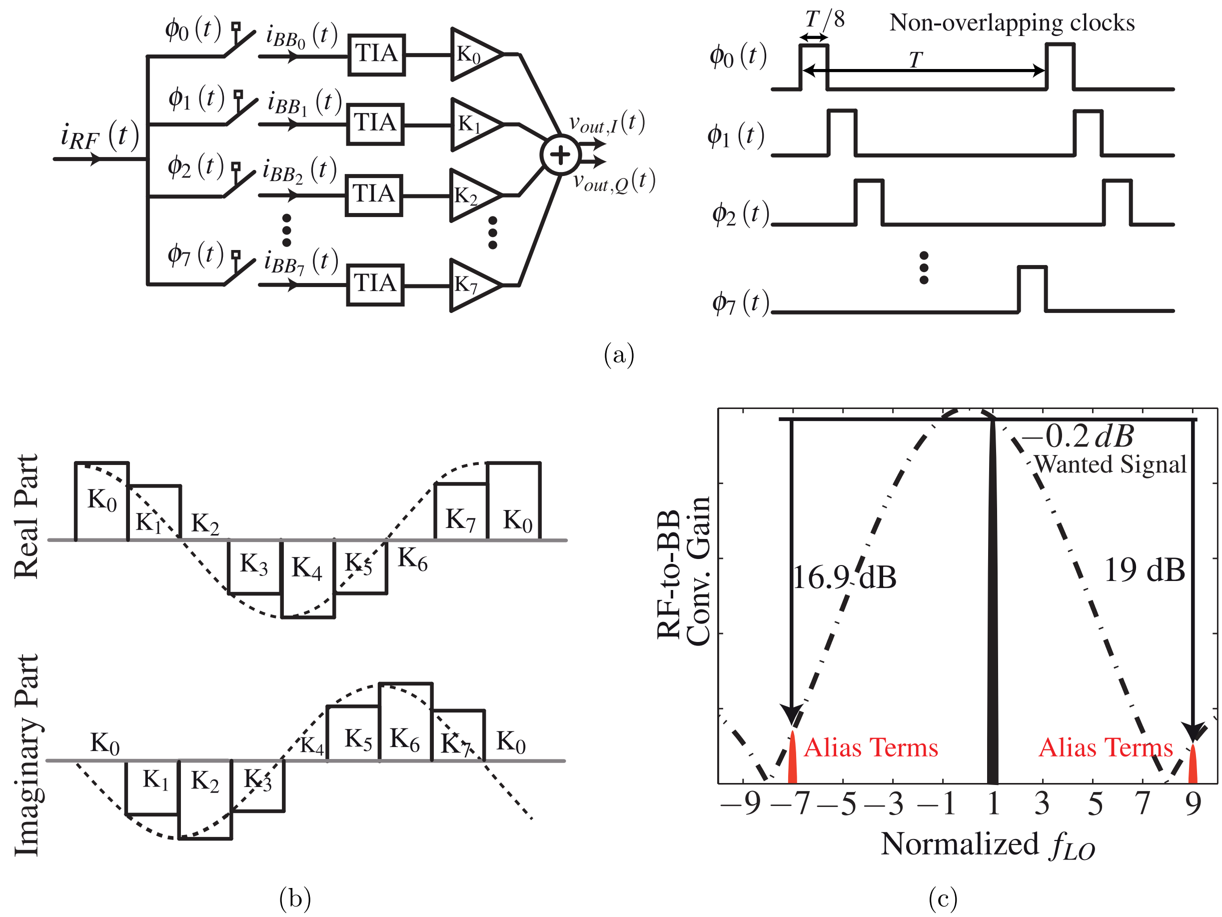
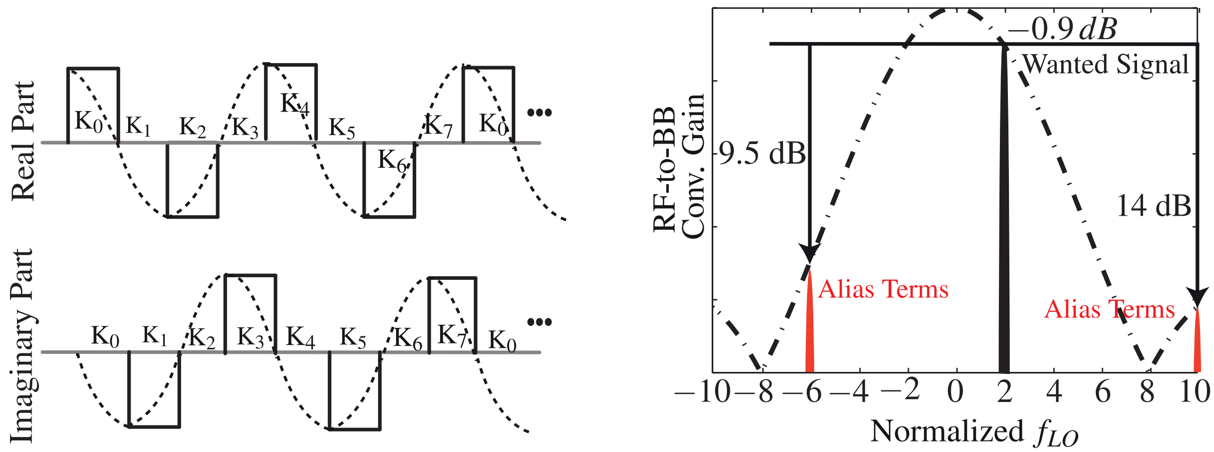


Figure 3.7: (a) 8-phase Mixer downconversion, (b) Sampled-and-held complex sine wave, (c) Spectrum of the complex sine wave

frequency of receiver to $f_{LO} = 3GHz$. One way to overcome this constraint is to reconfigure baseband coefficients ($K_0, K_1, ..., K_7$) such that the mixer downconverts RF signal from 2nd harmonic of f_{LO}. This is illustrated in Fig. 3.8a. Notice that the first alias term is now moved to -6th harmonic and is 9.5 dB lower relative to the fundamental (see Fig. 3.8b). This results in a receiver whose max operating frequency is now $2f_{LO} = 6GHz$, covering majority of frequency spectrum in use today. Similar schemes have been studied in [9, 22, 23] and is also used in this work to extend the operating frequency range of the receiver.



(a) (b)

Figure 3.8: Reconfigure baseband coefficients to downconvert RF signal from $2f_{LO}$ (a) Resulting complex sine wave , (b) Spectrum of the complex sine wave

3.3 LO Design

High linearity receivers require low phase noise LO to avoid increasing receiver noise figure due to reciprocal mixing. Phase noise of the LO $\mathcal{L}(\Delta f)$ can be determined using the following relation.

$$\mathcal{L}(\Delta f)\,[dBc/Hz] \approx BlockerNF\,[dB] - 174\,[dBm/Hz] - P_{blkr}\,[dBm]\,. \tag{3.27}$$

From (3.27) $\mathcal{L}(\Delta f)$ should be -172 dBc/Hz if the receiver noise figure is 10 dB in the presence of +8 dBm blocker (12 MHz offset). To meet this phase noise specification, the test chip uses shift register based divide-by-4 circuit shown in Fig. 3.9.

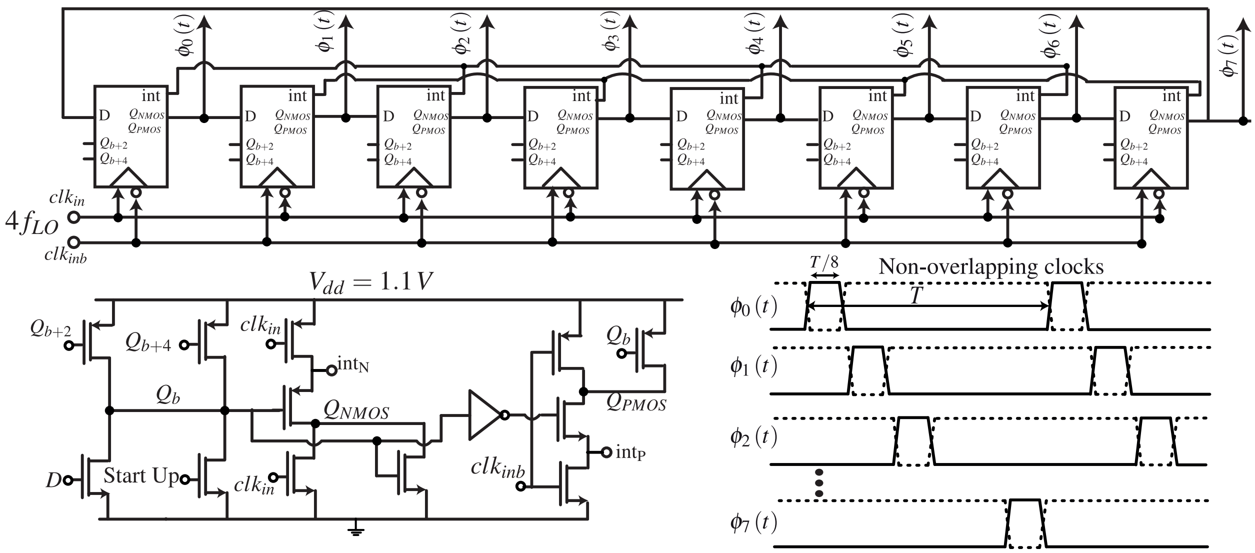
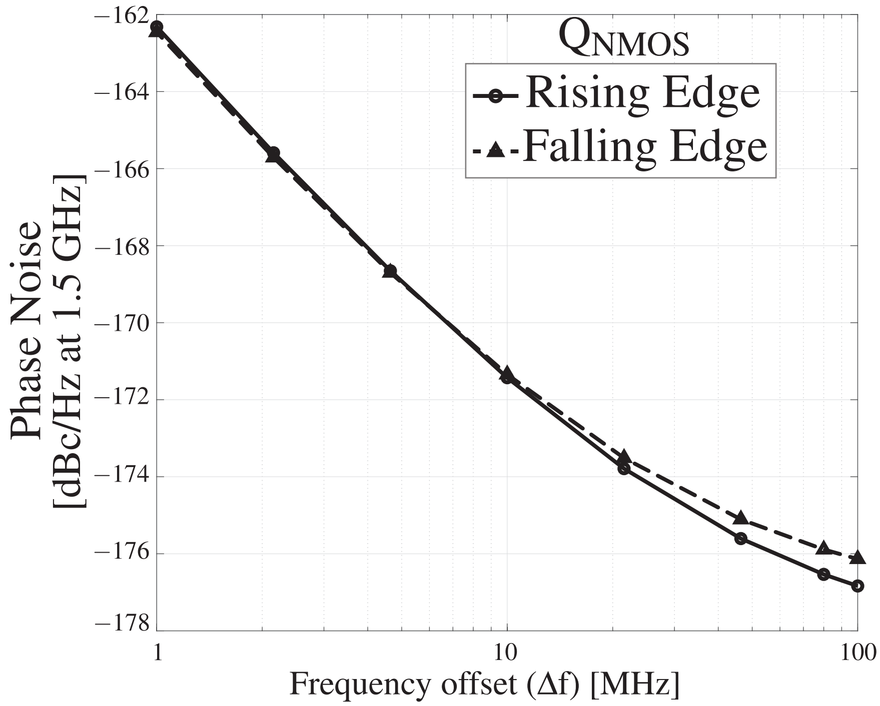
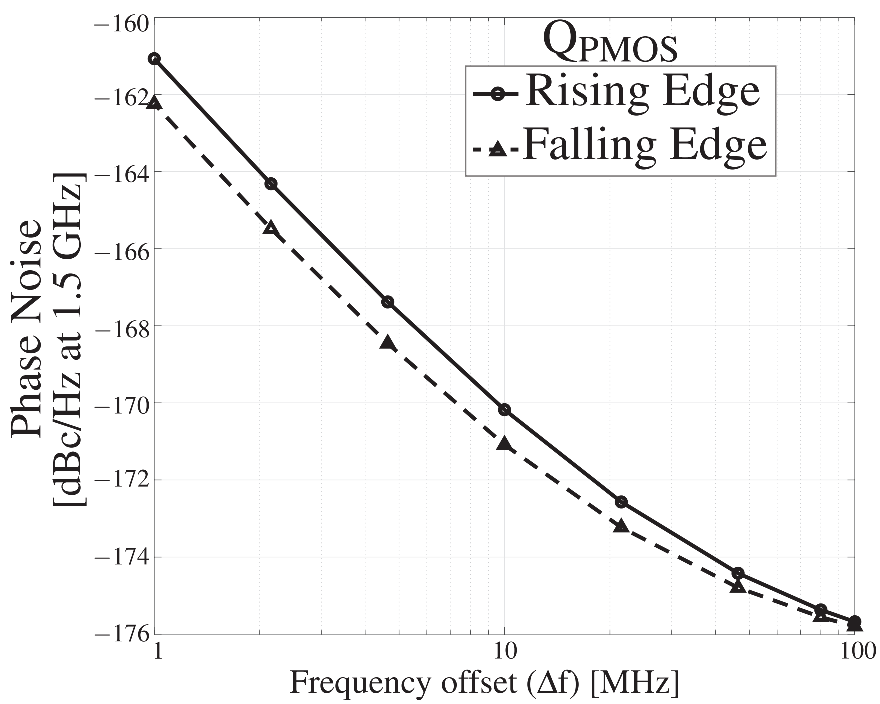


Figure 3.9: Shift register based divide-by-4.

Outputs of each register cell Q_{NMOS} and Q_{PMOS} are re-timed using clk_{in} and clk_{inb} resulting in low-phase noise LO driving CMOS mixer switches. Simulation plots in Fig. 3.10a and Fig. 3.10b show the phase noise profile of outputs Q_{NMOS} and Q_{PMOS}. Divider power consumption is proportional to the LO frequency, and is about 30mW at $f_{LO} = 1GHz$.



(a)



(b)

Figure 3.10: Phase noise at f_{LO}=1.5 GHz (a) Output Q_{NMOS} , (b) Output Q_{PMOS}

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3.4 Conclusion

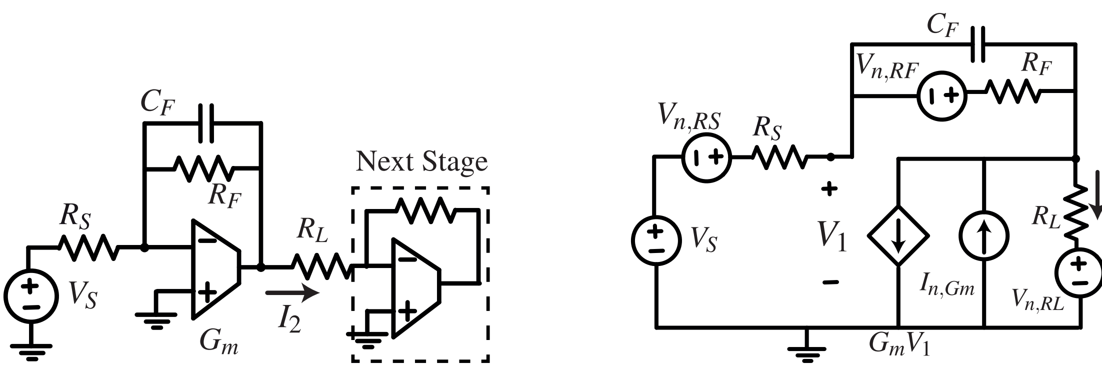
In this chapter EKV based FET model was used to analyze mixer switch nonlinearity. Expressions for IIP3 and P_{1dB} were found, which showed that increasing $\frac{R_s}{R_{on}}$ can be used to lower mixer switch distortion. Design of LO path was also described using a low phase noise divide-by-4 circuit (-172 dBc/Hz at 12MHz offset). Since the divider output frequency was limited to 3 GHz, it was shown that baseband weighting coefficients of the receiver can be reconfigured to downconvert wanted signals from $2f_{LO}$. As a result receiver maximum operating frequency can go up to 6 GHz.

CHAPTER 4

Transimpedance Amplifier Design

In a receiver TIA is used in the baseband section to amplify and isolate wanted signal from the rest. In this chapter we will look at a simple first-order TIA, and study its large signal behavior as well as its noise.

4.1 Noise Figure of TIA



(a) (b)

Figure 4.1: Transimpedance Amplifier (a) Schematic. (b) Circuit with noise sources identified

Fig. 4.1a shows a TIA with a voltage source V_S and resistance R_S at the input. Its output is connected to another TIA stage (e.g. a buffer or the next filtering stage). TIA output is a current I_2 flowing through R_L. Fig. 4.1b is a simplified schematic with noise sources explicitly shown in the network. Dissection theorem [24] can be used to calculate transfer functions from the noise sources in Fig.4.1b to the output of interest I_2 and are given below. For simplicity the transfer functions are evaluated at DC.

$$
\begin{aligned}
H_{n1} = \quad & \frac{I_2}{I_{n,Gm}} = \quad \frac{R_F + R_S}{G_m\, R_L\, R_S + R_F + R_L + R_S}\,, && \text{(4.1a)}\\
H_{n2} = \quad & \frac{I_2}{V_{n,RL}} = \quad -\frac{\left(1 + \frac{1}{G_m R_S}\right)}{R_L}\left(\frac{1}{1+\frac{1}{T}}\right)\,, && \text{(4.1b)}\\
H_{n3} = \quad & \frac{I_2}{V_{n,RF}} = \quad \frac{\left(1 + \frac{1}{G_m R_S}\right)}{R_L}\left(\frac{1}{1+\frac{1}{T}}\right)\,, && \text{(4.1c)}\\
T = \ & \text{Loop Gain} = \frac{G_m\, R_L\, R_S}{R_L + R_F + R_S}\,. && \text{(4.1d)}
\end{aligned}
$$

Power Spectral Density (PSD) of the noise sources in Fig. are

$$S_{I_{n,Gm}} = 4kT\gamma G_m\,, \tag{4.2a}$$

$$S_{V_{n,RL}} = 4kTR_L\,, \tag{4.2b}$$

$$S_{V_{n,RF}} = 4kTR_F\,. \tag{4.2c}$$

$$S_{V_{n,RS}} = 4kTR_S\,. \tag{4.2d}$$

$k = 1.38 \times 10^{-23}\ J/K$ is the Boltzmann constant, and γ is the noise coefficient of the TIA G_m.

The signal gain ($\frac{I_2}{V_S}$) is

$$A_v = \frac{I_2}{V_S} = -\frac{R_F}{R_S\, R_L}\frac{\left(1 - \frac{1}{G_m R_F}\right)}{\left(\frac{1}{1+\frac{1}{T}}\right)}\,. \tag{4.3}$$

Noise Factor (F) of the TIA can be found using the noise transfer functions from (4.1), noise PSD from (4.2) and the signal gain (4.3) and is given as

$$
\begin{aligned}
F = 1\ + & \frac{\gamma}{G_m R_S}\left(1 + \frac{R_S}{R_F}\right)^2\left(\frac{1}{1 - \frac{1}{G_m R_F}}\right)^2 \\
& + \frac{R_L R_S}{R_F^2}\left(\frac{1 + \frac{1}{G_m R_S}}{1 - \frac{1}{G_m R_F}}\right)^2 + \frac{R_S}{R_F}\left(\frac{1 + \frac{1}{G_m R_S}}{1 - \frac{1}{G_m R_F}}\right)^2\,.
\end{aligned} \tag{4.4}
$$

(4.4) can be simplified by assuming $G_m R_S \gg 1$ and $G_m R_F \gg 1$

$$F \approx 1\ + \frac{\gamma}{G_m R_S}\left(1 + \frac{R_S}{R_F}\right)^2 + \frac{R_L R_S}{R_F^2} + \frac{R_S}{R_F}\,. \tag{4.5}$$

Lowering Noise Factor of TIA

(4.5) gives design insights to lower noise factor F of TIA. Let's go through them one by one.

- R_F appears in the denominator of terms in (4.5). Therefore a larger value of R_F brings down F. It should be noticed that a higher R_F also results in higher signal gain (from (4.3)) and that can result in compression at TIA output in the presence of blockers.

- R_L appears in the numerator of one of the terms in (4.5) and therefore should be minimized to obtain a low noise factor. It should be noted from (4.1d) that TIA loop gain depends on R_L too, and loop gain $\gg 1$ to achieve linearity benefits of feedback.

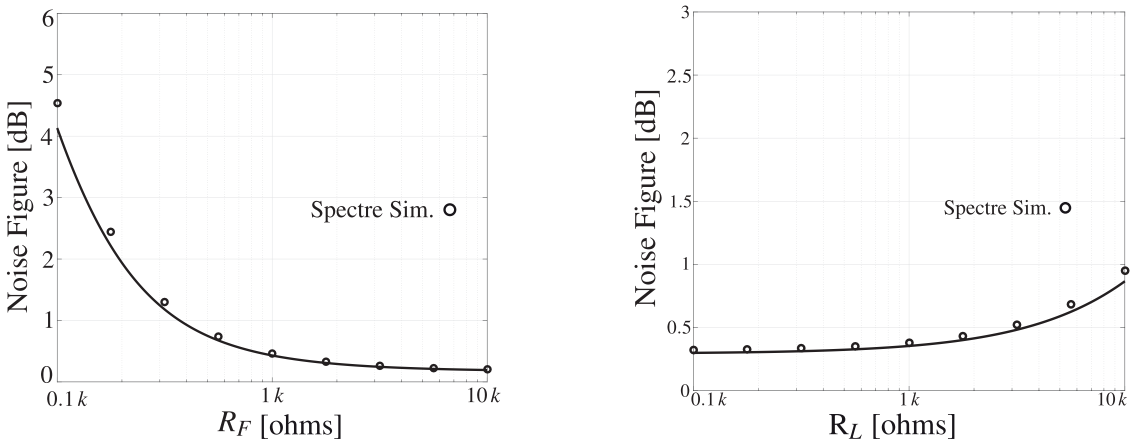
- G_m should be maximized to lower noise factor of the TIA, and to maintain loop gain $\gg 1$. Also note that input resistance of the TIA is $\frac{1}{G_m}\left(1+\frac{R_F}{R_L}\right)$. Keeping the input resistance low helps maintain good linearity of circuit blocks preceding TIA (e.g. RF transconductor or mixer) by ensuring a good virtual ground at TIA input. However large TIA G_m also results in high power consumption.

Fig. 4.2a and 4.2b show simulated noise figure ($10log(F)$) of TIA and compare it against the value obtained from (4.5). For both simulations $R_S = 50\,\Omega$, $G_m = 500\,mS$, and $\gamma = 1$. From the plots it can be concluded that (4.5) correctly predicts noise figure of TIA.

4.2 Large Signal Performance of TIA

The choice of G_m used in a TIA determines its large signal behavior. Many receivers [8, 25] use an inverter-based G_m in the TIA (as shown in Fig. 4.3a).The main reasons for this choice are high $\frac{g_m}{I_d}$ efficiency for an inverter, and ease of design. Alternatively, two stage opAmp can be used but it has potential common-mode instability as explained in [25] especially at low supply voltages. Therefore in this chapter we will look at the large signal performance of the TIA that employs an inverter-based G_m.

First, let's take a look at the small-signal transfer functions $|G_{2S}(j\omega)| = |\frac{V_2}{V_S}(j\omega)|$ and $|G_{1S}(j\omega)| = |\frac{V_1}{V_S}(j\omega)|$ (shown in Fig. 4.3b). Notice that $|G_{1S}(j\omega)| \ll |G_{2S}(j\omega)|$, therefore



(a) (b)

Figure 4.2: Noise Figure of TIA when (a) R_F is varied, (b) R_L is varied.

the signal swing at V_1 will be much smaller than that at V_2. In other words, compression will happen due to clipping at node V_2 rather than at node V_1. This can be shown with a clipping characteristic (see Fig. 4.4) where $\hat{V_S}$ and $\hat{V_2}$ represent the amplitude of voltages at the onset of clipping.

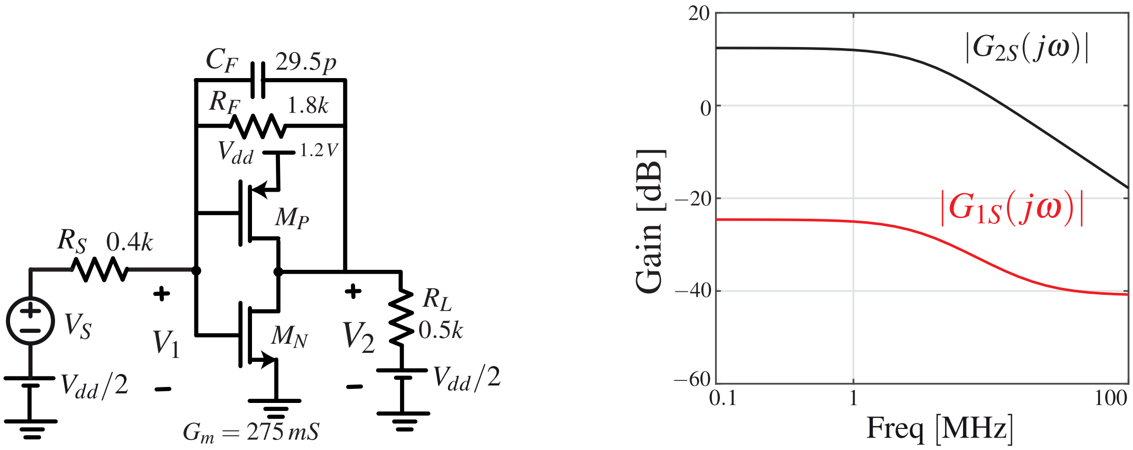
The next step is to figure out the value of $\hat{V_2}$. Clipping of signal happens when M_n (or M_p) enters triode. According to EKV model [10] this occurs when the drain potential of M_n ($\frac{V_{dd}}{2} - \hat{V_2}$) becomes equal to its pinch voltage $V_P = \frac{1}{n}\left(\frac{V_{dd}}{2} + \hat{V_1} - V_{t0}\right)$. Since V_1 is a virtual ground node with very small signal swing, it can be assumed to be sitting at a fixed potential $\frac{V_{dd}}{2}$ (i.e. $\hat{V_1} \approx 0$). Hence

$$
\begin{aligned}
V_P &= \frac{V_{dd}}{2} - \hat{V_2}\,, \\
\hat{V_2} &= \frac{V_{dd}}{2}\left(1 - \frac{1}{n}\right) + \frac{V_{t0}}{n}\,. \qquad (4.6)
\end{aligned}
$$

$V_{dd} = 1.2\,V$ is the supply voltage of the inverter-based TIA G_m, $n = 1.1$ in 16nm FETs and $V_{t0} = 0.45\,V$ is the threshold voltage of NMOS (same value for PMOS). $\hat{V_S}$ can be found by dividing $\hat{V_2}$ by the small-signal gain $|G_{2S}(j\omega)|$. Mathematically,

$$\hat{V_S} = \frac{\hat{V_2}}{|G_{2S}(j\omega)|}\,, \qquad (4.7a)$$

$$\hat{V_S} \approx \frac{V_{t0}}{|G_{2S}(j\omega)|}\,. \qquad (4.7b)$$



(a) (b)

Figure 4.3: TIA with inverter based G_m (a) Schematic, (b) Small signal gain.

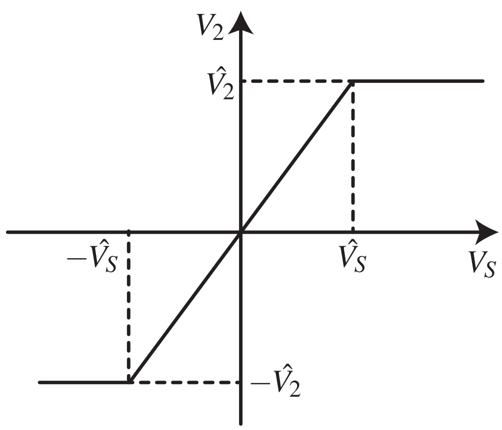


Figure 4.4: Clipping characteristic of TIA at node V_2

In terms of available power from source V_S, input-referred compression point is

$$P_a = \frac{\hat{V_S}^2}{8R_S} \approx \frac{V_{t0}^2}{8|G_{2S}(j\omega)|^2 R_S}\,. \tag{4.8}$$

Fig. 4.5a shows the simulated gain compression of the TIA as a function of the blocker frequency using 16nm BSIM-CMG models. For comparison the value obtained from (4.8) is also show in the Fig. 4.5a as a solid line and there is good agreement between the two curves.

Notice that according to (4.8), for a given source driving the TIA and a certain filtering profile of TIA (i.e. $|G_{2S}(j\omega)|$), input-referred compression point is mostly independent of the

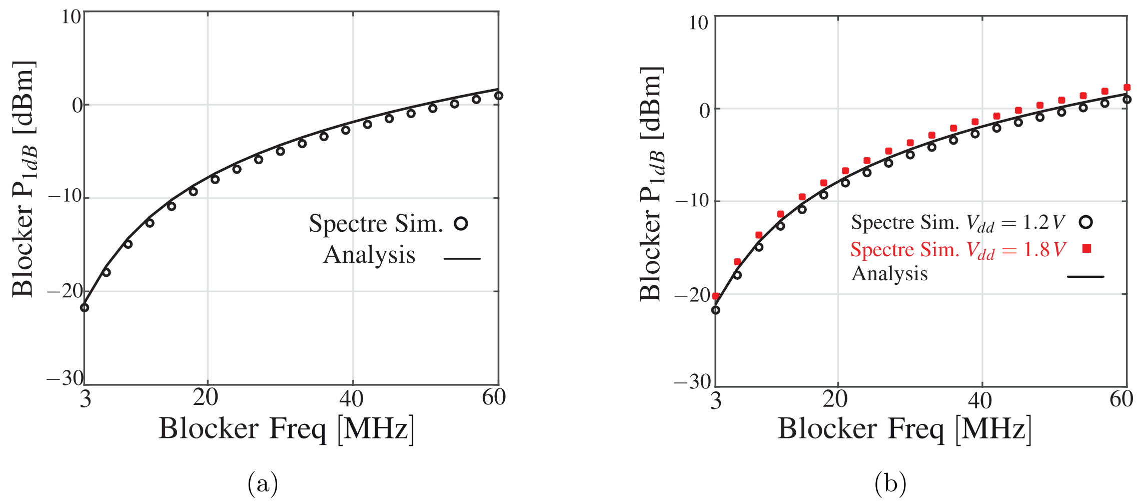


Figure 4.5: Gain compression of TIA as a function of blocker frequency (a) when $V_{dd} = 1.2V$, (b) when $V_{dd} = 1.8\,V$.

supply voltage V_{dd} for the inverter based architecture. This is illustrated in Fig. 4.5b that compares the gain compression of TIA with $V_{dd} = 1.2V$ vs raised supply voltage $V_{dd} = 1.8V$. Notice the two are within 1.3 dB of each other.

4.3 Source Follower and Inverter based TIA G_m

It has been shown in the previous section that the compression point of inverter based TIA is mainly a function of threshold voltage V_{t0} of its FETs, and increasing its supply voltage V_{dd} has very little impact on the compression point. The question now arises what design changes can be made to break this constraint.

According to (4.8), compression point can be increased by increasing the threshold voltage V_{t0} of the FETs. One way to accomplish this goal is by inserting offset voltage sources V_{bn} and V_{bp} at the gate of devices M_n and M_p (see Fig. 4.6a). This effectively increases V_{t0} of these FETs and ultimately results in higher compression point of the TIA. The value of the offset voltage is selected so that the pinch-off voltage V_{Pn} of M_n is about $0.1\,V$. This implies that $\hat{V_2}$ can be $(\frac{V_{dd}}{2} - V_P)$.

The offset voltages can be implemented by source followers as shown in Fig. 4.6b. These

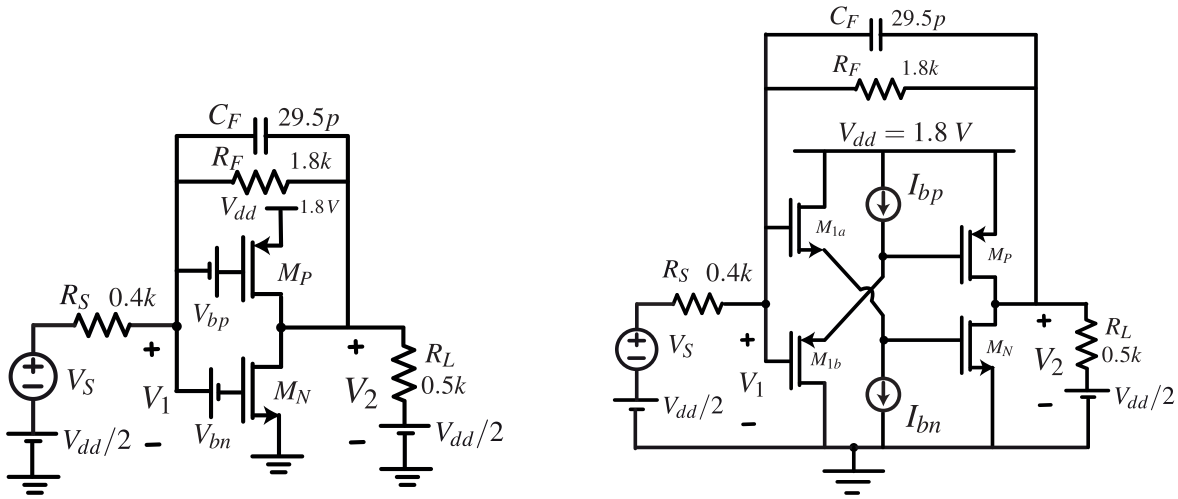


Figure 4.6: Improving TIA input-referred compression point (a) using offset voltages V_{bn} and V_{bp}, (b) Implementation of offset voltages using source followers.

source followers act as level-shifters, and bias the gate of M$_n$ at $(\frac{V_{dd}}{2} - V_{GS,1a})$. The amount of shift can be controlled by adjusting the bias current I_{bn} through M$_{1a}$. Fig. 4.7 shows the input-referred compression of the TIA using source followers with inverter as the TIA G_m in 16nm FETs. Compared to the inverter based G_m P$_{1dB}$ is about 4 dB higher.

4.3.1 Noise analysis of Source Follower and Inverter based TIA G_m

In case of simple inverter based G_m (shown in Fig. 4.8a), PSD of the equivalent noise source v_n is given as

$$S_{vn} = 4kT\frac{\gamma}{G_m}\ , \tag{4.9}$$

where G_m represents the overall transconductance of the inverter. Assuming M$_n$ and M$_p$ have equal transconductances (i.e $g_{mn} = g_{mp} = g_m$), $G_m = 2g_m$.

Let's now consider the source follower and inverter based G_m shown in Fig 4.8b. Assuming that $g_{m1a} = g_{m1b}$, and $g_{m1c} = g_{m1d}$, PSD of the noise source v_n is given as

$$S_{vn} = 4kT\frac{\gamma}{G_m}\left(1 + \frac{g_{mn}}{g_{m1a}}\left(1 + \frac{g_{m1c}}{g_{m1a}}\right)\right)\ . \tag{4.10}$$

(4.10) shows that the source follower inverter based G_m is more noisier than that of a simple

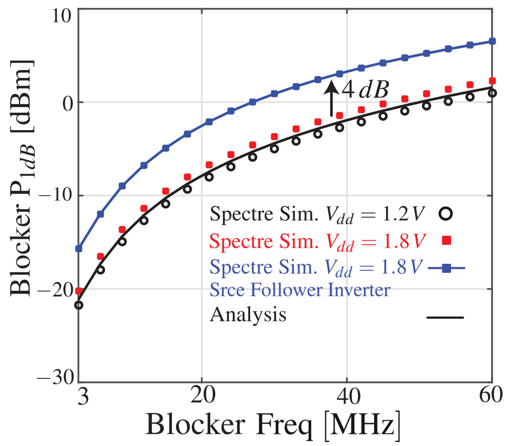


Figure 4.7: Gain compression of the TIA as a function of the blocker frequency using source follower inverter based G_m in 16nm technology.

inverter based G_m. Thus there exists a tradeoff between the higher compression point of the TIA and its overall noise factor when using source follower inverter based G_m.

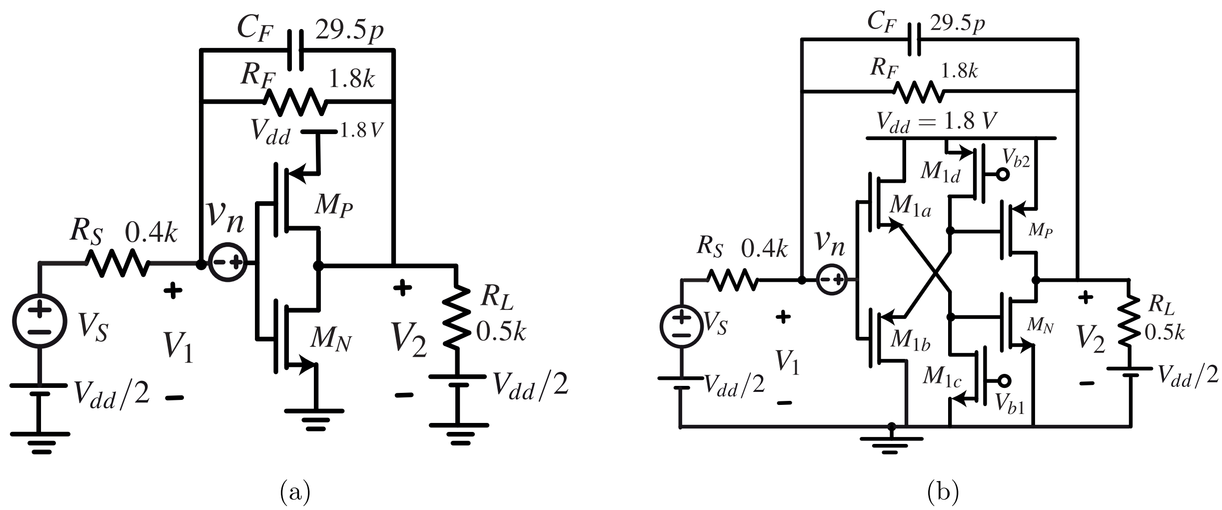


Figure 4.8: Noise voltage source v_n (a) Inverter, (b) Source follower and Inverter.

Noise Optimization

Input noise PSD S_{vn} can be optimized by making $\frac{g_{m1c}}{g_{m1a}} < 1$ and $\frac{g_{mn}}{g_{m1a}} < 1$. In this work $\frac{g_{m1c}}{g_{m1a}} = \frac{1}{2}$ and is achieved by reducing $\left(\frac{W}{L}\right)_{1c}$ relative to $\left(\frac{W}{L}\right)_{1a}$. Additionally, $\frac{g_{mn}}{g_{m1a}} < 1$ by burning more current in the source followers relative to the output inverters (assuming

$V_{Pn} = V_{P1a}$).

4.3.2 Pseudo-differential Implementation

Fig. 4.9a shows a pseudo differential implementation of the TIA G_m based on source follower inverter architecture. A common-mode feedback (CMFB) circuit is connected at its output. The CMFB circuit provides a large differential-mode impedance, which preserves the differential gain. However it provides a low common-mode impedance which in turn lowers the common-mode gain of the TIA G_m.

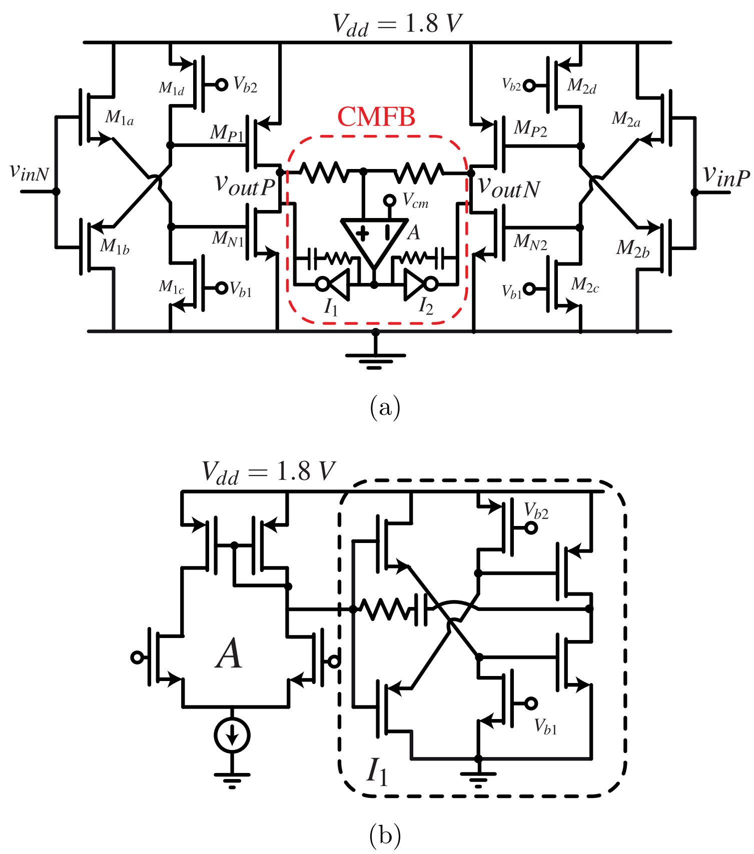


Figure 4.9: (a) Pseudo-differential Realization, (b) Details of the CMFB Network.

4.3.3 How to generate bias voltages V_{b1} and V_{b2} ?

Bias voltages V_{b1} for M_{1c} and V_{b2} for M_{1d} are generated using a replica bias arrangement as shown in Fig 4.10.

The bias scheme uses a replica cell as shown in Fig 4.10. I_{ref} sets up a reference voltage $V_{g,refN}$, and the opAmp A changes V_{b1} until V_{gN} becomes equal to $V_{g,refN}$. This V_{b1} is then fed to the TIA G_m. C_1 ensures that the feedback loop stays stable with phase margin $\geq 60°$. A complementary version of the loop is used to generate V_{b2} for M_{1d}.

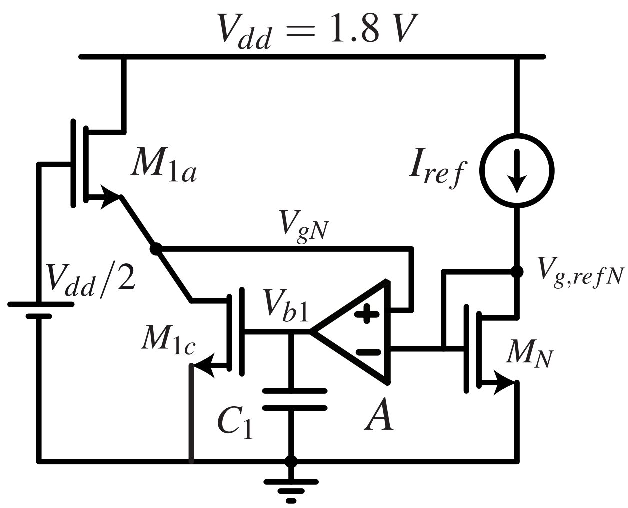


Figure 4.10: Bias network to generate V_{b1} for the Source follower Inverter based TIA G_m.

4.4 Conclusion

This chapter looked at the design of TIA for use in the baseband section of the receiver. Noise factor of TIA as well as its large-signal operation was analyzed to understand the trade-offs involved. It was shown that using source follower inverter based TIA G_m gives higher compression point but it also results in higher input noise. Pseudo-differential realization of source follower inverter based TIA G_m along with CMFB network and biasing circuitry were also described in this chapter.

CHAPTER 5

Receiver Architecture and Measurement Results

This chapter describes architecture of the receiver implemented in 16nm FinFET CMOS technology. It also explains the different operating modes of the receiver. Measured results of the prototype receiver are also included this chapter.

5.1 Receiver Architecture

Block diagram representation of the receiver architecture implemented in 16nm CMOS is shown in Fig. 5.1. RF transconductor G_m in the auxiliary path is realized using the composite G_m architecture studied in chapter 2. It uses thick oxide FETs with channel length $0.135\mu m$ because G_m experiences full blocker swing ($\approx 1.6V_{pp}$) at its input node v_2. Bias voltages needed for the composite G_m are generated using 6 bit resistor DACs (digital-to-analog converters). The output of the composite G_m is directly connected to the auxiliary path passive mixer that uses CMOS switches ($R_{on} \approx 3\,\Omega$). R_{on} and the up-converted auxiliary path TIA impedance together present about $6\,\Omega$ impedance at the composite G_m output.

Impedance matching to the antenna is done by series combination of padding resistor R_2, main path CMOS mixer switches ($R_{on} \approx 6\,\Omega$), and the upconverted main path TIA impedance. R_2 reduces the voltage swing appearing across the main path mixer which in turn avoids compression in the main path.

The baseband filtering section is comprised of 1^{st} order TIAs in the main and auxiliary paths followed by a 2^{nd} order biquad filter. TIA outputs are weighted and summed in current domain using programmable resistors. The resulting current is then fed to the biquad filter [26]. The cascade connection of TIA and biquad results in overall 3^{rd} order Butterworth response at the final output v_{06}. Programmable passive components in TIA and biquad set the baseband bandwidth to 3 MHz. Active elements in TIA and biquad are implemented using the source follower and inverter based architecture studied in chapter 4. Output nodes of TIA and biquad filter provide rail-to-rail swing capability to maximize P_{1dB} of the receiver.

A divide-by-4 circuit, based on shift register approach, generates the required eight-phase non-overlapping clock pulses. Since the mixer uses CMOS switches, each register cell in the divider generates complementary clock swings. The clock waveform is level-shifted to mid-rail, and then fed to the gate of mixer switches. The maximum output frequency of the divider is around 3 GHz. However RF signal can be downconverted from $2f_{LO}$ by reconfiguring baseband weighting resistors which in turn extends the receiver operating frequency to 6 GHz.

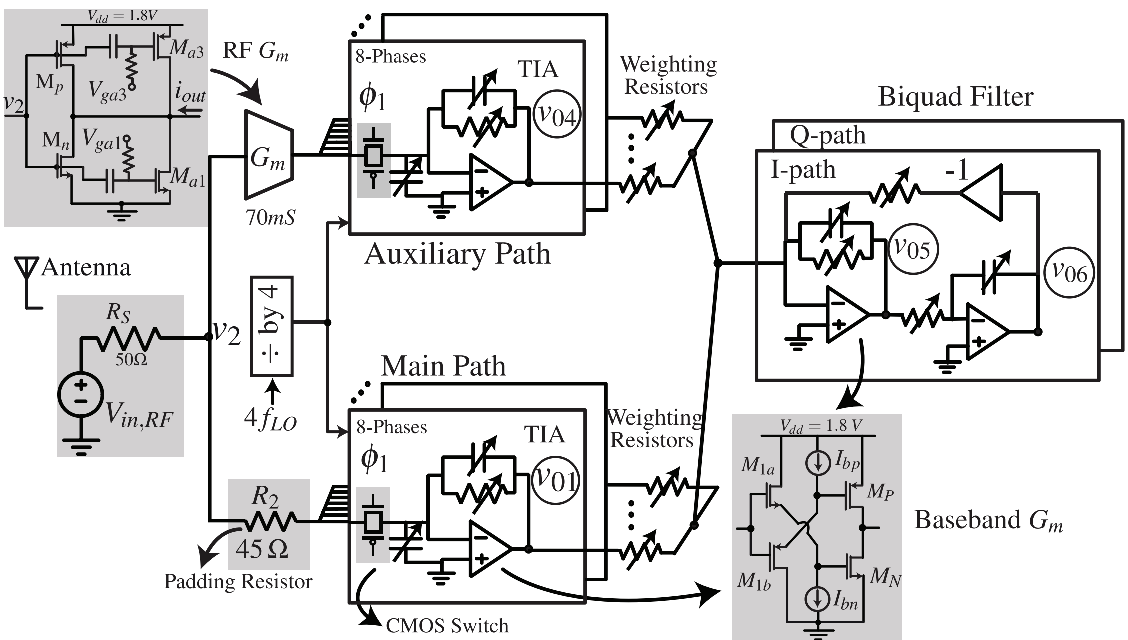


Figure 5.1: Receiver architecture.

5.2 Receiver Operating Modes

The prototype receiver can be programmed to operate in three modes.

- High-linearity mode (intended for close-in +12 dBm blockers)

- Low-noise mode (suitable for far-away blockers)
  - Noise-cancellation OFF (receiver can withstand +12 dBm blockers at 80MHz offset from wanted signal, receiver noise figure is 6.3 dB)
  - Noise-cancellation ON (receiver can withstand -0.5 dBm blockers at 80MHz offset from wanted signal, receiver noise figure is 3.6 dB)

5.2.1 High-linearity mode

In this mode, only main path of the receiver is active and gain of TIA and biquad is reduced to avoid compression from large close-in blockers. Fig. 5.2 shows receiver operation in this mode, and key performance metrics are given in table 5.1

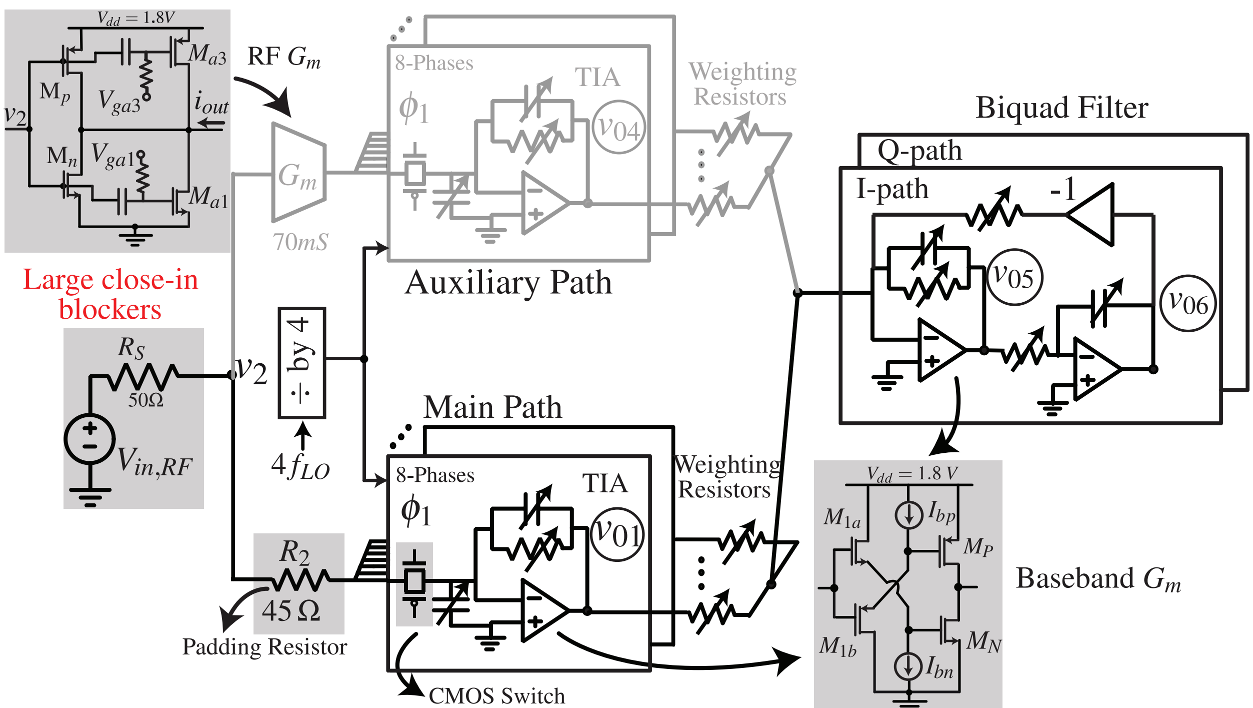


Figure 5.2: Receiver operating in high-linearity mode.

Table 5.1: Receiver operation summary in high-linearity mode

Conv. Gain [dB]	NF [dB]	Blocker P_{1dB} @ 12 MHz offset	Blocker P_{1dB} @ 80 MHz offset	Power [mW]
43	8	+7.2 dBm	+12 dBm	112

5.2.2 Low-noise mode (noise-cancellation OFF)

In this mode, only main path of the receiver is active and gain of TIA and biquad is higher than in the high-linearity mode. Because of this input-referred noise contribution of biquad is lower and overall receiver noise figure is 6.3 dB. This mode is suitable when the blockers are located at >80 MHz from wanted signal . Fig. 5.3 shows receiver operation in this mode, and key performance metrics are given in table 5.2

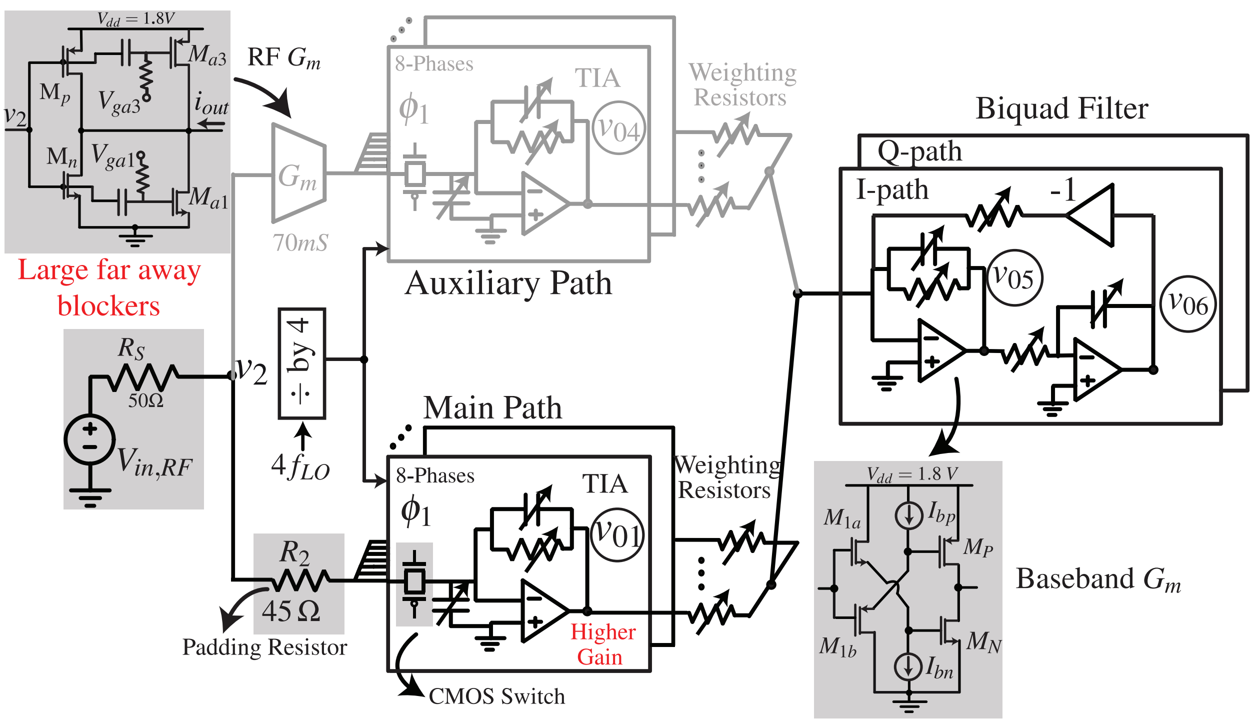


Figure 5.3: Receiver operating mode: Low-noise (Noise cancellation OFF)

Table 5.2: Receiver operation summary in low-noise mode (noise-cancellation OFF)

Conv. Gain [dB]	**NF [dB]**	**Blocker P_{1dB} @ 12 MHz offset**	**Blocker P_{1dB} @ 80 MHz offset**	**Power [mW]**
50	6.3	-11 dBm	+12 dBm	79.9

5.2.3 Low-noise mode (noise-cancellation ON)

In this mode, both main and auxiliary paths of the receiver are active and gain of TIA and biquad are at the highest setting. Overall receiver noise figure is 3.6 dB. This mode is suitable for moderate level blockers located at >80 MHz from wanted signal . Fig. 5.4 shows receiver operation in this mode, and key performance metrics are given in table 5.3

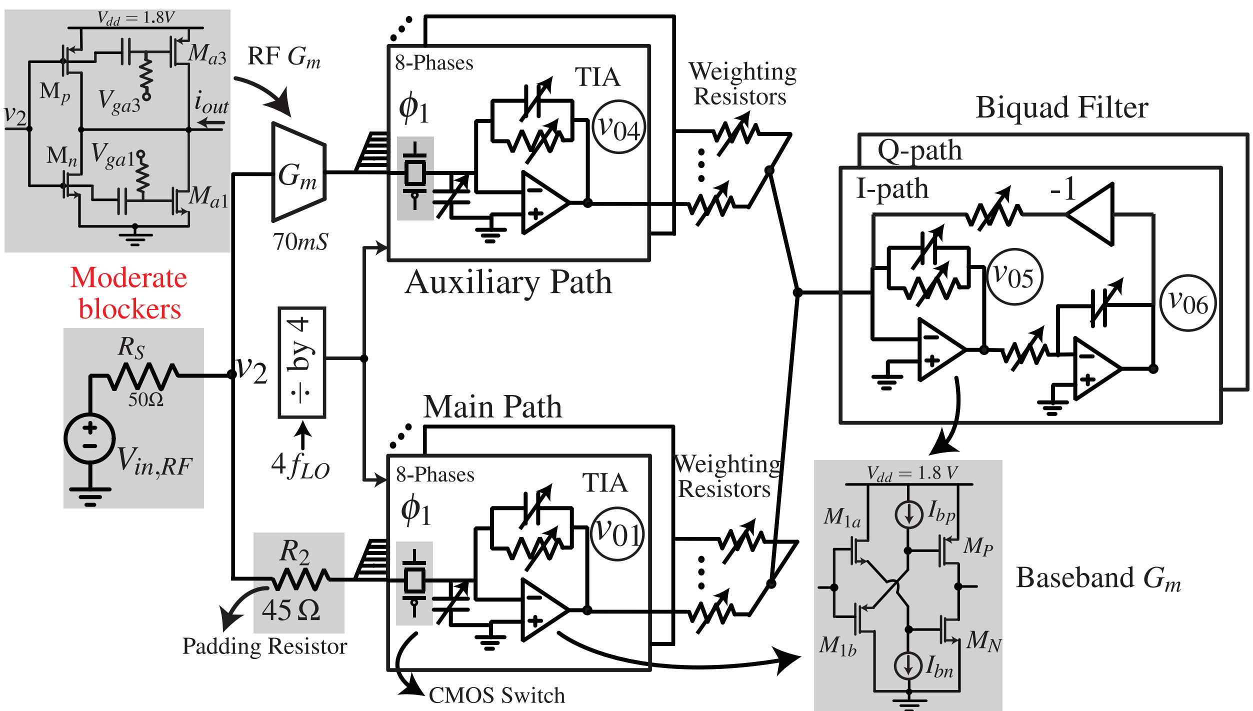


Figure 5.4: Receiver operating mode: Low-noise (Noise cancellation ON)

Table 5.3: Receiver operation summary in low-noise mode (noise-cancellation ON)

Conv. Gain [dB]	**NF [dB]**	**Blocker P_{1dB} @ 12 MHz offset**	**Blocker P_{1dB} @ 80 MHz offset**	**Power [mW]**
55.6	3.6	-12 dBm	-0.5 dBm	148.3

5.3 Measurement Results

A test chip was fabricated in 16nm FinFET CMOS process. Die photograph is shown in Fig. 5.5 and its active area is 2.64 mm^2. Input return loss (s_{11}) was about -9 dB at 1500 MHz, a few dB worse than expected. Simulations confirmed that the additional capacitance from thick oxide ESD and flip-chip bump at the RF input of the test chip was the cause of higher input return loss. Off-chip inductor (2.9 nH) was added in series with the RF input to reduce s_{11} to -11.5 dB. Fig. 5.6 compares the measured and simulated s_{11} before and after adding the matching inductor.

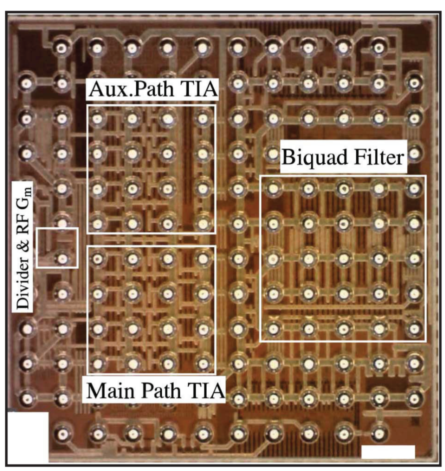


Figure 5.5: Die photograph of test chip.

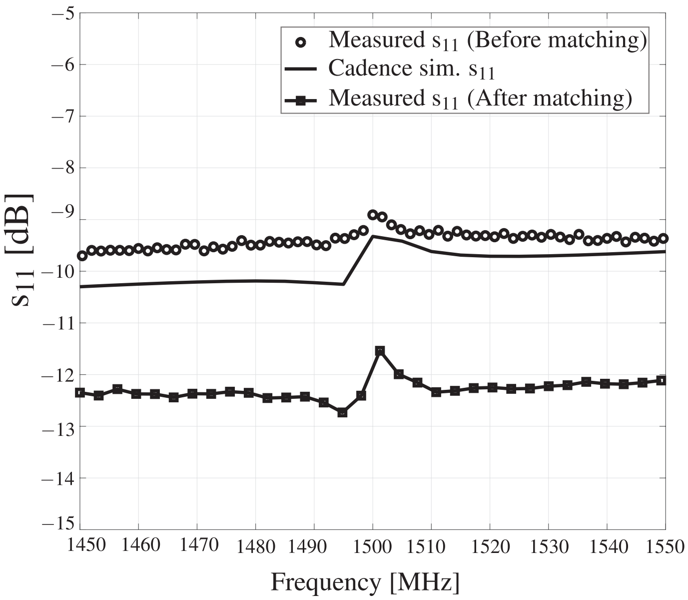


Figure 5.6: Measured s_{11} at f_{LO}=1.5 GHz, before and after matching.

5.3.1 Receiver filtering profile and noise figure

Fig. 5.7 shows the receiver selectivity when it is tuned at 1.5 GHz (high-linearity mode). RF bandwidth (-3 dB) of the receiver is about 6 MHz with a 3rd-order filtering response resulting in 61 dB of selectivity at 30MHz offset.

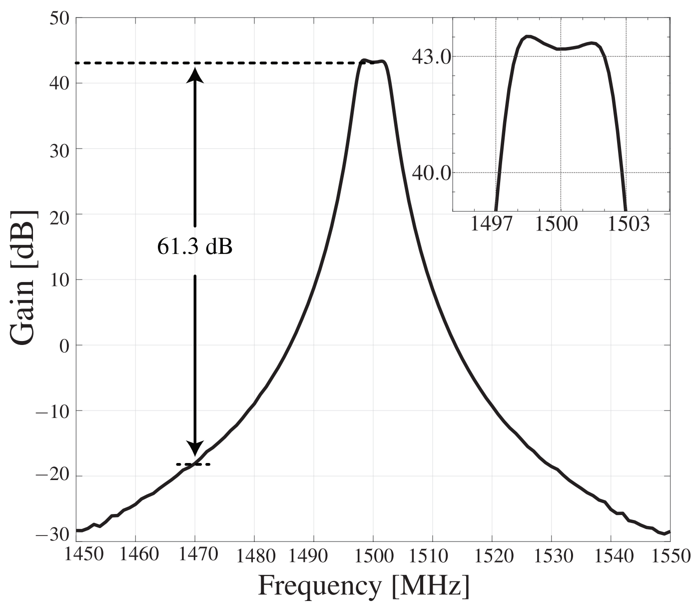


Figure 5.7: Measured selectivity of receiver at f_{LO}=1.5 GHz.

Receiver gain and small-signal across the full LO operating range is shown in Fig. 5.8.

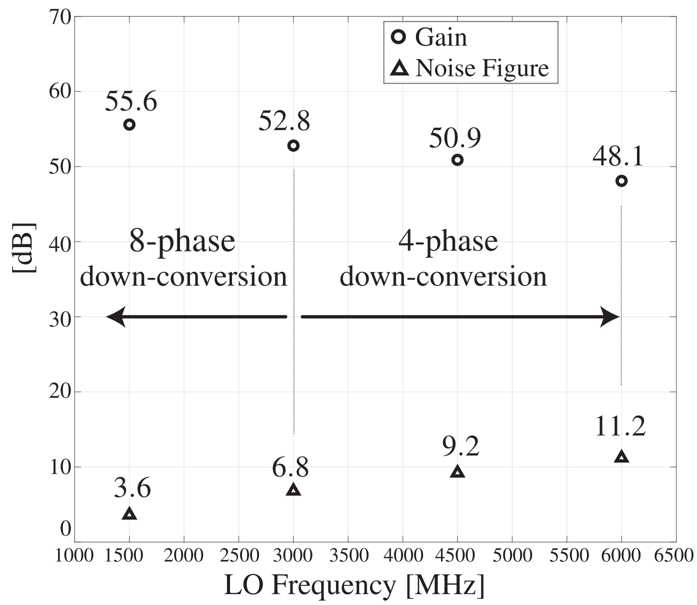


Figure 5.8: Measured gain and DSB noise figure vs LO frequency.

5.3.2 Receiver Input referred 1dB Compression Point (P_{1dB})

Receiver input-referred 1dB compression point (P_{1dB}) vs blocker offset is shown in Fig. 5.9. In high-linearity mode, receiver P_{1dB} is limited by gain compression of the TIA output when blocker is located close to the edge of signal band and P_{1dB} increases rapidly as the blocker moves farther away from band-edge. For blockers >24 MHz, receiver P_{1dB} reaches its maximum value of +12 dBm limited by distortion of main path mixer switches.

When receiver is operating in low-noise mode (noise cancellation OFF), its P_{1dB} for close-in blockers is limited by gain compression at TIA output. For blocker offset >80 MHz, receiver P_{1dB} becomes+12 dBm limited by distortion of main path mixer switches. With noise cancellation ON, RF G_m limits receiver P_{1dB} to -0.5 dBm.

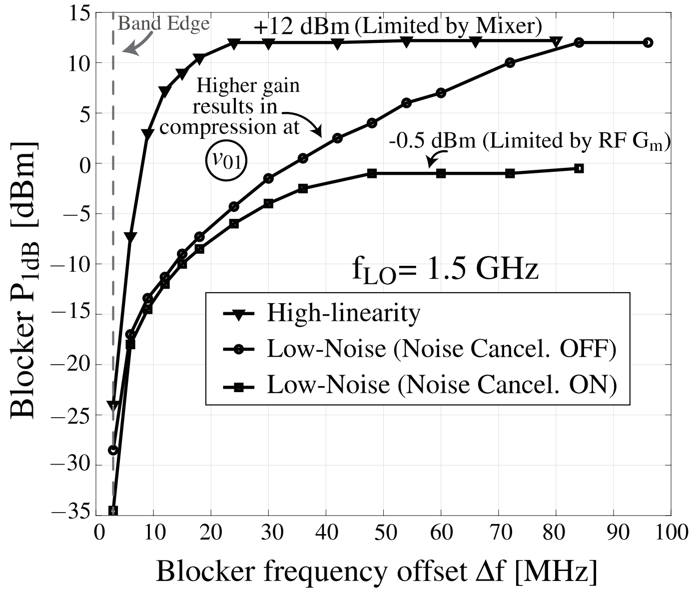


Figure 5.9: Measured 1-dB compression point P_{1dB} (dBm) vs blocker offset frequency; different receiver operating modes at f_{LO}=1.5 GHz.

5.3.3 Receiver noise figure in the presence of blockers

Fig. 5.10 shows receiver noise figure as a function of continuous wave (CW) blocker power measured at different blocker offsets and operating modes. In high-linearity mode, noise figure is 8 dB (for very low blocker level at 20 MHz offset). As the blocker power is increased, noise figure rises due to reciprocal mixing of LO phase noise and becomes 12.7 dB for + 10dBm blocker.

When receiver is operating in low-noise mode (noise cancellation OFF), its noise figure is 6.3 dB (for very low CW blocker level at 80 MHz offset). As the blocker power is increased, noise figure rises to 8.9 dB for +10dBm blocker due to reciprocal mixing of LO phase noise. In low-noise mode (noise cancellation ON) noise figure starts off at 3.6 dB (for very low blocker level at 80 MHz offset) and then rapidly increases for blocker >0 dBm due to compression of RF G_m.

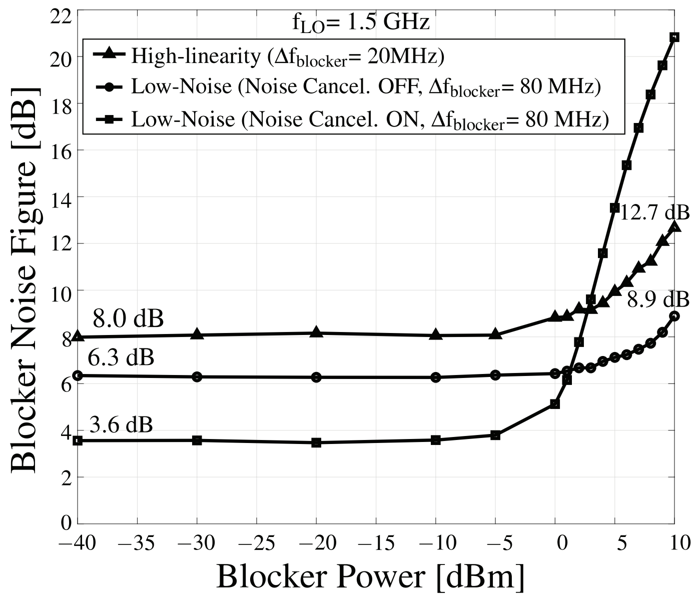


Figure 5.10: Measured noise figure versus blocker power at different blocker offsets and receiver operating modes (f_{LO}=1.5 GHz).

5.3.4 Receiver IIP2 and IIP3

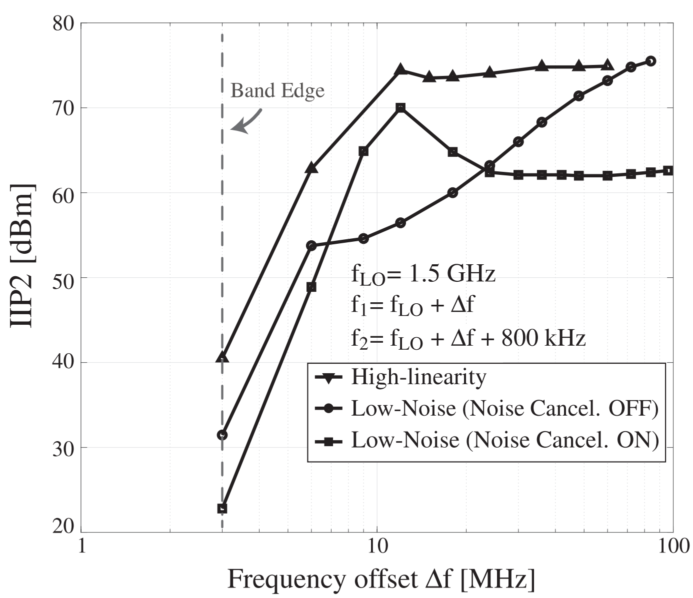


Figure 5.11: Measured IIP2 vs.two-tone offset for different receiver operating modes (f_{LO}=1.5 GHz).

Fig. 5.11 shows receiver IIP2 vs two-tone offset in different operating modes of receiver. In high-linearity mode, out-of-band (OOB) IIP2 is + 74dBm in high-linearity mode. In low-noise mode (noise cancellation OFF) OOB IIP2 is limited by the high gain of TIA for two-tone offset <60 MHz, eventually reaching + 74 dBm at higher offsets. When the receiver is operating in low-noise mode (noise cancellation ON) OOB IIP2 is limited by RF G_m to +62 dBm.

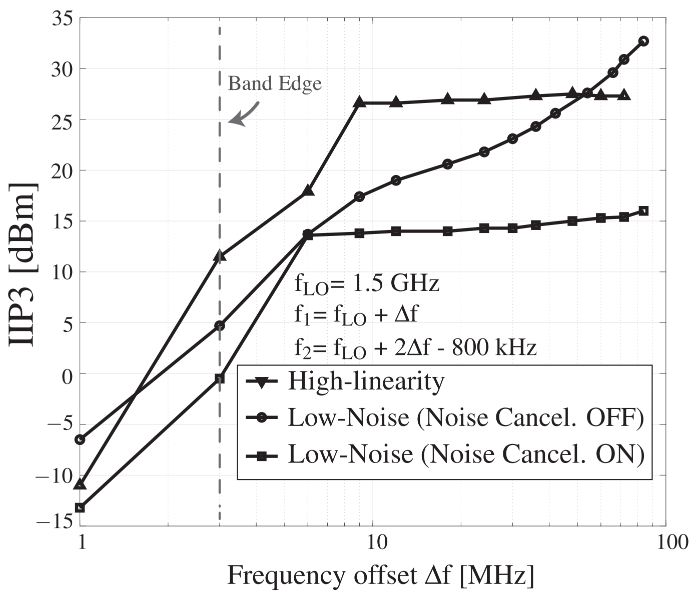


Figure 5.12: Measured IIP3 vs.two-tone offset for different receiver operating modes (f_{LO}=1.5 GHz).

Fig. 5.12 shows receiver IIP3 vs two-tone offset in different operating modes of receiver. In high-linearity mode, out-of-band (OOB) IIP3 is +26.6dBm in high-linearity mode limited by mixer switches in the main path. In low-noise mode (noise cancellation OFF) OOB IIP3 is limited by the high gain of TIA for two-tone offset <50 MHz, eventually reaching + 32.7 dBm at higher offsets. When the receiver is operating in low-noise mode (noise cancellation ON) OOB IIP3 is limited by RF G_m to +15 dBm.

5.4 Comparison with prior art

Table 5.4 compares this work with other recently published blocker tolerant receivers. Its linearity is comparable to prior art, but it rejects downconversion of unwanted channels at 3rd and 5th harmonic of the LO due to 8-phase mixing. With a single-ended RF input, it also achieves better blocker noise figure than similar receivers.

Table 5.4: Prototype receiver comparison with recently published blocker tolerant receivers

	[27]	**[28]**	**[7]**	**This Work**
Architecture	N-path + DT Filtering	FA with time interleaving	Mixer-1st with positive cap feedback	FTNC Rx
Technology	40 nm CMOS	65 nm CMOS	45 nm SOI	16 nm CMOS
RF Input	Differential	Differential	Differential	Single-ended
RF Frequency [MHz]	100-700	100-1000	200-8000	100-6000
Gain [dB]	40	23	20	42-55*
Channel BW ** [MHz]	6.4-9.6	2.4-40	20	6
3rd/5th Harmonic Rejection [dB]	66 / 73 (cal)	No	No	41.7 / 47.3 (cal)
Blocker P_{1dB} [dBm]	+15 (Δf_B=4.7×Ch. BW)	+13 (Δf_B=4×Ch. BW)	+12 (Δf_B=4×Ch. BW)	+12 (Δf_B=4×Ch. BW)
+10 dBm Blocker NF [dB]	> 12 (Δf_B=30 MHz)	20 (Δf_B=20 MHz)	>10.3 (Δf_B=80 MHz)	12.7†(Δf_B=20 MHz) 8.9‡(Δf_B=80 MHz)
OOB IIP3 [dBm]	+24 (Δf_B=4.7×Ch. BW)	+21 (Δf_B=1.2×Ch. BW)	+39 (Δf_B=4×Ch. BW)	+26.6†(Δf_B=2×Ch. BW) +32.7‡(Δf_B=14×Ch. BW)
OOB IIP2 [dBm]	NA	+64	+88	+74†
NF [dB]	6.8-9.7§	7§	2.5§	3.6 (noise cancel on) 6.3(noise cancel off)
Power [mW]	52 (Analog) 16.2 (0.2GHz LO)	77.6 (Analog) 12.7 (1GHz LO)	50 (Analog) 45 (1.5GHz LO)	79.9-148.3*(Analog) 45(1.5GHz LO)
Supply [V]	1.2	1.2 (Analog)/ 1.0 (LO)	1.2	1.8(Analog)/1.1(LO)
Area [mm^2]	2.03	2.3	0.8	2.64

* Depends on receiver operating mode

** Channel BW is twice the baseband BW

† in high-linearity mode of receiver

‡ in low-noise (noise cancel. off) mode

§ excludes balun loss

CHAPTER 6

Conclusion

6.1 Summary

This dissertation described a wideband reconfigurable blocker tolerant receiver for cognitive radio applications. EKV model was used to understand distortion of major circuit blocks of the receiver and methods to improve their linearity were also described. Low phase noise design of the LO path was also included as a part of this dissertation.

Chapter 2 described RF G_m nonlinearity using EKV based FET model. Expressions for its IIP3 and $\mathrm{P_{1dB}}$ were found, which showed that raising supply voltage V_{dd} increases the linearity of inverter based G_m. Derivative superposition method was shown to boost inverter linearity by making G_{m3} zero over wide range of input amplitude without compromising noise figure.

Chapter 3 detailed EKV based FET model to analyze mixer switch nonlinearity. Expressions for its IIP3 and P_{1dB} were given, which showed that increasing $\frac{R_s}{R_{on}}$ can be used to lower mixer switch distortion. Design of LO path was also described using a low phase noise divide-by-4 circuit (-172 dBc/Hz at 12MHz offset). Since the divider output frequency was limited to 3 GHz, it was shown that baseband weighting coefficients of the receiver can be reconfigured to downconvert wanted signals from $2f_{LO}$. As a result receiver maximum operating frequency can go up to 6 GHz.

Chapter 4 looked at the design of TIA for use in the baseband section of the receiver. Noise factor of TIA as well as its large-signal operation was analyzed to understand the trade-offs involved. It was shown that using source follower inverter based TIA G_m gives higher compression point but it also results in higher input noise. Pseudo-differential realization of source follower inverter based TIA G_m along with CMFB network and biasing circuitry were also described in this chapter.

Chapter 6 introduced receiver reconfigurability. Measurement results including receiver noise, small-signal gain, and its linearity under different operating modes were also given in this chapter. Linearity of the receiver is comparable to prior art, but it rejects unwanted channels at 3rd and 5th harmonic of the LO. With a single-ended RF input, it also achieves better blocker noise figure than similar receivers.

6.2 Future Work

Power consumption of the baseband filter in the prototype receiver can be lowered by using higher-order (>1) TIAs upfront without raising V_{dd} to withstand large close-in blockers. This would allow significant power savings (up to 50%).

Future work on the linearity of RF G_m can include the design of a control loop that tunes the offset voltage of auxiliary FETs to maintain a high receiver P_{1dB} over process, voltage, and temperature (PVT) corners.

Future work on the distortion analysis of mixer switches can include the impact of imperfect virtual ground. One approach could be to model virtual ground imperfection using resistors, and then analyze the resulting nonlinear network to see its impact on receiver IIP3 and P_{1dB}. This will result in a more accurate model for mixer switch distortion.

APPENDIX A

EKV Transistor Model

EKV model [10] is used in many places through out this dissertation. Here a brief description about this model is given. To keep the explanation simple and easy to understand, we will discuss EKV model for an n-type MOSFET.

Fig. A.1 shows a cross section view of an n-type MOSFET. Note that the source V_S, drain V_D and gate V_G voltages are all defined with respect to the substrate (substrate is assumed to be at $0\,V$). Let's assume that initially the source and drain are also at $0\,V$, and the gate voltage $0\,V$. As V_G becomes positive, it repels any holes in the substrate away from the gate region leaving behind immobile negatively charged ions of the substrate. Also mobile electrons are attracted closer to the surface right underneath the gate region because of the positive potential applied at the gate terminal. At a certain positive V_G, the charge density of electrons (minority carriers) in the channel region becomes greater than that of holes (majority carriers). At this point, the channel is said to be "inverted", and the value of gate voltage at which this occurs is called the zero bias *Threshold Voltage* V_{t0}.

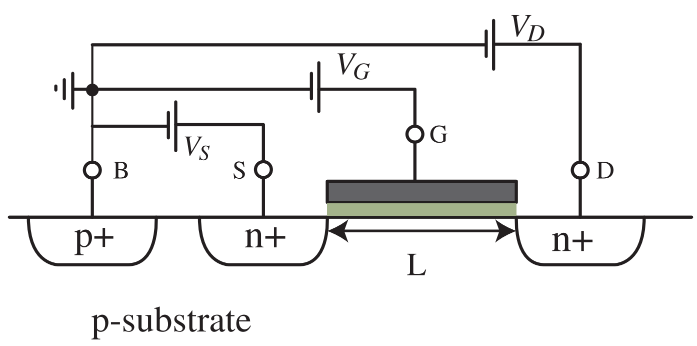


Figure A.1: Cross-section view of n-type MOSFET.

For a certain gate voltage V_G, the inversion layer charge density Q'_{inv} decreases if the drain voltage V_D becomes positive ($V_S = 0\,V$). The value of channel potential V_{ch} at which $Q'_{inv} = 0$ is called the pinch-off voltage V_P. Fig. A.2 shows the graphical representation of Q'_{inv} as a function of channel potential V_{ch}. From Fig. A.2 it is clear that Q'_{inv} is a linear function of V_{ch}, and the slope of the straight line is $n > 1$. n is called the body effect or slope factor in EKV model.

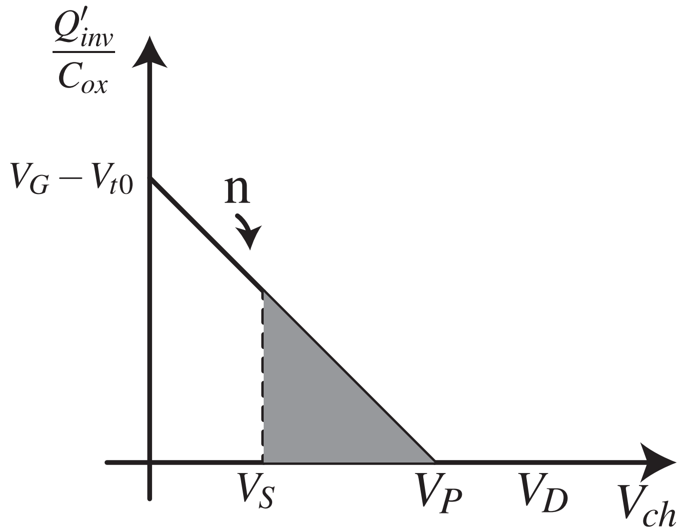


Figure A.2: Inversion layer charge density Q'_{inv} vs channel potential V_{ch}.

In Fig. A.3 $V_D < V_P$, and nmos is said to be in triode region. The current through nmos in triode region can be calculated easily from the area of the shaded region in Fig. A.3. This can be done conceptually in three steps: first calculate the area underneath the curve from V_S to ∞ (this gives the *Forward Current* I_F), in second step calculate the area underneath the curve from V_D to ∞ (this gives the *Reverse Current* I_R), and in the third step net current flowing through the nmos is $I_F - I_R$.

$$Area = \frac{I_F}{\beta} - \frac{I_R}{\beta} = \frac{n}{2}\left(V_P - V_S\right)^2 - \frac{n}{2}\left(V_P - V_D\right)^2 \ . \tag{A.1a}$$

$$I = I_F - I_R = \frac{n\beta}{2}\left[\left(V_P - V_S\right)^2 - \left(V_P - V_D\right)^2\right] \tag{A.1b}$$

where $\beta_n = \mu_n C_{OX}\left(\frac{W}{L}\right)_n$. μ_n is the electron mobility and C_{OX} is the oxide capacitance per unit gate area. $\left(\frac{W}{L}\right)_n$ is the width to length ratio of the nmos device.

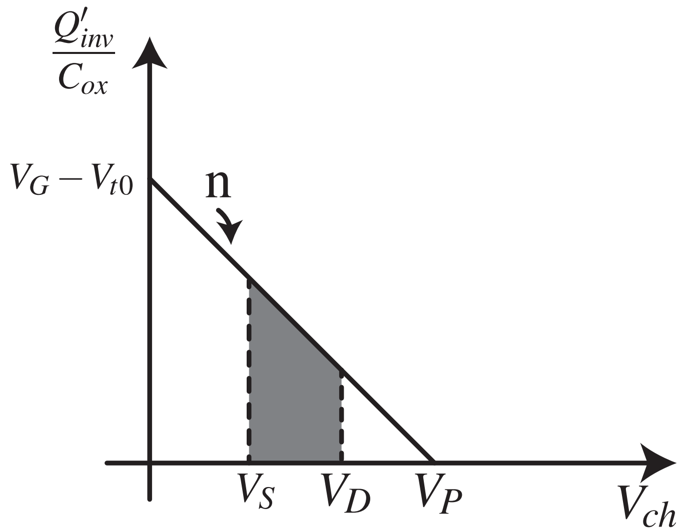


Figure A.3: Inversion layer charge density Q'_{inv} vs channel potential V_{ch} when FET is in triode.

In case if $V_D > V_P$, then nmos is said to be in saturation. The current through nmos in saturation region can be calculated easily from the area of the shaded region in Fig. A.2. Note that in this case *Reverse Current* I_R is zero.

$$I = I_F = \frac{n\beta}{2}\left(V_P - V_S\right)^2 . \tag{A.2}$$

In above equations V_P is the pinch off voltage of nmos, and is given as

$$V_P = \frac{V_G - V_{t0}}{n} . \tag{A.3}$$

In general, EKV model uses two controlled current sources to model the drain current of n-type MOSFET : *Forward Current* I_F (function of V_G and V_S) and *Reverse Current* I_R (function of V_G and V_D). These current sources are given by the following equations.

$$I_F = \begin{cases} \frac{n\beta}{2}\left(V_P - V_S\right)^2 & V_P > V_S \\ 0 & V_P \leq V_S \end{cases} \tag{A.4}$$

$$I_R = \begin{cases} \frac{n\beta}{2}\left(V_P - V_D\right)^2 & V_P > V_D \\ 0 & V_P \leq V_D \end{cases} \tag{A.5}$$

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