Title
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H. G. Jackson, Fred Kirsten, and Dick A. Mack

September 7, 1966

At present the basic integrated circuit cell is the AND/OR gate. In discussions with manufacturers we find that by next summer production quantities of circuits with various configurations of AND/OR gates with propagation times of 1.5 nsec should be available. In terms of scalers this means one will be able to count at rates up to 150-MHz. The projected price, when suitable production is achieved, will be 10 cents per gate; as many as 200 gates may be included in a single package. The price for low-production, custom circuits, which we would often wish to employ in nuclear instrumentation, is expected to be as low as 50 cents per gate. Circuit reliability will continue to improve as more and more connections are made on the silicon die itself.

Present Equipment

For the moment consider some of the limitations of the presently available counting equipment. Figure 1 shows the experimenter's view of the fast-logic portion of a typical large experiment:

It is difficult to keep track of the cabling.

Controls and readout are not readily accessible behing the maze of cables.

It is time-consuming and difficult to make substantial changes in the logic without introducing errors.

The time delay due to the length of patch cables can be appreciable.

The packaging is bulky compared with integrated circuits presently being developed (see Figure 2).

However, controls or readout requiring human intervention cannot be reduced below a certain limit. The advantage of present equipment is that modules can easily be replaced, interchanged, or reconnected into other systems.

We have developed prototype discriminators, coincidence circuits, and memory flip-flops where each circuit is constructed on its own small printed circuit board. These in turn plug into another larger inter-connection board. Figure 3 shows a laboratory-designed cordwood construction flip-flop on the left and a 50-MHz tunnel-diode discriminator on the right.

Proposed System

The next generation of fast-logic circuits should be aimed at keeping the desirable aspects of present equipment while eliminating as much as possible the areas where one has had problems. We would expect to replace presently available modules with miniature plug-in packages. Integrated circuits would be used whenever possible; where they are not available, one can continue to construct cordwood bundles or printed circuit boards using discrete components. A group of these packages could plug into a universal logic panel as shown in Figure 4. Thus the entire fast-logic portion of a large experiment could be located on one or two 19-inch panels. Monitoring, power, and ground buses can be permanently supplied to each circuit position by means of printed wiring. Input and output signals from individual circuits can be interconnected as desired with miniature coaxial patch cables. As an example, all detector- and test-signal connections could appear along the left-hand side of the panel and output and monitor connectors on the right.

Most circuits require some switching or control elements; we propose that the experimenter have the option of switching circuits or making adjustments either manually or under computer control. During the initial part of the experiment most of the adjustment would be done manually; as the experiment progresses and programs are refined,more and more of the switching would come under the direction of the computer program.

Computer Control

A number of recent experiments have employed a small computer to organize both the data-gathering and "housekeeping" functions of the experiment. The data-gathering aspects have been described elsewhere.[1,2] Housekeeping functions have included such checks as the singles counting rate of each detector, the ratios of the rates of several detectors, the background or noise counting rate, and the detector transit time. It has been possible to keep account of cable delays as well as catastrophic shorts and open circuits. The computer has been used to check for double pulsing or no pulsing at all. The computer can keep track of the accumulated counts from any counter, or counter ratios, and alert the experimenter if they depart from expected range values. The time drift of an entire system can also be checked by requiring the computer to measure the slopes of the coincidence delay curves at appropriate intervals; if signal pulses are not available, test pulses can be substituted for them at the programmer's option.

Circuit Design

At present most of our circuits are designed so that all switching or control functions do not operate on the signal itself; they are achieved by adjustment of dc bias levels. Thus both the computer and the control panel can be located remotely from the circuits themselves, and each in a position convenient for the experimenter. Figure 5 shows such a control panel. It will be noted that for ease in operation, the controls are located in the same spatial positions on the control panel as are the circuits themselves on the fast-logic panel.

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[1] S. Andreae, The Use of the PDP-5 in Nuclear Experiments at LRL, Lawrence Radiation Laboratory Report UCRL-16723, February, 1966 (unpublished).

[2] C. M. Ankenbrandt, et al, Orthogonal Dispersion Spectrometer for Missing Mass Spectra, IEEE Trans. on Nuclear Science, NS-12, No. 4, Pages 113-119.

Typical System

Figure 6 illustrates the fast-logic portion of a typical counter or spark chamber experiment. The x and y counters may have two angular positions or be arranged in rows and columns. Some portions of the logic which can readily be brought under computer control have been accentuated.

The functions introduced are controllable attenuation (gain), delay, and discrimination threshold and output pulse length. Several uses for this controllable logic are immediately apparent. The time now used in initial setting up and calibration could be greatly reduced by employing computer supervision.

Automatic checks and corrections for timing and amplitude drifts can be made by appropriate variations in the logic configuration (e.g., between beam bursts of an accelerator). If stable thresholds are important, stabilization can be accomplished by using test signals or radioactive sources. Thus, one can study system performance without using actual accelerator beam time.

Specific Circuits

A remotely controlled variable delay unit is particularly useful. Two methods of accomplishing this are described. Figure 7 illustrates for linear or standard-amplitude pulses an array of AND and OR gates used to progressively switch in differential delays of 1, 2, 4,....nsec, for example, to achieve any integral delay up to the maximum of the unit. Figure 8 indicates a single-shot multivibrator used as the delay element, for pulses of standard amplitude. Manual control is available from the delay-adjust potentiometer; for computer control the instruction sent to a one-word register is decoded into an analog signal in the digital-to-analog converter. The time measuring-circuit is a time-to-amplitude converter and a comparison circuit which report to the computer if the delay element has carried out its instructions properly. If not, the computer can attempt a correction; if this is ineffective, an alarm is sounded.

The functions of amplitude discriminators lend themselves to computer control. Figure 9 shows the block diagram of how a typical unit may be constructed. Linear AND gates allow either detector or test pulses to be fed to the threshold circuit. Both the threshold level and the pulse length are capable of manual adjustment with a switched or rotary potentiometer; for computer control one uses a register and D-to-A converter described above.

In this application the coincidence circuit must have means for remotely activating each channel of coincidence and anticoincidence. This is illustrated in Figure 10. Coincidence inputs enter through logic OR gates and anticoincidence inputs through logic AND gates. If a coincidence channel is to be made inoperative, the alternative OR input is turned on either by manual or by computer control.

Summary

A number of logic functions have been described that can readily be controlled with very modest computer programs. The savings in accelerator and experimental time that can be effected by having programmed checks on system performance more than offset the additional circuit complication.

FIGURE CAPTIONS

1. Fast-logic portion of a typical large experiment.
2. Integrated circuits compared with modular boxes.
3. Cordwood construction flip-flop and a 50-MHz tunnel-diode discriminator.
4. Universal logic panel.
5. Universal control panel.
6. Block diagram of a fast-logic portion of a typical experiment.
7. Block diagram of a digital delay circuit.
8. Block diagram of a multivibrator delay circuit.
9. Block diagram of a discriminator.
10. Block diagram of a coincidence-anticoincidence circuit.

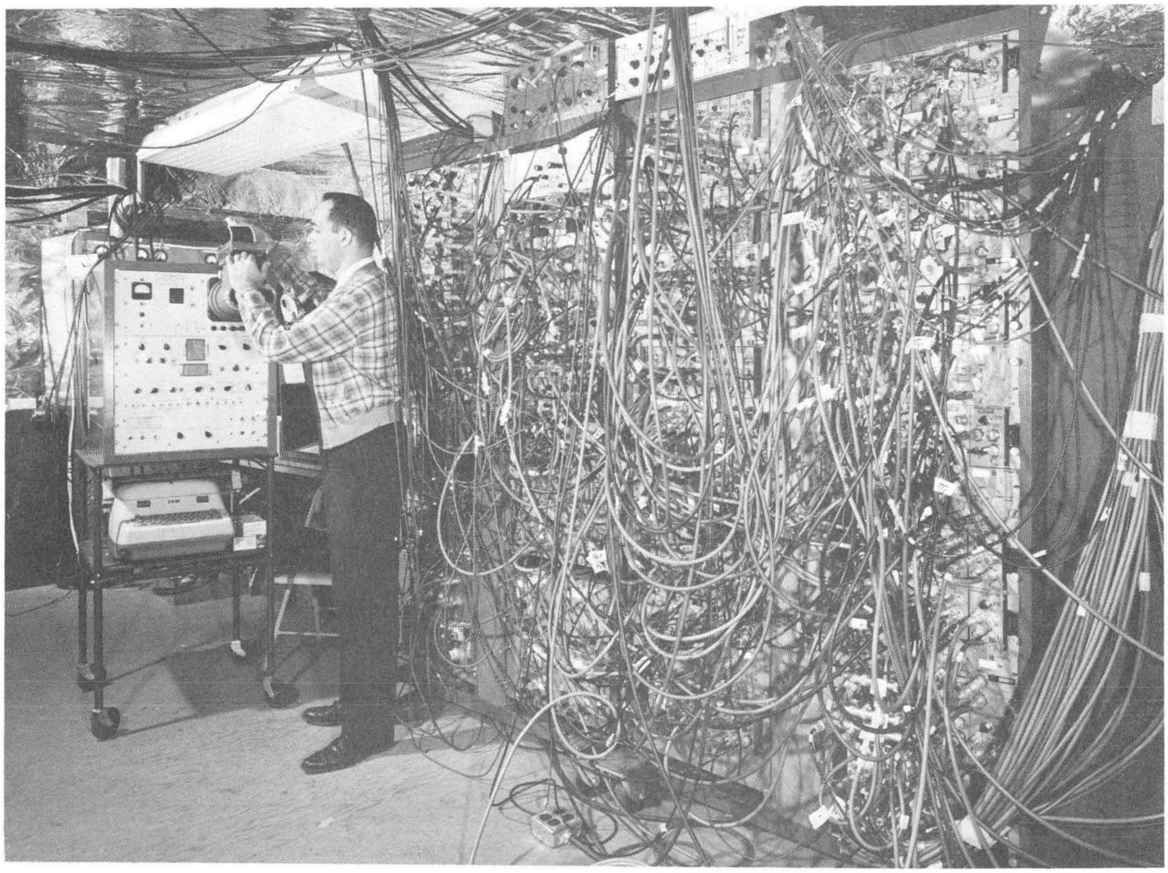

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Fig. 1

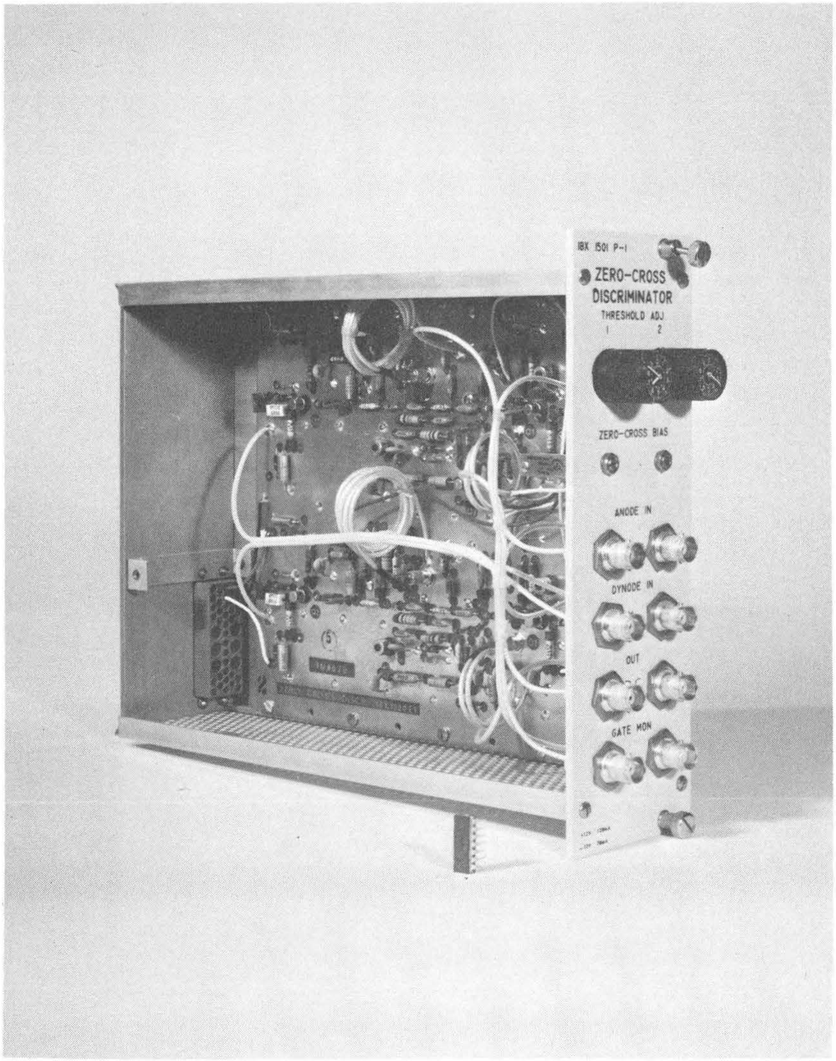
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Fig. 2

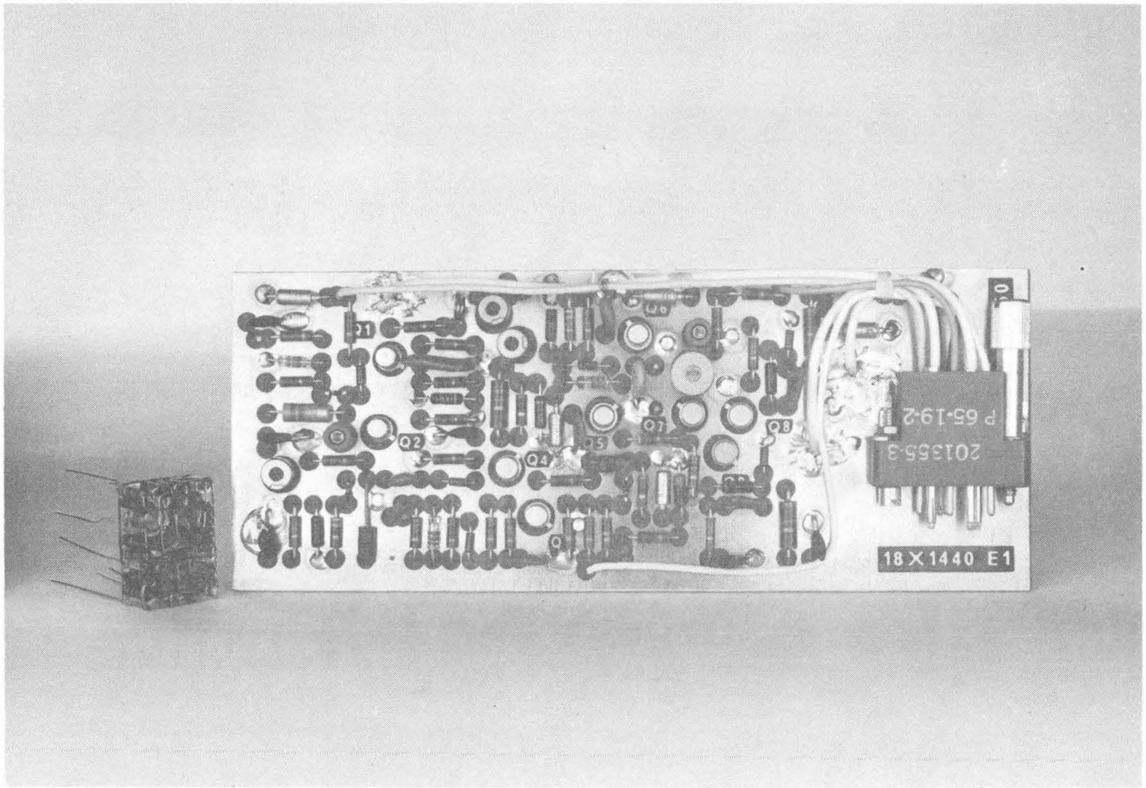

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Fig. 3

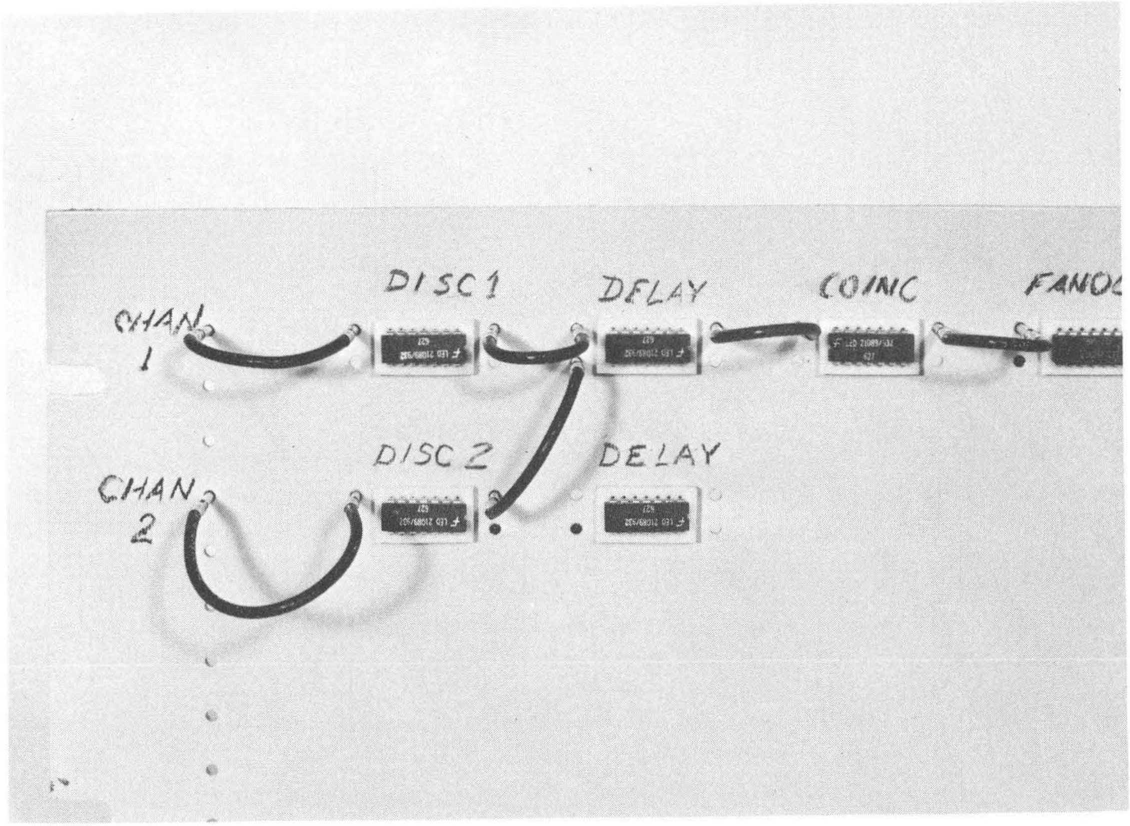

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Fig. 4

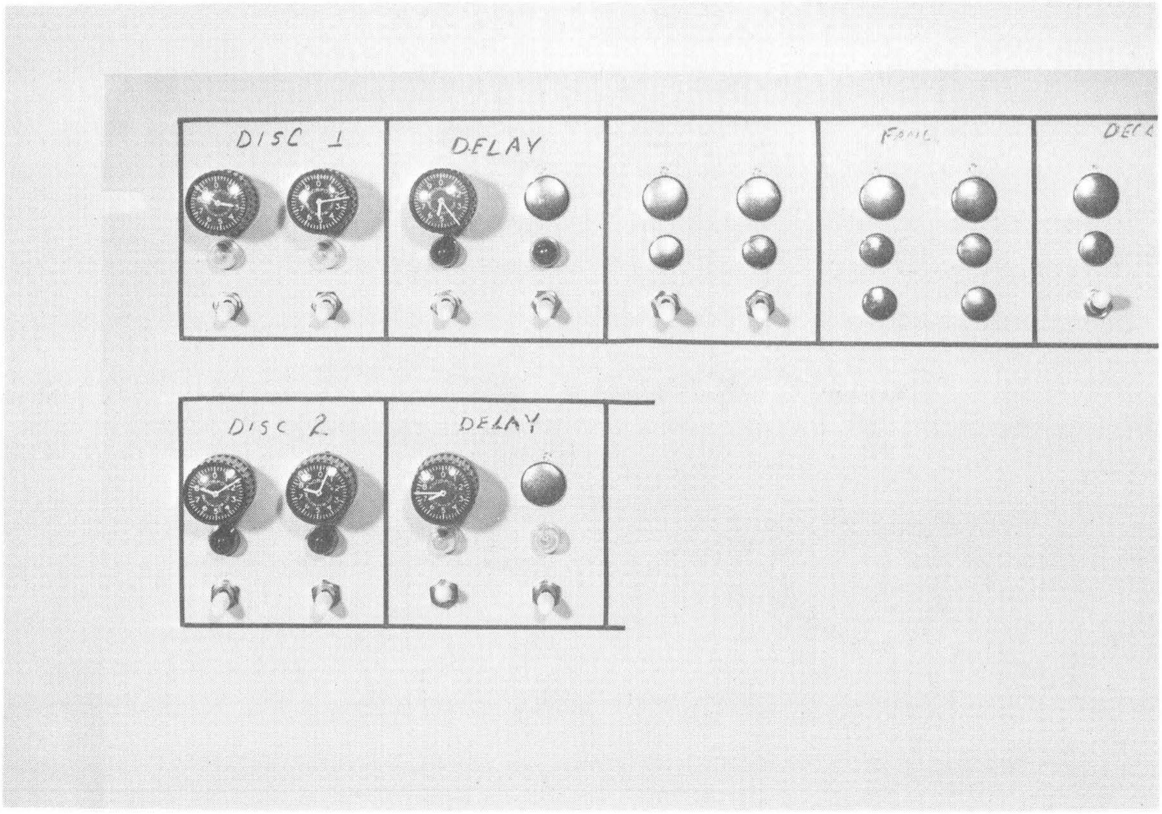

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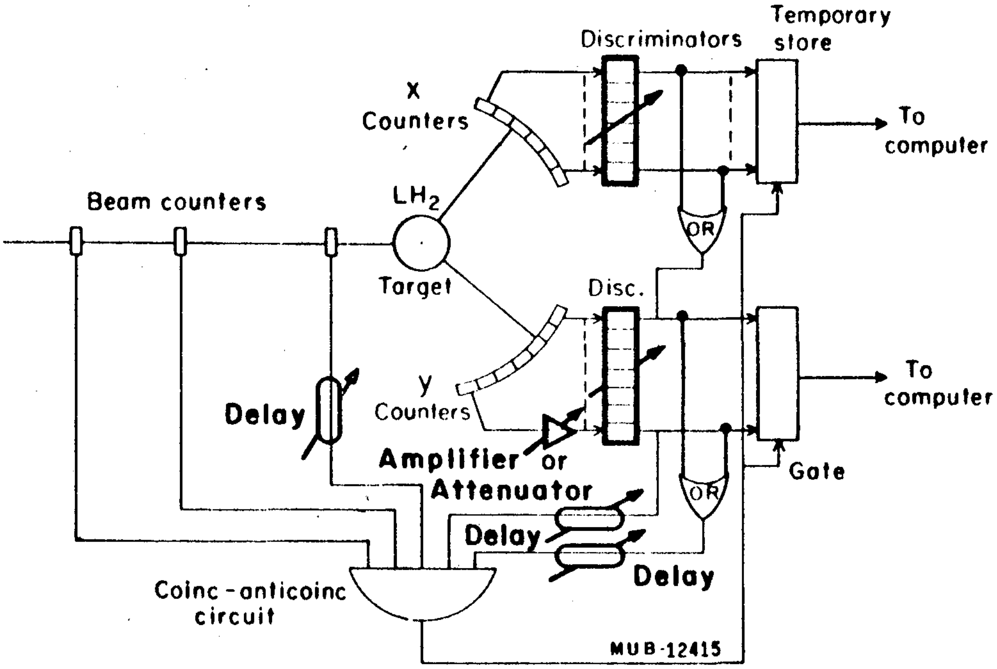
Fig. 5


Temporary store
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X Counters
To computer
Beam counters
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Coinc-anticoinc circuit
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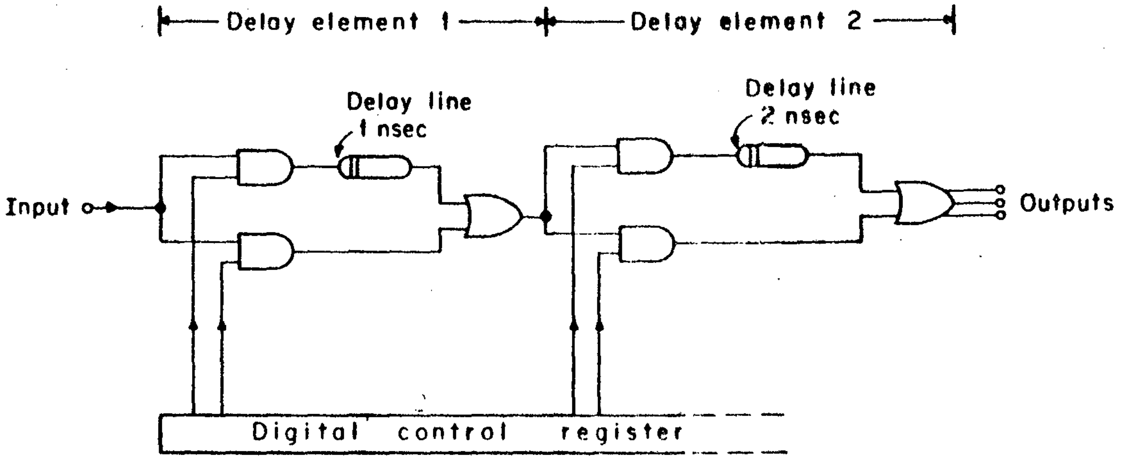
Fig. 6



Delay module

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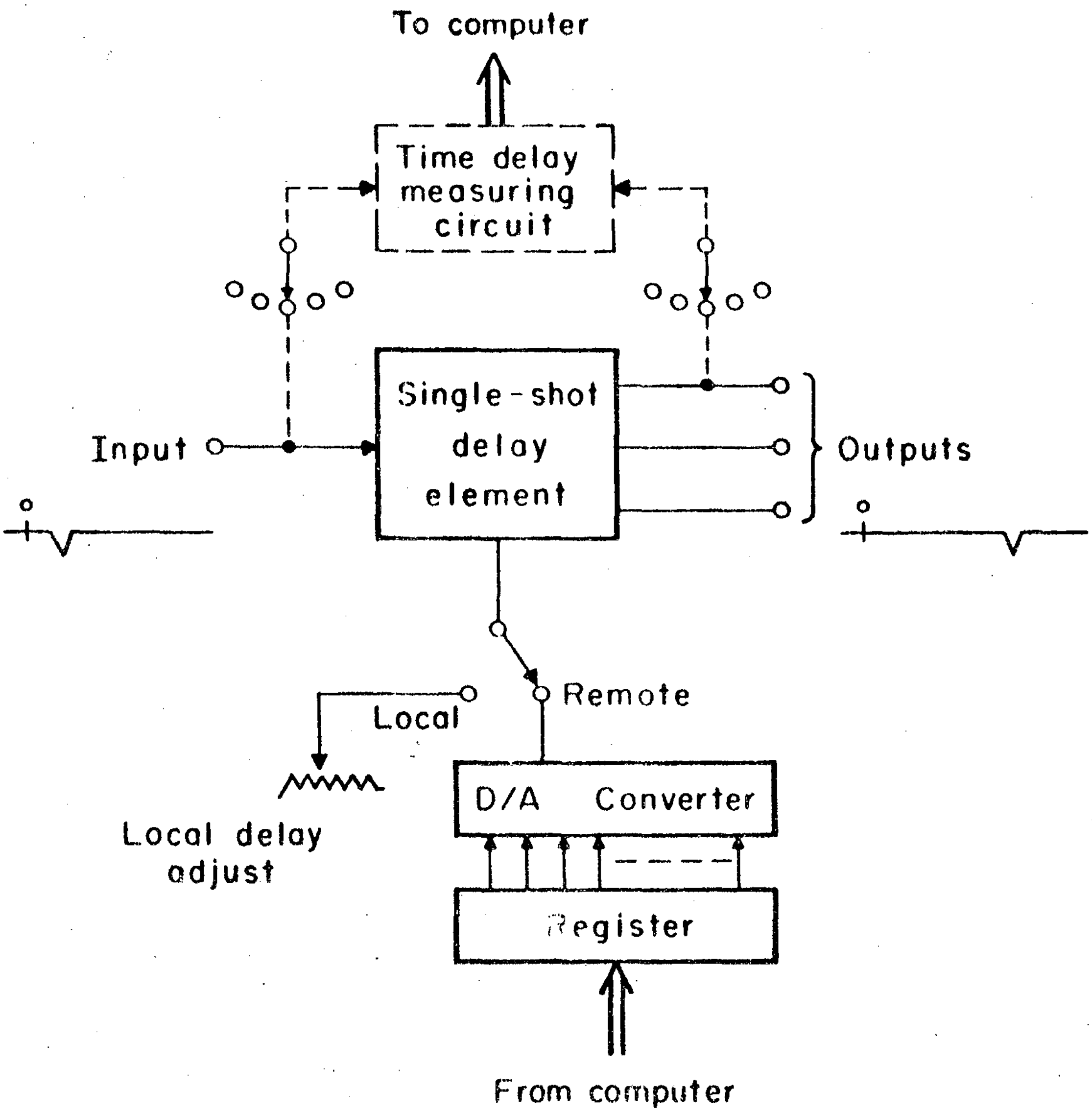
Fig. 7



Delay modules

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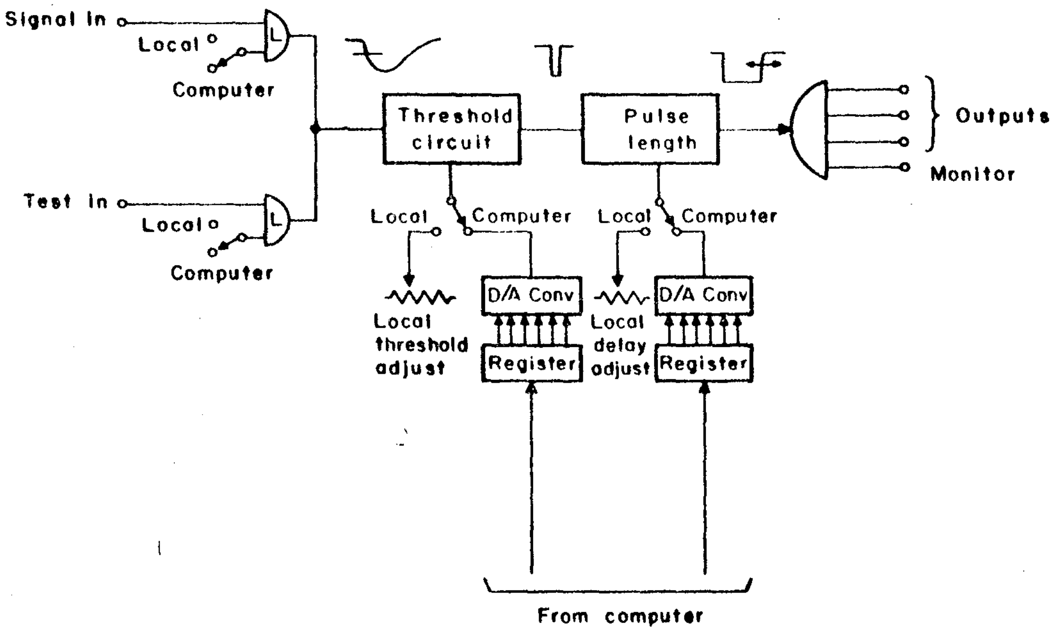
Fig. 8



Discriminator module

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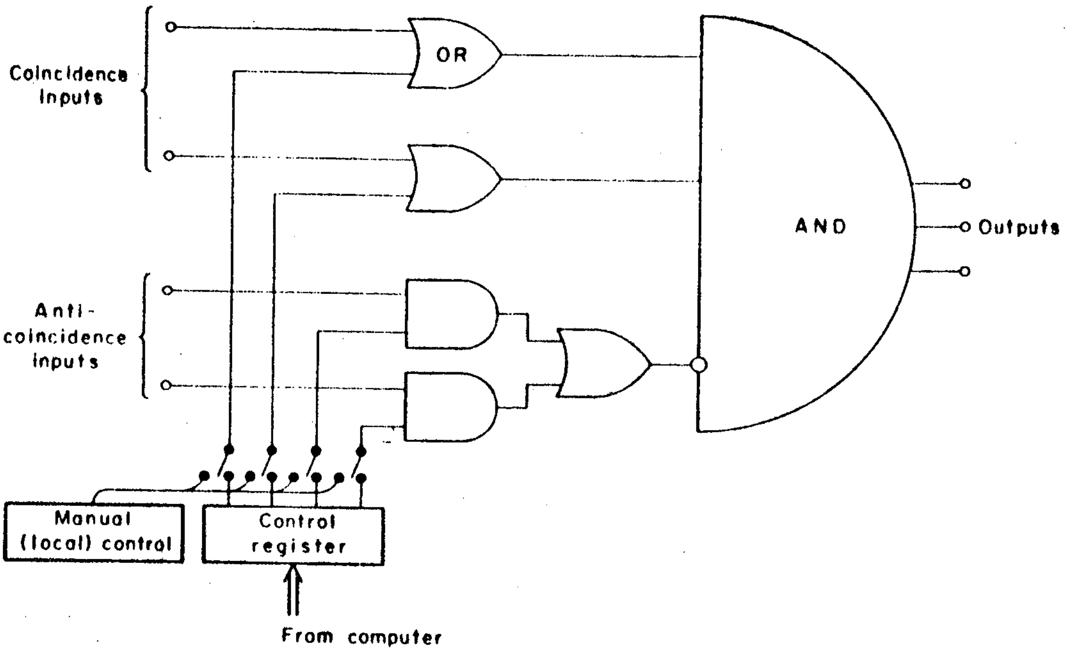
Fig. 9



Coincidence module

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Fig. 10