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Molecular Beam Epitaxy (MBE) II-VI-III-V System for Photonic and Electronic Devices

By

ZONGJIAN FAN DISSERTATION

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Abstract

Comprehensive investigations of the materials properties and device applications made from molecular beam epitaxy (MBE) prepared ZnSe-GaAs epilayers have been performed. The properties of ZnSe-GaAs (100) interfaces were studied in order to enable the fabrication of high quality ZnSe-GaAs heterovalent structures (HS). The atomic structure of the ZnSe/GaAs interface with different surface terminations of GaAs was examined. ZnSe deposited on Ga-terminated GaAs was found to have a superior optical and microstructural quality. It is a highly coherent interface consisting of a mixture of both GaAs and ZnSe atomic constituents. To prepare GaAs on ZnSe interfaces, a low-temperature migration enhanced epitaxy (LT-MEE) growth technique was developed to grow GaAs layers under the conditions compatible with ZnSe. Both Ga and As-initialized LT-MEE GaAs/ZnSe interfaces were investigated. A defective transition layer was observed along the As-initialized GaAs/ZnSe interface, which may be attributed to the formation of the Zn₃As₂ compound. The correlation between the observed optical and structural properties of ZnSe-GaAs interfaces and growth conditions is discussed in detail.

The second component of this thesis was to study ZnSe/GaAs/ZnSe quantum well (QW) structures for potential light emitting devices. Unfortunately, ZnSe/GaAs based QWs formed with abrupt interfaces cannot produce ideal photoluminescence (PL) performance due to inherent defect formation at heterovalent interfaces. However, Ga-initialized MEE GaAs growth and high temperature annealing was found to be able to facilitate a compositionally graded ZnSe-GaAs interface. The annealed QW structures exhibited strong, novel PL emission with broad peaks from 500-800 nm at room temperature. Transmission electron microscopy (TEM) results revealed that the annealed QW structure has an intermixed ZnSe-GaAs layer in the QW region with all four elements. Detailed investigations have been conducted to understand the luminescence mechanism. Evidence suggested that intermixed ZnSe-GaAs was responsible for the broad PL emission. Finally, novel ohmic contacts to n-ZnSe were demonstrated using both in-situ deposited single crystal Al films by MBE, and ex-situ deposited Cu films. For Al contacts, electron backscatter diffraction (EBSD) confirmed the single crystalline structure of the Al films. The (110)-oriented Al layer was rotated 45° relative to the substrate to match the ZnSe (100) lattice constant. Leaky Schottky behavior in lightly doped ZnSe samples suggested that Al-ZnSe formed a low-barrier height, Schottky limit contact. For Cu contact, X-ray photoelectron spectroscopy (XPS) detected the traces of Cu₂Se bonding environment at Cu/ZnSe interface, which contributed to the ohmic contact formation. Both as-grown contacts exhibited nearly ideal ohmic electrical characteristics without any additional treatment. The contact resistances are in a range of $10^{-3} \Omega$ cm² for even lightly doped ZnSe. The novel metallization method could greatly simplify the ZnSe-based device fabrication complexity and lower the cost.

1 Introduction

1.1 The Demands of Light Emitting Diode (LED) Market

From torch, to oil lamp, then to Thomas Edison's light bulb, our human being's pursuit of light source never stops. LEDs are believed to be the most advanced active lighting technique we currently have [1, 2]. It embraces attractive features like high efficiency, high color accuracy control, long lifespan, and finds lots of applications including general illumination, color display, communications [2]. The light emission process of a LED relies on the radiative recombination of electron-hole pairs in direct band-gap semiconductors. Practically, it is generally achieved through a p-n junction, as shown in Figure 1.1 [3]. The holes from p-side and electrons from n-side diffuse across the p-n junction under forward bias voltage, and radiatively recombine with each other to generate light emission. The wavelength of emitted light wave is determined by the band-gap of the semiconductor. In the other word, the color of emitted light depends on the used semiconductor. Therefore, there are generally two essential requirements for realizing an efficient LED at a given emission wavelength: one is to use a direct band-gap semiconductor with desired band-gap

energy and high materials quality, the other is to be able to dope it both n- and p-type robustly. Although it appears not difficult, practically, the development of efficient LEDs has largely lagged behind theory.



Figure 1.1. A schematic structure of a p-n junction LED (Figure is from Ref. [3]).

The development of efficient LEDs had been a long-term dream for researcher across the world. Since our human eye cells have three unique response peaks to visible light, approximately at red, green, and blue (RGB) wavelengths, any color of visible light could be generated by RGB color mixing in theory. Therefore, the development of individual colored-LEDs for red, green, and blue has been placed at the most important position. The effort to realize RGB colored-LEDs started at early 1960s. As shown in Figure 1.2 [4], a red LED based on gallium arsenide phosphide (GaAsP) was developed by Holonyak and Bevacqua in 1962 [5]. Although the quantum efficiency (0.1%) was not desirable due to poor crystal quality and lack of p-type doping [5], it was recognized as the first visible LED in the world. After that, more efficient Ndoped GaAsP and Zn- or O-doped gallium phosphide (GaP) were developed as red and red-green LEDs [6, 7], which relies on the radiative recombination through the complex pairs or sub-band states inside the semiconductor band-gap. However, the limited density of sub-band states hindered the further improvement of efficiency and brightness for these LEDs [6, 7]. Later, high efficiency aluminum gallium arsenide (AlGaAs)-based red LEDs became dominant owing to its high materials quality [8]. It was later replaced by aluminum gallium indium phosphide (AlGaInP)-based red LEDs for better light extraction technique [9]. On the other hand, the importance of efficient blue LEDs was more valued because the blue light photon has the biggest energy in visible light spectrum. Theoretically, it can be later converted to longer wavelength visible light photons by other techniques. As described above, an efficient blue LED requires a p-n junction made by wide band-gap semiconductors. However, it is generally difficult to fabricate high-quality wide band-gap semiconductors, and even harder to create both n- and p-type conductivity [3, 4]. In late 1970s, candidate materials for blue LEDs included silicon carbide (SiC), zinc selenide (ZnSe) and gallium nitride (GaN) [3]. GaN-based LEDs finally beat other candidates and became the choice for high-efficient blue and blue-green LEDs. More importantly, combined with yellow phosphors which converts the blue light to yellow light, GaN-based LEDs can emit white light to human eyes [4]. It is gradually replacing fluorescent lamp as general illumination light sources. The development of GaN-based blue and white LEDs was awarded for Nobel Prize of Physics in 2014.



Figure 1.2. Evolution of luminous efficacy of red, green, and blue LEDs (Figure is from Ref. [4]).

As the LED technology advances, there are increasing application scenarios, as well as increasing requirements for technology. To achieve true RGB light emission with optimal chromaticity, one needs LEDs with red, green, and blue colors right at human eyes' response peaks. As described above, currently, high efficiency GaN-based blue, and blue-green LEDs and GaInP-based red LEDs are commercially available (Figure 1.3) [2, 4]. However, true green LED is still missing due to lack of semiconductor materials with suitable band-gap, which inhabits the full color mixing ability over the whole spectrum by LEDs. Besides, different colored LEDs from different materials are typically difficult to be integrated together, which limits the development of multiple color application circumstances such as color display. Therefore, RGB pixelated LEDs made from a single materials system could define the ultimate stage in this field.



Figure 1.3. Efficiencies of current commercially available colored LEDs and the "green gap" (Figure from Ref. [2]).

More recently, there are emerging interest on innovative technologies based on micro-size LEDs (or microLED), which is defined as LEDs with pixel size < 30 µm. Emerging microLED products include augmented reality/virtual reality (AR/VR) display applications, high brightness/resolution large panel displays, wearable devices, and light source/network for visible light communications (Li-Fi) [10]. According to MarketWatch, "The global MicroLED market is expected to reach \$17 billion by the end of 2025, growing at a compound annual growth rate (CAGR) of 78.3% during 2019–2025" [11]. However, traditional semiconductor LEDs including GaN are facing new challenges for the novel microLED applications [12-15]. For GaN-based LED, it shows a strong size-dependent efficiency and significant efficiency droop at high current density when the size is small [12, 14]. It is mainly caused by the surface states of InGaN at device sidewalls. As the downscaling of the pixel size at the demands of microLED

applications, the sidewall surface to volume ratio dramatically increases and thus the surface state becomes a significant problem [14]. On the other hand, organic-LED (OLED) is also a candidate for micro-size LED applications [16]. OLEDs have successfully been commercialized in small displays like mobile devices, and large-scale televisions [16, 17]. There are typically two different branches for OLED display business. First, RGB OLEDs are mostly used in mobile displays and TVs. Currently, the fabrication procedures for separated RGB OLED pixels relies on depositions through a fine-metal mask (FMM) [16, 17]. But it has challenges to achieve desirable small pixel size because of shadowing effects in the deposition. Besides, another technique using white OLEDs with color filters could solve the downscaling problem in some ways. However, as the color filters bring in a large optical loss (>70%), the power consumption of displays becomes a problem especially for small devices, such as display degradation [16, 18].

In summary, although the LED technology witnessed tremendous development over the past decades, there is still plenty of room for further improvement. To satisfy the ever-increasing demands for today's and next-generation technology, a fundamentally new materials, device, or fabrication approach is clearly needed.

1.2 Molecular Beam Epitaxy (MBE)

MBE is an epitaxial thin film growth technique for various kinds of materials including semiconductors, metals, and insulators [19, 20]. It finds a lot of applications in both research lab and mass production. It serves as the fabrication tool for many electronic and photonic semiconductor devices including LEDs, solar cells, lasers, transistors [19]. Here in this work, we mainly focus on solid-source MBE for semiconductors.

In MBE, the grown thin film is formed based on the interaction of atoms/molecules beams impinging on a crystalline surface at elevated temperature under ultra-high vacuum (UHV) conditions [19, 20]. As shown in Figure 1.4, a typical MBE growth chamber contains several effusion cells with different

source materials, mechanical shutters, a substrate heater, and some characterization tools (quadrupole mass analyzer, ion gauges, reflection high energy electron diffraction (RHEED)). For semiconductor growth, the composition of the grown epilayer and its doping level depend on the relative arrival rates of the atoms/molecules from effusion cells [19]. The arrival rates could depend on the evaporation rates of the sources, mainly temperature. Simple mechanical shutters are placed in front of every cell to interrupt the beam fluxes, *i.e.*, to start and to stop the deposition or doping [19]. In addition, the typical slow growth rate (monolayer (ML) /sec), abrupt, atomic scale changing of film composition and doping could be achieved.



Figure 1.4. The schematic diagram of a solid-source MBE system (Figure is from Ref. [20]).

The advantages of MBE over other crystal growth techniques mainly lie in two ways. First, the growth chambers are equipped with several vacuum pumps which give the base pressure in UHV range

(typically $< 10^{-10}$ torr) [20]. The UHV environment could ensure that the background contaminants are reduced to minimum level. Quadrupole mass analyzer is equipped inside the chamber to monitor the partial pressures of background species (hydrogen, nitrogen, oxygen, carbon, etc.). Otherwise, those contaminants could incorporate into grown epilayers as unintentional dopant, deep levels, etc., which could affect the performance of following fabricated devices. Furthermore, the atoms/molecules beam under UHV condition could have a very long mean-free path of kilometer level. Therefore, the beam has a collision-free path towards the substrate, which can easily be interrupted by mechanical shutters mentioned above. Less than single atomic layer of material deposition could be achieved by this way.

In addition, the UHV environment also enables the second main advantage of MBE: the ability to perform in-situ monitor and characterization of grown films. Among many characterization tools embedded in MBE, RHEED has been recognized to be the most powerful one. As shown in Figure 1.4, the RHEED electron gun could generate a collimated electron beam with energies from 5 to 50 keV. The electron beam impinges with a very small angle (< 3°) onto the substrate surface. Due to the geometry of the system, the electron beam does not interfere with the molecular beams, and diffracted electrons create a diffraction pattern on the fluorescent screen [20]. As directly inferred from the analysis of the Ewald sphere, the electron diffraction pattern from a low angle impinged electron beam reflects a reciprocal two-dimensional (2D) lattice of the sample surface [20]. Therefore, RHEED allows direct measurements of the surface structure of the epilayer as well as the dynamics of MBE growth [19]. Firstly, if the growth surface is smooth, the reciprocal lattice will have thin rod shape, which gives rise to the well-known streaky RHEED pattern. Otherwise, a rough growth surface will show a spotty diffraction pattern. By observing that, one could know the growth dynamics is a 2D layer-by-layer growth mode, or a 3D Stranski–Krastanov (SK) growth mode. Figure 1.5 (b) shows examples of typical streaky and spotty RHEED pattern, corresponding to 2D and 3D growth mode respectively.

Besides, the intensity of diffraction pattern also indicates the quality of the epilayer, as well as the growth dynamics. By observing the time-dependent intensity of the zero-order diffracted beam, one can

measure the real-time in-situ growth rate. As shown in Figure 1.5 (a), during the MBE growth, before one monolayer (ML) is completed, there could be some 2D islands with 1 ML height on the surface. The island edges behave as scattering centers to the electron beam that reduce the intensity of the beam diffracted: the higher the surface density of steps, the lower the diffracted intensity [20]. Therefore, during the completion of 1 ML, the zero-order diffracted beam intensity will decrease to a minimum at the middle of the cycle, then regain maximum upon the completion of 1 ML. The oscillation behavior named as RHEED oscillation could provide a real-time growth rate monitor. By measuring the growth rate of each component, one could be able to precisely control the composition of semiconductor alloys such as AlGaAs. Furthermore, clean crystalline surface in UHV will typically show different kinds of surface reconstructions, which could also be seen from the RHEED pattern. For example, GaAs shows different surface reconstructions depending on many parameters such as growth temperature, III/V beam flux ratio, and is verified by direct characterization tools like Scanning Tunneling Microscopy (STM) [21, 22]. Figure 1.5 (b) shows a typical (2×4) reconstruction pattern of GaAs. Since the reconstructions are sensitively depending on the growth parameters, RHEED could also act as an indirect in-situ monitor of serval growth parameters like temperature and beam flux ratio. For example, due to the UHV environment, the heat conduction inside MBE growth chamber is mainly through radiation. This will often cause an offset between the substrate heater (real temperature) and thermocouple (read temperature), since there's no direct contact between those two objects. By observing the temperature-sensitive surface reconstructions through RHEED, one can calibrate the substrate temperature for an MBE system. The ability to accurately control temperature is crucial in many crystal growth procedures. The powerful RHEED has no doubt given another advantage for MBE over other growth technique.

Except for RHEED, the UHV environment of MBE could enable many other in-situ characterization tools such as Auger Electron Spectroscopy (AES), X-ray Photoelectron Spectroscopy (XPS), and Ultraviolet Photoelectron Spectroscopy (UPS) [19]. They won't be discussed in detail here since not used in this work.



Figure 1.5. (a) Different stages of layer-by-layer growth by nucleation of 2D islands and the corresponding intensity of the zero-order diffracted RHEED beam (from Ref. [20]) and (b) the RHEED pattern and oscillation curve during GaAs growth from this work. The lower right corner in (b) shows examples of spotty & streaky RHEED patterns during MBE growth (InAs & GaAs growth on GaAs substrate, respectively).

In summary, MBE is a sophisticated technique to growth crystalline thin semiconductor films. The UHV environment and in-situ characterization tools like RHEED provide precise control of composition,

doping and thickness of grown semiconductor films with superior materials quality. It will be used as a main fabrication tool in this work.

1.3 The ZnSe-GaAs System by MBE

ZnSe, a wide band-gap ($E_g = 2.67 \text{ eV}$) II-VI material, was once extensively researched in the 1980s to 1990s because of its potential usage as a blue-green laser diode [23-26]. It was one of the candidates for blue LEDs like GaN and SiC [3]. At first, it faced a big challenge in the availability for both n- and p-type doping like all other wide-gap semiconductors: the self-compensation mechanism tends to prevent wide-gap semiconductor to be doped both n- and p-type [27]. For ZnSe, p-type doping appeared to be the difficult part. Researchers firstly used Li as a p-type dopant for ZnSe, then switched to N for higher doping concentration limit [28], although the upper limit of doping is at 10¹⁸ cm⁻³ due to self-compensation [29]. Subsequently, ZnSe-based p-n junction laser diodes (LDs) and LEDs at blue and blue-green wavelength were successfully demonstrated in 1990s [23-25]. However, the lifetime of ZnSe-based devices was proved to be a problem due to materials degradation [26, 30, 31]. And the p-type dopant was one of the main causing mechanisms for degradation [30, 31]. As the GaN research proceeded rapidly, ZnSe was replaced by GaN as the material choice for blue-green light emitting devices [3, 4].

The most appealing nature of ZnSe in this development was based on the fact that it can be grown lattice-matched to commercially available GaAs substrates (mismatch is 0.25% at room temperature) [34]. There are many fascinating applications based on ZnSe-GaAs lattice-matched interfaces. Among them, the ZnSe-GaAs digital superlattice system (DSS) is predicted to have tunable effective band-gaps between 1.42 eV and 2.67 eV (Figure 1.6), *i.e.*, from infrared to blue [35-37]. If experimentally verified, this DSS could provide a path to true RGB light emission with optimal chromaticity, including improved RGB displays, LEDs, and lasers, in a single lattice-matched, direct energy gap materials system. Except for DSS described above, ZnSe-GaAs as a lattice matched, direct wide-gap semiconductor system with many explorable

interface properties, could find many applications as other electronic and photonic devices. For example, ZnSe's attractive properties such as high breakdown electric field and high carrier saturation velocity could lead to high power hybrid bipolar transistor (HBT) [32, 33].



Figure 1.6. (a) ZnSe-GaAs superlattice band offsets diagram and (b) ZnSe-GaAs superlattice calculations of effective band gap as a function of barrier and well thicknesses (figure from Ref. [7]).

Although the ZnSe-GaAs heterovalent structures (HS) exhibits a low lattice mismatch (0.25% at room temperature), the chemical valence mismatch at the ZnSe-GaAs HS interface is a bottleneck to practically integrate these two materials with tolerable interface defect density [22, 38, 40]. Basically, the II-VI ZnSe atoms and III-V GaAs atoms have different valence electrons and then bond charges. Therefore, when they are directly bonded together, charge neutrality can't be easily satisfied. The chemical valance mismatch introduces defect states inside the energy band-gap of ZnSe-GaAs HS system, which could degrade the radiative emission efficiency of devices [35-38, 41]. Moreover, these interface imperfections

were found to be responsible for the high stacking fault density in ZnSe-GaAs HS, which could further degrade the lifetime of devices [42].

In this regard, extensive investigations were carried out by various researchers to understand the nature of ZnSe-GaAs HS interfaces, including the widely studied ZnSe on GaAs interface (ZnSe/GaAs interface) [43-54] and the less investigated GaAs on ZnSe interface (GaAs/ZnSe interface) [38, 54]. The detailed investigations using capacitance-voltage (CV) and photocurrent spectrum (PS) techniques revealed that the ZnSe/Ga-terminated GaAs interface contains the lowest interface defect state density compared to ZnSe/As-terminated GaAs [43-45, 48]. Though, the ZnSe/Ga-terminated GaAs interface is electrically good, structurally it was found to contain an ultra-thin Ga-Se (Ga₂Se₃) compound transition layer [51], which could promote 3D nucleation of subsequently grown ZnSe, resulting in bulk ZnSe with high defect density [50]. In contrast, the electrically poor ZnSe/As-terminated GaAs was reported to contain a transition layer of Zn-As (Zn_3As_2) [51], which could promote 2D nucleation of ZnSe resulting in bulk ZnSe with low defect density [50]. The formation of these compound Ga₂Se₃ and Zn₃As₂ ultra-thin transition layers may be attributed to the reaction between Ga (Zn) and Se (As) atoms during the initial stages of epitaxial deposition of ZnSe on Ga and As-terminated GaAs surfaces [43, 47, 50, 51]. There were also a few reports on the stoichiometry of GaAs (100) surfaces intermediate between Ga-rich and As-rich extremes, which could promote 2D growth mode of subsequent ZnSe with improved optical and electrical properties [48, 54].

In contrast to the widely studied ZnSe/GaAs interface, the GaAs/ZnSe interface was rarely investigated due to the fact that the underlying ZnSe decomposes at temperatures (around 400°C) lower than the typical growth temperatures of GaAs using MBE (around 580°C) [36, 54]. In order to examine the GaAs/ZnSe interface, therefore, the GaAs layers have to be grown at typical growth temperatures of ZnSe (*i.e.*, around 300°C), where the GaAs layers usually have poor crystalline quality. It was reported that the microstructure of GaAs layers grown on Zn-rich ZnSe at 300°C by MBE was observed to contain antiphase domains, which could degrade the surface quality of GaAs layers [54]. In this contribution, Migration

Enhanced Epitaxy (MEE) technique was used to develop GaAs epitaxial layers at temperatures as low as 200°C with adequate crystalline quality [55, 56]. Nevertheless, the ZnSe/GaAs/ZnSe quantum structures developed using MEE were only able to deliver desirable photoluminescence (PL) at extremely low temperatures due to poor interface quality [36, 37, 58-60]. Moreover, the surface termination of ZnSe and the initial growth layer of GaAs were proven to affect the GaAs/ZnSe interface quality [38, 48-52]. Understanding the structural and optical properties of GaAs/ZnSe interface in relation to the widely studied ZnSe/GaAs interface is, therefore, essential to realize high quality ZnSe-GaAs HS systems. Furthermore, previous studies showed that the p-type dopant in ZnSe is responsible for device degradation in LDs [30, 31]. In order to fulfill the needs of commercial products, methods to mitigate this problem, or new device architectures are needed for ZnSe-based devices.

In summary, ZnSe is a wide-gap semiconductor compatible to well-developed GaAs technology. The ZnSe-GaAs HS has great potential in novel electronic and photonic devices, and could fulfill the demands of current LED market. More detailed examinations on the nature of ZnSe-GaAs interface, as well as device fabrication and architecture are crucial for the further development of ZnSe-GaAs HS.

1.4 Chapter Overview

This study seeks to explore the application of MBE-grown ZnSe-GaAs system in various electronic and photonic devices, especially light emitting device. Chapter 1 gives the motivation as well as necessary background of this study. Chapter 2 looks in-depth at the ZnSe/GaAs and GaAs/ZnSe interfaces, which act as an essential building block for high quality ZnSe-GaAs HS and corresponding devices. Previous openended questions in this system are revisited, and effort has been made to optimize the interface quality and explain the mechanism. In Chapter 3, based on findings in Chapter 2, a common structure for light emitting devices, ZnSe/GaAs/ZnSe single quantum well is explored in detail. The interesting while complicated luminescence mechanism from single quantum well is examined, and the correlation with the fabrication procedure has been established. In addition, some preliminary results on light emitting device based on the single quantum well structure are demonstrated. This work can provide a solid foundation for the future device studies. In Chapter 4, attention is given to ohmic contacts for ZnSe-based devices. Both novel insitu grown aluminum (Al) contact and ex-situ grown cooper (Cu) contact have been investigated. They both exhibit intriguing properties as well as great potential for applications. Finally, Chapter 5 summarizes these results in this work and provides an outlook for potential future work in this explorable materials system.

2 Interface Studies of ZnSe-GaAs Heterovalent Structures (HS)

2.1 Introduction

As described in Chapter 1, ZnSe-GaAs heterovalent structure (HS) has long been recognized as a potential candidate for fabricating various optoelectronic devices including displays, light emitting diodes, and lasers with optimal chromaticity, which has potential to fulfill the ever-increasing demands of LED market. However, the heterovalent interfaces inhibits a practical way to integrate those two materials with tolerable interface defect density. We therefore revisit the growth of ZnSe-GaAs HS system with the aim of understanding the structural as well as the optical nature of ZnSe/GaAs and GaAs/ZnSe interfaces. The interfaces of ZnSe layers grown on MBE grown GaAs as well as MEE grown GaAs buffer layers were investigated in detail. Subsequently, the effect of the initial growth layer of GaAs on the quality of GaAs/ZnSe interfaces was examined. Room temperature (RT) PL and transmission electron microscopy (TEM) techniques were used to evaluate the optical as well as structural quality of these hetero-valent interfaces. An attempt has been made to establish a systematic correlation between the observed properties of these interfaces and the growth conditions used in this work.

2.2 ZnSe/GaAs Interface

The investigations in this study were started from the relatively well-studied ZnSe/GaAs interface. The ZnSe and GaAs layers in this study were grown in a single chamber Varian Gen II MBE system. The substrates used were n-type GaAs with (100) orientation and exhibit an etch pit density (EPD) < 500 cm⁻². Prior to growth, the substrates were baked in the load-lock chamber at a temperature of 300°C for three hours to remove the absorbed water vapor. Subsequently, the GaAs substrates were treated thermally in the growth chamber at ~610°C under As overpressure to remove the native substrate oxide layer. The thermal treatment process was continued until an intense single crystalline diffraction pattern was confirmed by

RHEED. In order to provide a better-quality growth surface for ZnSe growth, a 500 nm thick Si-doped GaAs buffer layer was grown on oxide removed GaAs substrates at 580°C and with a V/III flux ratio of \sim 15. Streaky RHEED with (2 ×4) As-rich pattern was observed during GaAs buffer layer growth. The grown ZnSe-GaAs HS samples were characterized ex-situ using PL and TEM. All PL characterizations were measured by a 405 nm excitation laser with maximum power of \sim 51 mW at RT. For different incident laser power measurements, the laser power was altered by neutral density filters and calibrated by a power meter. The microstructural and interface investigations were carried out using JEOL JEM 2100F-AC TEM, operating at an accelerating voltage 200 kV. The cross-sectional TEM lamella in this study were prepared using FEI Scios dual-beam focused ion beam (FIB).

Previously, the MBE ZnSe is typically grown by two different ways: from a ZnSe compound source [61] or from separated Zn and Se elemental source [62, 63]. In this work, the ZnSe compound source is embedded in the MBE chamber responsible for other III-V growth, which is a major difference from other studies. In order to verify the quality of grown ZnSe epi-layer, some properties of unintentional doped (UID) ZnSe grown from compound source (this work) and elemental source (from references) are given below for comparison purpose. A RT-PL response of UID ZnSe to a 405 nm excitation laser is shown in Figure 2.1. As shown in Table 2.1, the ZnSe grown from compound source doesn't have significant difference with those from elemental source in terms of mobility and band-edge PL full width at half maximum (FWHM), which are typically indicators of crystal quality. The ZnSe layers grown using compound source material has lower mobility due to the typical lower purity of compound source material compared to elemental sources. Besides, the ZnSe in this work was grown in the MBE chamber for III-V growth, while those from elemental source were done in a separated II-VI chamber. The different background environment could possibly have some influence on the incorporated defect concentration and/or ZnSe stoichiometry. The carrier concentration of UID ZnSe from compound source is close to elemental source, and the PL response (Figure 2.1) is dominant by band-edge emission, which suggests that the ZnSe layer in this work doesn't contain significant concentration of defects or has a major stoichiometry issue.

Therefore, the MBE growth configuration in this work will not alter the properties of grown ZnSe layer in any significant ways. The other advantages/disadvantages of this configuration will be elaborated in the following paragraphs.

	Mobility (300K) (cm²/V-s)	UID carrier concentration (cm ⁻³)	Band-edge PL FWHM (300K) (nm)
Compound source	303	3.46×10 ¹⁶	8.03
Elemental source	380 [62]	2.5×10 ¹⁶ [62]	8.14 [63]

Table 2.1. Comparison of some properties of UID ZnSe grown from compound or elemental source.



Figure 2.1. RT-PL response of UID ZnSe grown from compound source on GaAs. The spectrum is dominant by the band-edge emission at 460 nm, with ignorable defect peak at around 600 nm.

Since there are many different samples used in this chapter, a list of samples that have been used in this chapter were tabulated in Table 2.2 along with the growth conditions used. The details of those samples will be given later in this Chapter. For ZnSe/GaAs interface study, ~ 700 nm thick Ga-doped ZnSe layers were grown at 300°C on different surface terminated GaAs buffer layers in the same MBE growth chamber (Figure 2.2(a)). The ZnSe growth was initiated only after As background pressures brought by GaAs stabilized low enough in the growth chamber to prevent ZnSe from unwanted doping effects. The background pressure in the chamber was constantly monitored by residual gas analyzer (RGA). An effusive cell with compound ZnSe source material was used to provide the beam flux for ZnSe growth [61]. A c(2 \times 2) Zn-rich RHEED patter was observed during the growth of ZnSe. Prior to ZnSe growth, the surface structures of GaAs buffer such as the as-grown (2 \times 4) As-rich surface and (4 \times 2) Ga-rich surface of GaAs buffers were confirmed by RHEED. The (4 \times 2) Ga-rich surface was obtained via thermal annealing of GaAs buffers at 560°C, and in the absence of As environment. For comparison purpose, a ZnSe/GaAs heterostructure was grown, where GaAs buffer was grown at low temperatures (LT) 300°C and at V/III \sim 1. The lower V/III \sim 1 was used to prevent excess As incorporation in bulk GaAs at LTs, as excess As is known to suppress the radiative recombination [65].

Sample ID	Stack Structure	Growth Temperatures	V/III Ratio of GaAs
А	ZnSe/Ga-terminated GaAs	300 °C/580 °C	~15
В	ZnSe/As-terminated GaAs	300 °C/580 °C	~15
С	ZnSe/LT-MBE GaAs	300 °C/300 °C	~1
D	ZnSe/LT-MEE GaAs	300 °C/300 °C	NA
Ε	Ga-initialized GaAs/Zn-rich ZnSe	300 °C/300 °C	NA
F	As-initialized GaAs/Zn-rich ZnSe	300 °C/300 °C	NA

Table 2.2. Stack structures, growth methods, and growth conditions of the samples used in this chapter.

Figure 2.2(b) shows the band-edge PL emission spectrum obtained from the ZnSe layers grown under identical conditions on different GaAs buffers, including the Ga-terminated GaAs (sample A), Asterminated GaAs (sample B), and LT-MBE GaAs (sample C) in Table 2.2. The surface termination of GaAs buffers was confirmed by RHEED, prior to the growth of ZnSe, including the (2×4) As-rich and (4×2) Ga-rich GaAs surface. Since a large portion of GaAs PL signal will come from the GaAs substrate, which could bring ambiguity to this study, ZnSe PL was used to measure the interface quality.

As expected, the ZnSe layer grown on Ga-terminated GaAs (sample A) exhibits a high intense band-edge emission when compared to ZnSe/As-terminated GaAs (sample B) and ZnSe/LT-MBE GaAs (sample C) in Table 2.2. Although, the growth conditions of ZnSe layers were identical in this study, it appears that the surface termination of GaAs buffer strongly influences the quality of ZnSe layers and hence the band-edge emissions. The variation in PL intensity that we see in Figure 2.2(b) is, therefore, attributed to the interface quality of these samples. Our results confirm that ZnSe/Ga-terminated GaAs interface has superior quality than ZnSe/As-terminated GaAs. Moreover, the long wavelength defect peaks that are commonly observed in the PL spectrum of ZnSe are minor in this study [61]. This suppression may be attributed to the Zn-rich growth condition in this study using ZnSe compound-source material [61].



Figure 2.2. (a) Sample stack structure for ZnSe/GaAs interface study, (b) PL responses of ZnSe layers on different MBE GaAs buffer layers (sample A, B, C in Table 2.2) and cross-sectional TEM micrographs of ZnSe/Ga-terminated GaAs (sample A) heterostructure acquired under various operating reflections along the [001] orientation, (c) shows the microstructures of ZnSe and GaAs epi-layers obtained under two-beam bright field conditions for g=400 reflection, (d) & (e) shows the corresponding microstructures of ZnSe and GaAs obtained under weak-beam dark field microscopy conditions, and for g=200 and 400 reflections.

The bulk microstructural and interface quality of ZnSe/GaAs sample which delivered best PL response (*i.e.*, sample A) was examined by TEM. Figure 2.2(c)-(e) shows the corresponding cross-sectional

TEM micrographs along the [001] direction as indicated by the selected area diffraction (SAED) patterns. The results show that both the GaAs and ZnSe bulk epitaxial layers of sample A exhibit superior microstructural quality (see Figure 2.2(c)). The nature of ZnSe/Ga-terminated GaAs interface has been examined by weak beam dark field microscopy for the operating reflections g = 200, and g = 400 in Figures 2.2(d) and 2.2(e). It should be noted that the weak beam dark field images do not show any complementary contrast (bright and dark) along the interface for g = 200 and 400 reflections (indicated by red arrows in Figure 2.2(d) and 2.2(e)), suggesting that the ZnSe/GaAs interface of sample A contains no signature of Ga-Se (*i.e.*, Ga₂Se₃) compound transition layer formation at the interface.

With the aim of understanding further the interface structure of sample A, high-resolution TEM investigations were carried out at the ZnSe/Ga-terminated GaAs interface, however, along the [011] orientation (see Figure 2.3(a)). It can be seen that the interface is highly coherent without any misfit dislocations. The chemical composition of these layers across the interface was examined by scanning TEM coupled with the energy dispersive spectroscopy (EDS) in Figure 2.3(b). It should be noted that the composition of ZnSe and GaAs atomic constituents varies abruptly at the interface within a thickness range of ~ 6 nm. The Fast Fourier Transform (FFT) obtained from this ultra-thin 6 nm interface layer is provided in Figure 2.3(a), along with the FFTs of the corresponding bulk GaAs and ZnSe layers. It can be seen that all the three FFTs are similar, and especially the FFT obtained from the interface region is not different from the FFTs obtained for ZnSe and GaAs epitaxial layers. This result suggests that the 6 nm interface layer is similar in structure to bulk ZnSe, and GaAs layers, however, chemically it is expected to contain a mixture of GaAs and ZnSe atomic constituents. The corresponding extracted lattice parameters are 0.5769 nm, 0.5702 nm, and 0.5741 nm respectively for the bulk ZnSe, interface layer, and bulk GaAs layer.

The TEM results in this work, therefore, suggest that the ZnSe/Ga-terminated GaAs interface (sample A) has a transition layer which is entirely different in nature from the commonly observed Ga₂Se₃ transition layer. The EDS and high-resolution TEM analyses suggest that the interface layer has a structure similar to ZnSe and GaAs, and contains all the four atomic constituents with variable concentration.



Figure 2.3. (a) Cross-sectional high-resolution TEM micrograph of ZnSe/Ga-terminated GaAs (sample A) heterostructure along [011] orientation. The corresponding FFTs have been acquired at different regions of the image, (b) shows the scanning TEM image of the same heterostructure along the with the EDS line scan profiles across the interface.

Earlier CV and PS investigations revealed that the ZnSe/Ga-terminated GaAs interface has the lowest interface state density [45, 47, 48], which was lower than the usual ZnSe/As-terminated GaAs interface obtained under As-rich MBE growth conditions. The results in the current study show that the MBE grown ZnSe/Ga-terminated GaAs hetero-structure (sample A) has the best optical as well as structural quality when compared to sample B. Many investigators studied the nature of the transition layer which forms at the interface of ZnSe/Ga-terminated GaAs [43, 51, 64]. It was reported that the transition layer has a structure similar to zinc-blende Ga₂Se₃ and exhibits a bright and dark contrast at the interface of ZnSe/GaAs for the operating reflections g = 200 and 400 in the weak beam dark field TEM [43]. In a later study, Dai *et al.* [66], intentionally grown a thin Ga₂Se₃ compound layer on Ga-terminated GaAs surface

and observed vacancy ordering in Ga₂Se₃ layer. The TEM results in the current study revealed no signature of Ga₂Se₃ at the ZnSe/Ga-terminated GaAs interface. The absence of complementary contrasts along the interface for g = 200 and 400 reflections in dark field TEM images confirm the same (Figures 2.2(d) and (e)). Furthermore, the FFT analysis doesn't reveal any spots corresponding to vacancy ordering at the interface (Figure 2.3). Importantly, the extracted lattice parameter of the interface (*i.e.*, 0.5702 nm), which is higher than the lattice parameters reported for Ga₂Se₃ in literature: 0.529 nm, 0.538 nm [43, 51], suggesting that the interface in this work has a different nature. The extracted lattice parameter of the interface is (0.5702 nm) is comparable to the lattice parameters of bulk ZnSe (0.5769 nm) and GaAs (0.5749 nm) respectively. Chemically, this interface is found to have a thickness of ~ 6 nm with the presence of ZnSe and GaAs atomic constituents, suggesting that the interface may be an intermixture of Zn, Ga, As, and Se atoms situated in a zinc-blende structure with variable composition over a range of 6 nm in thickness. No complementary contrasts are observed for this intermixed layer for g = 200 and 400 reflections in the TEM dark field images due to the close values of atomic scattering factors associated with Zn, Ga, As, and Se atoms. It was suggested that the intermixing at ZnSe/GaAs interface could occur due to the interdiffusion of Zn and Ga atoms during the post-growth annealing of ZnSe/GaAs layers [67]. In relation to this observation, the ZnSe growth in the current study was performed at 300°C for a relatively longer time on a Ga-rich GaAs surface. We speculate that the observed 6 nm of intermixed region in this study, therefore, may be attributed to the inter-diffusion of atomic species across the interface during ZnSe growth.

Moreover, the superior quality of ZnSe/Ga-terminated GaAs hetero-structure (sample A) can be rationalized from the observations proposed by Farrell *et al.* [54], where it suggested that a ZnSe/GaAs interface consists of 50% Ga-Se and 50% Zn-As bonds maintains the charge neutrality, thus, provide high quality ZnSe layers in 2D growth mode. The EDS observations in this study revealed the intermixing nature of ZnSe/GaAs interface (Figure 2.3(b)), however, it doesn't provide the actual stoichiometry of the interface. On the other hand, electron counting model suggested that the bonding between ZnSe and pure Ga-terminated GaAs surface cannot directly satisfy charge neutrality without the formation of transition layers,

like Ga₂Se₃ [39, 54]. Since there is no trace of Ga₂Se₃ formation in this study, inter-diffusion could be an alternative way to satisfy charge neutrality. It appears that the inter-diffusion of atomic species across the ZnSe/GaAs interface resulted in a stable configuration which could yield high quality ZnSe given the growth conditions used in this study.

The formation of Ga₂Se₃ layer at the conventional ZnSe/GaAs interface in earlier studies may be attributed to the exposure of GaAs surface to Se beam flux prior to the growth of ZnSe [45, 48]. It was also suggested that the formation of Ga₂Se₃ can be prevented by exposing GaAs surface to Zn beam flux prior to ZnSe growth [45, 48]. It should be noted that in earlier studies the ZnSe/GaAs hetero-structure growth was performed in two separate MBE chambers using elemental source materials as precursors for GaAs and ZnSe [47, 48]. In these studies, prior to the growth of ZnSe, the as-grown GaAs samples were transferred to II-VI chamber and were annealed under the ambient of Se to obtain Ga-rich GaAs surface [45, 47, 48]. The reaction between Se and Ga-rich GaAs surface could result in the formation of Ga₂Se₃ compound layer on the GaAs surface [43, 47, 48]. In contrast to these earlier studies, in the current work both the GaAs and ZnSe depositions were conducted in a single MBE chamber using Ga and As elemental sources for GaAs and a compound source material for ZnSe. As a consequence, there were less chances for Se species to react with the Ga-rich GaAs surface during the annealing process and to form Ga₂Se₃. The absence of Ga₂Se₃ at the interface of ZnSe/GaAs (sample A) in our study may be attributed to the use of compound-source material for the growth of ZnSe on a Ga-rich GaAs surface in a single MBE chamber.

Previous studies showed that the ZnSe layers grown using compound-source material contains high concentration of impurities and has lower mobility due to the typical lower purity of compound-source material compared to elemental sources [61, 68]. However, the use of compound-source material allows us to better maintain the GaAs surface chemistry by reducing the background Zn and/or Se species especially in the case of single chamber MBE systems. Therefore, we believe that compound-source material could be a better choice to obtain II-VI/III-V heterostructures with optimum quality especially when single growth chambers are used for the growth of these materials.

2.3 Optimization of GaAs LT-MEE Growth

Because the realization of ZnSe-GaAs HS system requires the GaAs layers to be grown at LTs compatible to ZnSe. In this contribution, we have examined the comparative performance of ZnSe/LT-MBE GaAs (sample C in Table 2.2), in which the GaAs buffer was grown at temperatures compatible to ZnSe growth, *i.e.*, 300°C and at a V/III ratio ~ 1 to avoid excess As in bulk GaAs materials [65]. It can be seen that sample C indeed compromised the PL intensity greatly (see Figure 2.2(b)), further proving other epitaxy technique than regular MBE is required to develop high quality GaAs layers at LT for the realization of HS.

Having established that the PL intensity of ZnSe/Ga-terminated GaAs (sample A) in this study as a standard reference, we have proceeded further to develop high quality GaAs buffer layers at LTs compatible to ZnSe. We optimized the LT-MEE GaAs growth conditions and grown a ZnSe/LT-MEE GaAs heterostructure similar to samples in Chapter 2.2 (Figure 2.2(a), 700 nm Ga-doped ZnSe) for a comparative study. The LT-MEE GaAs layers were grown at 300°C with fixed Ga amount (1 ML) and varying As amount per cycle [51, 52] using both As₄ and As₂ (see Figure 2.3(a)). The relationship between the number of surface sites and the beam flux pressure was derived from elsewhere [51, 52]. All LT-MEE buffer layers were 100 nm (*e. g.* sample D). In this contribution, the LT-MEE growth conditions were optimized by varying the As amount per cycle at a fixed Ga amount (1 ML). Initially, a ZnSe/GaAs sample was grown, where the 100 nm LT-MEE GaAs layer was grown at 300°C and with a Ga beam flux equal to ~ 1 ML/cycle and As₄ ~ 0.5 ML/cycle [51, 52]. However, the resulting PL intensity from this sample was nearly as low as the LT-MBE GaAs buffer (sample C), although the RHEED pattern remained streaky during the growth. This might be explained by the deficient associativity of As₄ at LTs. In order to verify that, a set of ZnSe/GaAs samples were grown, where the 100 nm LT-MEE GaAs layers were grown for various amount of As₂ per cycle. The normalized PL band-edge emission intensity of ZnSe obtained from these samples versus the amount of As₂ per cycle used, is plotted in Figure 2.4(b). It can be seen that ZnSe PL intensity increases with the amount of As₂ per cycle, and reaches the optimal value when the As₂ dimmers supplied per cycle was precisely equal to the number of surface sites of GaAs (100) surface. From the prospective of PL performance, the optimized ZnSe/LT-MEE GaAs interface (sample D) was nearly as the same quality as the widely believed least defective ZnSe/Ga-terminated GaAs interface (sample A). Therefore, the same optimized growth conditions of LT-MEE GaAs (sample D) were used in the subsequent studies.



Figure 2.4. (a) MEE growth process schematic diagram of each one cycle used in this work. (b) PL peak responses intensity of ZnSe layers on different LT-MEE GaAs buffer layers and (c) proposed model during the bonding procedure of MEE GaAs growth using As₂.

As for the reason behind the optimized As_2 dose per cycle, we proposed the explanations as the following. Because one As_2 dimmer has two As atoms, during the bonding process, half of the absorbed dimmers were left behind for bonding and the other half will re-evaporate (see Figure 2.4(c)). Similar assumption was also proposed in [52], but for As_4 . Previous works have shown that the crystal quality of

MEE GaAs has a high sensitivity of As amount per cycle due to the high As sticking coefficient to both Ga and As surfaces at LT [52]. Deficient As will lead to unoccupied surface sites, and excess As at LT will occupy Ga site and result in island nucleation. Therefore, in both cases the growing surface will be roughed, and several defects could be incorporated during growth. That could further degrade the interface quality and PL performance of following ZnSe layer. The optimized growth condition could also be seen from RHEED patterns, when the As₂ amount per cycle was deficient or excess, spotty RHEED patterns were observed during growth, which is related to a 3D island growth mode. And the optimized As₂ amount gave rise to smooth growth by streaky RHEED. The slightly different starting growth surfaces could lead to ZnSe layer with various optical performance, which further proves the importance for the interface studies.

2.4 GaAs/ZnSe Interface

Having established that the LT-MEE technique can produce ZnSe/GaAs interfaces (sample D) which are comparable to the standard MBE based ZnSe/Ga-terminated GaAs (sample A), we turned our attention to investigate the LT-MEE GaAs/ZnSe interfaces. The GaAs/ZnSe interface has been identified as the bottleneck in the development of ZnSe-GaAs HS. A systematic investigation of GaAs/ZnSe interface, therefore, is essential for the development of HS.

For GaAs/ZnSe interface study, ~100 nm thick LT-MEE GaAs layers were grown on $c(2 \times 2)$ Znrich ZnSe at 300°C. Both the Ga-initialized and As-initialized LT-MEE GaAs layers were grown on ZnSe (see Figure 2.5(a)). The Ga-initialized GaAs growth was initiated by depositing a Ga ML on $c(2 \times 2)$ Znrich ZnSe surface at 300°C. In contrast, the As-initialized LT-MEE GaAs growth involves various steps: initiating the GaAs deposition at low temperatures below 80°C to achieve high As sticking coefficient on ZnSe surface [37], annealing the grown GaAs at 300°C to obtain single crystal RHEED pattern, and then continuing further MEE GaAs growth at 300°C. The processing cycle used for As-initialized MEE GaAs growth is described in Figure 2.5(d).


Figure 2.5. (a) Sample stack structure for GaAs/ZnSe interface (sample E and F in Table 2.2), (b) PL peak responses intensity versus incident laser power from ZnSe layers under different initialized MEE GaAs conditions, (c) RHEED pattern during MEE GaAs growth on ZnSe and (d) Illustration of procedure used to grow As-initialized GaAs on ZnSe surface.

In this study, we carefully controlled the initial growth layer of LT-MEE GaAs on $c(2 \times 2)$ Zn-rich ZnSe surface by the methods mentioned above. It is observed that both the Ga-initialized GaAs/ZnSe and As-initialized GaAs/ZnSe samples have a decent ZnSe PL intensity (samples E and F in Table 2.2). Nevertheless, it was difficult to examine the absolute value of the intensity quantitatively since the top ~100 nm GaAs layers on ZnSe absorb the incident laser and ZnSe emission signals. Moreover, the top GaAs layers were too thin to produce significant PL intensity. Instead, Figure 2.5(b) shows the ZnSe PL bandedge emission peak intensity as a function of incident laser power obtained for the samples E and F. The plot is a good qualitative indicator of defect density, since the defect states trap the excited carriers and influence the rate of radiative recombination. At lower incident laser powers, most of the laser energy will be consumed to fill the available defect states, provided the density of defect states is relatively fixed per sample. Consequently, the plot will exhibit a strong nonlinearity if the defect states play a dominant role. From Figure 2.5(b), It can be seen that the As-initialized GaAs/ZnSe (sample F) exhibits a strong nonlinear PL response, whereas the Ga-initialized GaAs/ZnSe (sample E) exhibits a more linear PL response. Moreover, the absorption coefficients of ZnSe and GaAs are high for 405 nm laser, which has much higher energy than their band-gaps, the corresponding defect states should be near the surface, especially the GaAs/ZnSe interface. The result in this study indicates that the As-initialized GaAs/ZnSe interface (sample F) is more defective. Besides, the RHEED pattern showed some transitional behavior from spotty to streaky for both the samples during growth (Figure 2.5(c)), suggesting that both the interfaces were not ideally abrupt and flat, and a 3D to 2D growth mode transition might have occurred during the interface formation.

The structural quality of Ga and As-initialized LT-MEE GaAs/ZnSe interfaces (samples E and F in Table 2.2) were investigated by TEM. Figure 2.6(a) and 2.6(b) shows the corresponding cross-sectional TEM bright field micrographs along the [012] orientation of GaAs/ZnSe interface, and for the operating reflection g = 400. The SAED patterns were acquired from the GaAs/ZnSe interface regions. The following observations were made from these two micrographs: the interfaces between LT-MEE GaAs and ZnSe layers are quite rough, both MEE GaAs layers are highly defective, and a defective transition region is present beneath the As-initialized GaAs layer (sample F) as indicated by the yellow-colored dashed lines in Figure 2.6(b).

The interface quality of LT-MEE GaAs/ZnSe layers were investigated by weak beam dark field microscopy in Figures 2.6(c) to 2.6(f). It can be seen that the top thin Ga and As-initialized GaAs layers exhibit a bright contrast for g = 400 operating reflection, and dark contrast for g = 200 reflection (indicated by red arrows in Figures 2.6(c) to 2.6(f)). It should be further noted that the As-initialized GaAs/ZnSe (sample F) interface exhibits a continuous bright contrast for g = 200 reflection as indicated by blue arrow in Figure 2.6(f), whereas the bright contrast is absent for Ga-initialized GaAs/ZnSe (sample E) interface for the same g = 200 reflection (Figure 2.6(e)). Importantly, the bright contrast is absent for g = 400 reflection

in both the MEE GaAs/ZnSe interface layers (Figures 2.6(c) and 2.6(d)). These observations imply that the Ga and As-initialized GaAs/ZnSe interfaces (samples E and F) are different in nature. It appears that the non-linear PL behavior of the As-initialized GaAs/ZnSe sample seen in Figure 2.5(b), could be attributed to the defective transition region present along the interface.



Figure 2.6. Cross-sectional TEM micrographs of the Ga-initialized GaAs/ZnSe and As-initialized GaAs/ZnSe heterostructures (samples E and F in Table 2.2) along the [012] orientation. (a) & (b) shows the corresponding microstructures acquired under two-beam bright field diffracting conditions and for the g=400 reflection. (c), (d), and (e), (f) shows the images of the same heterostructures under weak beam dark filed microscopy conditions for g=400 and 200 operating reflections. The red and blue colored arrows indicate the position of top GaAs layers and the position of GaAs/ZnSe interface.

In contrast to the well-established ZnSe/GaAs interface, the GaAs/ZnSe interface was less investigated [38, 54], due to the difficulties involved in the deposition of this hetero-structure. For instance, ZnSe decomposes below the conventional growth temperatures used for MBE GaAs [36, 54]. In order to realize GaAs/ZnSe interface, the GaAs layers, therefore, have to be grown at temperatures as low as 300°C *i.e.*, where the ZnSe deposition usually occurs. However, the LT-MBE GaAs layers obtained under conditions favorable to ZnSe, exhibit poor crystalline quality, and poor optical performance due to incorporation of excess As in the bulk of GaAs. The PL response obtained from the ZnSe/LT-MBE GaAs (Figure 2.2(b), sample C in Table 2.2) in the current study confirms the same. Moreover, the chemical valance mismatch at the GaAs/ZnSe interface adds further difficulty [38-40]. The alternative option is to use a different growth method such as MEE, which is known in producing high quality GaAs epitaxial layers at low growth temperatures [51, 52]. In MEE growth, the Ga and As precursors are supplied alternatively to enhance the mobility of Ga adatoms at such low growth temperatures, and to achieve high crystalline quality [51, 52]. The other advantage with MEE is its ability to control the interface configuration by different initial modes. As a validation, we have employed this technique to initially produce ZnSe/LT-MEE GaAs hetero-structures (sample D) with optical repose comparable to the conventional ZnSe/Gaterminated GaAs (sample A) and we were successful. Having established that, we have subsequently grown ~100 nm thick LT-MEE GaAs layers on $c(2 \times 2)$ Zn-rich ZnSe surfaces (samples E and F in Table 2.2) under different initializations of GaAs. However, the LT-MEE GaAs/ZnSe interfaces obtained were quite rough (see Figure 2.6). The evolution of surface roughness was monitored from the transition of RHEED patterns. During the growth of first few monolayers of GaAs for both the interfaces, the RHEED exhibited spotty pattern (Figure 2.5(c)), which can be correlated to the 3D growth mode of GaAs and hence the associated GaAs/ZnSe interface roughness. Previous studies showed that the deposition of GaAs at low temperatures using MBE on $c(2 \times 2)$ Zn-rich ZnSe surfaces resulted in GaAs layers with 3D growth morphology up to a thickness of 200 nm, then subsequently transformed to a 2D growth mode [54]. The rough morphology in these layers was correlated with the presence of antiphase domains [54]. However, Se pre-deposition followed by a low temperature deposition of one-half ML of Ga prior to the deposition of GaAs at 300°C, resulted in a decrease in 3D to 2D transition thickness to 20-25 nm of GaAs [54]. Though our GaAs layers were grown using MEE at 300°C, they also exhibited 3D growth mode for the first few nano meters followed by a transition to 2D mode. We didn't measure the actual thickness at which this transition occurs, however, we have seen this transition within a minute from the time at which GaAs growth started, which can be correlated to an approximate thickness less than 10 nm.

Although structurally the interfaces are quite rough, both the samples E and F still showed decent ZnSe PL response, but exhibiting different dependency on the incident laser powers (Figure 2.5(b)). Our results show that the As-initialized GaAs/ZnSe sample exhibits a strong non-linearity in PL response (Figure 2.5(b)), suggesting the more defective nature of this interface. Moreover, a defective transition region with complementary contrast (bright and dark) was observed along the As-initialized GaAs/ZnSe interface for g = 200 and 400 reflections (Figure 2.6(d) and 6(f)). The TEM analysis in this study indicates that the transition region should have a structure factor higher than ZnSe and GaAs for g = 400 reflection, and lower than ZnSe and GaAs for g = 200 reflection (see Figure 2.6(f)) and dark for g = 400 reflections (Figure 2.6(d)). Kuo *et al.* [51], observed a similar bright contrast region along the ZnSe/GaAs interface for the conditions where the As-stabilized GaAs surface was treated with Zn. It was suggested that the transition region consists of Zn, As and vacancies as constituents and similar to Zn₃As₂ compound layer [51]. We believe that the defective transition region observed in this work along As-initialized GaAs/ZnSe interface is attributed to the formation of Zn₃As₂ compound layer.

The formation of Zn_3As_2 defective transition region may be explained from the process cycle used in this study (Figure 2.5(d)). The initial As exposure at 80°C to c(2x2) Zn-rich ZnSe surface coupled with the subsequent temperature ramp up and anneal processes could induce the reaction between As-initialized GaAs and Zn-rich ZnSe surface [67], resulting in the formation of a transition region similar to Zn₃As₂ with structure factor higher (lower) than ZnSe and GaAs for 200 (400) operating reflections (Figure 2.6(d) and 2.6(f)). A similar transition region was not observed along the Ga-initialized GaAs/ZnSe interface (Figure 2.6(e)). However, the Ga-initialized GaAs/ZnSe interface (sample E) obtained in this study was not abrupt as well. The interface roughness associated with the Ga-initialized GaAs/ZnSe interface may be explained from the reaction between the initial Ga and ZnSe surface. Previous studies show that group III (Ga, In) liquid droplets could be formed during the growth of III-V materials using MBE, and they could alter the interface properties [69, 70]. Chen *et al.* reported that during the growth of InAs on GaP, the initial In adlayer could form liquid droplets and dissolve GaP surface, resulting a rough interface between InAs/GaP [69]. It was also reported that Ga droplets could dissolve ZnSe during the growth of GaAs on ZnSe [70, 71]. It appears that a similar reaction might have occurred for sample E, during the Ga-initialization on Zn-rich ZnSe at 300°C, and it resulted in a rough interface between GaAs/ZnSe.

We believe that the findings in this chapter could provide a better understanding of the nature of interfaces for the realization of ZnSe-GaAs HS, using the combination of MBE and MEE as growth techniques. However, further optimization of growth conditions may require to practically realize GaAs/ZnSe/GaAs interfaces with tolerable defect density.

2.5 Summary

Systematic investigations on both the ZnSe/GaAs and GaAs/ZnSe interfaces for the realization of ZnSe-GaAs HS were performed using PL and TEM. For ZnSe/GaAs interface, the ZnSe/Ga-terminated GaAs is found to deliver excellent PL performance. Detailed TEM investigations of this interface excluded the possibility of Ga₂Se₃ formation at the interface, instead an intermixed interface consisting of ZnSe and GaAs atomic constituents with variable composition was confirmed. An optimized low temperature MEE procedure using As₂ was used to develop the GaAs layers with adequate GaAs/ZnSe interface quality, which could resolve the previous challenges involved in the deposition of GaAs at low temperatures, while

maintaining the adequate interface quality. Both the Ga and As-initialized LT-MEE GaAs/ZnSe interfaces were investigated, where the As-initialized GaAs/ZnSe interface is found to be more defective and associated with a transition region corresponding to Zn_3As_2 . The observed properties of ZnSe/GaAs and GaAs/ZnSe interfaces were discussed in detail in relation to the growth conditions used in this study. We believe that the findings in this study are important to understand the nature of these interfaces for the realization of high quality ZnSe-GaAs HS.

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3 Studies of ZnSe/GaAs/ZnSe single quantum well (QW)

3.1 Introduction

Quantum well is a quantum physics concept. It could be demonstrated by particles under quantum confinement. Figure 3.1(a) shows a scheme of a finite quantum well. The particles inside the well, which can move freely initially, are now confined by two big potential barriers. When the quantum well thickness is thin enough (comparable to the de Broglie wavelength of particles), the particle's energy inside the well is not continuous anymore. Instead, discrete energy levels depending on the quantum well thickness appear inside the well, and the particles can only occupy those discrete energy levels.

For semiconductors, a quantum well can be realized by semiconductor heterostructures with different band-gaps (E_g). The semiconductor quantum well was developed in 1970 by Esaki and Tsu [72]. Figure 3.1(b) shows a semiconductor quantum well by a double-heterostructure (DH). Basically, a narrow band-gap semiconductor layer (*e. g.* GaAs) is sandwiched by two wide-gap semiconductors (*e. g.* AlGaAs). When the middle layer is thin enough, the DH acts as a quantum well. Since the energy states inside the narrow-gap semiconductor are discrete due to quantum effects, its effective band-gap is not the original E_g anymore. And clearly, the effective band-gap can be altered by the quantum well thickness. Therefore, by utilizing quantum confinement effects, the properties of semiconductor devices can be finely tuned. The development of semiconductor devices using heterostructures and quantum effects resulted in Nobel Prize of Physics in 2000.



Figure 3.1. Schemes of (a) a finite quantum well with discrete energy levels E_1, E_2, \ldots, E_n and (b) a semiconductor quantum well by a double heterostructure, CB and VB stand for conduction band and valence band.

The DH structure is widely used for various semiconductor LEDs including AlGaAs, AlGaInP, and GaN [4, 9]. It has two main advantages [4]: firstly, the carriers are confined by the wide-gap materials inside the active layer (quantum well). Therefore, it prevents the loss of carriers into nonradiative recombination centers such as surface states, defects by drift field, and thus improves the efficiency of LEDs. Secondly, the emitted photon has an energy approximately equal to the effective band-gap of the active layer. Therefore, the emission wavelength could be finely tuned by the quantum well thickness. However, the fabrication of a semiconductor quantum well is not trivial practically. It requires high quality semiconductor hetero-interfaces. A defective interface contains a high density of interface states, which act as nonradiative recombination centers for carriers. Instead of recombining radiatively, most carriers in the active layer will non-radiatively recombine through the interface states, and thus reduce the luminescence efficiency.

Therefore, high-quality interface is an essential requisite of semiconductor quantum structures. Accordingly, being able to observe quantum effect is also an indicator for the quality of semiconductor heterostructure. ZnSe-GaAs DSS is a complicated quantum system. Many researchers have studied several ZnSe-GaAs quantum structures including quantum wells and superlattice. However, the quantum structures developed were only able to deliver desirable PL at extremely low temperatures due to poor interface quality, or lack of the evidence for quantum effects [36-37, 58-60, 72-75]. Having established a deep understanding as well as an effective fabrication procedure for ZnSe-GaAs HS in Chapter 2, we hereby carried out studies of the ZnSe/GaAs/ZnSe single QW structure.

3.2 Fabrication Methods for ZnSe/GaAs/ZnSe QWs

To begin with, we firstly fabricated a simple ZnSe/GaAs/ZnSe QW structure as shown in Figure 3.2(a). The ZnSe and MBE GaAs buffer growth procedures were as the same as described in Chapter 2.2. The GaAs QW was grown by LT-MEE technique described in Chapter 2.3, with Ga-initialized mode, since it was proved to be less defective. However, the room-temperature (RT)-PL response of as-grown sample (see Figure 3.2(b)) to a 405 nm laser didn't show much difference compared to a plain ZnSe/GaAs heterostructure: the emission spectrum is dominant by ZnSe band-edge emission, with a neglectable defect peak centered at around 600 nm.



Figure 3.2. (a) Sample stack structure of ZnSe/GaAs/ZnSe single QW and (b) RT-PL response to a 405 nm excitation laser of the single QW.

Previous researchers also used to fabricate ZnSe/GaAs/ZnSe QW structures by both MBE and MEE with QW thickness from ~3 nm to ~10 nm [58, 59]. They observed QW-related PL peaks only at 9 K. And the PL peaks were largely broadened when the QW thickness was reduced [58, 59]. Also, ZnSe/GaAs/AlGaAs QW was fabricated by another group of researchers [57] and it exhibited desired PL peaks. But the GaAs/AlGaAs interface was widely known to have low intensity defect density, which is not the case for GaAs/ZnSe as described previously in Chapter 2. At low-temperature (LT), the defect states will be inactive due to the so-called freeze-out of semiconductors. Therefore, it is possible to observe the QW PL peaks at LT even if the interface is defective. In our case, the naïve trial of single QW sample didn't exhibit any QW-related features in terms of PL at RT. It suggested that the interface quality was still not tolerable even after the optimized LT-MEE procedures. Because of the complicated heterovalent interface and unideal low-temperature growth procedure, we believe it is very challenging to obtain high quality interface free of optically active defects through direct growth methods. However, during the previous interface studies in Chapter 2, an interesting phenomenon was observed for Ga-initialized GaAs/ZnSe interface (see Figure 3.3). The Ga-initialized GaAs/ZnSe interface was not perfectly flat. Importantly, it showed some faceted features along the interface (Figure 3.3). Earlier studies showed that group III (Ga, In) liquids could form during MBE growth and alter the interface property [69, 70]. Since Ga droplets could form during Ga-initialized MEE growth of GaAs on ZnSe, and ZnSe could dissolve in Ga solution [71], we believe similar effect could explain the faceted interface: incident Ga atoms during the initial Ga layer formation could "etch" the underneath ZnSe layer and result in the faceted interface. Furthermore, the exposed interface facet surface was determined to be (111) orientation. Since the (111) planes in zinc blende crystal structure have the highest surface density of atoms, it would slow down the etch process of liquid Ga. That might explain the observations in Figure 3.3.



Figure 3.3. High-resolution TEM micrographs of Ga-initialized GaAs/ZnSe interface, faceted interface feature is marked with orange line.

Since it was proved that abrupt ZnSe-GaAs interfaces are almost inevitable to have interface states, compositionally graded interface might be able to provide a smooth transition across the hetero-interface. The intermixed ZnSe/Ga-terminated GaAs interface and faceted Ga-initialized GaAs/ZnSe interface could

unveil many new possibilities to eliminate interface states: ZnSe could dissolve in Ga, and introduce intermixed hetero-interface; thermal driven force could be in favor of the intermixing. And thus, both processes can possibly facilitate the formation of a graded interface. To verify the intermixing method and the influence of a compositionally graded interface on PL, we started the investigation on the annealed ZnSe/GaAs/ZnSe single QW by different methods.

Firstly, we fabricated LT-MEE GaAs QW sandwiched by ZnSe, with different GaAs thicknesses from 5 MLs to 100 MLs (Figure 3.4(a)). To study the effects of annealing, two types of annealing methods were used: in-situ annealing where the as-grown LT-MEE GaAs/ZnSe structure was annealed at 600°C for 3 min under As₂ overpressure to prevent the thin GaAs epi-layer from decomposing, top ZnSe layer was grown afterwards; ex-situ annealing which used an Annealsys As-One RTP to carry out rapid thermal annealing (RTA) on as-grown QW samples at 600°C for 3 min under inert N2 gas flow. After in-situ and/or ex-situ annealing, QW samples exhibited multiple strong, broad PL peaks never appeared in unannealed samples or pure ZnSe (Figure 3.3(b)). After the GaAs QW layer became too thick, the QW PL signal was significantly reduced, so we won't include them into the following studies. Samples having the same structure but with different annealing procedures (in-situ or ex-situ) showed peaks at similar wavelengths with different intensities, suggesting that the emission origins causing the observed PL peaks are consistent and robust over different annealing procedures. Besides, if the in-situ annealed sample was ex-situ annealed again, the PL spectrum didn't change significantly, except for slightly increased intensity. This could indicate that once the graded interface was formed, it won't be easily changed by thermal process again. To be noted, ex-situ annealing would lead to much stronger PL intensities than in-situ annealing. And the exsitu annealing seemed to improve the PL intensity of in-situ annealed sample also (see green and blue curves in Figure 3.4(b)). After ex-situ annealing, the QW sample showed intense luminescence to the excitation laser even under room light. The improvement of luminescence intensity can be seen directly by eyeballs (Figure 3.4(c)). The influences on PL intensity by RTA (Figure 3.4(b)) could be explained by two reasons. Firstly, it might be due to the rapid temperature ramp process during RTA. Secondly, for ex-situ annealed samples, the top ZnSe/MEE-GaAs interface was also annealed, which might give rise to the stronger emission by improving the interface quality. However, the detailed reasons are still unclear. Different annealing temperatures were also studied, as shown in Figure 3.4(c). But it only affected the intensity of PL responses. Degraded PL at higher temperatures could be attributed to crystal damage due to ZnSe decomposition, as the used temperatures were far above ZnSe decomposition temperature (400°C) [73].



Figure 3.4. (a) Stack structures for the QW samples, the red arrow indicates performing in-situ annealing after MEE GaAs layer was completed. RT-PL responses of selected samples to a 405 nm laser as-grown and after (b) different annealing procedures & (c) temperatures, samples in (b) & (c) have 15 MLs & 10 MLs of GaAs QW, respectively. The photos in (c) showed the PL response of corresponding samples (indicated by blue and red arrows) under room light.

In summary, both in-situ and ex-situ annealing (*i.e.*, RTA) could create totally different PL peaks compared to as-grown QW samples. The intensities of those peaks were strongly depended on the annealing

procedures. But the center wavelengths of PL peaks seemed to be independent of annealing procedures or temperatures, and only depend on the sample structure. Since the peak center wavelengths are more related to the luminescence mechanism, and they're not depending on annealing procedures. RTA (600°C, 3 min under N₂ flow) will be used as a standard annealing procedure in the following studies unless otherwise specified. Although the luminescence mechanism is not clear at this point, the resulted RT luminescence is extremely intense, as shown in the comparison between unannealed sample and annealed one in Figure 3.4(c). This showed great potential for applications as light emitting devices.

3.3 Characterizations of ZnSe/GaAs/ZnSe QWs

Having obtained strong luminescence from annealed ZnSe/GaAs/ZnSe QWs, we moved forward to carry out more characterizations on the QW samples in order to further understand this structure. As mentioned in Chapter 3.1, the thickness-dependent energy gap is one of the signatures of semiconductor QWs. Therefore, we firstly fabricated several QW samples with the similar structure as shown in Figure 3.4(a), but with different GaAs thicknesses. All samples were annealed using RTA with the same procedure stated above. Figure 3.5 shows partial PL spectra of different QW samples, as well as the peak center wavelengths fitted using Gaussian functions. The ZnSe band-edge peak was not included since it is not relevant here.



Figure 3.5. (a) Normalized RT-PL responses of QW samples with different GaAs thickness to a 405 nm laser, ZnSe peak not included and (b) extracted peak center wavelengths versus QW thickness by Gaussian fit of the PL spectrum.

As shown in Figure 3.5(a) and (b), the PL spectra of QW samples are broad, and Gaussian fitting results indicate that they contain multiple Gaussian peaks, typically three main peaks (see Figure 3.5(b)). Therefore, there should exist different emission mechanisms related to those peaks. However, there's not an obvious correlation between peak wavelength and QW thickness: the emission center wavelengths in all samples are scattered between 500 to 700 nm. This observation is totally different from previous studies. Zhang *et al.* used to fabricate ZnSe/GaAs/ZnSe QW by MBE with a GaAs thickness of 3, 4, and 6 nm [58]. They observed size-dependent PL shift from ~1.5 eV (~826 nm) to ~1.63 eV (~760 nm) at 9 K. Moreover, the PL peak became very broad when the QW thickness was reduced to 3 nm. But all three samples only showed a single QW-related emission peak. Besides, Funato *et al.* also measured the ZnSe/GaAs/ZnSe QW was increased. Besides, they believed that the cutoff wavelength at 22 K when the thickness of GaAs QW was increased. Besides, they believed that the cutoff wavelength also depends on the band offset between GaAs and ZnSe, as the band offset can be tuned by the growth procedures during metal-organic vapor phase epitaxy (MOVPE) [38, 74]. Nevertheless, all previous measurements were done at LTs. Some energy states will be inactive due to the LT measurement environments. That could be the reason why previous studies only observed separated emission peaks,

while the PL spectrum of our sample, which was measured at RT, showed broad, multiple peaks. In addition, there were various fabrication procedures in previous studies mentioned above, including solid phase epitaxy, MBE and MOVPE [58, 74]. Therefore, it is possible that we have observed a new mechanism or materials structure other than the conventional QW emission in previous studies.

To bring more insights, TEM was performed on selected annealed samples using the procedure described in Chapter 2.2. As seen from Figure 3.6(a) and (b), the GaAs QW region is not laterally continuous with a uniform thickness. The interfaces at both sides of QW region are not abrupt, but very rough instead. Besides, the diffraction patterns obtained respectively from bottom ZnSe layer, GaAs QW and top ZnSe layer have a similar single-crystal, zinc-blende diffraction pattern, which indicates good crystal quality and exclude the possibility of second phase formation. To examine the composition profile along the QW region, EDS analysis was performed at different positions across the interface (Figure 3.6(c) and (d)). As expected, the composition across the interfaces is graded from ZnSe to GaAs, then back to ZnSe again. The intermixed region contains all four elements, and both ZnSe and GaAs component appears to be stoichiometric. Importantly, the composition profiles of ZnSe-GaAs intermixed materials are not the same at different positions. As shown in Figure 3.6, position in (c) has a lower GaAs concentration than position in (d), which is consistent with the observation that the QW layer does not have a uniform thickness.



Figure 3.6. (a) Scanning-TEM image with atomic mass contrast and (b) high-resolution TEM image of QW sample cross-section after annealing (RTA). Diffraction patterns from ZnSe, and GaAs QW regions are shown in (b) at corresponding positions. (c) and (d) shows the scanning TEM image of the QW sample along the with the EDS line scan profiles acquired across different positions of the QW.

TEM and other structural analysis of several ZnSe-GaAs quantum structures including QWs, superlattice (SL) were also carried out by many previous researchers [36, 37, 73, 75]. Ramesh *et al.* used MEE to fabricate ZnSe-GaAs SLs at 250°C. They observed flat, coherent ZnSe-GaAs interfaces in the SL by X-ray Diffraction (XRD) and TEM, which was also confirmed by Kobayashi *et al.* using similar growth procedures [36, 37]. Funato *et al.* studied ZnSe-GaAs multiple-QW by MOVPE, and XRD along with TEM results showed that the ZnSe-GaAs interfaces were well-defined [75]. They also mentioned that the GaAs

QW layer as thin as 1 nm had a high degree of lateral uniformity [75]. The TEM of annealed ZnSe-GaAs SL has been performed by Zhang *et al.* [73]. They used a combination of solid phase epitaxy and MEE to fabricate ZnSe-GaAs SL and studied the annealing effects up to an annealing temperature of 520°C [73]. Strain relief inside the SLs after a 20 min annealing at 520°C was confirmed by XRD. Nevertheless, no significant intermixing was observed even after the annealing [73]. The non-uniform, intermixed interface present in our work has not been observed in previous research works.

In summary, the properties ZnSe-GaAs QW structure in this work from PL and TEM measurement are different from all previous studies in many ways. Firstly, we observed broad, intense PL at RT, and with no obvious correlation to QW thickness. Secondly, the QW region in our sample is not uniform laterally, and the interface is intermixed rather than well-defined. More importantly, the material in the QW region is not pure GaAs in this work. Those differences can be contributed to the fabrication procedure in this work, which was different from previous studies in many ways: the ZnSe compound source, the Gainitialized LT-MEE growth of GaAs on ZnSe, and the annealing procedures at very high temperatures compared to previous studies. Those fabrication procedures could lead to a material structure with new natures. The detailed discussion about the correlation between growth procedures and characterization results will be given in the next section.

3.4 Luminescence Mechanism of ZnSe/GaAs/ZnSe QWs

Characterization results on ZnSe/GaAs/ZnSe QWs in this work exhibited versatile new phenomena, as well as significant differences from previous studies on conventional QWs. Firstly, the QW samples have broad PL spectra and don't show strong correlation with their thickness. The origins of each different emission peaks in PL spectra need to be determined to fully understand and control the QW structure in this work. Besides, the QW region in this work lacks laterally uniformity. Since various compositions at different spots in the QW were observed, some growth mechanisms resulting in those non-uniformities

must exist in order to explain the observed phenomena. Correlation between fabrication procedures and grown materials needs to be established. Furthermore, understanding the nature of ZnSe-GaAs intermixed materials in the QW region is also important to explain the nature of the QW structure in this work. All three unclear questions stated above are crucial for understanding and further development of this ZnSe-GaAs materials system. However, there are very few available studies on this topic due to its complexity. In the following paragraphs, efforts made to explore and understand those three aspects will be described and discussed, respectively.

3.4.1 A Hybrid Epitaxy Model

The QW layer in this work has rough and compositionally graded interfaces at both sides, and it lacks any degree of laterally uniformity. As mentioned above, the compositionally graded interface was intentionally designed in this work, as abrupt interface was proved to be under-optimized. The original inspiration of this idea is from the TEM image of Ga-initialized MEE GaAs on ZnSe: faceted interface with (111)-oriented step surfaces was observed. A hybrid epitaxy model proposed by Chen *et al.* was used to explain this effect [69]. In their work, they found that during MBE growth of InAs on GaP substrate, the initial In layer could form a thin liquid phase, and resulting a liquid solution of In-Ga-P, since the solubility of InGaP in liquid In is higher than solid GaP phase [69]. Upon the following supersaturation brought by incoming As beam, the growth of a compositionally graded layer between the GaP substrate and the InAs was initialized [69]. They referred this vapor-liquid-solid (VLS)-like procedure as an MBE/liquid phase epitaxy (LPE) hybrid epitaxy.

Ga liquid phase could also be formed during MBE growth of GaAs in many scenarios [70, 76, 77]. The oval defect in MBE GaAs layer could facilitate Ga-droplets formation around the defect during GaAs growth [76]. And the Ga-droplets on MBE GaAs surface was found to be leading to following ZnSe hillocks formation by a VLS growth mechanism [77]. Moreover, Chikyow *et al.* deliberately deposited Ga-droplets layers by MBE on ZnSe surface to synthesize GaAs microstructures. Other researchers also used similar VLS method to grow GaAs nanowires on Si (111) surface by MBE [78]. Therefore, Ga-droplet formation

from MBE Ga source is commonly observed. Since Ga-initialized MEE was used to grow the GaAs QW in this work, initial Ga droplets could form on ZnSe surface and form a Ga-Zn-Se liquid solution. The sizes of Ga-droplets could vary from different positions on the surface, which could result in different amount of ZnSe being dissolved. Those liquid solutions in various size of Ga-droplets could act like "seeds" to initialize the upcoming hybrid epitaxy and annealing procedures. The composition of intermixed material is likely to be determined by the corresponding droplet size, which could also give rise to different emission wavelengths.

To verify this possibility of hybrid epitaxy model, a growth procedure based on the previous QW structure was designed. As shown in Figure 3.7(a), pure Ga layers were deliberately deposited on as-grown ZnSe/GaAs at 300°C to facilitate the Ga-droplets formation. The beam flux of Ga was fixed as 1 ML/s (measured during GaAs growth). The as-formed Ga-droplet layer was then annealed under As over pressure at 600°C for 3 min, followed by top ZnSe growth at 300°C. As shown in Figure 3.7(c), the growth surface became rough without reconstruction after a few MLs of Ga layer deposition, indicated by RHEED pattern. This was probably caused by the Ga droplets formed at various position on the ZnSe surface, which dissolved some of the surface ZnSe layer and disturbed the previous surface reconstruction. But it will regain steaky, single crystal pattern after the As annealing started (Figure 3.7(c)). We believe similar process as Chen et al. proposed happened at this stage: the As beam flux caused supersaturation and crystal growth at the solid-liquid interface [69]. As shown in Figure 3.6(b), the intermixed ZnSe-GaAs layer was determined to be single crystal with high quality from the electron diffraction pattern. It is likely that the crystal grown from Ga-Zn-Se liquid solution under As pressure was a single crystal ZnSe-GaAs mixture. The intense RHEED pattern could also confirm the single crystalline nature of the mixture material. Besides, the RHEED pattern was streaky during the mixture growth, while the Ga/ZnSe surface was rough. Previous researchers showed that a rough MBE GaAs surface could become smooth after high temperature annealing under As beam flux [51]. It is reasonable that similar self-flattening mechanism might also exist during As annealing in this work.

After growth, all samples showed similar PL spectra as the QW samples with multiple peaks (Figure 3.7(b)), indicating similar structure was formed during this growth. Thicker Ga layer (45 MLs) was studied to improve the coverage and uniformity of initial Ga-droplets layer, but the corresponding PL spectrum didn't show much difference with the other samples (Figure 3.7(b)). Figure 3.7(d) demonstrates the detailed procedures of the proposed hybrid epitaxy model: initial Ga deposition formed Ga droplets with different sizes on ZnSe surface and created Ga-Zn-Se liquid solutions with different amount of ZnSe dissolved. The upcoming incident As beam flux and elevated temperature broke the liquid-solid phase equilibrium between solution and solid ZnSe, and caused the growth of the ZnSe-GaAs intermixed material at the solid-liquid interface. Although the growth surface after Ga layers deposition was rough and amorphous, annealing under As will "heal" the growth surface. Similar phenomenon was also observed in MEE GaAs growth [51], where researchers found rough GaAs surface will become atomic flat again after annealing under As overpressure at appropriate temperature. At high temperature, the adatoms (*i.e.*, Ga) could migrate on the surface, which would flatten the surface.



Figure 3.7. (a) Stack structures for the samples to verify the hybrid epitaxy model, the red arrow indicates perform in-situ annealing after the Ga droplet layer was completed and (b) RT-PL responses of selected as-grown samples to a 405 nm laser, ZnSe peak was not included. (c) shows the RHEED pattern after Ga layer deposition and after As annealing. (d) shows the proposed model to explain the hybrid epitaxy procedure and origin of multiple emission centers.

The hybrid epitaxy model could also be used to explain the growth mechanism of previous QW samples: since the GaAs QW layer was grown by Ga-initialized MEE, Ga and As beam flux was supplied to the ZnSe surface alternatively. Therefore, similar procedure in the first two steps of the hybrid epitaxy model could happen multiple times, and resulting in the formation of intermixed material in QW. The following annealing procedure could further facilitate the intermixing and change the whole QW region to be intermixed. Besides, when the QW was too thick, the annealing procedure might not be adequate for the whole layer to be intermixed. And that could probably explain the reason why the QW PL signal was significantly reduced after certain thickness.

In summary, a hybrid epitaxy model of MBE and LPE was proposed to explain the growth procedure of ZnSe/GaAs/ZnSe QW in this work. The model is consistent with current experiments. However, more evidence will be needed to verify the assumption.

3.4.2 The Origins of Different Emission Peaks

As described in Chapter 3.3, the QW samples have broad PL spectra and don't show strong correlation with thickness. Since the fabrication procedure in this work was very complicated, and ZnSe as a wide band-gap semiconductor has many possible deep-level states by itself [67, 79-81]. Those defect peaks with center wavelength from 500 - 800 nm observed in previous studies were summarized in Table 3.1.

Table 3.1. Summary of known deep-level emissions in MBE ZnSe epi-layer from literatures. Some of the peaks are present in this study while the others are not, but presented peaks might be not reasonable for this study given our fabrication procedures/environment (described in the main text).

Peak wavelength	Origin	Reasonable for this work
560 nm	As substitutional [79]	Yes
750 nm	As substitutional [79]	Yes
630 nm	Zn vacancy-donor complex [80]	Yes
550 nm	Donor-alkaline impurity complex [80]	No
780 nm	N-H pair [81]	No

As shown in Table 3.1, there are many known defect-related emission peaks in ZnSe. Some of them seem to be reasonable to exist in this work, such as the As substitutional defects and Zn-vacancy, since the growth environment of ZnSe in this work contains As species. And Zn-vacancy in crystal is almost

unavoidable to form. However, other defects are unlikely to be in the ZnSe for this work. The donor-alkaline pair is from source of alkaline atoms sometimes used as a dopant for ZnSe, and the N-H pair is typically due to the growth environment of MOVPE, which contains a high level of hydrogen. However, those peaks, due to their recombination mechanisms, are typically sensitive to temperature. In fact, all defect peaks mentioned above were observed at least below liquid nitrogen temperature (90 K). And many of them have close center wavelengths to each other and/or to the QW-related peaks in this study. Therefore, sophisticated characterization techniques are required to isolate and identify those peaks, which will be very challenging and may not be effective. Under this regard, spatial information about the emission centers might be helpful.

In order to acquire spatial information of the emissions from QW sample by PL, QW samples with different top ZnSe layer thicknesses were fabricated (Figure 3.8(a)). All samples were annealed by RTA with sample upside down to minimize decomposition of the top ZnSe layer during annealing. As shown in Figure 3.8(b), the samples with different top ZnSe layer thicknesses exhibit different PL responses to the same laser source, even though they have the same GaAs QW thickness. This difference could reflect the depth-resolved PL emission of QW sample in some ways: since the ZnSe layer will absorb the 405 nm laser with an absorption coefficient of $\sim 10^5$ cm⁻¹ [82], the laser could only reach a certain depth into the sample before attenuated to a neglectable energy. The absorption percentage of top ZnSe layer with different thicknesses are given in Figure 3.8(c). To be noted, the top ZnSe layer would decompose during the RTA. Therefore, the real thickness of the top ZnSe layer when the PL measurements were taken should be smaller than nominal thickness. Especially for the sample with only 20 nm top ZnSe, the top layer should be neglectable after RTA. From previous TEM results, there are two region having intermixed ZnSe-GaAs: the QW region, and the bottom ZnSe/GaAs interface. Therefore, the PL measured from sample with 20 and 50 nm ZnSe is mainly coming from the bottom ZnSe and ZnSe/GaAs interface, while the PL from the sample with 500 nm ZnSe is mainly from the top layer and QW region. As for the sample with 150 nm ZnSe, it can be treated as the combination of both situations stated above.



Figure 3.8. (a) Stack structures of the QW samples with different top ZnSe thicknesses. All samples were annealed by RTA at 600°C for 3 min. (b) RT-PL responses of those samples with different top ZnSe layer to a 405 nm laser, (c) shows the absorptions of top ZnSe with different thicknesses to the 405 nm laser.

This assumption about the depth-resolved emission could also be confirmed from the difference in ZnSe band-edge emission: the samples with thin top ZnSe layers have very weak band-edge PL emission, while the samples with thicker ZnSe have much stronger band-edge PL emission. For samples with 20 or 50 nm top ZnSe, the top layer, which was partially/totally decomposed, cannot give strong band-edge emission. But the bottom ZnSe are sandwiched by low band-gap GaAs layers. The band bending from wide band-gap ZnSe towards low band-gap GaAs will drift the majority of excited carriers away from ZnSe. As a result, the ZnSe band-edge PL emission will be significantly reduced. Therefore, it is reasonable that the sample with only 20 or 50 nm top ZnSe layer don't have strong ZnSe band-edge emission after RTA. As the ZnSe thickness increases from 150 nm to 500 nm, more laser energy will be consumed in the top ZnSe layer, and thus stronger ZnSe band-edge PL emission can be observed as the top ZnSe layer thickness increases.

After knowing about the depth profile of PL emission origins, it is clear that the bottom ZnSe/GaAs intermixed material and/or the bottom ZnSe is responsible for a single, broad PL peak centered at ~600 nm, as seen from the red and blue curves in Figure 3.8(b). When the top ZnSe layer thickness is increased to 150 nm, intermixed material in QW region start to contribute to the PL spectrum (green curve in Figure 3.8(b)). Except for the peak centered at ~600 nm, another peak shoulder at ~560 nm appears in the PL spectrum, and the 600 nm peak width is reduced, suggesting that the intermixed ZnSe-GaAs in the QW region is different from the bottom side in terms of PL emission. When the top ZnSe layer thickness further increases to 500 nm, the PL will be mainly from the top layer and QW region. PL spectrum features observed in 150 nm top ZnSe sample (~560 nm shoulder and ~600 nm narrower peak) still remain but with lower intensities due to more laser absorption in the top ZnSe layer. However, another shoulder centered at ~700 nm appears, which might be originated from top ZnSe layer itself due to some defect levels.

To further strengthen the discussion above, a more direct experiment trying to locate the depthresolved emission centers was carried out. One of the annealed QW samples in Figure 3.8(a) with 150 nm top ZnSe layer was etched in an etchant of HCl:H₂O₂:H₂O = 1:1:2 [32] to remove the top ZnSe layer as well as the QW layer (Figure 3.9(a)). The etch depth was measured by a Bruker Dektak XT to be ~350 nm. The PL spectra before and after the QW removal are shown in Figure 3.9(c). After QW removal, the sample exhibited similar PL spectrum as the samples in Figure 3.8(b) with thin (20 or 50 nm) top ZnSe layer thickness. This result could further validate our previous assumption on the depth-resolved PL emission experiment: the bottom side ZnSe/GaAs structure after annealing will give rise to a broad, single PL peak centered at ~600 nm, while the QW region and/or top ZnSe layer is responsible for other PL peaks centered at different emission wavelengths.



Figure 3.9. (a) Stack structures of the etched QW sample and (b) RT-PL responses of the samples before/after the QW removal to a 405 nm laser.

From the PL point of view, the only difference between the sample after QW removal (blue curve in Figure 3.9(b)) and the QW sample with thin top ZnSe layer (red curve in Figure 3.8(b)) is the intensity of ZnSe band-edge emission. As discussed above, the reduced ZnSe band-edge emission in the QW sample with thin top ZnSe layer is attributed to the band bending towards low-band-gap surface GaAs layer (Figure 3.8). But for the QW removed sample, the surface GaAs layer is absent. Therefore, it still exhibits strong ZnSe band-edge emission (Figure 3.9). Under this regard, the bottom ZnSe layer in the QW sample with thin top ZnSe layer (Figure 3.8) does not make significant contribution to the PL spectrum, since it does not have strong ZnSe band-edge emission due to band bending. Therefore, we can exclude the possibility that the 600 nm broad peak should be correlated to the bottom ZnSe layer itself. Instead, the intermixed ZnSe-GaAs material at the bottom ZnSe/GaAs interface is the origin of the 600 nm broad peak, and the intermixed ZnSe-GaAs material in the QW region is probably responsible for other peaks centered at from 500 to 800 nm.

In order to further investigate whether intermixed ZnSe-GaAs is the origin of complicated PL emission peaks, another set of samples were fabricated. As shown in Figure 3.10(a), the samples have the

similar structure as the QW samples, but the previous MEE-GaAs layer is replaced by an intermixed ZnSe-GaAs layer. The layer was grown by controlling the beam flux ratio of ZnSe compound source to GaAs, and the GaAs component was kept at Ga beam: As_2 beam = 1:1 to get stoichiometric GaAs at low growth temperature. All Ga, As and ZnSe shutter were deliberately opened simultaneously during the intermixed layer growth. The growth rate was treated as a simple summation of the separate ZnSe and GaAs growth rates. Single crystalline, spotty RHEED pattern was observed during the intermixed layer growth, but it turned to amorphous after ~20 MLs. Therefore, the intermixed layer in all samples were set to be 10 MLs. After growth, the samples were annealed by the same RTA procedure (600°C, 3 min). The PL responses to a 405 nm laser before and after RTA were taken as Figure 3.10(b) and (c).



Figure 3.10. (a) Stack structures of the intermixed ZnSe-GaAs samples, x:y was increased from 3:7, 1:1, 2:1 to 9:1, and RT-PL responses of the samples (b) before and (c) after RTA to a 405 nm laser. The intensity scale in (c) is 6 times as big as in (b).

As shown in Figure 3.10(b), surprisingly, the as-grown samples with an intermixed ZnSe-GaAs layer exhibit strong PL signal as well as the ZnSe band-edge emission. For the precious as-grown QW samples with a pure GaAs QW layer, the PL spectrum was dominant by ZnSe band-edge emission (see Figure 3.2(b)). Only after the interface intermixing by annealing, the plain QW samples can show PL spectrum with longer wavelength peaks like Figure 3.10(b). This could add another evidence that the broad PL peaks from 500 – 800 nm are originated from the intermixed ZnSe-GaAs. Interestingly, the ZnSe band-edge PL emission intensity monotonically increases with the ZnSe concentration in intermixed layer as seen in Figure 3.10(b), while the overall intensity of longer wavelength peaks decreases with the ZnSe concentration. The reason behind this phenomenon is still unclear to us. It is possible that as the ZnSe concentration in the intermixed layer increases, the whole sample becomes more like pure ZnSe, but with a "dirty" layer containing Ga and As inserted. In addition, the GaAs component in the intermixed material seems to be responsible for the longer wavelength peaks, as their overall intensity increases with GaAs concentration. However, more investigations are needed to further understand this material.

As shown in Figure 3.10(c), the samples have much stronger PL emission from 500 – 800 nm after RTA (intensity scale in Figure 3.10(c) is six times big as (b)), and reduced ZnSe band-edge emission. The shapes of each PL spectrum did not change significantly after RTA. From previous results in this Chapter, RTA could facilitate the intermixing between ZnSe and GaAs. Since the samples were grown at relatively low temperature, the adatoms on the substrate didn't have enough energy to migrate to their lowest-energy positions. For example, the As background pressure at low temperatures will hinder the migration of Ga adatoms on the substrate during GaAs growth, resulting in point defects like vacancies, anti-site atoms or interstitial atoms [51]. It is likely that the intermixed layer also contained a high concentration of defects, and was not intermixed thoroughly due to the poor adatoms migration at low growth temperature. During annealing, the thermal energy might help the crystal to release some of the defects, and thus a boost of PL intensity was observed (Figure 3.10(c)). However, more detailed investigations are needed to further understand this intermixed material.

3.4.3 The Nature of Intermixed ZnSe-GaAs

Experiments designed previously in this Chapter revealed that ZnSe-GaAs intermixed material is likely to be the origin of novel, intense PL emission observed in this work. However, the nature of intermixed ZnSe-GaAs is extremely complicated and lacks available research. Although ZnSe and GaAs have similar lattice constants, they also have different chemical potentials, bond charges, and bond strengths. Besides, they could cross-dope each other. For example, Ga could dope ZnSe to be n-type, and Zn could dope GaAs to be p-type. The ZnSe-GaAs intermixed material, as seen in the QW region of ZnSe/GaAs/ZnSe QW samples, is obviously not like other III-V or II-VI alloys (AlGaAs or ZnSeTe). The intermixed ZnSe-GaAs could be pseudo-binary alloy obeying Vegard's law, or nonisovalent alloy, which can be viewed as the doping of a host semiconductor with a lower (higher) valent cation and a higher (lower) valent anion, or other complex intermixed materials [71, 83, 84]. Therefore, multiple theory models could be used to describe the intermixed ZnSe-GaAs system.

There are very few available studies on intermixed ZnSe-GaAs as it is an extremely complicated system. Yim *et al.* and Ku *et al.* have studied the solid solution of ZnSe and GaAs, and treated it as a pseudobinary system [71, 84]. Both groups of researchers had success in synthesizing ZnSe-GaAs solid solution crystals by different methods, and proved that ZnSe and GaAs are miscible throughout the entire composition [71, 84]. Besides, both groups have measured a sublinear dependence of lattice constants and band-gaps on the composition of solid solutions [71, 84]. From Figure 3.6, there are no obvious divergence between Zn and Se (also Ga and As) in the intermixed material of the QW region in this work. Therefore, it is possible that the ZnSe and GaAs formed pseudo-binary alloys inside the QW region by annealing. Furthermore, Figure 3.6 suggests different composition of intermixed ZnSe-GaAs at different spots. If the intermixed ZnSe-GaAs is pseudo-binary alloy, whose band-gap depends on the composition, it is reasonable that the broad PL spectrum of QW samples with multiple peaks is due to alloy composition variance inside the samples. However, it appears that varying the supplement amount of GaAs by changing GaAs QW thickness cannot directly control the composition of formed alloy very well, since the PL peaks don't have a strong dependance on the QW thickness. Further proof is still needed to make the conclusion that the intermixed ZnSe-GaAs is a pseudo-binary alloy.

Another possible model to describe the intermixed ZnSe-GaAs is by treating it as a dilute nonisovalent alloy [83]. Conventional III-V or II-VI compound alloys like AlGaAs or ZnSeTe are isovalent. Basically, they are electrically neutral, and don't have any new energy levels inside the band-gap by themselves. In contrast, the simultaneous introduction of low-valent and high-valent elements (e. g. Zn or Se in III-V) into those compounds will result in formation of nonisovalent alloys, such as the (III-V)_x(II-VI)_{1-x} alloys. The intermixed ZnSe-GaAs in this work could be one of them. The dilute nonisovalent alloy could be viewed as the doping of a host semiconductor with a lower (higher) valent cation and a higher (lower) valent anion [83]. For intermixed ZnSe-GaAs, we can first assume ZnSe is the host crystal consisting of Zn-centered and Se-centered tetrahedra. As shown in Figure 3.11, the Ga and As atoms can replace one or more atoms in each tetrahedra, leading to reformed tetrahedra in terms of Zn-(Se_nAs_{4-n}) and Se-(Zn_nGa_{4-n}). Since the system is nonisovalent, the reformed tetrahedra will have different charges, and thus generate new energy levels in the alloy. Wang *et al.* studied multiple possible types of tetrahedra using *ab initio* pseudopotential plane-wave calculations [83]. They found that different types of tetrahedron have different formation energies, and thus some kinds of tetrahedra are more stable than the others. Importantly, the impurities (e. g. Ga or As in ZnSe) form stable but charge neutral pairs in the nonisovalent alloy, and there's an asymmetry between anion and cation incorporation energies. Therefore, the nonisovalent alloy exhibit a single type of conducting (n- or p-type) with high mobilities. The specific conducting type depends on the alloy growth conditions (e. g. As-rich or Se-rich) [83]. Moreover, they also predicted a dependency of alloy band-gap on composition.



Figure 3.11. An illustration of the process where Ga and As atoms replace atoms in ZnSe host crystal, and forms new tetrahedra with different charges in the ZnSe-GaAs nonisovalent alloy.

If the intermixed ZnSe-GaAs in the QW region in this work follows the nonisovalent model, it can be treated as alloy clusters with different compositions along the QW region. They will exhibit a single conducting type, since the formation environmental conditions were similar for all of them, and have different band-gaps determined by their compositions. This theory is consistent with observed PL emissions, where the samples exhibited strong and broad PL spectra. However, the model does not give many inspirations in terms of composition (*i.e.*, band-gap) control. And there's no easy way to verify the theoretical calculation results by the model.

In summary, the intermixed ZnSe-GaAs material is highly likely to be responsible for the novel PL emission observed in this work. However, the intermixed material is an extremely complicated system and lack of relevant studies. Several models were employed trying to describe the complicated system, including pseudo-binary alloy and nonisovalent alloy. The models are both consistent with experiment

results from previous studies and this work in many ways. However, they cannot be simply verified. Furthermore, no models could provide instructions on how to control the emission wavelength of the intermixed ZnSe-GaAs in this work. Further investigations from both experimental and theoretical perspectives are needed for this material system.

3.5 Potential Applications of ZnSe/GaAs/ZnSe QWs

As discussed in this Chapter previously, novel, intense PL emissions have been observed from annealed ZnSe/GaAs/ZnSe QW samples. Even though the luminescence mechanism is not totally clear so far. The attractive PL performance suggests that the QW structure has great potentials for applications as light emitting devices. Detailed discussion from device application perspective will be given in this section.

ZnSe has been once extensively researched since 1980s as many photonic devices including bluegreen laser diode and LED [3, 23-26]. ZnSe-based laser diodes and LEDs were successfully realized a long time ago [23-25]. However, the lifetime of ZnSe-based devices was proved to be a problem due to materials degradation during device operation under high optical power [26, 30, 31]. Furthermore, the p-type dopant was recognized as one of the main failure mechanisms for degradation [30, 31]. The degradation process is believed to be associated with vacancy generation under high optical power. If photons with energies bigger than a threshold are absorbed by the crystal, shallow p-type acceptors could be excited to the conduction band and generate vacancies accordingly [30, 31]. As a result, a high concentration of vacancy will lead to degradation and even failure of ZnSe-based devices.

For successful application as a commercial product, lifetime is one of the major figures of merits. Since ZnSe has a negative history reputation in terms of lifetime, our QW structure, which is based on intermixed ZnSe-GaAs and n-type ZnSe, is also possible to have a similar issue. To exclude that possibility, an aging test to high optical power was performed on the QW samples from this work. Basically, one of the annealed QW samples was put into the PL measurement apparatus. A 405 nm continuous-wave (CW) laser with a power of ~25 mW was used to continuously pump the QW sample for ~30 hours. The PL response spectra were taken regularly during that time period. As shown in Figure 3.12, the overall PL intensity of the QW sample generally stays the same as the initial PL intensity, with some minor variations. The variation of PL intensity during measurement could be introduced by environmental disturbance during the long-time measurement. The purpose of this aging test is to mimic the photonic device operation scenario under high optical power densities, as it is known to cause degradation in p-type ZnSe [31]. Clearly, the QW sample doesn't show degradation in terms of PL intensity. PL intensity is sensitive to the quality of crystal defects, since defect like vacancies will introduce non-radiative recombination centers and thus reduce the radiative recombination efficiency. If a high concentration of vacancy is generated by the long-time operation under high optical power, the PL response intensity to the same pump source (the 405 nm laser) would significantly drop. Therefore, the stable PL intensity over time could exclude the possibility that intermixed ZnSe-GaAs has similar degradation mechanism like p-type ZnSe.


Figure 3.12. Overall RT-PL intensity of a QW sample over time under continuous excitation by a 405 nm CW laser (power: ~25 mW). Initial PL intensity at the beginning of measurements is indicated by the blue dash line.

Since the QW samples do not degrade under optical power as p-type ZnSe, it can lead to a bright future to be used as high-brightness, high-efficiency light emitting devices. Recently, there are emerging interests on the optically pumped light sources for applications such as display and laser, demanding high quantum efficiency materials [85-89]. Since it is difficult to realize full-colored LED with a single material system, and also challenging to integrating different colored LED in a single panel, the optically pumped light source could be an alternative way. This passive lighting technology utilizes commercially available efficient blue laser diode or LED based on GaN to pump other phosphor-like medium with high conversion efficiencies to realize full-color applications [85-89]. This method could simplify the fabrication procedure for full-colored light emitting devices, as well as keep a tolerable efficiency by using efficient light source and medium. Since the QW samples exhibit strong PL responses to the blue laser source, it is very suitable to be used as the conversion medium in the optically pumped light source system. Moreover, as smartphone penetration saturates, there is an emerging trend in personal mobile devices: wearable mobile devices [90, 91]. Wearables come in many different forms and flavors, targeting different accessories, and clothing that people wear [90]. They will not only provide a more convenient and versatile human-computer interface, but also could improve quality of human life in many ways, such as continuously sensing, collecting, and monitoring various health conditions data [90, 91]. For all those applications, electronic and photon devices with bendable thicknesses, or soft devices, are demanding [90-92].

To study the potential of QW samples as soft photonics, an epitaxial lift-off procedure was carried out on the QW samples. To fabricate a QW membrane with a thickness less than 1 μ m, a 100 nm AlAs epitaxial lift-off layer was inserted under bottom ZnSe layer in the QW structures in Figure 3.2(a). The asgrown samples were annealed by the same RTA procedure. Then, the samples were cleaved into ~0.5 cm × 0.5 cm squares, and the front side of the samples was glued to a transparent supporting substrate by black wax. An etchant of HF:H₂O = 1:3 was used to selectively remove the AlAs epitaxial lift-off layer. The samples were soaked the in the etchant overnight to lift-off the QW layers.

The QW flakes glued to a supporting substrate after lift-off are shown in Figure 3.13(a). Even though the total thickness of the flake is less than 500 nm (Figure 3.2(a)), as seen in the photo, the QW flake has a smooth surface with clean edges following the shape of the black wax glue. It also exhibits intense PL response to the blue laser (see Figure 3.13(b)). From Figure 3.13(c), the PL spectrum of QW flake doesn't show big difference compared to the bulk sample. There's a slight redshift of the QW flake PL spectrum. Since the thicknesses of top and bottom ZnSe layers are different in the QW structure (Figure 3.2(a)), the small redshift could be due to this asymmetry, as the pumped laser was shining on the different sides of the flakes. More importantly, the < 500 nm thick QW flakes have similar overall PL intensity as the bulk sample, suggesting that the lift-off procedure will not bring any damage on the optical performance of the QW samples. Furthermore, as shown in Figure 3.13(d) and (e), the QW flakes are smooth and intact over a big area. Only very few mechanical defects could be observed on the flakes even at the flake edge

region, which indicates that the lift-off procedure didn't bring significant mechanical damage to the flakes either. The seminal result shows that the QW samples could be easily fabricated into soft photonic devices without damages optically or mechanically.



Figure 3.13. Photos of QW flakes after epitaxial lift-off under (a) room light and (b) a 405 nm excitation laser. (c) shows the RT-PL responses of the bulk sample (front side) and after lift-off (bottom side) to a 405 nm laser. Nomarski optical micrograph of the QW flakes on (d) center region as well as (e) edge region.

In summary, an aging test to high laser power density was performed on the QW samples. The QW sample exhibited stable optical performance over long-time operation under high optical power, unlike the degradation behavior in p-ZnSe. Besides, epitaxial lift-off was performed on the QW samples and QW flakes with a thickness less than 500 nm was successfully fabricated. The QW flakes have similar PL emission intensity as the bulk samples, and have mechanically high-quality over a big area. The preliminary

results suggest that the QW samples could find many applications as photonic devices, including the emerging passive lighting technology and wearable devices.

3.6 Summary

Fabrication method established in Chapter 2 was used to study ZnSe/GaAs/ZnSe QW structures for potential light emitting devices. As-grown QWs with abrupt interfaces cannot produce satisfactory PL performance due to under-optimized interface quality. Ga-initialized MEE GaAs and high temperature annealing is found to be able to facilitate interface intermixing significantly, and generate compositionally graded ZnSe-GaAs interface. The annealed QW structures exhibits intense, broad PL emission with multiple peaks from 500 to 800 nm at RT, which does not show strong correlation with QW thickness. TEM results reveal that the annealed QW structure has an intermixed ZnSe-GaAs material in the QW region with all four elements, as well as compositionally graded interfaces at both sides. New PL emission phenomenon other than conventional QW with eigenstate emission is believed to exist in this work.

Detailed investigations utilizing available experimental setup and previous studies have been conducted to understand the luminescence mechanism in the versatile PL emissions from annealed QW structures. Evidence suggests that intermixed ZnSe-GaAs is responsible for the broad PL emission from 500 to 800 nm. Different theory models and experimental efforts have been applied to understand the nature of the intermixed material. The intermixed ZnSe-GaAs system could be treated as a pseudo-binary alloy, or a nonisovalent alloy, but further investigations are still needed to draw a convincible conclusion. Seminal results on the QW aging test and QW membrane fabrication show that the annealed QW structure in this work has great potential to be used as stable, efficient light emitting devices including in the passive lighting technology and soft photonic devices.

4 Ohmic Contacts to ZnSe-based Devices

4.1 Introduction

Ohmic contact is an essential component for all semiconductor devices. We firstly review the basic physics of metal-semiconductor contacts in order to understand the parameters that determine optimal performance and use them to guide the device design and growth procedures. In order to receive input or generate output electrical signals, semiconductor devices need to be integrated in metal interconnects through metal-semiconductor contacts. There are two kinds of metal-semiconductor contacts: Schottky contact, and ohmic contact. In this analysis, we will firstly assume an ideal metal-semiconductor contact following the Schottky model [93] with a metal work function (Φ_M), and an electron affinity (χ_{SC}) of a n-type semiconductor. The difference in metal work-function and semiconductor electron affinity gives rise to a fermi level imbalance at the metal-semiconductor interface. To return to equilibrium, carriers will diffuse across the interface to re-balance the fermi level of each side until an equilibrium is reached. If the Φ_M is greater than χ_{SC} , electrons at semiconductor side will have higher energy and thus will flow to the metal side, which gives rise to an energy barrier called Schottky barrier (Φ_B) [93]:

$$\Phi_B = \Phi_M - \chi_{SC}$$

This situation is illustrated in Figure 4.1(a): after the Schottky contact formation, electrons at both sides will encounter a barrier before flowing to the other side. Therefore, a Schottky contact will exhibit a diodelike non-linear current-voltage characteristics. On the other hand, if the Φ_M is smaller than χ_{SC} , electrons at semiconductor side will have lower energy than metal side. In this case, an ohmic contact will form at the metal-semiconductor interface, and carriers will go through no barrier when they're flowing across the interface (Figure 4.2(b)). Therefore, an ohmic contact will have a resistor-like linear current-voltage characteristics, obeying Ohm's law. Ohmic contact is typically wanted to connect semiconductor devices to metal interconnections.

While this ideal Schottky model can be used as an initial rough estimate for the property of a metalsemiconductor contact, real interface usually includes nonidealities like interfacial oxides, non-perfectly abrupt interfaces, and other interfacial reactions that would dramatically affect the barrier height [94, 95]. If a high density of interface state is introduced, the fermi level at the semiconductor surface will be "pinned" at certain position to maintain the charge neutrality [94, 95]. As a result, the $\Phi_{\rm B}$ at the metal-semiconductor interface will be solely determined by the fermi level pinning position regardless of metal work-function (Figure 4.1(c)) [94-96]. The case where the Schottky barrier height is almost completely insensitive to the metal's work-function can be described by Bardeen model [96]. Therefore, in practice, it is usually not possible, and not necessary to fabricate ohmic contacts like Figure 4.1(b) which has perfectly linear currentvoltage characteristics. It is generally required that ohmic contacts must be able to supply the device current, and have a smaller voltage drop across the contact compared to across the active device regions. And it should not inject minority carriers [97]. In practice, a heavily doped surface layer in semiconductor is commonly used to facilitate ohmic contacts. As shown in Figure 4.1(d), heavily doped n^+ layer at the semiconductor side has very narrow space-charge region width. For metal-semiconductor contacts with a very narrow space-charge region, electrons can tunnel from the metal to the semiconductor and from the semiconductor to the metal through field emission [97]. Therefore, although the Schottky barrier at metalsemiconductor interface still exists due to fermi level pinning, electrons can tunnel through it easily under a small bias voltage. The Schottky contact will become very leaky electrically and has a quasi-linear current-voltage characteristic. Practically, this is good enough to be treated as an ohmic contact.



Figure 4.1. Energy band diagram of different types of metal-semiconductor contacts including (a) Schottky contact, (b) ohmic contact and (c) metal-semiconductor contact where fermi level pinning occurs. The barrier height Φ'_{B} in (c) is solely determined by the fermi level pinning position regardless of metal work-function. (d) Metal-n⁺-n semiconductor contact with fermi level pinning and a very heavily doped n⁺ surface layer.

Ohmic contacts have been a challenge for many wide-gap II-VI compound semiconductors due to their poor thermal stability, including ZnSe [32, 98]. Many researchers have been working on methods to fabricate low-resistance ohmic contacts to ZnSe. Complicated graded structures like ZnS_xSe_{1-x} or ZnSe_xTe_{1-x} were employed to facilitate ohmic contact formation [32, 99]. Previous studies have also found many metal combinations like titanium (Ti)/platinum (Pt)/gold (Au), magnesium (Mg)/copper (Cu), indium (In)/Au could form ohmic contacts to n-ZnSe [99, 100]. However, most of them require a very high doping concentration of ZnSe and many additional treatments, such as plasma treatment or annealing, and suffer from high contact resistances [99, 100]. In has also been used as an ohmic contact, but this contact has high resistivity and low reliability due to In's low melting point and poor wetting [101]. Very recently,

researchers also realized local ohmic contacts to a buried n-ZnSe layer through selective regrowth of heavily doped ZnSe layer, then deposited low work function metals such as aluminum (Al), Mg and Ti [102]. However, for all high-performance device applications, low-resistance ohmic contacts with simplified fabrication procedures are still demanding. In this Chapter, we will explore several low-resistance ohmic contacts to ZnSe.

4.2 Methods for Contact Resistance Measurement

As the integration level of circuits dramatically increasing in past decades, power dissipation and heat management becomes an increasingly important issue. Heat generated by the semiconductor devices is proportional to the square of resistance value. The metal-semiconductor contacts, which is a necessary component for all devices, are basically resistors in circuits point of view. Therefore, among many parameters, contact resistance is one of the most important parameters for an ohmic contact.

Contact resistance is a less clearly defined concept used to describe the resistance right at, and related to metal-semiconductor contact interface. It contains the resistance of the metal-semiconductor interface, and also includes a portion of the metal immediately above, a part of the semiconductor below, and any interfacial oxide or other layer that may be present [97]. If the ohmic contact has a measured current density J at an applied bias voltage V, the specific contact resistance ρ_c can be written as

$$\rho_c = \frac{dV}{dJ}|_{A \to 0}$$

where A is the area of the contact [97]. The term is very useful since it is independent of contact area when comparing contacts of various sizes.

To measure the contact resistance, consider a simplified diagram in Figure 4.2 first. The total resistance R_T between the two terminals is

$$R_T = 2R_M + 2R_C + R_S$$

with a metal resistance R_M , semiconductor resistance R_S , and contact resistance R_C . Among these, the metal resistance R_M is typically ignored since the metal resistance is very small compared to the others. Semiconductor resistance R_S is proportional to the distance d between two contacts (assuming the semiconductor layer is homogenous). Therefore, if several total resistances R_T between two ohmic contacts with different distance d could be measured, one could extract the contact resistance value R_C from the intercept of R_T - d plot.



Figure 4.2. A schematic diagram showing two ohmic contacts to a semiconductor layer, with the metal resistance, the contact resistances and the semiconductor resistance indicated.

Using the idea above, ohmic contact patterns like shown in Figure 4.3 are commonly used to measure the specific contact resistance. Basically, they are repeating patterns with different distances between each other in order to extract the contact resistance. However, practically, current crowding effect

occurs at the metal-semiconductor interface. To take the current crowding into consideration, a detailed theoretical investigation based on the transmission line model (TLM) considering both the semiconductor sheet resistance R_{sh} and specific contact resistance ρ_C is used [97]. R_M is typically ignored since it is a small value.



Figure 4.3. Test patterns to measure specific contact resistance: (a) rectangular pattern with same the height and width (w and z), but different distances d; (b) circular pattern with same inner radii, but different spacing d between inner and outer circle contacts.

Besides, the geometry of the patterns plays an important role also. For the rectangular contacts in Figure 4.3(a), the current flow at the contact edge can significantly affect the results of contact resistance measurement. This can be totally avoided by using the circular pattern, which is symmetric in all directions [103]. For the circular pattern in Figure 4.3(b), if the sheet resistances under the metal and in the spacing

gap are equal, and the inner radii is much bigger than the spacing ($r_0 >> d$), the total resistance between the inner and the outer contacts is [97]

$$R_T = \frac{R_{sh}}{2\pi r_0} (d + 2L_T)C$$

where C is the correction factor

$$C = \frac{r_0}{d} \ln(1 + \frac{d}{r_o})$$

and L_T is the transfer length (where the applied voltage drops to l/e of the value at contact edge)

$$L_T = \sqrt{\rho_C / R_{sh}}$$

Using the total resistances measured at different *d*, one can extract the specific contact resistance by a simple linear fitting.

However, all derivations above are under the assumption that the metal resistance R_M is zero, and the contact size (r_0) is much bigger than transfer length (L_T) $(r_0 >> L_T)$. In practice, the conditions may not apply. Marlow *et al.* took the effect of contact size and non-zero sheet resistance of the metal overlay into consideration, and analyzed the current spreading under the circular patterns by differential equation [103]. They found a good approximation to the exact Bessel function solution of the differential equation using the parameters extracted from the simple linear fitting above [103]. Assuming the simple linear fitting gives a contact resistance of R_C and sheet resistance of R_{sh} , and a non-zero metal resistance R_M , an effective transfer length L_T after considering the influence of contact size and R_M is [103]

$$L'_{T} = \frac{\frac{R_{C}}{a} + R_{M}(r_{0} - a) + \frac{aR_{M}^{2}}{R_{sh}}}{R_{M} + R_{sh}}$$

where *a* is a constant as

$$a = \sqrt{R_C / (R_M + R_{sh})}$$

Note that when R_M is zero, L_T can be reduced to L_T . Under this regard, a more accurate specific contact resistance R_C can be expressed as [103]

$$R'_C = R_{sh}L'^2_T$$

The analytical results have been compared with experimental data obtained from Au-Ge based ohmic contacts to n-GaAs, and proved to be effective [103]. Therefore, circular TLM pattern with the accurate model described above will be used in this work to determine the specific contact resistance.

4.3 In-situ Grown Single Crystal Al as an Ohmic Contact to N-ZnSe

Single-crystal Al has been grown in-situ on GaAs (100) by Molecular Beam Epitaxy (MBE) at room temperature, and was found to form a Schottky rectifying contact [104]. Furthermore, researchers have shown that MBE-grown Al can form a leaky Schottky-based ohmic contact as well as a self-aligned mask for selective etching in GaAs solar cell fabrication [105]. Al was also used as a n-type dopant for ZnSe [106], and could be embedded in many MBE systems for ZnSe growth. Moreover, it has close work function (4.06 - 4.26 eV) compared to the electron affinity of ZnSe (4.09 eV) [107, 108]. Therefore, MBE grown Al appears to be a good candidate for an ohmic contact to n-ZnSe.

In order to verify that, Al films were deposited on as-grown ZnSe samples by MBE. All samples were grown in a Varian Gen II MBE system on semi-insulating GaAs (100) substrates. Figure 4.4(a) shows the typical sample stack structure. Prior to growth, the substrates were first baked in the load-lock chamber at a temperature of 300°C for three hours to desorb water vapor. The GaAs substrates were then loaded in the growth chamber, and heated to 610°C under As overpressure to remove the native GaAs oxide layer. The thermal treatment process was continued until a dot diffraction pattern was confirmed by Reflection High Energy Electron Diffraction (RHEED). In order to provide a better-quality growth surface for ZnSe growth as well to electrically isolate the ZnSe layer, a 300 nm thick undoped GaAs buffer layer was grown

on oxide removed GaAs substrates at a temperature of 580°C, and with a V/III flux ratio of 15. Then a 1000 nm thick Al- or Ga-doped ZnSe was deposited in the same MBE growth chamber at 300°C. Carrier concentrations in ZnSe epi-layers were measured via Differential Capacitance-voltage (CV) measurements. An effusive cell with compound ZnSe source material was used to provide the beam flux for ZnSe growth.

The details of samples fabricated for this study could be found in Table 4.1. The 100 nm Al layers on differently doped ZnSe (sample A, B, C) were grown at room temperature (unheated substrate) in the same chamber right after ZnSe growth, with a growth rate of 1 Å/s. For comparison, one ZnSe sample was intentionally exposed to air for a day, and then reloaded into MBE system to grow Al under identical growth temperature and rate (Sample D). A circular transmission line (CTLM) pattern shown in Figure 4.4(b) was applied to all samples. HF:H₂O = 1:3 etchant was used to develop the patterns [104]. In addition, Ti/Au (20 nm/200 nm) layer grown by an e-beam evaporator with same CTLM patterns on ZnSe (sample E) was also fabricated for comparison to the in-situ Al contacts.

All I-V characteristics were measured by contacting the device with a probe station connected to a Keysight B1500A Semiconductor Parameter Analyzer. The Electron Backscatter Diffraction (EBSD) map was measured by a FEI Scios Dual Beam FIB/SEM system equipped with an Oxford EBSD detector. The specific contact resistances in Table I were calculated by methods described in a previous study and Chapter 4.2, since the contact size in this work does not satisfy the conditions in Chapter 4.2 ($r_0 >> L_T$) [103]. The model and solutions with non-zero metal sheet resistance was used to avoid underestimation of contact resistance [103].



Figure 4.4. (a) Sample stack structures for this study. (b) Schematic of the CTLM pattern. The inner circles have a radius of 50 μ m, and the spacings between inner and outer circles are 5 μ m, 10 μ m, 15 μ m, 20 μ m, 25 μ m, 30 μ m, respectively.

|--|

Carrier concentration	Contact metal and conditions	Measured specific contact
(cm ⁻³)		resistance ($\Omega \cdot cm^2$)
5×10 ¹⁸	Al as grown (sample A)	2.433×10 ⁻³

9×10 ¹⁷	Al as grown (sample B)	6.911×10 ⁻³
2×10 ¹⁷	Al as grown (sample C)	1.05×10 ⁻²
5×10 ¹⁸	Al reload (sample D)	7.033×10 ⁻³
5×10 ¹⁸	Ti/Au as grown (sample E)	Not ohmic
1.15×10 ¹⁹	Mg/Au as grown [99]	9.95×10 ⁻²
1.15×10 ¹⁹	In/Au as grown [99]	1.04×10 ⁻²
4.5×10 ¹⁸	In/Au + 250 °C anneal [99]	1.18
5×10 ¹⁶	Ti/Pt/Au as grown [100]	8.8×10 ⁻²
4×10 ¹⁸	Ti/Pt/Au as grown [100]	6.2×10 ⁻²
2×10 ¹⁹	Ti/Pt/Au as grown [100]	3.4×10 ⁻⁴
2×10 ¹⁸	In + 200 °C anneal [101]	5×10 ⁻²

Previous studies have shown Al could be grown epitaxially on GaAs at both elevated and room temperatures [104, 109-111]. In this work, Al films were grown at room temperature to form the contact to n-ZnSe. As shown in Figure 4.5(a), the ZnSe as grown (100) surface showed streaky RHEED pattern before Al growth, indicating an atomically flat surface. After initializing the Al growth, the RHEED pattern changed to spotty within first 3 minutes (corresponding to 20 nm Al), indicating a 3D growth mode. During the very first few Å, some additional diffraction spots were observed, which was also observed in previous study on Al on GaAs growth [104]. That could be caused by the change of Al lattice at the initial growth. The RHEED pattern turned streaky gradually and ended up with (3×1) surface reconstruction after a while (Figure 4.5(c) and 4.5(d)), which suggested the Al growth surface was highly perfect. Another point to be noted from the RHEED patterns is that the spacings between diffracted beams for Al and ZnSe were nearly the same (indicated by the arrows in Figure 4.5 with same separation distance). Previous studies also observed same diffracted beam spacings for Al on GaAs growth, and they proposed that a rotation of the face-center cubic (FCC) Al unit cell of 45° about the c axis will closely match the underlying GaAs lattice

[104, 109, 110]. Since ZnSe has very similar lattice constant with GaAs, we believe the same phenomenon happened during Al on ZnSe growth. To confirm that, EBSD was performed on the surface of Al film, and the orientation of the grown Al layer was confirmed to be (110)//(100) (Al/ZnSe) (Figure 4.5(e)). The orientation distribution map showed no divergence over the whole surface for all three directions, which further confirmed the single crystalline of Al film. Since the lattice plane spacing between d_[220] Al and d_[400] ZnSe only has a mismatch of 0.56%, it reasonable that the Al lattice could be rotated to match the ZnSe (100) lattice constant. The transient RHEED pattern mentioned above during initial growth was likely due to the lattice rotation. Identically (110)-oriented Al film was also observed during the Al on As-rich GaAs (100) growth at room temperature [109, 110].



Figure 4.5. RHEED patterns of (a) MBE ZnSe (100) as-grown surface, (b) after depositing 30 nm of Al on the MBE ZnSe. And (c), (d) shows RHEED patterns of Al when stabilized from different coordinates. The arrows indicate the positions of the diffraction from the bulk. (e) shows the orientation distribution map of Al surface by EBSD, z-axis is perpendicular to the growth surface. Color code: crystal axis along the axis direction.

The Al ohmic contacts used in this study were single-crystal Al grown on n-type ZnSe MBE layers, doped with Ga or Al with different carrier concentrations (sample A-C). Using MBE for in-situ contact

deposition, one could obtain an impurity-free metal-semiconductor interface, which is important for both device performance and scientific research [104]. For comparison, one ZnSe sample (sample D) was intentionally exposed to air for a day and then reloaded into MBE system for Al deposition. Ti/Au on n-ZnSe sample (sample E) was also fabricated as a traditional method to form ohmic contact for comparison study, since Ti/Pt/Au showed the lowest contact resistance among available literatures [100]. The I-V characteristics of as-grown Al, reload-and-grown Al, and Ti/Au on N-ZnSe layers are shown in Figure 4.6(a)-(d). It could be seen that all Al on ZnSe samples showed nearly ideal linear characteristics over a large current density range (up to 390 A/cm²). Especially, all Al on ZnSe samples exhibited great linearity in low operation voltage region. However, the Ti/Au on ZnSe sample showed rectifying (blocking) behavior, suggesting the existence of Schottky barrier blocking electron flows. Previous study showed as-deposited Ti/Pt/Au (10 nm/100 nm/200 nm) could form ohmic contact to n-ZnSe with an electron concentration greater than 10¹⁹ cm⁻³, and researchers attributed this to the interface interdiffusion between Ti and ZnSe, as well as the low work function of Ti [100]. Since Ti was identified as the key role for ohmic contact, in this study, Ti/Au (20 nm/200 nm) was deposited on n-ZnSe with a carrier concentration of 5×10^{18} cm⁻³ (sample E), but it failed to form an ohmic contact. This could be due to the lower doping level used in this study compared to previous one, or different content of interdiffusion due to fabrication procedures, or that a mechanism other than Ti plays the key role in the Ti/Pt/Au ohmic contact formation. Table 4.1 summarizes the properties of ohmic contacts in this study and previous literatures. It should be noted that Al contact has order of magnitude lower contact resistance compared to other known metal contacts with similar carrier concentrations in ZnSe. Interestingly, the contact resistance do not degrade for lightly doped ZnSe. In addition, there is no need for additional treatments, such as thermal annealing to form the Al ohmic contact. The in-situ metallization method using a low-cost single metal Al could greatly simplify the device fabrication procedure and save product costs.



Figure 4.6. I-V characteristics of (a) Al (sample A - D) and (c) Ti/Au (sample E) contact to n-ZnSe. The current limit set in (a) was 30 mA. (b) and (c) shows the corresponding I-V in semi-log scale. All data was measured from the circle with largest spacing on the CTLM pattern.

Theoretically, abrupt metal-semiconductor contacts can be described by the Schottky barrier model [93]. In practice, several non-ideal mechanisms including surface state, fermi-level pinning, and interface reactions make the measured barrier heights strongly diverge from the theoretical values [94, 95]. Previous studies obtained a barrier height of 0.66 eV for Al on n-type As-rich GaAs surface by MBE, and 0.72 eV for Ga-rich GaAs [104]. It is well-known the fermi level of n-type GaAs (100) as-grown surface will be strongly pinned at mid-gap due to formation of surface acceptor states during MBE growth [112]. The extracted barrier height values in previous study clearly demonstrate that the measured barrier height is intrinsically determined by fermi level pinning position [94, 112], *i.e.*, different surface stoichiometries of GaAs, which follows the Bardeen model [96]. In this study, the work functions of Al are comparable to the ZnSe electron affinity [107, 108]. Therefore, it would form a low-barrier Schottky contact if it follows the

Schottky model. The slightly nonlinear I-V characteristics of Al on ZnSe layers with lower carrier concentrations or exposed to air suggested the existence thermionic emission and/or quantum tunneling mechanism, indicating it behaves as a leaky Schottky contact with a very low barrier height. Besides, the contact resistances increase slightly with decrease of carrier concentrations, suggesting a higher barrier height for lower doped n-ZnSe. The result agrees with that Al-ZnSe is a Schottky limit contact. However, another metal combination (Ti/Au) would result in a rectifying contact to the same ZnSe surface (exposed to air). Since Ti has similar work (4.33 eV) function compared to Al, it seems contradict with the Schottky limit assumption. But a more recent work also showed that ex-situ deposited Ti on n-ZnSe with 2×10¹⁹ cm⁻ ³ carrier concentration exhibited rectifying behavior, and researchers attributed this to the ZnSe surface oxide after being exposed to air [102]. Therefore, the in-situ deposited Al on ZnSe could still follow the Schottky model. Furthermore, the low barrier height Schottky contact formed between Al and lightly doped ZnSe samples suggests there is no significant mid-gap fermi level pinning at n-ZnSe surface (as grown and air exposed), unlike GaAs mentioned above [104]. More interestingly, previous studies observed ex-situ deposited Al on heavily doped n-ZnSe $(2 \times 10^{19} \text{ cm}^{-3})$ by a metal evaporator showed rectifying behavior, like Ti [102], which appeared that the fermi level of air-exposed ZnSe surface will be re-pinned at mid-gap. However, in this study, MBE grown Al on air-exposed ZnSe with lower carrier concentration still exhibited a very low barrier height leaky Schottky characteristic. It is reasonable to expect that polycrystalline Al by evaporator could have different interface behavior compared to epitaxially grown single crystalline Al, or the epitaxial growth procedure could alter the surface properties of ZnSe. Further experiments are required to illuminate the difference between the epitaxial and polycrystalline interface.

In summary, we demonstrated in-situ MBE growth of single-crystal Al on n-ZnSe as a non-alloyed, low-resistance ohmic contact: (1) 2D growth mode with surface reconstruction was observed by RHEED during Al growth, and EBSD confirmed that Al lattice was rotated by 45° relative to substrate to (110)oriented in order to match the ZnSe (100) lattice constant; (2) I-V characteristics of Al on heavily n-ZnSe layers showed ideal ohmic characteristics, and similar contact resistances from n-ZnSe with different carrier concentrations were observed; (3) Leaky Schottky I-V characteristics for Al on lightly doped ZnSe samples suggests the Al-ZnSe could form a low barrier height Schottky contact, and there is no strong mid-gap fermi level pinning at n-ZnSe surface (both as-grown and air exposed), which is different from n-GaAs. In-situ grown Al on n-ZnSe could be a Schottky limit contact; (4) Comparison with recent work [102] showed polycrystalline Al by evaporator and epitaxially single crystalline Al have different interface behaviors. More investigation will be performed to further explain the nature of Al/ZnSe interface.

MBE grown Al was found to form ohmic contact to n-ZnSe without any additional treatment like plasma or annealing used for traditional ohmic contacts. It has lower contact resistance (up to 2.433 x 10^{-3} Ω •cm²) compared to all current available metal contacts to n-ZnSe with similar carrier concentration. Moreover, the low contact resistance doesn't rely much on the carrier concentration of bulk ZnSe, which could enable application to circumstance that requires lightly doped material. This method could greatly reduce the fabrication complexity and cost for ZnSe based device applications. Furthermore, it could be generalized to solve the common ohmic contact difficulty for other wide-gap II-VI materials with similar electron affinity.

4.4 Ex-situ Grown Cu as a Novel Ohmic Contact to N-ZnSe

In Chapter 4.3, we demonstrated that single crystal Al could be grown by MBE on ZnSe (100) surface at room temperature. In-situ MBE grown Al can serve as a uniform, low-resistance ohmic contact to n-ZnSe epi-layers over a large doping range without any additional treatment such as annealing or plasma. However, this method may not apply to all application scenario, since it requires Al effusion cell in the MBE system. Although in-situ Al ohmic contact has superior properties, another universal metal contact method without special requirements on MBE configuration will be explored.

Using the same structure as Figure 4.4(a), 100 nm of Cu films were deposited on MBE-grown ZnSe layers. The ZnSe growth procedure has been described in Chapter 4.3 and the same procedure was used

here. The Cu layers were deposited by an e-beam evaporator with a growth rate of 1 Å/s. Same CTLM pattern in Figure 4.4(b) was fabricated on the samples using lift-off procedures. All I-V characteristics were measured by contacting the device with a probe station connected to a Keysight B1500A Semiconductor Parameter Analyzer. The X-ray photoelectron spectrometer (XPS) measurements were taken by a Kratos Supra Axis XPS, with an Ar ion gun for cleaning and depth profile. The specific contact resistances in Table 4.2 were calculated by the same method in Chapter 4.2.

The details of samples fabricated with Cu contact could be found in Table 4.2, with a comparison to the Al-ZnSe samples in Chapter 4.3. The I-V characteristics of Cu and Ti/Au on different n-ZnSe layers are shown in Figure 4.7(a)-(b). It could be seen that the Cu on ZnSe sample with higher ZnSe doping concentration $(5 \times 10^{18} \text{ cm}^{-3})$ has nearly ideal linear characteristics over a large current density range. The one with lower doping concentration $(2 \times 10^{17} \text{ cm}^{-3})$ still exhibited quasi-linear I-V characteristic, but with higher resistivity. Especially, all Cu on ZnSe samples exhibited great linearity in low operation voltage region compared to the Ti/Au contact, which has a Schottky non-linear behavior. From Table 4.2, both Cu ohmic contacts have slightly higher contact resistance than the MBE-Al contact with the same ZnSe carrier concentration, but they're still within the same order of magnitude. The slightly nonlinear I-V characteristic of Cu on ZnSe layer with lower carrier concentration suggested the existence thermionic emission and/or quantum tunneling mechanism. Since the ZnSe layer was not heavily doped, the space charge region near the metal-semiconductor interface will not be thin enough to support massive tunneling of carriers. The slight nonlinearity in I-V characteristic indicated it behaves as a leaky Schottky contact with a very low barrier height. Therefore, Cu seems to be able to form an ohmic contact to n-ZnSe over a big doping range also.

Contact metal and	Measured specific contact
growth methods	resistance ($\Omega \cdot cm^2$)
Al as grown (MBE, sample A)	2.433×10 ⁻³
Al as grown (MBE, sample B)	6.911×10 ⁻³
Al as grown (MBE, sample C)	1.05×10 ⁻²
Al reload (MBE, sample D)	7.033×10 ⁻³
Cu as grown (E-beam)	7.651×10 ⁻³
Cu as grown (E-beam)	3.952×10 ⁻²
Ti/Au as grown (E-beam, sample E)	Not ohmic
	Contact metal and growth methods Al as grown (MBE, sample A) Al as grown (MBE, sample B) Al as grown (MBE, sample C) Al reload (MBE, sample D) Cu as grown (E-beam) Cu as grown (E-beam) Ti/Au as grown (E-beam, sample E)

Table 4.2. Comparison of the Cu ohmic contacts on n-type ZnSe with other metal contacts in this work (sample A-E,Chapter 4.3).



Figure 4.7. I-V characteristics of (a) Cu and Ti/Au contact to n-ZnSe. The current limit set in (a) was 10 mA, and (b) shows the I-V in semi-log scale. All data was measured from the circle with largest spacing on the CTLM.

Since it was demonstrated that the n-ZnSe in this work doesn't exhibit significant fermi-level pinning at the surface in Chapter 4.3. Therefore, the Cu-ZnSe metal-semiconductor contact should follow

the Schottky barrier model, like Al-ZnSe contact. However, the work-function of Cu (4.6 - 4.7 eV) is much lower than the ZnSe electron affinity (4.09 eV) [108, 113]. Theoretically, it should form a Schottky contact to n-ZnSe with a barrier height bigger than 0.5 eV, which contradicts the measured I-V characteristics.

Cu was once used to form ohmic contacts to p-ZnSe [99, 114]. Park *et al.* found that Cu/Au could form an ohmic contact to p-ZnSe $(1 \times 10^{17} \text{ cm}^{-3})$ with a contact resistance of 1.97 $\Omega \cdot \text{cm}^2$. It can be further reduced to 0.167 $\Omega \cdot \text{cm}^2$ with N₂ plasma treatment [99]. However, they also observed thermionic emission mechanism dominated that I-V characteristics of Cu to p-ZnSe contact, and with an estimated barrier height of 0.53 eV, which does not follow the Schottky barrier model. Moreover, Koide *et al.* extracted of a ~1.1 eV barrier height for Cu to p-ZnSe contact with C-V and I-V measurements [114]. Since p-ZnSe has a high electron affinity bigger than 6 eV (4.09 + 2.7 eV), the 1.1 eV estimation is close to the theoretical value from the Schottky barrier model. Previous studies, including the results in this work, showed a great contradiction about the nature of Cu/ZnSe contact. Some mechanisms must exist to alter the interface chemical properties of Cu/ZnSe.

To bring more insight, XPS spectra was taken near the Cu/n-ZnSe interface region in this work (Figure 4.8). From the XPS spectra, Cu-Se bond was detected at the interface, and the binding energies of Cu and Se orbits coincided with the binding energy of bulk Cu₂Se. This indicates the existence of Cu-Se bonds with similar bonding environment in Cu₂Se or a Cu₂Se phase at the Cu/ZnSe interface. Cu₂Se was believed to be a p-type semiconductor with a very low band-gap [115]. Aven *et al.* fabricated In-Ag/Cu₂Se/n-ZnSe junctions and observed injected electroluminescence at 77 K [115]. They estimated the band-gap of Cu₂Se to be 0.5 - 0.7 eV, but the electron affinity of Cu₂Se was unknown to them [115]. More recently, Cu₂Se was extensively explored as a candidate for thermoelectric (TE) devices [116]. Theoretical calculations showed that Cu₂Se has a semi-metallic behavior with a band-gap of 0.5 eV [116]. Moreover, the Cu (I) in Cu₂Se was used as a p-type dopant source in ZnSe grown by pulsed layer deposition [117]. Since the Cu to n-ZnSe contact in this work didn't show any diode behavior, and Cu-Se bond was observed by XPS. We believe the Cu (I) or a thin layer Cu₂Se might exist cannot convert the conducting type of n-

ZnSe surface layer to be p-type. According to all previous studies about Cu₂Se and ZnSe, Cu₂Se is a very low band-gap semiconductor or semi-metal. It is very likely that the Cu-Se bond provides a contacting layer with a low band-gap at the Cu/ZnSe transition region, or the Cu-Se bond reduces the local work-function of Cu. One of both the mechanisms mentioned above lowered the barrier height of Cu/n-ZnSe contact and thus facilitated the formation of a novel ohmic contact.



Figure 4.8. XPS spectra of (a) Cu 2p and (b) Se 3d orbits from the Cu/ZnSe interface. The binding energies of Cu and Se coincide with the binding energies of Cu and Se in bulk Cu₂Se.

In summary, we demonstrated ex-situ deposition of Cu layer on n-ZnSe as a novel, low-resistance ohmic contact: (1) I-V characteristics of Cu on heavily n-ZnSe layers showed ideal linear characteristics, with a slightly higher contact resistance than MBE-Al to n-ZnSe; (2) Slightly nonlinear I-V characteristics for Cu on lightly doped ZnSe samples suggests the Cu to n-ZnSe could form a low barrier height Schottky contact, which doesn't follow the Schottky barrier model; (3) XPS showed the existence of Cu-Se bond at

Cu/ZnSe interface, with the same binding energies as in the bulk Cu_2Se . The low-band-gap Cu_2Se phase or Cu-Se could act as a contacting layer which lowered the barrier height for Cu/n-ZnSe contact. The detailed mechanism is still under investigation.

Ex-situ deposited Cu was found to form ohmic contact to n-ZnSe without any additional treatment used for traditional ohmic contacts. It has a low contact resistance (up to 7.6 x $10^{-3} \Omega \cdot \text{cm}^2$) compared to available metal contacts to n-ZnSe with similar carrier concentration. The contact resistance is relatively insensitive to the carrier concentration of ZnSe. Although having slightly higher resistance than MBE-Al contact, the Cu contact doesn't require an Al cell in MBE system and could be a more universal contact for ZnSe-based devices.

4.5 Summary

Novel ohmic contacts to n-ZnSe are demonstrated using both single crystal Al films in-situ deposited on epitaxially grown ZnSe (100) by molecular beam epitaxy (MBE), and ex-situ deposited Cu films.

For the Al contact, EBSD confirmed the single crystalline structure of the Al films. The (110)oriented Al layer was rotated 45° relative to substrate to match the ZnSe (100) lattice constant. The asgrown Al-ZnSe contact exhibited nearly ideal ohmic electrical characteristics over a large doping range of n-ZnSe without any additional treatment. The contact resistances are in a range of 10⁻³ ohm-cm² for even lightly doped ZnSe (~10¹⁷ cm-3). Leaky Schottky behavior in lightly doped ZnSe samples suggested Al-ZnSe formed a low barrier height, Schottky limit contact. In-situ grown Al could act as a simple metal contact to n-ZnSe regardless of carrier concentration with lower resistance compared to other reported contacts in literatures. For the Cu contact, XPS revealed the existence of Cu-Se bond at the Cu/ZnSe interface, with similar binding energies as in Cu₂Se bulk material. This finding is believed to be responsible for the non-Schottky limit contact behavior. Cu-ZnSe contact has similar resistance with Al-ZnSe contact, and is relatively insensitive to ZnSe carrier concentration. It doesn't require any additional treatments, or special configuration of the MBE system. It could act as a universal contact method for ZnSe-based devices.

The reported novel metallization methods could greatly simplify the ZnSe-based device fabrication complexity as well as lower the cost. Part of this Chapter is reproduced from our publication: Z. Fan, R. Bunk, G. Wang, and J. M. Woodall, *J. Vac. Sci. Technol. B* **38**, 042204 (2020) [98], with the permission of AIP Publishing.

5 Summary and Future Directions

In summary, this work explored the MBE ZnSe-GaAs semiconductor system, a well-recognized potential candidate for versatile electronic and photonic devices, in details from fabrication procedure, materials property to device application. Systematic investigations on the ZnSe-GaAs interfaces, the bottleneck for the realization of high-quality ZnSe-GaAs heterostructures, were performed using comprehensive materials characterizations. Correlations between observed properties and fabrication procedures have been established to guide the improvement of grown materials quality. Findings in this work are important to understand the nature of ZnSe-GaAs interfaces for the realization of high quality ZnSe-GaAs heterostructures for further device research. Besides, novel ohmic contacts to n-ZnSe were demonstrated using both in-situ deposited single crystal Al films on epitaxially grown ZnSe by MBE, and ex-situ deposited Cu films. Both contacts exhibited low contact resistances among available studies, and were relatively insensitive to carrier concentrations. Different mechanisms behind the ohmic contact formation were studied and discussed. As a necessary component for all semiconductor devices, these results could contribute to the industrial applications of all ZnSe-based devices. Especially, using the fabrication methods established in this work, ZnSe/GaAs/ZnSe single QW structures for potential light emitting devices were explored. Intense PL emission other than conventional QW with eigenstate emission was observed in this work. Detailed investigations utilizing available experimental setup and previous studies have been carried out to understand the luminescence mechanism in the complicated PL emissions from the QW structures. Although a non-ambiguous conclusion cannot be drawn regarding the luminescence mechanism right now, seminal results revealed that the QW structure in this work has great potential to be used as stable, efficient light emitting devices including in the passive lighting technology and soft photonic devices.

5.1 Outlook: ZnSe-GaAs System as Light Emitting Devices

The very original motivation for us to study the ZnSe-GaAs system is the potential usage as LEDs by fabricating digital alloys. After revisiting the previous challenges in fabricating high quality ZnSe-GaAs interfaces, as well as obtaining many new findings in this work as described in previous chapters, ZnSe-GaAs digital alloys fabrication by MBE appears to be difficult. However, instead of abrupt interfaces, the intermixed ZnSe-GaAs structures, like the ZnSe-GaAs QW in this work, might've unveiled another path to realize ZnSe-GaAs based highly efficient LEDs. It might be able to resolve the current challenges in microLED business, as conventional GaN-based LEDs face surface state induced efficiency degradation as the device size shrinks. As described in Chapter 1, a high-quality p-n junction is required to realized active LEDs. For this work, the intermixed ZnSe-GaAs in n-ZnSe exhibited strong luminescence. Therefore, another p-type layer is needed to inject holes into the n-ZnSe to realize an active lighting device. The goal seems to be trivial, since p-ZnSe, though under optimized, has been realized in 1980s. However, we can foresee challenges in two ways for using ZnSe homojunction p-n junction for the purposed LEDs:

- The highest p-type carrier concentration could be achieved in ZnSe is only around 10¹⁸ cm⁻³, which is not ideal for LED applications since we need more holes to be injected into the n-ZnSe, where the radiative recombination happens, to boost the efficiency. More importantly, the p-type dopant was identified as one of the main failure mechanisms for degradation in ZnSe-based photonic devices.
- The p-n homojunction structure is typically avoid in modern LED designs for efficiency concerns
 [4]. Semiconductor layers with higher band-gaps are typically used to confine the carriers in the
 active layer (in our case: the n-ZnSe-GaAs intermixed layer) in LEDs, such as doubleheterostructure (DH) LED designs.

Therefore, as described above, a p-type semiconductor other than ZnSe, preferably with a higher band-gap, will be an ideal choice for realizing ZnSe-GaAs based LEDs. Since ZnSe itself is a wide-gap semiconductor,

the candidates for this job are limited, especially considering the compatibility issues. GaN or other II-VI semiconductors like ZnS or ZnO could be possibly used, but the fabrication will be challenging due to compatibility issues. In addition, device architectures other than conventional p-n junction could also be a good way to go for ZnSe-GaAs based LEDs. Despite the foreseen challenges, we believe ZnSe-GaAs based LED is a direction with great potential and worthwhile to be further explored.

5.2 Outlook: Other Potential Devices Based on ZnSe-GaAs System

Except for the LED applications described above, ZnSe-GaAs as a lattice matched, direct band gap semiconductor system with many explorable interface properties, could find applications in other electronic and photonic devices. Hereby some potential structures are proposed in the following.

GaAs has been used as efficient solar cells since 1970s [118-120]. In addition, with a higher bandgap AlGaAs window layer latticed matched to GaAs, the solar cell efficiency could be greatly improved [118-120]. However, the absorption of solar power in the window layer could result in efficiency drop in shorter wavelength region. Simulation results showed that if a wider band-gap window layer is used, an overall higher efficiency could be achieved over larger solar spectrum [121]. ZnSe has a wider direct bandgap than AlGaAs, and we showed low defect density ZnSe/GaAs interface could be obtained by growing ZnSe on Ga-rich GaAs surface. If ZnSe could be used as a window layer for GaAs solar cell, it will further improve its efficiency especially in shorter wavelength spectrum. Moreover, AlGaAs has also been studied as the top cell, which is current matched to Si, for AlGaAs/Si tandem cells [122-123]. ZnSe could also replace the current window layer (Al-rich AlGaAs) to improve the shorter wavelength response as described above. Combined with epitaxial lift-off technique which has been successfully applied in MBE-grown GaAs solar cell [123], one could re-bond MBE-grown ZnSe/AlGaAs top cell to a Si solar cell for a highefficiency tandem cell with reduced fabrication complexity and cost. Except for the solar cell, AlGaAs/GaAs/GaN heterojunction bipolar transistors (HBTs) was extensively studied as a promising candidate for microwave device expected to have high-current gain, high cut-off frequency and to operate at high power densities [124-126]. All the attractive features are owing to the mature fabrication process for AlGaAs/GaAs HBTs as well as the large breakdown field and high anticipated saturation velocity of wide-gap GaN. However, since GaN and GaAs have different lattice constants and structures, researchers had to bond them together by wafer fusion, which not only add to the fabrication difficulty, but also introduce many interface states and thus greatly compromise the device performance [125-126]. ZnSe, on the other hand, is also a wide gap semiconductor with high anticipated saturation velocity, but lattice matched to GaAs. More importantly, ZnSe/GaAs interface showed low defect density as described above. Therefore, it will be a highly promising candidate for this technology.

In summary, ZnSe-GaAs system is a complicated but highly explorable research topic. I hope this work can lead to more future research on ZnSe-GaAs materials properties and the aforementioned explorable devices, and more potential application beyond.

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