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Low-Power Blocks for UWB Transceivers

DISSERTATION

submitted in partial satisfaction of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering and Computer Science

by

Joshua H. Kim

Dissertation Committee:

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Professor Stuart Keinfelder

2015

DEDICATION

To my loving wife and daughters

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ABSTRACT OF THE DISSERTATION

Low-Power Blocks for UWB Transceivers

By

Joshua H. Kim

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine, 2015

Professor Michael Green, Chair

In this dissertation, low-power blocks in UWB transceiver systems are presented. In particular, the main focus of this study is how low-power blocks in an impulse radio UWB (IR-UWB) system can be employed in sensor networks such as Body Area Networks (BANs).

The thesis is divided into three general parts. In the first part, the general history, definitions, regulations, and development of UWB systems are reviewed. In addition, a brief explanation of the fundamental concepts of radio frequency communication in short duration of pulses is given.

In the second part, the startup behavior of LC-VCOs used in UWB transmitters is investigated. In order to decrease the power consumption of the circuits without adding any complexity, we deliberately introduce a small asymmetry into the VCO that can greatly reduce the oscillation start-up time.

Finally, we study the super-regenerative receiver architecture and the challenges it presents. In this work, we have designed a low-power 4 Mb/s super-regenerative receiver in a 0.18 µm CMOS process that tracks the incoming signal carrier pulse and synchronizes it with a pulse

quench signal. The energy consumption for this receiver is 0.17 nJ/bit, which demonstrates the

lowest energy consumption reported so far for an IR-UWB receiver system.

Chapter 1. Ultra-Wideband Communication Overview

1.1 Introduction

A. UWB communication system

In 2002, the Federal Communication Commision (FCC) allowed unlicensed operation between 3.1 GHz and 10.6 GHz for UWB communication, using an appropriate wideband signal format with a low Effective Isotropic Radiated Power (EIRP) level (-41.3 dBm/MHz) [1]. Since that time UWB communication systems have emerged as an alternative to narrowband systems since their wide bandwidth (at least 500 MHz) allows more robust transmission in the presence of multipath, jamming, and other phenomena that are challenging to conventional narrowband systems. There are two main technical approaches to the development of UWB systems. One is multi-band (MB) OFDM UWB and the other is impulse radio (IR) UWB. Unlike an MB-OFDB UWB system, an IR-UWB system can be designed with relatively low complexity and low power consumption [2-10]. Therefore, IR-UWB can be well-suited for energy-constrained, short-range wireless applications including low-power sensor networks, personal-area-networks, and body-area-networks.

B. History of UWB

Most people would consider UWB as a recent breakthrough in wireless technology, but UWB has actually experienced well over 40 years of technological developments. UWB had its origins in the spark-gap transmission design of Marconi and Hertz in the late 1880s. Sparked gaps and arc discharges between carbon electrodes were the dominant wave generators about 20 years after Hertz's first experiments [11-15]. The physical cornerstone for understanding UWB

pulse propagation was established by Sommerfeld in 1901 when he investigated the diffraction of a time-domian pulse by a perfectly conducting wedge [16]. As mentioned in the previous section, continuous waveform had been the dominant form of wireless communications in early radio development, and it was not until the 1960s that research began again heavily in the area of time-domain electromagnetic waves. The introduction of the sampling oscilloscope in the early 1960s further motivated development of techniques for generating sub-nanosecond baseband pulses sped up the development of UWB [17]. In 1973, the first US patent was awarded for UWB communications [18], and the field of UWB was expanding into applications such as automobile collision avoidance, positioning systems, liquid-level sensing, and altimetry [14]. Most of these applications and development occurred in the military or in work funded by the US Government under classified programs. For the military, accurate radar and low probability of intercept communications were the driving forces behind research and development [19]. The late 1990s was the time to commercialize UWB communication devices and systems. Companies such as Time Domain and XtremeSpectrum were formed around the idea of consumer communication using UWB [20-21]. A substantial change occurred in February 2002 when the US Federal Communications Commission (FCC) issued a ruling that UWB could be used for data communications as well as radar and safety applications [22-23].

C. Basic definitions of UWB

The U.S Federal Communication Commission (FCC) makes the following definitions [22,23]:

1) UWB bandwidth

As illustrated in Fig. 1.1, UWB bandwidth (f_h - f_l) is the frequency band bounded by the points that are 10 dB below the highest radiated emission, as based on the complete transmission

system including the antenna. The upper boundary is designated f_h and the lower boundary is designated f_l. The frequency at which the highest radiated emission occurs is designated f_m.

2) Center frequency

The center frequency f_c is the average of f_h and f_l, that is,

$$f_c = \frac{f_h + f_l}{2}$$

(1.4)

Fig 1.1 illustrates graphically the definitions of f_h, f_l, and f_c. In this example, the center frequency, f_c and f_m are equal.

3) Fractional bandwidth

The fractional bandwidth is defined as

$$FB = 2\frac{f_h - f_l}{f_h + f_l}$$

(1.5)
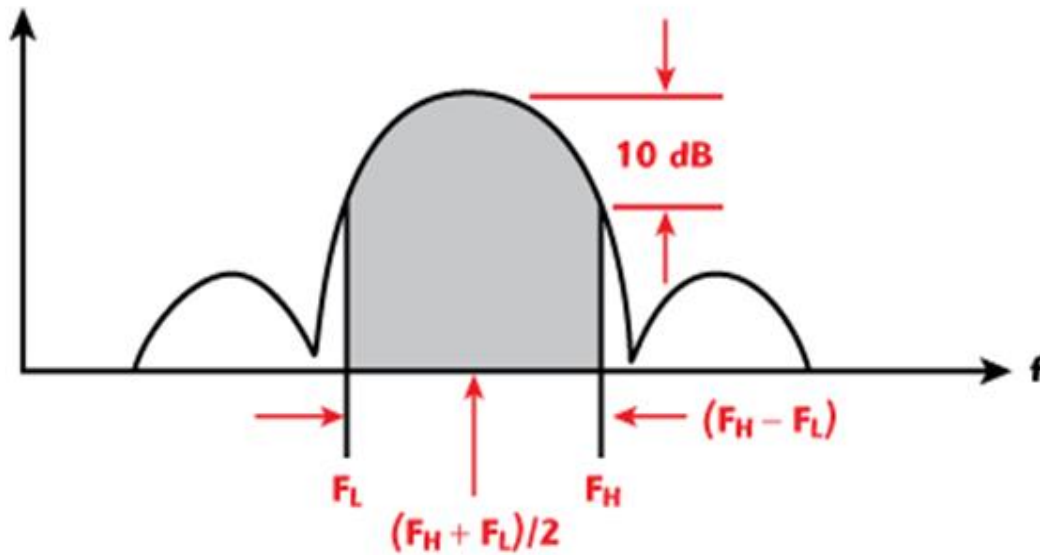
Fig. 1.1. Definition of UWB bandwidth, upper bounded frequency, low bounded frequency, and center frequency [30].

4) UWB transmitter

A UWB transmitter is an intentional radiator that, at any point in time, has a fractional bandwidth greater than or equal to 0.20 or has a UWB bandwidth greater than or equal to 500 MHz, regardless of the fractional bandwidth.

5) Equivalent isotropically radiated power (EIRP)

EIRP is the product of the power supplied to the antenna and the antenna gain in a given direction relative to an isotropic antenna. EIRP refers to the highest signal strength measured in any direction and an any frequency from the UWB device.

D. Regulatory Consideration

All radio communication is subject to different regulations about power output in certain frequency bands in order to prevent interference from other users in nearby or the same frequency bands. The spectrum of a UWB signal is one of the major issues confronting the industry and governments for the commercial use of UWB. UWB systems cover a large spectrum and interfere with existing users. In order to keep this interference to a minimum, the FCC specifies spectral masks, such as the one in Fig. 1.2 [24]. A large bandwidth of 7.5 GHz is available between 3.1 GHz and 10.6 GHz at a maximum power output of -41.3 dBm/MHz. The major reasons for the very low ouput power specification in the frequency bands 0.96-1.61 GHz is to avoid interference with other existing services, such as mobile telephony, GPS, and military usage [17].
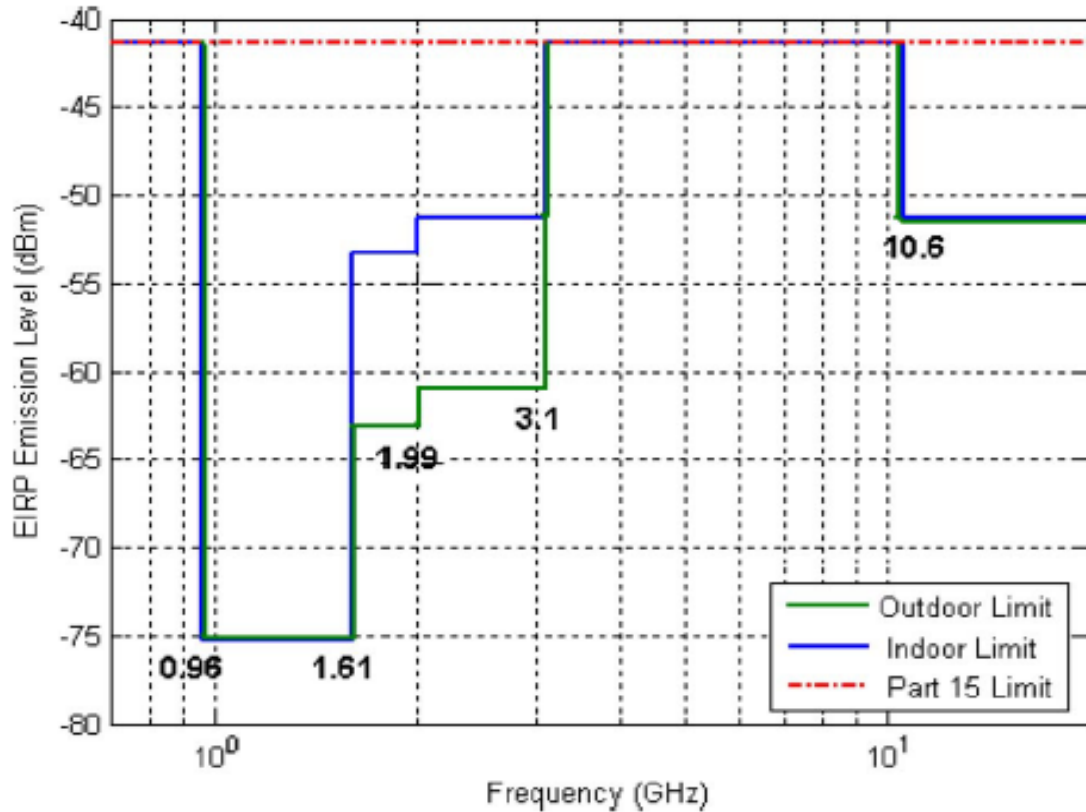
Fig. 1.2: Spectral mask mandated by FCC for indoor UWB system [35]

E. Advantage of UWB

UWB has a number of advantages that make it attractive for consumer communications applications. First, UWB systems transmit a noise-like signal, which makes unintended detection quite difficult. In addition, UWB transmissions do not cause significant interference to existing radio systems [26]. As shown in Fig 1.3. [27], in contrast to narrowband signals used in commercial radio and broadband communication like WLAN 802.11a, the emitting signal power level of UWB appears similar to the noise floor. Consequently, there is no interference with other conventional narrow band and carrier wave used in the same frequency band.
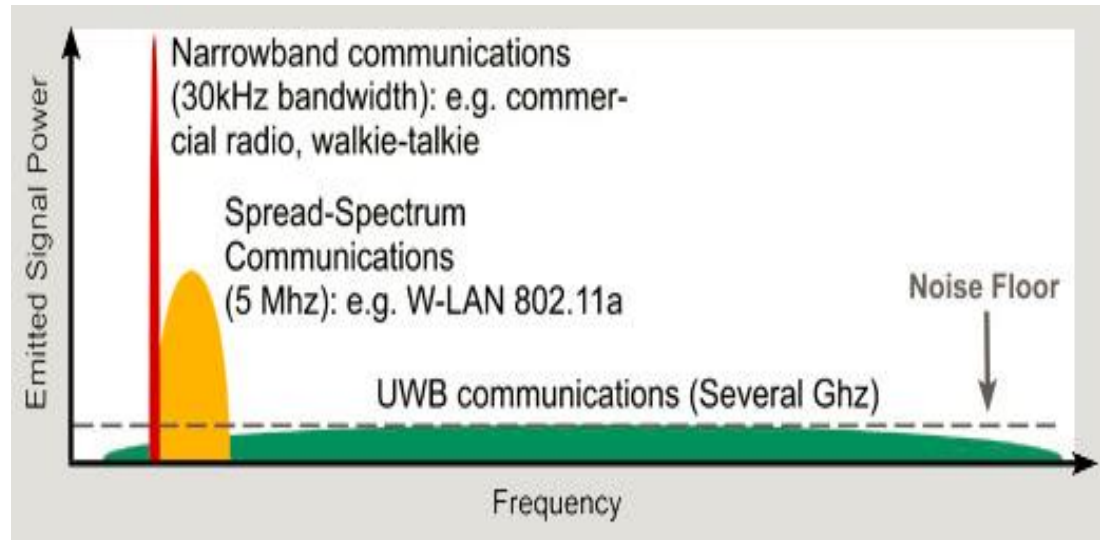
Fig. 1.3: Comparison of spectrum occupation of narrowband, wideband, and UWB

Another advantage of UWB systems has to do with their robust performance in the presence of multipath signals [17]. Multipath is the phenomenon at the receiver whereby an electromagnetic signal travels by various paths to the receiver after transmission. This effect results from reflection, absorption, diffraction, and scattering of the electromagnetic energy by objects in between the transmitter and the receiver. Due to the different lengths of the paths, transmitted pulses will arrive at the receiver at different times, with the delay proportional to the path length. As a result, longer pulses will likely overlap with each other, and thus will interfere, resulting in inter-symbol interference (ISI). However, the very short pulses used in a UWB systems are very unlikely to overlap; thus, they can be filtered out in the time domain. In addition to these characteristics, UWB systems have very good time-domain resolution, which allows for location and tracing application. If the time of arrival of a pulse is known, then it is possible to accurately estimate the distance travelled by the pulse from the source. By combining the distance estimates at multiple receivers, the position of the source can be

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estimated by employing triangulation techniques. For example, the maximum time resolution of a pulse for a UWB system with a 7.5 GHz bandwidth is on the order of 133 picoseconds, which means that time of the flight of the pulse can be estimated when the pulse arrives. Consequently, the pulse displays 4 cm spatial error corresponding to the order of 133 picoseconds time uncertainty. For a more modest bandwidth of 500 MHz, the corresponding time resolution is 2 nanoseconds, which corresponds to a spatial uncertainty of approximately 60 cm. Because of the short pulse duration, it is possible to achieve sub-meter accuracy in positioning with any UWB signal [26].

F. Application

1) High data rate (IEEE 802.15.3a)

UWB systems offer very promising wireless data connectivity between a host, such as a desktop PC, and associated peripherals, such as a keyboard, mouse, or printer. A UWB link can meet transfer data rate requirements that range from 100 kbps for a wireless mouse to 100 Mbps for rapid file sharing or download of images and/or graphic files [28]. In order to achieve a high data rate, there are three viable techniques that meet the UWB regulatory requirements: Orthogonal Frequency Division Multiplexing (OFDM), Direct Sequence Ultrawideband (DS-UWB), and Time Division/Frequency Division Multiple Access (TD/FDMA) pulses. Each of them is briefly summarized in Table 1 [11].

Table 1. Three techniques of implementing UWB systems for high data rate

	OFDM	DS-UWB	TD/FDMA pulses
Bands	3–13	2	3–13
Bandwidths	3 × 528–13 × 528 MHz	1.5 and 3.6 GHz	3 × 550–13 × 550 MHz
Frequency ranges, GHz	3.1–4.8 4.8–10.6	3.1–5.15 5.825–10.6	3.1–5 4.9–10.6
Modulation	OFDM-QPSK	M-BOK, QPSK	M-BOK, QPSK
Modulation efficiency: 10^{-3} BER	6.8 dB	4.1–6.8 dB	6.1–6.8 dB
Error correction	Convolutional	Convolutional and Reed–Solomon codes	Convolutional and Reed–Solomon codes
Margin at 10 m	6 dB at 110 Mbps	6 dB at 112 Mbps	6 dB at 108 Mbps
Margin at 4 m	11 dB at 200 Mbps	11 dB at 224 Mbps	8 dB at 288 Mbps
Margin at 4 m	6 dB at 480 Mbps	6 dB at 448 Mbps	4 dB at 577 Mbps

2) Low data rate (IEEE 802.15.4a)

An important emerging application of UWB is for sensor networks that range from mobile computing to body area networks (BAN). Various Ultra-Wideband wireless sensor network applications include locating and imaging of objects and environments [31], perimeter intrusion detection [32], video surveillance [33], in-vehicle sensing [34], outdoor sports monitoring [35], monitoring on the highway, bridges, and other civil infrastructure [36]. There have also been many reported devices and systems to demonstrate the possibility of UWB technology for wireless sensor network applications including UWB chips and radio module design [37-43], precision locating system designs [44], and body area network system design [45]. The widely used modulation schemes for low-data rate UWB include pulse amplitude modulation (PAM), on-off keying (OOK), and pulse position modulation (PPM) [29]. With

selection of the appropriate modulation scheme, UWB allows a low-power and low-cost implementation of a communication system.

G. Dissertation outline

The rest of the dissertation is organized as follows.

In Chapter 2, an LC-VCO that exhibits a fast startup time, useful for a UWB transmitter, is characterized. This chapter includes comprehensive research of power-efficient pulse transmitting theory, analysis, and CMOS implementation.

In Chapter 3, a super-regenerative receiver (SRR) is presented. Novel design techniques are presented that allow for very low power dissipation. In addition, a delay-locked loop and digital blocks are realized to obtain synchronization.

In Chapter 4, we conclude with a summary of our contributions, and directions for future research.

Chapter 2. Fast Start-up of Energy Efficient UWB Transmitter

2.1 Introduction

In a wireless sensor network (WSN), many spatially distributed radio transceivers with attached sensors are employed to monitor environmental conditions, such as temperature, sound, vibration, pressure, or motion at various locations on the structure being monitored [46-51]. Typically, these transceivers should be small, simple, inexpensive, and allow for a long battery life. In addition, they must be robust in order to communicate sensor data without interference, and allow for various types of networking protocals.

A. Body Area Networks (BANs)

As shown in Fig. 2.1., a Body Area Network (BAN) that connects nodes attached to the body surface, implanted in a tissue or body, or dispersed clothing has becomes an emerging technology due to the significant research and development in WSN [52]. The nodes in a BAN can be implanted medical devices, biomedical/biochemical sensors such as electrocardiogram (ECG) electrodes, assistive devices, activity sensors, and data storage. Due to the stringent energy consumption of the future BAN, UWB can be the most suitable candidate for low-power short-range radio [52].
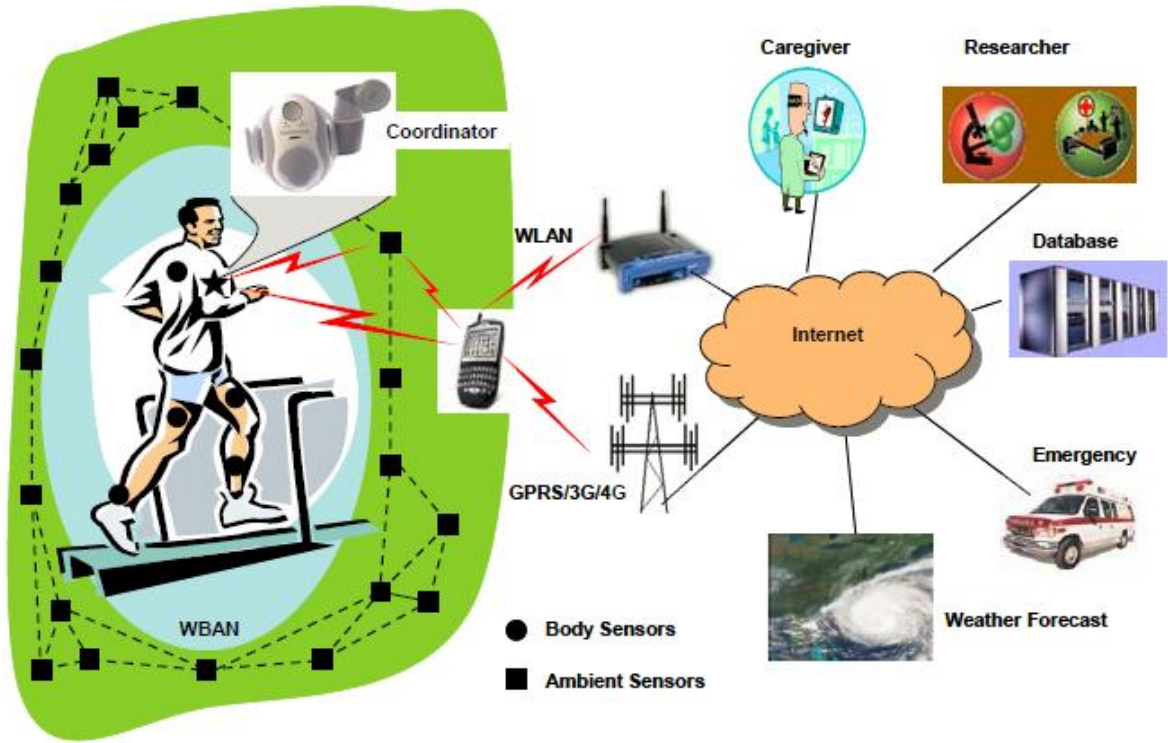
Fig. 2.1: System architecture integrating BAN with pervasive sensing [52].

A BAN consists of many transmit-only sensor nodes that need to be simple, low cost, and energy efficient. Some of these transceiver nodes can be more complex in order to sense and act, and a few of these high-capability nodes (e.g., master nodes) have high computational and communication capabilities. The sensor nodes of BANs usually have a low data rate, allowing the radio to operate in burst mode with minimal duty cycle. The sensor node operates mainly as a transmitter and there is a strong asymmetry in the communication link. This asymmetry can be exploited by shifting as much complexity as possible to the more capable device (e.g., master device). In a pulse-based UWB, the transmitter only needs to operate during the pulse transmission, which reduces the baseline power consumption. In UWB communication, most of the complexity is in the receiver, allowing the realization of an ultra-low-power, lowest-complexity transmitter in the sensor node, which fits the asymmetric nature of communication

between the sensor nodes and the more powerful master node. The low complexity of the UWB transmitter offers the potential for low-cost and highly integrated solutions.

2.2 UWB Transmitter Architecture

As shown in Fig. 2.2, the pulsed-based UWB transmitter architecture is quite simple. Pulsed-based UWB transmitters can be typically categorized into two groups, depending on how pulses are generated in the 3.1 GHz to 10.6 GHz band. Transmitters in the first group generate a single pulse in the UWB band without requiring frequency translation. This type of transmitter often employs pulse-shaping circuitry to meet the FCC emission limit. The UWB signal generated by such transmitters is referred to as carrier-free impulse or mono-pulse UWB signal.
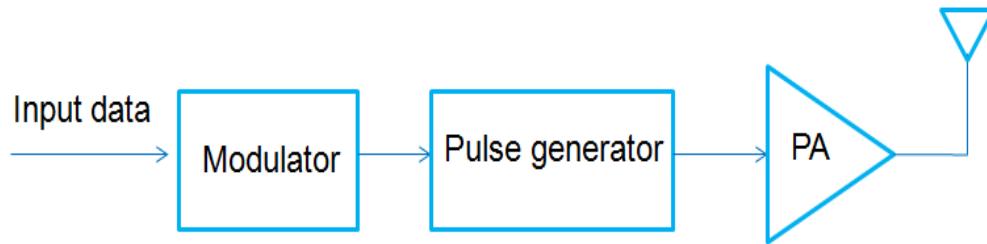
Fig. 2.2: A typical UWB transmitter architecture.

The other group includes transmitters referred as carrier-based UWB transmitters that generate a pulse at baseband and up-convert it to a center frequency in the UWB band using a local oscillator. In order to meet the FCC emission limit, the width of the input pulse and frequency of the oscillator are adjusted to generate the appropriate bandwidth and center frequency, respectively, in the UWB band. Compared to the carrier-free impulse UWB technology, carrier-based UWB systems generally offer more diversity and control over the frequency spectrum, but at the cost of higher power consumption due to the fact that the local oscillator must operate at the UWB band. In order to minimize the power consumption for

carrier-based UWB transmitter, LC VCOs, such as the one shown in Fig. 2.3, can be employed in both input data modulator and the pulse generator. For example, baseband input data can be fed into the gate of the tail current transistor through the switch circuit, which is then upconverted by the oscillator. A more concrete explanation of this will be discussed in the next section.
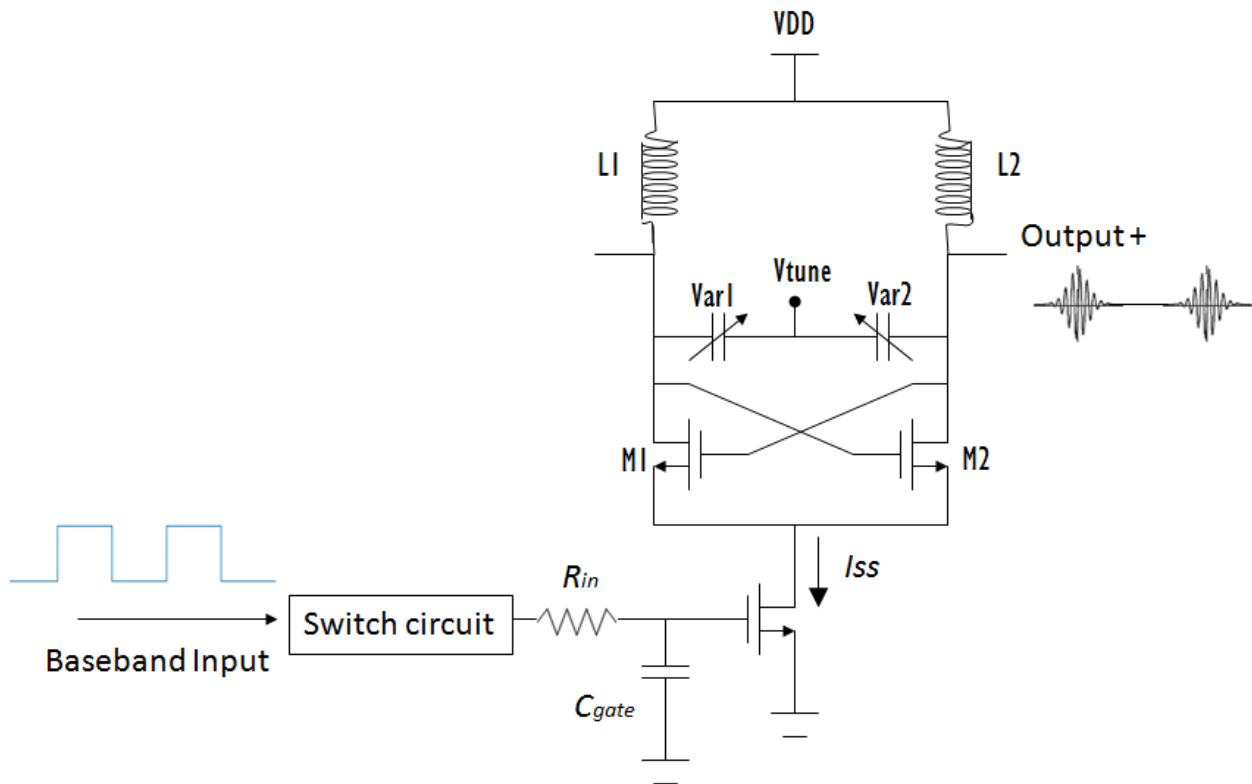
Fig. 2.3: LC VCO Circuit with a switch circuit and a tail current source.

The design of LC VCOs is very common in many communication circuits that require high carrier frequencies and low jitter generation. In most communications applications the oscillation is implemented in continuous mode, in which case the power dissipation and jitter are the most important attributes. Techniques for optimizing performance based on these criteria are well known [53]. However, the start-up characteristics of the VCO are generally not considered important in continuous-mode operation. For UWB pulsed-based transmitters used in a BAN

where the power consumption is also an important criterion, the pulse duration, pulse repetition frequency (PRF), and peak-to-peak voltage of the carrier can be the critical parameters. Fig. 2.4 illustrates these parameters translate into the frequency domain. Longer pulse duration, higher pulse repetition frequency, and higher peak-to-peak voltage all contribute to higher power consumption. To meet the FCC spectral mask, the pulse duration and peak-to-peak voltage must be carefully controlled for a given pulse repetition frequency. Thus, the startup transient, which provides a lower bound for the pulse duration, is of great interest to the designer, and often poses an important trade-off between low power dissipation and fast start-up time of the oscillation of the LC VCO.
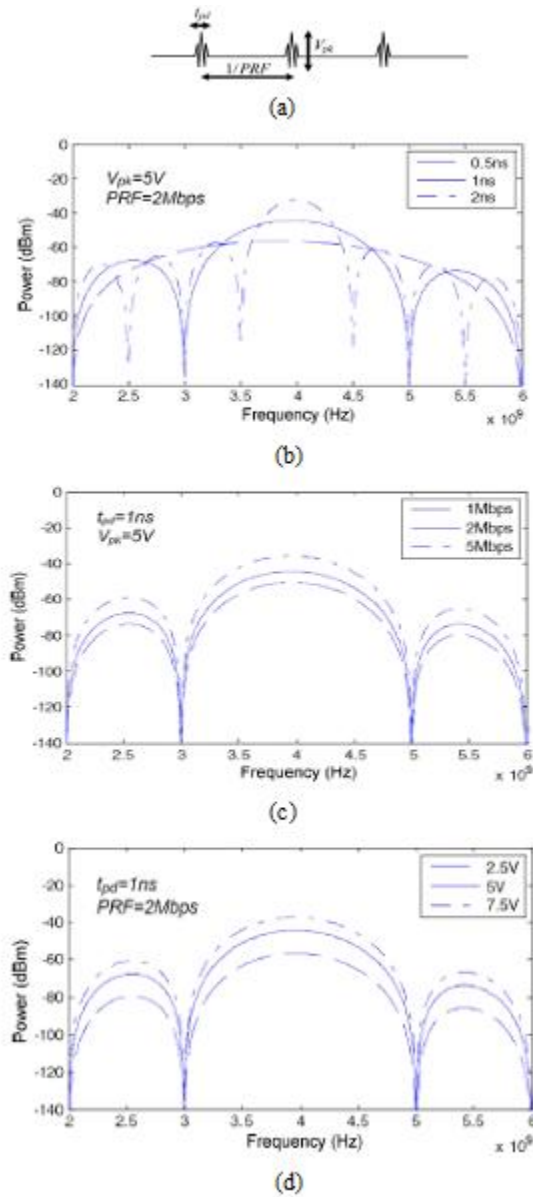
Fig. 2.4: Pulse duration, pulse repetition frequency, and peak-to-peak voltage in (a) time domain; (b) 3 different pulse width with the steady-state voltage held constant at 5V and the pulse repetition held constant at 2 Mbps in frequency domain; (c) 3 different pulse repetition rate with the pulse width held constant at 1ns and the steady-state voltage held constant at 5V; (d) 3 different steady-state voltage with the pulse width held constant at 1ns and the pulse repetition rate held constant at 2 Mbps.[55]

As illustrated in Fig. 2.3, a differential LC VCO uses a cross coupled transistor pair, a pair of varactors, on-chip differential inductors, and a tail current source transistor. For analysis consideration, the oscillator can be represented as negative resistor (-*R*) by a cross-coupled transistor pair and RLC parallel resonator, which R_T represents loss in the inductor as shown in Fig. 2.5.
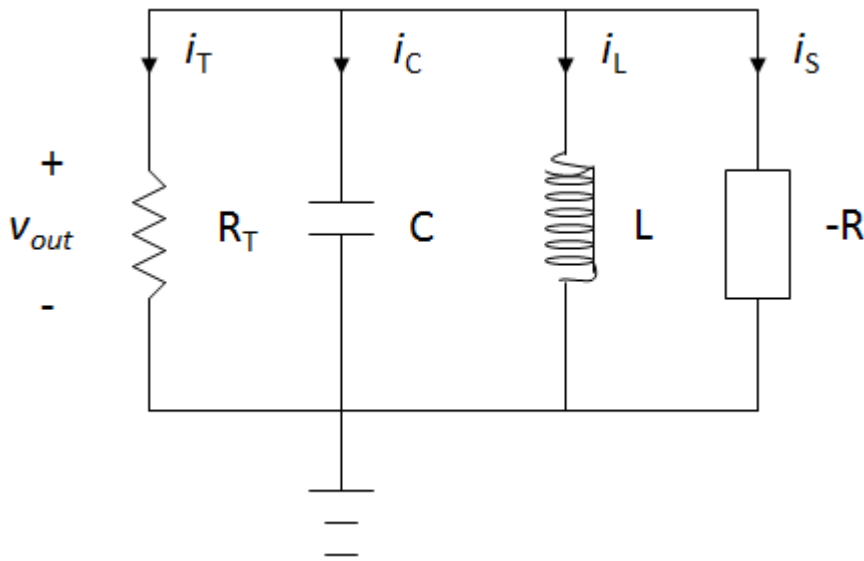
Fig. 2.5. Equivalent Circuit of the LC oscillator.

In the equivalent circuit of a differential LC oscillator shown in Fig. 2.5., the current i_s conducted by −*R* can be represented by an odd-order nonlinear polynomial function of v_{out}

$$i_s = av_{out} + bv_{out}^3 \qquad (2.1)$$

where *a* <0 and *b* >0 are the first- and third-order coefficients, respectively. From [10], v_{out} of LC oscillator can be solved as

$$v_{out}(t) \approx \frac{\sqrt[4]{\frac{I_{SS}}{\mu_n C_{ox} W/L}\left(\frac{2}{3} - \frac{2}{3A_{OL}}\right)} \cdot \cos(\omega_0 t + \phi)}{\sqrt{1 + [(\frac{\sqrt[4]{\frac{I_{SS}}{\mu_n C_{ox} W/L}\left(\frac{2}{3} - \frac{2}{3A_{OL}}\right)}}{v_{out}(0)})^2 - 1] \cdot \exp\left(-\frac{A_{OL}-1}{Q}\omega_0 t\right)}} \qquad (2.2)$$

where $A_{OL}=gmR$ is the open-loop gain, $Q=R(C/L)^{1/2}$ is quality factor of the tank, $v_{out}(0)$ and φ_0 are the initial values of v_{out} and phase, and ω_0 is the oscillator resonant frequency. The more detail and derivation of (2.2) will be discussed in the following section. Based on (2.2), in order to achieve fast oscillation start-up time, A_{OL} must be increased and/or the quality factor Q must be decreased. There have been several studies to improve fast transient time of oscillation. In [55], an Q of the LC VCO is deliberately reduced, by direct connection of the 50 Ω external termination to the VCO outputs. The result is a fast oscillation start-up time, but the power dissipation is rather high due to the 70 mA tail current in the VCO that is required to overcome the low Q of the tank circuit. One method to resolve this trade-off is reported in [10], where a pair of current sources is used to bias the VCO, and where a differential start-up delay between the current sources is applied in order to force an initial condition that allows faster start-up of the oscillation. This comes at the cost of a somewhat more complex circuit, including the differential delay circuitry, as well as capacitive degeneration used in the cross-coupled pair, which could cause some decrease of the Q of the VCO. We consider as an alternative a small asymmetry deliberately introduced into the LC VCO that can greatly reduce the oscillation start-up time without an increase in the circuit complexity.

2.3 Analysis of Oscillation Start-Up Time

A. Transient Behavior

As described in [55], the start-up of an LC VCO can be described as illustrated in Fig. 2.6. The various start-up phases include the setup period t_{setup}, the startup period t_{start}, the steady-state period t_{s-s}, and the decay period t_d. The length of t_{setup} is determined by how quickly the gate voltage of the transistor that realizes the tail current source as shown in Fig. 2.3. can exceed the threshold voltage when the switch turns on. In other words, the gate capacitance (C_{gate}) must be charged up exponentially following the $R_{in}C_{gate}$ time constant. Thus, we can write:

$$V_{th} = V_a(1 - \exp^{-\frac{t_{setup}}{R_{in}C_{gate}}})$$ (2.3)

where V_a is the applied gate voltage.

Solving for t_{setup}, we have:

$$t_{setup} = -R_{in}C_{gate}\ln(1 - \frac{V_{th}}{V_a})$$ (2.4)

This period can be decreased by minimizing the gate capacitance of the tail current transistor for a given tail current according to (2.4). As mentioned in the previous section, to speed up the startup period, there are two parameters have to be considered. For a conventional (symmetric) *LC* VCO, this startup period can be only reduced by decreasing the tank Q value and /or increasing the open loop-gain, A_{OL}.
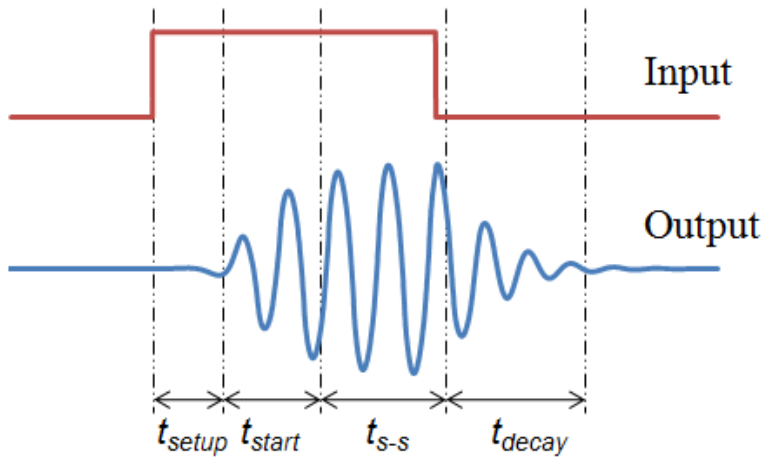
Fig. 2.6. The oscillator waveform.

B. *Transient Analysis of a Conventional LC VCO*

In order to understand the main aspects of the differential LC VCO analytical derivation, we refer to the simplified equivalent circuit in Fig. 2.7, originally presented in [56,57], where the active part of the circuit is represented by a nonlinear two-terminal element. This element exhibits a negative differential resistance within a restricted range of voltage, while the *RLC* parallel resonant circuit models the tank circuit.
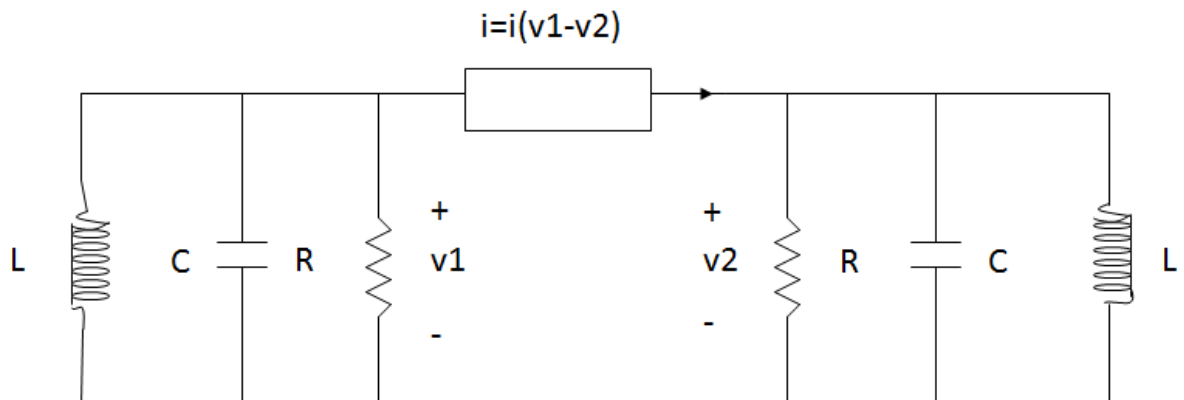
Fig. 2.7: Small signal equivalent circuit of differential LC VCO.

As derived in [12], the nodal equations corresponding to the Fig. 2.7 circuit are given by:

$$\frac{1}{L}\int v_1 \, dt + \frac{v_1}{R} + C\frac{dv_1}{dt} = -i(v_1 - v_2) \tag{2.5}$$

$$\frac{1}{L}\int v_2 \, dt + \frac{v_2}{R} + C\frac{dv_2}{dt} = i(v_1 - v_2) \tag{2.6}$$

The nonlinear function $i(v_1 - v_2)$ represents the current provided by the cross-coupled pair and is an odd function of $(v_1 - v_2)$ due to circuit symmetry. Taking the difference between the above two equations, the resulting differential equation can be written as:

$$\frac{d^2 v_d}{dt^2} + \frac{1}{C}\left[\frac{1}{R} + 2\frac{di}{dv_d}\right]\cdot\frac{dv_d}{dt} + \frac{1}{LC}v_d = 0 \tag{2.7}$$

where $v_d \equiv v_1 - v_2$.

As mentioned earlier, the non linear function, $i(v_1 - v_2)$ can be approximated as the following form:

$$i(v_1 - v_2) \equiv av + bv^3 \tag{2.1}$$

where $a = -gm$ and $b = (1/8)\cdot I_{SS}/(I_{SS}/\mu_n C_{OX}(W/L))^{\frac{3}{2}}$ from the Taylor approximation. After inserting (2.8) into (2.7) with algebraic manipulation, the resulting equation can be written as:

$$\frac{d^2 v_d}{dt^2} + \varepsilon\omega_0[v_d^2 - 1]\cdot\frac{dv_d}{dt} + \omega_0^2 v_d = 0 \tag{2.9}$$

where $\varepsilon = \left(g_m - \frac{1}{R}\right)\sqrt{\frac{L}{C}} = \frac{A_{OL} - 1}{Q}$ is a damping factor and $\omega_0 = \frac{1}{\sqrt{LC}}$ is the natural angular frequency of the oscillator. Solving for the exact solution of (2.9), which is the well-known "van

der Pol" equation, is quite complicated. However, for small ε this equation can be approximated by the averaging method [77]. Since for this high frequency LC oscillator ε stays typically smaller than one, an approximate solution of (2.9) can be solved as:

$$v_d(t) \approx \frac{2V_{d0} \cdot \cos(\omega_0 t + \phi)}{\sqrt{1 + \left[\left(\dfrac{2V_{d0}}{v_d(0)}\right)^2 - 1\right] \cdot \exp(-\varepsilon\omega_0 t)}} \qquad (2.10)$$

where $V_{d0} = 2\sqrt{\dfrac{I_{SS}}{\mu_n C_{ox} W/L}\left(\dfrac{2}{3} - \dfrac{2}{3g_m R}\right)}$, and $v_d(0)$ is the initial condition [10]. By replacing V_{d0}

with $\sqrt{\dfrac{I_{SS}}{\mu_n C_{ox} W/L}\left(\dfrac{2}{3} - \dfrac{2}{3g_m R}\right)}$, gmR with A_{OL}, and ε with $(A_{OL}-1)/Q$, (2.10) turns out to be (2.2).

As mentioned earlier, based on (2.10) A_{OL} must be increased and/or Q must be decreased in order to speed up the start up period for LC VCO. It is the setting of the initial condition and decreasing Q of (2.10) that is employed in [10] to minimize the oscillation startup period.

2.4 ANALYSIS OF ASYMMETRIC LC VCO

A. Theory

We consider the behavior of the LC VCO shown in Fig. 2.8 in which a small mismatch ΔC between the two varactor capacitors is introduced, keeping all other components perfectly matched. The resulting node equations are:

$$\frac{1}{L}\int v_1 dt + \frac{v_1}{R} + \left(C + \frac{\Delta C}{2}\right)\frac{dv_1}{dt} = -i(v_1 - v_2) \qquad (2.11)$$

$$\frac{1}{L}\int v_2\,dt + \frac{v_2}{R} + \left(C - \frac{\Delta C}{2}\right)\frac{dv_2}{dt} = i(v_1 - v_2) \qquad (2.12)$$
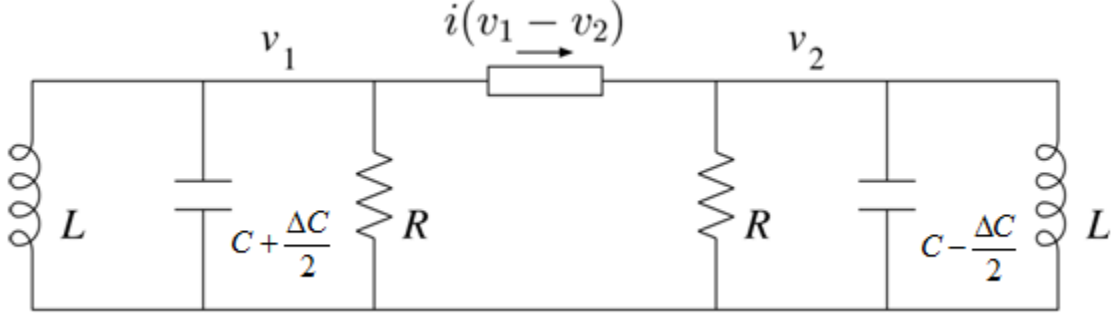
Fig. 2.8: Small signal equivalent circuit of differential asymmetric LC VCO.

We now consider the difference and the sum of the above two equations, with $v_d \equiv v_1 - v_2$ as before and $v_c \equiv \frac{1}{2}(v_1 + v_2)$:

$$\frac{1}{L}\int v_d\,dt + \frac{v_d}{R} + i(v_d) + C\frac{dv_d}{dt} = -\Delta C\frac{dv_c}{dt} \qquad (2.13)$$

$$\frac{1}{L}\int v_c\,dt + \frac{v_c}{R} + C\frac{dv_c}{dt} = -\frac{\Delta C}{4}\frac{dv_d}{dt} \qquad (2.14)$$

Equation (2.13) is identical to the KCL equation that describes the symmetric VCO model shown in Fig. 2.7, but with the derivative of the common-mode voltage acting as a forcing function; this is illustrated in Fig. 2.9(a). In a similar manner, (2.14) can be interpreted as the KCL equation corresponding to the passive tank circuit portion of the VCO, with the derivative of the differential-mode voltage acting as a forcing function; this is illustrated in Fig. 2.9(b).
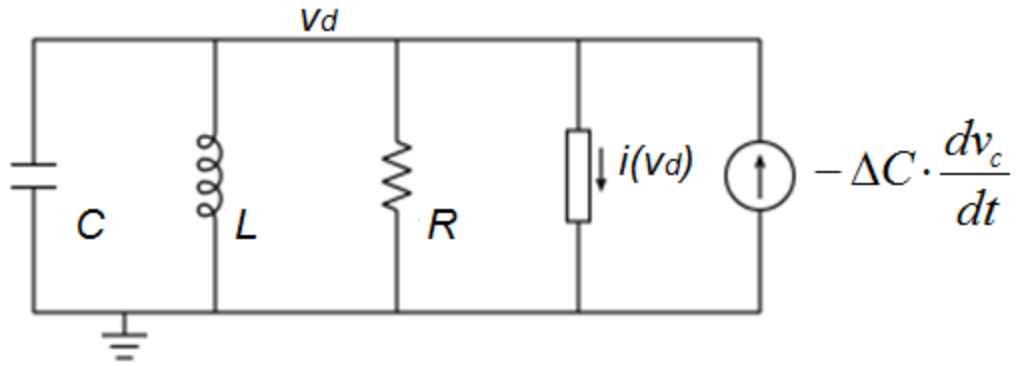
(a)
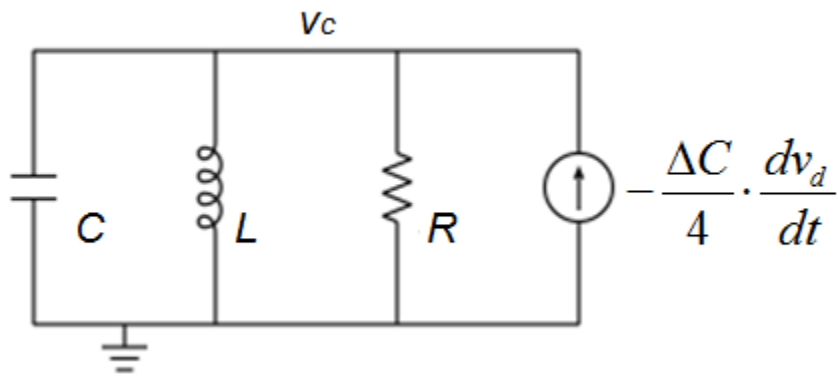
(b)
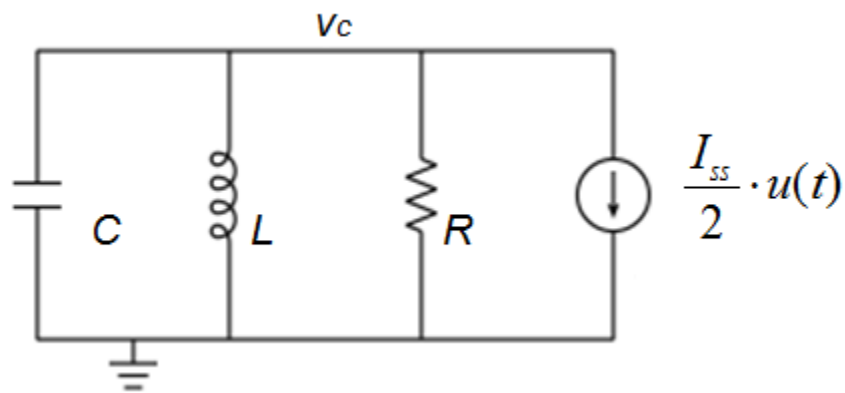
(c)

Fig 2.9. (a) Equivalent circuit for VCO differential-mode dynamics; (b) equivalent circuit for VCO common-mode dynamics; (c) equivalent circuit for VCO common-mode dynamics with input step current applied.

B. Start-up Analysis

We now consider the start-up of the Fig. 2.3 LC VCO where the tail current source is applied as a step function from 0 to I_{SS} at $t=0$. In this case the differential voltage v_d does not have an appreciable initial condition, and thus (2.10) does not give a good prediction of start-up dynamics; they are instead determined by the noise in the circuit components. As a result, there is an appreciable delay before v_d (as well as its derivative) changes from 0. For this reason, the dynamics of the common-mode voltage v_c are determined primarily by the step change of the tail current source rather than by the dv_d/dt term. Thus, we will consider the Fig. 2.9(c) common-mode circuit in place of Fig. 2.9(b) where I_{SS} is the steady-state value of the tail current source. The solution to this circuit is easily found to be:

$$v_c(t) = \frac{2I_{SS}}{C\beta} \cdot e^{-\alpha t} \cdot \sin(\beta t) \cdot u(t) \tag{2.15}$$

where $\beta \equiv \sqrt{\dfrac{1}{LC} - \dfrac{4}{(CR)^2}}$ and $\alpha = \dfrac{1}{2CR}$.

It is the derivative of the expression in (2.15), which exhibits a step at $t = 0$, and scaled by the mismatch ΔC, that is the effective driving force to the differential circuit as shown in Fig. 2.9(a). We will show simulation results for the circuit that verify the derivations and assumptions made in the previous section. All transient simulations include noise sources to accurately predict the oscillation start-up times of the VCO.
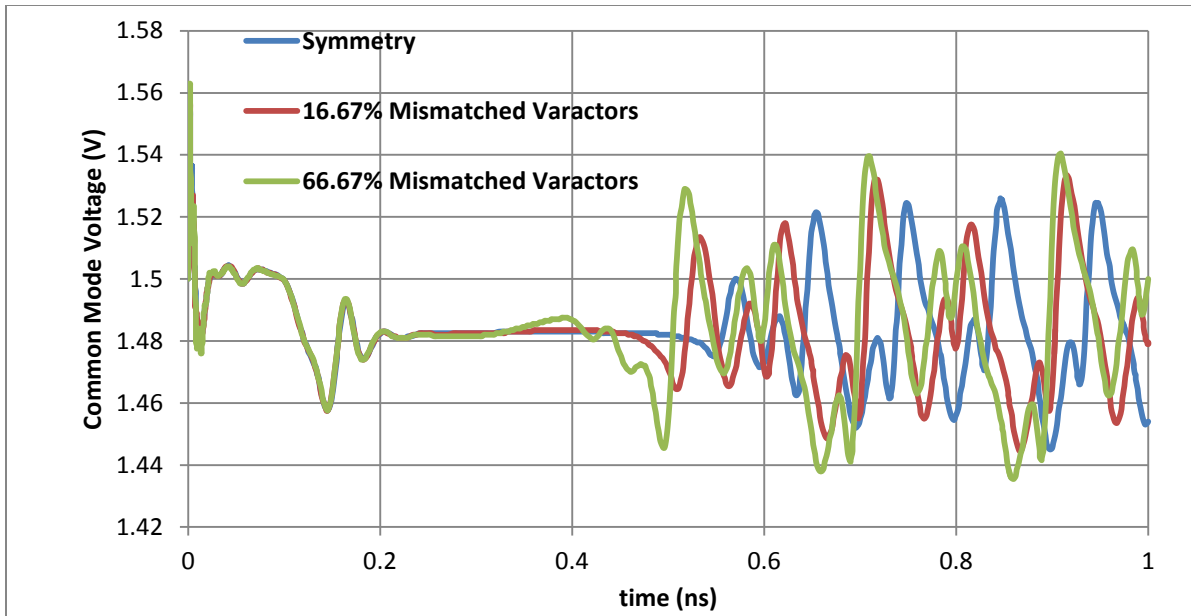
(a)
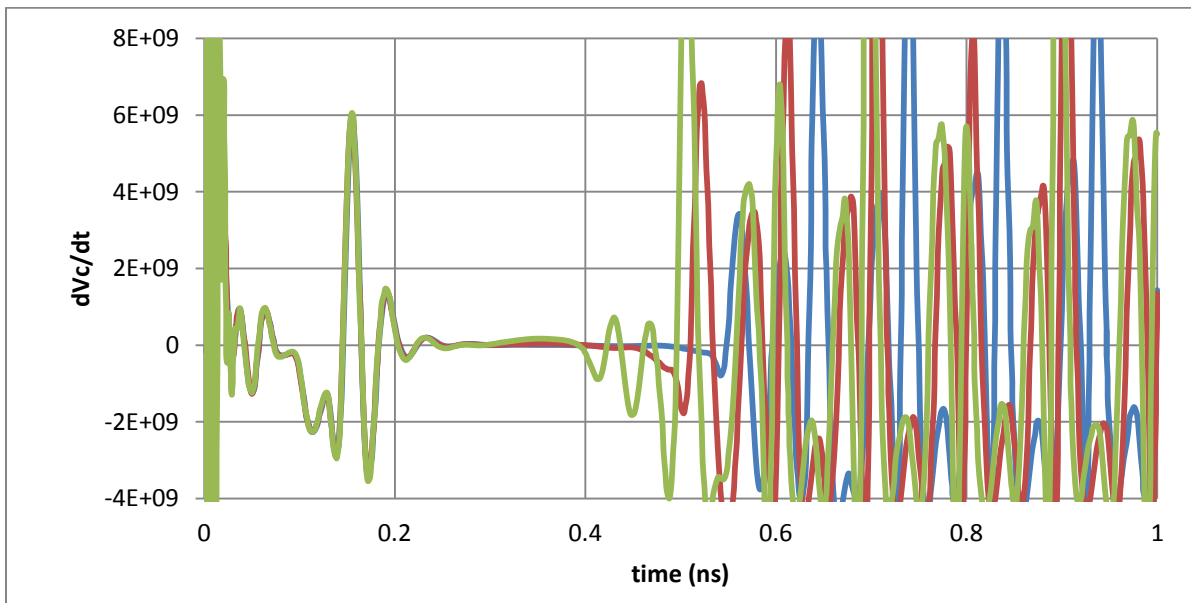
(b)

Fig. 2.10: Simulation results for three different values of capacitor mismatch; (a) common-mode start-up transient of VCO; (b) its derivative.

Fig. 2.10(a) shows the start-up transient of the VCO output voltage's common-mode component for different mismatch values of the varactor capacitor; Fig 2.10(b) shows the time derivative of this waveform. (The initial transients near $t = 0$ are not relevant for this analysis since the cross-coupled transistors do not turn on until $t \approx 0.15$ ns. It is at this time where (2.15) holds.) It can be observed that the amount of mismatch has little effect on the start-up transient of the common-mode output voltage.

Fig. 2.11(a) shows the start-up transient of the VCO output voltage's differential-mode component, also for different mismatch values of the varactor capacitor. In this case it can be observed that a larger capacitor mismatch – corresponding to a larger forcing function amplitude on the right-hand side of (2.13) – results in a faster start-up time. A similar effect can be found in implementing a mismatch in the (W/L) of the cross-coupled transistors, as shown in Fig. 2.11(b).
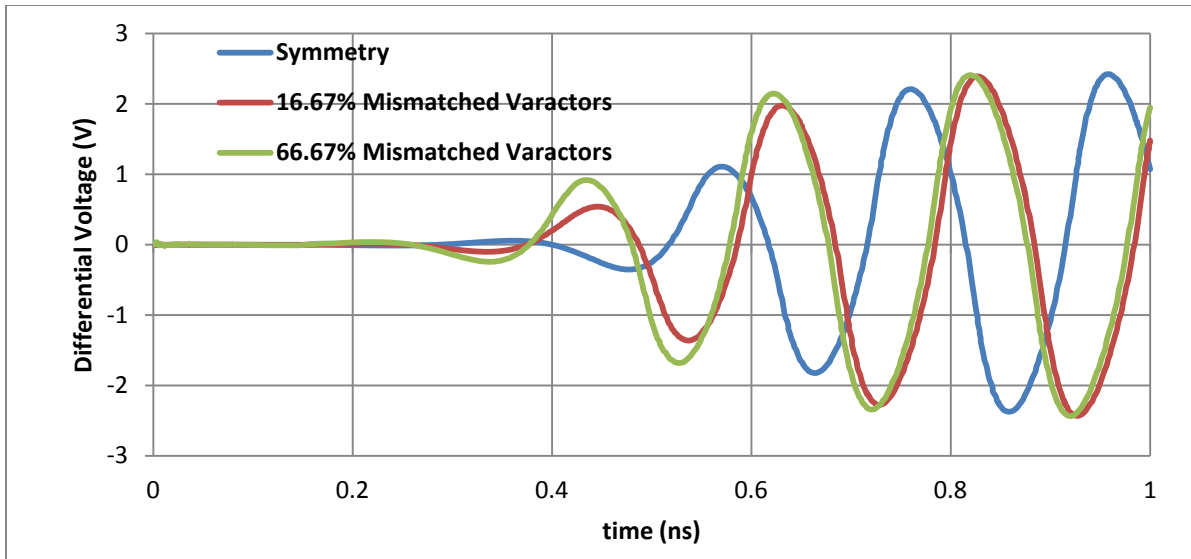
(a)
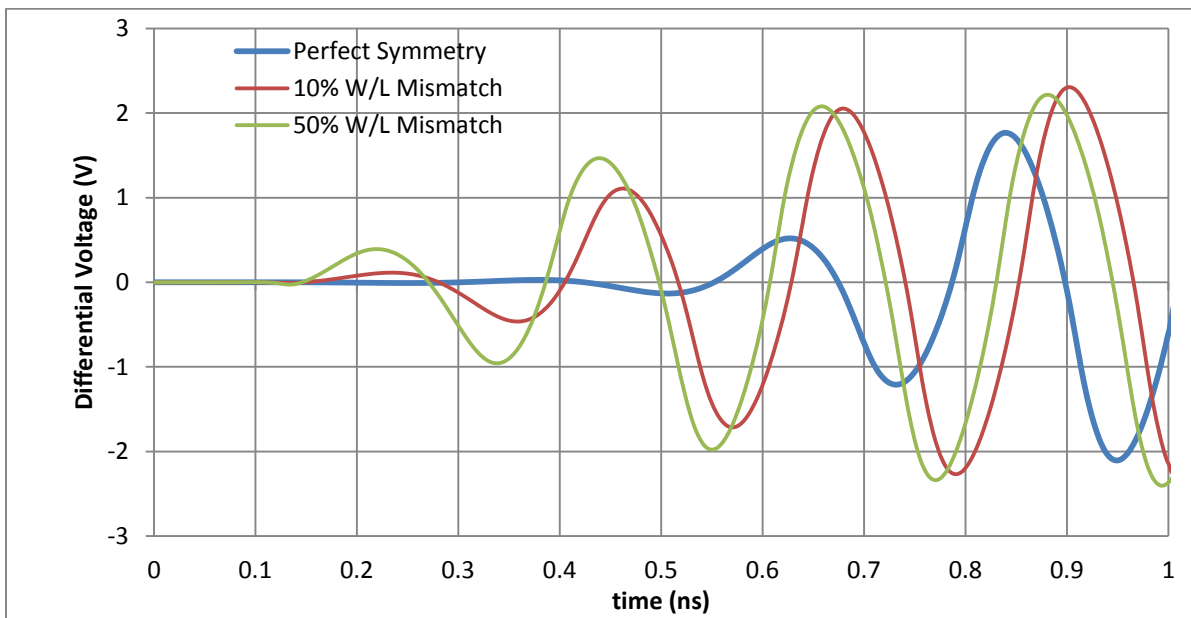
(b)

Fig. 2.11: Simulation results of differential start-up transient of VCO (a) for three different

values of capacitor mismatch; (b) for three different values of (W/L) mismatch.

2.5 Proposed Transmitter Architecture

The schematic of a UWB transmitter, consisting of a mismatched LC VCO and a buffer used to drive an external 50 Ω termination, is shown in Fig. 2.12.
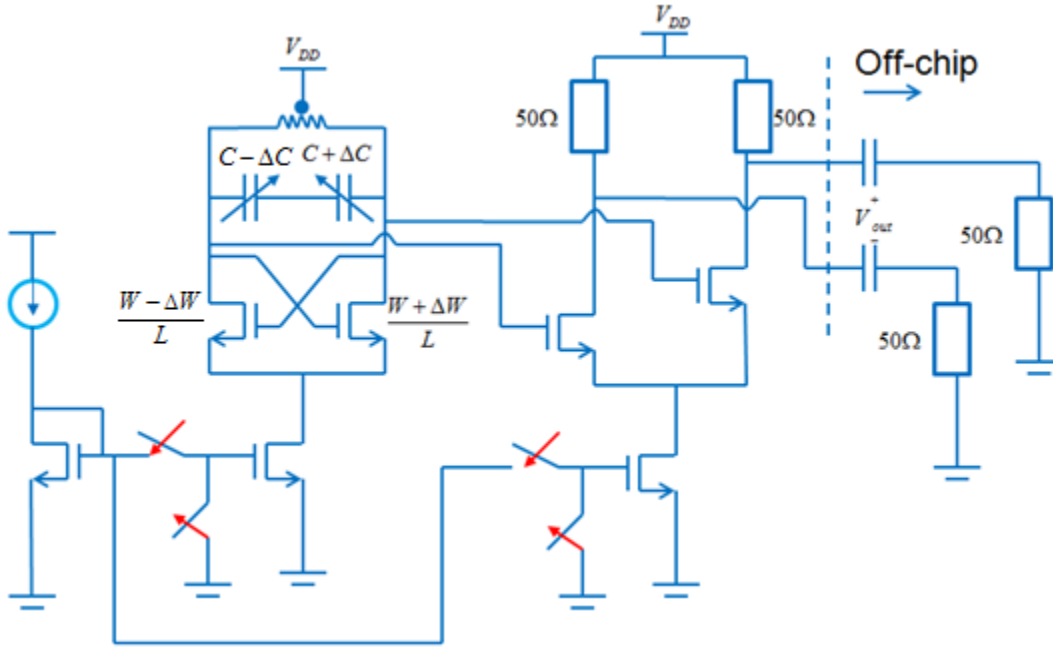
Fig. 2.12: Schematic of Proposed UWB Transmitter circuit.

A center-tap on-chip inductor is implemented and the Q value of the LC tank circuit is 10. In the symmetric oscillator prototype, the nominal values of the varactor capacitors are 241 fF and the nominal W/L values of the differential pair transistors are 38 μm/0.18 μm. To enforce more asymmetric capacitors in LC VCO, larger W transistor and a larger varactor were implemented on the same side to enhance the fast start-up time of LC oscillator. The tail current, *Iss* is designed to conduct 3 mA. Both the oscillator and the driver are switched as shown in Fig. 2.12, assuming an on/off keying (OOK) modulation scheme is used. In order to attain the very low energy data rate, NMOS switches are implemented in series with the gates of the two tail current

transistors while PMOS switches are implemented in series with a ground node as well as across the LC tank of LC VCO. All switches turn on and off simultaneously. The switches are controlled by an internal pulse generator, which consists of three tunable cmos delay cells and an AND gate as shown in Fig. 2.13.

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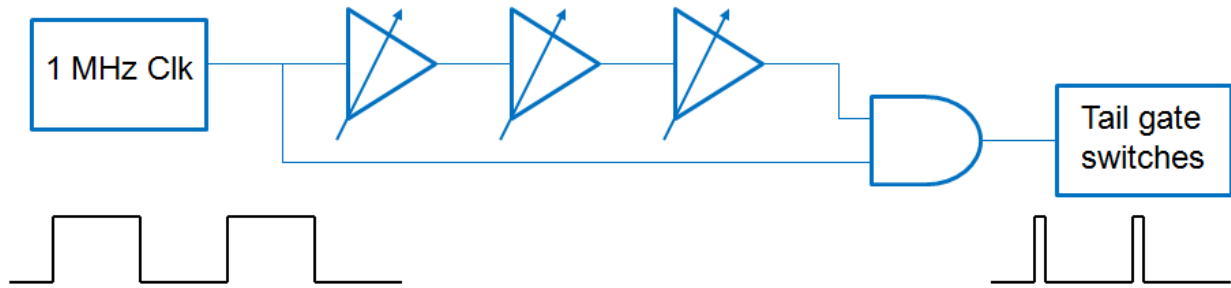
(a)
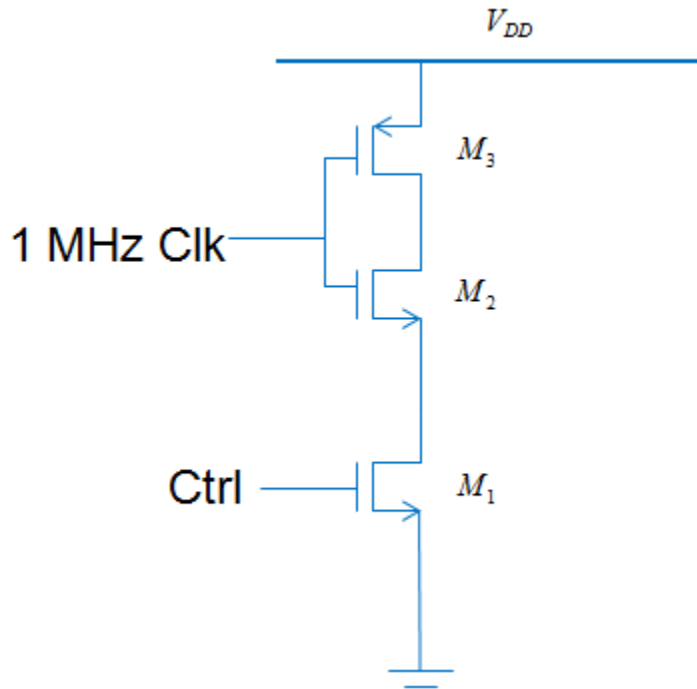
(b)

Fig. 2.13: (a) Internal pulse generator; (b) transistor schematic of delay cell.

2.6 Measurement and Results

The UWB transmitter has been fabricated in the SBC 0.18 μm BiCMOS process (only CMOS is used) and occupies an area of 900 μm x 1400 μm (including pads). The chip was mounted directly onto the printed circuit board and tested. The die photo and PCB are shown in Fig. 2.14(a) and (b), respectively. The implemented UWB transmitter is designed for a 1.5 V power supply. The output of high frequency 4.2 GHz pulse is monitored by an Agilent Infinium DSA91204A Digital signal Analyzer. Pulse train with a 1 Mbps repetition rate is applied to the switches of the transmitter as illustrated in Fig. 2.12.
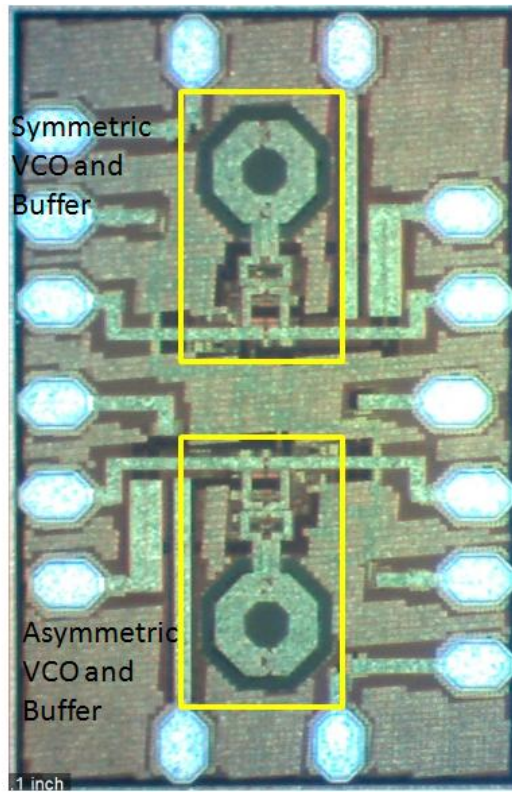
(a)
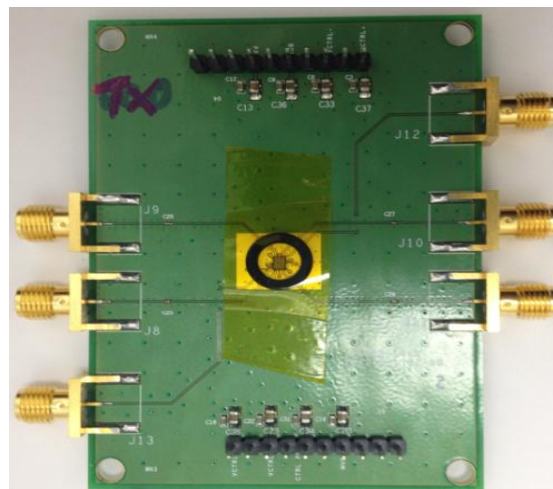
(b)

Fig. 2.14. (a) A chip photograph of symmetric and asymmetric LC-VCOs and Buffers (b) PCB.

The output carrier pulse width can be adjusted from 3.5 ns to 1.2 ns, which corresponds to a signal bandwidth of 500 MHz to 2 GHz. The measured carrier frequency was 4.2 GHz for both the symmetric and asymmetric UWB transmitters. As illustrated in Fig. 2.15, the asymmetric transmitter displays about 300 ps faster start-up time, which is defined as the time to reach 80% of steady-state value. The current consumption for each VCO is 3.0 mA, which corresponds to 31.5 pJ per bit for a 3.5ns output pulse width. Table II summarizes the performance of the implemented UWB transmitter.
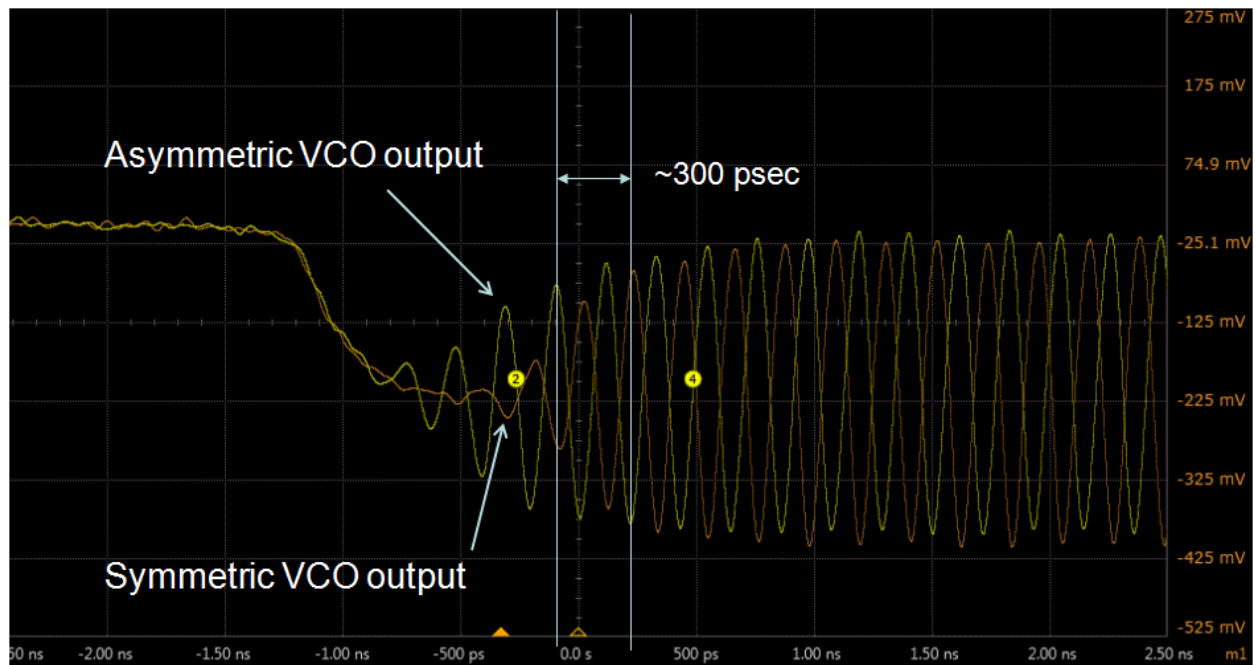
Fig. 2.15. Measured asymmetric and symmetric VCO outputs.

Table 2.1 Summary of the measured UWB transmitter

Supply Voltage	1.5 V
Modulation	OOK
Data Rate	1 Mbps
Die area (include pads)	900 μm x 1400 μm
Current consumption	6 mA
Center Frequency	4.2 GHz
Energy per bit	31.5 pJ/bit

2.7 Summary

The design, realization, and results of a fast starting low power UWB transmitter have been presented. The asymmetric LC-VCO can generate 300 ps faster startup pulse compared to the symmetric VCO without adding extra circuitry. The pulse data rate is 1 Mbps and its oscillation frequency is 4.2 GHz. The energy dissipation per pulse is 31.5 pJ per bit.

Chapter 3. Track and detection of Super-Regenerative Receiver

3.1 Introduction

The receiver system architecture for a pulsed-based UWB can be either coherent or non-coherent. Coherent receivers are usually based on a rake receiver, which recovers pulse energy by correlating the input signal with an internally generated template waveform [77-79]. A typical coherent receiver architecture is shown in Fig. 3.1(a). Since this receiver has correlator elements that act as an analog pulse-matched filter, it shows better performance than a non-coherent receiver. However, it requires many power-consuming blocks such as a high-gain LNA, at least one mixer, and a template generator. On the other hand, a non-coherent receiver is based on collecting the energy contained in the entire channel. In this receiver architecture, the input signal is squared and integrated to recover all the received useful energy as illustrated in Fig. 3.1(b) [80-82]. However, the major drawbacks for this type of receiver are the lack of timing information when energy is collected and high RF gain requirement in front of the squaring function block. Fortunately, super-regenerative receiver architecture resolves the tradeoff between the coherent and non-coherent techniques.
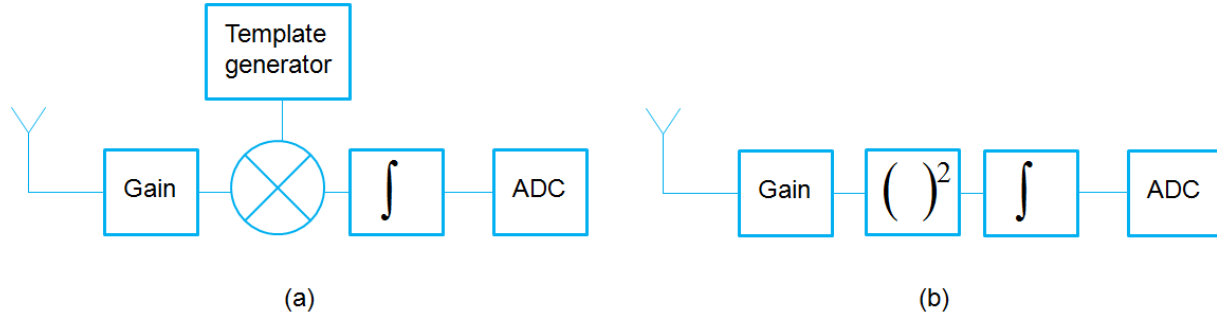
Fig.3.1: UWB architectures (a) Coherent; (b) Non-coherent. [60]

3.2 Super-Regenerative Principle

One of the common techniques used in the design of IR-UWB receivers makes use of the super-regenerative principle, which achieves relatively low complexity and low power consumption. The super-regenerative (SR) principle is a circuit technique that was introduced by Edwin Armstrong in 1912 and was widely used in radio receivers between 1915 and World War II. An embodiment of such a receiver is shown in Fig. 3.2. It detects reception of short carrier pulses with very low power dissipation and is well-suited for demodulation of Impulse Radio-Ultra Wide Band (IR-UWB) signals [58], explained as follows.
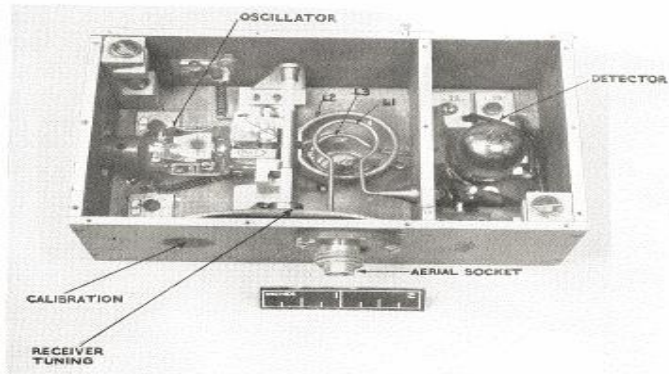
Fig. 3.2. First generation of SRR, German air interception. [58]

A. Theory

The super-regenerative principle can be explained by studying the parallel resonant tank, which is the essential part of a resonant oscillator as shown in Fig. 3.3.
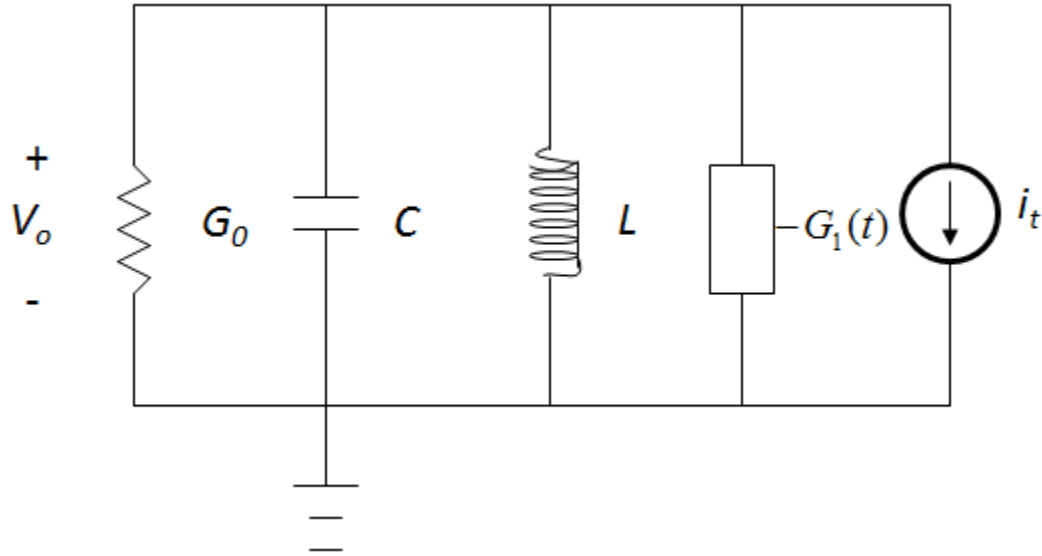
Fig. 3.3. Parallel resonant tank circuit with a current source.

The resonant tank consists of an inductor L, a capacitor C, a positive shunt conductance G_0, which represents the parasitic loss of the tank circuit, and a time-varying negative shunt conductance $-G_1(t,)$ which is typically realized by a cross-coupled transistor pair whose tail current varies with time. These active devices compensate the loss in the tank and the overall conductance $(G_0\text{-}G_1)$ can be either positive or negative depending on the amount of compensation provided by the active devices. A sinusoidal current source $i(t) = A \sin \omega t$ is applied to the Fig. 3.2 circuit at $t=0$. To determine its response, we write the KCL equation as:

$$C\frac{dV_0}{dt} + (G_0 - G_1)V_0 + \frac{1}{L}\int V_0 dt = A\sin \omega t \qquad (3.1)$$

The solution to this differential equation is:

$$V_0(t) = e^{-\alpha t}(k_1 e^{j\omega_d t} + k_2 e^{-j\omega_d t}) + \frac{A\sin(\omega t)}{\sqrt{(G_0 - G_1)^2 + (\omega C - 1/\omega L)^2}}$$ (3.2)

Where

$$\alpha = (G_0 - G_1)/2C$$

$$k_1 = \frac{V_0(0)}{2} + \frac{\alpha V_0(0)}{2j\omega_d} + \frac{1}{2j\omega_d}\frac{dV_0(0)}{dt}$$

$$k_2 = \frac{V_0(0)}{2} - \frac{\alpha V_0(0)}{2j\omega_d} - \frac{1}{2j\omega_d}\frac{dV_0(0)}{dt}$$

$$\omega_d = \sqrt{(1/LC) - [(G_0 - G_1)/2C]^2} = \sqrt{(\omega_0^2 - \alpha^2)}$$

The first term in (3.2) is the homogeneous response of a transient oscillation at frequency ω_d with the damping factor α while the second term represents the forced response to the injected signal, which is the steady-state oscillation. If G_0-G_1 > 0, then the homogeneous response dies out due to the fact that the active devices do not provide enough energy to compensate for the loss in the tank, and only the second term remains as the steady state. Super regeneration occurs when the overall conductance, G_0-G_1, is negative. In this case, the active devices supply sufficient energy to build up a free oscillation from an initial voltage that increases in magnitude, thereby achieving a gain that increases exponentially. The overall conductance can be controlled by varying the negative conductance of the cross-coupled pair, which is -2/g_m, since the positive conductance always presents as loss in the tank. This is done by controlling the current bias, known as the "quench signal." If an incoming input RF carrier pulse is present at the output of the oscillator core circuit as shown in Fig. 3.4(a) during the brief turn-on period of the quench signal, the VCO will be forced to start immediately and attain higher amplitude than the case when there is no input signal. The VCO output signal is then applied to an envelope detector,

whose peak value is sampled and compared with a reference voltage to make a decision on the

presence of pulse. The principle of the operation is shown in Fig. 3.4(b).
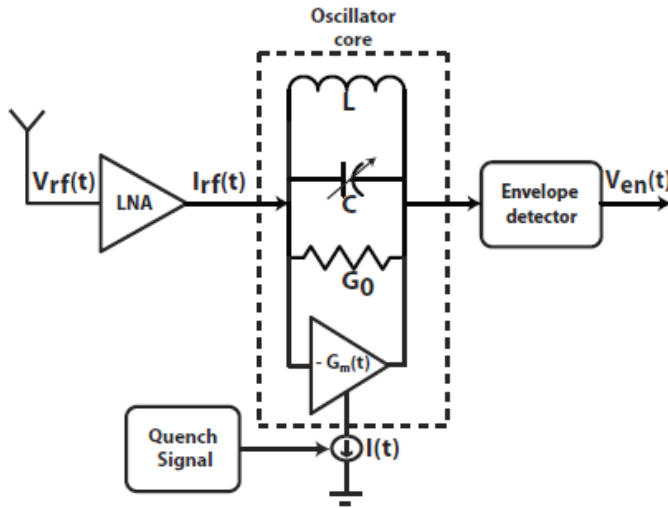
(a)
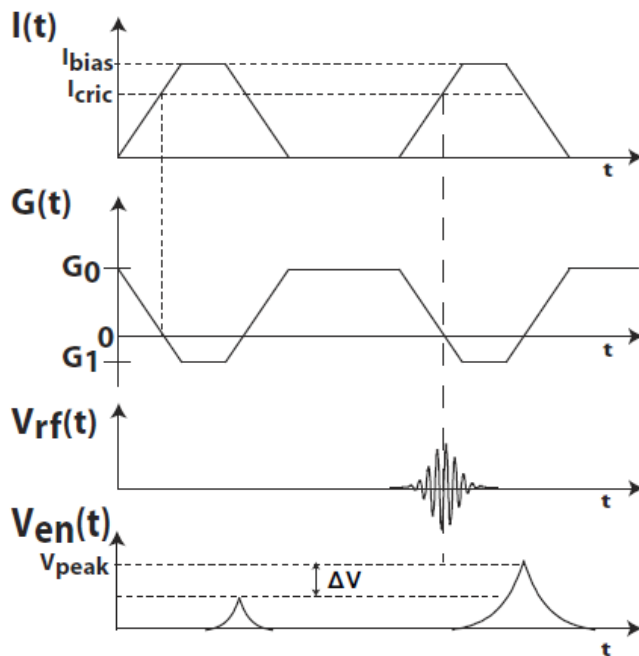
(b)

Fig. 3.4: Super-Regenerative Principle (a) schematics (b) Voltage, Current, Conductance

waveforms respect to time. [63]

Based on the super-regenerative principle stated above, the On-Off Keying (OOK) modulation scheme often leads itself well to an IR-UWB communication system. Basically, the presence of an incoming RF input carrier indicates a "1" while the absence of the RF input carrier indicates a "0".

The proper operation of this receiver is predicated on having the quench signal $I(t)$, which is generated on-chip, synchronized with the applied RF carrier signal. However, when RF carrier signal is not align with the quench signal as shown in Fig. 3.5(a), the RF carrier signal is lost and error occurs. Thus, the quench signal somehow must find the RF carrier signal and stay locked with the RF carrier signal as shown in Fig. 3.5(b).

RF Signal

Quench Signal

(a)

RF Signal

Quench Signal

(b)
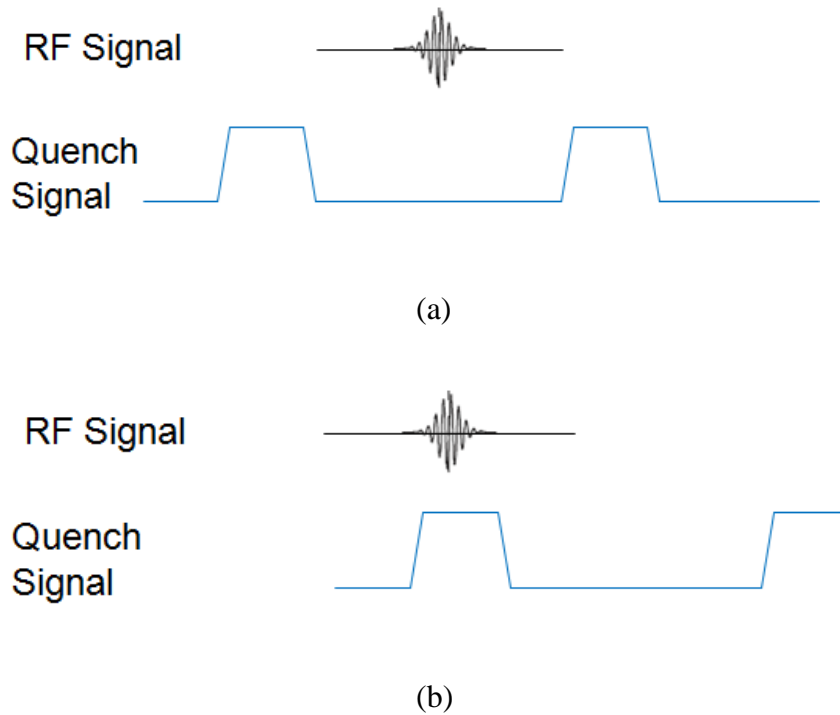
Fig. 3.5: quench signal and RF signal (a) not synchronized; (b) synchronized.

Some recent attempts at such synchronization were reported in [59-60], where a sinusoidal quench signal was used. However, it has been shown that a sinusoidal quench signal

shows poor selectivity to detect an incoming carrier pulse [61]. On the other hand, a trapezoidal quench signal that can be realized by implementing digital gates provides required selectivity and gain [62]. In addition, other studies assume synchronization between incoming RF carrier signal and external quench signal is already attained without any explanation or using sinusoidal quench with PLL [63-67]. In the work described here, a trapezoidal quench pulse signal is chosen to attain high selectivity and gain. Based on [62], the optimum value of the rising time and fall time is 5 ns and the duration of the pulse is 25 ns.

In this work, we have designed a low-power 4 Mb/s super-regenerative receiver in a 0.18 µm BiCMOS process (but we only utilize CMOS in this work) that tracks the incoming signal carrier pulse and synchronizes it with a pulse quench signal. The energy consumption for this receiver is 0.12 nJ/bit, which demonstrates the lowest energy consumption reported so far for an IR-UWB receiver system.

3.3 IR-UWB Receiver Architecture

A. Proposed Receiver Architecture

The main building blocks of a super-regenerative receiver are a low-noise amplifier (LNA), which contributes the initial gain as well as isolation that prevents the reradiation of the signal to the antenna, an oscillator whose bias current is controlled by the quench signal, an envelope detector, a baseband amplifier, a decision circuit, and a track and detection circuit, which consists of a delay-locked loop, a selector circuit, digital logic, and a counter as shown in Fig. 3.6.
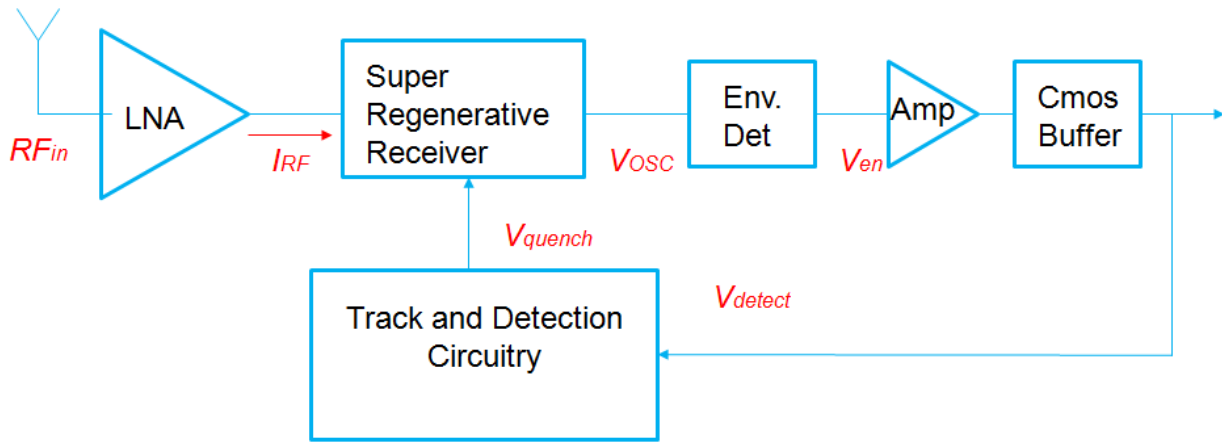
Fig. 3.6: Block diagram of proposed Super-Regenerative Receiver.

There were two main challenges in the design of this receiver: First, since the RF input pulse is very short (approx. 10 cycles of the 4 GHz carrier signal), the VCO must start up very quickly once the quench signal has been activated. Second, the quench signal, generated internally on-chip, must synchronize with the input RF signal within a reasonable amount of time.

The first challenge was addressed in Chapter 2, where it was shown that a mismatch deliberately embedded into an LC-oscillator can significantly speed up its startup time. In this section, we will explain in more detail about how we design such mismatch in the transistor level to enhance its start-up time. To resolve the second challenge, a delay-locked loop (DLL) and detection circuit have been designed to control the quench signal so that it can be adjusted relative to the input RF pulse, with very low power dissipation. The architecture of this synchronization circuitry will be discussed in the next Section.
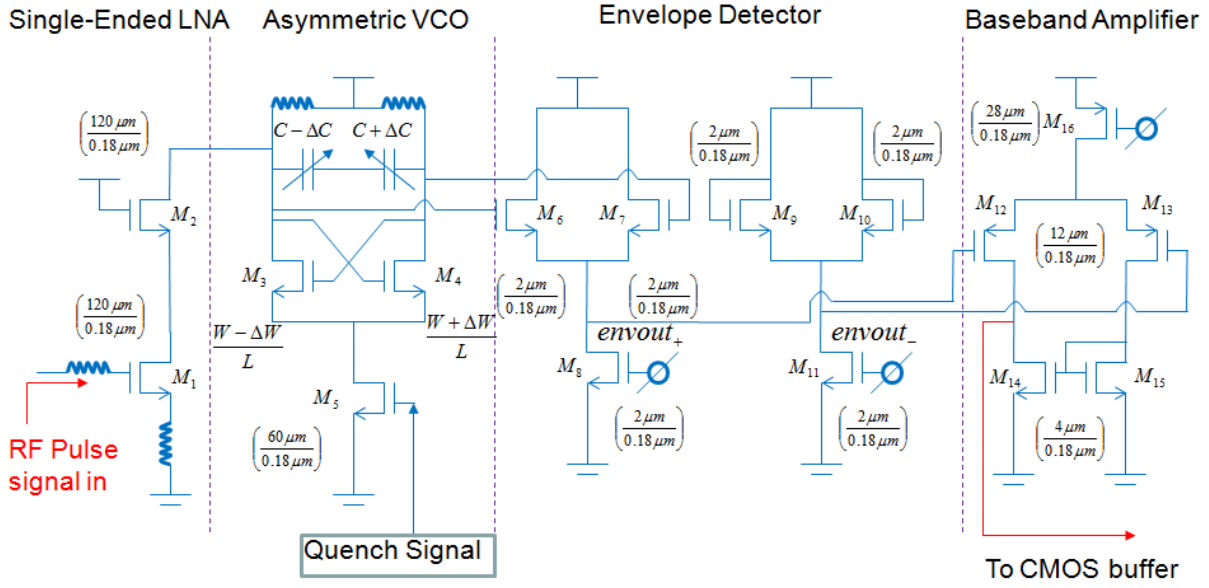
Fig. 3.7: Front-end transistor-level schematic of the proposed super-regenerative receiver.

1) Single-Ended Low Noise/ Isolation Amplifier

A cascode amplifier topology is used to realize the single-ended low-noise amplifier (LNA) as shown in Fig. 3.7. The LNA and the oscillator use the same resonant tank elements; this allows reduction of the chip area due to the lack of extra on-chip inductor. For 50Ω input matching, an inductor-degenerated LNA configuration is employed.

2) Core Oscillator

An LC VCO used as the core oscillator is shown in Fig. 3.7. The VCO is designed to be asymmetric by mismatches both of the cross-coupled transistor pair M3 & M4 and the varactor capacitors so that the start-up time of the oscillator will be reduced. The nominal W/L values of the cross-coupled transistor pair is implanted to be 108 μm/0.18 μm with 15% mismatch while that of the varactors is to be 650 fF with 10% mismatch. The mismatch will result in being more

sensitive to the incoming RF signal with a given short duration of quench signal compared to a perfectly matched LC VCO as shown in Fig. 3.8.
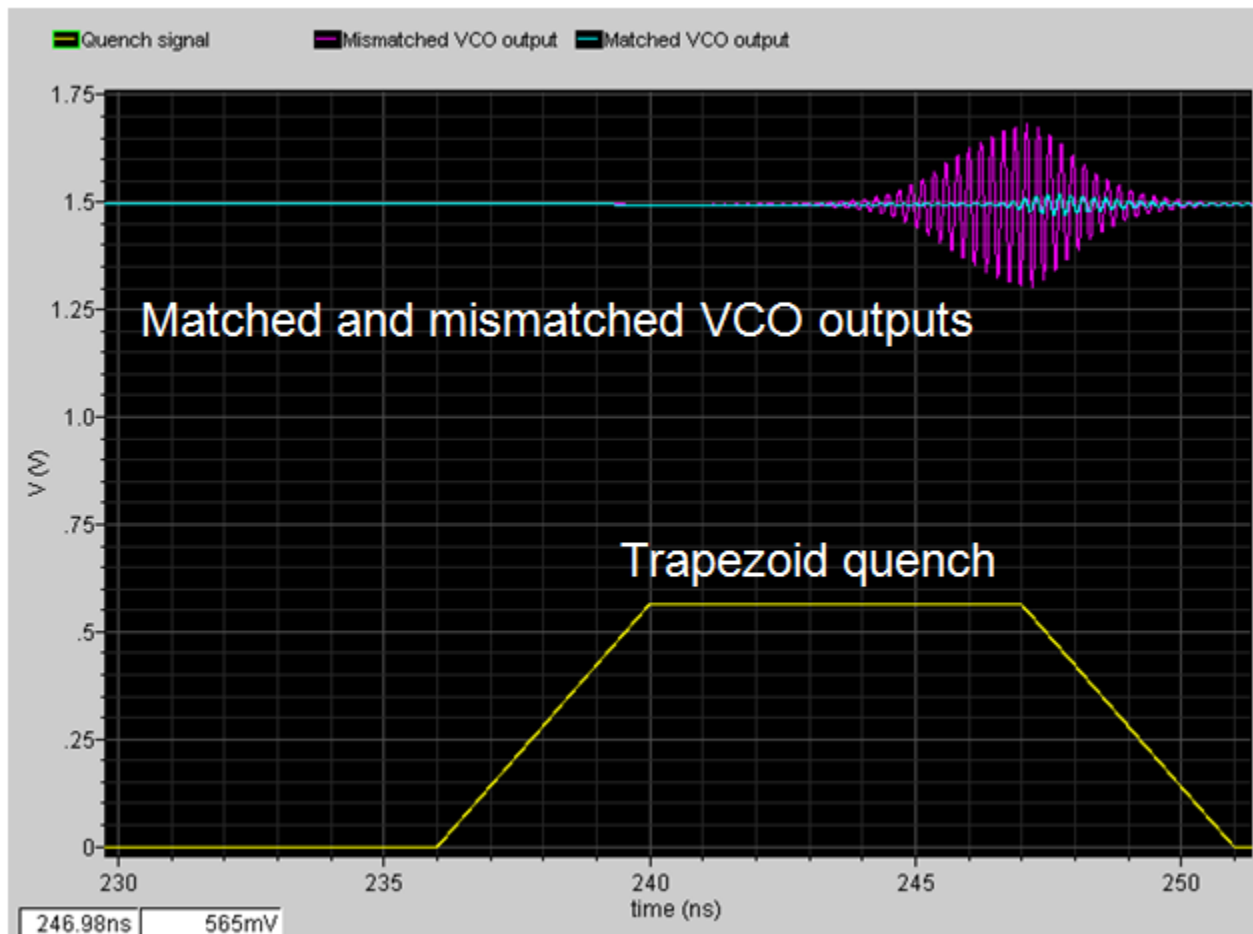
Fig. 3.8: Simulation results of matched and mismatched LC VCO outputs with an incoming RF signal.

In order to achieve high selectivity, the quench signal must be generated as a trapezoid shape. Since the slope of trapezoid shape depends on the size of the transistors, large size of length of CMOS drive buffer whose W/L ratio for pmos and nmos designed to be (16μm/1μm) and (8μm/1μm), respectively, has been implemented to charge the gate capacitor of the tail current source in 5 ns [62]. As illustrated in Fig. 3.9, since the duration of the trapezoid quench

is very short (~15 ns), the effect of the thermal noise to startup the VCO is minimized. Thus, only the amplified RF input signal from the LNA has enough energy to oscillate within the short transient time. The frequency of the oscillator circuitry is tuned to achieve 4.5 GHz.
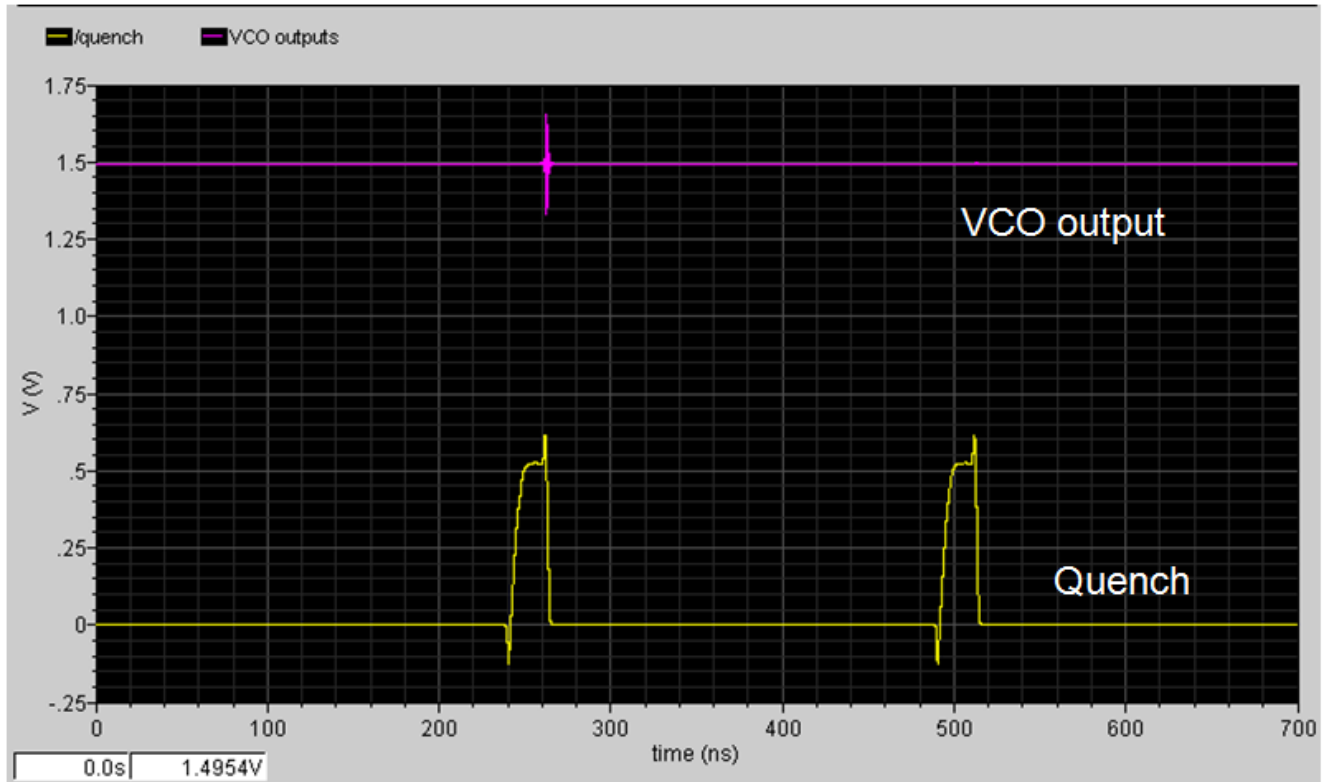
Fig. 3.9: Simulation result of mismatched LC VCO output in response to with and without an incoming signal.

3) Envelope Detector

A simple envelope detector, which consists of squaring and low-pass filtering operations, is shown in Fig. 3.7. Transistors M6 and M7 form a differential pair as a peak detector whose input is connected to the output of the LC VCO, and its output, *envout+* is taken at the common-source node, which filters high frequencies by the parasitic capacitances at this node. The reference voltage is generated by having transistors M9 and M10 exactly match M6 and M7 in

size as a replica circuit but with its input connected to Vdd. If the VCO doesn't oscillate, the output of the VCO remains at the supply voltage, and output of the peak detector remains same as the replica circuit. When the VCO starts to oscillate, the common-source node of M6 and M7 follows the peak oscillator differential voltage, which increases its dc voltage. However, the amplitude of the oscillator output must be at least 60 mV to be detected by the envelope detector, which is illustrated in Fig. 3.10. In order to increase the quadratic gain of the envelope detector, both the peak detector and the replica circuit operate in subthreshold region[75]. The differential output between the common-source node of M6 and M7 and that of M9 and M10 is applied to the input of the PMOS transistors, M 12 and M 13, in the baseband amplifier.
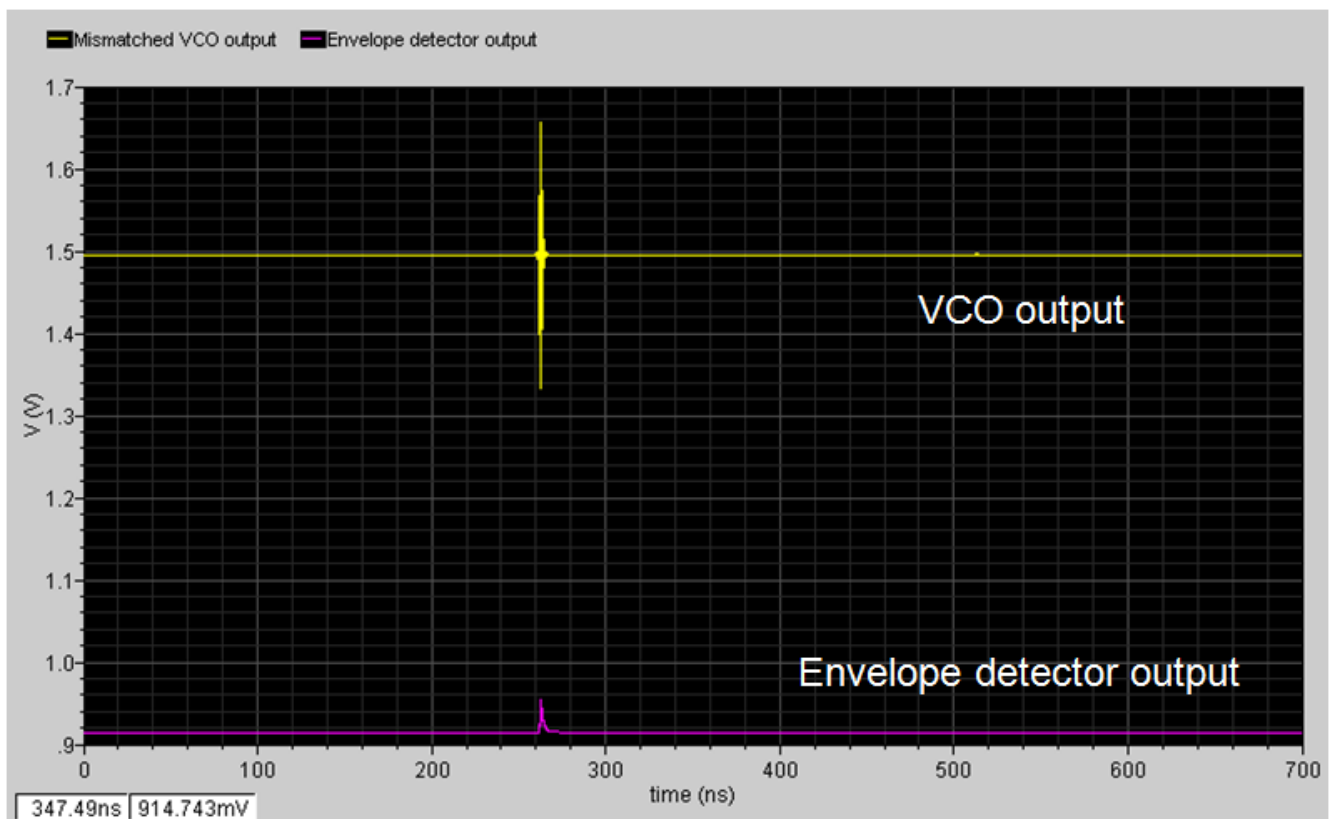
Fig. 3.10. Simulation result of mismatched VCO output and its corresponding a differential output of envelope detector.

4) Baseband amplifier

A self-biased baseband amplifier amplifies the differential envelope signal between the presence and absence of the incoming RF signal. Since this differential envelope signal has a low amplitude of approximately 70 mV if there is the incoming RF signal present, the baseband amplifier must provide enough gain so that the decision circuit can resolve the appropriate logic levels. In this study, the threshold voltage of the CMOS buffer circuit is 500mV. As shown in Fig. 3.11., the gain of this amplifier is approximately 6, which is high enough to exceed the decision circuit's threshold level when there is the incoming RF signal present. The current consumption for the baseband amplifier is 100 μA.
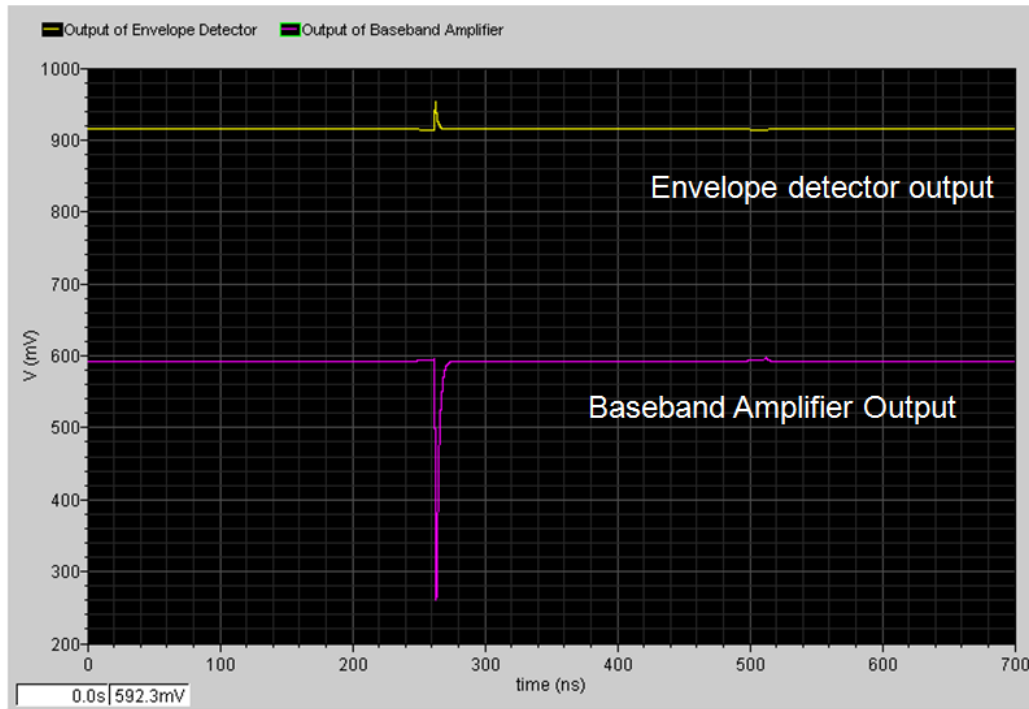
(a)
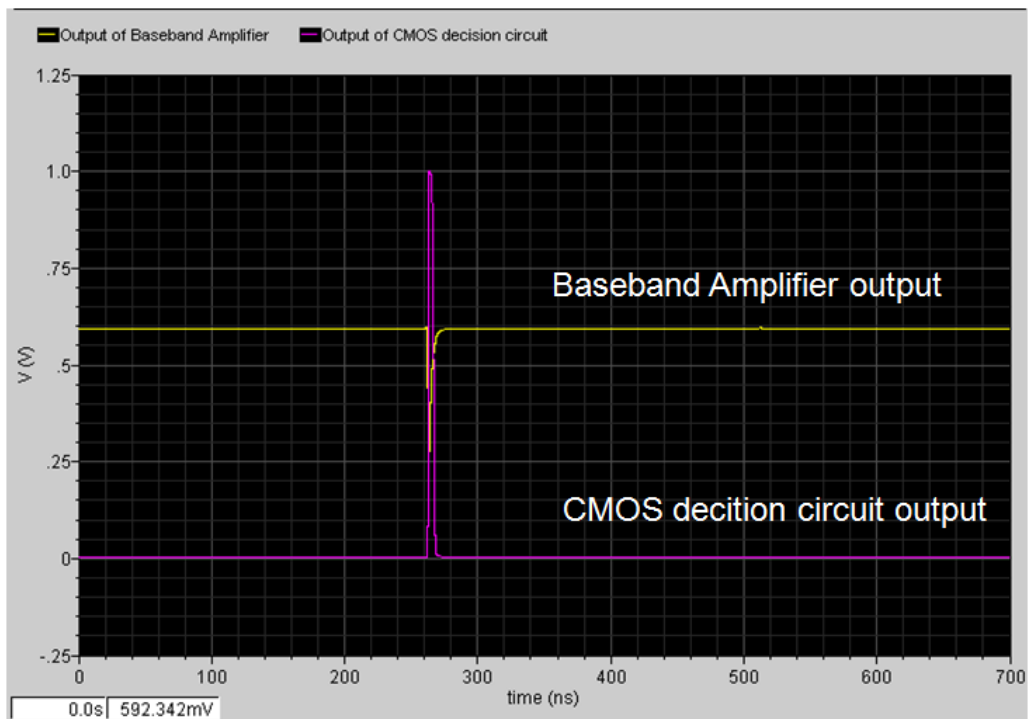
(b)

Fig. 3.11: Simulation result of a) Outputs of envelop detector and of baseband amplifier; b) Outputs of baseband amplifier and of CMOS decision circuit.

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B. Proposed Synchronization Circuitry Architecture

As mentioned in the previous section, an incoming RF signal must be aligned with quench signal to be amplified in super-regenerative receiver architecture. Thus, appropriate synchronization circuitry must be implemented. Unlike other studies [63-68], which employed sinusoidal quench signal with Phase-Locked Loop for alignment with an incoming RF signal or external quench signal for manual alignment, a tract-and-detection circuit, based on a dealy-locked loop (DLL), has been implemented in this study. The main blocks of the track and detection circuitry consist of a DLL, a Johnson counter, digital logics, selector circuits, pulse generators, and a switch MUX as shown in Fig. 3.12.
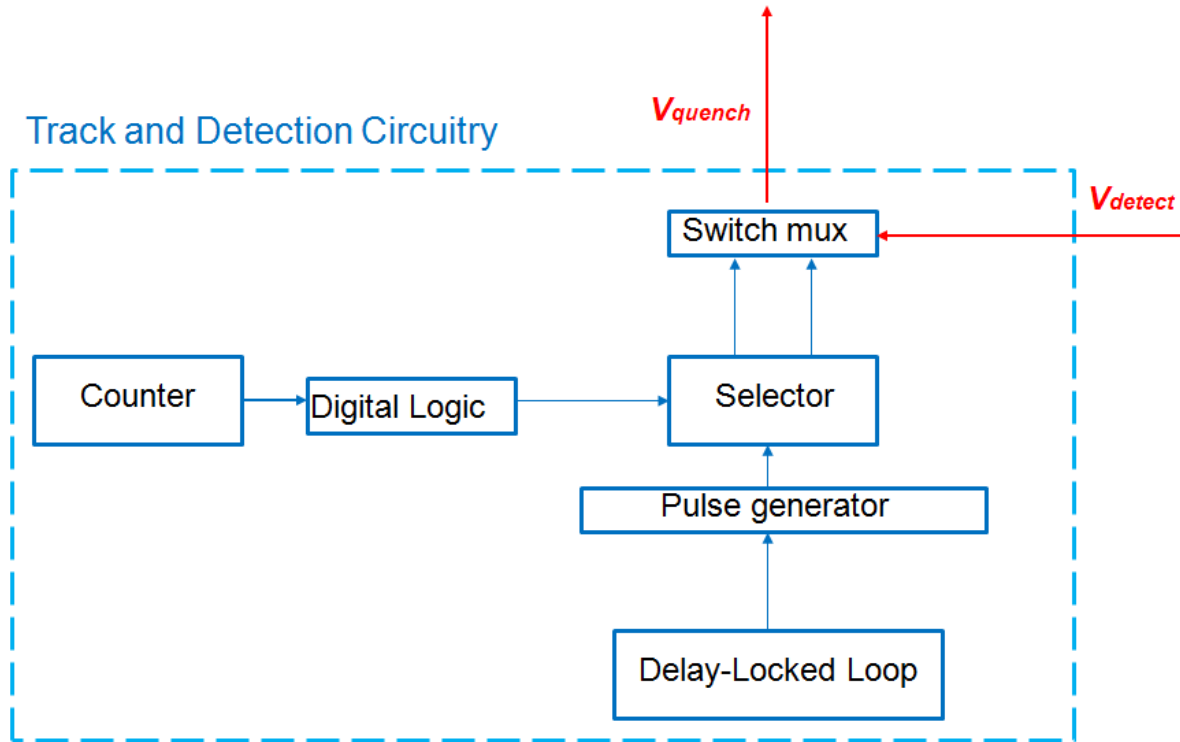
Fig. 3.12. The block diagram of track and detection circuitry.

1) Delay-Locked Loop

A 4 MHz reference clock is applied to a delay cell, which generates ten clock phases, each spaced by 25 ns. The reference clock and the output of the 10th delay cell are applied to the inputs of a Phase/frequency detector (PFD). Fig. 3.13 shows the block diagram of delay-locked loop.
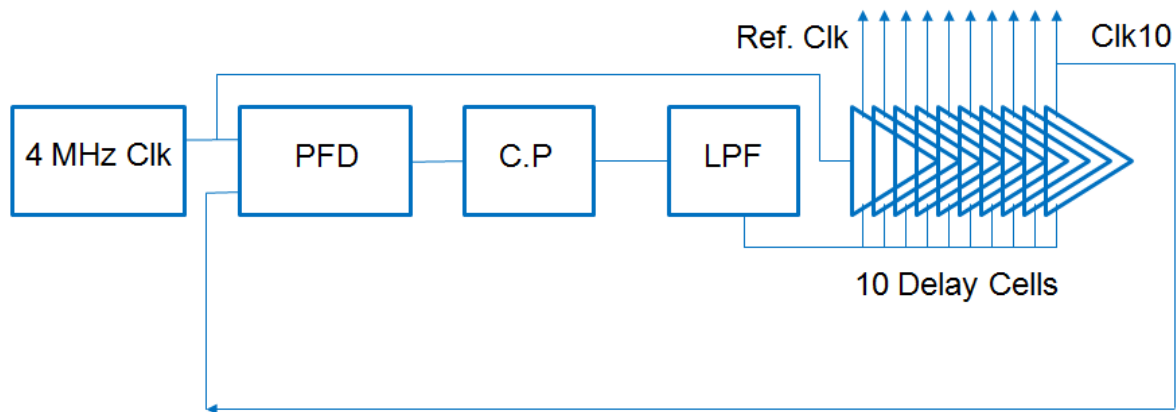
Fig. 3.13. Block Diagram of Delay-Locked Loop.

a. Voltage-controlled delay cell

In conventional DLL circuit implementation, the control voltage *Vctrl* is generally bounded by the supply voltage and the threshold voltage of controlled voltage input transistor. This limitation results in a limited tuning range. To widen the tuning range, the delay cell shown in Fig. 3.14 is used. Transistors M7 and M8 are employed to provide an auxiliary current path for a wide tuning range and rail-to-rail operation. The sizes of all transistors have been designed to achieve a nominal 25 ns delay.
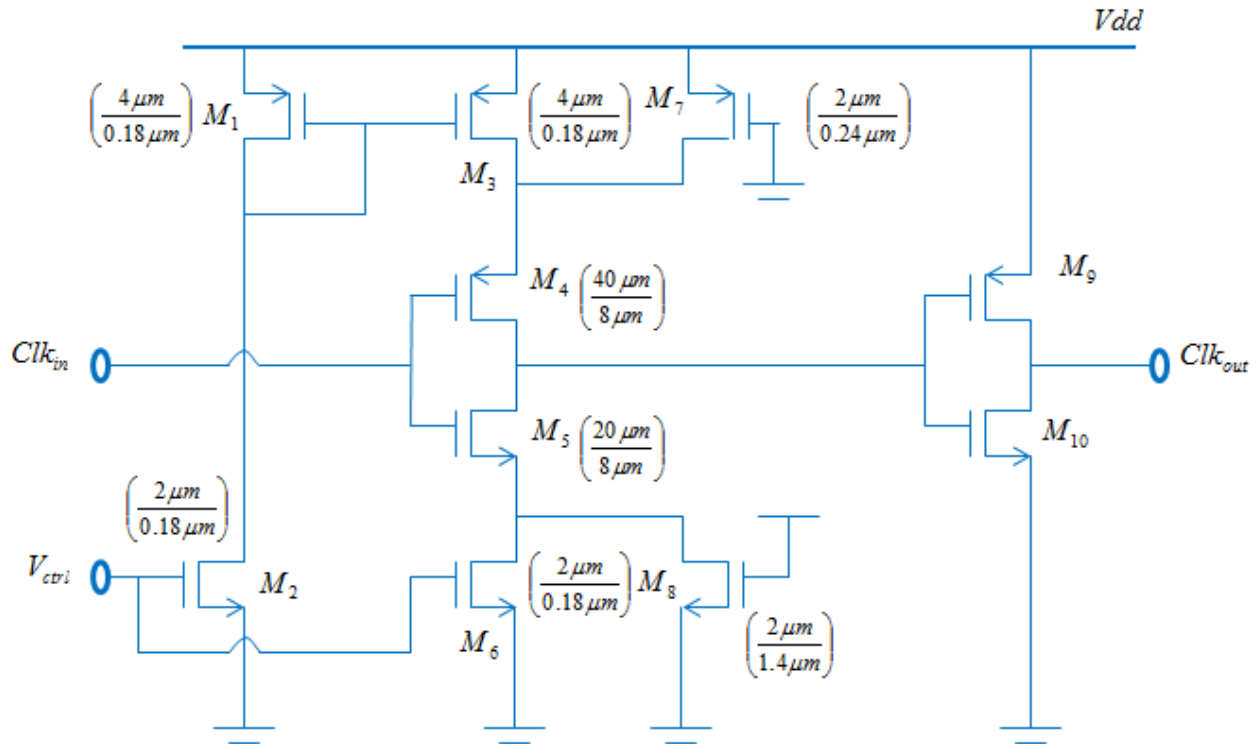
Fig. 3.14: Voltage-controlled delay cell.

b. The PFD/Charge pump and low pass filter

The PFD/Charge pump circuitry and the low-pass filter are shown in Fig. 3.15(a). The reset DFF, realized by TSPC circuitry, is shown in Fig. 3.15(b). The NAND gate is realized using standard static CMOS. The output of each D flip-flop controls the charge pump switch that conducts charge in or out of the filter capacitor.
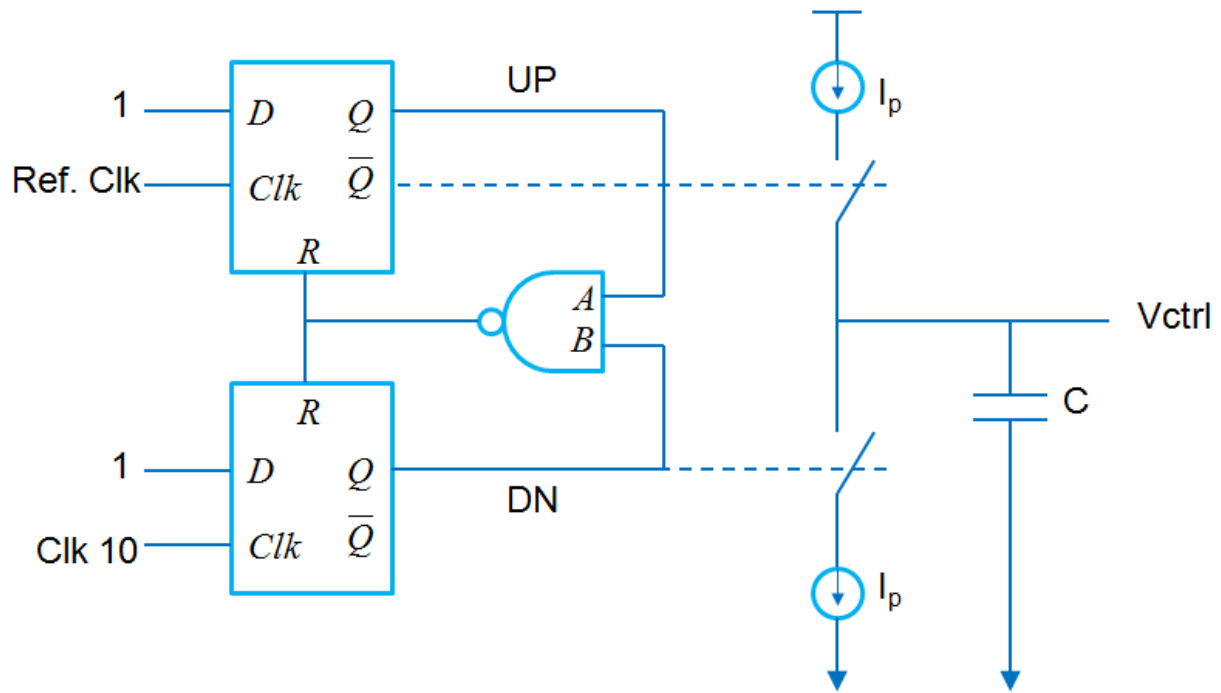
(a)
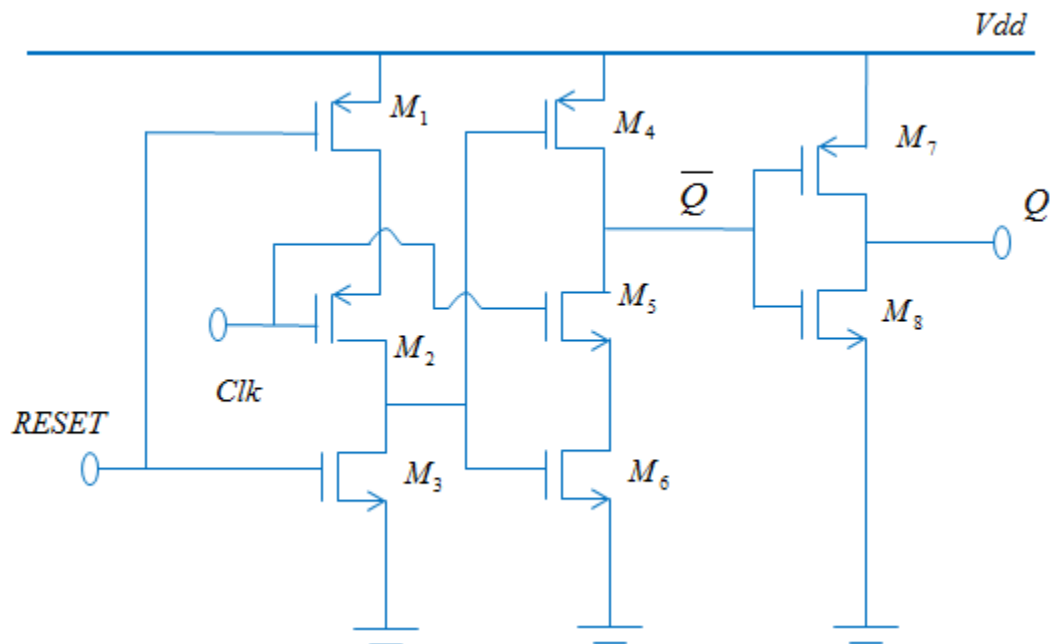
(b)

Fig. 3.15: (a) Schematic diagram of PFD/charge pump and low pass filter; (b) Transistor schematic of PFD.

2) Pulse Generator/Selector and Counter circuitry

As shown in Fig. 3.18, the pulse generator/selector circuitry consists of 5 XOR gates (Pulse Generator 1), 5 D flip-flops for Selector 1, 2 D flip-flops for Selector 2, 3 variable delay cells, 1 AND gate and 4 switch Multiplexers (MUX 1-4). Each XOR gate in the pulse generator 1 receives inputs from two adjacent clock signals in order to generate 25 ns pulses at the rate of 8 MHz. There are only 5 XOR gates are required because the pulse, for example, that is generated by reference clock and 1st delay cell (Clk1) is equivalent to the pulse generated by 5th delayed cell (Clk5) and 6th delayed cell (Clk6) as illustrated in Fig. 3.16.
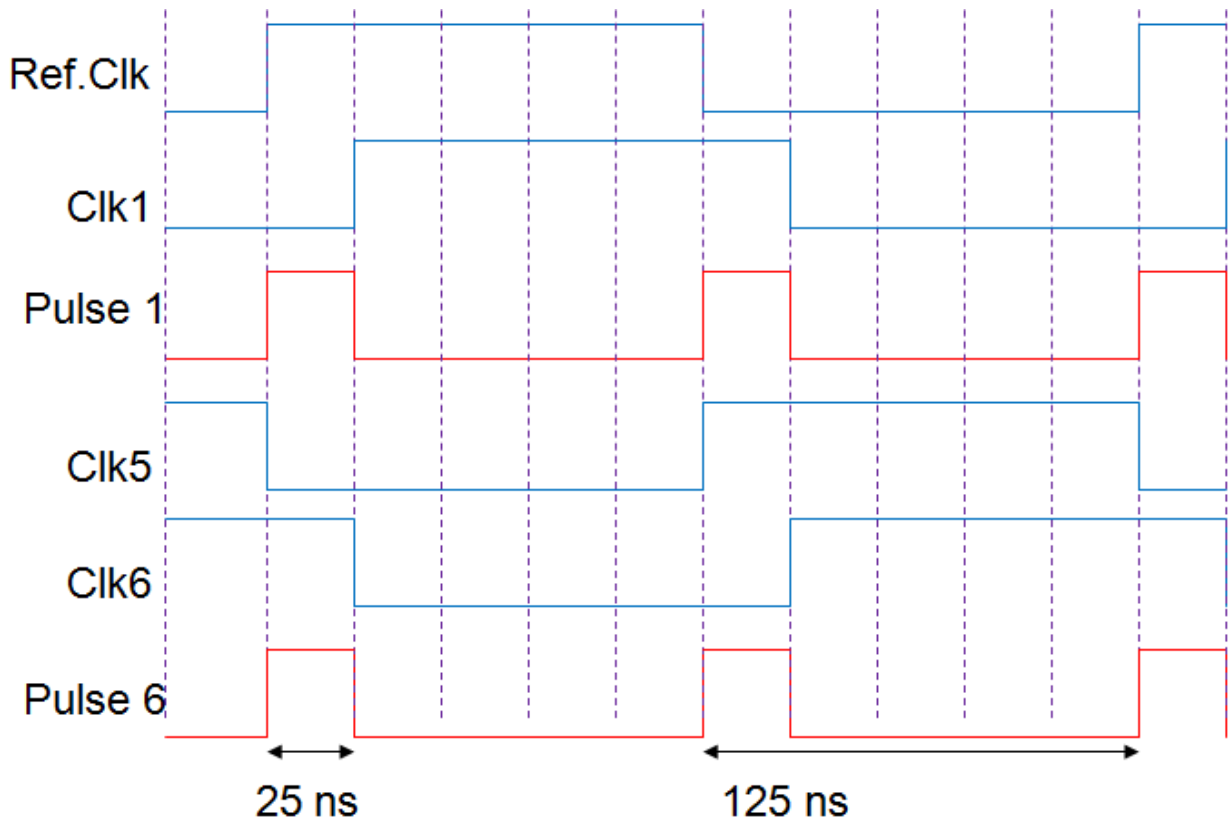
Fig. 3.16: Clocks and Pulse generator waveforms.

Each 25 ns pulse is sent as a "track" quench signal in one at a time, which is controlled by the unique state of counter circuitry. The counter circuitry consists of a 3 flip-flop Johnson counter and six 3 input NAND gates. A 3 flip-flop Johnson counter and six different combination input of 3 input NAND gate are implemented in Fig. 3.17 and Fig 3.18, respectively.
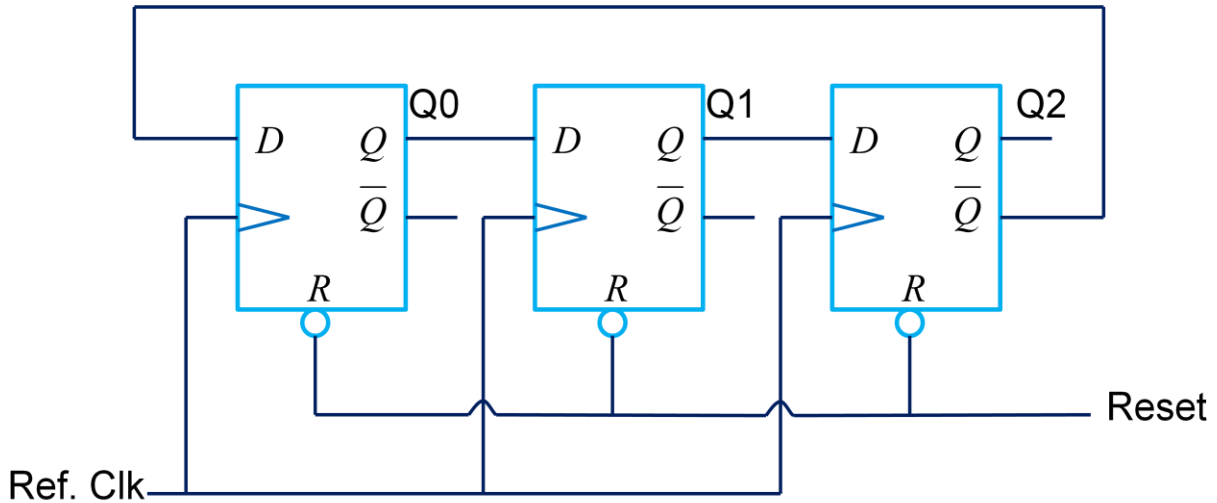
Fig. 3.17:   3 Flip-flop Johnson counter.

The number of unique states of this counter is 6 because a typical Johnson counter represents $2N$ states where N is number of bits. The truth table for the all possible states is shown in Table 3.1. The six unique states shown in Table 3.1 correspond with six 3 input NAND gates. Thus, each NAND gate acts as a switch to regulate the pulse so that only one 25 ns pulse can propagate as a quench signal in every 250 ns. For example, at the state of $Q_0=1$, $Q_1=0$, $Q_2=0$, which corresponds with the 3 input NAND gate switch in Fig. 3. 18(b) that controls a 25ns pulse generated by Ref.clk and the first delay cell, only the pulse is sent as a quench signal for the first 250 ns. For the next 250 ns, at the state of $Q_0=1$, $Q_1=1$, $Q_2=0$ only 25 ns pulse

generated by clk1 and clk2 is sent as a quench signal by the corresponding 3 input NAND gate switch.
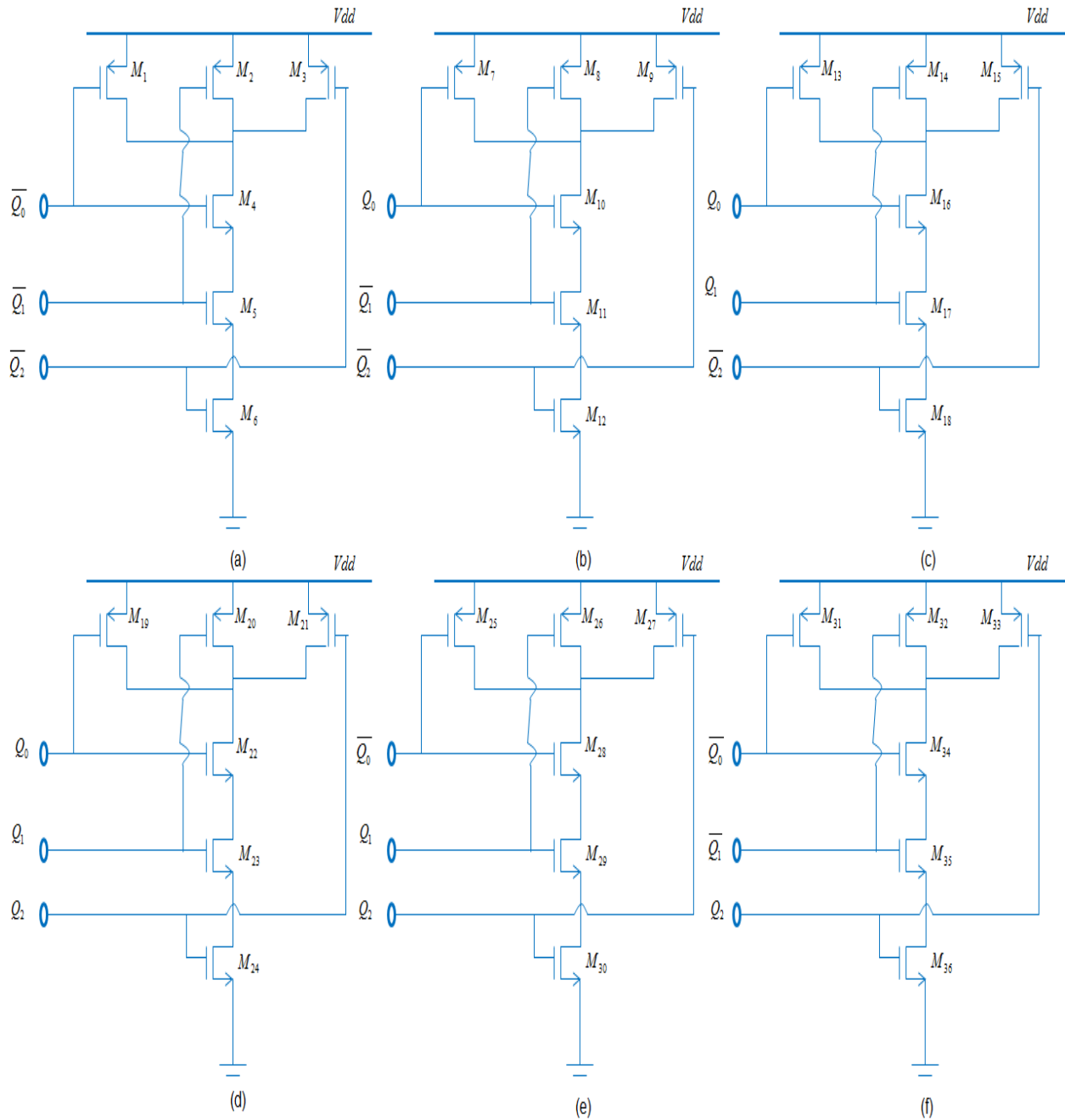
Fig. 3.18: Six NAND gate configuration state of (a) 000; (b) 100; (c) 110; (d) 111; (e) 011; (f) 001.

Table. 3.1 Truth Table for 3 Flip-flop Johnson counter

Truth Table			
State	**Q0**	**Q1**	**Q2**
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

The 3 flip-flop Johnson counter shown in Fig. 3.17 generates each state and a corresponding 25 ns pulse is sent as a quench signal until the incoming signal is detected. Once the incoming signal (*Venv*) is detected, the same incoming signal (*Venv*) also sends to the selector 1 and the selector 2 as a clock signal. Whenever a particular DFF in selector 1 and 2 detects the incoming signal, its output turns on the switch and the corresponding the delay cell output is sent to the pulse generator and eventually to a "detect" quench signal. In other words, once the incoming signal is detected and the baseband signal arrives from the CMOS decision circuit in the frond-end, the selector circuitry chooses the appropriate delay cell to which the incoming RF signal is applied and holds the pulse generated by the delay cell as the quench signal as shown in detail in Fig. 3.19. while deactivating the counter circuitry to save power consumption.
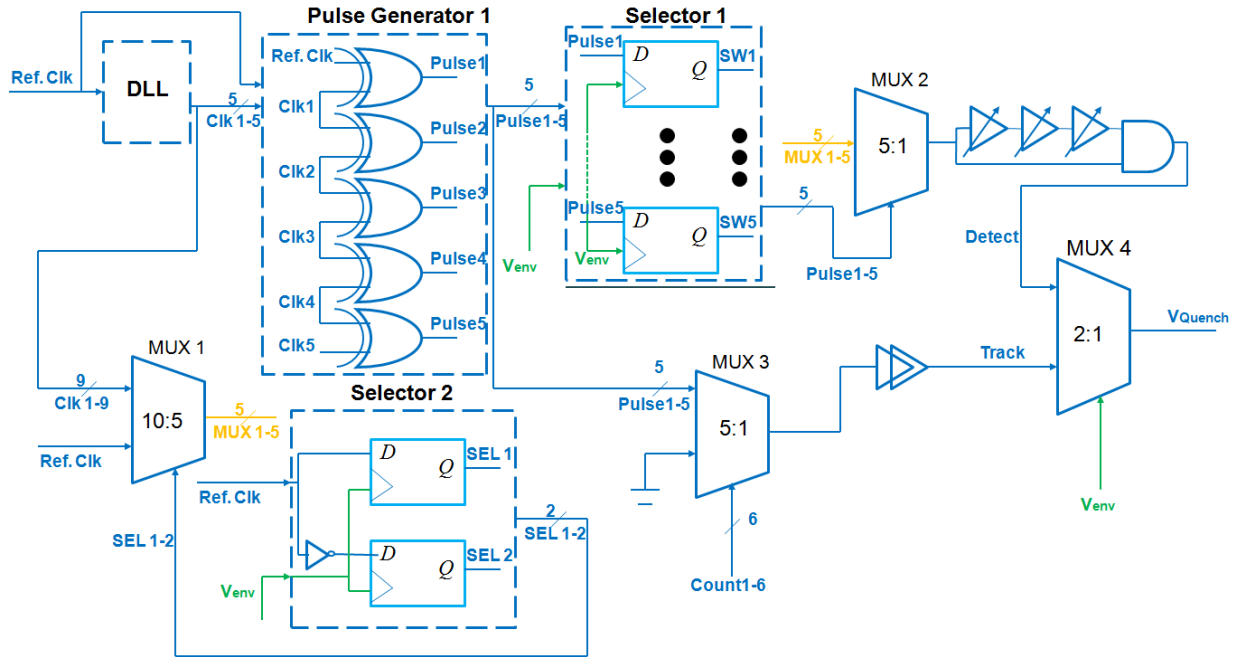
Fig. 3.19: Pulse generator and selector circuitry.

3.4 Measurement and Results

The receiver has been implemented in a SBC 18 BiCMOS 0.18 μm technology, with a die size of 900 μm x 1400 μm, whose area is mostly occupied by bond pads and an on-chip inductor. The chip microphotograph and the chip mounted PCB are shown in Fig. 3.20.
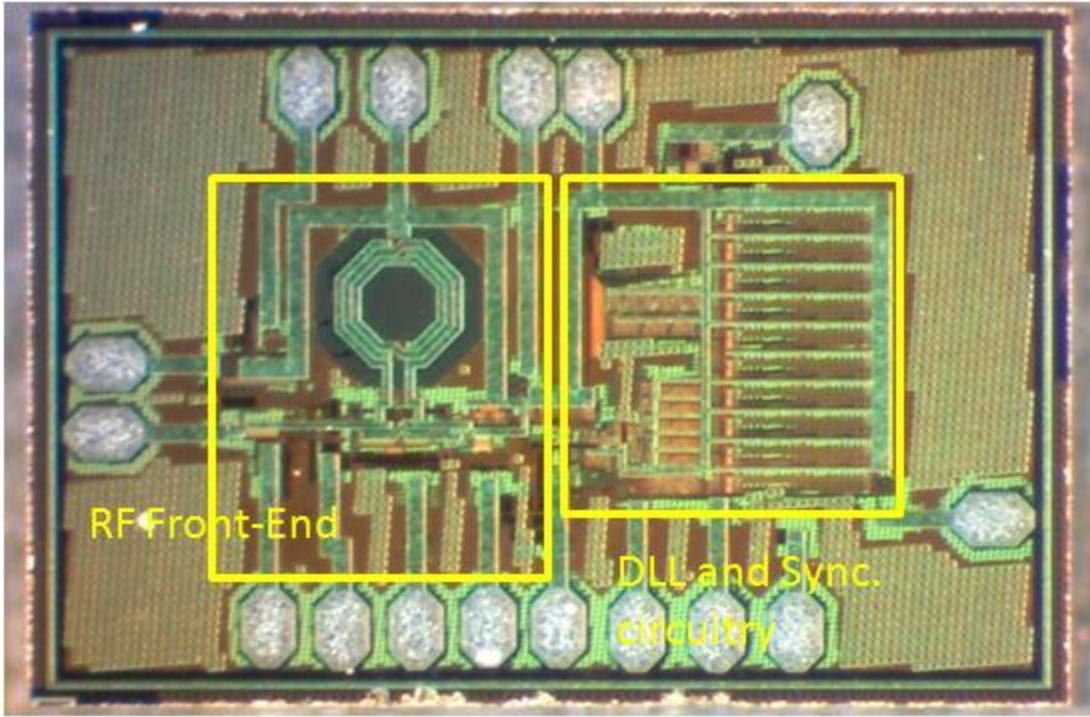
(a)
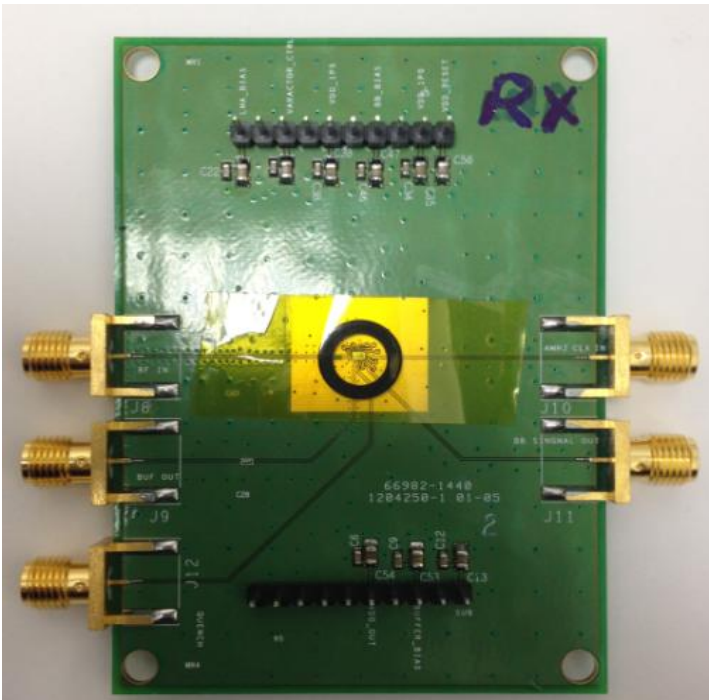
(b)

Fig. 3.20: (a) Die photo (b) Chip mounted PCB.

The measurement setup is shown in Fig. 3.21. The incoming RF pulse whose bandwidth is 500 MHz is generated using combination of two waves; the first pulse is generated using a pulse generator/divider and an HP 8665B synthesized signal generator. The other waveform is a 4.5 GHz sine wave generated by another HP 8665B synthesized signal generator. The two signals are mixed employing a passive mixer Anzac MD-525-4.
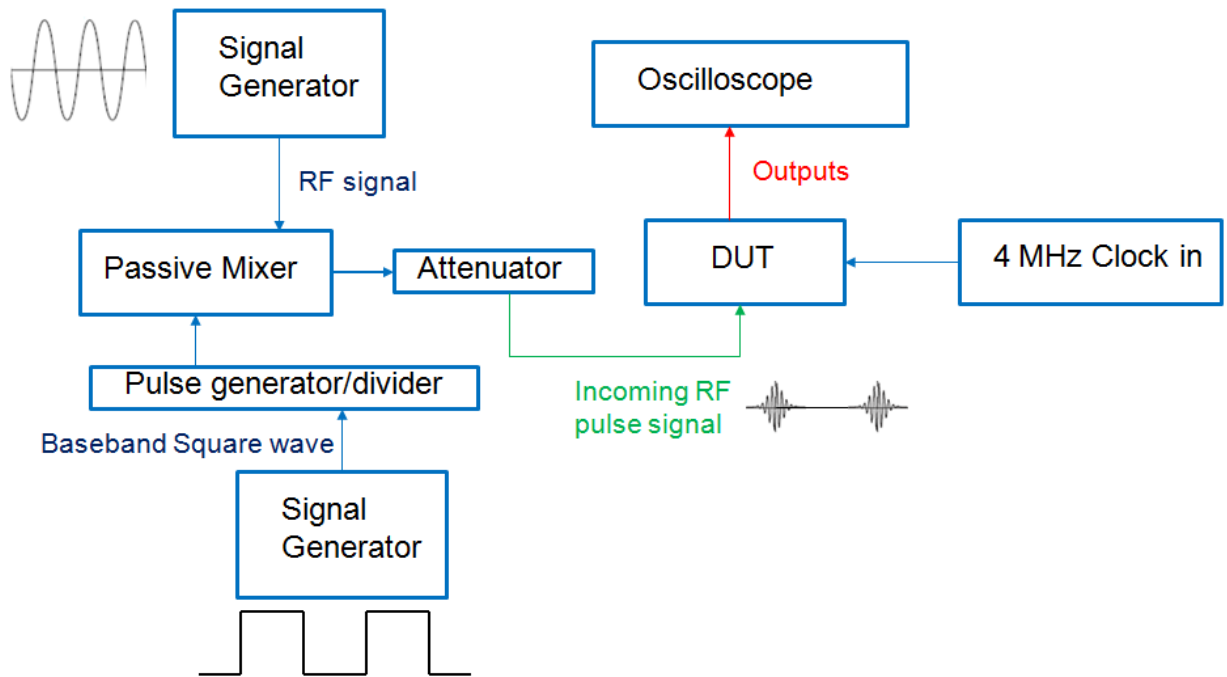
Fig. 3.21: Measurement setup.

Following the mixer, the IR-UWB signal is passed through an attenuator to mimic the path loss in the wireless transmission. The measured RF signal and baseband signal are monitored in the time domain by an Agilent Infiniium DSA91204A Digital Signal Analyzer while the frequency measurement of the VCO is generated using a Rohde & Schwarz FSW Signal & Spectrum Analyzer.

Since the super-regenerative receiver is periodically quenched, the front-end gain *(G)* is measured in the time domain. As the peak voltage at the resonator output is sampled to determine the presence of a pulse, the front-end voltage gain of the IR-UWB receiver is defined as the ratio between the peak oscillator output voltage and the input received voltage across 50 Ω to yield

$$G = \frac{\hat{V}_{OSC}}{V_{in}}$$
(3.3)

The input average power of –80 dBm (peak power = -63 dBm) is fed into the LNA input and the output peak-to-peak voltage across the VCO resonator in the presence of an incoming rf pulse is about 18 mV as shown in Fig 3.22. Thus, the front-end gain of asymmetric super regenerative receiver is calculated to be about 38 dB.
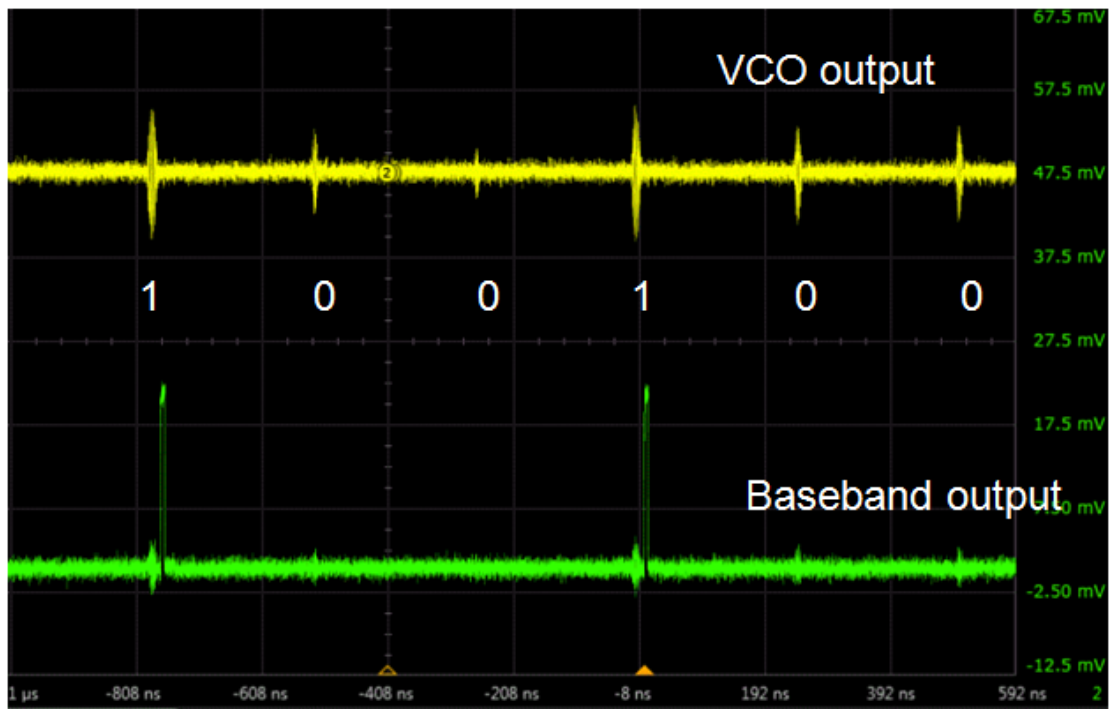
Fig. 3.22: Oscillator output (Yellow) and Detected Baseband signal (Green).

Once the incoming signal is detected, the system stays locked as explained in the previous section. Fig. 3.23 shows VCO outputs and detected baseband outputs in locking state of 0100100100100 sequences.
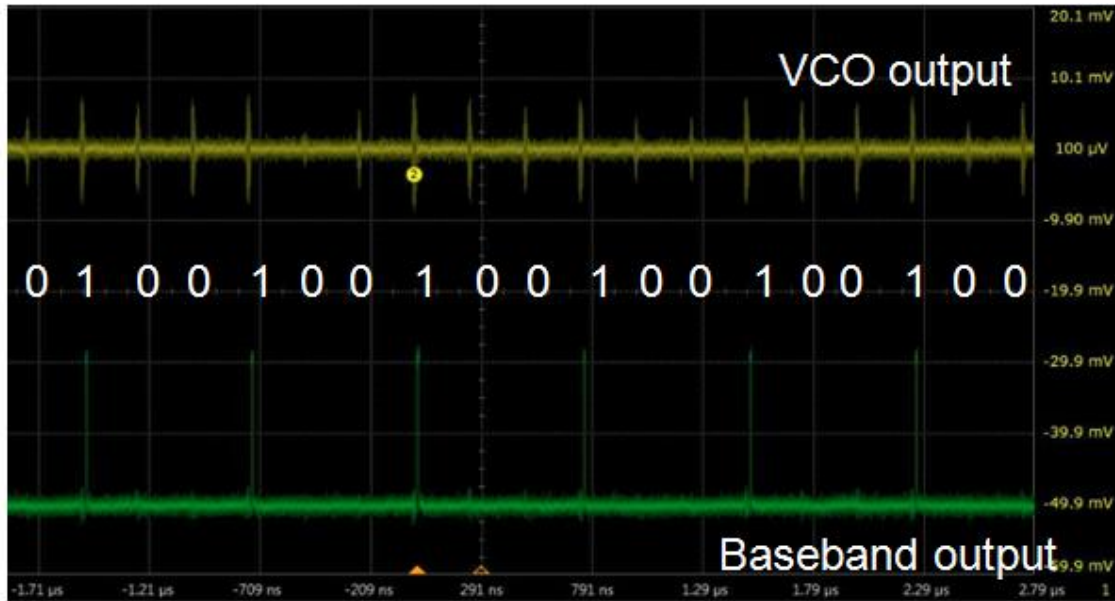
Fig. 3.23: Oscillator output (Yellow) and Detected Baseband signal (Green) of locking state.

The center frequency is measured to be 4.5 GHz as shown in Fig. 3. 24. A 1.5 V supply is used in the RF front-end circuits while a 1.0 V supply is used in the rest of the system. The current consumption for LNA is 2.2 mA and for the core oscillator is 1.8 mA. The RF front-end power consumption of 6.8 mW accounts for 90% of the total power consumption.
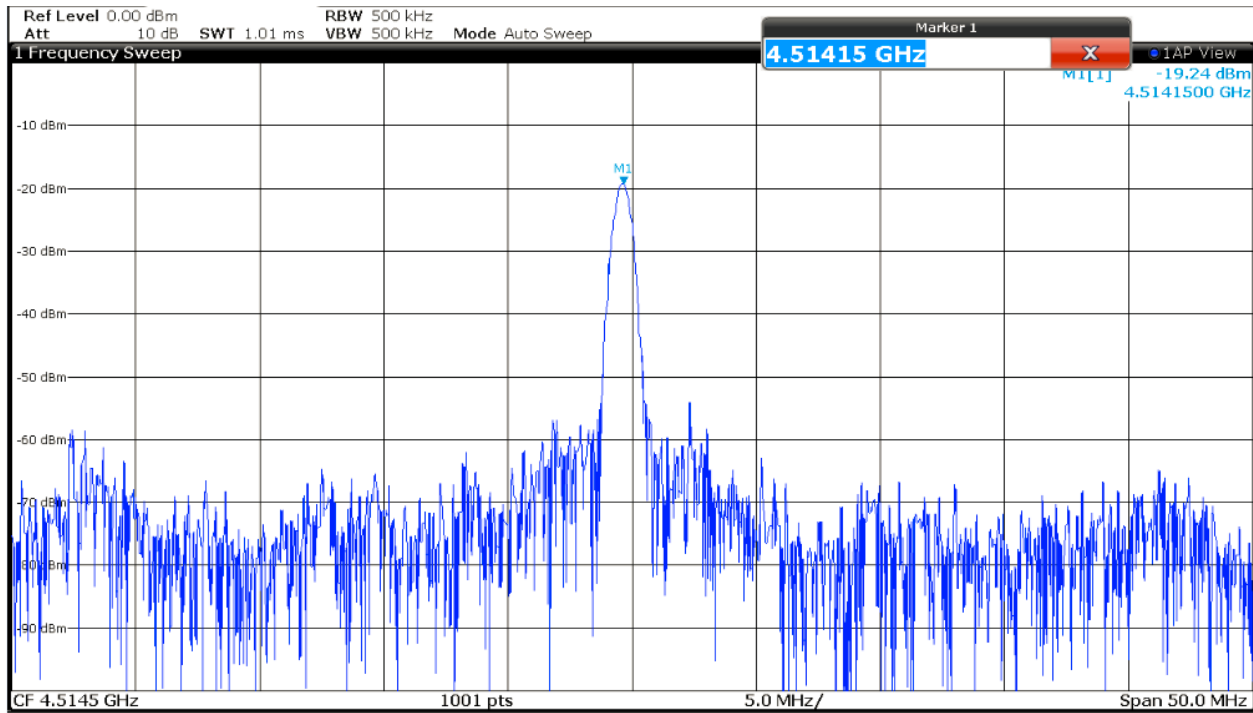
Fig. 3. 24: Core oscillator output spectrum at 4.5 GHz.

The performance summary of the receiver is shown in Table 3.2.

Table 3.2. Performance summary of tracking and lock asymmetric super-regenerative receiver

Supply Voltage	1.5 V(RF Front-End), 1.0V
Modulation	OOK
Duty Cycle	10%
Data Rate	4 Mbps
Die area (include pads)	900 μm x 1400 μm
Center Frequency	4.5 GHz
Energy per bit	0.17 nJ/bit
Total Power consumption	6.8 mW
LNA	2.2 mA
VCO	1.8 mA
Env.Detector&Baseband Amp.	0.15 mA
Track and detection Circuitry	0.58 mA

Energy consumption comparison with the other published IR-UWB receiver is summarized in Table 3.3

Table 3.3 Receiver performance comparison

	Data rate	Power consumption	Center Frequency	Energy/bit	System
Zheng et al [71]	15.6 Mbps	102 mW	3.1 to 9.5 GHz	6.51 nJ/bit	Coherent IR-UWB receiver system
Zhang et al [72]	50 Mbps	156 mW	3 to 9 GHz	N/A	Coherent IR-UWB receiver system
Lee et al [74]	100 kbps	35.8 mW	3.4 GHz, 3.9 GHz, and 4.4 GHz	2.5 nJ/bit	Non-coherent IR-UWB receiver system
Daly et al [73]	16 Mbps	22.5 mW	3 to 5 GHz	1.4 nJ/bit	Non-coherent IR-UWB receiver system
Vouilloz et al [75]	20 kbps	1.3 mW	N/A	65 nJ/bit	Narrow band super-regenerative receiver system
Chen et al [64]	500 kbps	2.8 mW	2.4 GHz	5.6 nJ/bit	Narrow band super-regenerative receiver system
Otis et al [76]	5 kbps	0.4 mW	1.9 GHz	80 nJ/bit	Narrow band super-regenerative receiver system
Bohorquez et al [65]	120 kbps	0.4 mW	391 to 415 MHz	3.3 nJ/bit	Narrow band super-regenerative receiver system
Ayers et al [78]	2 Mbps	215 uW	2.4 GHz	0.175 nJ/bit	
Pelissier et al [61]	1 Mbps	11.16 mW	4 GHz	N/A	Circuit consists of RF-Front only
Thoppay et al [63]	10 Mbps	10.8 mW	3.494 and 3.993 GHz	0.24 nJ/bit	Non-coherent IR-UWB receiver system
This work	**4 Mbps**	**6.6 mW**	**4.5 GHz**	**0.17 nJ/bit**	**Non-coherent IR-UWB receiver system**

3.5 Summary

In this study, RF front-end architecture with asymmetric LC-VCO based on the super-regenerative principle and baseband track and lock synchronization of an incoming rf signal with internal quench signal has been presented. The proposed receiver is implemented in 0.18 μm SBC 18 BiCMOS technology and is able to track and lock onto an incoming rf signal with an internal quench signal. The receiver system consumes 0.17 nJ per bit, which demonstrates the lowest energy consumption reported so far for an IR-UWB receiver system.

Chapter 4.   Conclusion

In this dissertation, a transmitter and a super-regenerative receiver used in an IR-UWB system have been analyzed theoretically and have been implemented in 0.18 μm CMOS technology. The motivation of this research is to focus on low power consumption in IR-UWB system architecture.

In Chapter 2, a low-power IR-UWB transmitter has been presented and implemented in 0.18 μm CMOS technology. By deliberately introducing mismatch to a cross-coupled transistors and varactors, the asymmetric LC-VCO can generate 300 ps faster startup pulse compared to the symmetric VCO without adding extra circuitry. The energy dissipation per pulse is 31.5 pJ per bit.

In Chapter 3, a low-power IR-UWB receiver based on the super-regenerative principle has been investigated and implemented in 0.18 μm BiCMOS technology. In order to enhance power consumption and to solve the synchronization issue, RF front-end architecture with asymmetric LC-VCO has been employed and DLL based track and detection circuitry has been developed respectively. The receiver system consumes 0.17 nJ per bit, which demonstrates the lowest energy consumption reported so far for an IR-UWB receiver system.

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