UNIVERSITY OF CALIFORNIA, SAN DIEGO

Integrated Tunable Duplexer in CMOS Technology for Multiband Cellular Transceivers

A dissertation submitted in partial satisfaction of the
requirements for the degree
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in

Electrical Engineering (Electronic Circuits and Systems)

by

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2013

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DEDICATION

To my family.

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S. Abdelhalem, P. Gudem, and L. Larson, "Hybrid transformer-based tunable integrated duplexer with antenna impedance tracking loop", *IEEE Custom Integrated Circuits Conference*, submitted for publication.

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S. Abdelhalem, P. Gudem, and L. Larson, "Hybrid transformer-based tunable differential duplexer in a 90-nm CMOS process", *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1316–1326, March 2013.

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ABSTRACT OF THE DISSERTATION

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Frequency division duplex (FDD) cellular standards, like WCDMA and LTE, require the simultaneous operation of the transmitter and receiver while sharing the same antenna. A duplexer, currently implemented as two highly selective off-chip SAW filters separates the transmit and receive signals. A high isolation is required to avoid saturating the receiver and keep its noise and linearity requirements feasible.

The need for high-Q resonators to implement these filters prohibits duplexer integration in a CMOS process. For each band of a modern multi-band transceiver, an off-chip duplexer is required. With over forty bands currently envisioned for

mobile applications, the system cost and complexity rises significantly. Replacing the bank of off-chip duplexers with a single integrated tunable duplexer would enable a fully integrated and reconfigurable multiband transceiver.

In this dissertation, the performance of hybrid transformer based integrated duplexer was significantly improved, making it suitable for reliable multiband operation. A hybrid transformer relies on electrical balance rather than frequency selectivity to achieve isolation, making duplexer integration in a CMOS process that lacks high-Q passives possible. Prior demonstrations of integrated hybrid transformer duplexers suffered from high insertion loss, poor common-mode isolation and isolation sensitivity to antenna mismatch. Novel solutions were reached in this research to solve most of these issues. Power recovery by using an RF-DC converter can effectively reduce the loss in the duplexer. A discrete prototype that achieves 60% power recycling efficiency with constant input impedance over wide dynamic range was demonstrated. A differential implementation of the hybrid transformer allows for both high differential and common-mode isolation. Implemented in a 90nm CMOS process, it maintains more than 60 dB of differential to common-mode isolation. And finally, an antenna impedance tracking loop was demonstrated to track any antenna impedance variation and maintain high isolation. Together with a novel high power balance network, that allows high isolation in both the transmit and receive bands, this 65nm CMOS chip achieves an isolation of more than 50 dB in the transmit and receive bands, with an antenna VSWR within 2:1. This work is the first implementation of a CMOS integrated, high-power and antenna mismatch tolerant duplexer.

Chapter 1

Introduction

Frequency division duplex (FDD) transceivers require the simultaneous operation of the transmitter and receiver while sharing the same antenna. Two different but closely spaced frequency bands are employed for transmission and reception. A duplexer, currently implemented as two highly selective off-chip SAW filters, one centered at the receive band and the other at the transmit band, separates the transmit and receive signals. Due to the finite isolation of the duplexer, the strong transmit signal leaks to the receiver input, desensitizing the receiver through several mechanisms: receive band noise, reciprocal mixing, cross-modulation distortion and second-order intermodulation. A high transmitter to receiver (TX-RX) isolation is required to limit these effects and keep the receiver noise and linearity requirements feasible.

The need for high-Q resonators to implement these highly selective filters prohibits duplexer integration in a CMOS process. Moreover, because the filter bandwidth and center frequency are not programmable, for every band of operation supported by a modern multi-band transceiver, a dedicated input and its corresponding duplexer are needed. A multi-pole switch selects the appropriate duplexer based on the operating frequency. With over forty bands currently envisioned for mobile applications by the 3GPP, the system cost and complexity rises significantly. Replacing the bank of off-chip duplexers with a single integrated tunable duplexer would enable a fully integrated and reconfigurable multiband transceiver.

In this chapter, the basic operation and performance metrics of a duplexer are explained. The transmitter (TX) leakage effect on the receiver design requirements in a FDD system is explained, and the motivation for duplexer integration is justified. An integrated implementation of the duplexer using hybrid transformer is introduced together with its main advantages and limitations.

1.1 Time and Frequency-Division Duplexing

Achieving two-way communication by a transceiver is a function called "duplexing". One method of duplexing is "time-division duplexing" (TDD) where the same frequency band is utilized for both transmit (TX) and receive (RX) paths, but the system transmits for half of the time while disabling the receive path and receives for the other half while disabling the transmit path. Illustrated in Figure 1.1(a), TDD is usually performed fast enough to be transparent to the user.

Another approach to duplexing is to employ two different frequency bands for the transmit and receive paths. Called "frequency-division duplexing" (FDD) and shown in Figure 1.1(b), this technique incorporates bandpass filters to isolate the two paths, allowing simultaneous transmission and reception. Since two such transceivers cannot communicate directly, the TX band must be translated to the RX band at some point. In cellular networks, this translation is performed in the base station.

To contrast the two duplexing methods, let us consider their merits and drawbacks [1]. In TDD, an RF switch with a loss less than 1 dB follows the antenna to alternately enable and disable the TX and RX paths. Even though the transmitter output power can be 100 dB above the receiver input signal, the two paths do not interfere because the transmitter is disabled during reception. Furthermore, TDD allows direct (peer-to-peer) communication between two transceivers, an especially useful feature in short-range applications. The primary drawback of TDD is that the strong signals generated by all of the nearby mobile transmitters fall in the receive band, thus potentially desensitizing the receiver. Examples of wireless

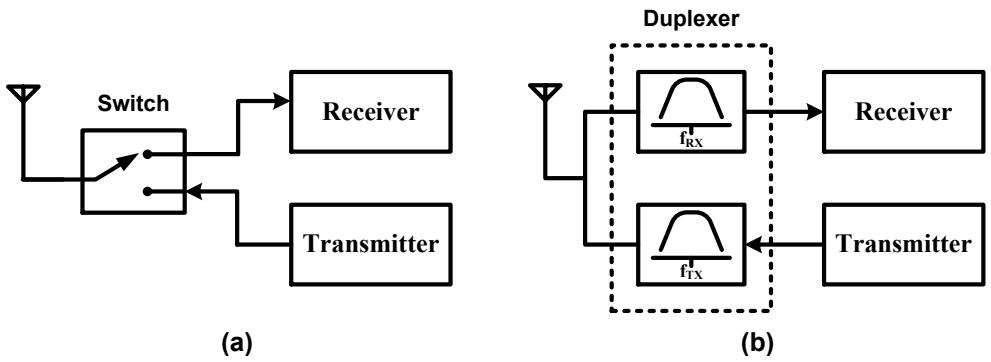


Figure 1.1: (a) Time-division duplexing. (b) Frequency-division duplexing.

technologies employing TDD include: GSM[1], China's TD-SCDMA and TD-LTE, and WLAN standards.

In FDD systems, the two front-end bandpass filters are combined to form a "duplexer filter". While making the receivers more immune to the strong signals transmitted by other mobile units, FDD suffers from a number of issues. First, components of the transmitted signal that leak into the receive band are attenuated by typically about 45–50 dB and still constitute a major concern on the receiver operation as detailed in the next section. Second, the loss of the duplexer is typically much higher than that of a TDD switch[2]. Note that a loss of 3 dB in the RX path of the duplexer raises the overall noise figure by 3 dB and the same loss in the TX path means that only 50% of the signal power reaches the antenna. While providing acceptable isolation between the TX and RX paths, typical off-chip duplexers indeed exhibit a loss of 2 to 3 dB. Despite these drawbacks, FDD is employed in many RF standards particularly in cellular communications, examples include: WCDMA and LTE.

[1]GSM transmitter and receiver employ different frequency bands but only one is active at a time.

[2]Even when a TDD receiver employs an RF filter for out-of-band blocker rejection, its loss is less than a duplexer due to the relaxed out of band rejection requirements relative to a duplexer.

1.2 TX Leakage Impact in FDD Systems

Due to the finite isolation of the duplexer, the strong transmit signal leaks to the receiver input, potentially desensitizing the receiver through several mechanisms. Each of these mechanisms are further explained in the following.

1.2.1 Receive Band Noise

Due to the phase noise in the transmitter local oscillator (TX LO), IQ modulator and power amplifier, the output spectrum of the transmitter has a high noise content at the RX frequency [2]. This transmitter noise falling into the receive band raises the receiver noise floor and can easily degrade the receiver noise figure unless adequate TX-RX isolation is achieved by the duplexer at the RX band. This noise contribution is given by

$$N_{TX}(\omega_{RX})(\text{dBm}) = NPSD_{TX}(\text{dBm/Hz}) + 10\log_{10}\big(BW(\text{Hz})\big) - ISOL_{TX-RX}(\omega_{RX}) \tag{1.1}$$

where $NPSD_{TX}$ is the noise power spectral density at the TX output, BW is the channel bandwidth, and $ISOL_{TX-RX}(\omega_{RX})$ is the duplexer isolation in the RX band. Typical implementations of the duplexer provide an isolation of 45 dB in the receive band.

1.2.2 Second-Order Intermodulation

In a direct-conversion receiver, even-order nonlinearity becomes problematic. Second-order distortion could down convert the strong TX leakage to DC as illustrated in Figure 1.2. The source of nonlinearity could originate from the LNA together with a finite direct feed through from the RF input to the IF output of the mixer, this can normally be minimized by AC coupling the LNA to the mixer. Another source could be the mixer itself, differential implementations minimize the second order distortion and it becomes limited only by mismatches [3, 4].

Another mechanism for second-order distortion that becomes important in a wideband receiver occurs when there is a jammer at $f_{TX} + f_{RX}$. When such a

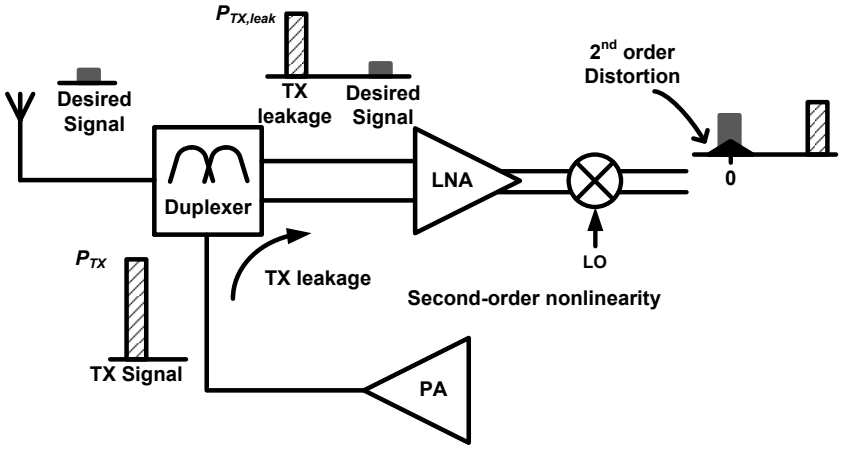


Figure 1.2: Second-order distortion generation due to transmitter leakage.

jammer mixes with the TX leakage, the resulting second order distortion falls at f_{RX}. In such a case, the second-order nonlinearity of the LNA is more important as it will fall in the same RF band as the desired signal.

Second-order distortion can be characterized using the second-order intercept point ($IP2$). Two equal-amplitude tones are applied at the input and their low-frequency intermodulation distortion ($IM2$) is observed at the output. Plotting the fundamental output and the $IM2$ versus the input power and extrapolating to get the intersection yields the $IP2$. In a two-tone TX leakage case, the generated second-order intermodulation distortion is related to the IIP2 by

$$IM2(\text{dBm}) = 2P_{TX,leak}(\text{dBm}) - IIP2(\text{dBm}) - 6 \text{ dB} \tag{1.2}$$

where the 6 dB corresponds to using two tones with half the TX leakage power each. A correction factor of about -5.4 dB is sometimes added to this equation to take into account the difference in second-order distortion created by two-tone test signals relative to that resulting from a modulated signal [5]. This factor is assumed to be extra design margin here.

1.2.3 Reciprocal Mixing

Referring to Figure 1.3, when the wanted signal is accompanied by a large TX leakage and the local oscillator exhibits finite phase noise, the downconverted

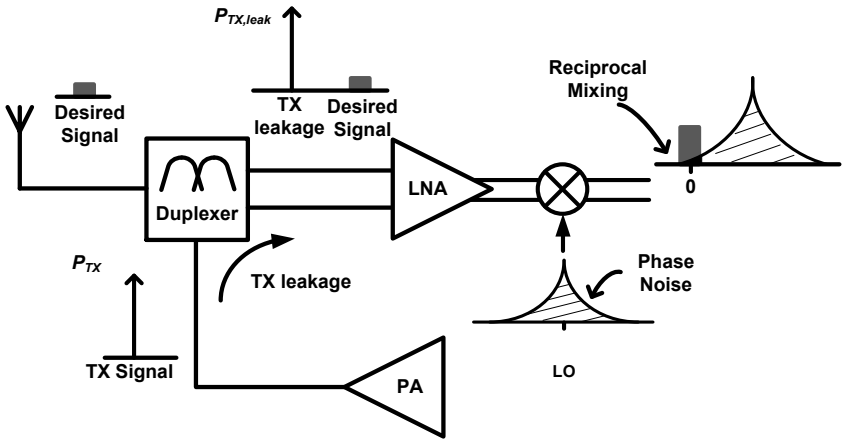


Figure 1.3: Reciprocal mixing.

band consists of two overlapping spectra, with the desired signal suffering from significant noise due to the tail of the downconverted TX leakage. This effect is called reciprocal mixing. The resulting noise added can be related to the LO phase noise at the TX offset frequency $\mathscr{L}(|f_{RX} - f_{TX}|)$ and the TX leakage power (P_{TX}) by:

$$N_{rmix}(\text{dBm}) = P_{TX,leak}(\text{dBm}) + \mathscr{L}(|f_{RX} - f_{TX}|)(\text{dBc/Hz}) + 10\log_{10}\left(BW(\text{Hz})\right) \tag{1.3}$$

1.2.4 Cross-Modulation Distortion

The generation of cross-modulation distortion that results from mixing the TX leakage with a strong in-band jammer is illustrated in Figure 1.4. This cross-modulation results from the third order nonlinearity and is proportional to the square of the TX leakage multiplied by the jammer (i.e $\propto TX_{leak}^2 \times$ Jammer) [6].

A common linearity test to assess the receiver linearity in the presence of TX leakage is the triple-beat (TB) test. The modulated TX signal is approximated by a two-tone signal injected at the PA port and a blocker is injected at the antenna port, and the resulting cross modulation is observed at the output. Using a power series expansion for the receiver nonlinearity, the generated cross-modulation

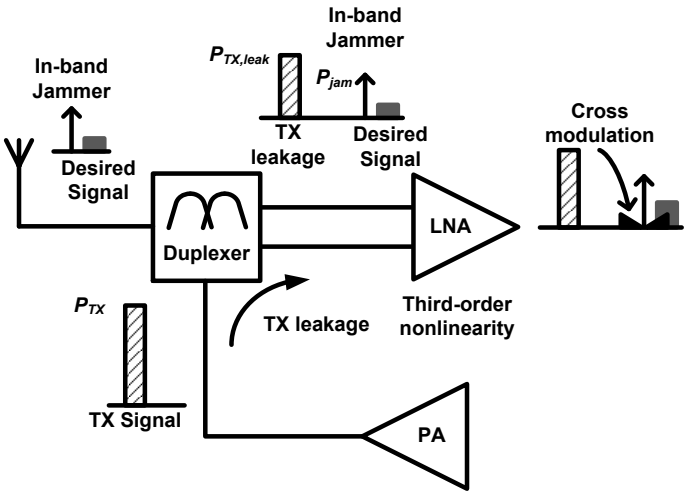


Figure 1.4: Cross modulation distortion generation due to transmitter leakage.

distortion (XMD) can be related to the TX power and receiver IIP3 by:

$$XMD(\text{dBm}) = P_{jam}(\text{dBm}) - 2IIP3(\text{dBm}) + 2P_{TX,leak}(\text{dBm}) \tag{1.4}$$

An improvement of 20 dB in cross-modulation distortion occurs for every 10 dB improvement in duplexer isolation.

1.2.5 Full-Duplex and half-Duplex Blocker

When the TX leakage is mixed by a large out-of-band blocker at half or twice the duplex spacing from the receive band, i.e. at $(f_{TX}+f_{RX})/2$ or $2f_{TX}-f_{RX}$, the resulting third-order intermodulation distortion will fall at f_{RX} and the receiver is potentially desensitized. The half-duplex blocker is more troublesome, as the duplexer RX filter rejection at that offset is lower than at the full-duplex offset. In that case, the out-of-band linearity (OOB-IIP3) requirement for the receiver can be related to the TX leakage power ($P_{TX,leak}$) and the blocker power at the receiver input (P_B) by

$$OOB - IIP3(\text{dBm}) = \frac{P_{TX,leak}(\text{dBm}) + 2P_B(\text{dBm}) - P_{IM3}(\text{dBm})}{2} \tag{1.5}$$

where P_{IM3} is the power in the intermodulation distortion that can be tolerated. Linearity requirement of the receiver will depend on the duplex RX filter out-of-

band rejection. Higher selectivity will attenuate the out-of-band blocker further and relax the linearity requirement.

1.2.6 Transceiver Design Specification

3GPP WCDMA specification requires meeting sensitivity at maximum TX power, while linearity and blocking are specified at 5 dB below maximum power [5]. This means that the receiver needs to meet noise figure and linearity requirements with very high TX leakage power. The TX leakage power $P_{TX,leak}$ at the receiver input is related to the maximum output power at the antenna $P_{TX,ANT}$ by

$$P_{TX,leak}(\text{dBm}) = P_{TX,ANT}(\text{dBm}) + L_{FE,TX}(\text{dB}) - ISOL_{TX-RX}(\omega_{TX})(\text{dB}) \quad (1.6)$$

where $L_{FE,TX}$ is the front-end TX insertion loss, which includes the RF switch, duplexer and transmission lines to route multiple bands on the board, that can be as high as 3 dB. For a Power Class 3 radio, the maximum output power could be 24 dBm at the antenna. With 3 dB of loss from the PA output to the antenna, and 52 dB of duplexer isolation at the TX frequency, the receiver will see TX leakage of -25 dBm (24 dBm + 3 dB $-$ 52 dB).

The sensitivity is given in terms of the total noise referred to the antenna input and the minimum signal-to-noise ratio (SNR_{min}) required for a given bit error rate by

$$Sensitivity(\text{dBm}) = N_{total}(\text{dBm}) + SNR_{min}(\text{dB}). \quad (1.7)$$

Where N_{total} includes total input referred noise generated within the receiver, noise of transmitter in receive band ($N_{TX}(\omega_{RX})$, noise due to reciprocal mixing of leaked transmit signal with receive LO phase noise (N_{rmix}), and effective noise due to second-order nonlinearity of the receiver ($IM2$). The sensitivity requirement for WCDMA is -106.7 dBm, with an SNR= -7.7 dB for a bit error rate not to exceed 0.001, thus N_{total} is equal to -99 dBm. Allowing for 1 dB margin to the specification, this becomes -100 dBm. With 4.0 dB front-end RX insertion loss, the maximum acceptable noise plus intermodulation distortion power, referred to transceiver input, is calculated to be -104 dBm. Allowing for 1 dB total

contribution of all the secondary effects other than the receiver noise, the receiver noise floor N_{RX} should be -105 dBm and the noise figure can be calculated from

$$N_{RX}(\text{dBm}) = NF - 174(\text{dBm/Hz}) + 10\log_{10}(BW(\text{Hz})), \tag{1.8}$$

to be 3 dB, where BW is the channel bandwidth (3.84 MHz for WCDMA). For equal contribution from the noise of transmitter in receive band $N_{TX}(\omega_{RX})$ and effective noise due to second-order nonlinearity of the receiver ($IM2$) of 0.4 dB, both (1.1) and (1.2) can be equated to -115 dB. Substitution in (1.1) and assuming a duplexer isolation in the RX band to be 45 dB shows that the noise power spectral density at the TX output should not exceed -136 dBm/Hz. While Substitution in (1.2) with -25 dBm TX leakage gives the IIP2 requirement of 59 dBm. The reciprocal mixing contribution can be set to 0.2 dB i.e $N_{rmix} = -117.47$ dBm in (1.3) giving a phase noise requirement for the RX LO to be -158.3 dBc/Hz.

The specification for cross-modulation distortion can be calculated from the 3GPP minimum intermodulation requirements. Requirements at the antenna input are specified with transmitted power of 19 dBm, CW jammer power of -43 dBm and desired signal power 10 dB above reference sensitivity. This corresponds to TX leakage power ($P_{TX,leak}$) of -30 dBm from (1.6), jammer power (P_{jam}) of -47 dBm, and desired signal power of -100.7 dBm at receiver input, with 4 dB front-end loss. To achieve -7.7 dB SNR, total noise plus distortion power cannot exceed -93 dBm at the receiver input. Noise power at the transceiver input is -104 dBm giving -93.36 dBm to the cross-modulation distortion. Substituting in (1.4) gives the IIP3 requirement of -6.8 dB

The out-of-band IIP3 requirements are derived from the out-of-band blocking requirements using a blocker signal at half the duplex spacing from the receive band. The desired signal power for the out-of-band blocker case is -103.7 dBm (3 dB above reference sensitivity) at the antenna or -107.7 dBm at the receiver input, assuming 4 dB front-end loss. With -107.7 dBm desired signal power, noise plus distortion power cannot exceed -100 dBm to achieve -7.7 dB SNR. The total noise power of the receiver referred to its input is -104 dBm leaving -102.2 dBm to distortion power. The out of band blocker power requirement is -15 dBm and assuming 25 dB of duplexer rejection at half-duplex frequency an out-of-band IIP3

of −3.9 dBm is needed from (1.5).

Table 1.1 summarizes the TX leakage related transceiver performance requirements and shows how these requirements change under degraded duplexer isolation performance. Up arrows indicate an increase in the corresponding parameter and down arrows indicate a decrease, while dashes indicate no change. It is clear now that there is a balance between the duplexer isolation requirement in the TX and RX bands on one side, and the receiver linearity, phase noise and transmitter RX band noise on the other side. A lower duplexer isolation tightens the noise requirement of the transmitter, and the linearity and phase noise requirements of the receiver. However, isolation in the RX band is more important than that of TX band, as it is more challenging to overcome RX band noise in the transceiver. While degraded TX band isolation drives higher linearity (IIP2 and IIP3) and RX LO phase noise requirements that can be achievable by burning a bit more current and using calibration as long as the degradation in isolation is not too high.

Table 1.1: TX leakage related transceiver design requirements.

	Typical Specification†	$ISOL_{TX-RX}(\omega_{TX})$ ↓ 5 dB	$ISOL_{TX-RX}(\omega_{RX})$ ↓ 5 dB
TX receive band noise	−136 dBm/Hz	—	↓ 5 dB
TX leakage RX IIP2	59 dBm	↑ 10 dB	—
RX LO Phase Noise	−158 dBc/Hz	↓ 5 dB	—
Triple-Beat RX IIP3	−6.8 dBm‡	↑ 5 dB	—
Out-of-band RX IIP3	−3.9 dBm	↑ 2.5 dB	—

† assumes $ISOL_{TX-RX} = 52$ dB in TX band and 45 dB in RX band,
FE rejection at half-duplex freq. = 25 dB, $L_{FE,TX} = 3$ dB, $L_{FE,RX} = 4$ dB,
RX small-signal NF = 3 dB.

‡ Sometimes specified as triple beat ratio (ratio of P_{jam} to XMD) = 46.4 dB.

1.3 Surface Acoustic Wave Duplexers

A surface acoustic wave (SAW) is a type of mechanical wave motion which travels along the surface of a solid material. These acoustic waves are often used in electronic devices. A basic SAW filter, shown in Figure 1.5(a), consists of two interdigital transducers (IDTs) on a piezoelectric substrate such as quartz. The IDTs consist of interleaved metal electrodes which are used to launch and receive the waves, so that an electrical signal is converted to an acoustic wave and then back to an electrical signal. The conversion process from electric to acoustic or acoustic to electric occurs by piezoelectricity, which is a property of many solid materials. In a piezoelectric material there is a mechanism which offers coupling between electrical and mechanical disturbances. Application of an electric field sets up mechanical stresses and strains. Conversely, a mechanical stress gives an electric field, and hence a voltage. The most common materials for SAWs are crystals of quartz, lithium niobate or lithium tantalate, which are all piezoelectric. Another important factor is because the material is anisotropic, the SAW properties depend on the orientation at which the substrate has been cut from the original crystalline material.

As shown in Figure 1.5(a), the teeth of the comb electrodes are arranged with a certain pitch between them, and a surface wave is excited most strongly when its wavelength λ is the same as the pitch of the electrode teeth. The center frequency of such a band-pass filter if given by

$$f_o = \frac{v}{\lambda} \tag{1.9}$$

Where v is the propagation velocity of the surface wave, which depends only on the substrate material and its cutting angle.

The IDT geometry is capable of almost endless variation, leading to a wide variety of devices. Figure 1.5(b) shows the basic structure of a SAW resonator. A high-Q resonator can be realized by generating a standing wave between comb electrodes (IDT). The resonator has a comb electrodes placed at the center and reflectors on both sides. A surface wave that has been excited by the comb electrodes is reflected by the reflectors, which then generates a standing wave. This

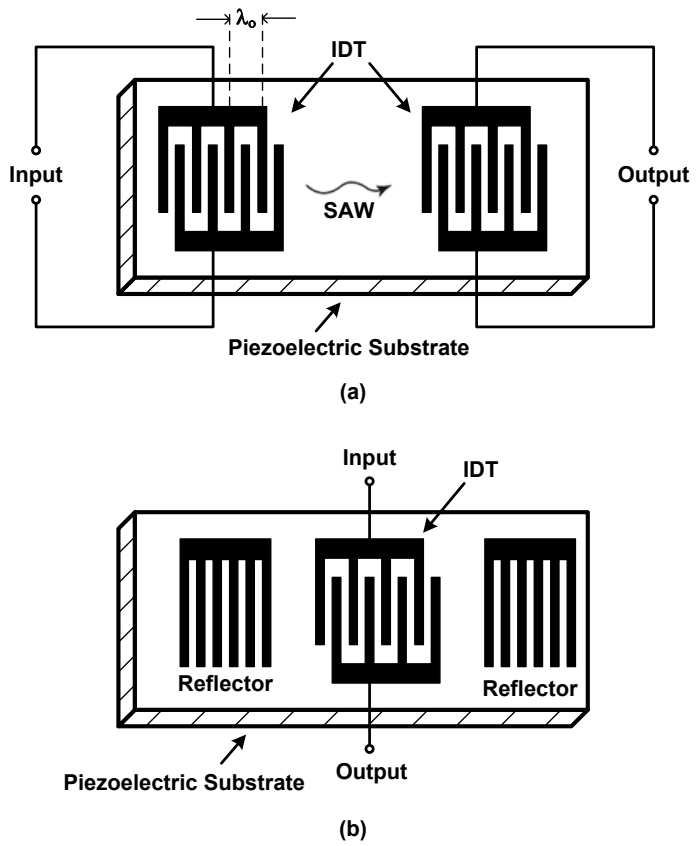


Figure 1.5: Basic structure of (a) SAW filter. (b) SAW resonator [7].

high-Q resonator is applied mainly to oscillators and narrowband filters.

SAW duplexer consists of two filters: a receiver filter and a transmitter filter, as shown in Figure 1.6(a). Each filter is implemented using ladder type filters made by connecting a number of one-port resonators in a ladder-like formation [8]. In order to connect two SAW filters at the antenna port, each filters impedance at the antenna port must be matched at its own pass band and become almost open (high impedance) at the other side filters pass band frequency. This is because when TX and RX filters are connected in parallel, the insertion loss of each filter increases due to the mutual interactions between them. Thus, in order to make the loss increases as small as possible, The TX filter input impedance must be designed to be large enough at the RX band and the RX filter input impedance must be designed large enough at the TX band. If this is not true, phase shifters, realized by transmission lines, are generally used to rotate the impedance on the

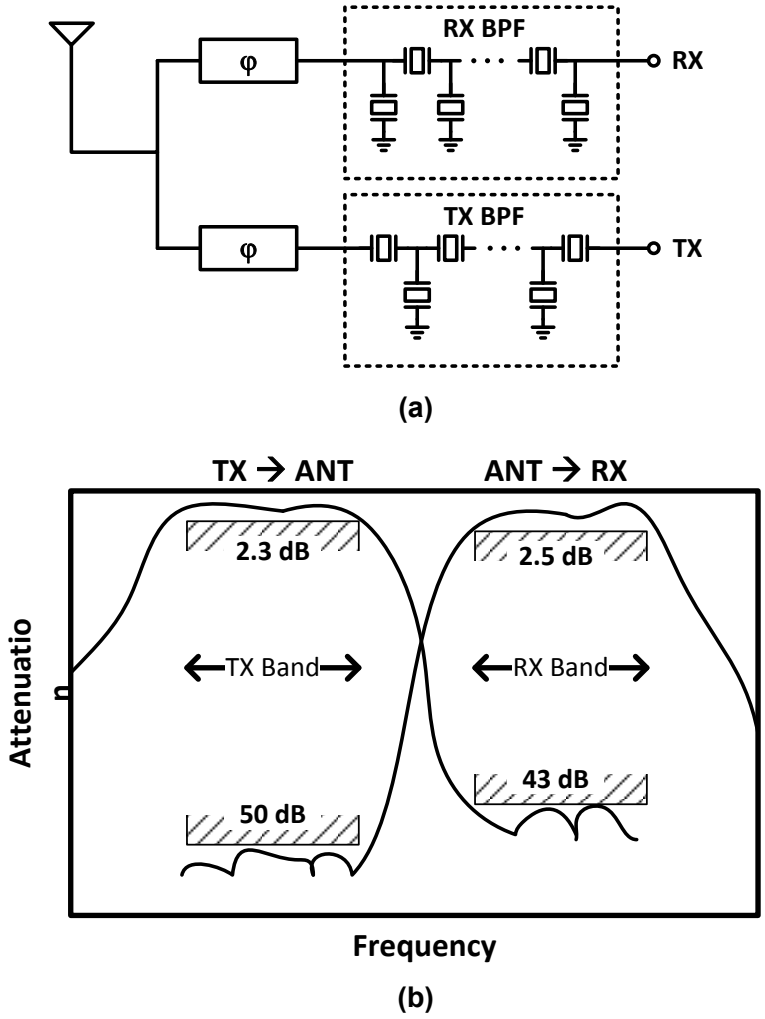


Figure 1.6: SAW duplexer (a) Structure. (b) Typical example of frequency response specifications [8, 9].

smith chart to the open area [10, 9].

Typical examples of frequency-response specifications for the antenna duplexer are also shown in Figure 1.6(b). The filters must have low insertion losses and a steep transition band. A summary of the performance for commercial SAW duplexers is shown in Table 1.2. As shown in the table, when the duplex spacing between the TX and RX bands decreases, the insertion losses increases. TX insertion loss ranges from 1.6 to 3 dB while RX insertion loss ranges from 2.1 to 3.8 dB. Isolation in the TX and RX bands is approximately 53 and 45 dB respectively.

Table 1.2: SAW duplexer performace for different bands.

Part number	Band	TX Band (MHz)		RX Band (MHz)		Duplex Spacing (MHz)	IL_{TX} (dB)	IL_{RX} (dB)	Isolation (dB)	
									TX Band	RX Band
SAYFP1G95AA0B00	1	1920	1980	2110	2170	190	1.6	2.1	53	44
SAYRJ1G88CE0B0A	2	1850	1910	1930	1990	80	3	3.3	54	50
SAYFH1G74CA0B0A	3	1710	1785	1805	1880	95	2.5	3.5	53	50
SAYRF1G73CA0F0A	4	1710	1755	2110	2155	400	1.6	2.3	53	50
SAYEV836MAC0F00	5	824	849	869	894	45	2	2.65	55	45
SAYFH2G53CC0F0A	7	2500	2570	2620	2690	120	2.2	3	53	48
SAYFH897MHC0F0A	8	880	915	925	960	45	2.5	3.3	53	50
SAYEV1G76AC0F00	9	1750	1785	1845	1880	95	1.75	2.2	51	40
SAYEV1G43AA0F00	11	1428	1448	1476	1496	48	2	2.2	53	43
SAYFP751MCC0F00	13	777	787	746	756	31	2.6	2.3	55	50
SAYFP763MAA0F00	14	788	798	758	768	30	2.8	3	54	53
SAYFP710MAA0F00	17	704	716	734	746	30	2	3	55	50
SAYFH822MCA0F0A	18	815	830	860	875	45	1.9	2.5	55	48
SAYFH806MCA0F0A	20	832	862	791	821	41	3	3.8	50	50

1.4 Motivation for the Design of Integrated Duplexer

Figure 1.7(a) shows the architecture for a modern multi-band transceiver, where highly selective SAW duplexers are used for FDD operation. Since the center frequency of such SAW filters depend on material properties and physically dimensions used to build them, the filter center frequency is not programmable and a different duplexer is needed for each band supported. A multi-pole switch selects the appropriate duplexer based on the operating frequency. Over forty bands are currently envisioned for mobile applications by the Third Generation Partnership Project (3GPP) standardization union, and for every band of operation a dedicated input and its corresponding duplexer are needed. This adds to the system cost and complexity, which is a serious concern for multiband mobile transceivers that require a highly integrated solution for cost reduction. A tunable integrated duplexer is highly desirable to reduce system cost and complexity.

Figure 1.7(b) shows an alternative implementation that greatly reduces the

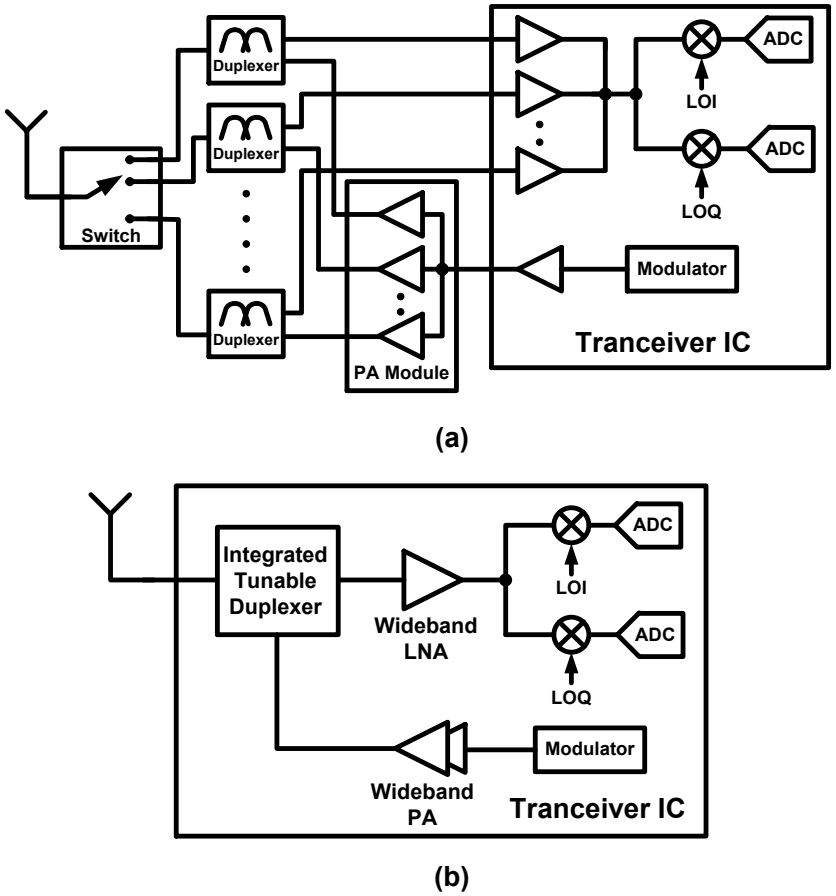


Figure 1.7: (a) Current multiband transceiver architecture based on off-chip duplexers (b) Future architecture based on integrated tunable duplexer.

cost and system complexity by replacing the bank of duplexers with an integrated tunable duplexer. An integrated tunable duplexer based on electrical balance of a hybrid transformer was introduced in [11]. Relying on electrical balance rather than frequency selectivity makes duplexer integration along with the rest of the CMOS RF IC possible, as it does not require any high-Q passives that are hard to implement in a CMOS process. This duplexer, which can achieve TX-RX isolation at an arbitrary frequency, enables a true fully integrated and reconfigurable multiband transceiver. The goal of this research is to implement such a tunnable integrated duplexer with a performance comparable to current off-chip implementations.

1.5 Hybrid Transformer Duplexer Operation

A duplexer should allow both the transmitter and receiver to share a common transmission medium, which is air in the case of wireless communication, while providing high isolation between them. A similar functionality was implemented in early telephony systems using hybrid transformers. In that case the common transmission medium was the phone line that extends from the central office to the subscriber. The need for hybrids came from the nature of old analog telephone service lines, where the two audio directions are combined on a single two-wire pair. A telephone hybrid is placed at the end of a subscriber line of the public switched telephone network (PSTN) and converts between two-wire and four-wire forms of bidirectional audio paths. The fundamental principle is shown in Figure 1.8. The microphone signal is applied to both the telephone line and a balancing network that is designed to have the same impedance as the line. The speaker signal is derived by subtracting the two, thus canceling the sent audio. This way, Hybrids are able to reduce the volume of microphone output that feed back to the earpiece. Without this, the phone users own voice would be louder in the earpiece than the other party's.

Another case that required such conversion was when repeaters were introduced in a two-wire circuit as shown in Figure 1.9. This was a frequent practice at

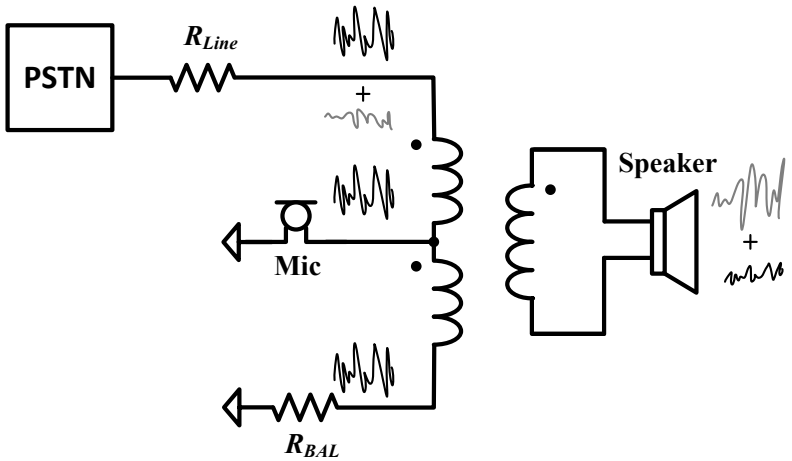


Figure 1.8: Telephone hybrid operation.

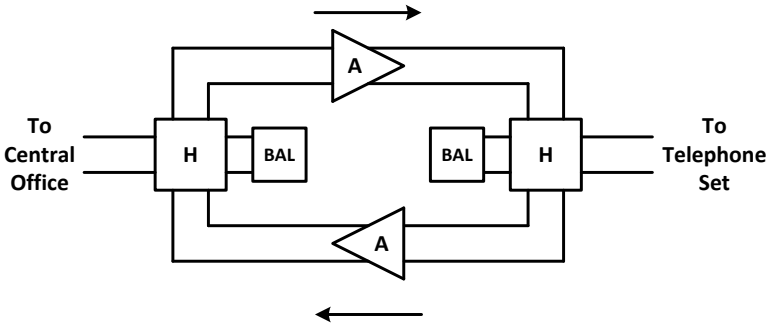


Figure 1.9: Two-wire to four-wire hybrid repeaters.

early 20th century telephony. The repeater includes two-wire to four-wire hybrid transformers, the four-wire outputs of which are connected through two amplifiers for amplifying the telephone signals in opposite directions. Without hybrids, the output of one amplifier feeds directly into the input of the other, resulting in oscillations. By using hybrids, the outputs and inputs are isolated, resulting in proper 2-wire repeater operation.

A hybrid transformer has several desirable properties: a biconjugacy between alternate sets of ports, i.e. alternate sets of ports are isolated, an impedance match at each port, and the ability to split power in any desired proportion between two receiving ports [12].

In the usual arrangement, four external circuits are connected together by means of the hybrid transformer, designated as Ports A, B, C, and D as shown in Figure 1.10. If we assume an ideal transformer, and if Ports B and D are properly terminated, no signal from Port A arrives at Port C; thus A and C are conjugate ports. If Ports A and C are properly terminated as well, Ports B and D are also conjugate. The analysis of the operation of the circuit can be simplified by assuming that the port conjugate to the sending port is open or shorted, whichever is more convenient.

The hybrid transformer can be used as an RF duplexer when port A connects to the PA, port B connects to the antenna, port C connects to the LNA and the fourth port D connects to a termination, which is called the balance port [13]. In this case the TX-RX isolation is merely a function of the matching between the antenna impedance and the balancing impedance. This condition, which is unlike

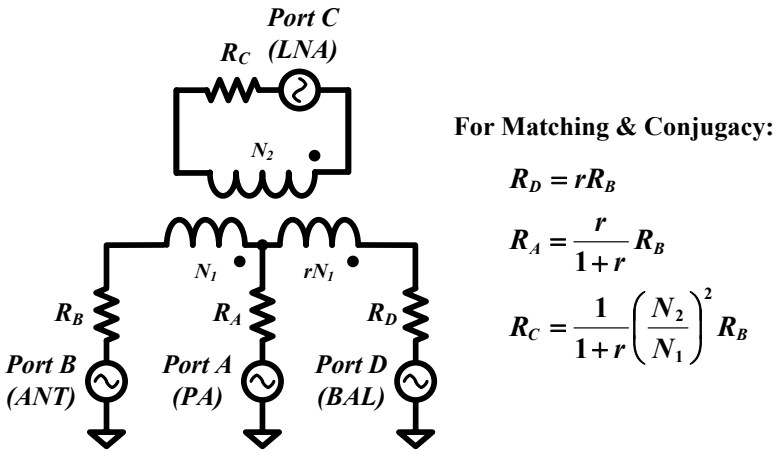


Figure 1.10: Hybrid transformer [12].

the external duplexers that rely on selectivity, can be implemented on-chip, where good resolution in the balance network programmability can be achieved.

When the PA is transmitting power, the LNA side is isolated and can be assumed shorted; by transformer action there will be no voltage drop on the primary windings, so the PA power is split between the antenna and the balance port with a ratio r, which is the tapping ratio of the primary windings. Thus, the insertion loss in the transmit path can be given as:

$$IL_{TX} = 10\log_{10}\left(\frac{1+r}{r}\right) \tag{1.10}$$

By reciprocity, when the antenna is receiving power, the same portion $r/(1+r)$ will go to the PA and the remaining part $1/(1+r)$ will go to the LNA due to conjugacy. Thus the insertion loss in the receive path can be given as:

$$IL_{RX} = 10\log_{10}(1+r) \tag{1.11}$$

These two equations quantify the trade-off between IL_{TX} and IL_{RX} as shown in Figure 1.11. Lower insertion loss in one path can be achieved only at the cost of higher loss in the other by skewing the transformer in favor of one of them. When the primary windings are tapped in the center, $r = 1$ (symmetric case), the insertion loss is 3 dB for the receiver and the transmitter. A practical implementation suffers an additional Ohmic loss, due to the non-zero resistivity of the transformer windings. The more than 3 dB insertion loss of a duplexer using

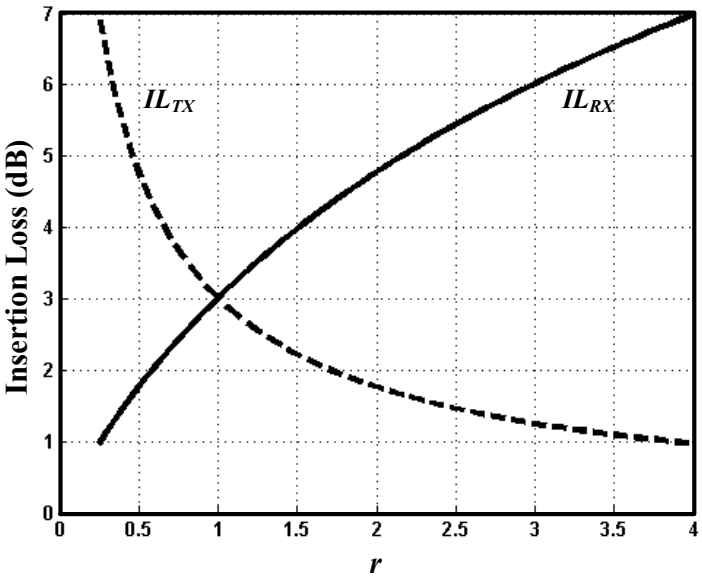


Figure 1.11: Insertion loss trade-off of ideal hybrid transformer-based duplexer.

hybrid transformers is a major limitation that we will try to get around by using a power recycler in the balance port as will be discussed in Chapter 2.

When every port of the hybrid transformer is terminated with the proper impedance given by

$$\begin{aligned} R_{LNA} &= \frac{1}{1+r}\left(\frac{N_2}{N_1}\right)^2 R_{ANT} \\ R_{BAL} &= r R_{ANT} \\ R_{PA} &= \frac{r}{1+r} R_{ANT} \end{aligned} \tag{1.12}$$

all ports are matched and opposite ports are isolated i.e. LNA and PA are isolated, and the antenna and balance resistor are isolated. Thus, the ideal S-parameters of the hybrid transformer duplexer can be written as[14]:

$$\begin{pmatrix} b_{PA} \\ b_{LNA} \\ b_{ANT} \\ b_{BAL} \end{pmatrix} = \frac{1}{\sqrt{1+r}} \begin{pmatrix} 0 & 0 & \sqrt{r} & 1 \\ 0 & 0 & 1 & -\sqrt{r} \\ \sqrt{r} & 1 & 0 & 0 \\ 1 & -\sqrt{r} & 0 & 0 \end{pmatrix} \begin{pmatrix} a_{PA} \\ a_{LNA} \\ a_{ANT} \\ a_{BAL} \end{pmatrix} \tag{1.13}$$

where $b_x = \frac{V_x^-}{\sqrt{R_x}}$ and $a_x = \frac{V_x^+}{\sqrt{R_x}}$; x is PA, LNA, ANT or BAL. When we have an antenna impedance $Z_{ANT}(\omega)$ and a balance impedance, $Z_{BAL}(\omega)$, and with power

incident from the PA port, a simple S-matrix manipulation can provide a general expression for TX-RX isolation as

$$\begin{aligned} ISOL_{TX-RX} &= 10\log_{10}\Big(\frac{|a_{PA}|^2}{|b_{LNA}|^2}\Big) \\ &= 20\log_{10}|\Gamma_{ANT}(\omega)-\Gamma_{BAL}(\omega)| - 20\log_{10}\big(\frac{1+r}{\sqrt{r}}\big) \end{aligned} \tag{1.14}$$

where

$$\Gamma_{ANT}(\omega) = \frac{Z_{ANT}(\omega)-R_o}{Z_{ANT}(\omega)+R_o} \tag{1.15}$$

and

$$\Gamma_{BAL}(\omega) = \frac{Z_{BAL}(\omega)-rR_o}{Z_{BAL}(\omega)+rR_o}. \tag{1.16}$$

When $\Gamma_{ANT} \approx \Gamma_{BAL}$, high isolation can be achieved. If Γ_{ANT} and Γ_{BAL} are frequency independent, or have the same frequency dependence, wide band isolation can be achieved. Figure 1.12 compares (1.14) to simulation for three different cases. For simulation, a lumped element model that captures the finite quality factor and magnetic coupling was used for the transformer ($L_1 = L_2 = 2$ nH, $r = 1$, $k = 0.8$ and $Q = 16$). Good agreement between simulation and analysis is shown, suggesting that isolation is more sensitive to the balance between the antenna and balance network rather than the real transformer parameters. In the first case, both the antenna and balance impedance are purely resistive, thus wide bandwidth isolation is achievable. In the second case, the antenna impedance, as seen at the duplexer port, has a board capacitance C_{brd}, bondwire inductance L_{bw}, and pad capacitance C_{pad} included, giving rise to frequency dependent isolation. In the last case, a more realistic planar inverted F antenna (PIFA) model was used [15], the antenna impedance has its own frequency dependence, not just 50 Ω resistance, further limiting the isolation bandwidth. In summary to achieve high isolation over a wide bandwidth will depend upon the antenna impedance versus frequency characteristic as compared to that of the balance network. As a duplexer should be robust enough to work with any antenna having arbitrary frequency dependence, accurate replication of the antenna impedance dependence in the balance network is hard to achieve, and thus maintaining high isolation in both the TX and RX bands can be quite challenging. Moreover, since a mobile

phone antenna impedance varies depending upon surrounding environment and human interaction, the balance network should be designed to account for that variation and track it, otherwise isolation will be compromised.

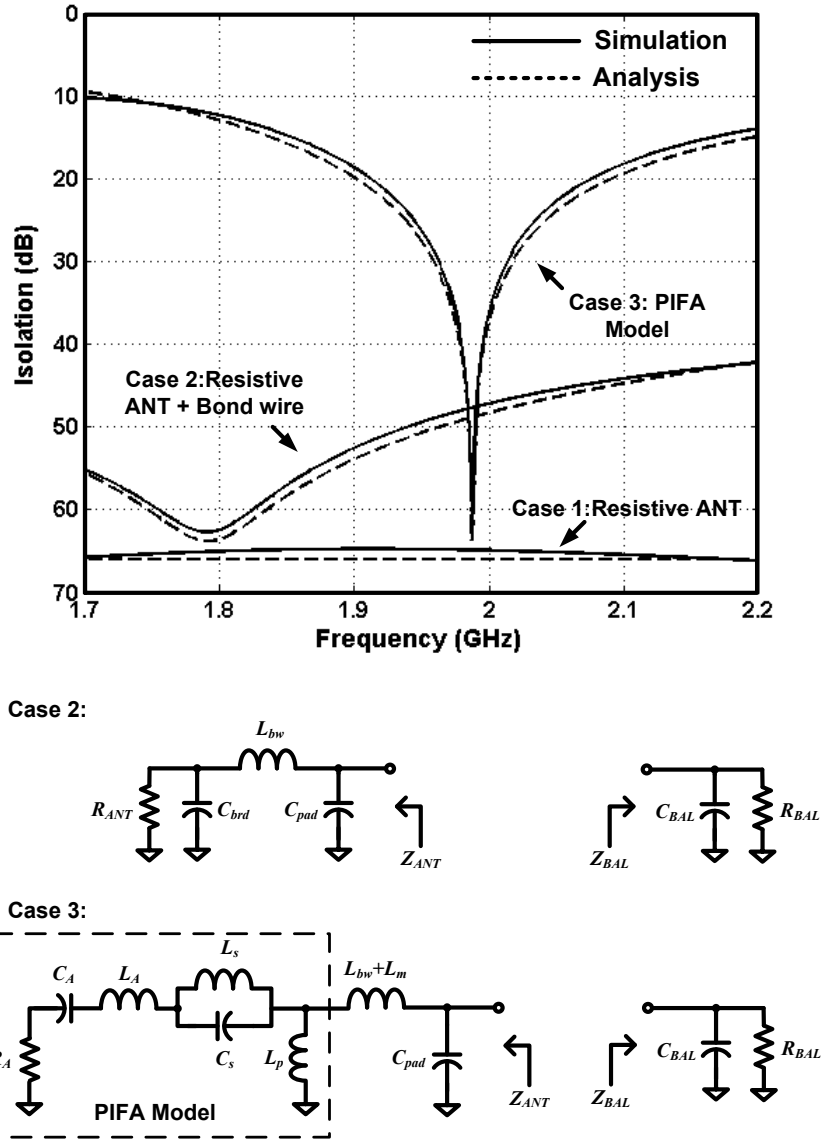


Figure 1.12: TX-RX isolation bandwidth dependence on antenna impedance characteristics (Case 1: $Z_{ANT} = 50\ \Omega$, $Z_{BAL} = 49.9\ \Omega$. Case 2: $R_{ANT} = 50\ \Omega$, $C_{brd} = 450$ fF, $C_{pad} = 240$ fF, $L_{bw} = 1.2$ nH, $R_{BAL} = 47\ \Omega$, $C_{BAL} = 180$ fF. Case 3: $R_A = 13\ \Omega$, $C_A = 2.7$ pF, $L_A = 1.9$ nH, $L_s = 1.8$ nH, $C_s = 8$ pF, $L_p = 3.2$ nH, $R_{BAL} = 50\ \Omega$, $C_{BAL} = 5$ fF).

Unlike frequency selective duplexers, an electrical balance duplexer does not provide sufficient rejection for out-of-band blockers as the transfer function from the antenna to the LNA input is relatively wideband. The out-of-band blocker requirements for WCDMA and LTE standards is −15 dBm, and assuming 3 dB minimum hybrid transformer duplexer insertion loss, that will be −18 dBm at the receiver input. This level might be not too high to cause any compression issue at the LNA and could be rejected in the baseband filter. However, when this blocker occurs at half or twice the duplex spacing from the receive band and mixes with TX leakage due to third-order front-end nonlinearity, the receiver would likely be desensitized as discussed in section 1.2. Without additional attenuation for out-of-band blockers the out-of-band IIP3 linearity requirement can be estimated from (1.5) to be 18.1 dBm instead of the −3.9 dBm currently required under 25 dB of duplexer rejection at half-duplex frequency. This is certainly very challenging even when employing LNA linearization techniques as in [16, 17]. Even if LNA linearity can be achieved, desensitization due to reciprocal mixing between the blocker and the LO phase noise will remain an issue and additional blocker filtering or blocker tolerant receiver architecture becomes necessary. Many such techniques have been proposed recently, including N-path filtering [18, 19], mixer-first receivers [20, 21] and feed-forward blocker cancellation [22].

In [13], a successful demonstration of an RF duplexer using a hybrid autotransformer was shown, Figure 1.13 . An autotransformer is a special case of the hybrid transformer that can be implemented as a center-tapped differential inductor, and hence can be less lossy than a two winding transformers. Indeed by tapping the autotransformer off the center and in favor of the transmitter, a low TX insertion loss of 2.5 dB was achieved. Also using a noise matched LNA, the receiver noise figure was 5 dB. However the low loss of the auto-transformer comes at the cost of a strong common-mode coupling. When balance is achieved between the balance network and antenna, same voltage swing appears across them and the differential LNA should reject that swing. However at full transmit power that common mode swing can reach 5 V easily causing oxide breakdown for the LNA input devices. Because of that issue, all measurements reported were for small-signal

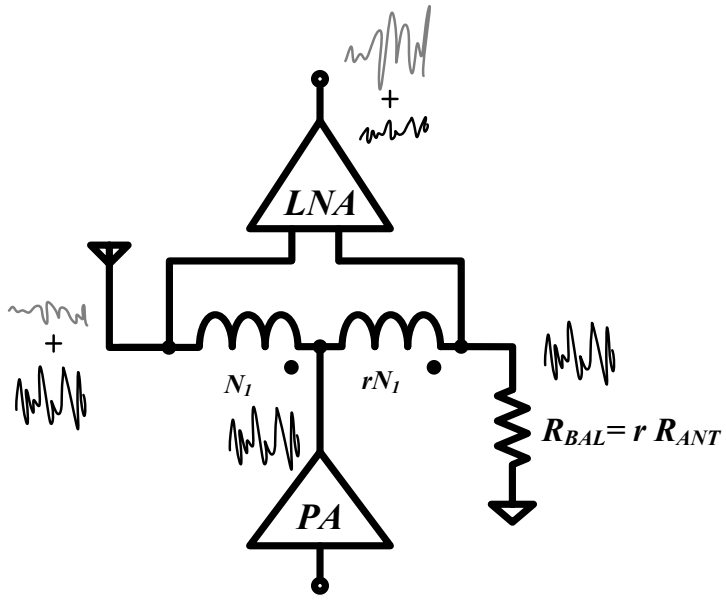


Figure 1.13: Hybrid autotransformer duplexer [13].

operation. Furthermore, wideband isolation was only possible because the antenna impedance was assumed to be fixed at 50 Ω and no realistic antenna impedance frequency dependence was taken into consideration. Also no measurements were carried out with antenna mismatch as the balance network did not have sufficient range to track antenna impedance changes.

1.6 Dissertation organization

The goal of this research is to make the integration of an RF duplexer in a CMOS product more practical and appealing for industry adoption by solving many of the current shortcomings of the hybrid transformer based duplexer. Chapter 2 deals with the high power loss in the hybrid transformer due to TX power splitting between the antenna and the balance network. An RF-DC converter is proposed to replace the passive balance network and recycle the power back to dc. To maintain the isolation, the input impedance of such a balance network replacement should be accurately controlled. A class-E rectifier with electronic tuning will be demonstrated for this task. Chapter 3 is concerned with improving

the common-mode isolation of the hybrid transformer. Due to capacitive coupling between the transformer windings, a strong common-mode TX signal couples to the RX side causing linearity issues. A differential implementation of the hybrid transformer is introduced to allow wideband common mode isolation. In Chapter 4, the sensitivity of the TX-RX isolation to the antenna impedance is solved by introducing an antenna impedance tracking loop. This loop detects any variation in the antenna impedance and corrects the balance network impedance accordingly to maintain high isolation.

Chapter 2

Power Recovery Using an RF-DC Converter

In a hybrid transformer duplexer, a portion of the transmit power is lost to the passive balance network. This limitation increases the transmitter insertion loss and would result in reduced system efficiency and battery lifetime. In this chapter, we propose an RF-DC converter that recycles the power lost in the balance load. Unfortunately, due to the highly nonlinear nature of the rectification process, the input impedance of a rectifier depends on the input power as well as loading conditions. The transmitter-to-receiver isolation ($\mathrm{ISOL_{TX\text{-}RX}}$) is highly dependent on the input impedance of the rectifier, since any power reflected will leak back to the LNA side. An improved RF-DC converter based on a class-E rectifier with wide dynamic range input matching is presented. This allows recycling the power lost in the balance load while maintaining the required constant input impedance over a wide range of input powers to achieve the desired transmit-to-receive port isolation. The input impedance is controlled by two varactor diodes to compensate for impedance changes with RF input power and DC loading conditions. The RF-DC converter achieved a peak efficiency of 60% and an $\mathrm{S_{11}}$ less than -20 dB over 12 dB input RF power range and 2.5 V to 4.2 V operating battery voltage at 800 MHz. An analytical model for input impedance and efficiency was developed and shown to match simulation and measurement results. In Section 2.1, the use of an RF-DC converter in conjunction with hybrid transformer based inte-

grated duplexer is shown and important duplexer metrics are linked to RF-to-DC converter performance. Section 2.2 provides the basic theory of operation of the proposed class-E rectifier, and derives the dependence of its input impedance on input power. Section 2.3 explains the efficiency improvement associated with the technique proposed. And finally, Section 2.4 discusses the measurement results.

2.1 Power Recycling in Hybrid Transformer Duplexer

Figure 2.1(a) illustrates the hybrid transformer duplexer with the balance port implemented with a conventional passive load. A major disadvantage of that topology is the power loss in the balance resistor. The only way to reduce this loss is to tap the primary windings closer to the antenna i.e. higher r, but this comes at the expense of higher insertion loss in the receiver path. The insertion losses in the transmit (IL_{TX}) and receive (IL_{RX}) paths were derived in Chapter 1 and are given by:

$$IL_{TX} = 1 + \frac{1}{r} \tag{2.1}$$

$$IL_{RX} = 1 + r \tag{2.2}$$

A better choice would be replacing the balance resistor with an RF-DC converter that provides the same input impedance while converting most of the RF power back to DC, instead of being wasted as heat in the balance resistor. This is shown in Figure 2.1(b). With the RF-to-DC converter in place, the effective IL_{TX} can be written as

$$\begin{aligned} IL_{TX} &= \frac{P_{PA} - \eta_{RF-DC}\eta_{PA}P_{BAL}}{P_{ANT}} \\ &= 1 + \frac{1}{r} - \frac{\eta_{RF-DC}\eta_{PA}}{r} \end{aligned} \tag{2.3}$$

where η_{PA} and η_{RF-DC} are the power conversion efficiencies of the power amplifier and RF-to-DC converter respectively. Equations (2.1) to (2.3) are plotted in Figure 2.2 showing good improvement in insertion loss with power recycling.

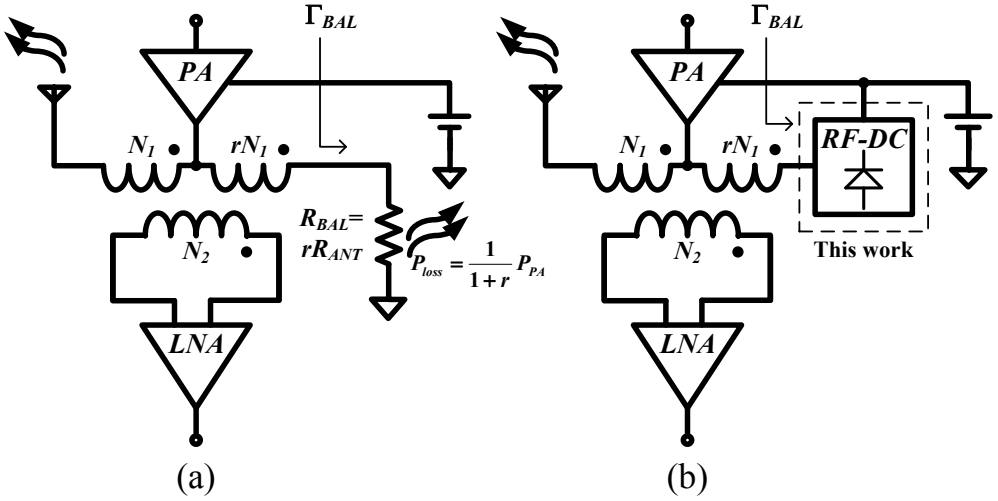


Figure 2.1: Hybrid transformer based duplexer (a) Conventional (b) With power recycling.

The transmitter-to-receiver isolation ($ISOL_{TX-RX}$) is highly dependent on the input impedance of the rectifier, since any power reflected will leak back to the LNA side. From (1.14) and assuming matched antenna, the $ISOL_{TX-RX}$ can be related to the reflection coefficient at the balance port (Γ_{BAL}) by:

$$ISOL_{TX-RX}(\text{dB}) = -\Gamma_{BAL}(\text{dB}) + 20\log_{10}(\frac{1+r}{\sqrt{r}}) \tag{2.4}$$

where r is the tapping ratio of the windings. Equation (2.4) shows that an RF-DC converter with high efficiency and near ideal matching is needed; for example when $r = 1$, to get $ISOL_{TX-RX}$ of 50 dB, Γ_{BAL} has to exceed -44 dB. This need for an RF-to-DC converter with high efficiency and excellent impedance matching motivated this work.

Other applications that require well controlled rectifier input impedance include: rectennas (rectifying antennas) [23], resonant DC-DC converters [24], and power recycling in outphasing power amplifiers [25, 26]. For the rectenna case, the impedance mismatch between the antenna and the rectifier causes a portion of the available power to be reflected, reducing conversion efficiency. In a resonant DC-DC converter, which is formed from an inverter followed by a rectifier, the inverter operation and efficiency is highly dependent on the load resistance offered by the rectifier. In energy recycling outphasing power amplifiers, the rectifier replaces

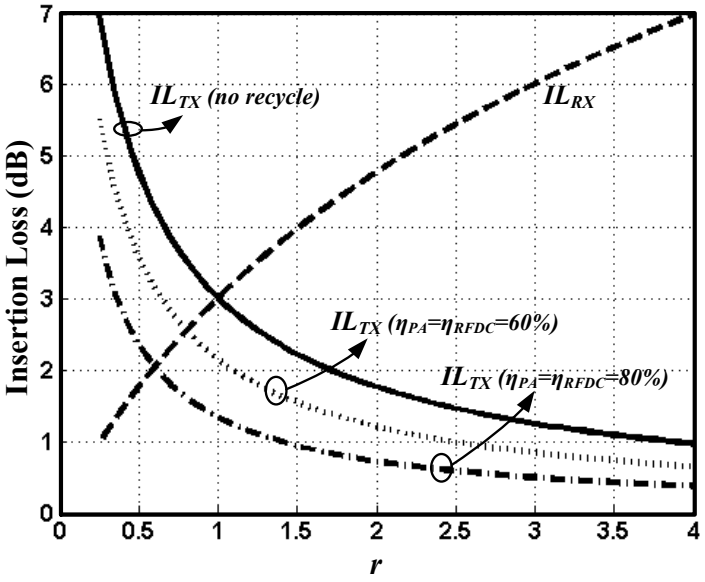


Figure 2.2: Insertion loss with and without power recycling.

the isolation resistor in the power combiner. In this case, the rectifier should offer a fixed impedance for isolation between, and proper operation of, the individual power amplifiers, as well as achieving maximum recycling efficiency.

A resistance compression network was introduced in [24, 26] to reduce the variation in input impedance seen from a rectifier. But the amount of compression is limited, especially if the input impedance has a reactive part, as most high frequency rectifiers do. In [27], a rectifier for RFID applications made use of a voltage multiplier with a reconfigurable number of stages to increase the dynamic range. Tighter control on the input impedance and higher power tolerance are required for power recycling applications. In the next sections, we demonstrate a technique that can be applied to class-E rectifiers to improve matching over a wide range of input power and loading conditions. We utilize the dependence of the input impedance of a class-E rectifier on some capacitance, by replacing these capacitors with varactor diodes to achieve a controlled impedance.

2.2 Class-E Rectifier Analysis

A class-E rectifier is the dual of a class-E power amplifier. It was first introduced in [28] as a new rectifier topology capable of high frequency high efficiency RF-DC conversion. This original topology suffers from a variable input impedance as a function of input power. An analytical model for this dependence is first derived, and then a technique to compensate for it is proposed.

To simplify the analysis of the class-E rectifier, shown in Figure 2.3(a), the following approximations can be made:

a. The diode DC I-V characteristics can be approximated as piecewise linear, with turn on voltage V_D, forward resistance R_D, and infinite reverse resistance.

b. Diode capacitance C_D is assumed linear, i.e. voltage independent, and is included in C.

c. All inductances from packaging and wiring are negligible.

d. The choke impedance at the fundamental and harmonics is much higher than

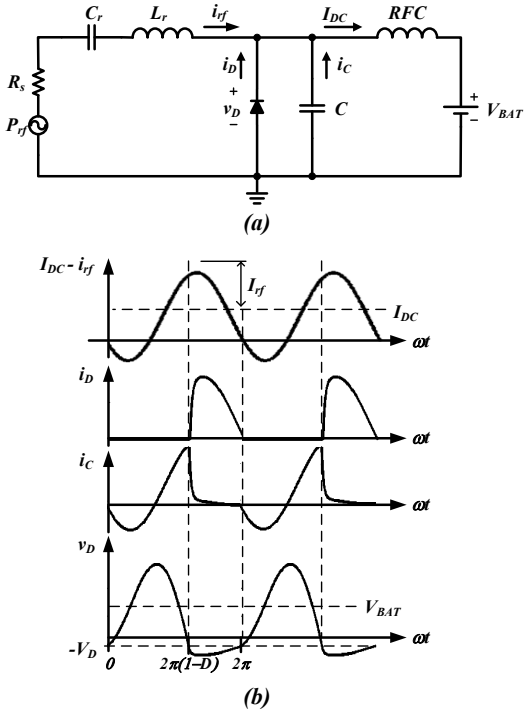


Figure 2.3: (a) Schematic of a class-E rectifier, (b) Ideal waveforms (D represents the diode conduction duty cycle).

the impedance of C, allowing only DC current.

e. The series resonance section formed by L_r and C_r offers a low impedance at the fundamental frequency, only allowing RF current at the fundamental frequency to flow, while all other harmonics flow in C.

With these assumptions, the waveforms in Figure 2.3(b) can be explained. The current in the parallel combination of the diode and capacitor C is the sum of the RF input current and the DC current in the choke (RFC). When the diode is *on*, the current is almost entirely flowing in the diode. This continues until the diode current reaches zero and the diode turns *off*, then the current start flowing in C and the voltage across it builds up to a peak, then decreases. When it reaches $-V_D$ the diode conducts again and the cycle repeats.

Figure 2.4 shows the simplified circuit model for the rectifier and its two modes of operation: diode *on* and diode *off*. In the diode *off* state ($0 \leq \omega t \leq 2\pi(1-D)$), we can write

$$C\frac{dv_D}{dt} = I_{rf}\sin(\omega t + \varphi) - I_{DC}. \tag{2.5}$$

Solving (2.5) using the initial condition $v_D(\omega t = 0) = -V_D$, we obtain

$$v_D(t) = \frac{I_{rf}}{\omega C}\cos\varphi(1 - \cos\omega t + \tan\varphi\sin\omega t) - \frac{I_{DC}}{C}t - V_D \quad ;0 \leq \omega t \leq 2\pi(1-D) \tag{2.6}$$

and using the condition $v_D(\omega t = 2\pi(1-D)) = -V_D$ in (2.6) we get

$$I_{DC} = \frac{I_{rf}\cos\varphi}{2\pi(1-D)}(1 - \cos 2\pi D - \sin 2\pi D\tan\varphi). \tag{2.7}$$

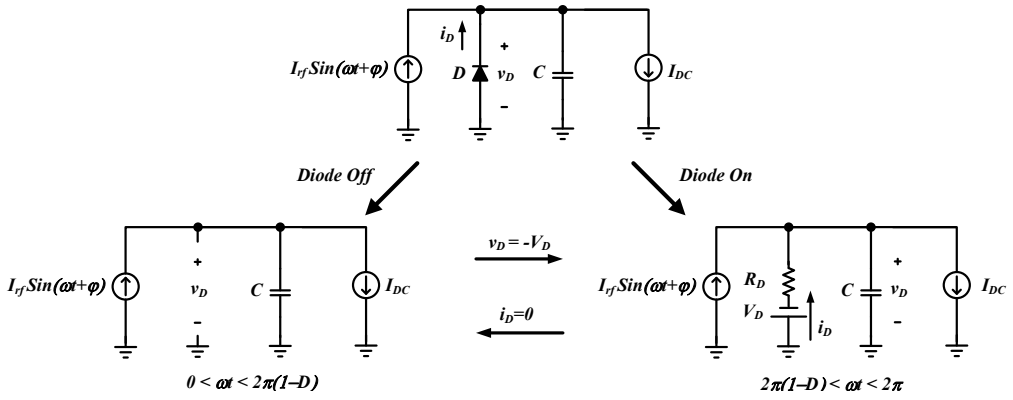


Figure 2.4: Class-E rectifier equivalent circuit.

In the diode *on* state ($2\pi(1-D) \leq \omega t \leq 2\pi$), we can write

$$CR_D\frac{dv_D}{dt} + v_D = I_{rf}R_D\sin(\omega t + \varphi) - I_{DC}R_D - V_D. \tag{2.8}$$

Solving (2.8) for $v_D(t)$, we obtain

$$\begin{aligned} v_D(t) = V_c e^{\frac{-\omega t}{\chi}} + \frac{I_{rf}R_D\cos\varphi}{1+\chi^2}\big[(1+\chi\tan\varphi)\sin\omega t + (tan\varphi - \chi)\cos\omega t\big] \\ - I_{DC}R_D - V_D \qquad\qquad ; 2\pi(1-D) \leq \omega t \leq 2\pi \end{aligned} \tag{2.9}$$

where $\chi = \omega C R_D$ and using the condition $v_D(\omega t = 2\pi(1-D)) = v_D(\omega t = 2\pi) = -V_D$ in (2.9) we obtain

$$V_c = \left[I_{DC}R_D - \frac{I_{rf}R_D\cos\varphi}{1+\chi^2}(\tan\varphi - \chi)\right] e^{\frac{2\pi}{\chi}} \tag{2.10}$$

and

$$\tan\varphi = \frac{\kappa(1-\cos 2\pi D) - 2\pi(1-D)\Big[(\sin 2\pi D + \chi\cos 2\pi D)e^{\frac{-2\pi D}{\chi}} - \chi\Big]}{\kappa\sin 2\pi D + 2\pi(1-D)\Big[1 - (\cos 2\pi D - \chi\sin 2\pi D)e^{\frac{-2\pi D}{\chi}}\Big]} \tag{2.11}$$

where

$$\kappa = (1+\chi^2)(1 - e^{\frac{-2\pi D}{\chi}}). \tag{2.12}$$

The average voltage across the diode $< v_D >$ should be equal to the battery voltage V_{BAT}, since there is no DC drop across the RF choke, i.e.

$$< v_D >= \frac{1}{2\pi}\int_0^{2\pi} v_D(t)\, d\omega t = V_{BAT}. \tag{2.13}$$

Using (2.6), (2.7), (2.9) and (2.10) in (2.13), we can relate the diode conduction duty cycle D to other circuit parameters in

$$\begin{aligned} & I_{rf}\cos\varphi\Bigg\{\frac{1}{\chi}\big[2\pi(1-D) + \sin 2\pi d + \tan\varphi(1-\cos 2\pi D)\big] \\ & - \frac{1}{1+\chi^2}\Big[\chi\big((\tan\varphi - \chi)e^{\frac{2\pi D}{\chi}} + \chi - \tan\varphi\cos 2\pi D\big) + 1 - \cos 2\pi D \\ & \qquad - (\tan\varphi - \chi)\sin 2\pi D\Big] \\ & - \frac{1}{1-D}(1 - \cos 2\pi D - \tan\varphi\sin 2\pi D)\Big[D + \frac{\pi(1-D)^2}{\chi} - \frac{\chi}{2\pi}\big(e^{\frac{2\pi D}{\chi}} - 1\big)\Big]\Bigg\} \\ & = \frac{2\pi}{R_D}(V_{BAT} + V_D) \end{aligned} \tag{2.14}$$

which, when solved with (2.11), completely defines the v_D waveform.

The rectifier input impedance can be defined at the fundamental frequency, and is related to v_D fundamental component by

$$v_{Dfund} = I_{rf} R_{in} \sin(\omega t + \varphi) - \frac{I_{rf}}{\omega C_{in}} \cos(\omega t + \varphi). \tag{2.15}$$

Thus R_{in} and X_{in} are given by

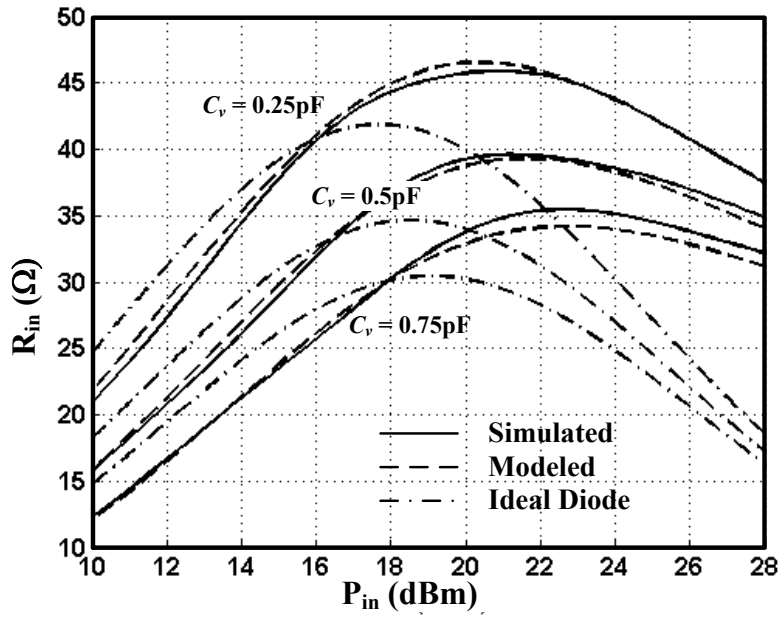
$$R_{in} = \frac{1}{\pi I_{rf}} \int_0^{2\pi} v_D \sin(\omega t + \varphi)\, d\omega t \tag{2.16}$$

$$X_{in} = -\frac{1}{\omega C_{in}} = \frac{1}{\pi I_{rf}} \int_0^{2\pi} v_D \cos(\omega t + \varphi)\, d\omega t. \tag{2.17}$$

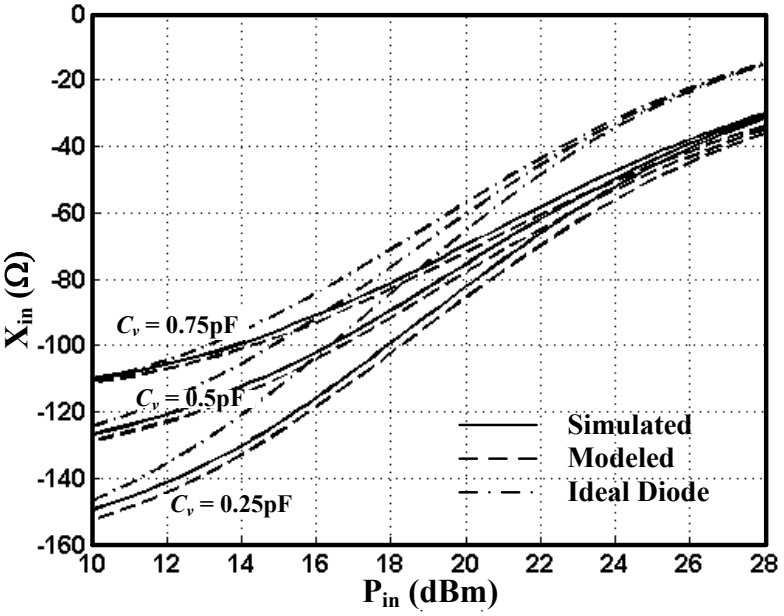
These equations can be solved numerically to find the input impedance. Setting R_D and V_D to zero results in identical closed-form relations from [29], which assumed an ideal diode model.

Figure 2.5 and Figure 2.6 compare the simulated values for the input impedance with the relations derived here and those from [29] with an ideal diode model. It shows the variation of the input impedance with RF power and battery voltage at 800 MHz for different values of capacitor C_v. For the simulation, the SPICE model of a packaged Schottky diode SMS3923-011LF from Skyworks was used, and a capacitor with fixed part C_f and variable part C_v was added in parallel with the diode. Our proposed model shows excellent agreement in the real and imaginary part of the input impedance with simulation over the entire 18 dB input power range and the voltage range for a Li-ion battery typically used in mobile phones. Results derived from [29] deviate from simulated values, especially for high power as the role of diode forward resistance becomes significant. The error in [29] is also larger at smaller battery voltages as V_D becomes comparable to V_{BAT} and can no longer be neglected.

To control the input impedance, capacitor C_v can be replaced with a varactor diode, whose bias voltage can be controlled to maintain constant input resistance, while the reactive part of the input impedance can be nulled by a second varactor diode replacing capacitor C_r in Figure 2.3(a). This combination allows the input impedance to remain constant despite input power and battery voltage variations.



(a)



(b)

Figure 2.5: Input impedance variation as a function of input RF power for different C_v (a) Real part (R_{in}), (b) Imaginary part. (X_{in}) ($V_D = 0.4$ V, $R_D = 10\ \Omega$, $C_D = 0.55$ pF, $V_{BAT} = 3.6$ V, $C_f = 0.4$ pF, $f = 800$ MHz)

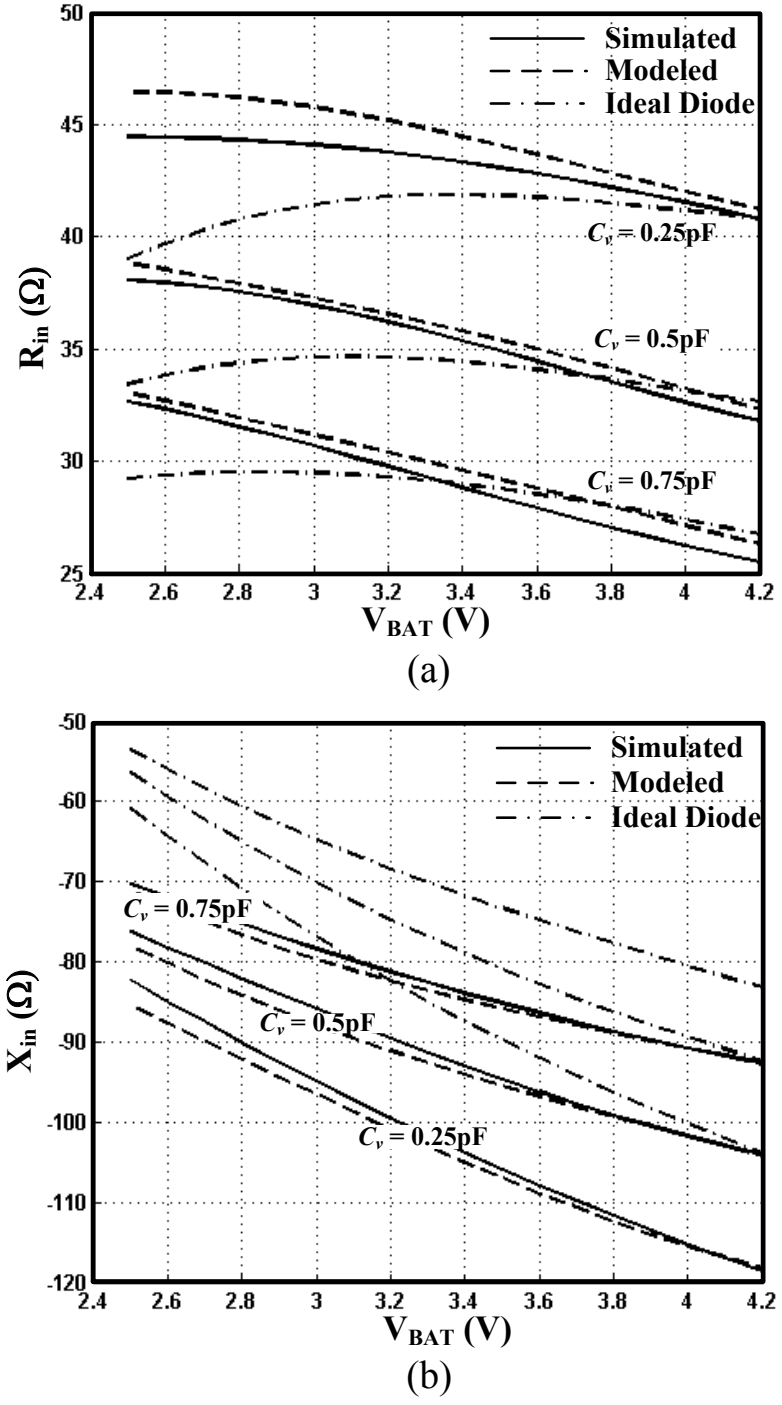


Figure 2.6: Input Impedance variation as a function of battery voltage for different C_v (a) Real part (R_{in}), (b) Imaginary part (X_{in}). ($V_D = 0.4$ V, $R_D = 10\ \Omega$, $C_D = 0.55$ pF, $P_{in} = 17$ dBm, $C_f = 0.4$ pF, $f = 800$ MHz)

2.3 Constant Impedance Operation

Using varactor diodes to control the rectifier input impedance has another benefit. Normally, the rectifier is matched to the source only at a certain input power level; away from that level a portion of the power is reflected, degrading efficiency. We define the overall power conversion efficiency (η_{CNV}) as the ratio of DC power delivered to the battery (P_{dc}) to available input RF power (P_{av}), i.e.,

$$\eta_{cnv} = \frac{P_{DC}}{P_{av}} = (1 - |\Gamma_{in}|^2) L_{MN} \eta_{rec} = (1 - |\Gamma_{in}|^2) L_{MN} \frac{P_{DC}}{P_{DC} + P_{loss}} \tag{2.18}$$

where Γ_{in} is the reflection coefficient at the input, $(1 - |\Gamma_{in}|^2)$ represents the power loss due to impedance mismatch, L_{MN} is matching network loss, and η_{rec} represents the rectifier intrinsic efficiency. The output DC power and total power loss in the rectifier can be given by

$$P_{DC} = I_{DC} V_{BAT} \tag{2.19}$$

$$P_{loss} = I_{DC} V_D + I_{drms}^2 R_D + \frac{I_{crms}^2}{C^2} (C_v^2 r_{cv} + C_D^2 R_D) + I_{DC}^2 R_{rfc} \tag{2.20}$$

where r_{cv} is the effective series resistance of C_v, and R_{rfc} is the choke (RFC) DC resistance. The first two terms in (2.20) represent the dominant part of power loss, which is caused by the diode conduction. Once turned on, the diode turn-on voltage V_D represents a constant loss in efficiency. This can only be improved by using lower barrier diodes, like Schottky diodes, or higher battery voltage which also increases the peak reverse voltage across the diode when off. Losses due to R_D scale with the input power and require using bigger devices for higher input powers. This also increases the diode junction capacitance and can limit the high frequency operation.

Although relations (2.5)-(2.14) were derived assuming an ideal capacitor and inductor, we can also use them to approximate the efficiency. Using this expression for power loss with the waveforms and input impedance, the efficiency can be calculated. Figure 2.7 plots the overall conversion efficiency; it shows that the mismatch severely impacts the conversion efficiency away from the matching condition. With the varactor diode tuning method suggested, matching can be achieved over a broad range of input power, maximizing the overall efficiency.

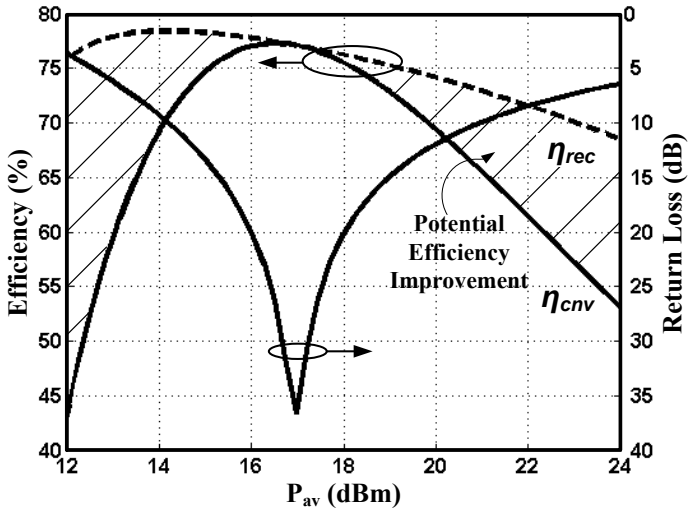


Figure 2.7: Efficiency and return loss versus available RF power with the RF-DC matched at single power level (V_D = 0.4 V, R_D = 10 Ω, C_D = 0.55 pF, V_{BAT} = 3.6 V, C_f = 0.4 pF, C_v = 0.5 pF, r_{cv} = 4.8 Ω, R_{rfc} = 1 Ω, f = 800 MHz, $Z_s = 35 + 100j$ Ω)

Control voltage generation for the varactor diodes will depend on the application. In some cases the control voltages can be changed to maximize the DC output power. In the hybrid transformer duplexer case, the transmitter leakage at the receiver side can be sensed and the varactor diode control voltages can be corrected in a closed-loop manner to minimize the leakage, or *a priori* knowledge of the transmitter power can be used to set the optimum values for the control voltages.

Due to the series resonance nature of the input impedance, this converter tends to be narrowband. The bandwidth is governed by the quality factor of the input series resonant network and wider bandwidth can be achieved by using a smaller series inductor L_r. The maximum achievable bandwidth will be limited by the capactive part of the rectifier input impedance. The proposed diode varactors can be used to tune the input impedance with frequency at the cost of reduced power range. For more demanding applications like a wideband hybrid transformer duplexer, two or more rectifiers can be combined in a staggered form to achieve wider bandwidth as shown in Figure 2.8.

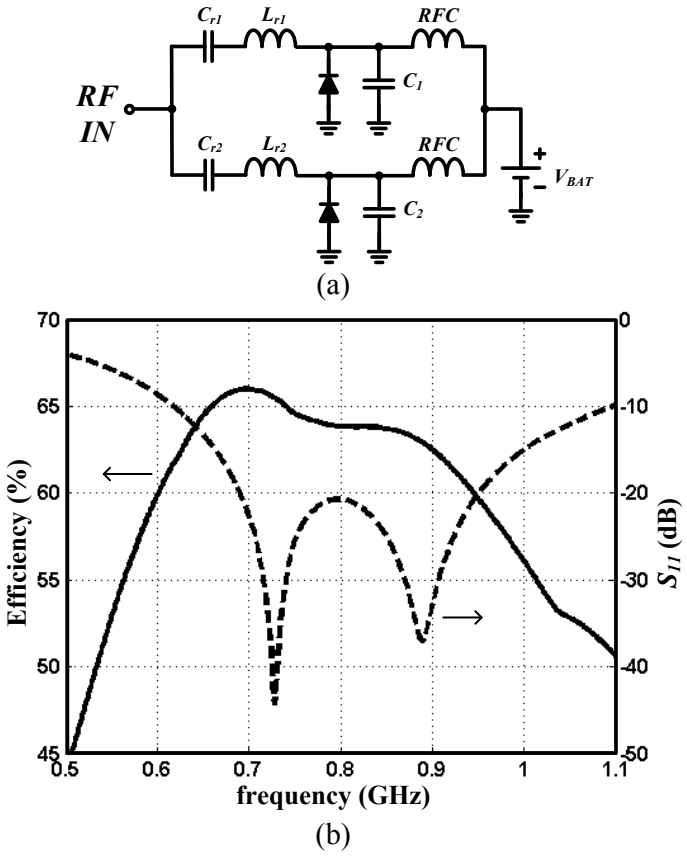


Figure 2.8: Staggered rectifiers for improved bandwidth (a) Schematic. (b) Simulated S_{11} and efficiency. ($L_{r1} = 11$ nH, $L_{r2} = 26$ nH, $C_{r1} = 15$ pF, $C_{r2} = 15.5$ pF, $C_1 = 0.65$ pF, $C_2 = 0.7$ pF, $P_{av} = 20$ dBm, $V_{BAT} = 3.6$ V)

2.4 Measurement Results

Figure 2.9 shows the test board schematic and photograph. A two-layer FR4 printed circuit board was designed for operation at 800MHz with discrete components. A Schottky diode SMS3923-011LF from Skyworks was used to minimize the diode loss. The diode has a 20 V break-down voltage, which is sufficient to withstand a maximum RF power of 27 dBm at a maximum battery voltage of 4.2 V. Also two hyper-abrupt varactor diodes SMV1800-079LF and SMV2019-079LF from Skyworks were used to maximize the tuning range.

To apply the equations developed in the previous section to the circuit in Figure 2.9, the source impedance seen by the rectifier at the diode terminals (Z_s)

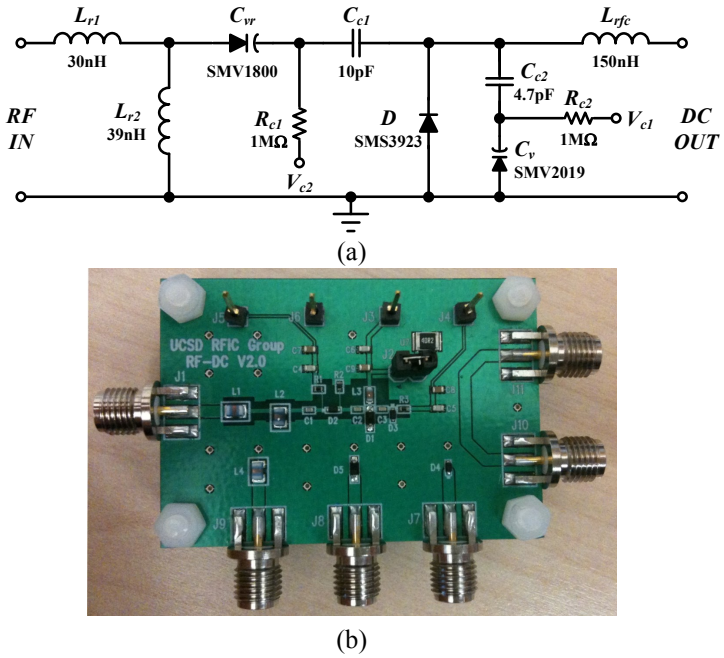


Figure 2.9: Test board (a) Schematic, (b) Photograph.

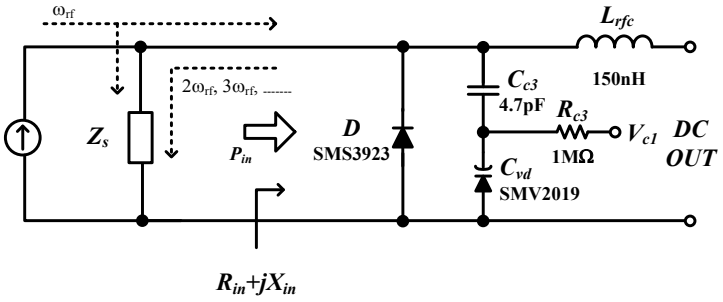


Figure 2.10: Harmonic current flow affects the input impedance at the fundamental.

has to be high at harmonic frequencies ($n\omega_{rf}$ where $n = 2, 3, 4, ...$). This condition is hard to satisfy in practice due to routing parasitics and the self resonance of the components. This is explained in Figure 2.10, having fundamental current going into Z_s is already accounted for by calculating the rectifier input impedance ($R_{in} + jX_{in}$) as a function of input power (P_{in}). On the other hand having harmonics flowing into Z_s changes the rectifier input at the fundamental due to the nonlinear nature of the circuit. Thus Z_s has to be included in the analysis, especially at harmonic frequencies. It was found that including Z_s only at the second harmonic

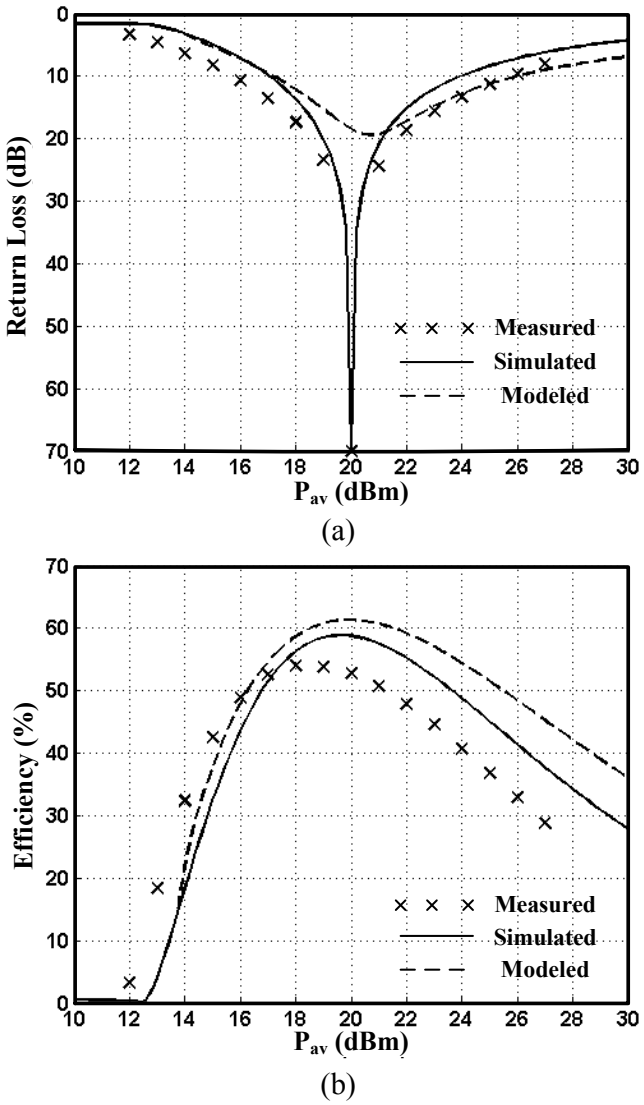


Figure 2.11: Comparison between theory, simulation and measurements (a) Return loss (b) Efficiency.

is sufficient for good matching between theory and simulation. At the second harmonic, Z_s is almost completely capacitive and can be easily included in the analysis since it becomes an extra capacitor (C_s) in parallel with the diode.

Figure 2.11 compares calculated values to simulation and measurements, with the varactor diodes biased for best matching at 20dBm input power. It should be mentioned that for all calculations, the varactor diodes were replaced with a

linear capacitor whose value is equal to the effective varactor capacitance, and parasitic capacitances were also estimated from an Agilent Momentum EM board simulation. Good agreement is shown for low power; the discrepancy at higher power is due to high peak forward currents that exceed the range of validity of the SPICE model. Specifically, the series ohmic resistance of the bulk semiconductor regions of a real diode increases for high-level injection, and it has a positive temperature coefficient. This leads to increased R_D at high power. This mechanism is not accounted for in the analysis nor in the SPICE model used for simulation.

For measurements, the input frequency was fixed at 800 MHz and input power was swept from 10 to 27 dBm. Figure 2.12 shows the large-signal S_{11} and power conversion efficiency ($\eta_{cnv} = \frac{P_{dc}}{P_{av}}$) as a function of the available source power. The figure show the case with a fixed varactor bias (a traditional class E rectifier), and then the case where the two varactor biases are changed to minimize S_{11}; both simulated and measured data are shown. With varactor tuning, S_{11} is less than -20 dB for approximately 12 dB of RF power variation. This was verified across the whole range of a lithium-ion battery voltage from 2.5 to 4.2 V, which is a significant improvement compared to the no-tuning case. The improved S_{11} improves conversion efficiency, as less power is reflected, especially for lower power levels where mismatch loss dominates. At higher power levels, the diode loss dominates due to the diode series resistance and better matching results in more power going to the diode; which amplifies its series resistance increase, further limiting the improvement to about 2%. Efficiency improves with higher battery voltage, which also increases the peak reverse voltage across the diode. The peak measured efficiency of 60% occurs at $V_{BAT} = 4.2$ V and $P_{rf} = 17$ dBm. A comparison to state-of-the art implementations is shown in Table 2.1; our technique achieves wider dynamic range with good efficiency.

This Chapter, in part, has been published in IEEE Transactions on Circuits and Systems–II, "An RF-DC converter with wide dynamic range input matching for power recovery applications". The dissertation author was the primary investigator and author of this paper and it was co-authored by Prof. Lawrence Larson and Dr. Prasad Gudem.

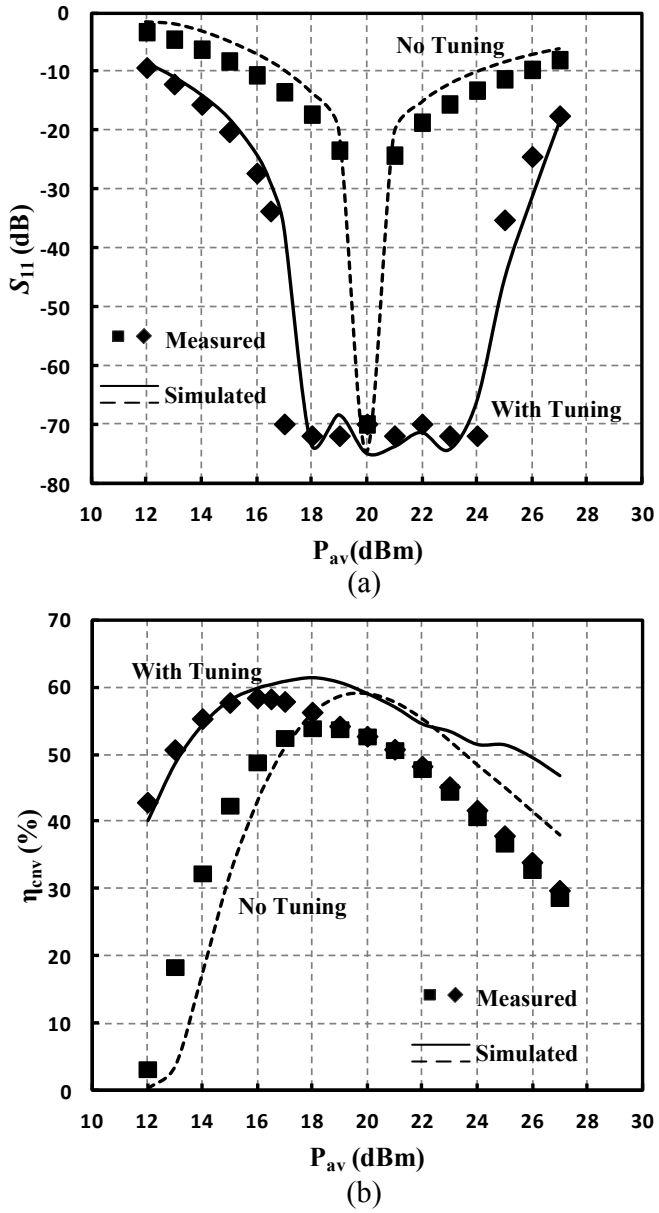


Figure 2.12: Measured and simulated S_{11} and efficiency versus available RF power with and without tuning at 800 MHz and $V_{BAT} = 3.6V$.

Table 2.1: RF-DC converter performance summary and comparison.

	Power Range ($S_{11} < -20\ dB$)	Peak Efficiency	DC Load Range
This work	12 dB	60 %	2.5-4.2 V battery
Ref. [25]	3 dB	63 %	3-4 V battery
Ref. [23]	4 dB	58 %	fixed 1 KΩ
Ref. [30]	10 dB	78 %	fixed 1 KΩ

Chapter 3

Hybrid Transformer-Based Tunable Differential Duplexer in CMOS Process

Practical implementation of monolithic hybrid transformer duplexers have been limited by the poor common-mode isolation. In this chapter, we introduce a differential hybrid transformer architecture to suppress the common-mode coupling and allow reliable high-power operation [31, 32]. A differential hybrid transformer duplexer that covers 3GPP bands I, II, III, and IX between 1.7 and 2.2 GHz is implemented in a 90-nm CMOS process. It achieves a differential to differential isolation of 60 dB in the transmit (TX) band and 40 dB in the receive (RX) band, and a differential to common-mode isolation of 60 dB in both bands. The duplexer with a cascaded low-noise amplifier (LNA) achieves a noise figure of 5.6 dB in the RX path and an insertion loss of 3.7 dB in the TX path. The duplexer and LNA consume 20 mA, and occupy an active area of 0.6 mm^2 .

3.1 Common-Mode Coupling in Prior-Art

When balance is achieved with the proper impedance ratios between the antenna and balance impedance in any of the single-ended versions of a hybrid transformer-based duplexer shown in Figure 3.1, the PA signal appears as an equal

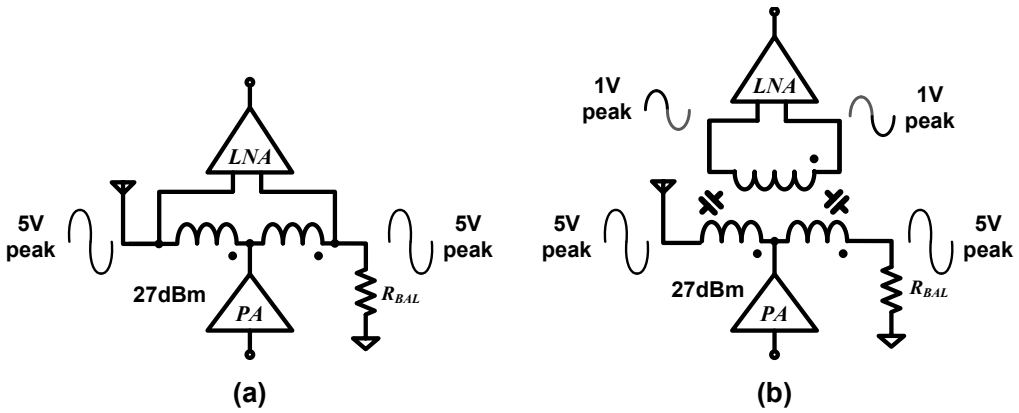


Figure 3.1: Common-mode coupling in hybrid transformer-based duplexer (a) Auto-transformer version [13]. (b) Two-winding transformer version.

voltage swing on the antenna and balance sides, and ideally no signal couples to the LNA side. However, in the the auto-transformer implementation in Figure 3.1(a), which is sometimes favored for its lower implementation loss, the entire power amplifier (PA) signal swing appear across the LNA inputs as a common-mode signal. At high power, this common-mode signal can cause LNA device breakdown rendering this approach impractical. Previous demonstration of an integrated duplexer in [13] relied on this auto-transformer topology, and operation was only verified under small-signal operation due to this limitation.

A two-winding transformer, as in Figure 3.1(b), although has higher loss, eliminates the LNA device breakdown concerns. However, the inevitable capacitive coupling between the primary and secondary windings [33, 34] still couples a common-mode PA signal to the differential LNA inputs. At high PA output powers, this common-mode signal can saturate the LNA or at least cause serious linearity issues.

The generation of cross-modulation distortion that results from mixing the TX leakage with an in-band jammer was explained in Chapter 1. This cross-modulation results from the third-order LNA nonlinearity and is proportional to the square of the TX leakage multiplied by the jammer (i.e. $\propto TX_{leak}^2 \times Jammer$), and thus common-mode and differential leakage are equally problematic. Similarly, the large common-mode noise coupling from the PA to the input of the LNA

can degrade the sensitivity of the receiver due to common-mode to differential conversion in the presence of mismatch. Clearly the same consideration applies to second-order distortion that downconverts the TX leakage to baseband in a direct conversion receiver [3, 4].

A possible solution to the common-mode coupling problem would be to place a common-mode trap on the LNA side [35]. A relatively high-Q would be needed for the trap to be effective, making it inherently narrowband, and hindering the possibility of a wideband tunable duplexer. An AC grounded center tap (CT) in the secondary windings of a hybrid transformer can reduce the common-mode signal coupled to the LNA, by reducing the common mode impedance seen on that side. This is analyzed in Figure 3.2 where C_{cd} and C_{cx} model the capacitive coupling between the windings [34]. For the PA signal, the drop across the primary windings is negligible and the voltage across the antenna and balance resistors is approximately $V_{PA}/2$, thus the common-mode half circuit reduces to that in Figure 3.2(b), from which the common-mode voltage on the LNA side can be written as

$$\begin{aligned} V_{CMLNA} &= \frac{\frac{R_{LNA}}{2} // sL_{21}(1-k_{21-22}) // \frac{1}{2sC_{LNA}}}{\left(\frac{R_{LNA}}{2} // sL_{21}(1-k_{21-22}) // \frac{1}{2sC_{LNA}}\right) + \frac{1}{s(C_{cd}+C_{cx})}} \times \frac{V_{PA}}{2} \\ &\approx s^2 L_{21}(1-k_{21-22})(C_{cd}+C_{cx})\frac{V_{PA}}{2} \end{aligned} \tag{3.1}$$

without the CT, the secondary windings will be open circuit for common-mode considerations, and the voltage on the LNA increases to

$$V_{CMLNA} = \frac{\frac{R_{LNA}}{2} // \frac{1}{2sC_{LNA}}}{\left(\frac{R_{LNA}}{2} // \frac{1}{2sC_{LNA}}\right) + \frac{1}{s(C_{cd}+C_{cx})}} \times \frac{V_{PA}}{2}. \tag{3.2}$$

Thus, a grounded CT provides some improvement by reducing the common-mode impedance level at the secondary windings to approximately $sL_{21}(1-k_{21-22})$, but realizing zero common-mode impedance is not possible, due to the less than unity magnetic coupling between the two halves of the windings (k_{21-22}) .

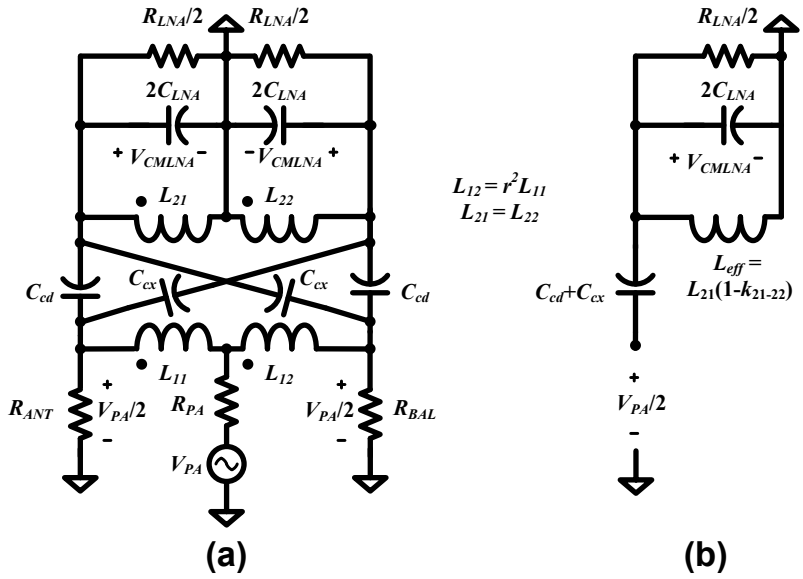


Figure 3.2: Analysis of common-mode coupling in conventional hybrid transformer. (a) Equivalent circuit with PA excitation. (b) Common-mode equivalent half-circuit.

3.2 Differential Hybrid Transformer

We propose a differential hybrid transformer that can achieve wideband cancellation of the common-mode signal. As shown in Figure 3.3, it relies on a differential PA, so that coupling from one phase of the PA cancels that from the other phase. This topology brings the advantage of a fully differential TX and RX path, and adds 3 dB to the PA maximum output power for the same voltage operation. The disadvantage of this approach is the added balun at the antenna port, whose loss adds to the transmitter insertion loss and receiver noise figure.

The extent of common-mode cancellation is only limited by mismatches. Figure 3.4 analyzes the effect of an R_{BAL} mismatch; a similar analysis can be applied to similar sources of mismatch, like antenna impedance mismatch due to amplitude and phase error in the balun. Neglecting the change in current through the balance resistor, the change in the voltage drop across it (Δ_v) can be approximated by

$$\Delta_v \approx \frac{\Delta R_{BAL}}{2} \frac{V_{PA}}{2R_{BAL}} = \frac{\Delta R_{BAL}}{4R_{BAL}} V_{PA}. \tag{3.3}$$

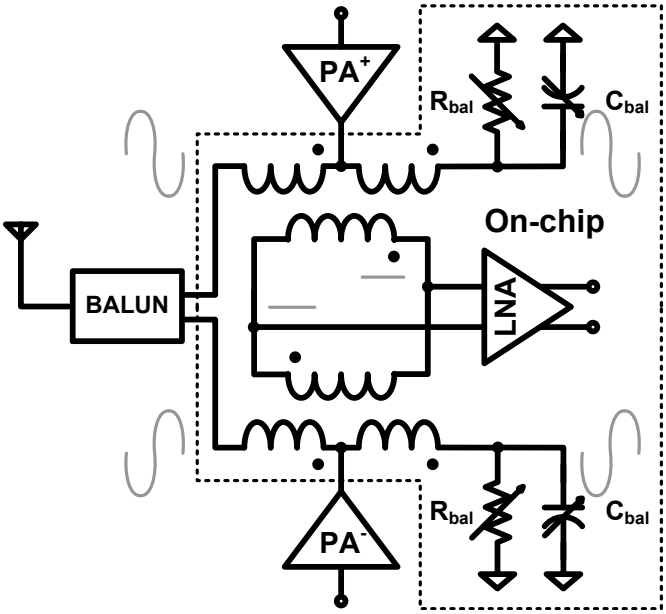


Figure 3.3: Proposed fully differential duplexer.

This creates a differential and common-mode component across each primary winding; the differential component can be dealt with in the same way as in Section 1.5, with $r = 1$ in this case. The first-order term reflected from the balance resistors from the positive and negative sides are in opposite phase and cancel, while second-order terms from multiple reflections add in phase, giving

$$ISOL_{TXDiff-RXDiff} = 20\ \log_{10}\left|\frac{1}{2}\Gamma_{BAL^+}\Gamma_{BAL^-}\right| \tag{3.4}$$

and given that

$$\Gamma_{BAL^+} = -\Gamma_{BAL^-} \approx \frac{\Delta R_{BAL}}{4R_{BAL}}. \tag{3.5}$$

Thus,

$$ISOL_{TXDiff-RXDiff} = 40\ \log_{10}(\frac{\Delta R_{BAL}}{4R_{BAL}}) - 6\ \text{dB}. \tag{3.6}$$

For the common-mode component, the circuit reduces to the equivalent circuit in Figure 3.4(b), from which the common-mode voltage on the LNA side is given by

$$\begin{aligned} V_{CMLNA} &= \frac{\Delta R_{BAL}}{4R_{BAL}} \frac{R_{LNA}//sL_{21}(1-k_{21-22})//\frac{1}{sC_{LNA}}}{\left(R_{LNA}//sL_{21}(1-k_{21-22})//\frac{1}{sC_{LNA}}\right) + \frac{1}{s(C_{cd}+C_{cx})}} V_{PA} \\ &\approx \frac{\Delta R_{BAL}}{4R_{BAL}} s^2 L_{21}(1-k_{21-22})(C_{cd}+C_{cx})V_{PA}. \end{aligned} \tag{3.7}$$

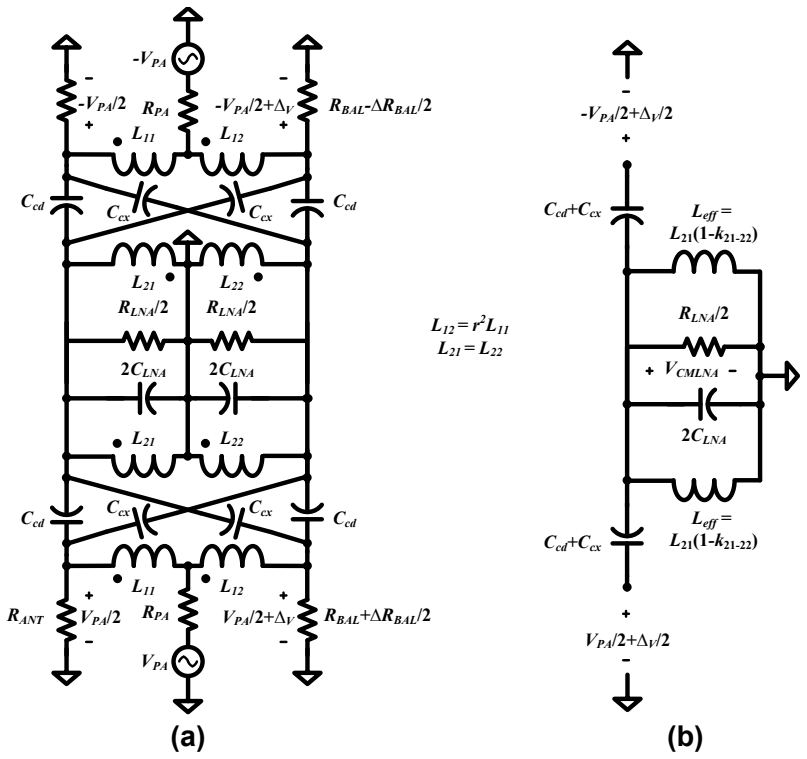


Figure 3.4: Balance impedance mismatch analysis (a) Equivalent circuit with PA excitation. (b) Common-mode equivalent half-circuit.

Figure 3.5 compares isolation results for different topologies, both simulated and calculated values are in good agreement. For the comparison, mixed-mode -parameters were used [36]. Single-ended to common-mode isolation, S_{cs21}, for the conventional single-ended duplexer is compared to differential to common-mode isolation, S_{cd21}, for the proposed duplexer, where port 1 is the PA and port 2 is the LNA. A grounded CT on the secondary windings provides approximately 25 dB of improvement in isolation, achieving about 37 dB of isolation, which is still not adequate for duplexer application in cellular transceivers. Our fully differential hybrid transformer duplexer almost completely cancels the common-mode leakage at the LNA input, and is only limited by mismatches.

Simulation and analysis results in Figure 3.6 with balance impedance mismatch show that with even a 10% mismatch, the isolation exceeds 70 dB. Therefore, very good isolation is achievable in the presence of mismatches, and the same control signals can be used for both sides of the balance impedance, to set its nominal

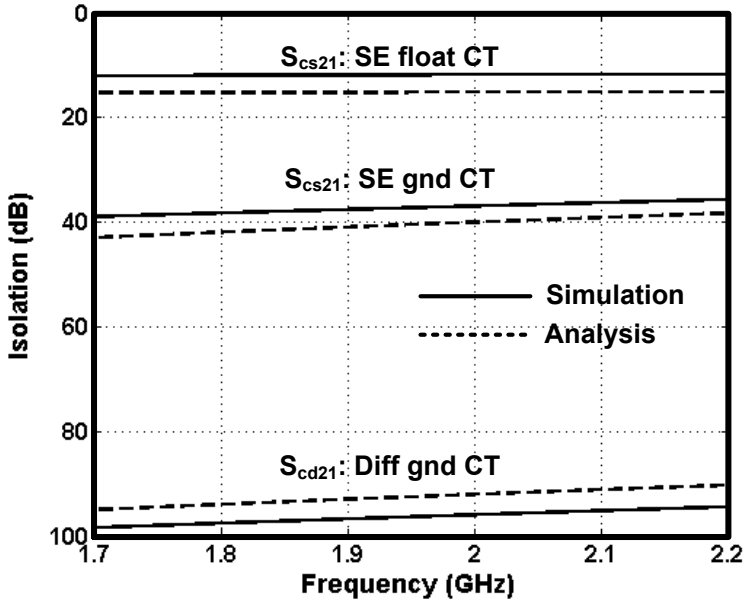


Figure 3.5: Comparison of common-mode coupling for traditional single-ended and differential duplexers (differential duplexer case has 2% R_{BAL} mismatch).

value to that of the antenna impedance, and thus achieve electrical balance in the same manner as the single-ended version.

If the differential PA of Figure 3.3 has a strong common-mode component due to mismatch inside the transmitter, that may limit the isolation. Any common-mode PA signal will only couple through the capacitive coupling between windings and creates common-mode TX leakage at the LNA side. Unlike the case for differential PA signal, coupling from both sides will add in phase and will not cancel. The common-mode to common-mode TX-RX isolation for the fully differential duplexer is expected to be 6 dB worse than the single-ended to common-mode isolation of the single-ended duplexer with CT shown in Figure 3.5, i.e., approximately 30 dB. This value was verified by simulation. If the common-mode PA component is more than 30 dB below the differential PA signal, the common-mode TX leakage will not exceed the differential leakage, assuming 60 dB differential to differential isolation. For example, amplitude and phase error between the two PA phases should be less than 0.74 dB and 5°, respectively, to meet that requirement. Other sources of common-mode signal in a differential PA output can be even-

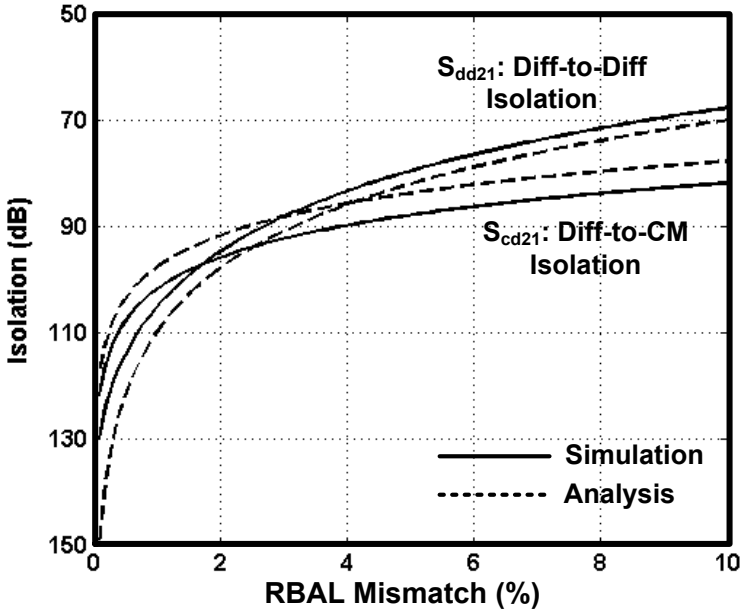


Figure 3.6: Balance resistor mismatch effect on differential-to-differential and differential to common-mode TX-RX isolation.

order distortion; however, these components will fall far out of band and should not constitute a big threat.

A common linearity test to assess the receiver linearity in the presence of TX leakage is the triple-beat (TB) test as explained in Chapter 1. An improvement of 43 dB in TB ratio is observed in simulation by employing the differential hybrid transformer duplexer instead of the single-ended one, which from (1.4) corresponds to 21.5 dB improvement in isolation.

3.3 Differential Duplexer Design in 90nm CMOS Process

3.3.1 Noise-Matched LNA

In typical transceivers with off-chip duplexers, the duplexer is designed to be generically used in various systems and must therefore operate with a standard

termination impedance, typically 50 Ω. If the source and load impedances seen by the duplexer deviate from 50 Ω significantly, the passband and stopband characteristics may exhibit considerable loss and ripple [1]. This necessities conjugate power matching between the duplexer and the LNA.

In hybrid transformer-based duplexers, power matching at the RX port is not required, and both TX-RX isolation and transmitter insertion loss are not affected by mismatch at the RX port. One can take advantage of this by optimizing the impedance presented by the duplexer to reduce the overall receiver noise figure, by providing a noise match rather than a power match [13]. Therefore, in this prototype, the LNA is noise matched by resonating its input capacitance and maximizing the voltage gain that the signal experiences from the antenna to the LNA input. Referred to the antenna, the equivalent input noise voltage of the LNA is divided by this gain.

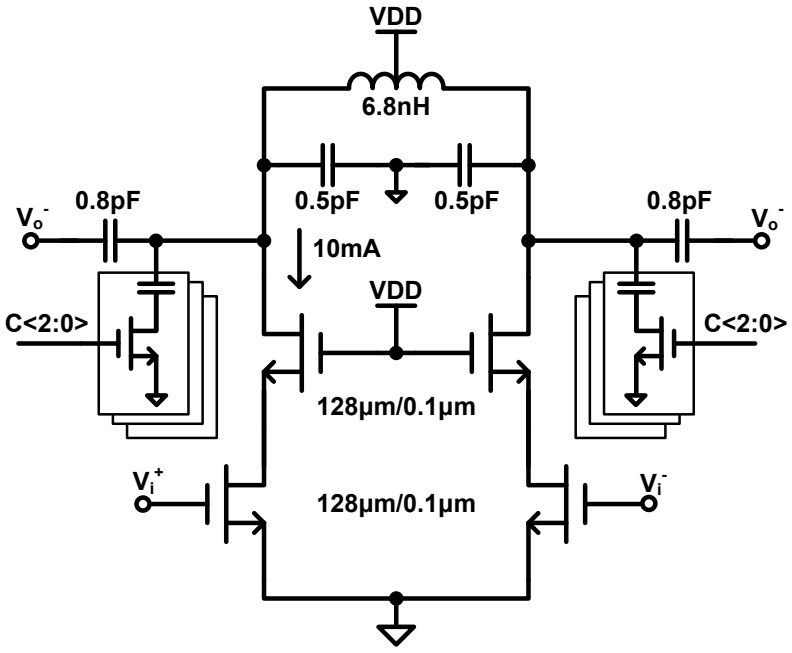


Figure 3.7: LNA schematic.

Figure 3.7 shows the LNA schematic. The LNA device size and current was co-optimized with the duplexer for noise figure while maintaining acceptable linearity. The LNA output was matched to 50 Ω for ease of measurement, and a 3-bit bank of capacitors was used to center the gain curve at the required RX

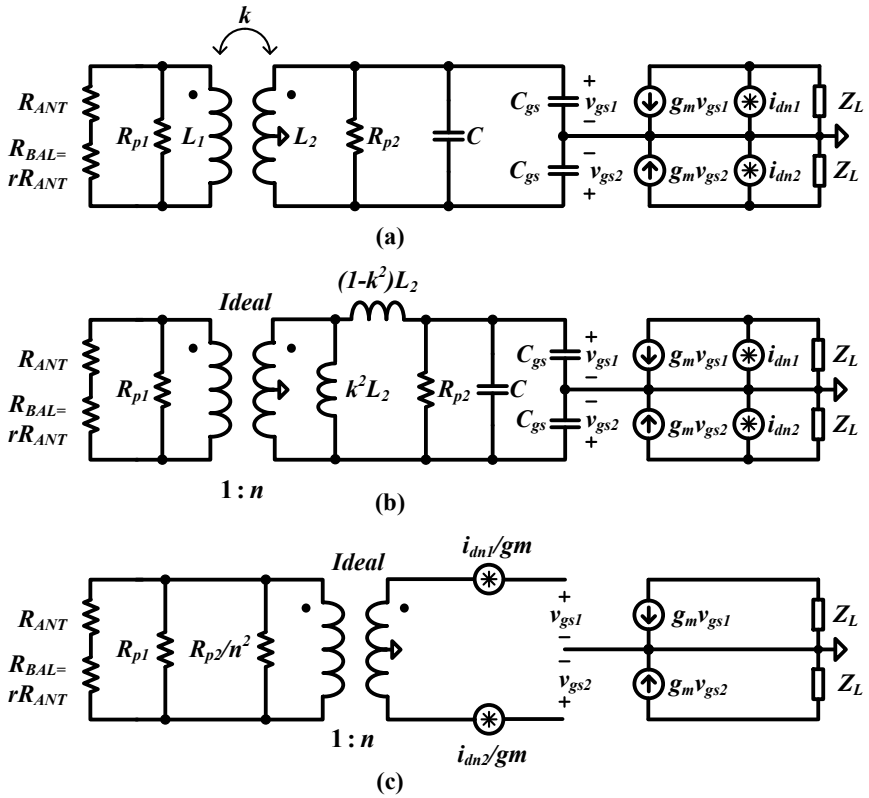


Figure 3.8: (a) Hybrid transformer and LNA equivalent circuit for noise analysis. (b) Transformer replaced with equivalent model. (c) Drain current noise referred to LNA input.

band.

For noise analysis, the equivalent circuit of the hybrid transformer cascaded with the LNA shown in Figure 3.8 is used. The single-ended version is analyzed for simplicity, but the same analysis applies to the differential version. As far as the noise at the LNA input is concerned, the PA port can be considered an open circuit resulting in the circuit in Figure 3.8(a). Resistors R_{p1} and R_{p2} represent the losses in the transformer primary and secondary windings, respectively, and are related to their quality factors Q_1 and Q_2 by

$$R_{p1} = \omega L_1 Q_1 \tag{3.8}$$

$$R_{p2} = \omega L_2 Q_2 \tag{3.9}$$

The transformer with finite magnetic coupling k can be replaced with the model

in Figure 3.8(b) [37], with a magnetizing inductance k^2L_2, a leakage inductance $(1-k^2)L_2$, and an ideal transformer with effective turns ratio n given by

$$n = k\sqrt{\frac{L_2}{L_1}} \tag{3.10}$$

For high k, we can neglect the leakage inductance $(1-k^2)L_2$. To maximize voltage gain and minimize the overall noise figure, the capacitor C together with C_{gs} of the input devices are chosen to resonate the secondary winding magnetizing inductance k^2L_2 . Referring R_{p2} to the primary and the transistors drain thermal noise to the gate results in Figure 3.8(c), from which the total noise referred to the LNA input is given by

$$\overline{v_{nLNA}^2} \approx \Big(\frac{nR_p}{R_p + R_{BAL} + R_{ANT}}\Big)^2 \Big[\overline{v_{nR_{ANT}}^2} + \overline{v_{nR_{BAL}}^2} + \Big(\frac{R_{ANT} + R_{BAL}}{R_p}\Big)^2 \overline{v_{nR_p}^2}\Big] + 2\frac{\overline{i_{dn}^2}}{g_m^2} \tag{3.11}$$

where $R_p = R_{p1}//(R_{p2}/n^2)$, and thus the overall noise factor for the single-ended duplexer cascaded with an LNA is given by

$$F_{SE} \approx 1 + r + \frac{R_{ANT}}{R_p}(1+r)^2 + \frac{2\gamma}{g_m R_{ANT}}\frac{L_1}{k^2L_2}\Big[1 + \frac{R_{ANT}}{R_p}(1+r)\Big]^2. \tag{3.12}$$

The first term $(1+r)$ represents the available power loss of the ideal hybrid transformer in the RX path, as was shown in Chapter 1. The second term represents the additional loss due to the finite quality factor, and the third is the contribution of the LNA; as expected, this contribution can be minimized by having a higher secondary to primary ratio (L_2/L_1). The same expression applies for the fully differential implementation, except that the third term is doubled; as the impedance from each half appears in parallel at the LNA input, thus

$$F_{Diff} \approx 1 + r + \frac{R_{ANT}}{R_p}(1+r)^2 + \frac{4\gamma}{g_m R_{ANT}}\frac{L_1}{k^2L_2}\Big[1 + \frac{R_{ANT}}{R_p}(1+r)\Big]^2. \tag{3.13}$$

To maintain the same noise performance, the turns ratio has to be doubled. The noise match is narrowband due to the need to resonate the capacitance at the LNA side with the inductance looking into the transformer at the RX frequency. Wider bandwidth can be achieved by replacing capacitor C in Figure 3.8 with a high-Q switched capacitor that covers the range of RX bands.

3.3.2 Planar Hybrid Transformer

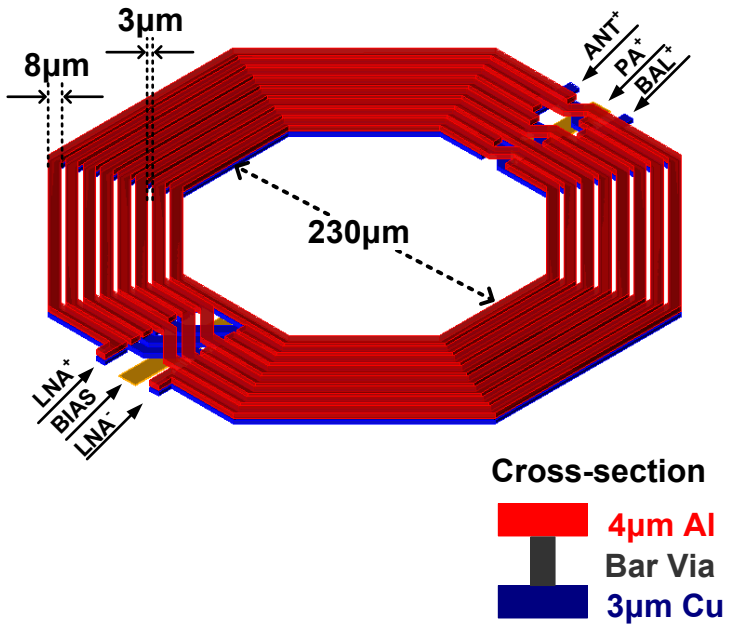


Figure 3.9: Hybrid transformer layout. Two of these are required for the proposed duplexer.

Figure 3.9 shows the layout of the hybrid transformer. To reduce metal resistive losses, the two thick top metal layers, a 4 μm-thick aluminum and a 3 μm-thick copper, were stacked together with a bar via. A 2:6 physical turns ratio was chosen to minimize the LNA noise contribution. The primary and secondary windings were interwound and a minimum turns spacing of 3 μm was used to maximize magnetic coupling [33]. Turn width and outer radius were optimized by Momentum EM simulations to provide a compromise between quality factor and self-resonance frequency, and an 8 μm width together with a 200 μm outer radius was found to be a good compromise. The final parameters were $r = 1$, $L_1 = 2.24$ nH, $L_2 = 15.3$ nH, $Q_1 = 10.5$, $Q_2 = 14.6$, and $k = 0.84$. Using these values in (3.13) with $g_m = 70$ mS and $\gamma = 1$ gives a noise figure of 5.5 dB.

3.3.3 Balance Network

The balance between the antenna impedance and the balance impedance is critical to obtain the required isolation. An on-board tunable open stub together with the bondwire inductance and pad capacitance provides a nearly 50 Ω antenna impedance to the duplexer. On the balance side, a voltage-controlled resistor (VCR) in parallel with a voltage-controlled capacitor (VCC) was used.

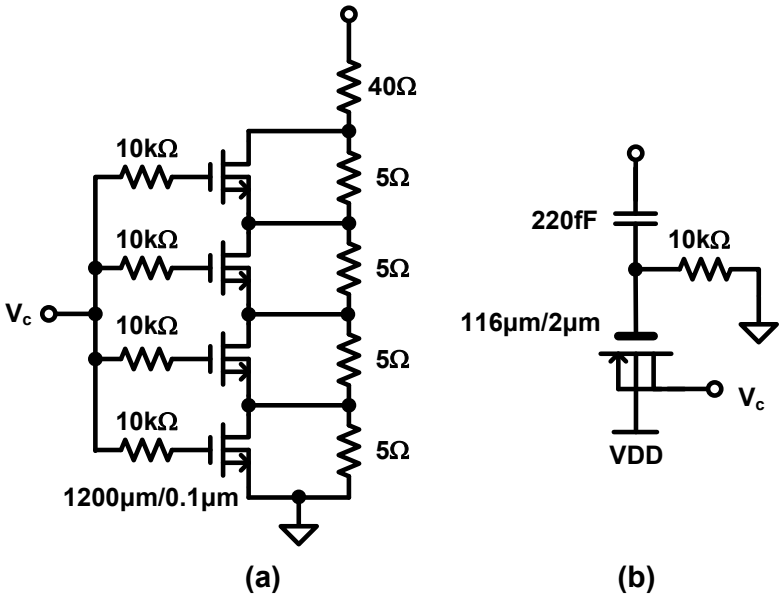


Figure 3.10: Balance network schematic. (a) VCR. (b) VCC.

As shown in Figure 3.10(a), the VCR can vary from roughly 40 to 60 Ω . To withstand high powers, the variable part was split into four components in series with a larger resistor to divide the voltage swing among them, and an RF floating gate was utilized so that voltage swing splits between V_{gs} and V_{gd}. Figure 3.10(b) shows the VCC, it varies between 150 and 200 fF. A series metal-insulator-metal (MIM) capacitor was used to reduce the voltage swing across the varactor, which was implemented with an inversion-mode thick-oxide pMOS varactor [38]. The series fixed resistor or capacitor that limits the voltage swing across the MOS switches or varactors also limit the range of impedance that can be achieved. This, together with linearity considerations that are discussed next, necessities the use of high voltage switched capacitors and resistors to further extend the range of

the covered impedance. The same techniques used for antenna switches: stacking, drain/source bias, and RF floating bulk/gate can be used to allow high power tolerance without reliability issues for the MOS switches [39, 40].

Analog control of the balance impedance can ideally provide perfect balance with the antenna impedance without the quantization steps of a digital alternative. However it will also make the optimum control voltages power level dependent causing some nonlinearity. Any nonlinearity generated in the balance network would leak back into the LNA input degrading the effective isolation. Therefore, analog variability should be kept to a minimum, and may ideally be combined with other highly linear digital controls to maximize the covered range [40].

Another concern arises from the antenna impedance variation, which could significantly degrade the duplexer isolation unless the balancing network impedance tracks it. In a mobile environment, due to variation in surroundings and human interaction, the antenna impedance could change considerably. An antenna tuner could be used to limit the range of variation, and the TX leakage can be dynamically monitored at the LNA side so that the balancing network impedance can be corrected accordingly. This was proposed in [2] and implemented in discrete form in [41]. In the next chapter a complete implementation of such an antenna impedance tracking loop will be presented.

3.4 Measurement Results

The differential duplexer based on hybrid transformers was implemented in a 90-nm CMOS process. Figure 3.11 shows the die microphotograph. The die active area is 0.6 mm^2. Special care was taken in layout to maintain symmetry and minimize any additional coupling from the TX side to the RX side. The die was packaged in a 24-pin QFN plastic package and mounted on an FR4 board for testing.

For small-signal -parameter characterization, a four-port network analyzer was used to directly measure mixed-mode S-parameters; the unconnected ports were properly terminated. Figure 3.12 shows the measured TX-RX isolation. Dif-

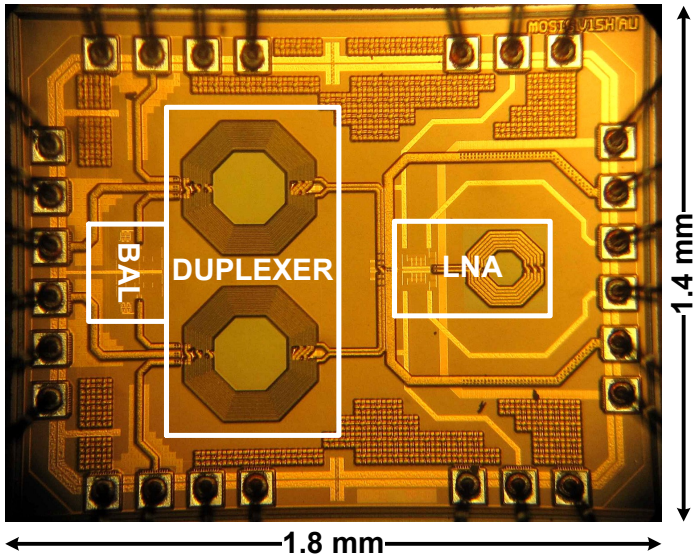


Figure 3.11: Die microphotograph.

ferential to differential TX-RX isolation greater than 70 dB can be achieved at any channel between 1.7 and 2.2 GHz. The isolation in the RX band exceeds 40 dB for the worst case duplex spacing of 190 MHz between the TX and RX bands (IMT band case). It should be mentioned that for a hybrid transformer duplexer, it is easier to achieve isolation when the duplex offset between the TX band and RX band is smaller, in contrast to conventional SAW duplexers. The main reason for isolation bandwidth limitation is the frequency dependence of the antenna impedance, as seen by the duplexer relative to that of the balance network, as explained in Chapter 1. Differential to common-mode TX-RX isolation better than 60 dB was measured. It is almost frequency independent and is limited by the mismatches in the circuit, board, and measurement setup.

Figure 3.13 shows the measured cascaded noise figure and gain of the duplexer followed by the LNA, and S_{11} at the antenna port. More than 14 dB of gain is achieved across the RX bands with a noise figure ranging from 5.2 to 5.9 dB. Even though the LNA is noise matched, the measured S_{11} is less than -8 dB,which is in part due to the PA port resistance that still provides a real part for the input impedance, as seen from the antenna port. This is acceptable, especially as there are no external SAW filters that require 50 Ω termination for proper operation.

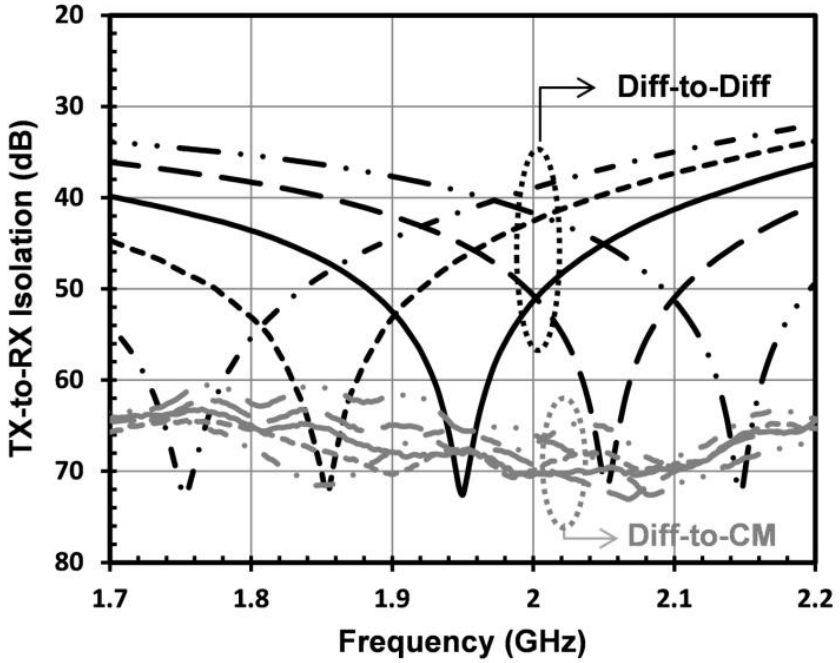


Figure 3.12: Measured differential-TX to differential-RX isolation and differential-TX to common-mode-RX isolation.

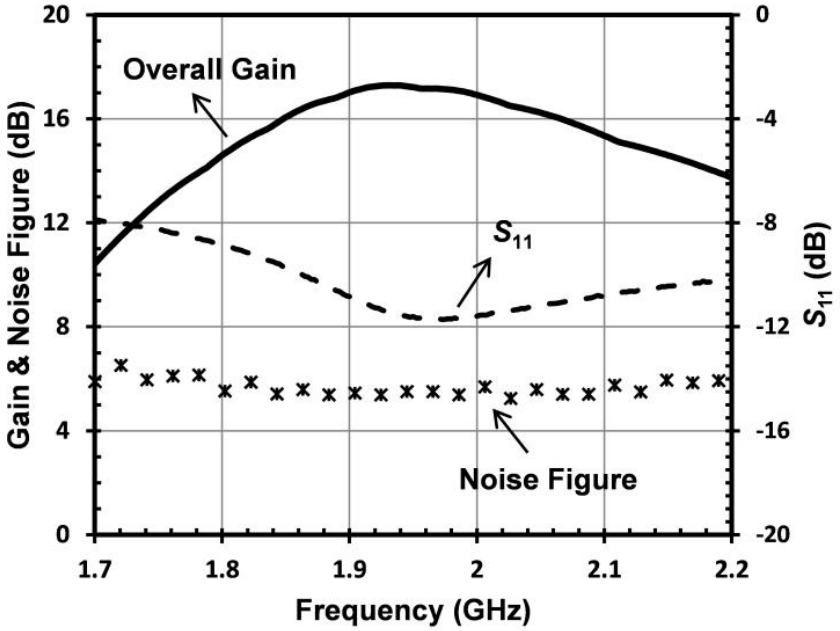


Figure 3.13: Measured cascaded gain and noise figure of duplexer and LNA.

Figure 3.14 shows the measured return loss at the PA port and the insertion loss from the PA to the antenna. The insertion loss, including 0.2 dB board loss, was less than 3.9 dB. The hybrid transformer PA port impedance is 25 Ω, this impedance transformation can be useful for PA designers to achieve higher output power with the same voltage swing. In our case, that port was matched to 50 Ω on board for ease of measurement.

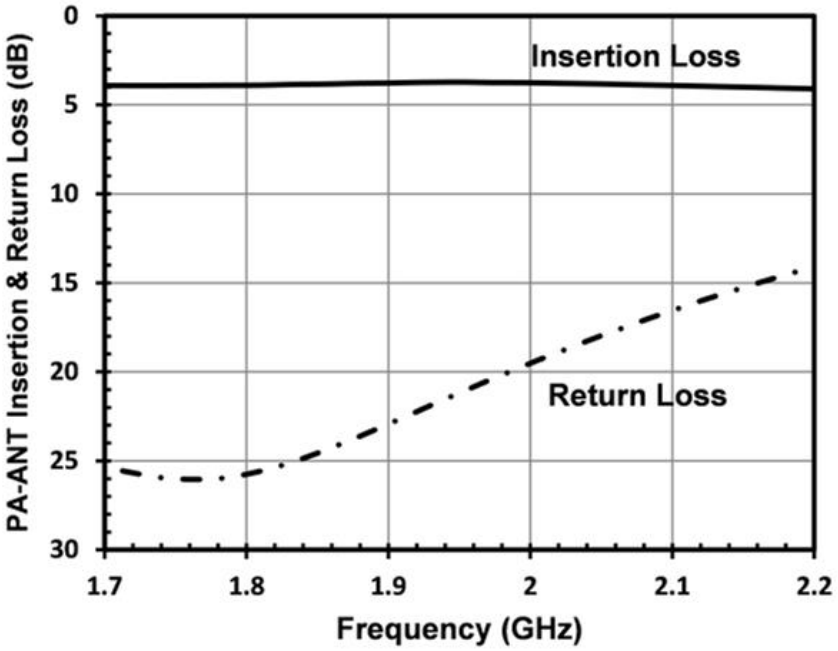


Figure 3.14: Measured TX insertion and return loss.

The high-power measurement was carried out using external baluns, and balun loss was dembedded from the results. Isolation with TX powers up to 27 dBm was verified. Figure 3.15 shows the IIP3 measurement results. Two tones with a center frequency of 1.96 GHz and 5 MHz spacing were injected at the antenna port and the fundamental output and IM3 were plotted. The measured IIP3 was −5.6 dBm. Figure 3.16 shows the LNA output spectrum in a triple-beat (TB) test. Two tones with 27 dBm of power were applied to the PA port with a center frequency of 1.95 GHz and 5-MHz spacing, a single-tone jammer of −43 dBm at 2.14 GHz was applied to the antenna port, and the resulting cross modulation at 2.145 GHz was observed at the LNA output. The measured TB ratio (the ratio

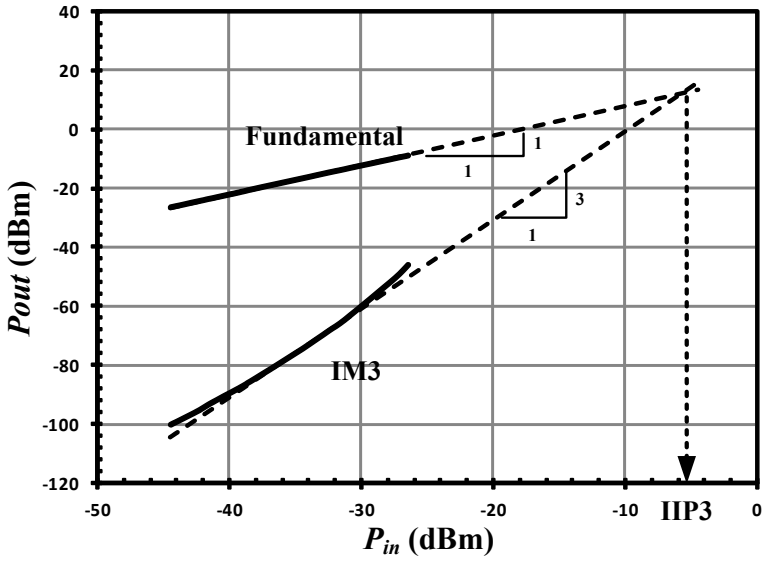


Figure 3.15: Receiver two-tone IIP3 measurement.

between jammer and cross modulation distortion) was 58.2 dB. With the receiver IIP3 of −5.6 dB, this corresponds to an effective duplexer isolation of 61.7 dB.

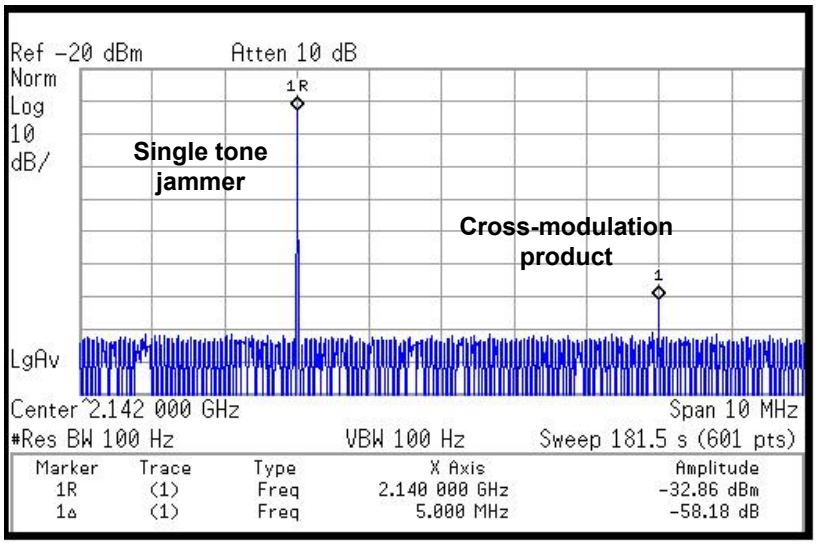


Figure 3.16: Measured spectrum from triple-beat test ($P_{TX} = 27$ dBm, $P_{jammer} = -43$ dBm).

The performance of the duplexer is summarized and compared to other state-of-the-art implementations in Table 3.1. It is compared to a conventional off-chip duplexer from Murata, a discrete hybrid transformer implementation for the RF identification (RFID) reader from [41], and an autotransformer-based integrated duplexer from [13]. The hybrid transformer duplexers have the flexibility to cover more bands, while SAW duplexers cover one band per duplexer and to cover more bands, a bank of more duplexers and a switch are needed. Our work is a demonstration of a high-power capable integrated duplexer since it solves the common-mode isolation issue, which, together with the balance network design, allows reliable high-power operation. Very good differential and common-mode isolation was achieved. The noise figure and insertion loss in the TX path are high compared to other approaches, due to the inherent 3-dB loss of the hybrid transformer, the higher loss of a two-winding transformer compared to the autotransformer of [13], and the extra balun loss required for conversion to single-ended at the antenna.

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Table 3.1: Comparison with state-of-the-art duplexer implementations.

Parameter	Typical SAW	Ref[41]	Ref[13]	This Work
Technology	SAW	Discrete	65nm CMOS	90nm CMOS
Bands Covered	1 band	UHF RFID Band	3GPP bands 1, 2, 3, 9	3GPP bands 1, 2, 3, 9
High Power	Yes	Yes	No	Yes
TX Band Isolation	57 dB DM, 45 dB CM	50 dB DM	55 dB DM, 0 dB CM	70 dB DM, 60 dB CM
RX Band Isolation	50 dB	N/A	45 dB	40 dB
IL_{TX}	$2^{\star} + 1^{\dagger} =$ 3 dB	2.7 dB	2.5 dB	$3.9 + 0.8^{*} =$ 4.7 dB
Casc. NF	$3^{\star}+1^{\dagger}+2^{\ddagger} =$ 6 dB	$7 + 2^{\ddagger} =$ 9 dB	5 dB	$5.9 + 0.8^{*} =$ 6.7 dB
Area (mm^2)	3.2	N/A	0.1	0.6

* Assumes typical SAW duplexer insertion loss $IL_{TX} = 2$ dB $IL_{RX} = 3$ dB.

† Assumes Skyworks SKY13380-350LF SP4T switch and 0.2dB board loss.

‡ Assumes 2 dB LNA NF.

* Assumes Anaren BD1722N5050AHF antenna balun with 0.8dB loss.

Chapter 4

Antenna Impedance Tracking Loop for Hybrid Transformer Duplexer Calibration

Electrical balance between the antenna and the balance network impedances is crucial for achieving high isolation in a hybrid transformer duplexer. In all the previous demonstrations of hybrid transformer duplexers, the antenna impedance was assumed to be 50 Ω and isolation would degrade significantly under realistic antenna impedance frequency dependence and variation in a mobile environment. In this chapter, we introduce a calibration loop that can detect the TX leakage generated due to imbalance in the duplexer and correct the balance network impedance to track antenna impedance variation and restore isolation. The design of a novel high power balance network is proposed to achieve high isolation at the TX and RX bands simultaneously under antenna impedance mismatch. It achieves an isolation of more than 50 dB in the transmit and receive bands, with an antenna VSWR within 2:1, and between 1.7 and 2.2 GHz. The duplexer, along with a cascaded direct-conversion receiver, achieves a noise figure of 5.3 dB, a conversion gain of 45 dB, and consumes 28 mA from a 1.2 V supply and 7 mA from a 2.5 V supply. The insertion loss in the transmit path was less than 3.8 dB. Implemented in a 65-nm CMOS process, the chip occupies an active area of 2.2 mm^2.

4.1 Antenna Impedance Variation

Antennas vary substantially in impedance, with particularly rapid changes near the edges of their useful bandwidth. Moreover, when a mobile phone call takes place there is an interaction between the user and the antenna housed within the phone [42]. For example, many calls occur with the phone held next to the head. In such circumstances, there is a strong interaction between the antenna and the users head and hand, which act as lossy dielectrics. This causes a significant reduction in the antenna radiation efficiency. User interaction also causes a change in the antenna driving point impedance that leads to a further, often significant, loss of performance.

In [42] a dual-band planar inverted F antenna (PIFA) is studied, such antennas are commonly used in mobile phones. The effect of user interaction on the fundamental performance of the antenna is analyzed in both its low (around 900 MHz) and high (around 1800 MHz) frequency bands. A model of a head and hand is included into HFSS EM simulations. It is found that the fundamental impedance of the antenna becomes more resistive and inductive as the level of user interaction increases. The antiresonant frequency of the slot, used for dual-band operation, moves to a lower frequency with user interaction, and some loss resistance is also introduced. Figure 4.1 shows antenna impedance variation with frequency for different spacing between the antenna and user hand. These results show that very large mismatches are possible.

The design of circuitry that can adaptively recover some of this lost performance, namely antenna tuners, has been the subject of active research for many years [43, 44, 45, 46, 47]. Traditionally, cell phone antennas have been designed to cover multiple frequency bands establishing tradeoffs with other important parameters such as antenna efficiency or overall size. With the increase of allocated frequency bands, designing and developing broadband antennas becomes a difficult task. Current wireless standards span a frequency range from 700 MHz up to 2700 MHz. It is a difficult design challenge for a small antenna to achieve high efficiency over such wide range. Antenna tuners can relax the antenna impedance bandwidth leading to a potential reduction in size and design time. In addition,

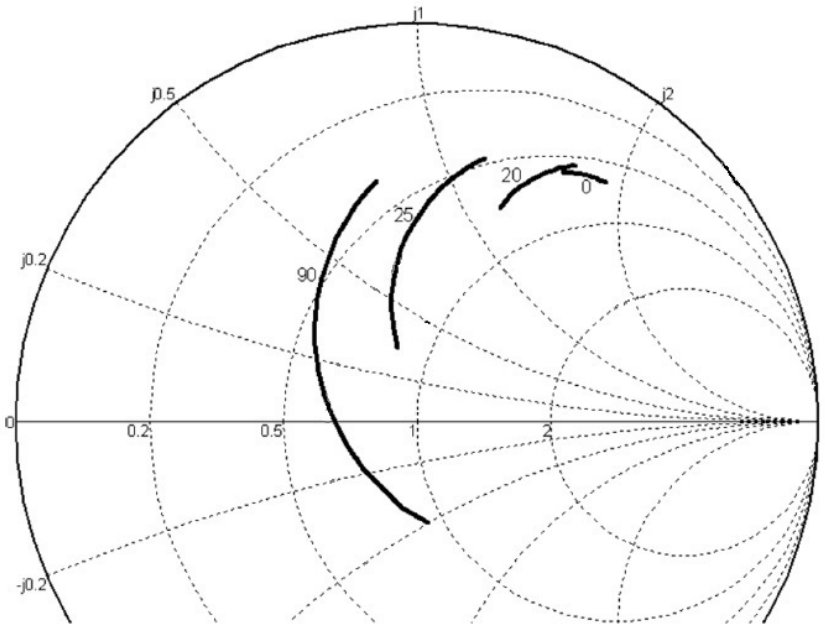

Figure 4.1: Antenna impedance variation for different hand spacing d=0, 20, 25, and 90 mm (indicated adjacent to the points) from 1710–1880 MHz [42].

the antenna can be re-tuned to mitigate user interaction effects, thus enhancing the power transfer to/from the transciever [46].

Using such antenna tuners, the antenna impedance variation could be limited to a smaller range. Typically a voltage standing wave ratio (VSWR) of 2:1 is considered very acceptable as it means that 89% of the power is delivered to the antenna. As explained previously in Chapter 1, the isolation in a hybrid transformer duplexer is achieved when the balancing network impedance tracks the antenna impedance and is given by

$$ISOL_{TX-RX} = 20\log_{10}|\Gamma_{ANT}(\omega) - \Gamma_{BAL}(\omega)| - 20\log_{10}(\frac{1+r}{\sqrt{r}}) \tag{4.1}$$

where

$$\Gamma_{ANT}(\omega) = \frac{Z_{ANT}(\omega) - R_o}{Z_{ANT}(\omega) + R_o} \tag{4.2}$$

and

$$\Gamma_{BAL}(\omega) = \frac{Z_{BAL}(\omega) - rR_o}{Z_{BAL}(\omega) + rR_o}. \tag{4.3}$$

For example the VSWR of 2:1 case corresponds to $\Gamma_{ANT} = 1/3$, if the balance network does not track the antenna and is fixed at 50 Ω, the TX-RX isolation will be around only 16 dB for the symetric case ($r = 1$), which is unacceptable. Hence, the balance network should be able to follow these antenna impedance variations with high enough resolution so as not to compromise the TX-RX isolation.

4.2 Tracking Loop Design

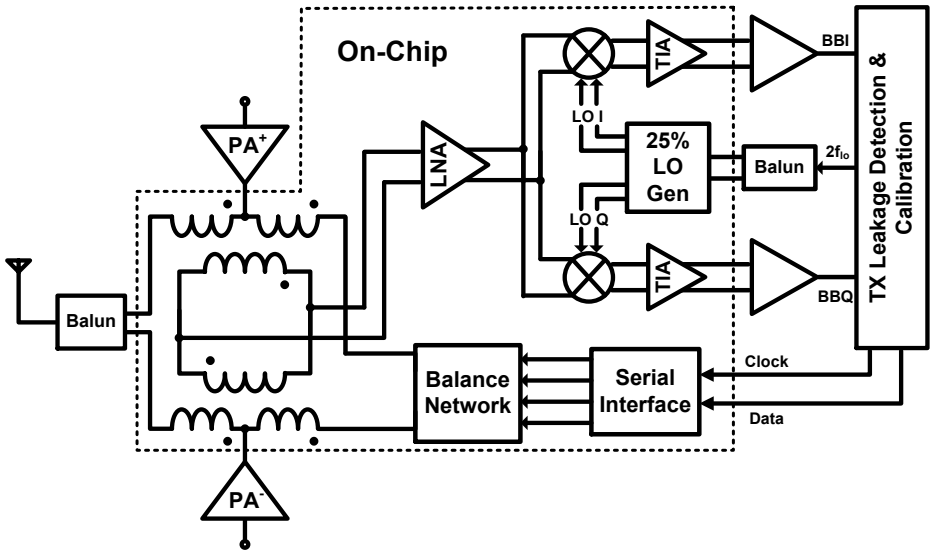

Figure 4.2: Integrated differential duplexer with antenna impedance tracking loop.

From (4.1), good TX-RX isolation can be maintained only if Γ_{BAL} tracks the variations in Γ_{ANT}. Such variations are slow in nature and can be calibrated infrequently. Toward that goal, we propose the feedback loop shown in Figure 4.2. A differential duplexer similar to the one used in Chapter 3 together with a direct-conversion receiver is utilized. The receiver can be the same one used for normal reception, or a special receiver with relaxed performance requirements can be used. The receiver downconverts the TX leakage using the TX LO, measures the amplitude of that leakage, and feeds back a correction signal to the balance network to restore the hybrid transformer balance and minimize the leakage.

4.2.1 Balance Network Design

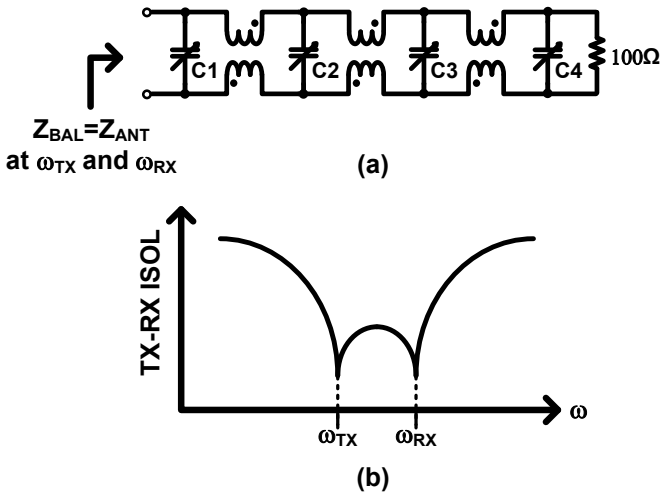

Figure 4.3: (a) Proposed balance network. (b) Desired TX-RX isolation response.

The balance network should provide a wide range of impedances and also tolerate high power; meanwhile it should be highly linear as any intermodulation products generated will leak back to the LNA degrading isolation and would also distort the transmited output spectrum. From (4.1), if Γ_{ANT} and Γ_{BAL} have the same frequency dependence, wideband isolation can be achieved. In practice, for a generic antenna the frequency dependence of Z_{ANT} cannot be easily matched by Z_{BAL}, limiting the achievable isolation bandwidth. A practical approach would be to match Z_{ANT} and Z_{BAL} at both the TX and RX frequencies, and only achieve high isolation at the transmit and receive frequencies, i.e.

$$Z_{BAL}(\omega_{TX}) \approx Z_{ANT}(\omega_{TX}) \tag{4.4}$$

and

$$Z_{BAL}(\omega_{RX}) \approx Z_{ANT}(\omega_{RX}). \tag{4.5}$$

Matching the real and imaginary parts of the impedance at two different frequencies requires four tuning parameters. A possible implementation of this tuner is a cascade of three π-sections with four high voltage highly linear switched capacitors, as shown in Figure 4.3. The π-section can convert the 50 Ω termination up or down and, with a proper inductance and capacitance range, can cover a wide range of

impedances between 1.7 and 2.2 GHz. The differential implementation makes use of coupled transformers to improve the Q-factor and reduce area, and a switched capacitor with stacked devices switches to tolerate high power and maintain high linearity.

The inductors in the balance network are chosen to be equal and their value is chosen to minimize the required capacitance tuning ratio needed to cover a certain area of impedance on a Smith chart. Doing so is equivalent to maximizing the covered impedance range for a given capacitor tuning ratio. For example to cover a VSWR of 2:1 on the Smith chart, Table 4.1 shows the required ranges of all capacitors (C_1, C_2, C_3 and C_4) for different inductor values, obtained using an optimizer for both IMT band operation with $f_{TX} = 1.95$ GHz and $f_{RX} = 2.14$ GHz, and PCS band operation with $f_{TX} = 1.88$ GHz and $f_{RX} = 1.96$ GHz. As any passive network impedance would rotate in a clockwise direction with frequency increase on a Smith chart, in this simulation Γ_{ANT} was assumed to rotate in same direction as frequency increases from the TX frequency to the RX frequency, i.e.

$$\Gamma_{ANT}(\omega_{RX}) = \Gamma_{ANT}(\omega_{TX}) \times Ke^{-j\varphi} \tag{4.6}$$

where K is assumed to be 1 and φ assumed to be $\pi/4$ in the IMT band and $\pi/8$ in the PCS band. The real value of K and φ will depend on the real antenna characteristics but the conclusion from this experiment remains valid. As seen in the Table 4.1, there is an optimum value of inductance (2.85 nH) that helps minimize the tuning range required for the capacitors.

The maximum isolation that can be achieved will be limited by the quantization step of the switched capacitors used in the balance network. Figure 4.4 shows the achievable isolation (minimum of isolation at the TX and RX bands) for antenna VSWR within 2:1 i.e. $|\Gamma_{ANT}| < 1/3$, with different switched capacitor bank LSB found using an optimizer. The minimum isolation is 43.6 dB, 49.2 dB and 55.4 dB for capacitor steps of 50 fF, 25fF and 12.5 fF respectively. Thus to guarantee more than 50 dB of isolation in both the TX and RX bands a capacitor step less than 25 fF should be used.

Since the achievable quality factor of the passives in a CMOS process is relatively low, it is important to check the dependence of the covered impedance

Table 4.1: Capacitance tuning ratio versus inductance value.

L(nH)	Band	C_1(pF)		C_2(pF)		C_3(pF)		C_4(pF)		Max.
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	C_{max}/C_{min}
2	IMT	1.38	4.97	2.25	11.36	5.36	11.23	2.48	5.43	5.83
	PCS	1.52	5.45	2.45	13.12	5.79	12.86	2.54	5.91	
2.85	IMT	2.66	3.95	5.87	7.92	6.03	7.47	3.16	4.16	1.59
	PCS	3.05	4.23	6.87	9.32	7.06	8.72	3.48	4.58	
3.7	IMT	1.49	3	2.7	5.46	1.75	4.81	1.5	3.14	3.17
	PCS	1.21	3.27	2.65	6.35	2.69	5.54	1.75	3.56	

range on the quality factor of the individual capacitors and inductors used in the balance network. Figure 4.5 plots the range of antenna impedance covered by the balance network for two cases of inductor quality factor (Q_L) and switched capacitor quality factor (Q_C). This was done for the IMT band with same assumptions about antenna impedance variation as before and a capacitor tuning ratio of 3. It is clear how the range of impedance shrinks toward the origin with lower Q. With the achievable $Q_L = 20$ and $Q_C = 35$, a VSWR range of 2:1 is fully covered and only few parts of the VSWR $= 3:1$ circle are missed.

The remaining feature that remains to be characterized is how if the assumption made earlier regarding antenna impedance variation from the TX to the RX frequency is not valid. In other word, what is the range of impedance that can be covered at the RX frequency given a certain impedance at the TX frequency. Figure 4.6 shows these ranges of impedance for different $\Gamma(\omega_{TX})$ for the IMT band with $Q_L = 20$ and $Q_C = 35$. As in the previous case, it was noticed in simulation that the lower Q causes the range to shrink, however it is very unlikely that the antenna impedance variation would be larger than the range already covered under achievable Q with CMOS integrated passives.

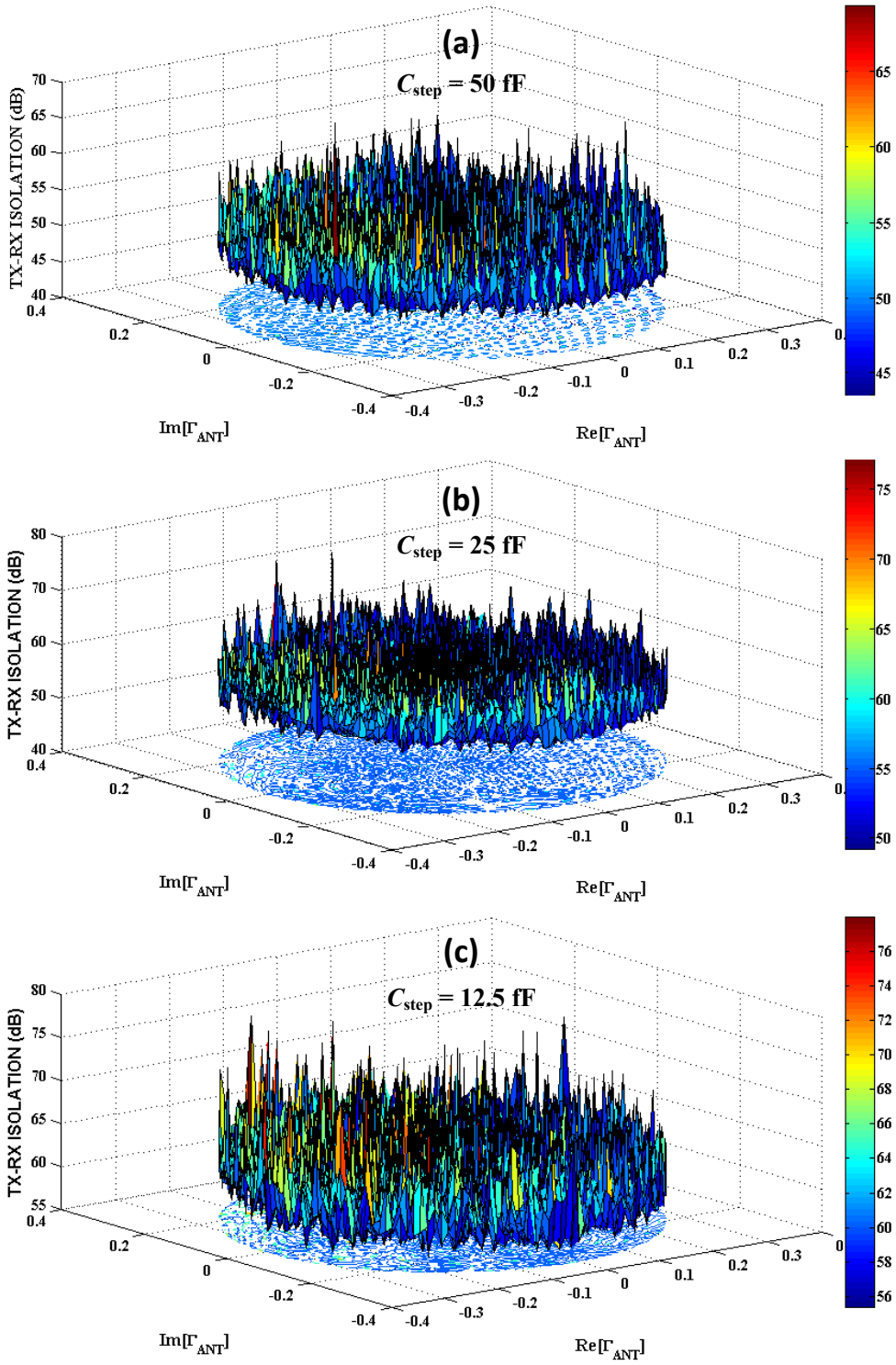

Figure 4.4: Achievable isolation for different capacitor step (a) LSB=50 fF. (b) LSB=25 fF. (c) LSB=12.5 fF.

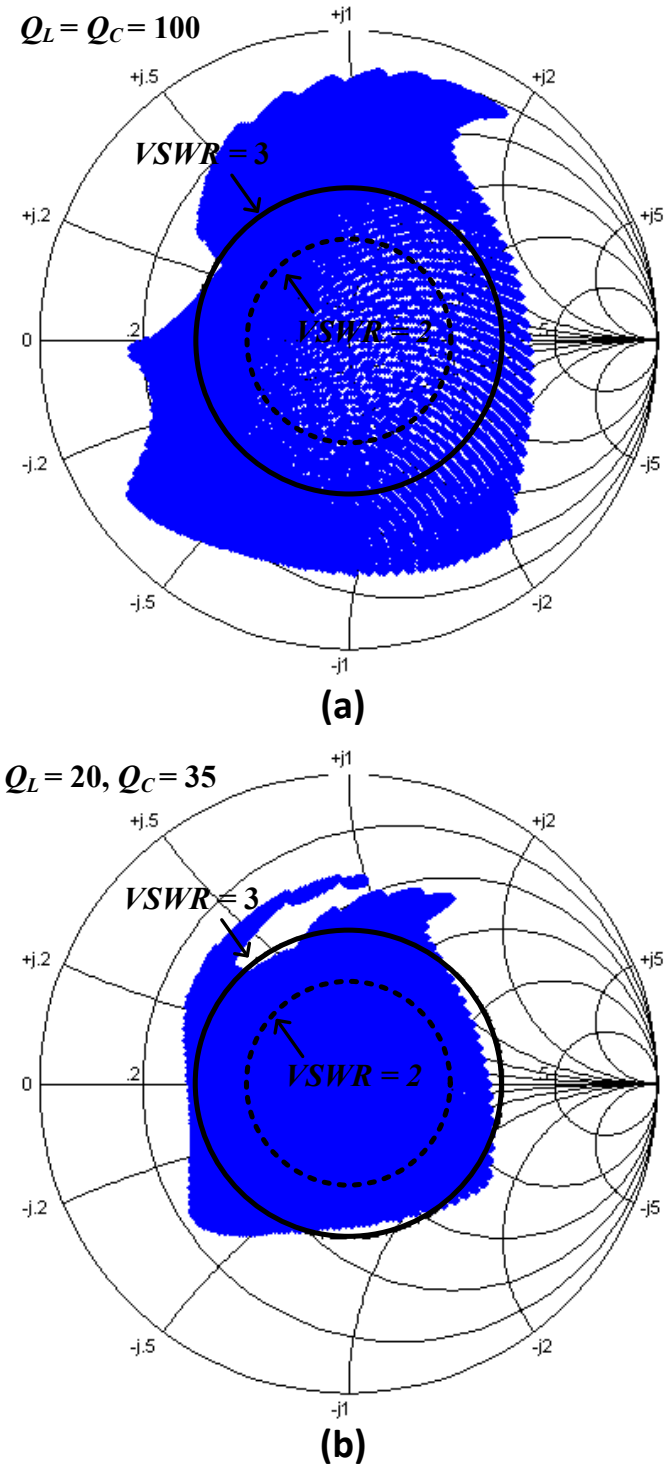

Figure 4.5: Range of impedance covered versus passives Q (a) $Q_L = Q_C = 100$. (b) $Q_L = 20$ and $Q_C = 35$.

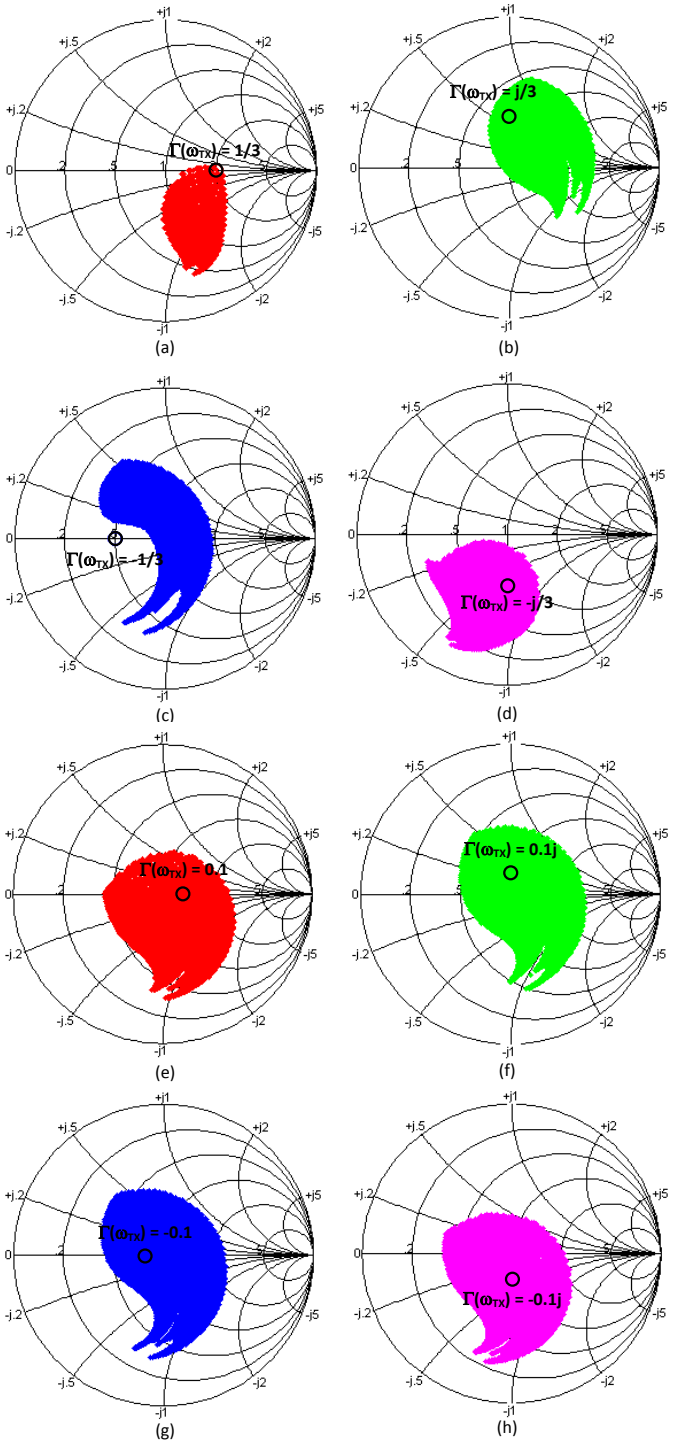

Figure 4.6: Range of impedance covered at RX frequency given certain $\Gamma(\omega_{TX})$ (a) $\Gamma(\omega_{TX}) = 1/3$. (b) $\Gamma(\omega_{TX}) = j/3$. (c) $\Gamma(\omega_{TX}) = -1/3$. (d) $\Gamma(\omega_{TX}) = -j/3$. (e) $\Gamma(\omega_{TX}) = 0.1$. (f) $\Gamma(\omega_{TX}) = 0.1j$. (g) $\Gamma(\omega_{TX}) = -0.1$. (h) $\Gamma(\omega_{TX}) = -0.1j$

Balance Network Linearity Requirement

The degree of linearity required by the balance network is investigated in Figure 4.7. Any intermodulation products generated in the balance network due to its nonlinearity will not be perfectly balanced on the antenna side which is mostly linear. This inter-modulation products will couple to the LNA input in the same manner as the received signal couples from the antenna, i.e. with ideally 3 dB power loss, degrading the effective isolation. To keep the coupled third-order intermodulation (IM3) distortion lower than the fundamental components leaked directly from the PA to LNA side, the balance network should satisfy

$$IM3_{BAL}(\text{dBm}) - 3\text{ dB} < P_{TX}(\text{dBm}) - 3\text{ dB} - ISOL_{TX-RX}(\text{dB}) \tag{4.7}$$

but

$$IIP3_{BAL}(\text{dBm}) = \frac{3}{2}\big(P_{TX}(\text{dBm}) - 6\text{ dB}\big) - \frac{1}{2}IM3_{BAL}(\text{dBm}) \tag{4.8}$$

thus

$$IIP3_{BAL}(\text{dBm}) > P_{TX}(\text{dBm}) + \frac{1}{2}ISOL_{TX-RX}(\text{dB}) - 9\text{ dB}. \tag{4.9}$$

For a maximum transmitter power of 27 dBm and to maintain 55 dB of isolation, the IIP3 of the balance network should exceed 45.5 dBm. This high linearity requirement was achieved by making use of highly linear switched capacitors and other fixed and linear passives in the implementation of the balance network. It was noticed in simulation that even a secondary effect like resistor self-heating, which is usually neglected, would hinder achieving such a high linearity. Wide enough resistor fingers should be used to minimize the self-heating and reach the required linearity.

High Voltage Switched Capacitor Unit Cell

The high voltage switched capacitor unit is shown in Figure 4.8, this differential implementation consists of two metal-insulator-metal (MIM) capacitors in series with a high voltage tolerant switch. The high-value resistors, are used to obtain an RF open while supplying dc bias. The bias conditions and capacitance values in both *on* and *off* states are described in Table 4.2.

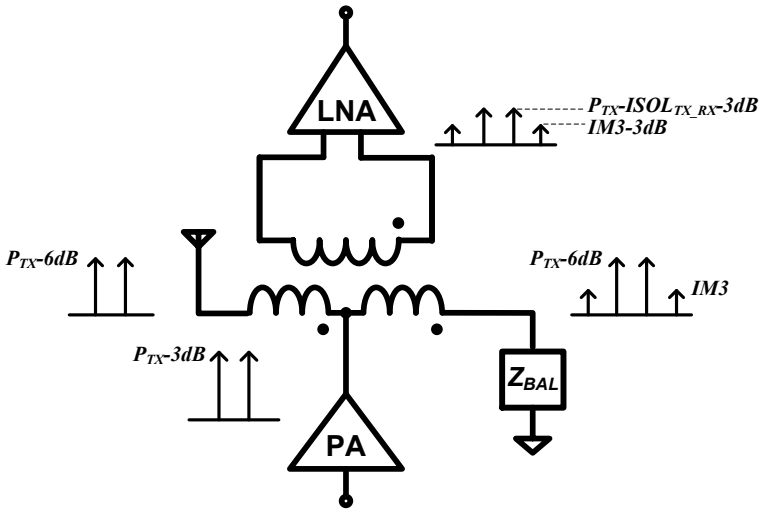

Figure 4.7: Nonlinearity generated in the balance network couples to LNA input.

Table 4.2: Bias conditions and capacitance value

State	Bias			Single-ended
	V_G	V_S, V_D	V_B	Capacitance
ON	V_{DDH}	0	0	C
OFF	0	V_o	0	$C//C_{par}$

The voltage swing across the switch transistor in the *off*-state condition is much larger than in the *on*-state. Thus, the power capability is mainly determined by the off-state. A potential problem arises when the switch is *off* and a large voltage swing appears across it. A stack of thick-oxide NMOS devices in deep n-well with RF floating gate and bulk allows the swing to almost split equally across them. A source/drain (S/D) bias (V_o) maintains the device and S/D to bulk junctions *off* to maintain high linearity. The operation is illustrated in Figure 4.9 and compared to less power tolerant implementations of the switch. To keep an *off*-state condition of the switch transistor, the positive peak of the voltage between the gate and source/drain (V_{gs} or V_{gd}) should be less than the threshold voltage (V_{th}), and the negative peak of the voltage between the source/drain and bulk (V_{sb} or V_{db}) should be less than the junction turn-on voltage (V_D). Otherwise, the switch transistor starts to turn on during some time periods causing high non-linearity.

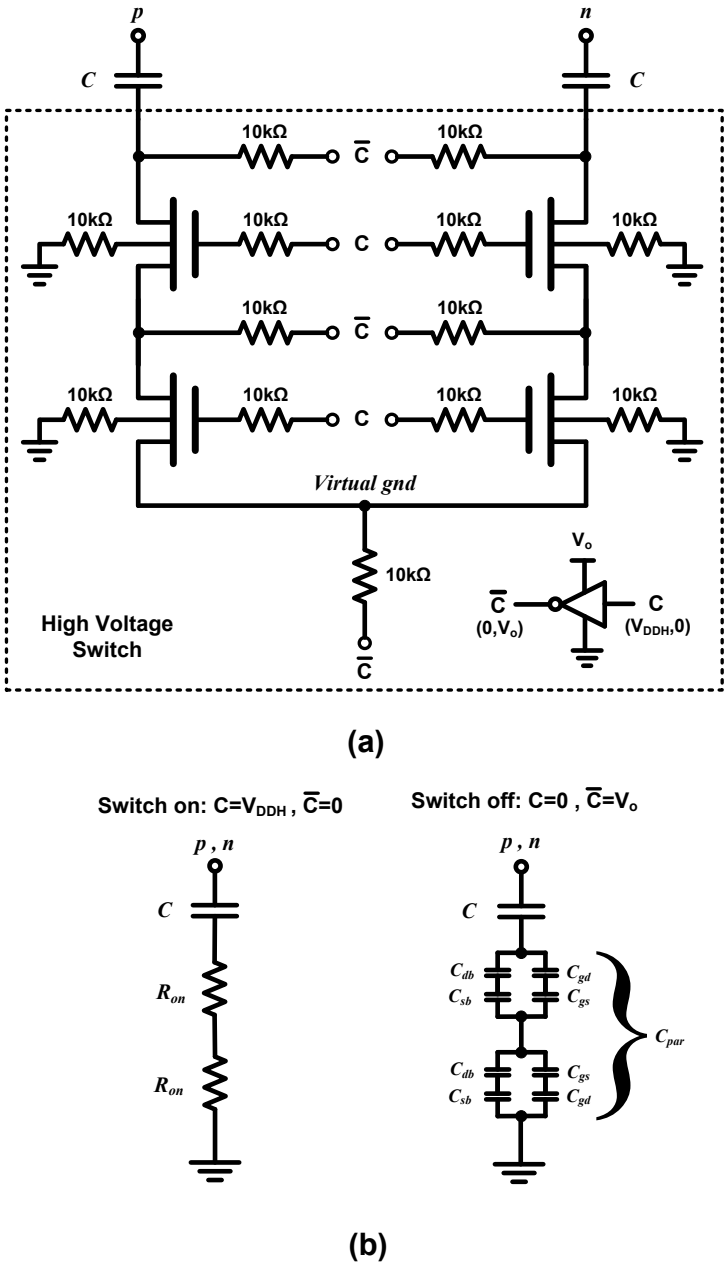

Figure 4.8: Differential high voltage switched capacitor (a) Schematic. (b)Equivalent circuit in *on* and *off* states.

A floating gate and bulk switch shown in Figure 4.9(b) would allow for double the voltage swing when compared to Figure 4.9(a), as the swing splits between V_{gs} and V_{gd} and similarly between V_{sb} or V_{db}.The structure in Figure 4.9(c) has a reverse

dc bias of V_o across the gate/bulk to source/drain, thus the swing is now limited by

$$V_{max} = 2n \times Min\Big[(V_o + V_{th}), (V_o + V_D)\Big]. \tag{4.10}$$

where n is number of stacked devices and V_o is the S/D DC bias. One limit is dictated by the NMOS device turning *on* and the other is by the S/D-to-bulk junction turning *on*. The value of V_o and n is chosen so that V_{gs} or V_{gd} across any device will not exceed the oxide breakdown reliability limit under maximum transmit power of 27 dBm. Consequently, the power capability of that structure in Figure 4.9(c) is decided by the device breakdown, which is the maximum achievable limitation, while that of the conventional structures in Figure 4.9(a) and (b) is determined by channel formation of the *off*-state switch. With the the improved power capability compared to the conventional structures, the floating gate/bulk switch with S/D bias should show improved linearity characteristics in the high-power region. In addition, the p-n junction is reverse-biased by V_o in that structure, while it is zero-biased in the conventional ones. Thus, the proposed structure improves linearity in the low-power region by shifting the bias condition, that minimizes the non-linear depletion capacitance of these junctions. Similar voltage enhancement and linearization techniques were used before in [40, 39].

In the previous discussion leading to (4.10), the effect of the deep n-well to substrate junction capacitance has been neglected. The cross-section of an NFET device in deep n-well is illustrated in Figure 4.10(a). The deep n-well to substrate junction capacitance in series with the bulk (p-well) to deep n-well capacitance causes the bulk terminal not to be completely floating at RF frequencies. This causes higher V_{db} and V_{gd} swing than V_{sb} and V_{gs} respectively as shown in Figure 4.10(c). This is an importent limitation for bulk CMOS processes when compared to an SOI process where the bulk can be made completely floating due to the barried oxide layer. If no proper layout that minimizes the deep n-well to substrate capacitance is practiced, this effect might limit the maximum swing across the device in the *off* state further than dictated by (4.10) and, even worse, would make stacking less effective. Using multiple fingers for the device, while sharing the same deep n-well, helps reduce the overhead in the n-well junction area. This together

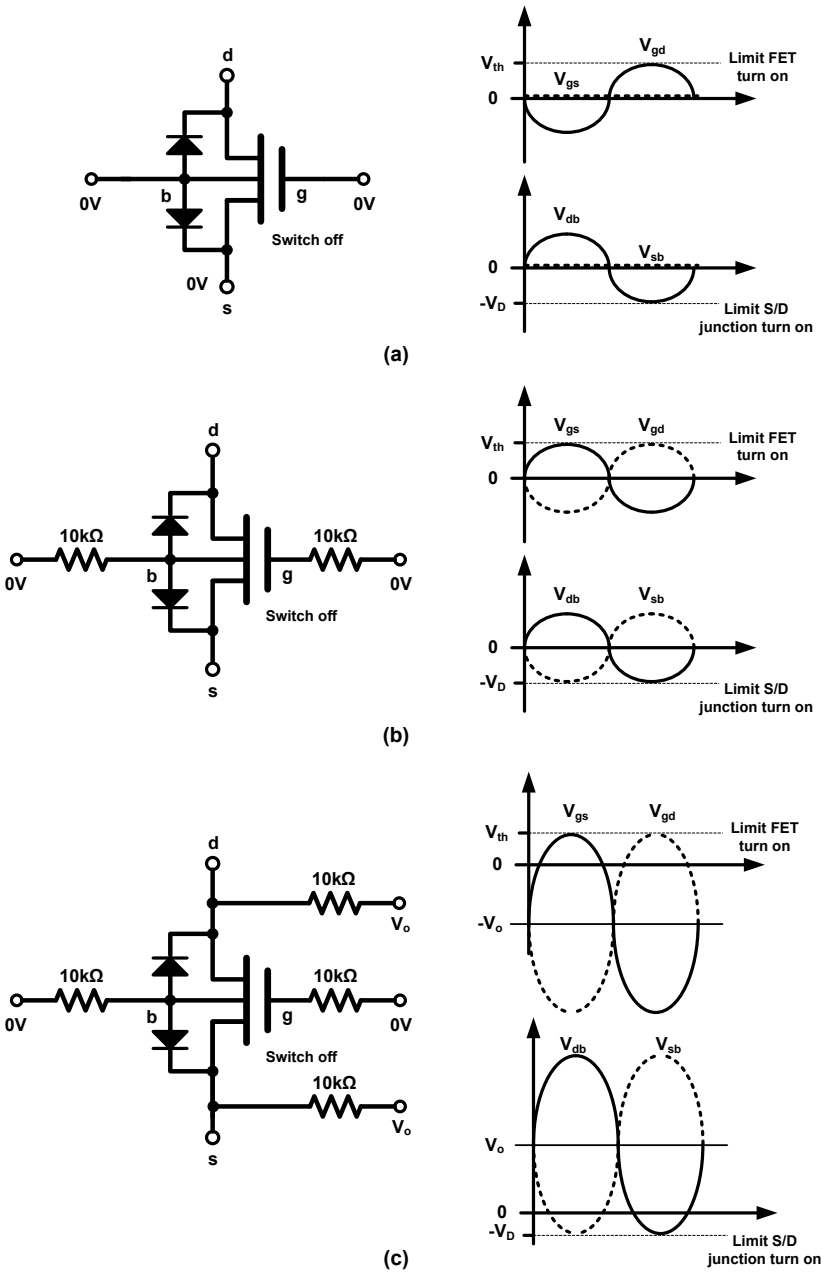

Figure 4.9: High voltage switch operation and waveforms (a) Conventional switch. (b) Floating gate/bulk switch. (c) Floating gate/bulk switch with S/D bias.

with a high reverse bias across the deep n-well to bulk/substrate, by raising the deep n-well bias, minimizes this effect. In this implementation, the minimum deep

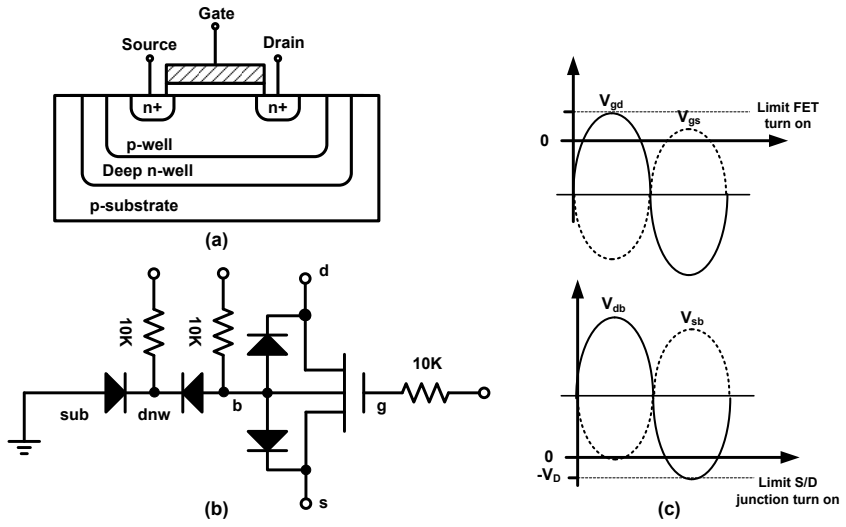

Figure 4.10: Deep n-well to substrate junction capacitance effect (a) Device cross-section. (b) Equivalent circuit. (c) Waveforms

n-well area allowed by the design rules was used and biased at 3.6 V.

Quality Factor and Tuning Range Tradeoff

Two important parameters for the switched capacitor are the quality factor in the *on* state (Q)and the capacitance ratio between the *on* and *off* states, i.e. the tuning range (C_{max}/C_{min}). Both high-Q and wide tuning range are desirable to cover a wide range of impedance on the Smith chart by the balance network. However, a tradeoff between the two exists. Since no dc current flows through the capacitor, no dc current flows through the transistor switch either. The drain-source dc voltage must then equal zero and the transistor will accordingly be operating in the triode region. And as long as Q is high enough, the RF swing across the switch when *on* should be small, thus the transistor remains in deep triode region. In the *on* state, the transistor can be replaced by its drain-source on resistance as shown in Figure 4.8(b) and given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{4.11}$$

where μ_n is the electron mobility, C_{ox} the gate oxide capacitance per unit area, W and L the width and length of the transistor, and V_{GS} and V_{th} the gate-source and

threshold voltage, respectively.

Since Q is given by

$$Q = \frac{1}{n\omega C R_{on}} = \frac{\mu_n C_{ox} W (V_{GS} - V_{th})}{nL\omega C} \tag{4.12}$$

where n is number of stacked devices, it is clear that Q is increased for wide and short transistors driven at a high gate voltage. For best performance, the length selected should be as short as possible and the gate voltage as high as possible. The width, however, will be used as a tradeoff between Q and tuning range. While n is determined by the largest RF swing at maximum transmit power in the *off* state and oxide reliability constrains as will be explained in the next subsection.

In the *off* state, the device resistance is very large and has no influence on the impedance. Instead, the drain-bulk/gate capacitances (C_{db}, C_{gd}) and source-bulk/gate capacitances (C_{sb}, C_{gs}), which may be omitted in the *on* state, dominate as shown in Figure 4.8(b). The drain-bulk and source-bulk capacitance is due to the reverse biased p-n junction formed by the p-doped substrate and the n-doped source/drain, and is given by

$$C_{db} = C_{sb} = WC_j \tag{4.13}$$

Wher C_j is the junction capacitance per unit width, whereas the gate-drain and gate-source capacitance is due to the gate oxide capacitance. Due to the source/drain bias applied in the *off* state, the dc gate-source/drain voltage (V_{GS} and V_{GD}) is negative forcing the device into accumulation [38]. In this mode the total gate to channel capacitance ($C_{ox}WL$) can be split into two equal capacitors from the gate to the souce and drain

$$C_{gs} = C_{gd} = \frac{1}{2} C_{ox} WL + C_{ov} W \tag{4.14}$$

Wher C_{ov} is the overlap capacitance per unit width due to the gate region that extends beyond the channel and overlaps the source and drain. The sum of all these parasitic capacitances is equal to

$$C_{par} = \frac{C_{db} + C_{gd}}{2n} = \frac{1}{2n}\big(C_j + \frac{1}{2} C_{ox} L + C_{ov}\big) W \tag{4.15}$$

When the switch is OFF, a series connection is formed with the switched C and the parasitic capacitance C_{par} giving a minimum capacitance equal to $C//C_{par}$ and a tuning range

$$\frac{C_{max}}{C_{min}} = C\Big(\frac{1}{C} + \frac{1}{C_{par}}\Big) = 1 + \frac{C}{C_{par}}. \tag{4.16}$$

From (4.12) and (4.16), since the parasitic capacitance is proportional to the width of the transistor (4.15), a wide transistor increases Q, but also increases the *off* capacitance, which in turn decreases the tuning range. This leads to a compromise between quality factor and tuning range.

Switch Reliability

When the switch is turned *on*, a small V_{ds} appears across it; however to achieve low on resistance for the switch, which helps improving Q, maximum possible V_{GS} is used. When the switch is off, a large V_{ds} and V_{gs} swing will appear across it. To limit the possibility of oxide breakdown, the reliability information supplied by the foundry is used to assure not exceeding the safe operation limits at maximum PA transmit power. It should be mentioned that hot carrier effects does not constitute a threat in this case; as the devices operate as a switch with either very small V_{ds} when *on* or no current when *off*.

Gate dielectric integrity is mainly driven by random process defects. Therefore, reliability failure rates depend on the total gate-oxide area. To reduce the impact of reliability failures caused by these defects, the following rules must be observed. IBM CMOS 10LPe, a 65 nm bulk CMOS process, offers two gate dielectric thicknesses: a thin oxide device with 1.8 nm gate dielectric, and a thick oxide device with 5.2 nm gate dielectric. The maximum permitted voltages across the gate dielectric are defined as follows [48]:

V_{max}: Maximum permitted dc voltage without transients.

V_{os}: Maximum permitted transient voltage when used with a maximum high level of V_h ($V_h < V_{max}$).

The equations below calculate the maximum voltages as a function of lifetime in K power-on-hours ($KPOH$), maximum junction temperature (T_j), and total gate

area for each device type listed in Table 4.3 [48]

$$|V_{max}| = V_{ref} \times \Big(\frac{100 \times A_A \times A_T}{KPOH \times D_f}\Big)^{\frac{1}{N}} \tag{4.17}$$

$$|V_{os}| = |V_h| \times \Big[\frac{100 \times A_A \times A_T \times A_V - (KPOH \times D_f) + t_{os}}{tos}\Big]^{\frac{1}{N}} \tag{4.18}$$

where

$$\begin{aligned} A_A &= \Big[\frac{Area(mm^2)}{Aref}\Big]^{\frac{-1}{B}} \\ A_T &= exp\Big[\frac{E_a}{8.62 \times 10^{-5}} \times \big(\frac{1}{T_j(K)} - \frac{1}{398}\big) + \frac{E_b}{8.62 \times 10^{-5}} \times \big(\frac{1}{T_j^2(K)} - \frac{1}{398^2}\big)\Big] \\ A_v &= \Big(\frac{|V_h|}{V_{ref}}\Big)^{-N} \\ t_{os} &= KPOH \times S_f \times D_{os}. \end{aligned} \tag{4.19}$$

D_f is the fraction of the product lifetime with a dielectric voltage at V_h or switching to V_h, S_f is the fraction of the total cycles where overshoot occurs when a switch to V_h occurs, and D_{os} is the fraction of a switching cycle where the voltage across the dielectric exceeds V_h. The constants V_{ref}, N, A_{ref}, B, E_a, and E_b are listed in Table 4.3 for each device type. Exceeding these maximum conditions can result in severe device degradation and gate-oxide failure.

Table 4.3: Gate oxide reliability parameters [48].

Device	V_{ref}	N	A_{ref}	B	E_a	E_b
1.8 nm NFET	1.32	45	1.27×10^5	1.35	0.41	0
5.2 nm NFET	3.6	36	0.2	3.25	0.42	0

Figure 4.11 plots V_{max}, the maximum dc voltage across the gate oxide, for thin and thick oxide devices againist the device area for 5 and 10 years lifetime from (4.17). To be able to tolerate larger swings, the thick oxide device with a turn on voltage of 3.6 V is used in the high voltage switch capacitor. This guarantees low *on* resistance and hence high Q, while having more than 100 mV of margin for a device area between 100 and 10,00 μm^2 and 10 years lifetime.

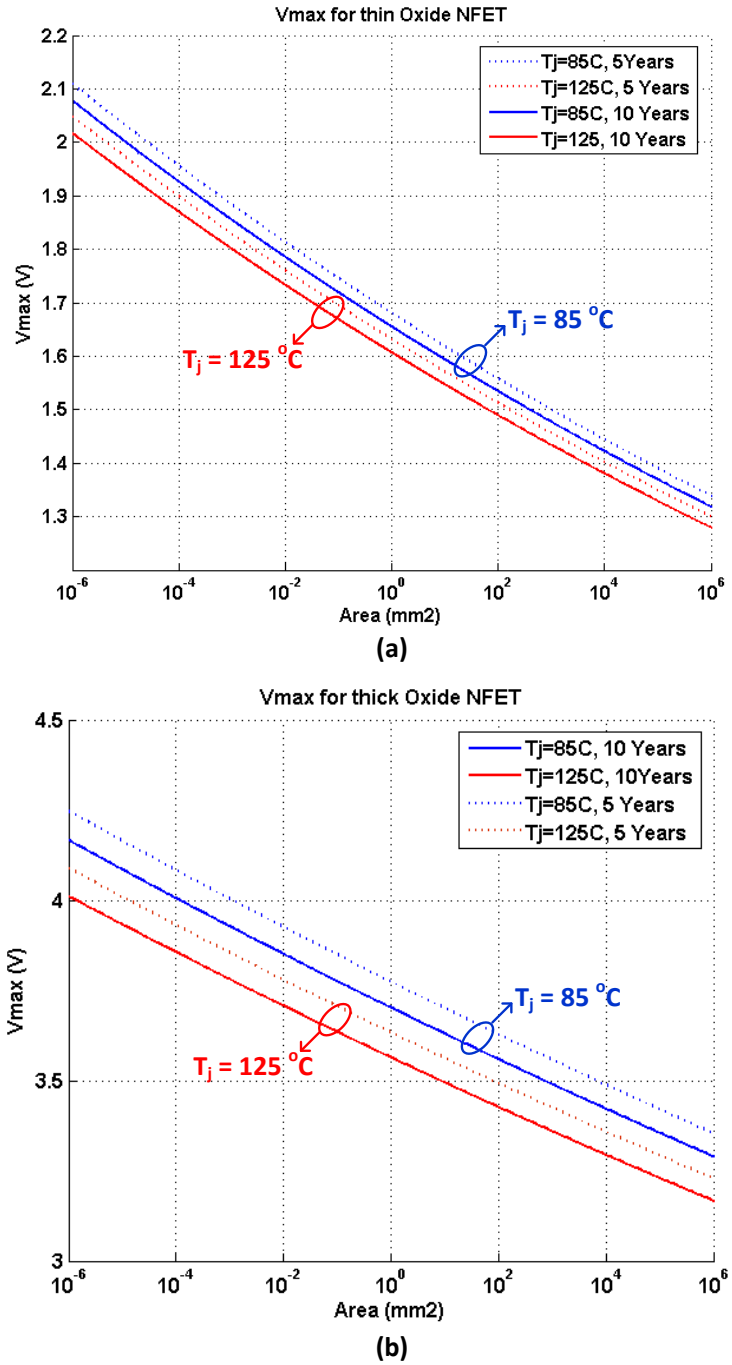

Figure 4.11: Maximum dc voltage across gate oxide. (a) Thin oxide device. (b) Thick oxide device.

To analyze the oxide stress under RF swing, the voltage waveforms for V_{gs} and V_{gd} can be approximated as shown in Figure 4.12(a). The RF signal is approx-

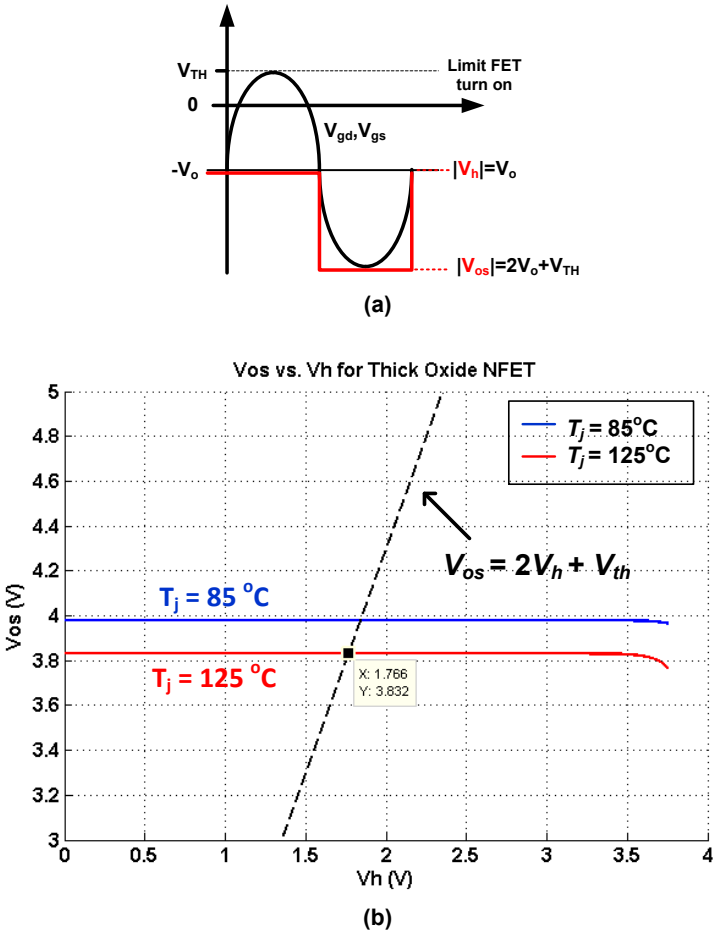

Figure 4.12: (a) RF stress approximation. (b) Graphical solution for maximum RF swing.

imated by a square wave whose lower value corresponds to V_h and maximum value correspond to V_{os} in (4.18), this is a conservative approximation of the sinusoidal RF signal. Relating the values for the swing and dc S/D bias to V_h and V_{os} gives

$$\begin{aligned} |V_h| &= V_o \\ |V_{os}| &= 2V_o + V_{th}. \end{aligned} \tag{4.20}$$

Solving (4.18) with (4.20) gives the largest possible signal swing across one device while not exceeding the oxide reliability limits. This is done graphically in Figure 4.12(b) for a thick oxide device; an RF swing of 4 V is achievable per device. To be able to withstand a maximum RF transmit power of 27 dBm to the antenna

under a VSWR of 2:1 the maximum differential swing across the antenna, and similarly the balance network, would be 14 V. This requires four stacked devices in the differential switch shown in Figure 4.8.

Full Implementation

The balance network in Figure 4.3 was implemented in a 65 nm CMOS process. Instead of using six inductors, the differential implementation made use of three transformers to save area. The mutual coupling between the windings of the transformer can be used to increase the effective differential inductance, hence further reducing the area and improving the achievable quality factor (Q). The transformer windings used the two thick top metal layers stacked together, a 3 μm thick Copper and 4 μm thick Aluminum connected with a bar via, to reduce the metal resistance and improve Q. With an outer diameter of 400 μm, turn width of 12 μm, spacing of 3 μm and 1.5 turns, the inductance was 2.88 nH with a Q of 22.7 at 2 GHz and a self-resonance frequency of 3.55 GHz.

The variable capacitors C_1, C_2, C_3 and C_4 in Figure 4.3 were implemented using high voltage switched capacitor banks built using the cell in Figure 4.8 as a unit cell. Each of the capacitors is implemented as a 7 bit capacitor bank with the four least significant bits binary weighted and the three most significant bits thermometer coded to guarantee monotonicity. The capacitor resolution was 25 fF to allow for high resolution in the overall balance network impedance. The achieved tuning range was 2.8 with a Q factor higher than 35.

Figure 4.13 shows the simulated IIP3 of the balance network. The input power is swept and the resulting power at the fundamental frequency and third-order intermodulation product is plotted. An IIP3 of 54 dBm is achieved which exceeds the requirement of 45.5 dBm from (4.9). Reducing the width of the termination resistor would magnify the effect of self-heating and reduce the IIP3 of the balance network to 40 dBm.

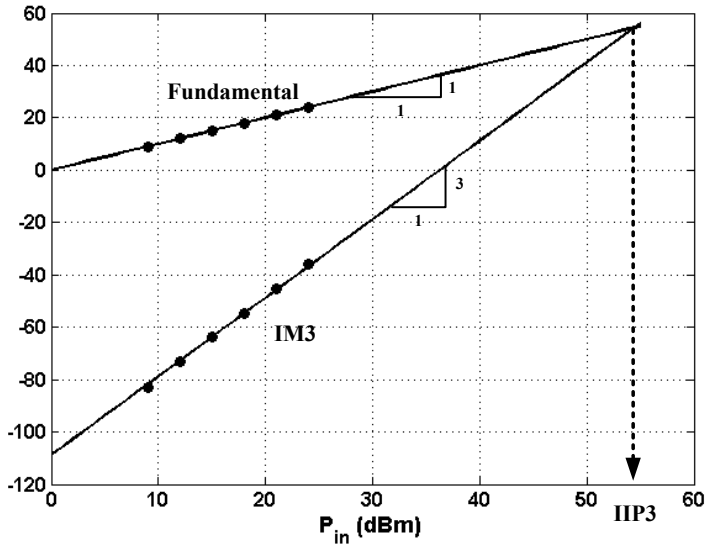

Figure 4.13: Simulation of balance network IIP3.

4.2.2 Direct-Conversion Receiver Design

A relaxed performance receiver could be used for the TX leakage detection. But in this implementation, a receiver with typical WCDMA/LTE performance requirements is designed to test the overall performance with the integrated duplexer. In a more complete implementation that allows concurrent reception and duplexer loop calibration, the output current of the main LNA can be tapped and directed to a downconversion mixer using the TX LO for the calibration loop besides the normal RX LO driven mixer for reception. As shown in Figure 4.2, the LNA acts as a transconductor that converts the input voltage to current for a current-mode passive mixer for downconversion. Finally a TIA provides some filtering and converts the signal back to voltage. The mixer is driven with a 25% duty cycle LO generated on-chip from twice the LO signal. The voltage conversion gain of the receiver is a function of the passive gain of the hybrid transformer (N_2/N_1), LNA transconductance (G_m), mixer conversion loss and TIA feedback resistor (R_F) and is given by

$$A_v = \frac{2\sqrt{2}}{\pi}\frac{N_2}{N_1}G_m R_F \tag{4.21}$$

The LNA, shown in Figure 4.14, is a noise-matched LNA [13, 32]. The

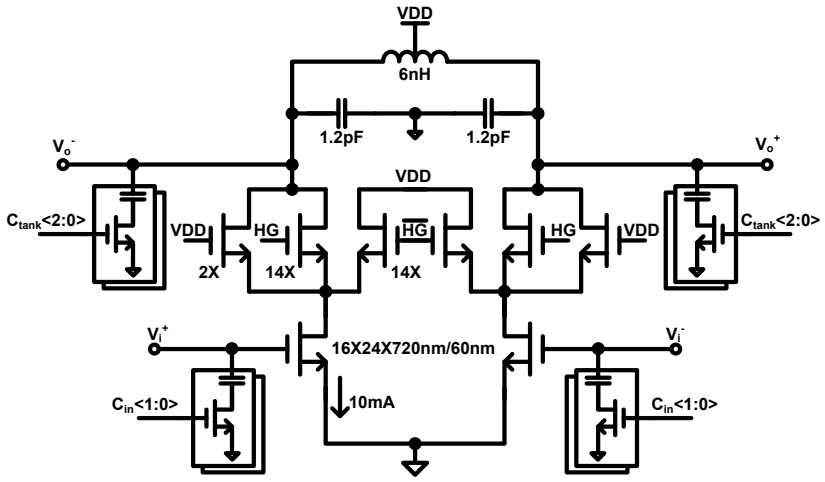

Figure 4.14: Noise matched LNA with gain programmability.

duplexer inductance resonates the LNA input capacitance to maximize the passive voltage gain in front of the LNA, thus minimizing its noise contribution. A switched capacitor at the input is used to tune that resonance across the operating frequency range. Two gain modes are provided using current steering in the cascode devices to reduce gain at high TX leakage so that the TIA output will not saturate. A tuned tank load is used to maximize the source impedance seen by the mixer at the RF frequency which helps minimize the TIA noise contribution and improves linearity [49, 5].

Figure 4.15 shows the schematic for the mixer and TIA. A current-mode passive mixer achieves high linearity and low flicker noise, as no DC current flows in the switches. The LO is AC coupled to the mixer switches with the DC level offsets to calibrate the mismatches in order to minimize second-order intermodulation distortion. The TIA provides a low input impedance across the channel bandwidth. At higher frequency (e.g. at the TX jammer offset), as the TIA gain decreases, the added capacitor at the TIA input reduces the input impedance to maintain good linearity. The TIA has a single pole at 2.5 MHz to provide low-pass filtering.

A fully differential two stage amplifier is used in the TIA as shown in Figure 4.16. For common-mode feedback (CMFB), the output common-mode voltage is sensed using two resistors, compared to a common-mode reference in a differential amplifier with diode connected pmos load, and a feedback signal connects to

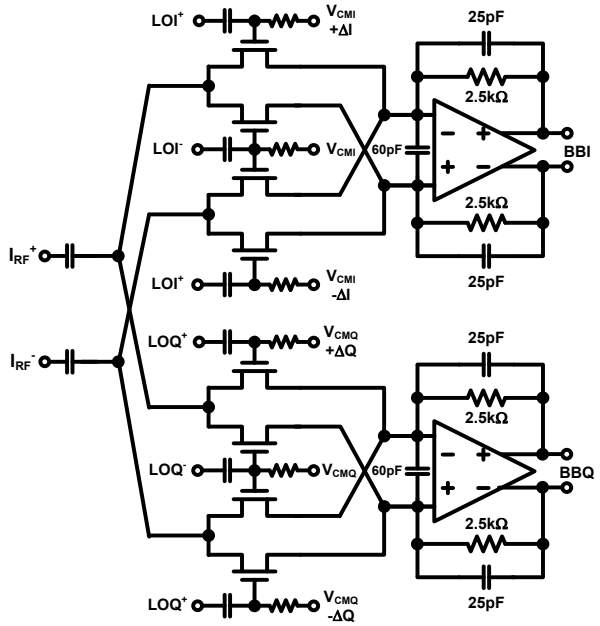

Figure 4.15: Current mode passive mixer with 25% LO duty cycle drive and output TIA.

the pmos load current source in the first stage of the amplifier. The amplifier is compensated using traditional Miller compensation and has 56^o and 58^o of phase margin in the differential and common-mode feedback loops respectively.

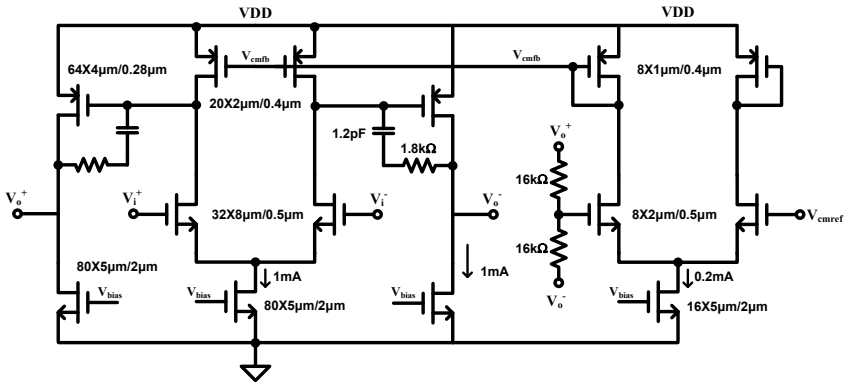

Figure 4.16: Two-stage amplifier with CMFB used in the TIA.

The 25% LO duty cycle reduces the interaction between the I and Q channels and provides 3 dB higher gain [49, 50]. Since the I and Q pulses do not overlap, as shown in Figure 4.17, the full RF current passes through each double-

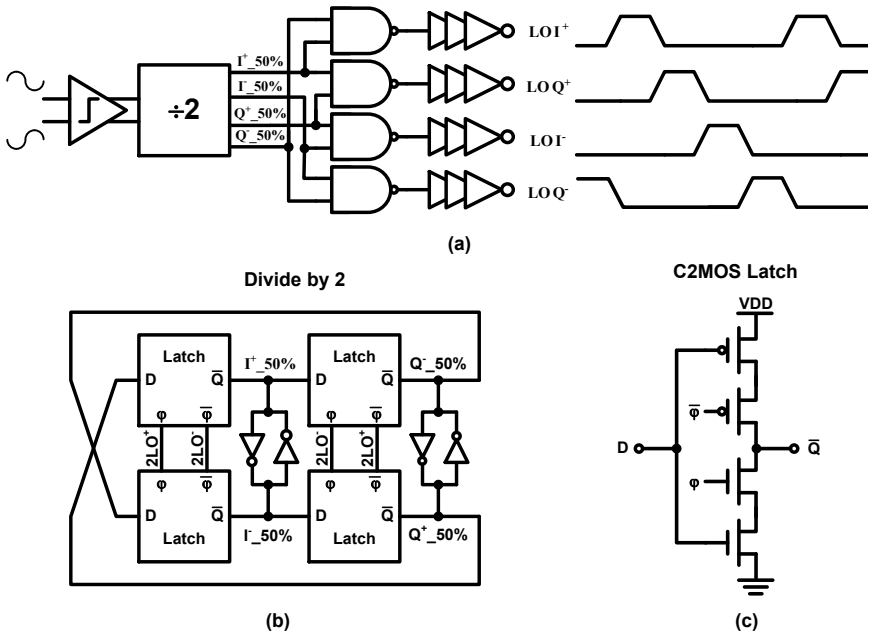

Figure 4.17: (a) 25% duty cycle LO generation. (b) Divide by 2 schematic. (c) Dynamic C^{2}MOS latch used in divider.

balanced mixer separately as opposed to being split between the I and Q mixers; as in receivers with 50% duty-cycle LO signals. The circuit for LO generation is shown in Figure 4.17. The input sinusoidal signal at twice the required frequency is amplified and applied to a divide by 2 divider to generate the 50% duty cycle I and Q LO signals, which are anded to generate the 25% duty cycle LO. The divider is a simple master slave flip-flop implemented with dynamic C^{2}MOS latches and connected in differential manner to generate the differential phases. Small cross-coupled inverters are used to guarantee differential phases and proper startup. Figure 4.18 shows the simulated phase noise at the output. At 80 MHz offset which is the smallest duplex offset for bands between 1.7 and 2.2 GHz (PCS band case), the phase noise is -159.6 dBc/Hz. That is sufficient so as not to degrade the noise figure due to reciprocal mixing with the TX leakage by more than 0.2 dB as was calculated in Chapter 1.

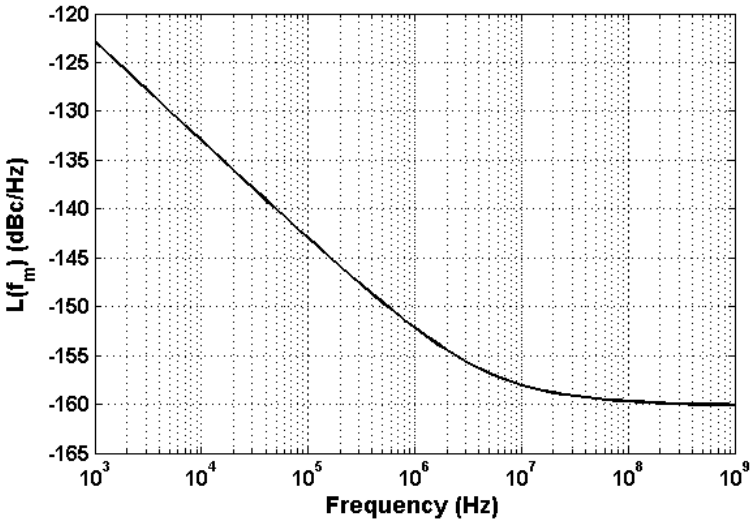

Figure 4.18: Simulated LO phase noise.

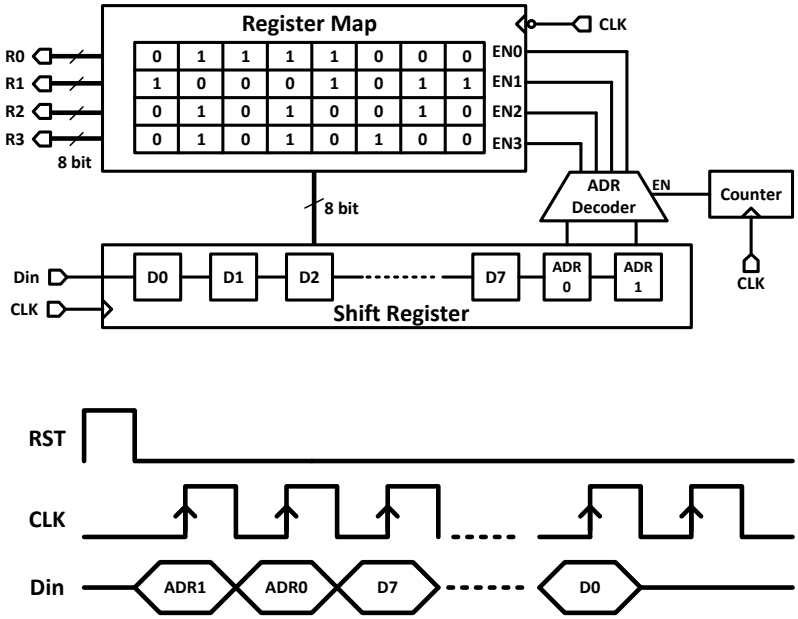

Figure 4.19: Serial to parallel interface.

4.2.3 Serial to Parallel Interface

To be able to program the digital controls on the chip without bringing out too many digital pins, a serial to parallel interface was implemented as shown in Figure 4.19. The serial input data (Din) is sampled at the rising edge of the

serial interface clock (CLK) into a shift register. The input data stream has two bits for address and eight bits of data, to be loaded into one of a 4×8 bit register map. After the 10 bits of data and address are shifted into the shift register, a counter enables the address decoder to decode the address bits and enable the corresponding register in the register map, and on the following falling edge the data is loaded to that register in parallel. The same method can be used to load the desired data into any of the registers by using the proper address. Each register is then hardwired to different digital controls within the chip. All blocks were implemented using a custom static CMOS design and operation was verified at 100 MHz clock frequency in post layout simulations.

4.3 Measurement Results

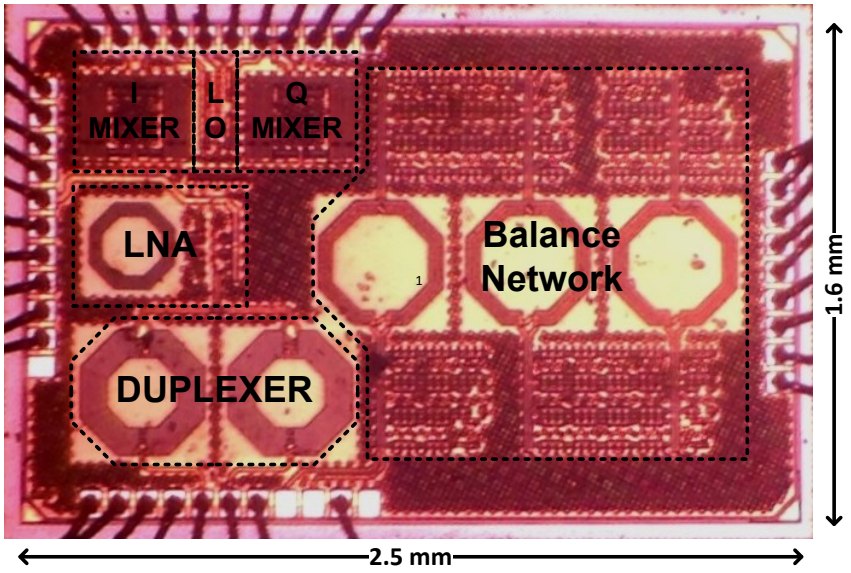

Figure 4.20: Die microphotograph.

The differential duplexer based on hybrid transformer with the newly proposed balanced network and cascaded with a direct conversion receiver was implemented in a 65-nm CMOS process occupying an active area of 2.2 mm^2. Figure 4.20 shows the die microphotograph. The die was packaged in a 40 pin QFN plastic package and mounted on an FR4 board for testing.

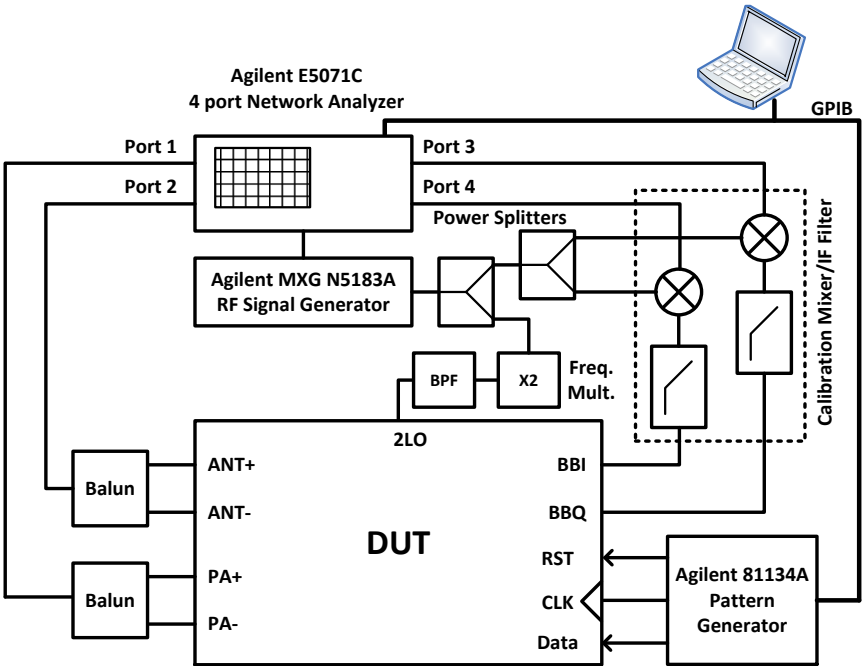

Figure 4.21: Small signal measurement setup.

On board a set of two high speed instrumentation amplifiers with unity gain were implemented using AD8045 low distortion high speed amplifiers and precision feedback resistors. These instrumentation amplifiers can convert the baseband I and Q outputs from differential to single-ended with negligible added distortion and noise and high common-mode rejection. They also have enough drive strength to directly drive the measurement instrumentation with 50 Ω input impedance. Also on board, a high frequency surface mount balun was used to convert the twice LO signal from single-ended to differential. A low amplitude and phase error balun, BD3150N50100A00 from Anaren, was used. Amplitude and phase error in the differential twice LO signal convert into quadrate error between the I and Q LO signals after the divider and should be minimized to reduce the quadrature error. Such an error could be better controlled in a fully integraed implementation with the frequency synthesizer included on-chip with a differential VCO.

Figure 4.21 shows the testing setup used for small-signal characterization. A four port network analyzer, Agilent E5071C, was used. Vector mixer calibration (VMC) of the network analyzer was used to be able to measure the relative phase

between the I and Q baseband signals [51]. VMC requires a calibration mixer and IF filter for up/down conversion so that all measurements by the analyzer are done at RF frequency. The calibration mixer and IF filter are characterized during calibration, and afterward de-embedded from the measurements using the fixture simulator function of the network analyzer. Other fixture analysis options allow for de-embedding the baluns and changing the port impedance. The network analyzer controls another RF signal generator to generate the LO signal to the calibration mixers and the mixer under test. As the chip expects twice the LO, a frequency multiplier and BPF were used to generate twice the LO signal for the chip. To program the chip through the serial interface, Agilent 81134A pulse/pattern generator was used to generate the clock and data signal in a manner similar to that shown previously in Figure 4.19. All the equipment where controlled from a computer running a Matlab program to automate the measurement through a GPIB interface. The graphical user interface for the matlab program is shown in Figure 4.22.

The calibration algorithm was implemented in Matlab using a genetic algorithm for global optimization of the balance network settings. The genetic algorithm creates a random starting population and the population keeps evolving to reach final population whose lowest value is the final solution and most probably is the global minimum of the optimization function. The algorithm is used to minimize the highest of the negative of TX-RX isolation at the TX and RX frequencies i.e. $\max(-ISOL_{TX-RX}(f_{TX}), -ISOL_{TX-RX}(f_{RX}))$. For each function evaluation, the corresponding C_1, C_2, C_3 and C_4 settings of the balance network are written to the chip through the serial interface, then isolation is measured using the network analyzer. The measured TX-RX isolation is shown in Figure 4.23. More than 50 dB of isolation is achieved at the TX and RX frequencies concurrently. Antenna VSWR up to 2:1 was measured. For each antenna impedance, the calibration algorithm optimizes the balance network settings to achieve the best isolation. The isolation bandwidth becomes narrower for higher antenna VSWR, but still the isolation bandwidth where $ISOL_{TX-RX} > 50$ dB is more than 6 MHz, which is sufficient for WCDMA and LTE 5 MHz standards but might not be suffi-

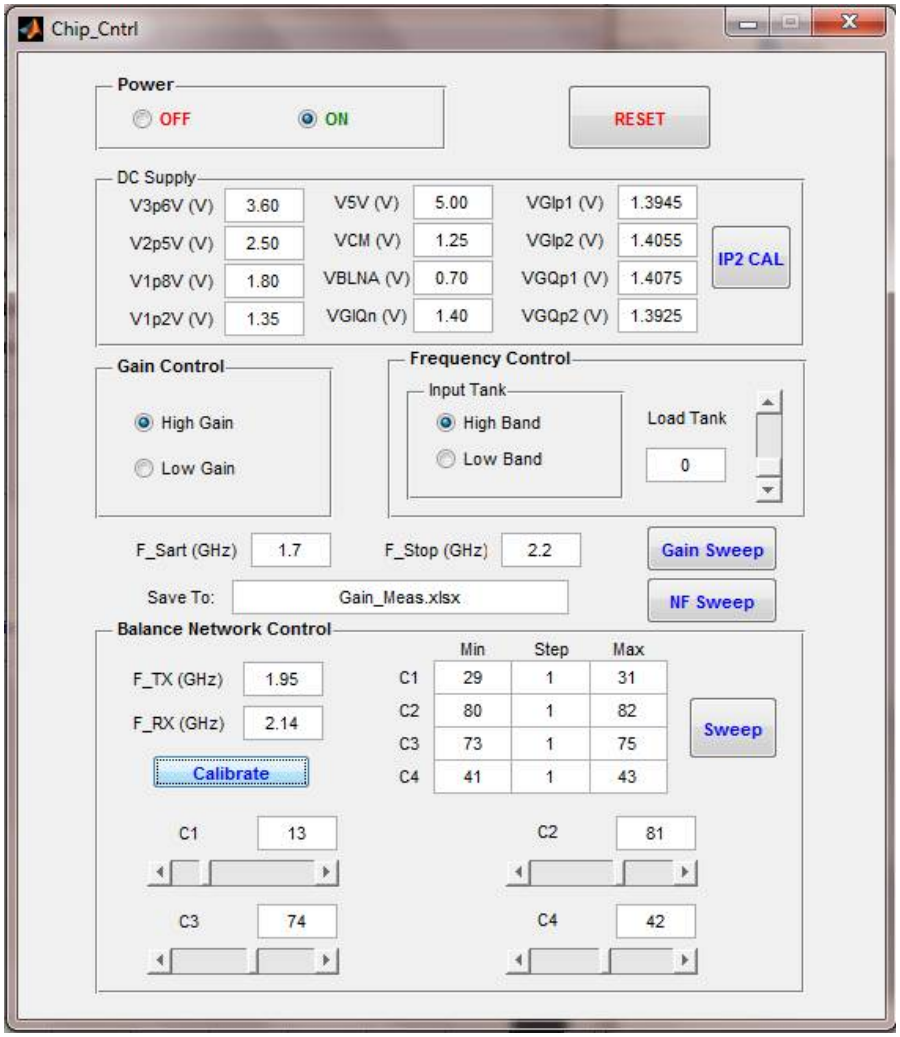

Figure 4.22: Measurment software.

cient for wider channel bandwidth standards unless the isolation requirements are relaxed.

Figure 4.24 shows the TX insertion and return loss, and the voltage conversion gain and noise figure in the RX path. The TX insertion loss was less than 3.8 dB. The power splitting between the antenna and balance network keeps the TX insertion loss at least 3 dB (in the symmetric transformer case), which means that the additional implementation loss due to the transformer winding resistance is less than 0.8 dB. Roughly 45 dB of gain was achieved with a cascaded noise figure around 5.3 dB. Also given that the integrated duplexer insertion loss is about

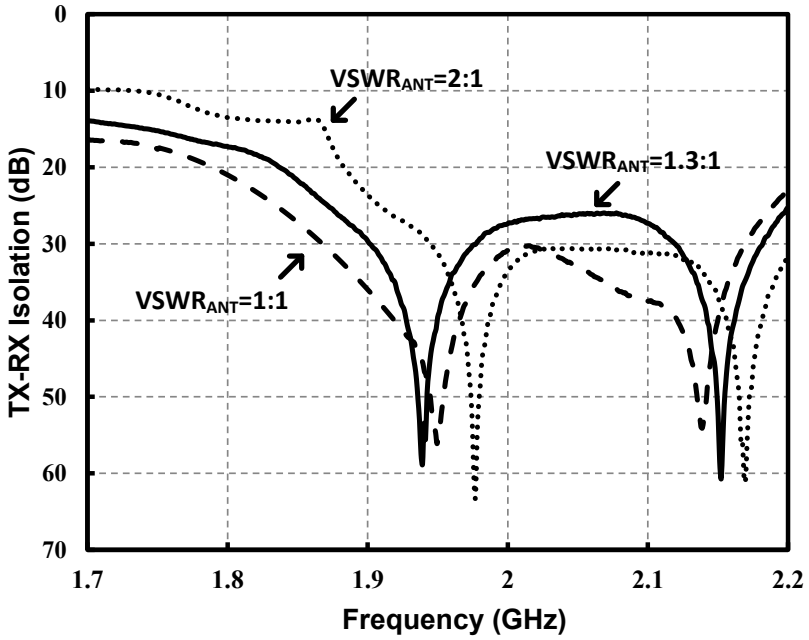

Figure 4.23: Measured TX-RX isolation for different channels and $\mathrm{VSWR_{ANT}}$.

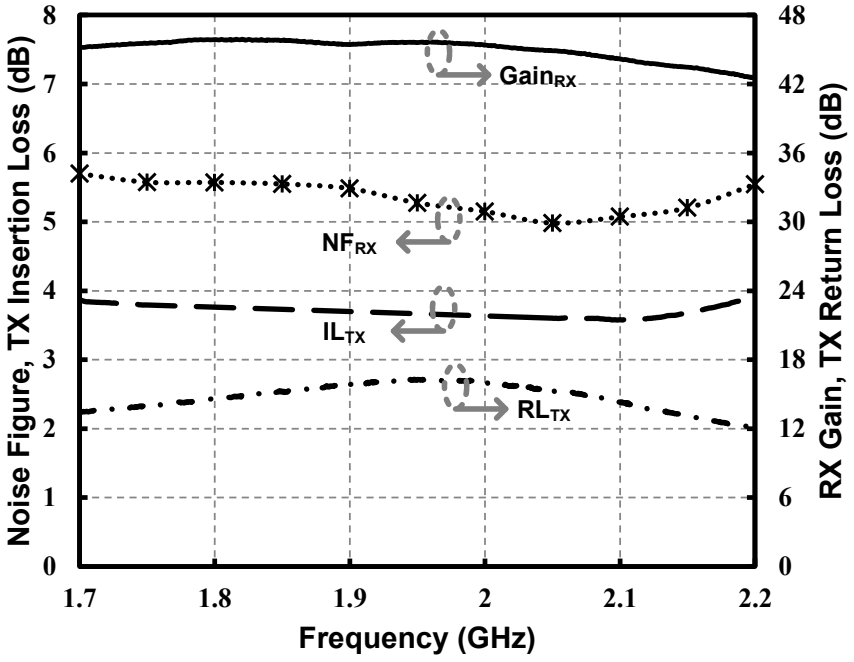

Figure 4.24: Measured RX gain, noise figure, TX insertion and return loss.

4 dB, means that the receiver noise is only 1.3 dB, thanks to the noise matched LNA and very small contribution from the baseband TIA.

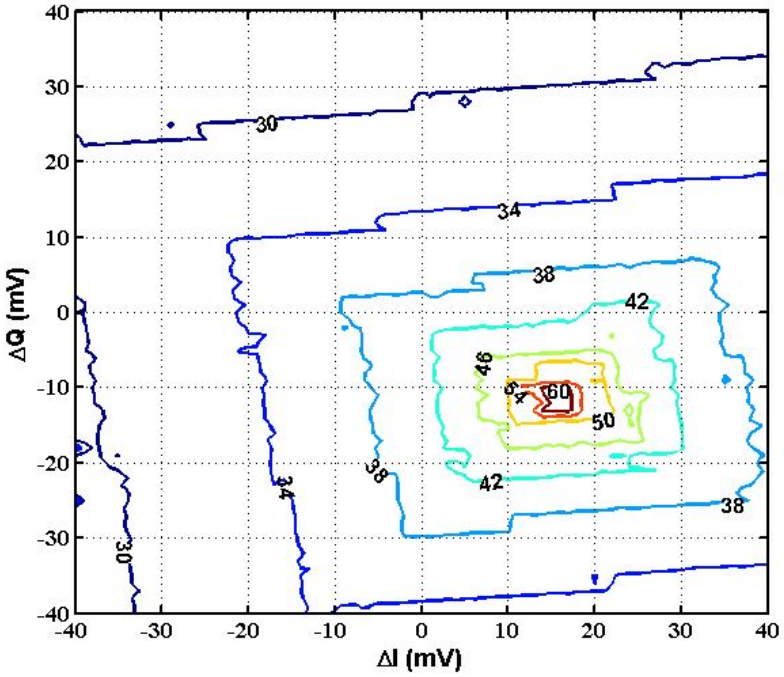

Figure 4.25: Receiver IIP2 calibration contours.

The IIP2 of the fully differential receiver is only limited by mismatches in the mixer. To keep the LO power consumption low, the mixer devices uses minimum channel length. The mismatches in these devices are calibrated by introducing an offset in the dc levels of the LO signal. Due to some interaction between the I and Q channels, offset in one channel affects the IIP2 of the other. Figure 4.25 shows the IIP2 calibration contours generated by sweeping the DC offset in the I and Q mixers shown in Figure 4.15 and plotting the minimum of the IIP2 measured in the I and Q channels. An uncalibrated IIP2 of 40 dBm was measured, and more than 60 dBm can be achieved after calibration.

Large signal isolation and balance network linearity are verified in Figure 4.26. A two-tone TX signal of 24 dBm each, i.e 27 dBm total TX power, is used and the TX LO downconverts any signal that couples to the LNA to baseband. The baseband output spectrum is shown. Given that the measured receiver gain at that frequency was 43.6 dB, this case corresponds to a TX-RX isolation of 61.7 dB (5.9 dBm − 24 dBm −43.6 dB). The third-order distortion in this case

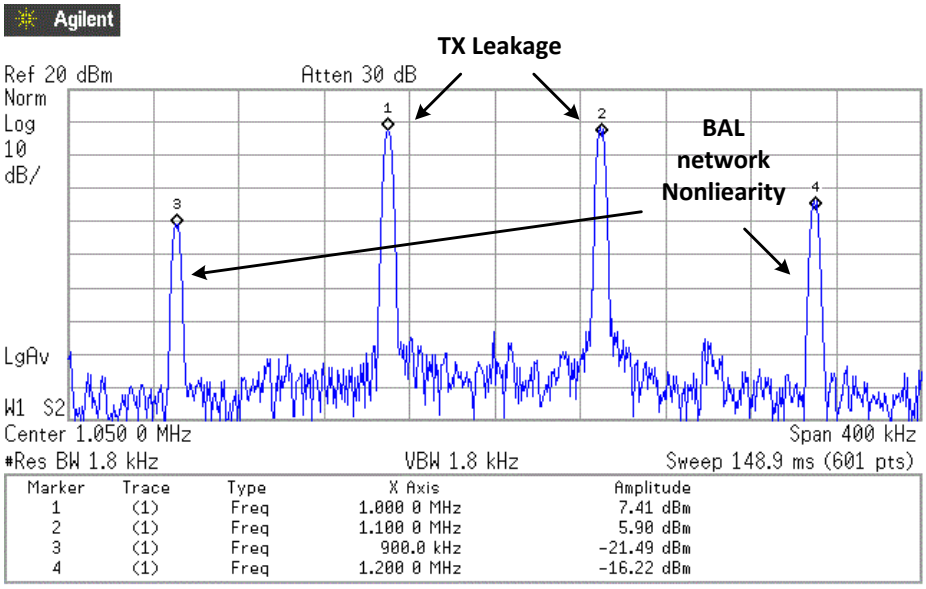

Figure 4.26: Output spectrum under two-tone TX input ($P_{TX,total} = 27$ dBm).

and at these power levels is dominated by the balance network nonlinearity and not the receiver. As was discussed in the previous section distortion generated in the balance network would couple with little isolation to the LNA input. As shown the coupled distortion is at least 10 dB lower than the fundamental components, confirming that isolation is not compromised, thanks to the high balance network linearity achieved.

Figure 4.27 shows the receiver IIP3 measurement. The power of two equal tones, at 2.5 MHz and 3.6 MHz offset from the receiver LO at 2.14 GHz , were swept and the fundamental and third-order intermodulation distortion (IM3) were plotted. An IIP3 of -4.6 dBm was measured. The baseband output spectrum in a triple-beat test is shown in Figure 4.28. Two-tones of 19 dBm each are injected at the TX port of the duplexer, and a single-tone jammer of -43 dBm was injected at the antenna port, at 190 MHz and 2.5 MHz offset from the RX LO respectively. The downconverted cross-modulation distortion is 58.4 dB below the downconverted jammer i.e. triple beat ratio (TBR) equals 58.4 dB.

Table 4.4 summarizes the measured performance of the duplexer cascaded with a direct-conversion receiver. The performance is comparable to off-chip SAW duplexer implementation with the added advantages of integration and tunability.

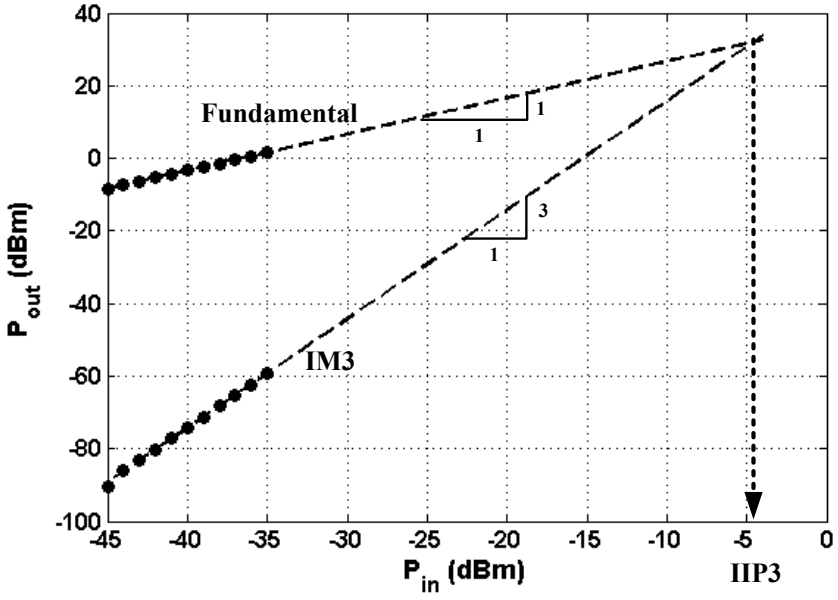

Figure 4.27: Receiver IIP3 measurement.

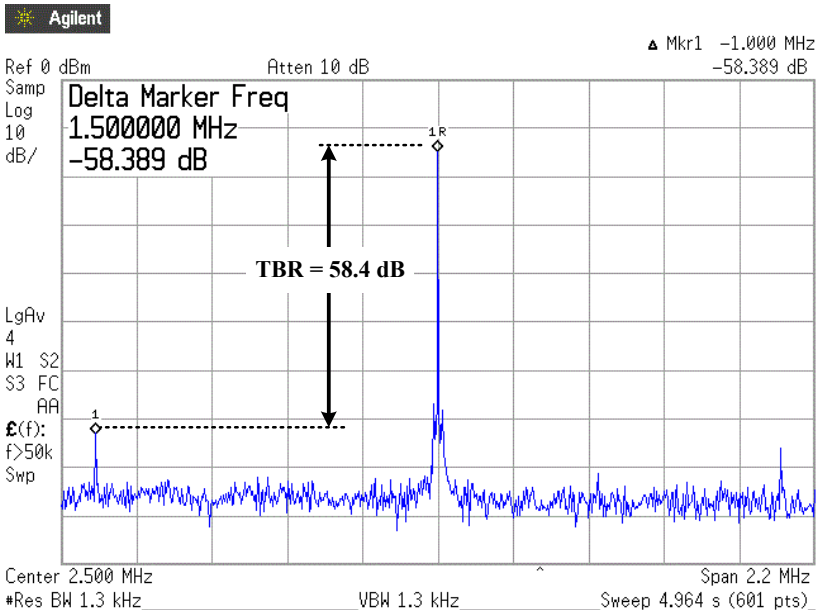

Figure 4.28: Output spectrum in triple-beat test ($P_{TX,total}$ = 22 dBm, P_{jam} = −43 dBm).

This Chapter, in part, has been submitted for publication in IEEE Custom Integrated Circuits Conference, "Hybrid transformer-based tunable integrated duplexer with antenna impedance tracking loop", and an extended paper is being pre-

Table 4.4: Performance summary.

Frequency	1.7–2.2 GHz
Isolation in TX Band	> 50 dB
Isolation in RX Band	> 50 dB
Antenna VSWR Range	2:1
Max. TX Power	27 dBm
TX Insertion Loss	3.7 dB
Cascaded Noise Figure	5.3 dB
Conversion Gain	45 dB
IIP3	-4.6 dBm
TBR	58.4 dB
IIP2	> 60 dBm
I and Q Quadrature Error	0.5 dB, 1.2 degree
Power	28 mA from 1.2V, 7 mA from 2.5V
Area	2.2 mm^2

pared for publication in IEEE Journal of Solid-State Circuits, "A WCDMA/LTE receiver with tunable integrated duplexer and antenna impedance tracking loop". The dissertation author was the primary investigator and author of these paper and it was co-authored by Prof. Lawrence Larson and Dr. Prasad Gudem.

Chapter 5

Conclusion

Hybrid transformer duplexer relying on electrical balance can be integrated in a CMOS process. They provide the tunability required to replace a bank of off-chip frequency selective duplexers, enabling true fully integrated multiband transceivers. The basic properties of a hybrid transformer-based duplexer were analyzed and techniques to improve prior state-of-the-art performance were demonstrated.

An RF-to-DC converter with well controlled input impedance and high efficiency over a wide range of input power has been shown. This converter may be used to replace the passive balance network in a hybrid transformer duplexer. Thus recycling most of the power in that port back to dc instead of being lost as heat. The operation of the class-E rectifier was analyzed and a new technique for controlling its input impedance has been presented. The technique depends on two varactors to compensate for input power and DC load variation. A PCB was designed at 800 MHz with commercial components, achieving a peak efficiency of 60% with S_{11} less than -20 dB over 12 dB input power variation and 2.5 to 4.2 V battery voltage change. This concept can be applied to other energy recycling applications where the rectifier closely emulates a load resistor without most of the power loss included in a real load.

A technique to achieve wideband differential and common-mode isolation in hybrid transformer integrated duplexers was introduced. This technique enables high TX powers and significantly improved cross-modulation performance. The

duplexer utilizes a differential version of a planar hybrid transformer to enable wideband differential to differential and differential to common-mode isolation between the transmitter and receiver. A differential hybrid transformer duplexer that covers 3GPP bands I, II, III, and IX is implemented in 90nm CMOS process. It achieves a differential to differential isolation of 60 dB in the transmit band and 40 dB in the receive band, and a differential to common-mode isolation of 60 dB in both bands. The duplexer with a cascaded LNA achieves a noise figure of 5.6 dB in the receive path and an insertion loss of 3.7 dB in the transmit path.

An integrated duplexer that is tolerant to antenna impedance variations was implemented. By downconverting the TX leakage and feeding back a correction signal to a wide impedance range balance network, high isolation can be maintained despite antenna impedance variations. A novel balance network architecture was also introduced to achieve high isolation at the TX and RX bands concurrently. Implemented in a 65-nm CMOS process, the duplexer achieves an isolation of more than 50 dB in the transmit and receive bands, with an antenna VSWR within 2:1, and between 1.7 and 2.2 GHz. The duplexer, along with a cascaded direct-conversion receiver, achieves a noise figure of 5.3 dB, a conversion gain of 45 dB and consumes 51 mW. The insertion loss in the transmit path was less than 3.8 dB.

This work is the first implementation of a high-power and antenna mismatch tolerant duplexer integrated in a CMOS technology. When adopted in a mutiband transceiver, it will simplify the front-end complexity and reduce the cost considerably by replacing the bank of off-chip duplexers with an integrated tunable duplexer. This duplexer, which can achieve TX-RX isolation at an arbitrary frequency, enables a true fully integrated and reconfigurable multiband transceiver with a performance comparable to current implementations that use off-chip duplexers.

Future work that can be based on this research can include a blocker tolerant receiver architecture to be able to withstand out-of-band blockers that are not filtered by the wideband duplexer presented. Integrating the RF-DC converter in a CMOS process and successful demonstration in conjunction with an integrated du-

plexer is also challenging. Removing the balun at the antenna port would further reduce the insertion loss. Extending the isolation bandwidth using prior knowledge of the antenna impedance characteristics or a variant of the balance network presented can be also important to extend the presented duplexer to wider channel bandwidth cases.

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