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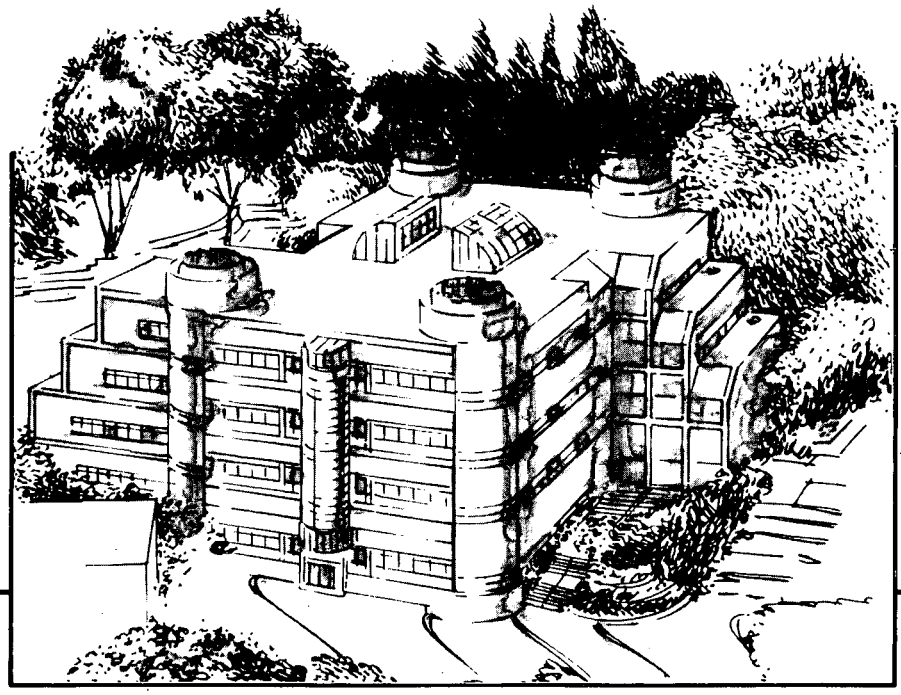

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CHAPTER 9

Structural Defects in Epitaxial III/V Layers

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I. Introduction

The main interest in epitaxial semiconductor layers has been concentrated on the electronic quality of the material such as carrier mobility or photoluminescence (PL)-output. Therefore, the extended structural defects

are often overlooked, even though they can be detrimental, especially in integrated circuit applications.

Near–lattice-matched heteroepitaxy is the fundamental growth process for all optoelectronic semiconductor devices and for the most advanced digital devices on III/V semiconductors. However, lattice-mismatched heteroepitaxy provides increased flexibility for band-gap engineering. Strained-layer quantum wells have been used to control the band gap of the active region of semiconductor lasers, (Fisher *et al.*, 1987; Kolbas *et al.*, 1988), permitting lasing at previously unattainable wavelengths. For this reason, the possibility of growing high-quality lattice-mismatched heteroepitaxial layers has attracted an ever-increasing interest. Over the past few years, there has been considerable research activity in the growth and fabrication of AlInAs high electron-mobility transistors (HEMTs) (Mishra *et al.*, 1988; Aina *et al.*, 1988a), motivated by large conduction band discontinuities at the heterointerfaces of AlInAs and GaInAs (People *et al.*, 1983) or InP (Aina *et al.*, 1988b). The large conduction-band discontinuity ensures the confinement of a high concentration of two-dimensional electrons at the heterojunctions GaInAs on InP or GaAs, which also have high electron mobilities and high saturation velocities. Most of these layers have been grown by molecular beam epitaxy (MBE); however, a wide variety of AlInAs HEMT structures can also be grown by metalorganic vapor phase epitaxy (MOVPE). These developments open up the attractive possibility of integrating electronic devices and optical devices, which can be more effectively grown by MOVPE. Further research is needed on defects due to lattice and thermal mismatch, interface roughness, and interdiffusion between constituents of semiconductor multilayers that can seriously degrade device performance.

In general, III/V substrates are fragile and brittle and mainly available in small wafer sizes. These disadvantages could be avoided by successful epitaxial growth of GaAs and other III/V compounds on Si. For microwave power devices, there is also the possibility of superior heat dissipation because of the higher thermal conductivity of Si compared with GaAs. III/V epitaxy on Si would enable monolithic integration of optoelectronic III/V devices with silicon integrated circuits. This would lead to a whole range of new device structures, taking into account the advantages of III/V optical device capability and silicon microelectronics. However, this system presents numerous difficulties. The large misfit between GaAs and Si ($\sim 4\%$) and the growth of a polar crystal on a nonpolar substrate results in a high density of lattice defects, including inversion boundaries, dislocations, and stacking faults.

High densities of dislocations and planar faults are not satisfactory for device applications. So far, growth of low–dislocation-density (below $10^5/cm^2$) GaAs epitaxial layers on Si has not been reproducibly demon-

strated. A wider application of this system therefore requires a greater understanding of the mechanisms of defect formation. This understanding should lead to a decrease of the defect density, and a decrease in the residual strain, eventually making GaAs/Si fully usable for optoelectronic and digital devices.

GaAs grown on Si can be treated as a model system that has not only a large lattice mismatch, but also a large difference in thermal expansion coefficient, both of which lead to defect formation. Therefore, much in this chapter will concentrate on the GaAs/Si system. However, lattice-matched systems (AlGaAs/GaAs, AlAs/GaAs), and other systems with increasing mismatch (InGaAs/GaAs or InP, InAlAs/GaAs or InP), will be considered.

In this chapter it will be shown not only that defects are a common problem for heteroepitaxial layers, but that some characteristic defects are also present in homoepitaxial GaAs layers grown by MBE at high and low temperatures. Defects formed in heterostructures grown by MOCVD and MOVPE will also be discussed briefly. Some methods that have been used to suppress defect propagation in epitaxial layers will be described.

II. Homoepitaxy

1. Oval Defects

MBE is a very effective technique for the growth of ultrathin layers, and for the control of interface abruptness and doping profiles. It has been demonstrated that GaAs epilayers can be grown by MBE with residual impurities in the low $10^{13}/cm^3$ range (Chand *et al.*, 1989). However, surface defects, so-called oval defects, are formed that degrade electrical and optical properties of the material. They may also cause serious problems in GaAs integrated circuits by limiting yields. The oval defects have been observed in gallium-containing compound semiconductor layers grown by MBE, but not in those layers grown by MOCVD or chemical beam epitaxy (CBE), in which a gaseous source of Ga was used (Tsang, 1985). The nature of these defects has been carefully investigated to clarify their formation mechanism and to reduce their density.

The name "oval defects" comes from their appearance in optical microscopy (Fig. 1). These defects usually are in the range of 1 to 15 μm in size, in layers up to 5 μm thick (Bafleur *et al.* 1982), and their density is in the range from 10^2 to $10^5/cm^2$. Their long axes are elongated in the $\langle 110 \rangle$ direction. Generally, these defects can be divided into two groups: one with a defined

FIG. 1. SEM micrograph of an oval defect formed in MBE-grown GaAs (courtesy of Dr. Calawa, MIT Lincoln Lab.).

core and one without the core. Fujiwara *et al.* (1987) have classified them in up to seven different types. In this classification, the surface oval defects that have macroscopic core are classified as the α type ($\alpha 1-\alpha 6$), while those without cores are classified as the β type. Electron microscopy studies showed that the central parts of α defects have a polycrystalline region surrounded by microtwins (Bafleur *et al.*, 1982). The facets that appear on the surface of the faulted region are probably due to the growth rate variation between various low-index crystallographic planes. An analysis of these defects (Bafleur *et al.*, 1982) by electron microprobe showed no deviation from stoichiometry or impurity accumulation. It has been suggested that these defects start from nucleation sites (Bafleur *et al.*, 1982), which are considered to be located at the substrate/layer interface. At these points the growth was assumed to be perturbed and polycrystalline regions developed. However, this conclusion has not been supported by other investigators.

There are also reports that the oval defects are related to substrate dislocations (Hwang *et al.*, 1983). However, later studies show that defects that are formed near dislocations are a special kind of oval defect having a surfboard shape, and they are not sensitive to growth conditions. They can easily be eliminated (Shinohara *et al.*, 1985).

There has been much effort to correlate the density of oval defects with growth parameters. It was shown that the density of oval defects does not

depend on the As_4/Ga ratio, but increases with an increase in growth rate and Ga cell temperature (Shinohara and Ito, 1989). These researchers suggested that oval defect density decreases with an increase in substrate temperature. However, Metze (Metze *et al.*, 1983) showed just the opposite, that oval defect density was closely correlated with the growth rate but not with substrate temperature. In general, the density of oval defects increases with an increase in epilayer thickness. It was reported that there are strong correlations between the density of oval defects and surface contamination by carbon (Bafleur *et al.*, 1982) and sulfur (Chai *et al.*, 1985).

Most investigators believe that these defects are Ga-related and are caused by Ga-spitting (Wood *et al.*, 1981; Schlom *et al.*, 1989; Chand, 1990) or gallium oxides: Ga_2O (Shinohara and Ito, 1989; Akimoto *et al.*, 1985; Weng, 1986) or Ga_2O_3 (Wood *et al.*, 1981; Weng, 1986). It was observed that heating the gallium source to well above its growth temperature in an attempt to outgas oxide just before the growth usually increases the density of Ga-related oval defects (Schlom *et al.*, 1989). This outgassing can cause a large number of Ga droplets near the opening of a Ga crucible, resulting in an increase of Ga-spitting.

A thermodynamic analysis of the formation mechanism of oval defects due to growth conditions and Ga oxide was first reported by Ito *et al.* (1984). It was shown that Ga_2O formed in the Ga cell or on the substrate causes oval defect formation (Shinohara and Ito, 1989). The reactions forming Ga_2O vary with Ga cell temperatures. In the temperature range below 930°C, these reactions are mostly between Ga and Ga_2O_3; above this temperature, most reactions are between carbon and Ga_2O_3. The relation of oval defects to carbon presence has been suggested earlier (Bafleur *et al.*, 1982). These authors postulated that carbon contamination can occur either during the substrate preparation or during epitaxial growth.

Smaller oval defects (β type) do not have extended polycrystalline regions at their centers but contain dislocations and stacking faults. It is generally accepted that β-type defects are due to particulates (Weng *et al.*, 1985; Nishikawa *et al.*, 1986; Matteson and Shih, 1986) landing on the substrate during substrate preparation, loading, transferring, or growth. Since these external factors, clean-room conditions, and wafer-transfer mechanisms can be improved, these defects can be avoided. However, α-type defects still appear to be a real problem for MBE layers of GaAs for integrated circuits.

2. GaAs GROWN BY MBE AT LOW TEMPERATURE

GaAs integrated circuits are typically fabricated on semi-insulating substrates. Frequently, heavy ion implantation between devices is used to create

additional defects in order to isolate the devices from each other. However, parasitic coupling through the substrate can still result in cross-talk between neighboring devices called sidegating. Recently, a solution to this problem was found by growing GaAs buffer layers at temperatures as low as 200°C (LT-GaAs). These layers were grown by molecular beam epitaxy (MBE) using typical Ga and As fluxes for arsenic-dominant growth condition at a rate of 1 μm/h (Smith *et al.*, 1988, 1989). Such layers exhibit high resistivity, which is sustained even after annealing at 600°C. All backgating effects can be removed, and effective device isolation can be achieved.

These layers can be applied as passivation layers as well. In addition, fast photodetectors can be built based on these layers, since the minority lifetime in this material is extremely short (in the range of a few hundred femtoseconds).

Earlier studies by electron paramagnetic resonance (Kaminska *et al.*, 1989a, 1989b) reveal $10^{20}/cm^3$ As_{Ga} antisite defects in as-grown layers, a defect level that decreases at least two orders of magnitude after annealing. These layers are grown from As supersaturation and show up to 1.5% excess As, which leads to $\sim$0.1% of expansion of the lattice parameter. This expansion of the lattice parameter disappears after annealing.

It was noticed earlier that the crystalline perfection of the layers is very sensitive to growth parameters (Liliental-Weber, 1990), such as growth temperature and As/Ga ratio used for the growth, often called the As/Ga beam equivalent pressure (BEP). Generally, samples grown at 200°C or higher on In-bonded molybdenum blocks with a BEP of 10 and a growth rate of 1 μm/h show high crystalline perfection up to a 3 μm layer thickness (Fig. 2). With increasing sample thickness, specific defects called "pyramidal

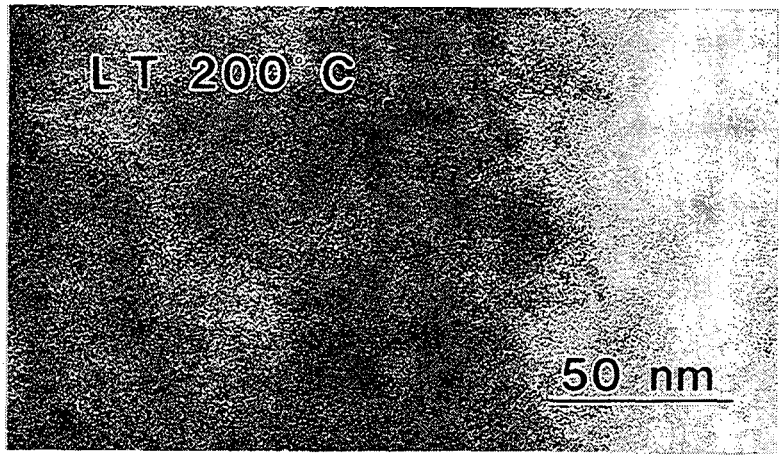

FIG. 2. Plan-view TEM micrograph of as-grown high-perfection monocrystalline LT-GaAs layer showing featureless surface.

defects," start to appear (Fig. 3). These pyramidal defects were described (Liliental-Weber, 1990; Liliental-Weber *et al.*, 1991a) as defects having a well-established polycrystalline core from which other defects, such as secondary microtwins, stacking faults, or dislocations, were formed. The thickness of the perfect material that can be grown before pyramidal defects start to appear decreased drastically with decreasing growth temperature. An increase of As concentration is observed in these layers. The dependence of the lattice parameter change on excess As is shown in Fig. 4.

The structural defects of pyramidal shape with a polycrystalline core surrounded by microtwins, stacking faults, and dislocations in the LT-GaAs layers grown at 200°C bear some resemblance to the so-called oval defects described in the previous section. Their description in the TEM study of Bafleur *et al.* (1982) is especially similar to the defects observed here. However, the density of oval defects in the best MBE layers, about 10^2 defects/cm^2, is many orders of magnitude smaller than the 3×10^8/cm^2 found in LT-GaAs. Impurities such as C, H, or O, in involved in the formation of Ga_2O_3, or Ga_2O were suggested as the source of oval defects (Shinohara and Ito, 1989; Akimoto *et al.*, 1985; Weng, 1986, Ito *et al.*, 1984). However, in LT-

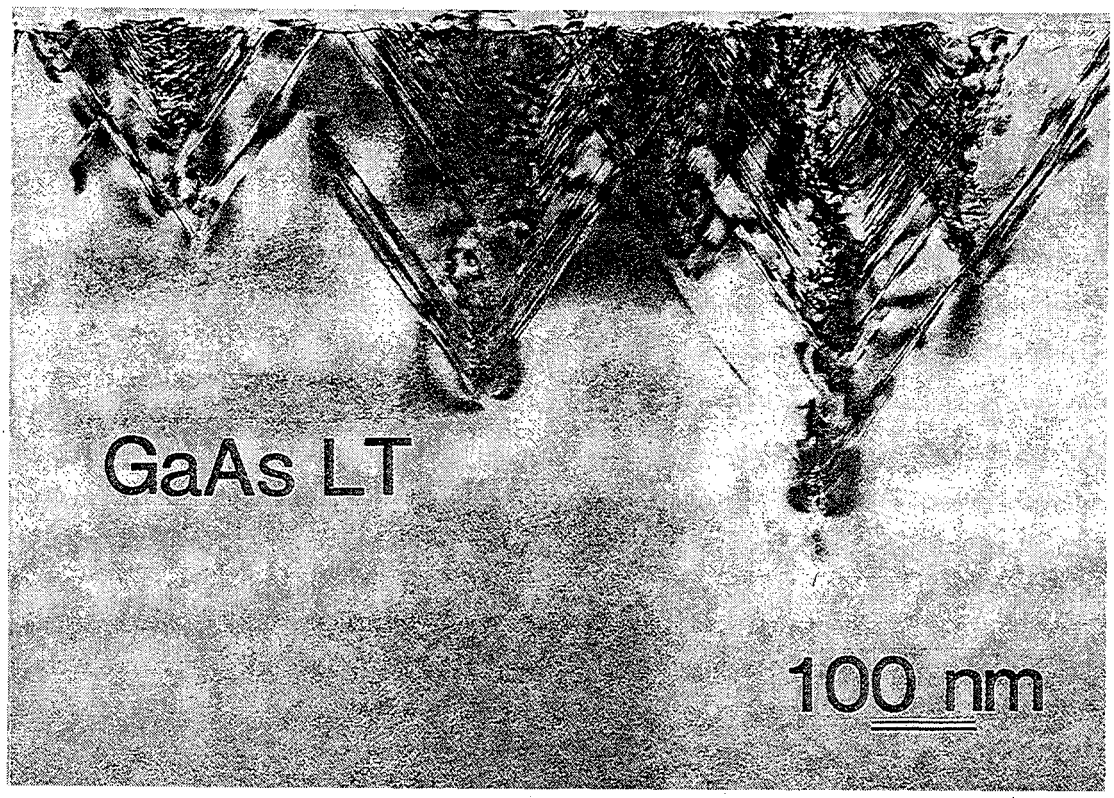

FIG. 3. Cross-sectional TEM image of pyramidal defects formed near the surface in the LT-GaAs layer grown at 190°C.

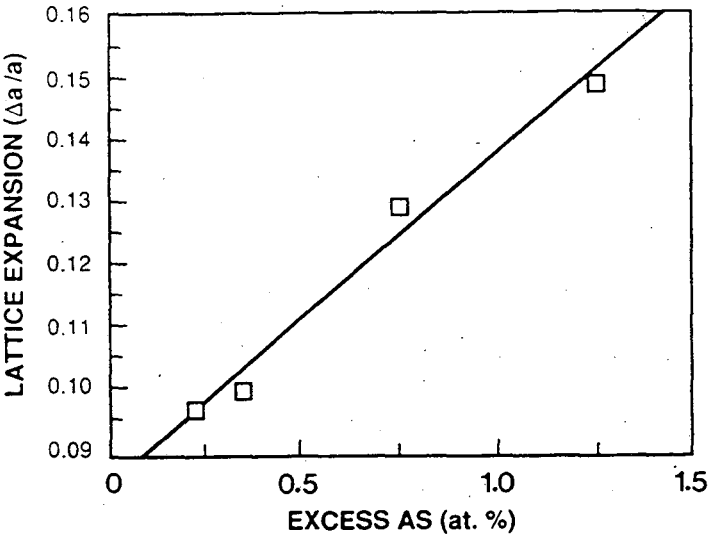

FIG. 4. Dependence of lattice parameter expansion of LT-GaAs epilayers grown at 210, 200, 190, and 180°C on excess As content in the layer.

GaAs such impurities could hardly explain the observed high densities of such defects that appear only after growth of a certain layer thickness.

The crystal quality of LT-GaAs layers grown at 180–210°C is very sensitive to small changes in the growth temperature. For example, a 5°C change within this range makes a noticeable difference in crystal quality: An increased density of pyramidal defects accompanies a decrease in the growth temperature (Fig. 5). It is possible that these defects and oval defects are formed by the same mechanism. The extremely high density may just be a consequence of the lower growth temperature.

If the LT layer is grown with a beam equivalent pressure (BEP) greater than 10 (Liliental-Weber *et al.*, 1991b; Claverie *et al.*, 1991), a higher growth temperature is required to obtain the same thickness of monocrystalline layer. For a 1-μm layer thickness, the dependence on growth temperature for a BEP of 20 is shown in Fig. 6. Figure 7 shows the decrease in monocrystalline layer thickness with increasing BEP. Generally, the layer grown with the higher BEP can be divided into three sublayers: a monocrystalline sublayer, a layer with dislocations and stacking faults that may be the origin of pyramidal defects, and a polycrystalline layer. At a particular monocrystalline layer thickness, related to both the growth temperature and the BEP ratio, dislocations and stacking faults begin to form. With an increase in layer thickness, microtwins are formed. In these areas void formation was also observed. If a cap layer is grown on top of such a layer, microtwins propagate through the cap layer, and the surface of the cap layer is usually undulated (Fig. 8).

There may be more than a single reason for the breakdown of crystallinity

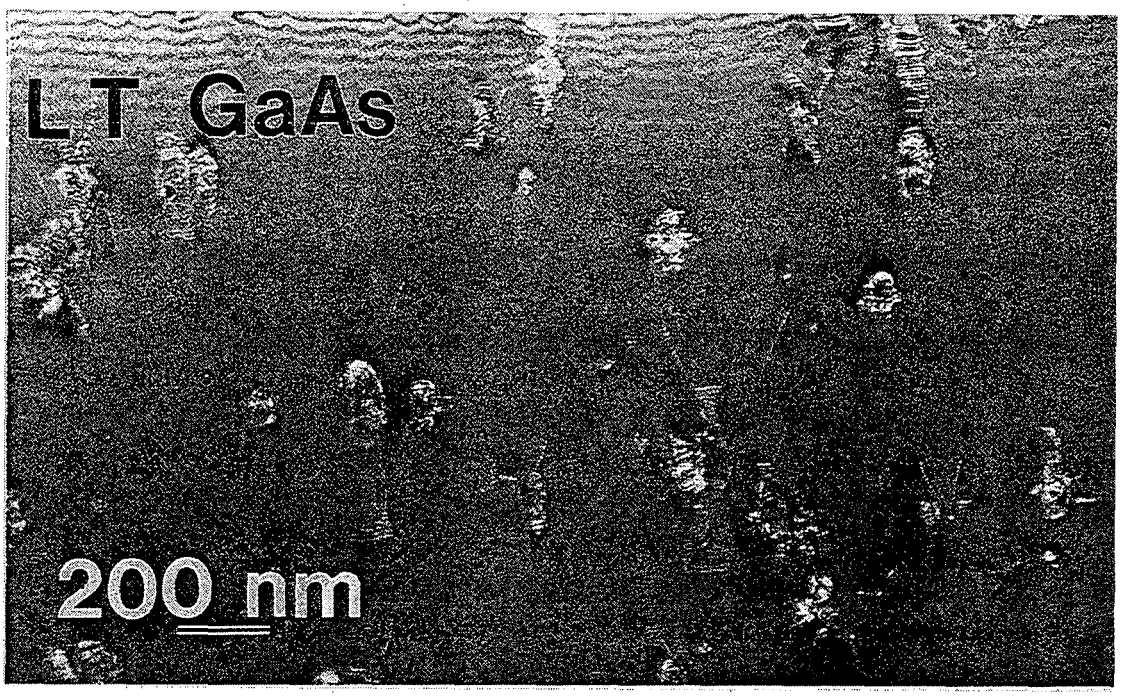

FIG. 5. Plan-view micrograph showing distribution of pyramidal defects on the surface of a 2-μm thick layer grown at 190°C.

of these layers. One factor may be strain build-up in the layer due to excess As causing expansion of the lattice parameter. Only a specific layer thickness, the "critical layer thickness" (h_c), may be possible at a given growth condition before misfit dislocation formation occurs at the surface. The dislocation loops may be pinned by segregation of excess As to the dislocation cores and eventually become nucleation sites for polycrystalline growth. Evidence for this mechanism includes dislocations and stacking faults found near the top

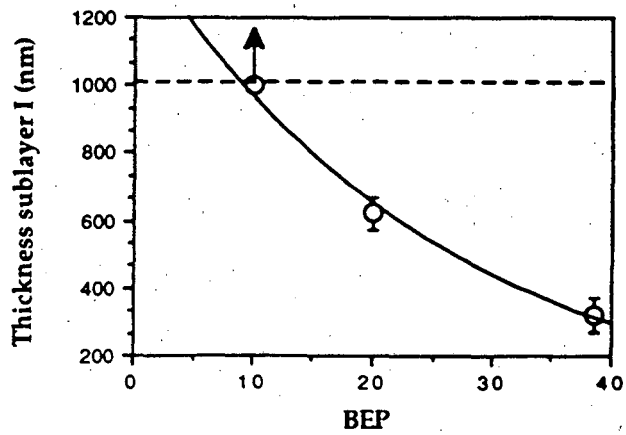

FIG. 6. Thickness of the defect-free layer as a function of BEP for a growth temperature of 200°C.

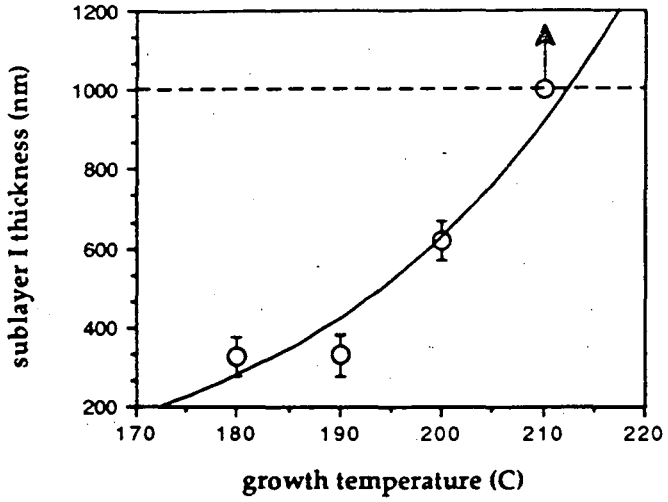

FIG. 7. Thickness of the defect-free layer as a function of growth temperature for a constant BEP of 20.

of the crystalline layer (at the origin of pyramidal cores). The LT-GaAs epilayer thickness at which the onset of pyramidal defects occurs lies between the theoretical critical layer thicknesses (h_c) for pseudomorphic growth predicted by People and Bean (1986) and by Matthews and Blakeslee (1974). Thus, it is possible that the elastic strain incorporated in the LT-GaAs layers as a result of the excess As is responsible for the defects formed in the layer. The presence of this strain in as-grown layers has been confirmed by large-angle and classical convergent-beam studies (Liliental-Weber *et al.*, 1991c; Liliental-Weber, 1992).

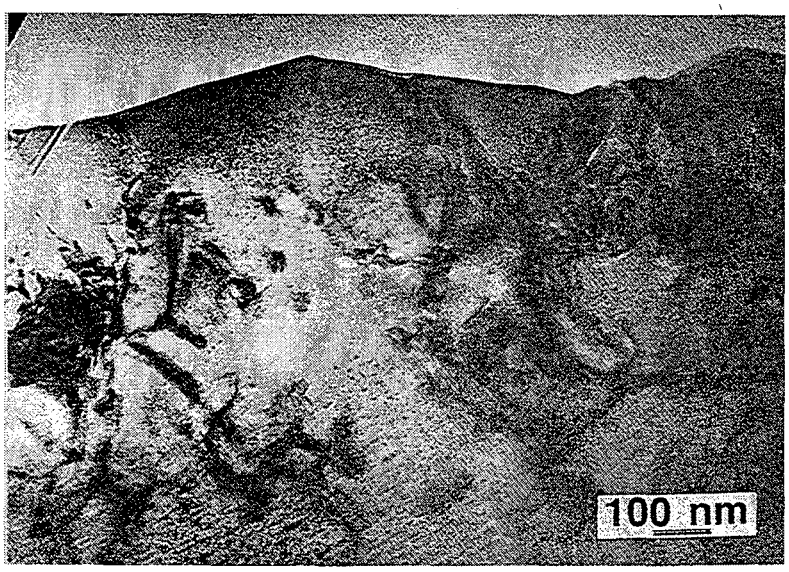

FIG. 8. Surface undulation of the LT-GaAs layer grown at high BEP.

It was shown that obtaining high-quality LT-GaAs layers grown at temperatures down to 200°C is possible, and a high concentration of point defects in such layers ensures high resistivity combined with low carrier mobility. These layers might as well be applied as strained layers, as was shown for GaAs grown on Si. Annealing of the layers at 600°C (the temperature used normally for MBE growth of GaAs) leads to formation of As precipitates, which removes a large part of the excess As from the GaAs unit cells, leading to the decrease in the lattice parameter (Liliental-Weber, 1990; Melloch *et al.*, 1990; Liliental-Weber *et al.*, 1991d, 1991e; Claverie and Liliental-Weber, 1992).

III. Heteroepitaxy

3. Origin of Defects

Failure to achieve high-quality material for devices is attributed to several problems that occur in heteroepitaxy, including differences in lattice constants and thermal expansion coefficients between the substrate and epilayers, and problems related to growth parameters and surface preparation before layer growth. Any line and area defects present in the substrate usually extend into the epilayer during growth. The resulting density of these defects in the layer is at least equal to that of the substrate. Therefore, the epilayer cannot be structurally more perfect than the substrate. A second class of defects is related to the cleanness of the substrate surface. If oxides and hydrocarbides are not completely removed from surfaces, some defects (similar to those described for homoepitaxy) will be formed. Even for a perfectly clean substrate, surface topography such as surface steps can induce defects. Thirdly, stacking mistakes during crystal growth can cause stacking fault formation. Build-up of impurities at the growth surface can cause inclusions, or even polycrystalline growth can take place. Cooling from the growth temperature to room temperature can lead to clustering of point defects and formation of dislocation loops. When the difference in thermal expansion coefficient between the substrate and the epilayer is large, more complex arrays of dislocations can be formed, because of plastic deformation during cooling. Plastic deformation also takes place during growth above critical thickness. In this case, misfit dislocations can be formed that also extend through the layer at the ends of the half-loops. In the following sections, the causes of defect formation will be discussed in more detail.

a. Lattice Mismatch (Critical Layer Thickness)

In heteroepitaxial growth, the overlayer has a unique orientation relationship with the substrate. In general, epitaxial growth occurs whenever an overlayer and a substrate can have an interface with a highly coincident atomic arrangement. Such an interface has a lower interfacial free energy than other possible orientation relationships. In semiconductor heteroepitaxy, the overlayer and the substrate usually have the same orientation and structure. However, lattice constants of the layers are usually different from those of the substrates. This lattice mismatch is initially accommodated entirely by elastic strain, but becomes partially relaxed by introduction of misfit dislocations into the interface above a critical thickness. In a perfectly coherent lattice-mismatched epitaxial system, the epilayer is strained to assume the lattice constants of the substrate, so that the epilayer strain equals the misfit strain (ε_{mis}), defined by

$$\varepsilon_{mis} = (a_e - a_s)/a_s \tag{1}$$

in terms of the equilibrium lattice constant of the thin film a_e and the substrate lattice constant a_s.

For cubic crystals, this strain leads to a tetragonal distortion of the unit cell in the epilayer, resulting in a difference of the lattice spacing parallel to the interface plane $a_\parallel$ from the spacing perpendicular to it $a_\perp$ ($=a_s$ for these thin layers), depending on the Poisson ratio v:

$$a_\parallel = a_e(1 + \varepsilon v). \tag{2}$$

The strain energy stored in the epilayer increases linearly with the thickness of the epilayer. Above a critical epilayer thickness, it becomes energetically favorable for the epilayer to assume its equilibrium lattice constant and to accommodate the misfit strain by introduction of misfit dislocations at the heterointerface. Above this "critical thickness" the commensurate (or coherent) layer will only be metastable with respect to a relaxation by forming misfit dislocations. However, nucleation and motion of dislocations into the interface to form a regular grid of misfit dislocations is a difficult process. In general, the misfit is accomodated partially by an elastic strain even though the critical thickness is far exceeded. The ideal equilibrium distance between misfit dislocations is given by

$$d = |\mathbf{b}|/\varepsilon_{mis} = |\mathbf{b}|/[a_e - a_s)/a_s]. \tag{3}$$

Here, $\mathbf{b}$ is the Burgers vector of misfit dislocations and ε_{mis} is the misfit strain. If the misfit dislocation density does not correspond to the lattice mismatch

or if dislocations are nonuniformly distributed, residual strain will still be present in the epilayer.

Much experimental and theoretical work has been done to understand the mechanisms by which misfit dislocations are generated, and how these mechanisms relate to the density of dislocations that thread through the epilayer (People and Bean, 1985, 1986; Matthews and Blakeslee, 1974, 1975, 1976; Frank and van der Merve, 1949; Matthews, 1975a, 1975b; van der Merve, 1972; van der Merve and Ball, 1975; Dodson and Tsao, 1987; Hull and Fischer-Colbrie, 1987; Hull *et al.*, 1988; Bean *et al.*, 1984; Maree *et al.*, 1987). The most obvious mechanism is that dislocations present in the substrate can glide to or within the epilayer so as to be extended along the interface. However, taking into account the extremely low defect density in many substrates, particularly Si, and the very high density of dislocations observed in semiconductor layers grown on these substrates, this mechanism often makes a negligible contribution.

Different dislocation introduction mechanisms have been found to operate for low and high misfit systems. Frank and Van der Merve (1949) calculated the theoretical critical layer thickness based on the energy of interfacial dislocations. Matthews (1975a, 1975b) considered the line tension of the misfit dislocation to obtain the critical layer thickness at which dislocations would extend along the interface. Matthews and Blakeslee (1974, 1975, 1976) calculated a critical thickness based on a specific mechanism in which misfit dislocations are formed by bending pre-existing threading dislocations in the epilayer. They calculated the critical thickness from the energy balance of the epilayer without and with misfit dislocations. Their predictions of critical thickness agree well with experimental results for metals, but there are discrepancies between predictions and experiments for diamond or sphalerite structure semiconductors. Experiments show that in semiconductors, a thicker layer can usually be grown before misfit dislocations appear than is predicted by theory. Hull *et al.* (1988) found that, for GaAs on Si, the GaAs islands can grow as thick as 6 nm, compared to 1.5 nm predicted by the Matthews theory (Matthews, 1975a, 1975b; Matthews and Blakeslee, 1975, 1976). In an attempt to explain the discrepancy, People and Bean (1985, 1986) developed an empirical model for the critical layer thickness that considered the nucleation of dislocations. Bean *et al.* (1984) pointed out that the activation barrier for dislocation nucleation must play a crucial role in determining a critical layer thickness. They calculated the critical layer thickness for a dislocation to be nucleated to be the point where the strain energy of the layer exceeds the areal energy density of elastic strain associated with a single screw dislocation averaged over an effective dislocation width, which was a free parameter in their fit. Their model did not take into account release of the lattice strain and dissociation into partial dislocations. Dodson

and Tsao (1987) emphasized that the kinetics of the misfit dislocation formation must be dominated by the two activation energies for dislocation motion and dislocation nucleation. They successfully modeled the critical layer thickness, but used a phenomenological fit to describe an arbitrary dislocation multiplication process. Hull and Fischer-Colbrie (1987) measured dislocation densities and velocities and their temperature dependance and used these data in order to determine energy for dislocation nucleation, but did not introduce a specific mechanism of dislocation formation.

Later, it was speculated that the discrepancies between metals and semiconductors should be attributed to the kinematical barriers to the generation and motion of misfit dislocations in semiconductors. Maree *et al.* (1987) suggested that there are at least two obstacles in semiconductors blocking the generation of misfit dislocations. The first obstacle is the large Peierls–Nabarro friction stress, which strongly reduces the mobility of dislocations, and through that, the length of misfit segment that can be formed along the interface. In metals, this friction stress is negligible. The second obstacle is the greater perfection of semiconductors compared to metals; therefore, new dislocations need to be generated during growth instead of just arising from the glide of pre-existing dislocations. Because of these factors, the residual elastic strain remains larger for semiconductors than for metals. If finally we take into account frictional forces and nucleation barriers, the same theoretical approach is applicable to both metals and semiconductors (Fox and Jesser, 1990a).

The frictional stress can also explain asymmetry of dislocation distribution in zincblende semiconductors in the two $\langle 110 \rangle$ directions. Since in the zincblende structure two types of dislocations are formed (α and β) having different frictional stress for each type, a different metastable critical layer thickness can be determined for each type of dislocation. It was shown that frictional stress is also very sensitive to the dopant present in the semiconductor. Therefore, two values of critical layer thickness for two types of dislocations are expected as a result of the doping. Indeed, this phenomenon was demonstrated for GaAsP layers grown on GaAs, for which the difference in critical thickness of the two types of dislocation decreased when GaAsP was heavily doped *p*-type (Fox and Jesser, 1990b).

Maree *et al.*, (1987) showed that the misfit dislocations in semiconductor interfaces are usually 60° dislocations whose dissociation into two partials can also lead to a difference in strain relaxation for tensile and compressive stressed films. They concluded that half-loops are nucleated at the surface and that they glide on $\{111\}$ planes inclined to the interface. Matthews (1975a) worked on the dislocation half-loop nucleation and propagation in strained epilayers and suggested that a half-loop in a perfect semiconductor

will have a critical radius whose activation energy for formation will increase at low misfit. He showed that a minimum misfit can exist below which it is not thermodynamically favorable to nucleate dislocations at any thickness in a perfect epilayer. For misfits lower than 2%, the nucleation barrier cannot be overcome and dislocation will be not formed at any thickness. This would suggest that, at low misfit, any layer thickness can be grown (Matthews *et al.*, 1976). Hull and Fischer-Colbrie (1987) showed empirically, however, that the defect nucleation barrier is as low as 0.7 eV, in contradiction to Hirth's prediction of 6.2 eV at 550°C. Kvam *et al.*, (1987) observed that in GeSi with about 0.8% misfit levels, long (10–100 μm in length) 60° dislocations were formed in the interface for layer thicknesses above 200 nm, in contrast to short (0.1–1 μm) edge misfit dislocations observed for the same material with higher misfit. These 60° dislocations were often grouped into bunches. Similar groupings of dislocations were observed by Hagen and Strunk (1978). They proposed a special multiplication mechanism, pointing out that two orthogonal misfit dislocations with the same Burgers vector of the $\langle 110 \rangle$ type intersect and react, one of the resulting right-angle nodes being repelled from the original point of intersection to the surface by image forces and back stresses, until the right-angle corner has been bent up to the surface. Upon reaching the surface, the dislocation splits into two segments, each glissile. The net result is three dislocations from the original two (Fig. 9). This process was reported in Ge/GaAs heterostructures (Hagen and Strunk, 1978) and by Rajan and Denhoff in GeSi/Si strained epilayers (1987). However, similar

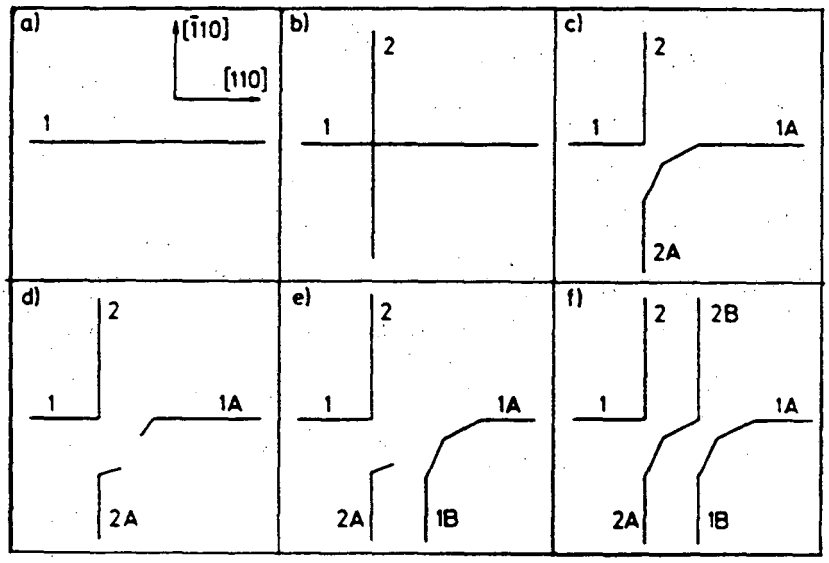

FIG. 9. Schematic drawing of the dislocation multiplication mechanism, after W. Hagen and H. Strunk, *Appl. Phys.* **17**, 85 (1978).

observations by Eaglesham *et al.*, (1989) produced a completely different interpretation, suggesting that the mechanism proposed by Hagen and Strunk is not necessary, but could be considered under specific geometric conditions. Eaglesham *et al.*, (1989), using TEM for identification of dislocations in their early stage of nucleation, identified a heterogeneous mechanism that exists in epilayers (GeSi/Si) at misfit levels below 1%. They identified a new type of dislocation source, a diamond defect (Fig. 10), which can arise either from pre-existing defects in the substrate, or from growth-induced defects in the epilayer. This diamond defect is a faulted loop with a bounding dislocation of $1/6\langle 114\rangle$. This bounding dislocation can dissociate into a variety of $1/6\langle 211\rangle$ and $1/2\langle 110\rangle$ pairs. The $1/2\langle 110\rangle$ dislocation is a glissile lattice dislocation upon which the misfit stress could operate. Gliding of this dislocation produces a glissile loop, and the bounding dislocation returns to the original configuration. When this glissile loop reaches the surface, it behaves in the same way as the half-loop described earlier, leaving a new 60° dislocation at the heterointerface. This process operates similarly to a Frank–Read source and can be repeated several times. This mechanism seems to be responsible for the microstructure in low-misfit epilayers.

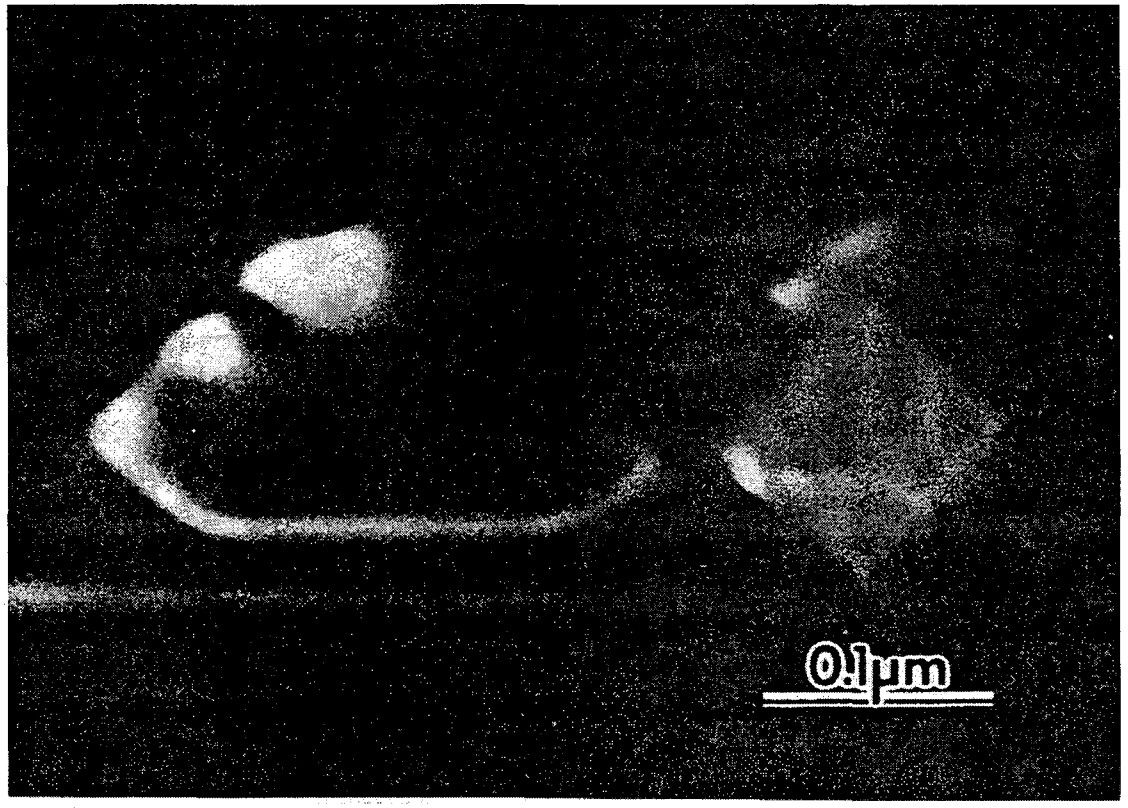

FIG. 10. The diamond defect in a GeSi layer as a source of dislocation multiplication, after D. J. Eaglesham *et al.*, *Phil. Mag. A* **59**, 1059 (1989).

A similar mechanism of strain relaxation from a source center in four slip-trace directions, resulting in a radial stress-relieved region, was proposed by Tuppen *et al.*, (1990). A modified cross-slip mechanism which leads to misfit dislocations in the direction orthogonal to the initial slip direction was proposed by Washburn and Kvam (1990). It was shown that this mechanism has eight crystallographic variants in (001) epitaxy. These models, described by Eaglesham *et al.*, (1989), Tuppen *et al.*, (1990), and Washburn and Kvam (1990), explain the configurations of dislocations observed in the epilayers for low misfits.

b. Nucleation Modes

The preceding models for misfit-dislocation formation and critical-layer thickness were assumed based on layer-by-layer growth. This is not always the case. In general, epitaxial layers show three different growth modes in the early stage of nucleation: (a) the Frank–van der Merwe mode (layer-by-layer growth); (b) the Volmer–Weber mode (cluster or three-dimensional growth); and (c) the Stranski–Krastanow mode, where one or more layers can be grown layer-by-layer followed by clustered growth. Classically, these modes were rationalized in terms of force balance between surface tensions (Bauer, 1958). Let us define a quantity $G = \gamma_{sv} - \gamma_{so} - \gamma_{ov}$, where $\gamma_{sv}, \gamma_{so}, \gamma_{ov}$ denotes the specific surface free energy of the substrate–vacuum, the substrate–overlayer, and the overlayer–vacuum interfaces, respectively. When $G < 0$, the Volmer–Weber mode is favored. When $G > 0$, the other modes are favored. It was shown that an interaction between the epilayer and the substrate and misfit strain also have an influence on the growth mode (van Delft *et al.*, 1985; Grabow and Gilmer, 1986). Grabow and Gilmer (1986) have investigated the conditions that favor three-dimensional clustering of the epilayer by molecular dynamics computer simulations in terms of the following factors:

E_{ee} = the bond energy between two atoms in the epitaxial layer,
E_{es} = the epilayer-substrate bond energy,
ε_{misf} = the misfit strain.

Layer-by-layer growth is favored when $E_{ee} < E_{es}$ and $\varepsilon_{misf} \sim 0$. Three-dimensional growth is favored when $E_{ee} > E_{es}$ and ε_{misf} is not equal to 0. The Stranski–Krastanow growth mode is favored when $E_{ee} > E_{es}$ and ε_{misf} is small.

The preceding theoretical considerations were based on the assumption that the system is under conditions in which the nucleus can retain its equilibrium shape. However, real crystal growth generally occurs far from

thermodynamic equilibrium. Therefore, epitaxial growth is very sensitive to adatom diffusion and local chemistry. In epitaxial growth, the surface diffusion depends on the substrate temperature and on the deposition rate. Low temperature may enhance layer-by-layer growth by reducing the surface diffusion length. This effect has been observed in the growth of Ge_xSi_{1-x} on Si substrates. Bean *et al.*, (1984) reported that the tendency for three-dimensional growth is reduced by reducing the substrate temperature.

The effect of growth temperature on the density of GaAs nuclei grown on Si was studied by Biegelsen *et al.*, (1987). They showed that the nucleus density is a function of temperature. The density of islands increases when the substrate temperature decreases. The kinetic effect of short diffusion length favors the high density of small nuclei that, according to Biegelsen *et al.*, produce the smoother surface of thick epilayers. These authors show that the size and separation between islands increases with an increase in substrate temperature, and in this case the thick epilayer surface becomes rough.

In general, two-dimensional growth is not easy to obtain, because many factors can disturb this growth mode; therefore, there are not many semiconductor systems where true two-dimensional growth has been confirmed experimentally. One example of such a system is AlGaAs grown on GaAs, in which lattice mismatch is small. However, even in this system monoatomic interface abruptness has never been observed (Ourmazd, 1989; Long *et al.*, 1991). The performance of an AlGaAs/GaAs heterostructure devices depends on the structural, electronic, optical, and morphological properties of AlGaAs. These properties of AlGaAs affect the subsequent AlGaAs/GaAs interface quality and the properties of overgrown GaAs. Because of the small surface migration of Al and enhanced surface segregation of impurities in AlGaAs, the inverted interface (GaAs on AlGaAs) was observed to be rougher (Fig. 11) than the starting interface (AlGaAs grown on GaAs) (Petroff *et al.*, 1984). Interface roughness increases the scattering of carriers and increases the threshold current of lasers. It was observed that the wavy nature of AlGaAs/GaAs interfaces is due to impurities in the Al source (Chand and Chu, 1990). Impurities with smaller solubility in AlGaAs than in GaAs segregate on the surface of AlGaAs during growth and are trapped in the overgrown GaAs layer. Some of these impurities may affect the surface reconstruction and prevent the lateral propagation of the atomic layer by pinning steps on the surface, resulting in a rough interface (Petroff *et al.*, 1984). The effect of impurities, especially oxygen contamination, on AlInAs properties is even more subtle than in the case of AlGaAs. Elimination of all sources of oxygen and moisture contamination is therefore important for growing high-quality AlInAs (Aina *et al.*, 1991).

In general, three-dimensional nucleation can be caused by many factors. One of them is strain energy due to lattice mismatch. This was demonstrated

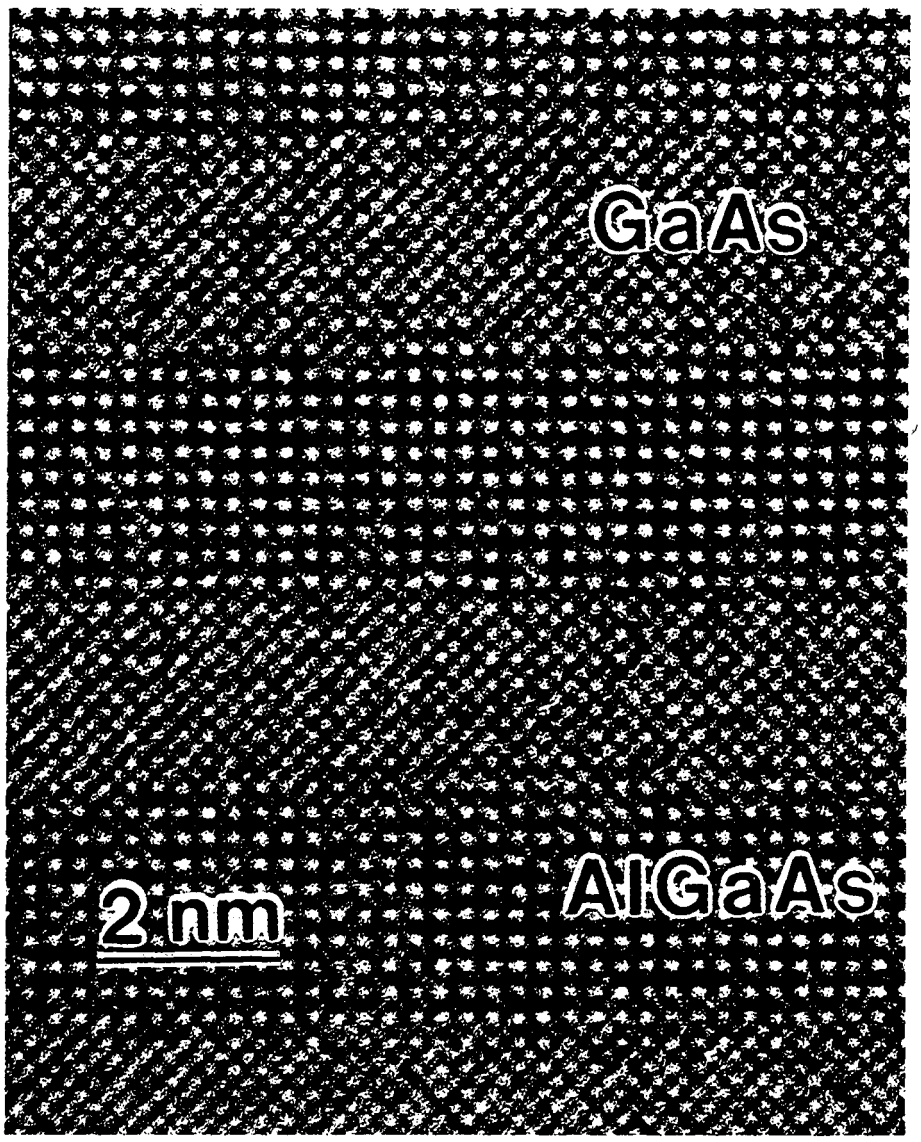

FIG. 11. High-resolution TEM micrograph of AlGaAs/GaAs quantum wells. Note different interface abruptness on inverted interface.

experimentally by George *et al.*, (1990). For In-rich compounds, a larger In content leads to three-dimensional growth. This growth mode was observed for InGaAs grown on GaAs at 640°C. The island size varied between 5 and 30 nm. Similar growth was observed for AlInAs grown on GaAs by MBE. In the growth of quantum wells of AlInAs/GaInAs by MOCVD, it was observed that GaInAs grown on top of AlInAs has a more abrupt interface (width of 1–2 monolayers) than AlInAs grown on top of GaInAs (having a width of 3–4 monolayers). The roughness increased with an increase in layer thickness (Bimberg *et al.*, 1989). When MBE was used at 575°C, two-dimensional growth was observed (Stolz *et al.*, 1987). In these materials, As and In

desorption from the surface is often observed creating column III vacancies and hence significant group III diffusion (Deppe and Holonyak, 1988). In addition to island formation, compositional variations occur in the ternaries (InAlAs) grown on InP (or GaAs) caused by surface migration effects, resulting in lateral inhomogenous strain and dislocation formation.

A good example of three-dimensional growth is GaAs grown on Si ($\sim 4\%$ mismatch). Hull et al., (1988) observed that for GaAs on a Si substrate, the initial nucleation occurs in the three-dimensional mode and that the GaAs nucleates with a high contact angle island on the Si substrate. They reported that the GaAs islands in general appear to be associated with steps on the Si surface. These islands are strained coherently to the substrate lattice even after exceeding the critical thickness.

Theoretical calculations by Northrup (Northrup *et al.*, 1987) predict that, for GaAs grown on Si under As-rich conditions, the equilibrium structure should consist of GaAs islands surrounded by a (100) Si surface that is 2×1 As-terminated, and under Ga-rich conditions, GaAs islands surrounded by a surface terminated by Ga–As dimers.

The model supported by total-energy calculation, by Kaxiras *et al.*, (1989), provides a description of GaAs growth on Si surface steps. The authors emphasize the role of double-layer steps on the Si surface in initiating layered epitaxial growth. They concluded that growth of zincblende GaAs stoichiometric structure on flat regions of Si (100) is suppressed and a mixed layer can be grown. Step topology prevents mixing in the immediate neighborhood of the steps and promotes three-dimensional growth. The exposed plane at the step is no longer the (100) plane of GaAs, but rather the (211) plane, which is a nonpolar plane. Further growth continues as three-dimensional growth in the direction oblique to the surface, in agreement with experimental observations. When these layers coalesce, thick layers of GaAs are obtained.

Another example of three-dimensional growth for a system with large mismatch (8% misfit) is the growth of GaSb on a GaAs substrate. For thicknesses up to 30 nm, the GaSb layer is not continuous. The islands are elongated, with facets on (111) planes. This elongated shape was related to an anisotropy of the growth rates of the island facets (Raisin *et al.*, 1991). Island height was related to growth conditions. Increasing the deposited GaSb layer thickness resulted in an increase in the lateral island size, which led to coalescence of the neighboring islands. Three-dimensional growth was also observed for InSb grown on GaAs (Zang *et al.*, 1990).

c. *Difference in Thermal Expansion Coefficient*

A difference in thermal expansion coefficients is also a potential cause of defects in the epilayer. In GaAs-on-Si heteroepitaxy, there exists a 4.1%

lattice mismatch. This misfit strain can be relieved by forming misfit dislocations, and the GaAs epilayer can recover its equilibrium lattice constant. However, when the sample is cooled to room temperature after growth, a high residual stress is again developed in the GaAs because of the difference in thermal expansion coefficient between GaAs and Si: $\alpha(\text{GaAs}) = 5.93 \times 10^{-6}/°\text{C}$, $\alpha(\text{Si}) = 2.6 \times 10^{-6}/°\text{C}$ (Touloukian *et al.*, 1977). This 2.5 times difference in thermal expansion coefficient results in a new misfit strain when the wafer is cooled to room temperature of about 2×10^9 dynes/cm.[2] The associated high residual stress modifies the band structures of GaAs, resulting in reduction of the band gap and a break in the degeneracy of valence bands. Photoluminescence studies (Bugajski *et al.*, 1988) have shown that a tensile strain is present in GaAs grown on Si, rather than the compressive strain expected from the lattice mismatch between GaAs (5.653 Å) and Si (5.431 Å). In our own study (Liliental-Weber *et al.*, 1988a), we found that the number of misfit dislocations is higher at room temperature than expected from the equilibrium lattice constants of GaAs on Si. The tensile strain observed experimentally is lower than the expected value of 2.4×10^{-3}, implying that this strain may also have been partially relieved by plastic deformation. Cooling from 600°C to only 400°C is sufficient to generate a biaxial tensile stress far above the experimentally determined critical resolved shear stress of 15 MPa at 400°C (Bourret *et al.*, 1987), which will result in the glide of additional dislocations of various types from the interface into the epilayer.

Recently it was experimentally observed by HCl vapor-phase etching of GaAs/Si and GaP/Si at growth temperature that the threading dislocation density in GaAs on Si and GaP on Si increased after cooling to room temperature (Tachikawa and Mori, 1990). For GaAs on Si at growth temperature, the density of etch pits was only $10^4/\text{cm}^2$, which is usually observed for commercially obtained GaAs wafers. When the sample was cooled to room temperature, the etch pit density using KOH increased to $8 \times 10^6/\text{cm}^2$. A similar change in etch-pit density from growth temperature to room temperature was observed for GaP grown on Si. There is a much smaller lattice mismatch between GaP and Si than between GaAs and Si. Therefore, these results show that the high density of dislocations observed in both these materials is mainly due to the large difference in thermal expansion coefficient and not to the difference in lattice constants.

Strain distribution in GaAs grown by MOCVD on a Si substrate has been determined by electrolyte electroreflectance (EER) spectra (Kallergi *et al.*, 1989). The GaAs layer was etched in certain sequences in order to reach interfacial areas. A shift of the EER peak was observed. That can be interpreted to mean that tensile biaxial stress exists in most of the GaAs epilayer because of the difference in thermal expansion coefficient, while a

compressive biaxial stress still exists in the layer close to the interface. Another induction that thermal expansion coefficient influences defect formation at heterointerfaces comes from the observation of the nature of misfit dislocations at GaAs/Si interfaces. As was described earlier, misfit dislocations in GaAs on Si are short lines and do not form a regular rectangular grid at the interface, as was observed for GeSi on Si. This rather complicated arrangement of misfit dislocations in GaAs grown on Si may be related to the lattice misfit, the island growth mode, combined with the thermal expansion coefficient difference. Support for this conclusion comes from a study of GaSb ($a = 6.094$ Å) on GaAs (5.653 Å) by Raisin *et al.*, (1991). In this case the lattice mismatch between these two compounds is about 8%, but the difference in thermal expansion coefficient is very small ($\alpha = 5.93 \times 10^{-6}$/C for the GaAs, and $\alpha = 5.7 \times 10^{-6}$/C for GaSb). For a GaSb layer with a thickness exceeding critical thickness, misfit dislocations accommodate the lattice mismatch, so that the grown layer is unstrained. This was confirmed by Raman spectroscopy, where no frequency shift of the GaSb was observed in comparison to the reference signal. This is different from GaAs on Si. Despite the large lattice mismatch between GaAs and GaSb, long Lomer-type misfit dislocations forming a rectangular pattern along the [110] and [1$\bar{1}$0] directions were contained at the interface. Their average spacing was 5.4 ± 0.5 nm, in good agreement with a calculated value of 5.365 nm. These two families of Lomer dislocations cross each other practically without interaction so that not many threading dislocation segments were formed. The threading dislocations were related only to some imperfections of the misfit dislocation network. The density of interfacial dislocations in GaSb was on the order of $8 \times 10^6/\text{cm}^2$. This perfect relaxation of GaSb was related by the authors (Raisin *et al.*, 1991) to two factors: perfect surface preparation before layer deposition, and growth temperature, which was high enough to enable a direct plastic relaxation of the grown layer. This study shows that an epitaxial layer relaxation and Lomer type of misfit dislocation can be formed even for a very large lattice-mismatched system that does not differ much in thermal expansion coefficient.

d. Process-Dependent Factors; Substrate Contamination

The preparation of substrate surface before the growth of epitaxial layers plays a very important role in the structural quality of epilayers. Therefore, different procedures for removal of residual impurities have been developed. This problem is especially important in Si technology, because it is not easy to remove oxides and hydrocarbides from the Si surface. Our own observation (Liliental-Weber, 1989) and those of others (Blakeslee *et al.*, 1987) lead to a conclusion that some impurities, such as oxides or carbides, still

exist on the Si surface despite the careful cleaning procedures applied to Si substrates. Most of the commonly used substrate preparation treatments employ a high-temperature silicon oxide reduction step described by Ishizaka and Shiraki (1986). Four major steps are involved in this procedure: degreasing, acid oxidation, alkaline oxidation, and boiling in $HCl:H_2O:H_2O_2$ (3 : 1 : 1) for 5–7 min followed by DI water rinse. After this procedure, the Si wafers are dried with filtered nitrogen and are mounted on a molybdenum block with In. In the MBE growth chamber, the sample temperature is raised to 800°C for 10 min to disorb the SiO_x. After this procedure the Si surface is considered oxide-free. However, such a high-temperature process is frequently undesirable or impossible in a given growth system. Even after this cleaning procedure, islands of impurities can still be observed (Liliental-Weber, 1989; Blakeslee *et al.*, 1987; Liliental-Weber *et al.*, 1990). Cross-sectional transmission electron microscopy (TEM) typically shows a white band at the interface between the GaAs and Si, which has frequently been attributed to artifacts of the TEM sample preparation (Fig. 12). Our own investigation of metal/GaAs heterostructures deposited *in situ* in ultrahigh vacuum on cleaved GaAs surfaces did not reveal such a white band (Fig. 13).

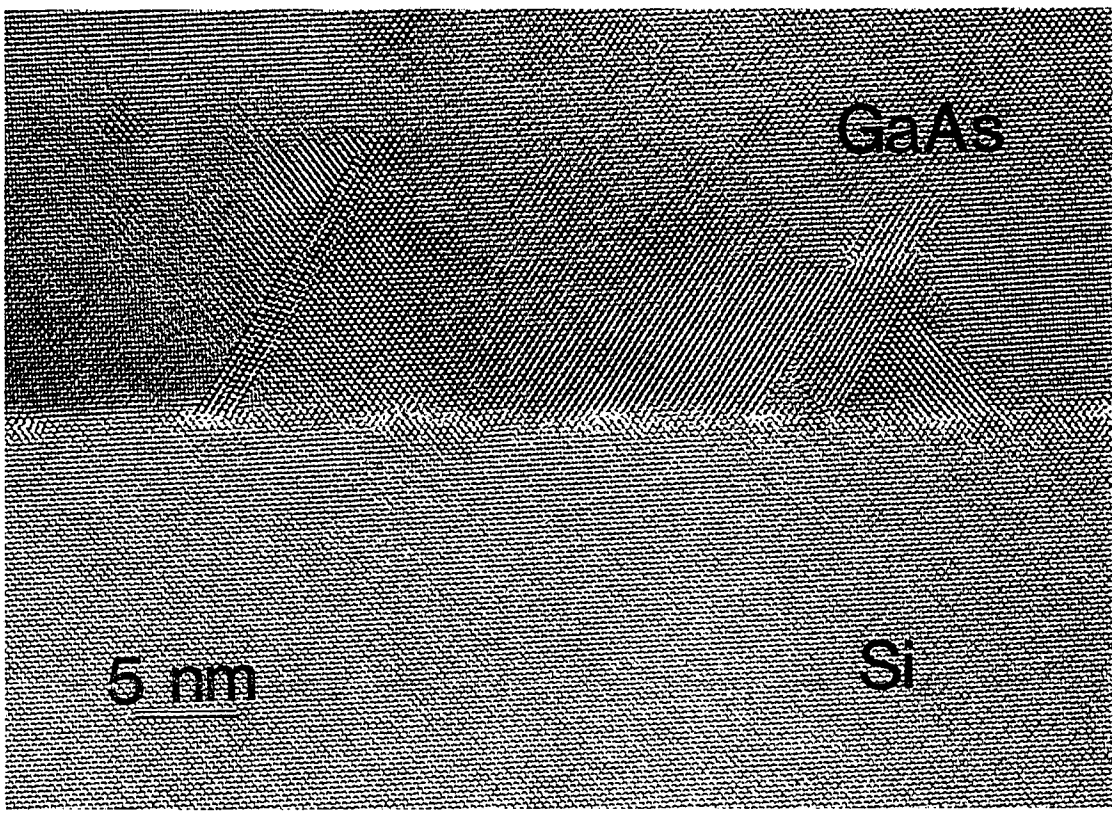

FIG. 12. High resolution TEM micrograph showing white band related to the impurities present at the interface of GaAs layer grown on Si.

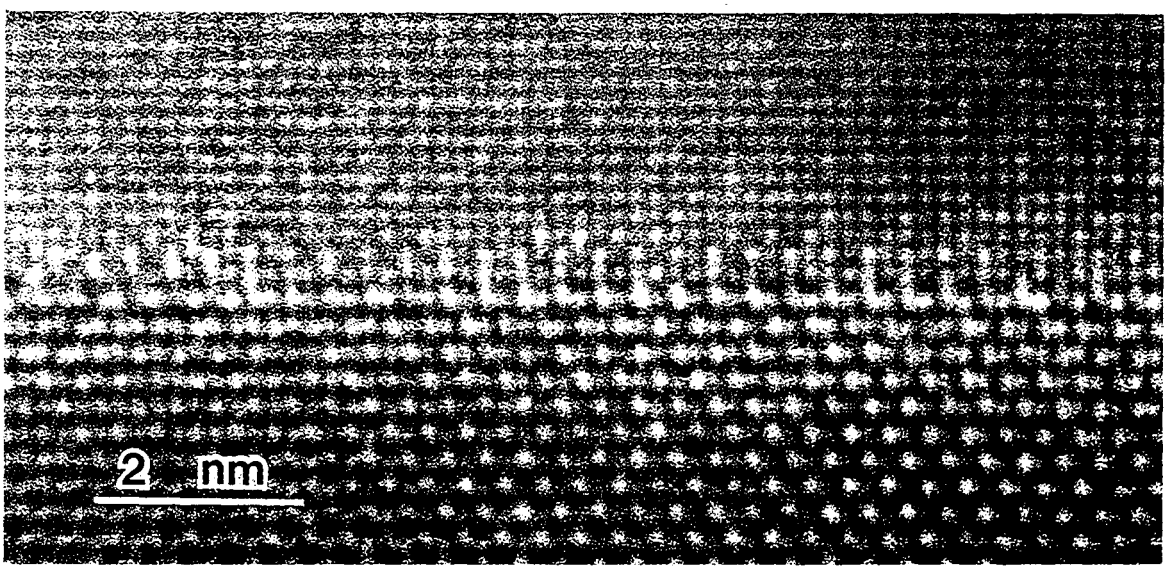

FIG. 13. High-resolution TEM micrograph of Al/GaAs interface for the metal deposited *in situ* on UHV-cleaved GaAs substrate. Note clean interface without white band.

Only air-exposed surfaces showed the white band at the interface (Liliental-Weber *et al.*, 1986, 1990; Liliental-Weber, 1987). In GaAs/Si heteroepitaxy, the formation of this white contrast band does not occur after application of a Ga reduction process (Liliental-Weber *et al.*, 1982), as suggested by Wright and Kroemer (1980). This last procedure differs from those previously described in that during annealing of the Si wafer at 800°C, a beam of Ga was simultaneously impinged on the sample surface. The surface was then considered oxide-free. Lack of a white contrast layer in TEM micrographs confirms that in most cases, this white contrast is indicative of contamination at the heterointerface. Defects such as stacking faults (Fig. 14) or inversion boundaries (Fig. 15) can originate at irregularities caused by contamination at the substrate.

e. Polar-on-Nonpolar Growth

In addition to all the problems previously described in the growth of all heteroepitaxial layers, the growth of GaAs on Si substrates has one more problem, polarity. The lattice structure of Si is composed of two interpenetrating fcc sublattices, both sublattices being occupied by Si atoms. The GaAs lattice is also composed of two interpenetrating fcc sublattices, but each sublattice is occupied by Ga or As atoms. The growth of polar semiconductors on nonpolar semiconductors usually leads to the formation of inversion domain boundaries when the allocation of each sublattice to a particular constituent atom is disturbed. Inversion boundaries are charged structural defects across which the same kind of atoms are bonded. The Ga–

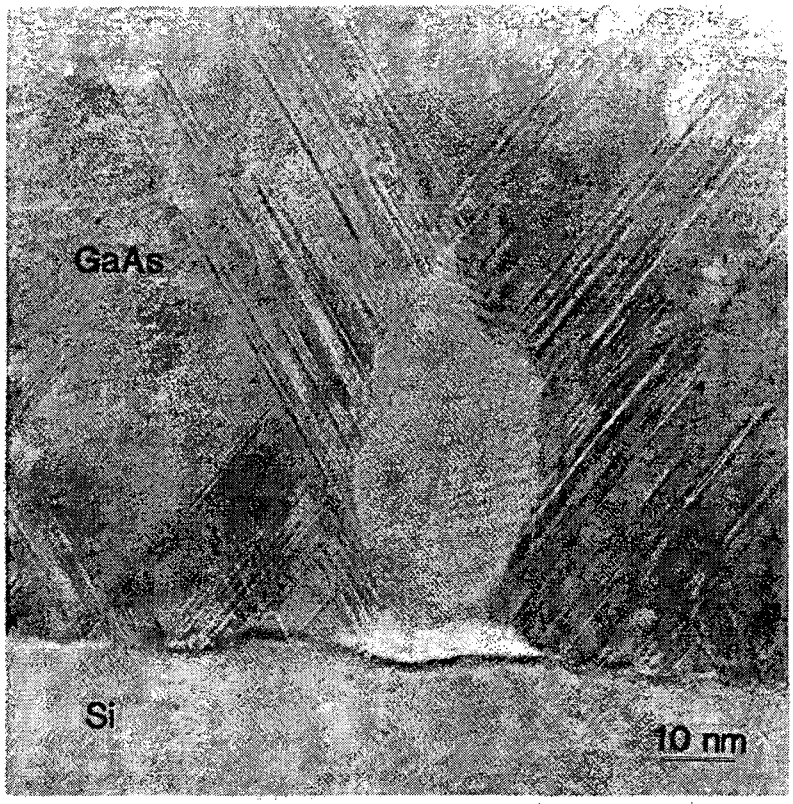

FIG. 14. Stacking faults originating from the impurity island present at the GaAs/Si interface.

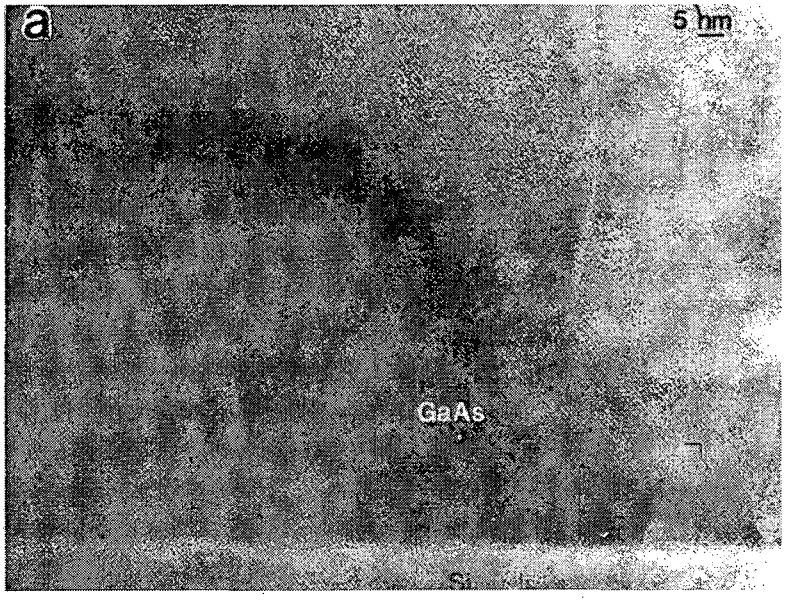

FIG. 15. (a) Inversion boundaries in GaAs grown on Si.

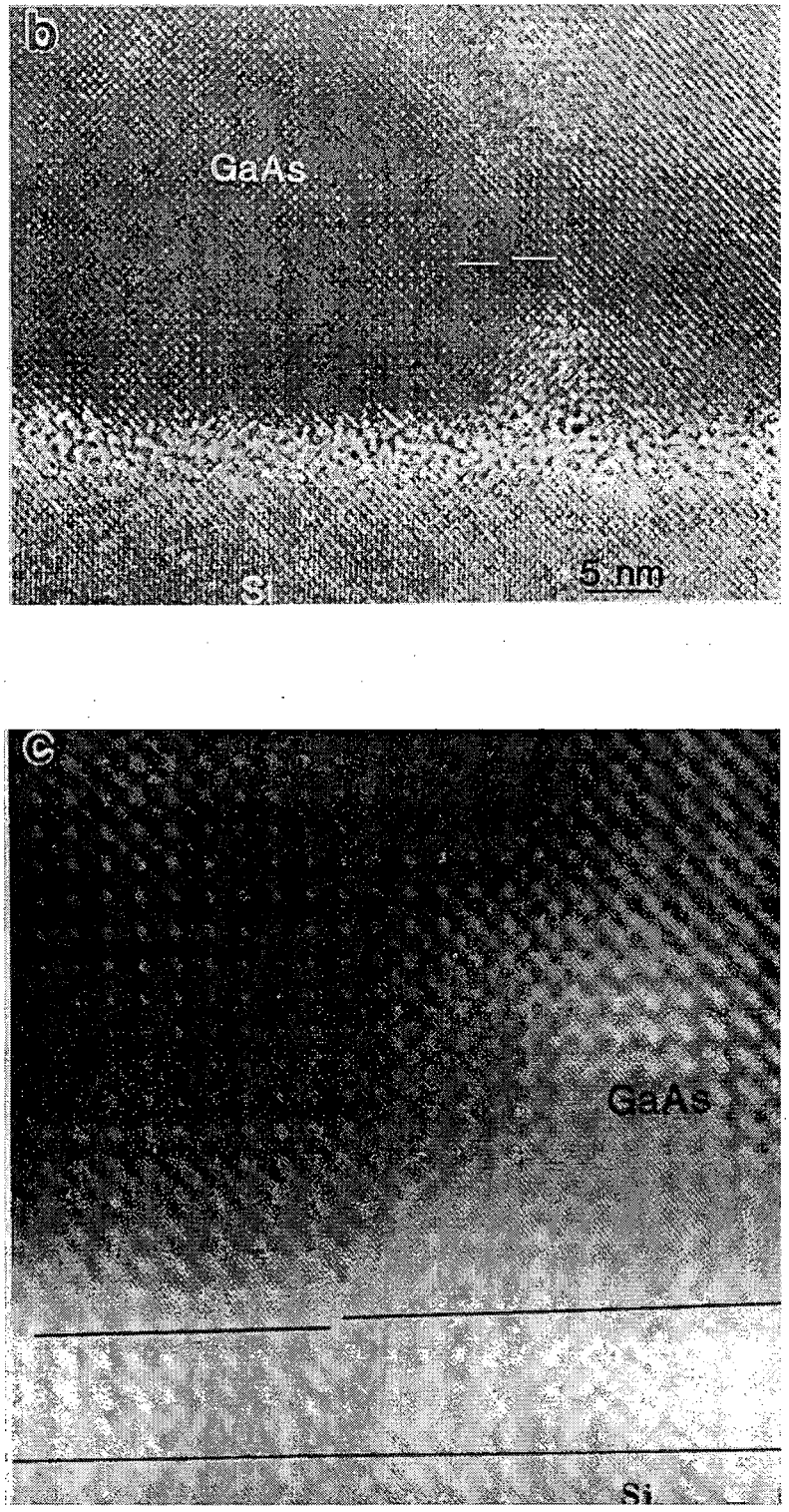

FIG. 15. (b) High resolution image of the inversion boundary shown in (a). Note a shift of (200) planes across the boundary; (c) The same boundary after Fourier image filtering. Note the $\frac{1}{4}$ a surface step at the origin of the inversion boundary.

Ga bond has a bonding electron difficiency and acts as an acceptor. The As–As bond has an excess bonding electrons and acts as a donor. An epilayer with inversion boundaries behaves as a highly compensated semiconductor.

The {100} surface of Si is generally reconstructed (Shirashi *et al.*, 1989) in (2×1) and (1×2), with a monoatomic step between these areas. Growth of GaAs starts with preferred interfacial bonding, mostly Si–As. Therefore, such a two-domain substrate generally results in a two-domain epilayer, with inversion boundaries between the domains. STM studies confirmed that on-axis (100) Si surfaces consist of (100) terraces with monatomic steps (Tromp *et al.*, 1985). The presence of inversion boundaries in GaAs grown on Si can be detected by etching of the GaAs surface (Upal and Kroemer, 1985; Morizane, 1977; Noge *et al.*, 1988) and by TEM analysis using either the convergent-beam method (Liliental-Weber *et al.*, 1988b; Liliental-Weber and Parachenian-Allen, 1986) or the (200) dark-field method (Ueda *et al.*, 1988).

4. DEFECTS IN EPITAXIAL LAYERS

a. Cross-hatches

The first criterion used to judge the quality of an epilayer is its surface morphology. Milky or foggy surfaces usually mean poor epilayer quality and represent rough surfaces. Surface roughening is attributed to unoptimized growth conditions, such as too high a growth temperature and inhomogeneous nucleation. Surface roughening is particularly detrimental to strained layer superlattices or quantum well structures and also causes problems for device fabrication. Although normal optical microscopy shows the mirror-like surface, Normanski interference microscopy can reveal cross-hatched patterns on the surface (Fig. 16). Cross-hatches are composed of ridges along two orthogonal ⟨110⟩ directions on {001} wafers and along ⟨110⟩ at 60° to each other on {111} wafers (Olsen, 1975). Structures with large lattice mismatch ($f > 2\%$) usually do not show cross-hatches, but rather exhibit an irregular, wavy surface (Olsen, 1975). Kishino *et al.*, (1972) reported that cross-hatches were clearly visible on a wafer of GaAsP/GaAs epitaxial system. The cross-hatches seems to be related to the mechanism of strain relaxation in strained epilayers. Cross-hatching can be removed by electrochemical polishing, which implies that cross-hatches are an indication of the surface roughness; however, their origin is not clear (Olsen, 1975). In a study of cross-hatch in InGaAs/GaAs, it was shown that sharp cross-hatch patterns developed only after misfit dislocations were formed at the interface, suggesting that there are surface steps left by moving dislocations (Chang *et*

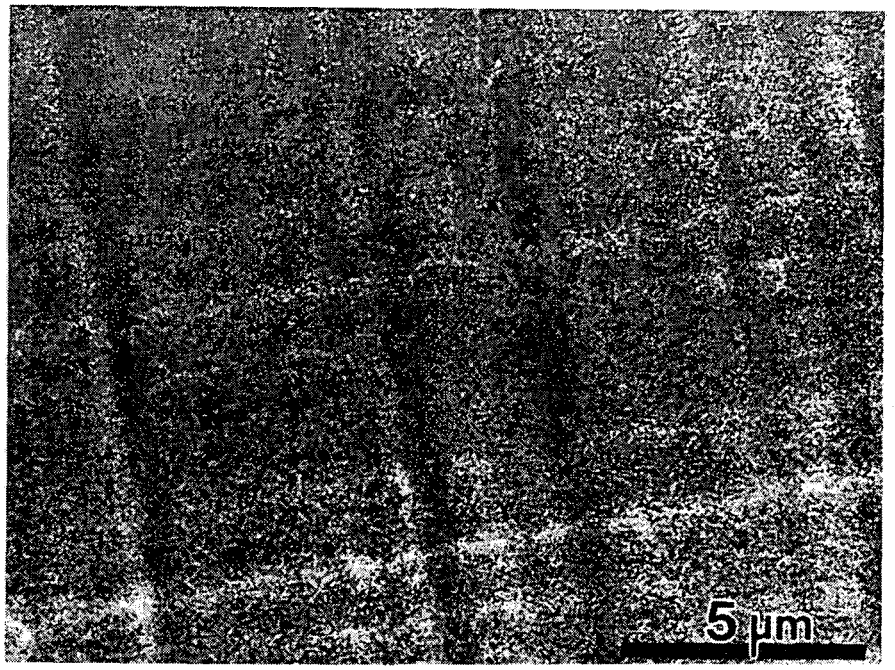

FIG. 16. Cross-hatches visible on the surface of the GaAs layer grown by MBE (after E. A. Fitzgerald *et al.*, (1992).

al., 1990). Fitzgerald *et al.*, (1988) showed that nonradiative recombination lines in CL in InGaAs/GaAs images come from groups of misfit dislocations formed at the interface. Comparison of the SEM and CL images shows that most of the surface ridges correlate with the dark line defects, which are groups of misfit dislocations at the interfaces. However, it is difficult to accept that surface ridges are formed solely by the slip steps if one compares the height of ridges with displacement due to one or two dislocations. These steps still may act as favorable nucleation sites during subsequent growth. Also, the strain field of misfit dislocations at the interface may make the surface just above preferable nucleation sites for growth, resulting in cross-hatched surfaces (Fitzgerald *et al.*, 1988). Cross-hatches can be used to determine the presence of misfit dislocations at the interface by optical microscopy.

b. Dislocations

Misfit Dislocations. In diamond or zincblende structures, perfect dislocations have Burgers vectors **b** of the type $\mathbf{a}/2\langle 110\rangle$, which are the shortest translation vectors. Dislocation lines **u** lie preferentially along $\langle 110\rangle$ directions in agreement with the Peierls potentials. From these Burgers vectors and line directions, one can expect three preferred orientations of perfect dislocations in the diamond structure: pure edge, pure screw, and 60° dislocations. Screw dislocations cannot accommodate misfit between

crystals. Hence, only two types of dislocations are expected to be found at the interface: edge dislocations, with both **b** (e.g., **a**/2[011]) and **u** (e.g., [011]) in the (100) interface, or 60° dislocations with only **u** in the interface (e.g., [011]), but **b** in the one of the four $\langle 110 \rangle$ directions inclined to the interface (e.g., **a**/2[101]). The first type of misfit dislocation is more efficient at accomodating misfit strain. They are sessile because (100) planes are not favorable glide planes in the diamond cubic lattice. The second type of dislocation (60° dislocations) is less effective at accommodating misfit strain because only the edge component of **b** in the interface can relieve misfit strain, the length of which is $\sim 50\%$ less than the Burgers vector of the dislocation. The 60° type of misfit dislocation is mobile because both the Burgers vector and dislocation line lie on a $\{111\}$ glide plane. Although 90° dislocations are more effective for relieving misfit strain than 60° dislocations, 60° dislocations are more often observed at the interface because they can glide into the layer from a nucleation site. Edge misfit dislocations are formed by an interaction between two 60° misfit dislocations. Both types of misfit dislocations can also dissociate into partial dislocations as $\mathbf{a}/2\langle 101 \rangle \rightarrow \mathbf{a}/6\langle 2\bar{1}1 \rangle + \mathbf{a}/6\langle 112 \rangle$, forming a ribbon of stacking faults between them.

As discussed in the previous section, three-dimensional (island) growth is observed for large mismatch. In this case, the high shear stress that develops near the edge of an island as it increases in size can promote formation of defects. In the GaAs on Si system, a TEM study showed that 60° degree misfit dislocations, as well as stacking faults, were often observed near the edges of islands (Tsai and Matyi, 1989). When the islands join to form a continuous layer, these defects remain in the layer, and additional dislocations may be formed by the coalescence.

Threading Dislocations. Misfit strain relaxation requires dislocations only at the interface. But a very high density of threading dislocations is often observed in lattice-mismatched epilayers. As mentioned previously in this chapter, dislocation loops are nucleated at the surface when the thickness of epitaxial layer exceeds a critical thickness. These dislocation half-loops can propagate on the $\{111\}$ planes inclined to the interface, leaving a 60° misfit dislocation segment in the interface and two arms at the end extending up through the layer. These threading arms remain in the layer as threading dislocations. Each loop leaves two threading arms inside an epitaxial layer. Hence, the density of threading dislocations will correlate with the density of misfit dislocation loops nucleated at the surface. Long segments of misfit dislocations in the interface correspond to a small number of threading arms, and short segments of misfit dislocations mean high threading dislocation density. When epilayers grow three-dimensionally, island coalescence can also be a cause of threading dislocations, when extra atomic planes associated

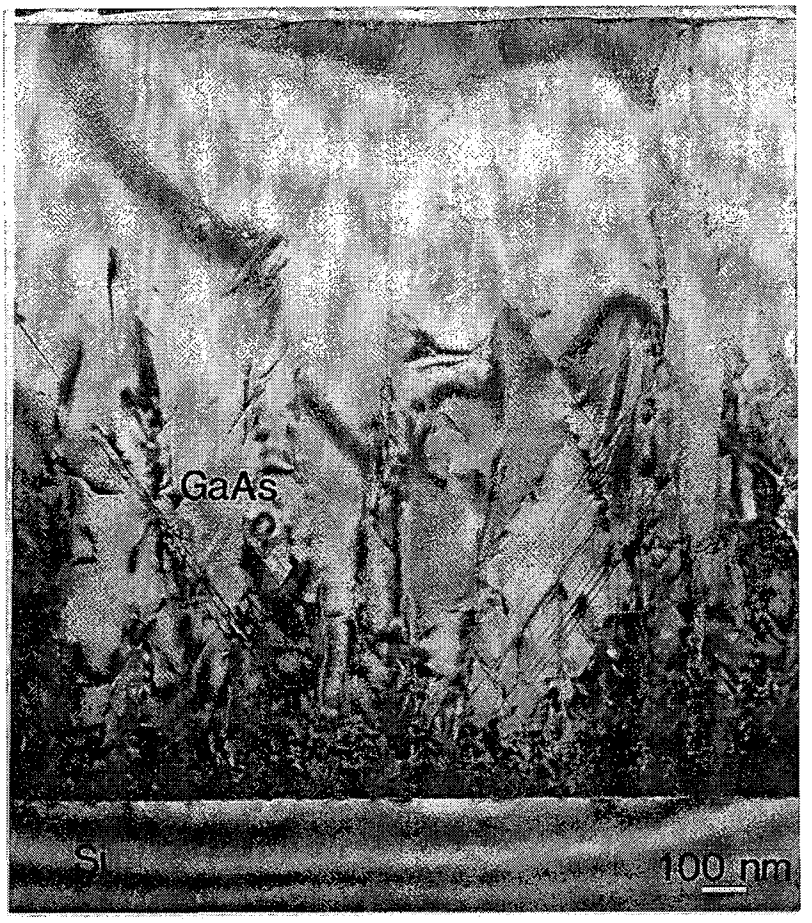

FIG. 17. TEM micrograph showing threading dislocations present in GaAs grown on Si substrate.

with misfit dislocations in adjacent islands do not line up with each other. In this case, densities of threading dislocations will be inversely proportional to the size of the islands at coalescence. Interaction between threading arms may lead to decreased number of threading dislocations. In the case of GaAs/Si epitaxy, the density of threading dislocations near the interface is above $\sim 10^{10}\,\mathrm{cm}^{-2}$, decreasing to $\sim 10^{8}\,\mathrm{cm}^{-2}$ at the top of the layer, even when no special effort to reduce their density has been applied (Fig. 17).

c. *Inversion Boundaries*

Polar on nonpolar growth is connected with the appearance of inversion boundaries (IBs) as previously described. Our observations show that very often such boundaries macroscopically lie on various planes (Fig. 18), such as {111}, although microscopically they consist of terraces on {110} (Fig. 19) (Liliental-Weber *et al.*, 1988b). Orientation of inversion boundaries on {110} is in agreement with Petroff's prediction that {110} and {112} APBs with

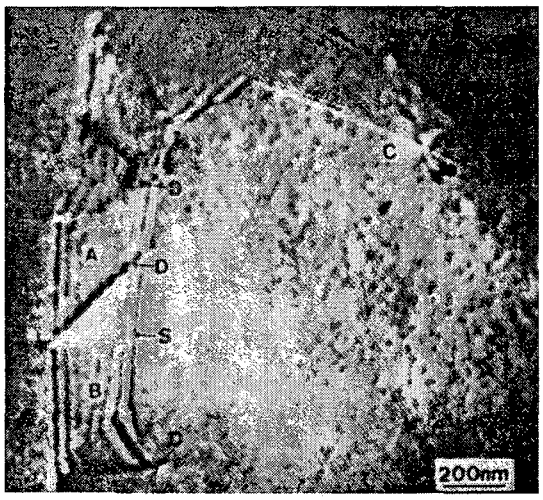

FIG. 18. TEM micrograph showing formation of an inversion boundaries on different crystallographic planes, after C. B. Carter, *et al.*, 1987.

alternating As–As and Ga–Ga bonds have the lowest free energy (Petroff, 1987).

It has been reported that misorientation of the substrate from the nominal (100) orientation by rotation of 2–4° about the [011] direction leads to the disappearance of inversion boundaries (Gale *et al.*, 1981; Masselink *et al.*, 1984; Aspen and Ihm, 1987). Our own observations show that even for such misoriented substrates, inversion domains can be found if the growth conditions are not optimized, preferentially in the areas close to the interface (Nauka *et al.*, 1990). Many of these domains terminate inside the epilayer so that only a small number of inversion boundaries extend to the surface. Drastic changes of the IB density are observed upon changing the growth parameters. After post-growth annealing, IB-free layers were found even on nominal (100) substrates (Noge *et al.*, 1988). The growth of IB-free GaAs is an important achievement in GaAs on Si heteroepitaxy, reached within past years. A self-annihilation mechanism was proposed by Shirashi *et al.*, (1989) to explain the fact that after the growth of about 200 nm of the GaAs by MBE, a change from double-domain to single domain structure occurred. This annihilation was attributed to the fact that two IBs, one on (112) and the second on $(\bar{1}\bar{1}2)$, meet during growth, resulting in annihilation. The Shirashi model was confirmed experimentally by Ueda *et al.*, (1989). The model is consistent with the preference for (112) orientation of IBs proposed by Petroff (1987).

Faceting of APDs was observed earlier by other researchers (Carter *et al.*, 1987), and it was proposed that self-annihilation is taking place on $\langle 111 \rangle$ planes (Cho *et al.*, 1985).

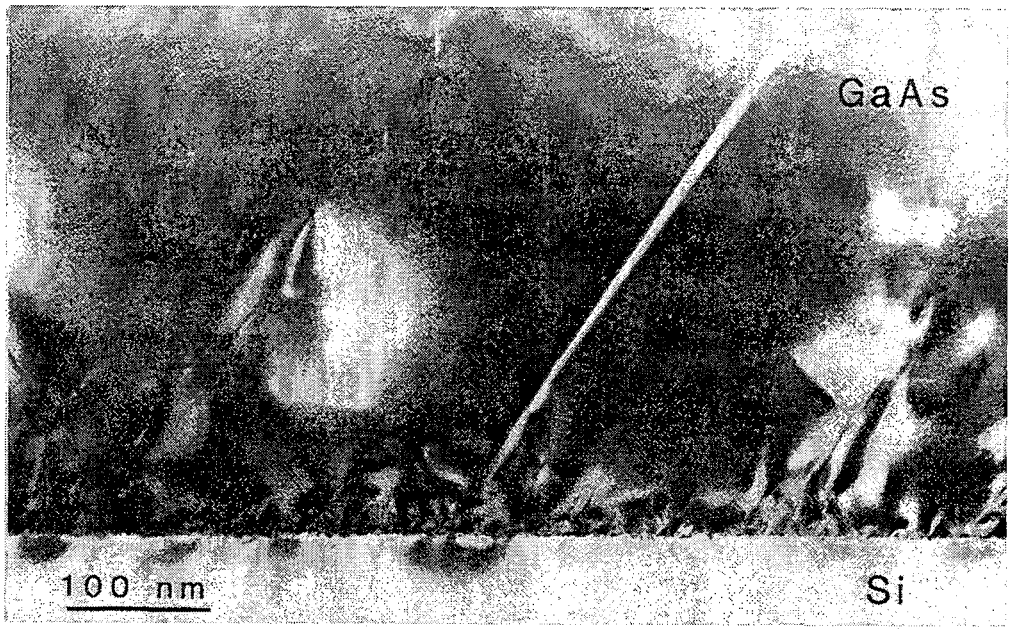

FIG. 19. Inversion boundaries macroscopically formed on (111) planes but microscopically staircase of the boundaries are formed on (110) planes.

d. Stacking Faults and Twins

Stacking faults and twins are major defects observed in GaAs heteroepitaxial layers grown on Si. However, it is not clear if stacking faults are always formed during growth or sometimes also during cooling. Ernst and Pirouz (1989) suggested that deposition errors in the early stages of film growth are responsible for generation of these defects. They suggested that differences in surface energy leads to faceting on low-energy planes. Deposition errors can then occur on {111} facets. They assumed that the energy associated with a misdeposited atomic layer is only 50% of the stacking fault energy, and therefore the misdeposition energy is smaller than the average thermal energy of an atom.

To test the idea that faceting is connected with stacking fault formation, GaAs grown on a {110} GaAs substrate (which has been reported to form a faceted surface—see Allen *et al.*, 1988) was investigated by plan-view and cross-section TEM. Plan-view TEM shows faceting on {111} planes (Fig. 20). However, cross-section TEM performed on these samples does not reveal any stacking faults (Liliental-Weber *et al.*, 1990) (Fig. 21). Therefore, this experiment failed to confirm Piroux's prediction that faceted growth leads to growth errors that nucleate stacking faults. A reason for stacking fault formation that has been supported experimentally is presence of imperfections at the Si surface (Booker and Stickler, 1962).

Another possible explanation for stacking faults is that these defects might

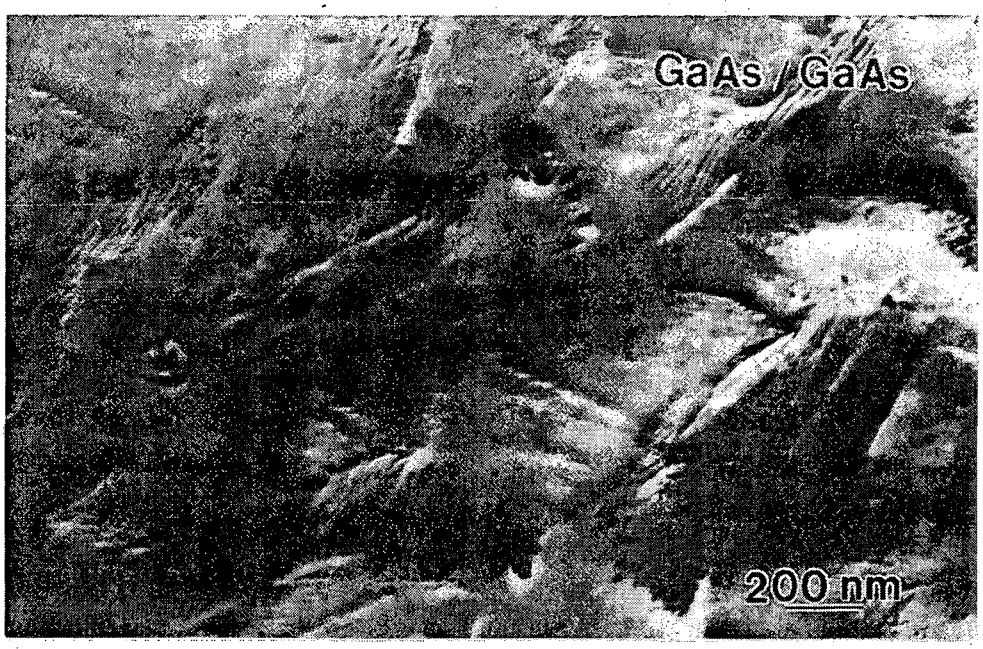

FIG. 20. Faceted surface of the GaAs layer grown on (011) GaAs surface.

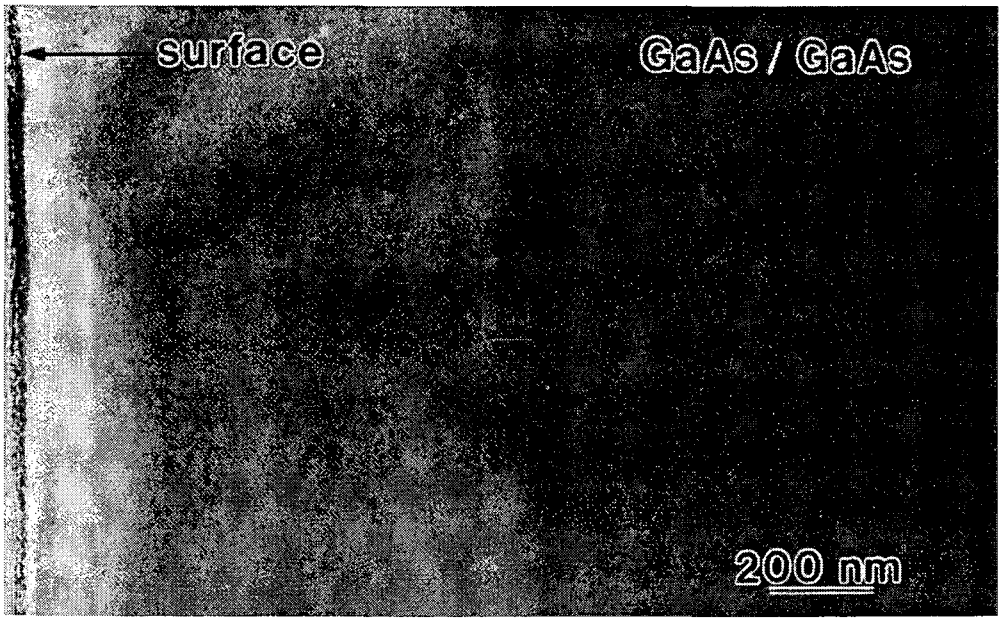

FIG. 21. Lack of stacking faults at the interface with the substrate for the layer shown in Fig. 20.

be formed during cooling. Misfit dislocations could dissociate on a {111} plane inclined to the interface, leaving one partial at the interface and forming an extended stacking fault. The formation of extended stacking faults by this glide process was first found in plastically deformed semiconductors cooled

under high stress (Wessel and Alexander, 1977; Kusters *et al.*, 1986). A misfit dislocation partial traveling from the interface to the top of the layer during cooling and from the top of the layer back to the interface during annealing is a possible explanation for disappearance of stacking faults during annealing.

Another explanation for formation of stacking faults can be their nucleation during the initial stage of growth for strain relief (Pirouz *et al.*, 1988). It was observed by TEM that a high density of stacking faults is formed and extends parallel to the {111} side faces of islands in the early stages of growth. It suggests that several processes can take place that nucleate faults: accommodation of surface irregularities due to contamination, plane misplacement, or island coalescence during growth.

More evidence that island coalescence is a main reason for this defect formation is supported by the work of Cho *et al.*, (1991). They deposited amorphous GaAs on a tilted Si surface at low temperature (solid phase eipitaxy–SPE) before the growth of the GaAs layer. In this case twin distribution on two perpendicular ⟨110⟩ axes was nearly the same, in contrast to the work reported by Lee and Tsai (1987; Tsai and Lee, 1987), who found a large difference in density of the stacking faults on the two perpendicular axes. Hsieh *et al.*, (1988) demonstrated that in two-step MOVPE growth the twin density increased with an increase in the substrate tilt angle. The number of stacking faults increased 80 times on step-rich surfaces compared to flat surfaces. In these techniques the growth is three-dimensional, and island shape was dependent on the degree and the direction of Si misorientation (Rosner *et al.*, 1988; Otsuka *et al.*, 1986). Since in SPE growth the substrate temperature is much lower, the density of nuclei is expected to be high. Nucleation of the GaAs islands probably occurs not only at the Si surface step edges but also on the terraces. This could explain why in SPE growth of GaAs the distribution of islands becomes more independent of substrate tilt. The coalescence of three-dimensional islands appear to be the main cause of stacking fault/microtwin formation (Cho *et al.*, 1991).

IV. Methods to Decrease the Defect Density in the Epitaxial Layers

5. Oval Defects

Oval defects have been attributed to several causes such as surface contamination, Ga-spitting, Ga oxides, and particulates. In order to reduce the density of oval defects, it is necessary that substrates be prepared carefully in an ultraclean environment to avoid C or S contaminations and adhesion of particulates. It is recommended that the growth chamber be baked out thoroughly. Also, sources cells and shutters should be outgassed with caution

in order to remove oxides that can react with Ga. In order to avoid Ga-spitting, it may be necessary to design effusion cells in such a way that the large temperature difference between the bottom and the opening of the Ga effusion cell is reduced so as to avoid the condensation of Ga droplets near the opening of the crucible.

It was shown that oval defects can be avoided using chemical beam epitaxy in which Ga atoms are formed by thermal pyrolysis of the metal alkalis at the heated substrate surface, while As atoms are believed to come from the As_2 dimers being thermally cracked (Tsang, 1985). Replacement of solid Ga sources with gas Ga sources appears to have a fundamental advantage in the elimination of oval defects.

There is experimental evidence that oval defect density is reduced by suppressing Ga oxidation, namely, the reduction of Ga_2O_3. In this case the remaining oval defects were shown to be caused by Ga_2O. The oxide Ga_2O was formed by the reaction between Ga and residual water at the Ga cell with additional reaction with carbon when growth temperature increased above 930°C. It was shown (Shinohara and Ito, 1989) that in order to eliminate these remaining oval defects, not only oxidation but also water content in the growth chamber needs to be drastically reduced.

6. METHODS TO IMPROVE THE QUALITY OF GaAs ON Si

a. Initial Growth; Buffer Layers

Much lower dislocation density in the epilayer can sometimes be obtained when a two-step growth is applied. Usually a buffer layer is grown, followed by the growth of the epilayer. For GaAs on Si grown at 650°C, a noticeable decrease in dislocation density is observed when an initial 10–30 nm buffer layer of the GaAs is grown at 400°C. Dislocation density also decreases with an increase in layer thickness because of the interaction and annihilation of dislocations. Pearton *et al.*, (1988) showed directly by x-ray rocking curve analysis the increase in crystalline quality of the GaAs epilayer with increase in its thickness. However, even with two-step growth, the defect density in these layers was still in the range of $10^9/cm^2$. Difference in thermal expansion coefficient and large lattice mismatch are the primary reasons for such high defect density for GaAs grown on Si.

Low-Temperature Growth. The density of misfit dislocations is related to the existing stress relaxation at the growth temperature. This density is too high after cooling down to room temperature (Liliental-Weber, 1989). TEM observation of this phenomenon confirms the photoluminescence observation of tensile stress in GaAs layers on Si at room temperature, instead of the

compressive stress that would be expected based on the difference in lattice parameters.

In order to have fewer dislocations at the interface and consequently a stress-free layers at room temperature, one can lower the growth temperature. However, results of growth at a temperature as low as 300°C show that instead of just a decrease in the dislocation density, there was an increase in the fraction of partial dislocations (Fig. 22) and consequently stacking faults (Liliental-Weber and Mariella, 1989). This suggests that at 300°C, atom mobility is reduced sufficiently to increase the probability of growth errors, as suggested by Pirouz *et al.*, (1988). Therefore, 400°C appears to be the lowest practical temperature for growth of an initial GaAs layer on a Si substrate.

Two-Dimensional Initial Growth. For low defect density, layer-by-layer growth is preferable instead to island growth. Application of migration-enhanced epitaxy (MEE) (Horikoshi *et al.*, 1986) to the growth of GaAs on Si has resulted in substantial improvements in the crystalline quality of the

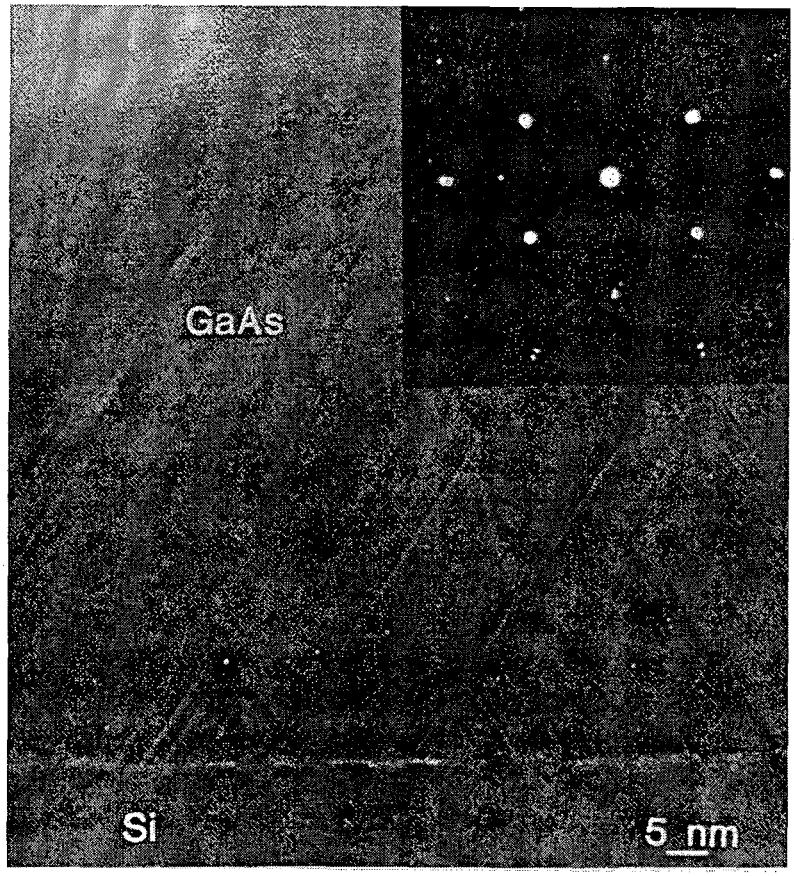

FIG. 22. High density of stacking faults formed at the Si/GaAs interface for a GaAs layer grown at 300°C; the insert shows the diffraction pattern obtained at this interface.

heteroepitaxial films compared with conventional growth methods. An important feature in MEE is the precise and independent control of the group III and V beam fluxes during growth. In MEE growth, the group III and group V beam fluxes are alternately modulated by the opening and closing of the shutter of each effusion cell. In the case of GaAs growth, the absence of As molecules on the host substrate increases the surface mobility of impinging Ga atoms/molecules, thereby increasing the surface diffusion length of the Ga atoms/molecules. This along with the modulation enables a more two-dimensional growth mode. It also allows the growing layer to achieve proper stoichiometry at lower substrate temperature than possible for conventional MBE.

A modification of this method is modulation enhanced epitaxy (Lee *et al.*, 1989), where only the As_4 beam flux is modulated (open and closed) and the Ga beam stays open during the entire growth period. A study of these samples by TEM in plan view showed moiré fringes distributed uniformly over large areas of the sample (Fig. 23). A photoluminescence study on these same samples showed very narrow lines. In these samples, the island nucleation density was increased. However, this growth technique leads to formation of a high density of V-shaped stacking fault pairs.

Another promising method for promoting two-dimensional growth is to start with a lattice-mismatched system, such as AlGaP, which provides very good wetting (George *et al.*, 1989; Noto *et al.*, 1989). The addition of small

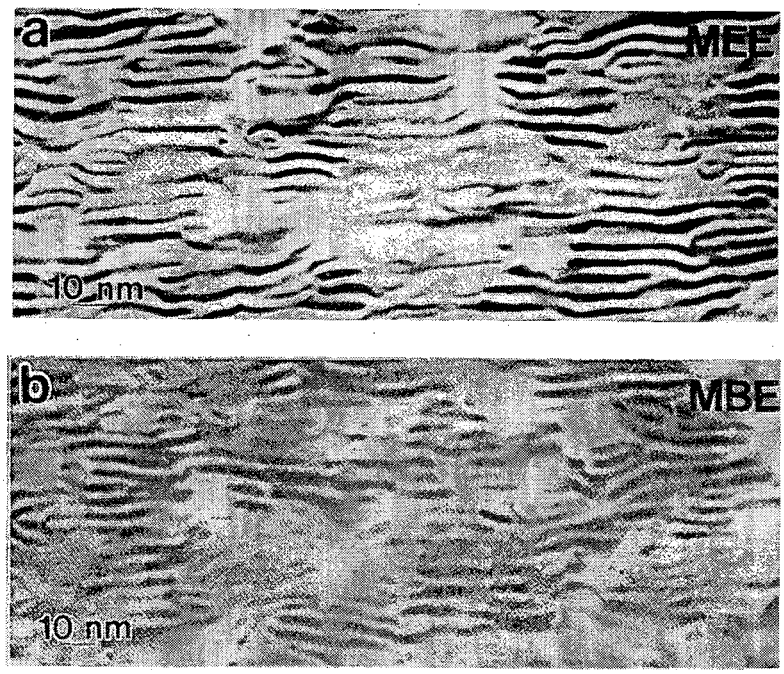

FIG. 23. Plan-view TEM micrograph showing moiré fringes in MEE grown GaAs on Si substrate.

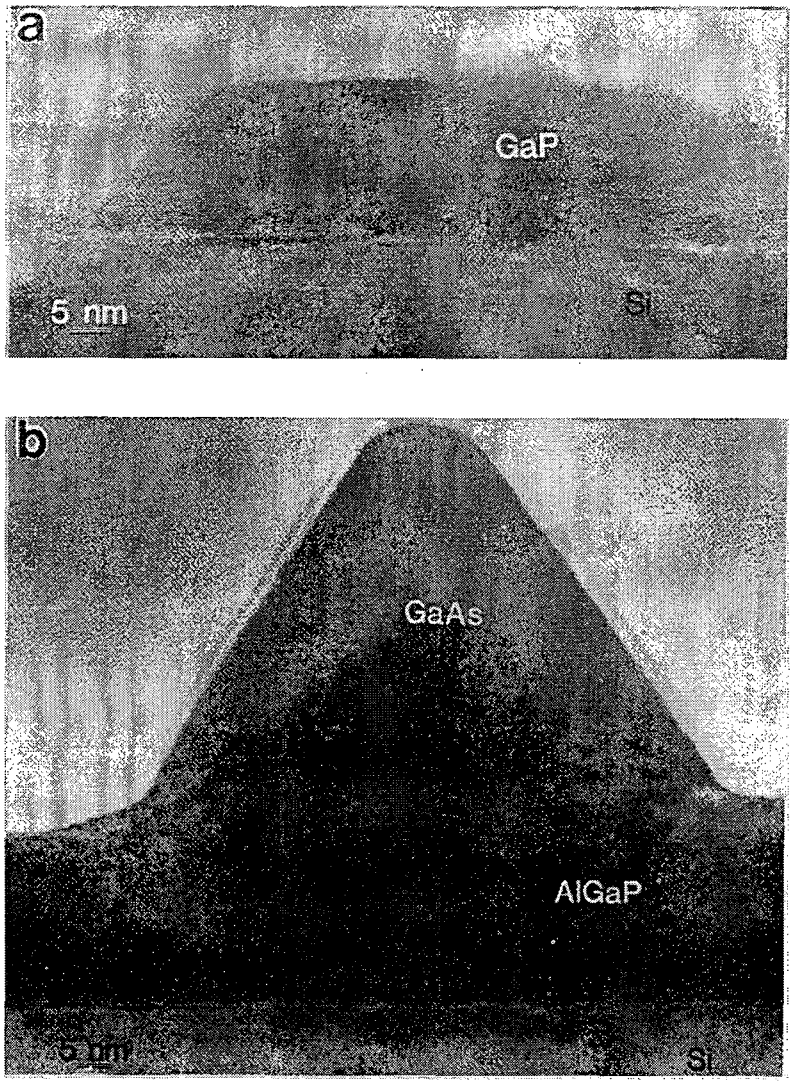

FIG. 24. (a) Island growth of GaP on Si. (b) Two-dimensional growth occurs after adding Al to GaP. Note island growth of GaAs on AlGaP.

amounts of Al causes perfect two-dimensional growth (Fig. 24). This might be due to the high affinity of Al for oxide formation, allowing Al compounds to grow on both clean and contaminated surfaces (George *et al.*, 1989).

b. Thermal Treatments

Conventional Post-growth Annealing. If the heteroepitaxial layer grows strain-free, with the right density of misfit dislocations, any change of temperature will subsequently induce strain, the sign and magnitude of which depend on the difference between the growth temperature and the annealing temperature. Thus, it is possible to move dislocations by changing temperature after growth. It has been reported that annealing of GaAs on Si at

850°C under arsenic overpressure results in dislocation rearrangement at the interface, leading to the formation of Lomer-type dislocations and decreasing the number of stacking faults (Tsai and Lee, 1987; Choi *et al.*, 1987). Our own observations (Liliental-Weber *et al.*, 1990) have not confirmed these results fully. Furnace annealing at 800°C for 10 min changed the defect rearrangement only slightly (Fig. 25). The dislocation density remained in the same range as for "as-grown samples," but dislocations were more tangled. A slight decrease in stacking fault density was observed.

Rapid Thermal Annealing. Noticeable improvements in the quality of GaAs/Si epilayers grown by MBE were observed after rapid thermal annealing (RTA) at 800°C for 10 s by the capless close-proximity method in a commercial heat-pulse furnace (Liliental-Weber *et al.*, 1990). The density of stacking faults after this treatment was reduced (Fig. 26). This result suggests that stacking faults that are removed during heating may be formed again during cooling for conventional furnace annealing by reverse migration of the partial dislocation. During rapid cooling there may be insufficient dislocation mobility for reformation. RTA is beneficial for the removal of stacking faults, but inhibits stress relief during cooling, as evidenced by cracking of the GaAs epilayers. Cracking after RTA was more severe than in as-grown samples. The heterointerfaces were also more undulated after RTA, compared to as-deposited samples. Independent electrical measurements of devices after RTA

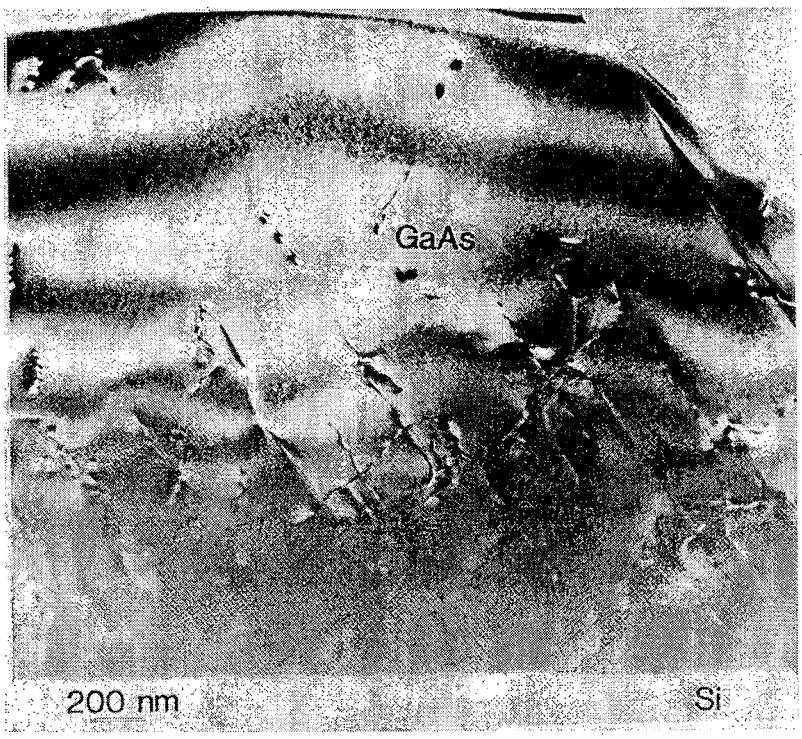

FIG. 25. Defect arrangement in a GaAs layer grown on Si substrate after furnace annealing.

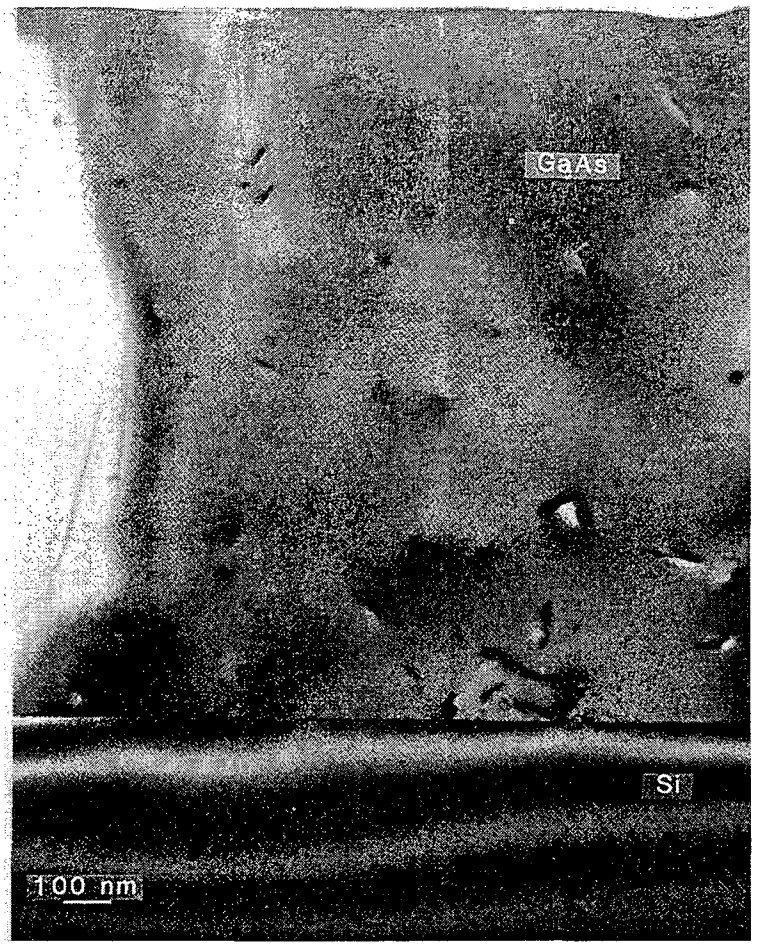

FIG. 26. TEM cross-section of GaAs on Si after rapid thermal annealing. Note lack of stacking faults after such annealing.

(Chand *et al.*, 1987) did show noticeable improvement for forward and reverse bias characteristics. Leakage currents were reduced by more than two orders of magnitude after this treatment.

Thermal Cycling during Growth. It has been reported that *in-situ* annealing at 800°C for 5 min during growth is more efficient for defect reduction than *ex-situ* annealing (Al-Jassim *et al.*, 1988). This causes dislocation to move, thus increasing the chance for threading dislocations to interact with each other or to move to the periphery of the wafer. After this treatment the density of dislocations was reduced (Al-Jassim *et al.*, 1988) to $2 \times 10^{-7}/\text{cm}^2$.

Yamaguchi *et al.*, (1988, 1989) carried out an even more successful thermal treatment during MOCVD growth. It involved thermal cycling during growth in which annihilation and coalescence of dislocations were caused by dislocation movement under an alternating thermal stress. The growth of the GaAs was interrupted several times, and the substrate temperature was

lowered to room temperature, followed by a temperature increase up to 900°C and subsequent annealing for up to 15 min at this temperature in an arsine atmosphere. After this treatment, the substrate temperature was again lowered to 700°C, and a new layer of GaAs was grown in the same fashion. This process was repeated several times. The reported dislocation density for GaAs grown on Si with such thermal cycling was estimated from the etch pit density to be as low as $1-2\times10^6/cm^2$. Such thermal cycling during growth appears to be a very promising approach for decreasing the defect density in heteroepitaxial systems.

c. *Strained-Layer Superlattices*

Another way to promote dislocation migration during growth is to use strained-layer superlattices (SLSs), which cause dislocations to bend into the strained interfaces, thus promoting dislocation interactions. It was reported (Liliental-Weber *et al.*, 1982, 1988a) that by application of SLSs of InGaAs/GaAs with 10-mm thick periods for the growth of GaAs on Si (211), the blocking of dislocation propagation occurred almost entirely at the uppermost interface between the strained layers and the final GaAs layer (Fig. 27). Therefore, reduction of dislocation density was only weakly dependent on the number of periods of the SLSs. InGaAs/GaAs SLSs proved

FIG. 27. TEM cross-section micrograph of the GaAs/Si interface with 50 periods of $In_{0.25}Ga_{0.75}As$/GaAs SLSL grown directly at the interface with Si. Note the large number of stacking faults formed at the interface, propagating through the SLSL and stopping at the last interface with the epilayer of GaAs. Bending of dislocations was most effective at this last interface.

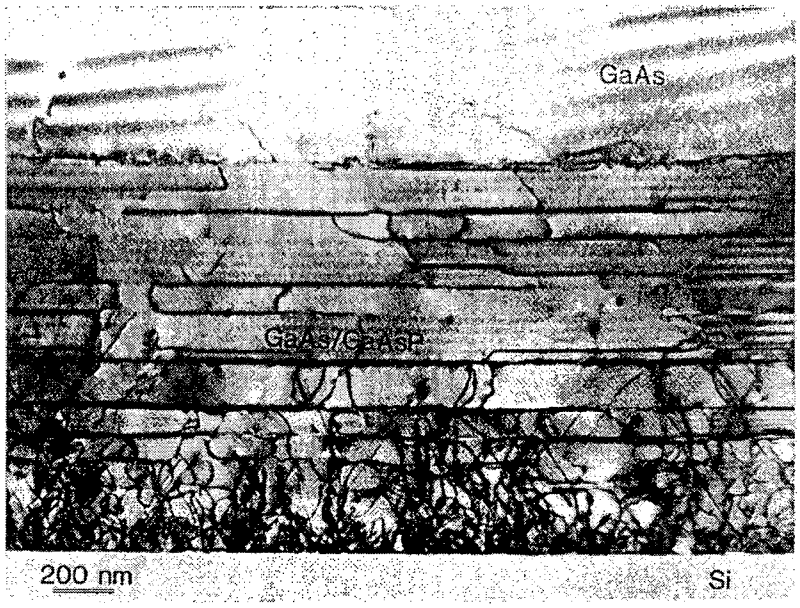

FIG. 28. Formation of new dislocations at the interface of SLSL. (Courtesy of Dr. T. George).

to be more efficient in dislocation bending than InGaAs/InGaP SLSs (Liliental-Weber *et al.*, 1982). Because the upper interface of SLSs was shown to be most efficient in dislocation annihilation, packages consisting of five periods of SLSs (InGaAs/GaAs) were used alternating with thicker layers of GaAs. Each set of SLSs then caused additional dislocation annihilation. However, in some areas additional dislocations were also formed at the lower interface between the buffer layer and the SLS (Fig. 28). On the average, the dislocation density in these samples was in the $\sim 2 \times 10^7/\text{cm}^2$ range, which is very low, taking into account that all misfit dislocations in the GaAs grown on Si(211) are 60° dislocations with Burgers vectors inclined to the interface.

This kind of SLS was also applied to growth of GaAs on Si(100), and results were similar to the ones obtained on Si(211) surfaces (George *et al.*, 1989). Strain is an important parameter to determine the composition of SLSs and their thickness (Yamaguchi *et al.*, 1989). Two critical thicknesses need to be considered to optimize application of SLSs: a critical thickness h_{c1}, which must be exceeded to introduce enough strain for dislocation bending, and a critical thickness h_{c2}, above which the generation of new dislocations becomes significant.

d. Growth on Patterned Substrates

The growth of epilayers on patterned substrates is another promising approach to the achievement of high-quality epilayers. In general, it is difficult to grow a lattice-mismatched epilayer with a network of misfit

dislocations confined entirely to the interface and with no threading dislocations in the epilayer. This would require the threading "arms" of the misfit dislocation half-loop to glide across a whole wafer without being blocked by other dislocations. However, it is easier to achieve this goal if the growth area is reduced by patterning the substrate into mesas.

Luryi and Suhir (1986) have proposed a possible approach to obtain dislocation-free lattice-mismatched epitaxial layers on small seed pads of lateral dimension L. That approach was based on reduction of the strain energy in the epitaxial layer by limiting the strained zone to a narrow layer adjacent to the interface. It was proposed that the entire misfit strain is accommodated by elastic strain if L is smaller than a critical length L_{min}, which depends on the misfit and dislocation type. They suggested that L_{min} is about 20 nm for GaAs on Si, which is too small a dimension to attain conventional photolithography.

Fitzgerald *et al.*, (1989) have shown that for $In_{0.05}Ga_{0.95}As$ grown on GaAs, a drastic reduction in threading dislocation densities can be achieved as the growth area is reduced for circular or square mesas. The interface misfit dislocations were also reduced for epilayers grown on small mesa areas. The experimental critical layer thickness was estimated to be approximately 10 times thicker in these samples compared to large-area samples. Small-area samples had a lower misfit dislocation density than expected from theory. Cathodoluminescence intensity increased approximately 25% as mesa size decreased from 400 to 25 μm, which is a direct proof of reduction in interface-dislocation density. A difference in the dislocation density in the two orthogonal $\langle 110 \rangle$ directions was also observed. This was related to the existence of α and β type dislocations in GaAs.

Three different sources of misfit dislocations were considered: fixed sources (related to defects in substrates), dislocation multiplication, and surface half-loop nucleation. It was shown that α dislocations nucleate more readily than β dislocations. Two-thirds of the fixed sources acted as nucleation sites of α $[1\bar{1}0]$ misfit dislocations, whereas one-third acted as the nucleation sites of β $[110]$ misfit dislocations. When mesa size was decreased close to zero, the dislocation density didn't go to zero. This result was related to the dislocation origination at the substrate surface and was additional proof that only fixed sources were responsible for dislocation nucleation. High elastic strain (Fitzgerald *et al.*, 1989) is necessary for the nucleation of half-loops at the surface. For a layer thickness much greater than the critical layer thickness, this heterogeneous surface nucleation does take place at mesa edges. Dislocation nucleation at round mesas was observed more often than at rectangular mesas. For mesa sizes up to 200 μm, the misfit dislocation density had a linear dependence on mesa size. For larger mesa size, dislocation density increased drastically, possibly because an interaction mechanism

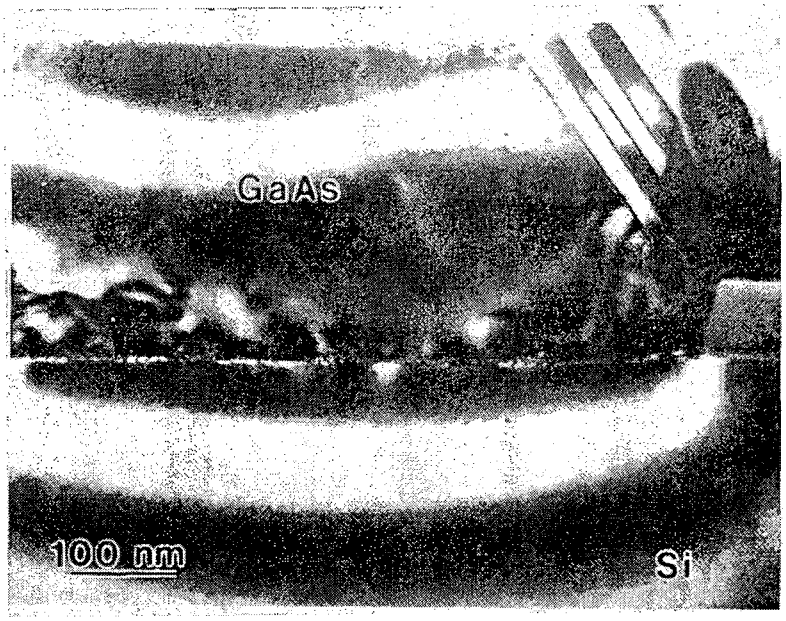

FIG. 29. Cross-section micrograph near the patterned boundary. Note stacking faults present at the boundary with material grown over SiN and very low density of defects within the stripe of GaAs grown on 100 nm stripe of Si.

such as cross-slip or the modified Hagen–Strunk mechanism (Hagen and Strunk, 1978) became possible.

It has been shown (Yamaguchi *et al.*, 1990) that in as-grown GaAs films on Si substrates the major component of the large residual stress of about 1.5×10^9 dyn/cm^2 is caused by differential thermal contraction. Substantial reduction in the biaxial stress was obtained by post-growth patterning of GaAs grown by MBE on Si substrates. It was shown that reduction in stress is dependent on the pattern size and shape. For stripe patterns less than 15 μm wide, the stress becomes uniaxial with stress relief normal to the stripe direction. Rectangular patterns exhibited stress relief in orthogonal directions and had the lowest stress in the narrow direction of the rectangle (van der Ziel *et al.*, 1989; Lee *et al.*, 1988).

High-quality GaAs films with low etch-pit density were obtained from low-pressure MOCVD and MBE on patterned Si films with various mesa sizes (Yamaguchi *et al.*, 1990; Sohn *et al.*, 1991). Cathodoluminescence peak shift was used for residual stress measurement in the MOCVD-grown samples (Yamaguchi *et al.*, 1990).

Results (Lee *et al.*, 1988) on the growth of GaAs on Si through openings in an oxide or nitride show that GaAs deposited on the Si_3N_4 mask was polycrystalline, but lower dislocation density was observed in the open areas where the nitride had been removed, similar to the observation for mesa growth (Sohn *et al.*, 1991). The stacking fault density was also much lower in

the monocrystalline GaAs regions, increasing only at the border with the nitride mask (Fig. 29).

Porous silicon has also been proposed as seed pads for GaAs on Si growth. But the improvement so far achieved in epilayer quality is not impressive (Lin *et al.*, 1987).

Improvement of the quality of GaAs on Si has also been obtained with growth on sapphire. A misorientation away from (100) was introduced and two sets of samples were compared: those grown directly on Si, and those grown on Si on sapphire (SOS). Low-temperature GaAs buffer layers were grown on both samples. In the samples grown on 6° misoriented SOS, the photoluminescence intensity increased 30 times, compared to the samples grown directly on Si. This was explained by stress relief. Reduction of stress for GaAs on SOS was expected because of the closer match of thermal expansion coefficients between GaAs and sapphire. Metal–semiconductor field effect transistors (MESFETs) fabricated on these materials had device characteristics comparable to those of GaAs on GaAs (Metzger *et al.*, 1990).

7. DEFECT REDUCTION FOR OTHER III/V HETEROEPITAXIAL LAYERS

Although the feasibility of InGaAs/InAlAs HBTs and MODFETs on GaAs substrates was demonstrated (Won *et al.*, 1988), the problem of the lattice mismatch between epilayers and substrates was left unsolved. More recently, it was shown that the use of a graded $In_xGa_{1-x}As$ buffer layer grown at a relatively low temperature of about 400°C improves the electron mobility in this lattice-mismatched system. The electron mobility at 300 K increases monotonically with an increase in In composition, from 7000 cm^2/Vs at $x = 0.2$, to 10,500 cm^2/Vs at $x = 0.53$, and to 20,000 cm^2/Vs at $x = 1.0$. At 77 K 118,000 cm^2/Vs was obtained at $x = 0.8$. These high mobility values indicate that the dislocations created to relieve the strain are efficiently confined in the buffer layer, and the propagation of threading dislocations into the active layer is minimal (Inoue *et al.*, 1991). Successful InGaAs/InAlAs modulation-doped heterostructures that are lattice-mismatched to GaAs substrates for a full In composition range have been demonstrated.

A highly perfect InGaAs/InP strained layer superlattice has been obtained by using gas-source molecular-beam epitaxy (Vanderberg *et al.*, 1989). The advantage of this method is a capability for excellent control of composition and layer thickness, which makes it possible to grow very closely matched layers as well as strained-layer superlattices (SLSs). The layers with a nominal In concentration as low as $x = 0.075$ and a thickness of ~ 2 nm were

obtained. High crystal perfection was reported based on high-resolution x-ray diffraction.

It has been shown that interface structure of AlGaAs/GaAs heterostructures is affected by surface segregation of impurities in the AlGaAs layer. Interface smoothness was improved by using substrates 2–4° off (100) toward ⟨111⟩ GaAs, and by incorporating thin layers of GaAs at regular intervals in AlAs (Chand and Chu, 1990). Incorporation of these GaAs smoothing layers increased photoluminescence three times.

V. Conclusions

This review makes it clear that there are many factors that influence defect formation in epitaxial layers. Defects are often formed because of impurities present on the substrate. This source of defects is common for homoepitaxial and heteroepitaxial layers. In many cases these defects can be avoided by proper cleaning procedures.

Another class of defects is related to the growth parameters, such as growth temperature and the flux ratio of the elements used to the growth. This has been observed for homoepitaxial growth such as GaAs grown at low temperature on GaAs. These defects can often be avoided by choosing optimum growth parameters. However, there are defects related to lattice mismatch and difference in thermal expansion coefficient that cannot be easily avoided, where they are detrimental for device performance. Methods to avoid their propagation into the active areas of the devices need to be applied. Reduction of dislocation density in difficult heteroepitaxial systems such as GaAs grown on Si has been possible to some extent. Controlled growth of antiphase domain-free GaAs/Si has been achieved. The cleaning of the Si substrates has been improved, but is not yet completely satisfactory. Of special interest should be development of cleaning procedures that avoid the high-temperature substrate annealing currently used. Such high annealing temperatures result in roughening of the Si surface and are generally incompatible with patterned epitaxy.

Further dislocation density reduction strategies, such as thermal cycling during growth, post-growth annealing, and the use of buffer layers such as strained-layer superlattices, still have to be optimized. Combined use of some of these methods together with use of patterned epitaxy should lead to higher-quality growth of lattice-mismatched heterostructures such as GaAs/Si and InGaAs/GaAs for practical application in minority carrier devices, the feasibility of which has already been demonstrated with GaAs/Si heteroepitaxy and other ternary compounds grown on GaAs or InP substrates.

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