UNIVERSITY OF CALIFORNIA SAN DIEGO

D-Band Wafer-Scale IF beamforming Transmit and Receive Phased-Array Systems with On-Chip Antennas

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Siwei Li

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor Kam Arnold
Professor Gert Cauwenberghs
Professor Drew Hall
Professor Tzu-Chien Hsueh

2021

The dissertation of Siwei Li is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2021

DEDICATION

To my beloved family and friends

EPIGRAPH

The people, and the people alone, are the motive force in the making of world history.

–Chairman Mao

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Chapter 2, in part, is a reprint of the material as it appears in: S. Li and G. M. Rebeiz, "A 134-149 GHz IF Beamforming Phased-Array Receiver Channel with 6.4-7.5 dB NF Using CMOS 45nm RFSOI," *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Los Angeles, CA, USA, 2020, pp. 103-106, doi: 10.1109/RFIC49505.2020.9218355. The dissertation author was the primary investigator and author of this paper.

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VITA

2016	Bachelor of Science in Microelectronics, Peking University, Beijing, China
2018	Master of Science in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego
2021	Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego

PUBLICATIONS

S. Li, Z. Zhang, B. Rupakula and G. M. Rebeiz, "An Eight-Element 140-GHz Wafer-Scale IF Beamforming Phased-Array Receiver with 64-QAM Operation in CMOS RFSOI", in *IEEE Journal of Solid-State Circuits*, doi: 10.1109/JSSC.2021.3102876.

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ABSTRACT OF THE DISSERTATION

D-Band Wafer-Scale IF beamforming Transmit and Receive Phased-Array Systems with On-Chip Antennas

by

Siwei Li

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2021

Professor Gabriel M. Rebeiz, Chair

5G wireless technologies have been developed for many years, and is meant to deliver multi-Gbps peak data rates, ultra low latency, and massive data capacity. With the recent advances in communication systems at $>$ 100 GHz, the so-called beyond 5G or 6G have been enabled at the wide sub-THz spectrum, which is unlicensed and and has few interferers due to low radiated power and high space loss factor at this frequency range. This frequency range is now available for promising applicatoins, such as low-range Internet-of-Things (IoT), advanced or virtual reality (AR/VR), immersive tourism, etc.

This dissertation focuses on building high performance and low cost phased-array systems

and the related circuits at D-band in an advanced CMOS silicon-on-insulator (SOI) process for short-range and high data rate communications. It presents eight-element receive (RX) and transmit (TX) wafer-scale phased-array systems with on-chip antennas at around 140 GHz. The antenna arrays are fabricated on the quartz wafer and attached to the chip wafer, and electromagnetic (EM) coupled to on-chip antenna feeds. Both arrays are wirebonded on low-cost printed circuit boards (PCB). A high-IF beamforming architecture is introduced at 140 GHz for low single sideband (SSB) noise figure (RX) and high in-band linearity (TX). An IF beamformer (phase and amplitude control) at 10-20 GHz is easier to implement with lower power consumption and RMS errors than an RF beamformer.

This dissertation also presents D-band power amplifiers (PAs) in CMOS SOI as the front-end circuits for transmitters or phased-array transmitters. A multi-way power combining technique is introduced and employed to realize PAs high output power and efficiency.

Record results in system NF and EIRP are demonstrated for RX and TX arrays, together with $>$ 10 Gbps communication links for TX and RX systems and using 64-QAM waveforms. The presented PAs also achieve record saturation power (Psat), output 1-dB compression power (OP_{1dB}) and power added efficiency (PAE), compared to the prior art in CMOS.

Chapter 1

Introduction

In the past decade, the wireless industry has witnessed a lot of research and commercialization efforts for the well-known fifth generation (5G) wireless communication to address the demand for high data rates, data capacity and low latency [1]. Mm-Wave spectrum, such as 28 GHz, 39 GHz, and 60 GHz have been assigned and licensed for the 5G networks. Besides the 5G bands, other frequency spectrum at $<$ 100 GHz has also been developed, such as 77 GHz, which is widely used for autonomous radars, and 94 GHz for short-range imaging systems.

To further investigate the potential for higher bands, the Federal Communications Commission (FCC) moved to open spectrum above 95 GHz for new technologies experimentation and wireless innovations, and this may lead to beyond 5G or 6G [2]. Communication systems at $>$ 100 GHz, as the most important hardware, are capable of using a lot of unlicensed and unallocated frequency spectrum resources for ultra-high data-rate links. Many promising applications have a soaring demand for data rate and capacity and one example is indoor automated end-to-end services or industrial IoT, such as the machine-machine and robot-robot real-time crosstalks. Another is the near-range high-data-rate/low-latency communications, like augmented reality (AR) or virtual reality (VR).

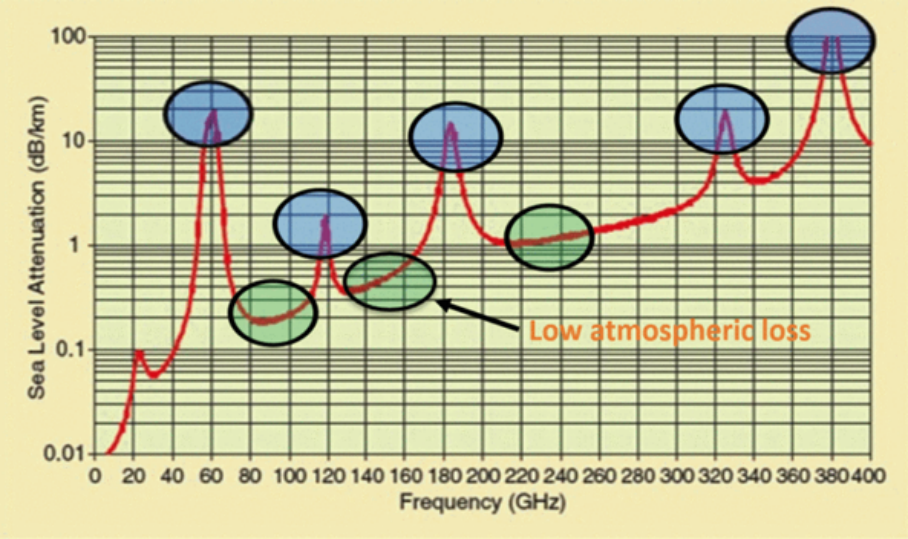


Figure 1.1: Atmospheric absorption of electromagnetic waves

1.1 140 GHz

There are abundant spectrum resources above 100 GHz. The spectrum at $\sim$ 140 GHz (130-150 GHz) typically called D-band has been used to demonstrate the work in this dissertation. There are two main reasons to choose this special sub band:

First, as presented in Fig. 1.1 [3], the 130-150 GHz frequency range, as one of the sub bands of D-band, is suitable for longer-range wireless broadband mobile since it has less atmospheric absorptions (e.g., oxygen and water molecule absorptions) resulting in lower path loss than the 120-130 GHz range or the 170-180 GHz range.

Second, it is possible to realize low-power communication and radar systems using low-cost silicon technologies, such as SiGe and CMOS at 140 GHz, since advanced CMOS processes usually have $>$ 300 GHz f_T and f_{max}, which means that a transistor or a transistor pair has enough intrinsic gain to realize a reasonable performance at 140 GHz.

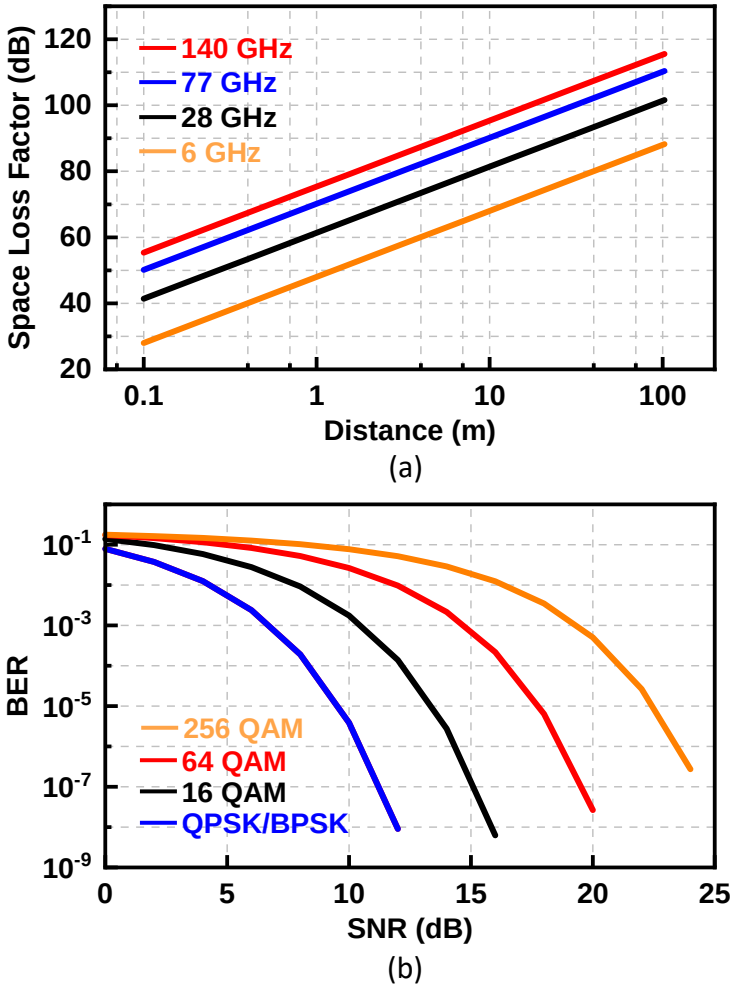


Figure 1.2: (a) Space loss facter versus communication distance. (b) Bit-error rate versus signal-to-noise ratio.

1.2 140 GHz Phased-Array Systems

Compared to lower frequency systems, 140 GHz systems have much higher free space path loss (FSPL) [Fig. 1.2(a)] which degrades the modulated signal SNR resulting in high bit error rate (BER), and this limits the data rate according to the Shannon theory [4] [see Fig. 1.2(b)]. To address the space loss issue, phased-array systems are important and desired to greatly improve the signal SNR (RX) and EIRP (TX), and also maintain a high link budget at 140 GHz over a

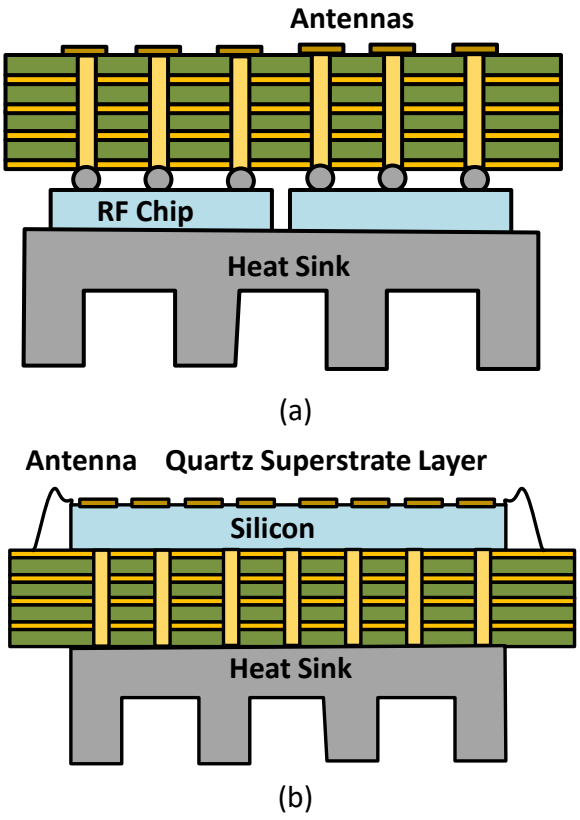


Figure 1.3: (a) Phased-array systems with antennas on PCB and chips mounted on PCB directly. (b) Wafer-scale phased-array systems with antennas on quartz superstrate

wide angular region by using electronic beam scanning.

Generally, there are two approaches to build phased-array systems. The conventional method is presented in Fig. 1.3(a) and is widely used up to W-band [5–8]. Antenna arrays are manufactured using a multi-layer printed circuit board (PCB) and the 2×2 or 4×4 RF beamforming beamformer chips are mounted on the PCB. They are easier to build with less chip-level design efforts (compared to wafer-scale approach) and good choices for scalability. Morevover, antennas also can be designed with wideband performance and more design flexibility. However, this method results in non-optimal performance above 94 GHz since the RF transitions from the chip to the antenna is lossy. Therefore, in this dissertation, the wafer-scale approach with

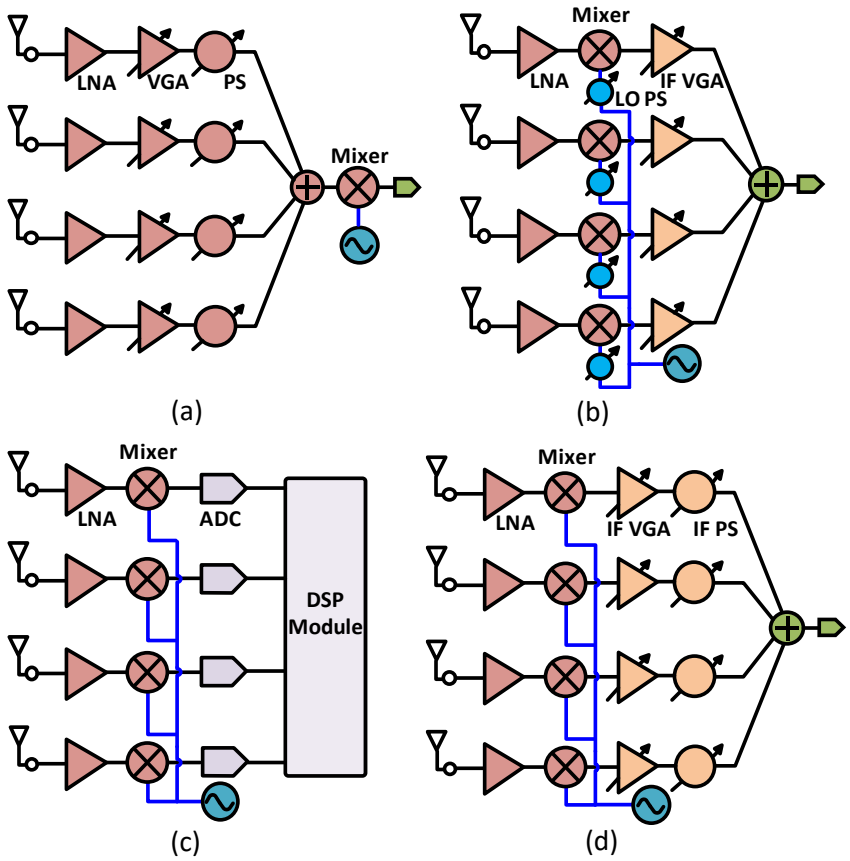


Figure 1.4: Beamforming architectures: (a) RF beamforming, (b) LO beamforming, (c) digital beamforming, (d) high-IF beamforming.

quartz superstrate approach [Fig. 1.3(b)] is employed and demonstrated [9–11]. High-efficiency on-chip quartz superstrate antennas greatly reduce the transition loss from the chip to antenna array. The cost of the PCB and its corresponding assembly is also much lower, compared to the conventional approach (antennas on PCB) since it only contains IF and LO (local oscillator) signals which are at much lower frequencies than 140 GHz.

1.3 140 GHz Beamforming Architecture

In order to build a large-scale phased-array at 140 GHz, a practical beamforming architecture with phase and amplitude control on each element is desirable. Fig. 1.4 presents serveral

different beamforming architectures and a receive (RX) architecture is analyzed as an example. The conventional all-RF beamforming architecture is widely used at 6-100 GHz [5–8]. However, at 140 GHz, it suffers from high phase shifter loss and noise figure. Also, to calibrate the gain difference among elements, RF gain control blocks with low phase variation are required, which are hard to implement at 140 GHz due to the transistor parasitic capacitance effects which distorts the phase as the gain is lowered. LO beamforming has similar phase shifter issues. Extra LO drivers are also required to compensate the phase shifter loss and consume a lot of power. Digital beamforming architecture is not practical due to much higher power consumption, which mostly comes from the I/Q quadrature LO paths to drive the mixers and analog-to-digital converters (ADCs) with high sampling rate and bandwidth. The high-IF beamforming architecture is introduced at 140 GHz for low single sideband (SSB) noise figure and power consumption. An IF beamformer (phase and amplitude control) at 10-20 GHz is easier to implement with lower power consumption and better NF and RMS errors than an RF beamformer. Compared to the digital beamforming and LO beamforming, which are power hungry, both IF and RF beamforming architectures are possible. In this work, the high-IF beamforming architecture is chosen as a promising solution for 140 GHz phased-arrays.

1.4 Challenges in D-band Power Amplifiers

As mentioned above, the free space path loss (FSPL) is high at D-band, and a practical system always requires a large transmit power with reasonable efficiency. This makes the power amplifiers (PAs) as one of the most important and challenging blocks in phased-array transmitter designs. A high gain, output power, linear and efficient PA is required to meet the system design target. In order to improve the system integration level and enable the proliferation of D-band systems, advanced CMOS processes with low-cost and high-yield are preferable. However, the III-V technologies, such as InP and GaN or SiGe processes outperform CMOS processes [12]

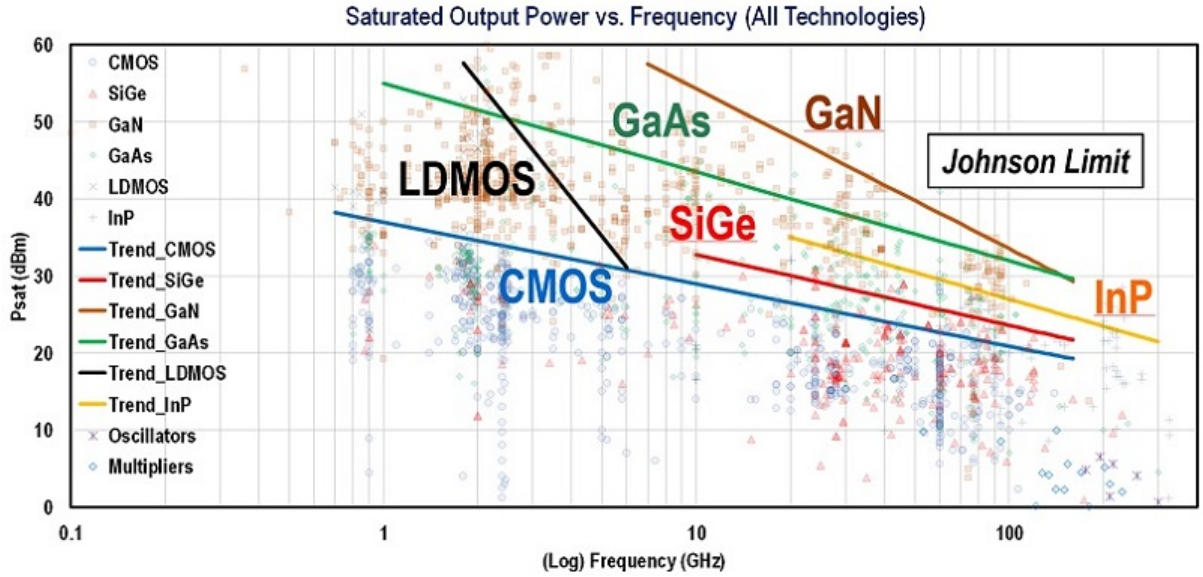


Figure 1.5: Power Amplifiers Performance Survey 2000-Present.

since the breakdown voltage of the advanced MOS transistors is very low ($\sim$ 1 V) which limits the transistor linearity and maximum output power. In the prior art, CMOS-based PAs above 110 GHz have been limited to $<$ 15 dBm in output power [13]. In this dissertation, an ultra-low loss multi-way power combining technique is proposed at 140 GHz and is implemented to break the performance limitation of CMOS power amplifiers.

1.5 Thesis Overview

This thesis presents demonstrations of low-cost and high performance D-band wafer-scale phased-array systems and their system analysis. High linearity and efficiency PAs are also presented in this dissertation.

Chapter 2 presents a 140-GHz 8-element wafer-scale phased-array receiver based on intermediate-frequency (IF) beamforming with 5-bit phase and 4-bit gain control. The chip contains a shared local-oscillator (LO) multiplier chain and distribution network, active combiners, LC-based combiners, digitally tuned attenuators, for a near system-on-chip solution. A differential

on-chip antenna feed (on the top metal) is electromagnetically (EM) coupled to a high-efficiency patch antenna (gold) on a 100-μm-thick quartz superstrate, and placed λ/2 (∼140 GHz) apart in the horizontal and vertical directions. The 4×2-element phased-array chip with attached quartz superstrate is wirebonded to a printed circuit board containing IF and LO ports, and scans to ±35° in the elevation plane (*E*-plane). The measured channel NF is 7 dB and the array electronic gain is 27-28 dB with an RF front-end 3-dB bandwidth of 139-155 GHz and an IF bandwidth of 9.5-12.5 GHz. To evaluate the over-the-air performance, a communication link is demonstrated with 16-quadrature amplitude modulation (QAM) and 64-QAM waveforms, realizing up to 9-10 Gb/s data rates. To the best of our knowledge, this paper presents the first CMOS wafer-scale phased-array receiver at 140 GHz with low system noise figure and high data rate.

Chapter 3 presents a 140-GHz 8-element wafer-scale phased-array transmitter based on intermediate-frequency (IF) beamforming with 5-bit phase and 4-bit gain control in the GlobalFoundries 45RFSOI process. The chip contains a shared local-oscillator (LO) multiplier chain and distribution network for a near system-on-chip solution. Image rejection filters are designed before the RF front-end power amplifiers to suppress the image and improve the power amplifier (PA) linearity. A differential high-efficiency patch antenna on a 100-μm-thick quartz superstrate is used, and the antennas are placed λ/2 (∼140 GHz) apart in the horizontal and vertical directions. The 4×2-element phased-array chip with attached quartz superstrate is wirebonded to a printed circuit board containing IF and LO ports, and scans to ±30° in the elevation plane (*E*-plane). The measured array peak electronic gain is 21 dB with an RF 3-dB bandwidth of 136-147 GHz and an IF bandwidth of 3-4 GHz. The measured array peak effective isotropic radiated power (EIRP) is 30-32 dBm at 134-142 GHz. To evaluate the over-the-air (OTA) performance, a communication link is demonstrated with quadrature phase-shift keying (QPSK), 16-quadrature amplitude modulation (QAM) and 64-QAM waveforms, supporting up to 16-18 Gb/s data rates. To the best of our knowledge, this paper presents the first CMOS wafer-scale phased-array transmitter at 140 GHz with high EIRP and data rate.

Chapter 4 presents fully integrated power amplifiers with eight-way low-loss power combining for D-band applications in the GlobalFoundries CMOS 45RFSOI process. The eight-way power combining (four-way differential) common source (C.S.) and cascode amplifiers are implemented using four-stage differential power amplifier (PA) unit cells as building blocks. The last stage of the cascode PA unit cell is with two devices stacking structure. The eight-way power combining network is composed of a 4-way balun-short transmission line (balun-STL) combiner and a conventional quarter wavelength transmission line (QWL TL) based combiner. The simulated two-stage eight way combiner in-situ (loaded) ohmic loss is only 1.1-1.4 dB at 130-150 GHz. The eight-way power-combining C.S. amplifier has a small-signal gain of 24 dB at 140 GHz with a 1.2 V supply and a 3-dB bandwidth of 131-150 GHz. The saturated output power (Psat) and output 1-dB compression point (OP_{1dB}) are 16.8-17.5 dBm and 13-14.2 dBm at 130-150 GHz, respectively. The corresponding peak power-added efficiency (PAE) is 11.7-14.2%. The eight-way power combining cascode amplifier achieves a small-signal gain of 24.8 dB at 135 GHz with a 3-dB bandwidth of 133-148 GHz.The Psat is 16.3-19 dBm at 125-150 GHz with a peak PAE of 6.5-12.1%. To our knowledge, compared to the prior art, these PAs achieve the highest Psat and figure-of-merit (FoM) at D-band in CMOS.

Chapter 5 concludes the dissertation and discusses future work.

Chapter 2

An Eight-Element 140-GHz Wafer-Scale IF Beamforming Phased-Array Receiver with 64-QAM Operation in CMOS RFSOI

2.1 Introduction

Recent advancements in the beyond fifth generation (5G) and $>$ 100 GHz millimeter-wave systems have enabled ultra-high data rate short-range communication [14–28]. Systems at these frequencies are good candidates to meet the increasing requirement of data consumption, since wide unlicensed frequency bands can be used with less interference. Also, they increase the channel capacity according to Shannon-Hartley theorem [4]. To overcome the increased path loss of millimeter-wave signals, especially at $>$ 100 GHz, phased-array systems are desired on both transmit and receive units to efficiently increase the equivalent isotropic radiated power (EIRP) and antenna gain [9, 29–34]. They can also be used to maintain the link margin over a wide angular region due to their electronic scanning capabilities.

In order to build a large-scale phased-array at 140 GHz, a practical beamforming archi-

tecture is desirable. The conventional all-RF beamforming architecture is widely used at 6-100 GHz [5–8]. However, at 140 GHz, it suffers from high phase shifter loss and noise figure. Also, to calibrate the gain difference among elements, RF gain control blocks with low phase variation are required, which are hard to implement at 140 GHz due to the parasitic capacitive effects. Digital beamforming architecture is not practical due to much higher power consumption, which mostly comes from the I/Q quadrature LO paths to drive the mixers and analog-to-digital converters (ADCs) with high sampling rate and bandwidth. The high-IF beamforming architecture shown in Fig. 2.1 is introduced at 140 GHz for low single sideband (SSB) noise figure and power consumption. An IF beamformer (phase and amplitude control) at 10-20 GHz is easier to implement with lower power consumption and better NF and RMS errors than an RF beamformer. Compared to the digital beamforming and LO beamforming, which are power hungry, both IF and RF beamforming architectures are possible. In this work, the high-IF beamforming architecture is chosen as a promising solution for 140 GHz phased-arrays.

There are successful demonstrations of chips assembled on a printed circuit board (PCB) with PCB-based antennas up to W-band [8, 35]. However, the chip to board transition at 140 GHz is lossy at 140 GHz and may not be suitable for arrays. Previous works have demonstrated a glass interposer technology at D-band for the assembly and packaging [14, 29], but with relatively high cost. The wafer-scale phased-array approach, which has been demonstrated in [9–11], is used here at 140 GHz as an alternative solution. High-efficiency on-chip quartz superstrate antennas greatly reduce the transition loss from the chip to antenna array.

This chapter presents an 8-element 140-GHz phased-array receiver based on the IF beamforming receive channel reported in [36]. Section 2.2 presents the wafer-scale phased-array receiver chipset architecture and block diagram. Section 2.3 presents the high-efficiency on-chip patch antenna. Section 2.4 focuses on the ultra low-noise RF front-end design and detailed analysis, and Section 2.5 elaborates other key circuit blocks design. The phased-array system analysis and measurements are demonstrated in Section 2.6 and 2.7. Section 2.8 concludes this

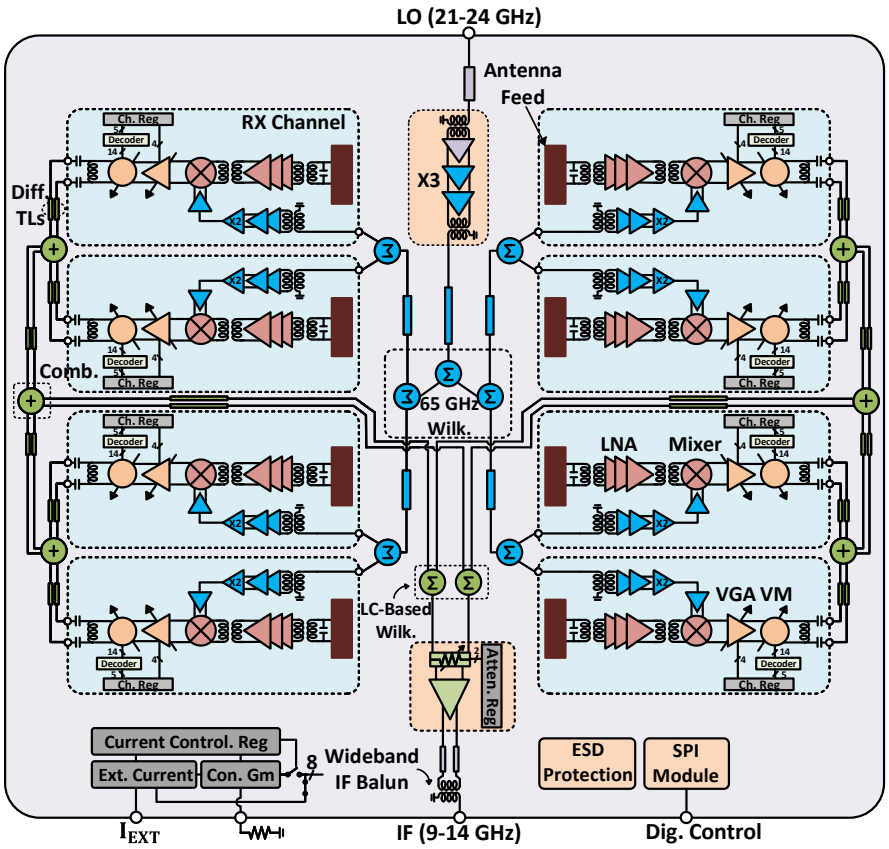


Figure 2.1: Block diagram of 8-element wafer-scale IF beamforming phased array receiver chip at 140 GHz.

chapter.

2.2 Wafer-Scale Phased-Array Receiver Architecture Using IF Beamforming

Fig. 2.1 presents the 140-GHz wafer-scale phased-array receiver chip. The array is composed of 8-element IF beamforming receive channels with 5-bit phase and 4-bit gain control, wideband active and LC-based Wilkinson IF combiners, a digital step attenuator and amplifier for variable linearity and a multiplier chain and distribution networks in the LO path to allow for an LO input frequency of 21-24 GHz. For lower LO distribution network loss, the input LO signal

first passes by a tripler ($\times 3$) to 63-72 GHz and is then distributed using Wilkinson power dividers to the 8 mixer blocks, each containing an LO doubler. On-chip EM-coupled antenna feeds are placed $\lambda/2$ (1.1 mm) apart at both vertical and horizontal directions for a 4×2 antenna array.

The mixer downconverts the 139-155-GHz RF signal after a low noise amplifier (LNA) to a 9-14 GHz IF signal using a 21-24-GHz ($\times 6$) LO. The image band is at 120-130-GHz and with high rejection due to the antenna response and the LNA tuned response. This lowers the noise contribution from the image band and reduces the receiver NF.

The chip is designed in the GlobalFoundries 45RFSOI process. The floating-body thin-oxide RF 40-nm CMOS-SOI transistor is used for RF/LO/IF circuits design and with associated f_t and f_{max} of 193 and 297 GHz (modeled to the top metal) at bias current density J_{DC} of 0.17 mA/μm.

2.3 High-Efficiency On-Chip Differential Patch Antenna On Quartz Superstrate

The patch antenna structure is similar to [9] and [11] and is fabricated on a 100-μm-thick quartz superstrate using 200-nm-thick gold layer. The diced quartz with the antenna array is then attached to the chip. Fig. 2.2(a) presents the detailed antenna structure and on-chip electromagnetic (EM) coupled feed stackup. The antenna couples to the LNA using a differential microstrip matching network with the UA layer being the ground plane 10.7-μm away from the antenna feed layer. In order to meet the metal minimum density requirement, the second and third metal layers (OA/OB) are filled with small square-shaped structures right underneath the array feeds. A differential 50-Ω (instead of 100-Ω) impedance is chosen as the interface impedance between the antenna and the LNA, since both the patch antenna and the first LNA stage have a small impedance real part at 140 GHz. Fig. 2.2(b), (c) and (d) present the antenna unit cell dimension and single-ended impedance transformation representations. The portion

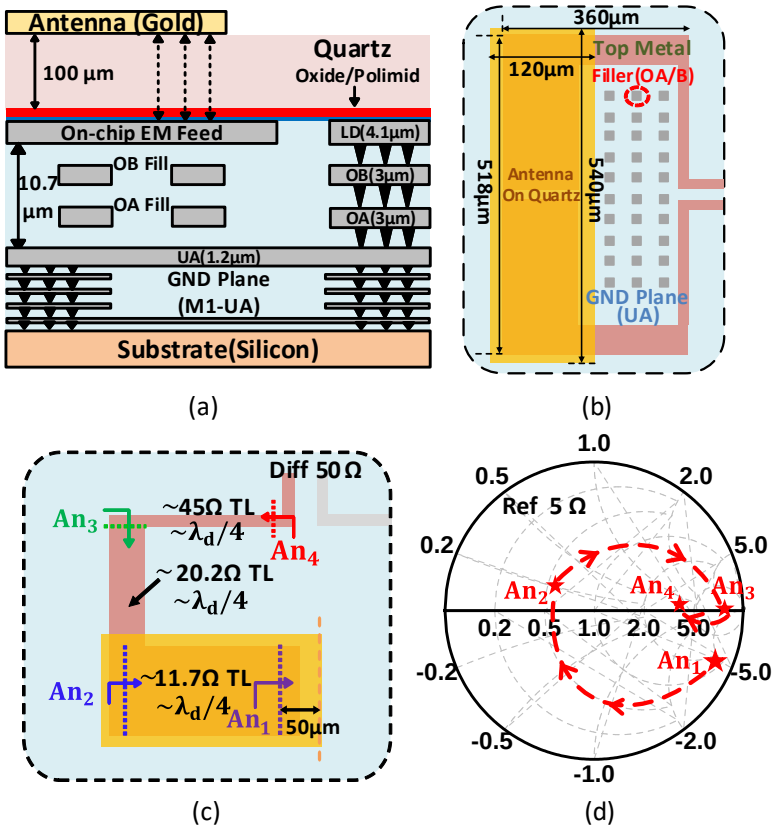


Figure 2.2: (a) On-chip EM-coupled feed stackup and antenna structure. (b) High-efficiency EM-coupled differential patch antenna unit cell. Single-ended representation of the (c) impedance transformation network and (d) that in smith chart.

between reference planes An_1 and An_2 is both a coupler from the top metal to the antenna and an impedance transformer at the same time. Another $\lambda_d/4$ low impedance transmission line is used between An_2 and An_3 for the impedance transformation in an area-efficient way, where λ_d is the wavelength in the dielectric.

The antenna E-plane is along its length (long side) and a 10-μm air gap is assumed between the quartz and the chip in simulation based on the previous experience on quartz assembly in [11]. Periodic boundary conditions are used to simulate the antenna performance in an infinite array. However, since the array is only composed of 4x2-elements, the simulated results might be slightly different from the finite array case. For the scanning performance, only the E-plane scan

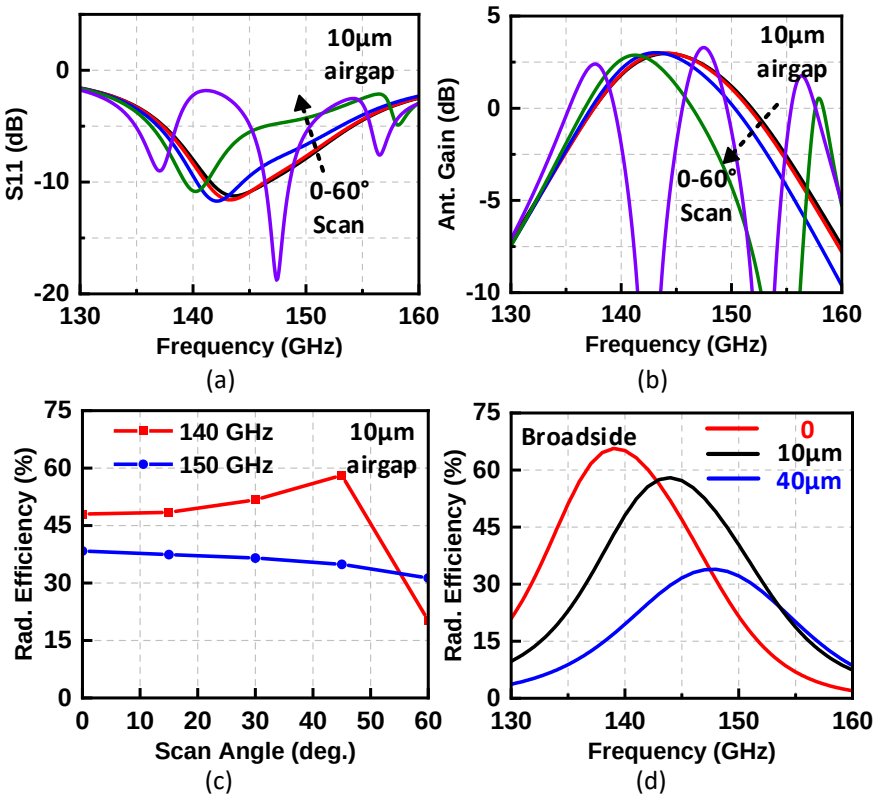


Figure 2.3: Simulated quartz superstrate antenna (a) impedance matching and (b) antenna gain with different scan angles in the *E*-plane. (c) Simulated antenna radiation efficiency versus scan angle at 140 and 150 GHz. (d) Effect of the air gap between the quartz and the chip (design is optimized for a 10-μm airgap).

performance is shown, due to the limited number of elements on the *H*-plane. The simulated antenna -7-dB S_{11} and 3-dB gain bandwidths are 140-153 and 137-152 GHz, respectively, up to 40° scan [Fig. 2.3(a) and (b)]. The maximum antenna radiation efficiency and gain are simulated to be 58% (2.4 dB loss) and 3 dB, respectively, at 144 GHz. There is virtually no loss in the quartz layer due to its very low tanδ (0.0001) even at 140 GHz. The antenna loss is dominated by the metal (ohmic) loss and the feed impedance transition network. Scan blindness is observed at around 155 GHz when the scan angle is 50-60° due to the impact of the TM0 surface wave for a 100-μm thick quartz substrate [37] [Fig. 2.3(c)]. The air gap effect is also simulated and presented in Fig. 2.3(d). A 40-μm air gap, possibly resulting from the manual quartz assembly,

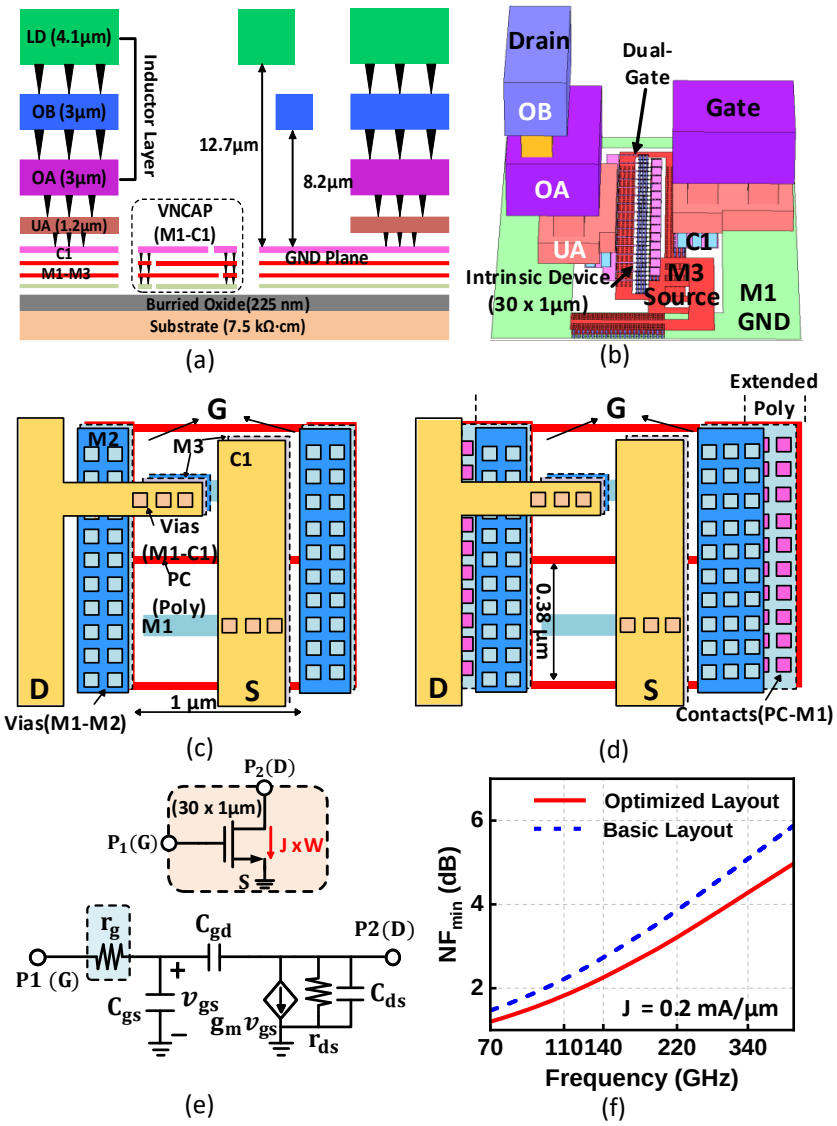


Figure 2.4: (a) Layer stackup in GF 45RFSOI showing custom VNCAP and cross section for the transmission lines and inductors. Single transistor (b) layout 3-D view, detailed interconnects view of (c) the basic double gate contact, (d) the optimized double gate contact with extended poly/poly-M1 contacts and (e) small-signal model. (f) Simulated NF_{min} of the transistor with two different layouts.

degrades the coupling efficiency from the feed line to the antenna by an extra 2.3 dB compared to the 10-μm case. The center frequency also increases with the air gap due to lower effective dielectric constant of the quartz and airgap combination.

2.4 Ultra Low-Noise RF Front-End Design

2.4.1 Device Optimization

Previous work, like [38], has reported low noise performance in W-band in GF45RFSOI process, which has several advantages on low-noise design due to its three ultra-thick metals (LD, OB and OA) and high resistive substrate [see Fig. 2.4(a)], which are ideal for low-loss matching inductor and transformer design. Another advantage is that the density and quantity of the poly-M1 contacts, which are the most lossy part of the transistor gate interconnects, is flexible and not restricted by the design rule check (DRC). Some previous works, like [39] and [40], has reported multiple transistor layouts and interconnections. In addition to using multi-finger device [see Fig. 2.4(b)] and double-gate contact configurations, an extension on the poly and poly-M1 contacts is employed to help reduce the transistor parasitic gate resistance r_g [see Fig. 2.4(c) and (d)]. Based on the small signal model in Fig. 2.4(e), the r_g of the two different layouts shown in Fig. 2.4(c) and (d) is obtained from:

$$r_g \cong \frac{Re(Y_{11})}{(Im(Y_{11}))^2} \tag{2.1}$$

where Y_{11} can be simulated and also calculated from the simplified small signal model in Fig. 4(e) as:

$$Y_{11} = \frac{j\omega(C_{gs}+C_{gd})}{1+j\omega r_g(C_{gs}+C_{gd})} \tag{2.2}$$

The r_g in the optimized layout [Fig. 2.4(d)] of a 30 x 1μm transistor (30 fingers with 1μm finger width) is simulated to be 3.3 Ω, which is almost 2 Ω lower than that of the basic layout [Fig. 2.4(c)]. Therefore, the simulated f_{max} is 320 GHz (increased by 45 GHz) and the simulated NF_{min} is as low as 2.3 dB (decreased by 0.5-0.6 dB) at 140 GHz when the transistor is biased at current density J_{DC} of 0.2 mA/μm due to the input referred r_g noise reduction [see Fig. 2.4(f)].

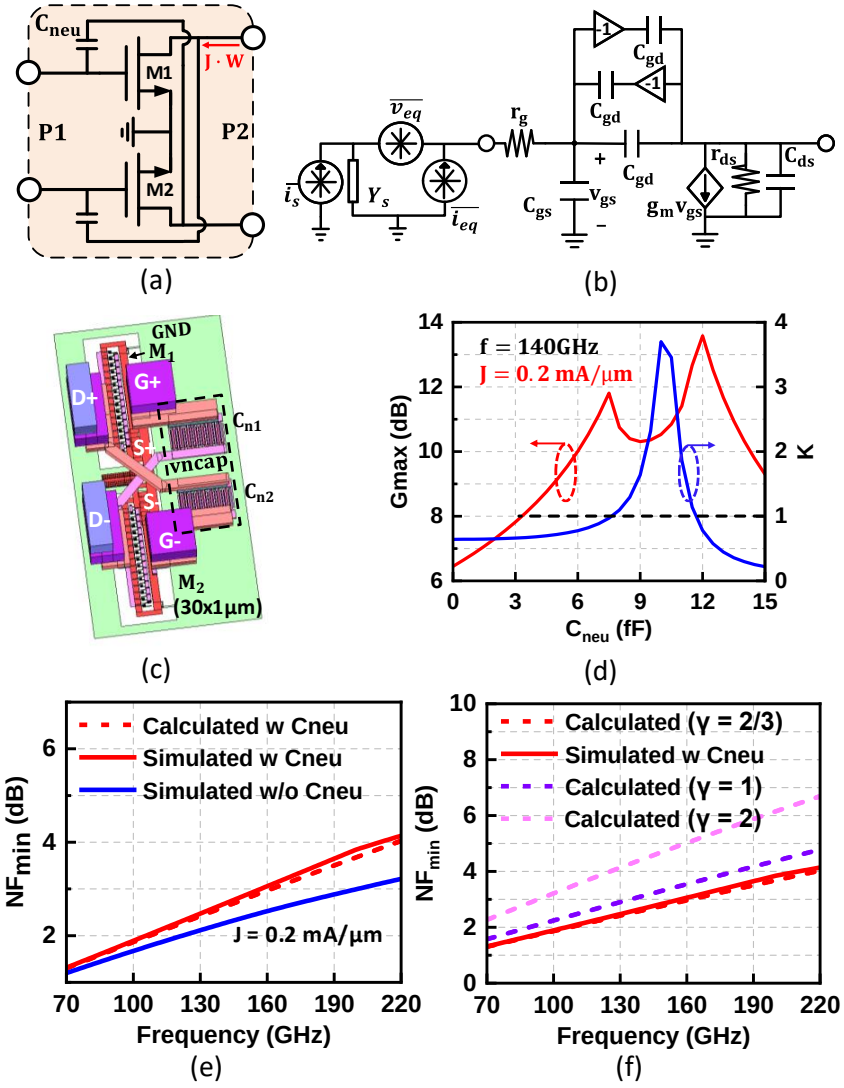


Figure 2.5: Neutralized differential transistor pair: (a) schematic, (b) half circuit small-signal noise model, (c) layout 3-D view and (d) simulated MAG (Gmax), K factor versus the value of C_{neu}, (e) simulated NF_{min} with and w/o C_{neu} and calculated NF_{min} with C_{neu} based on the noise analysis in (2.15), (f) calculated NF_{min} with different γ.

2.4.2 Capacitive Neutralization Technique

Capacitive neutralization technique has been widely adopted in mmWave amplifiers to stabilize the differential transistor pair (DP) and boost its maximum available gain (MAG) [Fig. 2.5(a)] [16], [24], [41,42]. Fig. 2.5(b) presents the equivalent half circuit small signal-model of

the neutralized differential transistor pair (NDP) [43]. A compact NDP layout is achieved using vertical natural capacitors (VNCAP) and metal fingers in a dense and stacked fashion with only M3 and C1 layers for a larger area and low capacitance variation [Fig. 2.5(c)]. The Q factor of a 2-layer VNCAP is also larger than a 3 or 4-layer VNCAP if they have similar capacitance due to its lower vias loss. To choose neutralization capacitors (C_{neu}) with reasonable capacitance value, the NDP's K factor and MAG are two key factors to consider. The K factor is derived using the Y-parameters as [44]:

$$K = \frac{2Re\left(Y_{11}\right)Re\left(Y_{22}\right) - Re\left(Y_{12}Y_{21}\right)}{\left|Y_{12}Y_{21}\right|} \tag{2.3}$$

where port 1 and 2 are the differential gate and drain ports, as shown in Fig. 2.5(a). Based on the model parameters in Fig. 2.5(b), the K factor is:

$$K \cong \frac{2\omega r_g C_T\left(\frac{C_T}{r_{ds}} + g_m C_D\right)}{\sqrt{\left(\omega^2\left({C_D}^2 + 2g_m C_D r_g C_T\right)^2 + {g_m}^2 {C_D}^2\right)}} \tag{2.4}$$

where C_T and C_D are given by:

$$C_T = \left(C_{gs} + C_{gd} + C_{neu}\right);\ C_D = \left(C_{gd} - C_{neu}\right) \tag{2.5}$$

When the value of C_D drops, which means the value of C_{neu} increases, the K factor becomes larger and surges at the point when the denominator in (2.4) is 0. Under this condition, C_{neu} is equal to C_{gd}. If C_{neu} keeps increasing, in addition to an increasing denominator, the numerator decreases due to the negative $g_m C_D$ term. Therefore, the K factor drops when C_{neu} is oversized. The NDP's MAG boosting from the neutralization is also critical for mmWave amplifier design.

The unconditional stable NDP's MAG is given by:

$$MAG = \frac{Y_{21}}{Y_{12}\left(K+\sqrt{K^2-1}\right)} \ (K > 1) \tag{2.6}$$

$$|MAG| \cong \frac{\sqrt{g_m+(\omega C_D)^2}}{|\omega C_D|\left(K+\sqrt{K^2-1}\right)} \tag{2.7}$$

Similar to the K factor, MAG becomes larger with increasing values of C_{neu}. However, the peak of the K factor degrades the MAG performance since the K factor term in the denominator of (4.1) increases. The simulated MAG and K factor curves show the predictable trends [see Fig. 2.5(d)], and 10 fF neutralization capacitors are used in the NDP stage to realize a K factor of 3.7 and MAG of 10.5 dB at 140 GHz, respectively. Their capacitance is almost equal to the simulated intrinsic transistor C_{gd} capacitance (10.1 fF) .

2.4.3 Equivalent Noise Model

Fig. 2.5(b) also presents the NDP's equivalent half circuit two-port noise model [45]. The noise figure is derived as:

$$F = \frac{\left(\overline{i_s}+\overline{i_{eq}}+Y_s\overline{v_{eq}}\right)*\left(\overline{i_s^*}+\overline{i_{eq}^*}+Y_s^*\overline{v_{eq}^*}\right)}{\overline{i_s^2}} = 1+\frac{\overline{i_{eq-u}^2}+(Y_s+Y_c)^2\overline{v_{eq}^2}}{\overline{i_s^2}} \tag{2.8}$$

where $\overline{i_{eq-u}}$ is the noise current uncorrelated with the noise voltage $\overline{v_{eq}}$, and Y_c is the correlation admittance. The relations are presented as:

$$\overline{i_{eq}} = Y_c*\overline{v_{eq}}+\overline{i_{eq-u}}; Y_c = \frac{\overline{v_{eq}^*}*\overline{i_{eq}}}{\overline{v_{eq}^2}} = G_c+jB_c \tag{2.9}$$

The NF_{min} is then calculated as:

$$F_{min} = 1 + 2R_n(\sqrt{\frac{G_u}{R_n} + {G_c}^2} + G_c) \tag{2.10}$$

$$R_n = \frac{\overline{v_{eq}^2}}{4kT}; G_u = \frac{\overline{i_{eq-u}^2}}{4kT} \tag{2.11}$$

Under the condition that C_{neu} is equal to C_{gd} and based on the NDP's small-signal model parameters [Fig. 2.5(b)], Y_c, R_n and G_u are calculated as:

$$G_c \cong \frac{\omega}{\omega_T \beta}(g_m \omega\, r_g C_T); B_c \cong \frac{\omega C_T}{\beta}; \beta = 1 + \frac{g_m r_g}{\gamma} \tag{2.12}$$

$$R_n \cong \frac{\gamma\beta}{g_m}; G_u \cong r_g \left(\left(\frac{C_T \omega}{\beta} \right)^2 + \left(\frac{\omega^2 g_m r_g C_T}{\omega_T \beta} \right)^2 \right) \tag{2.13}$$

Note that ω_T here is not a constant value versus C_{neu}, and decreases when C_{neu} increases, and is derived as:

$$\omega_T = \frac{g_m}{\sqrt{C_T^2 - C_D^2}} = \frac{g_m}{C_T} \quad (C_{neu} = C_{gd}) \tag{2.14}$$

The F_{min} can be written as:

$$F_{min} \cong 1 + 2\left(\frac{\omega}{\omega_T}\right)\left(\gamma r_g \omega C_T + \sqrt{\frac{\gamma r_g g_m \left(1 + (r_g \omega C_T)^2\right)}{\beta} + (\gamma r_g \omega C_T)^2} \right) \tag{2.15}$$

Fig. 2.5(e) presents the NDP's simulated and calculated NF_{min} using (2.15), given that the estimated γ and the simulated r_g, g_m and C_T are $\frac{2}{3}$, 3.3 Ω, 34.5 mS and 44 fF, respectively. Compared to the NF_{min} of a differential pair (DP) without neutralization, the NDP NF_{min} is 0.5 dB higher at 140 GHz at a current density of 0.2 mA/μm mainly due to its smaller ω_T, larger C_T and the cancelled C_D related term in the denominators of G_c and G_u (details are presented in Appendix I). γ is the excess noise factor. The NDP calculated NF_{min} for different γ is presented

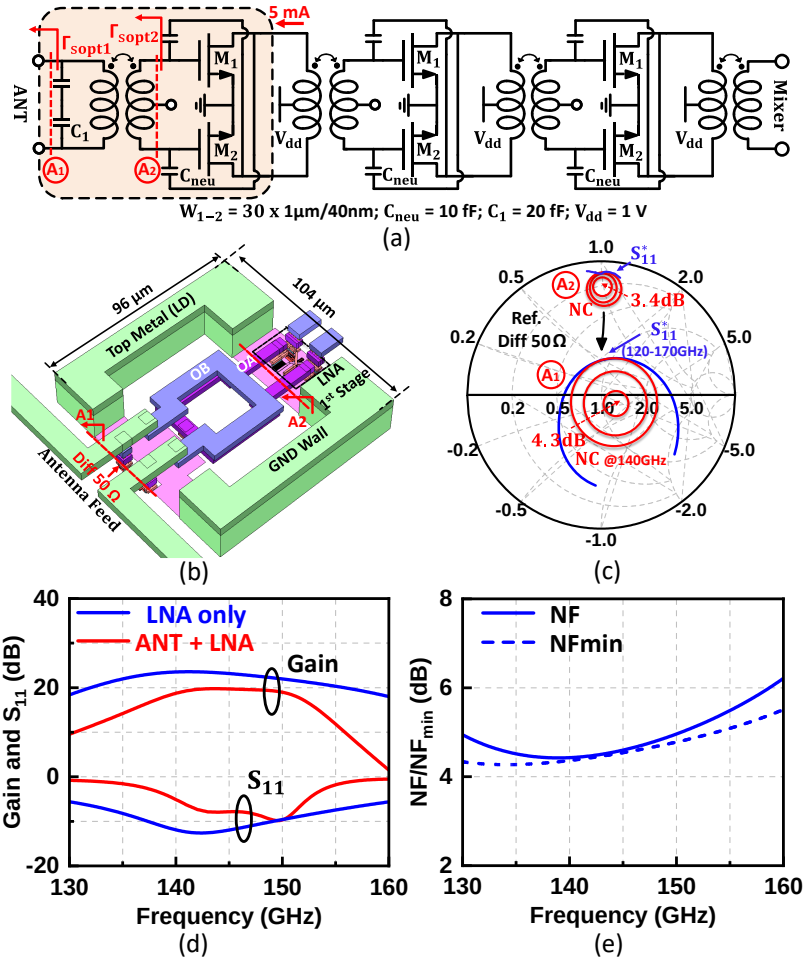


Figure 2.6: (a) Schematic of the 3-stage fully differential transformer coupled LNA. (b) 3-D layout of the interface transformer between the antenna feed and the LNA 1st stage. (c) Noise circles and S_{11}^* of the LNA with and w/o input transformer matching network. (d) Simulated LNA and LNA with antenna gain and input matching. (e) Simulated LNA NF and NF_{min}.

in Fig. 2.5(f). Even though the NDP is slightly noisier than the DP, it still results in better LNA performance since the DP is not unconditionally stable and has low intrinsic MAG (4 dB lower than the NDP) and extra matching loss. Also note that the NDP has a lower NF than a cascode differential pair and consumes less power. Therefore, the neutralization technique is useful for LNA design at 140 GHz, especially in CMOS technology with limited f_t/f_{max}.

2.4.4 LNA

The 3-stage differential transformer-coupled LNA is designed using the capacitive neutralization technique [Fig. 2.6(a)]. The input matching between the antenna feed and LNA 1^{st} stage is realized by a compact and low loss transformer [Fig. 2.6(b)]. In order to achieve the minimum noise figure, the NDP's optimal source admittance $Y_{s,opt}$ is required to be close to the conjugate of the input admittance Y_{in}^*, which are given by:

$$\begin{aligned} Y_{s,opt} &= G_{s,opt} + jB_{s,opt}; B_{s,opt} = -\frac{\omega C_T}{\beta} \\ G_{s,opt} &\cong \left(\frac{\omega C_T}{\gamma\beta}\right)\sqrt{\frac{\gamma r_g g_m}{\beta} + (\gamma r_g \omega C_T)^2} \end{aligned} \tag{2.16}$$

$$Y_{in}^* = {Y_{11}}^* \cong \omega^2 r_g C_T^2 - j\omega C_T \quad (Y_{12} \cong 0) \tag{2.17}$$

The ratio $\frac{G_{s,opt}}{{G_{11}}^*}$ is then calculated as:

$$\frac{G_{s,opt}}{G_{11}^*} \cong \frac{1}{\beta}\sqrt{1 + \frac{g_m}{\gamma r_g C_T^2 \beta \omega^2}} \tag{2.18}$$

Due to the high frequency operation at 140 GHz, the ratio $G_{s,opt}/G_{11}^*$ drops to 1-2, which means the NDP $Y_{s,opt}$ is already close to its input admittance conjugate Y_{in}^*. No additional technique, such as source degeneration, is necessary. Fig. 2.6(c) presents the LNA noise circles and S_{11}^* with and without the input transformer. The LNA NF_{min} degrades from 3.4 dB to 4.3 dB due to the transformer loss. The simulated gain and input matching of the LNA and LNA with antenna are shown in Fig. 2.6(d), respectively. When the antenna loss and the mismatch between antenna and LNA are included in the simulations, the maximum gain with the antenna degrades from 23 dB to 20 dB with a 3-dB bandwidth of 137.5-152.5 GHz. The LNA NF is simulated to be 4.4-6.2 dB at 130-160 GHz, and does not include the antenna loss [Fig. 2.6(e)].

The measured LNA test chip with input and output baluns for probing are presented in

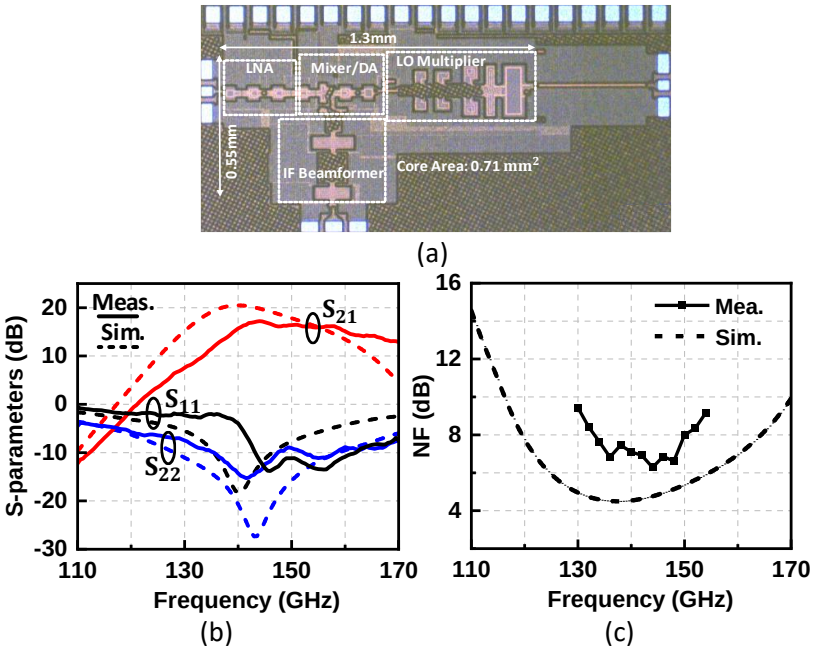


Figure 2.7: (a) Single-channel receiver die photo. (b) LNA (test chip with input/output balun for probing) simulated and measured S-parameters. (c) Measured NF for the single-channel receiver

Fig. 2.7(a). The LNA has 17.2 dB peak gain with a 3-dB bandwidth of 138-163 GHz. The single receive channel NF (comprising of an LNA, mixer, and the IF beamformer), which is mainly dependent on the LNA NF, is measured using the hot/cold Y-parameter method and a D-band ELVA noise source. The measurement setup and results are reported in [36]. The single sideband (SSB) NF is measured to be 6.4-7.5 dB at 134-149 GHz with an average of 7 dB [Fig. 2.7(b)].

2.4.5 Mixer

The mixer utilizes the active double-balanced architecture for large conversion gain and better NF [see Fig. 2.8(a)]. The neutralization technique is also employed to stabilize the g_m stage and improve the isolation between the LNA and mixer switching quad. In order to suppress the noise from the switching quad when the mixer is current steered, series inductors (L_{cas}) are placed between the g_m stage and switching quad. The impedance seen from Z_x, as shown in Fig.

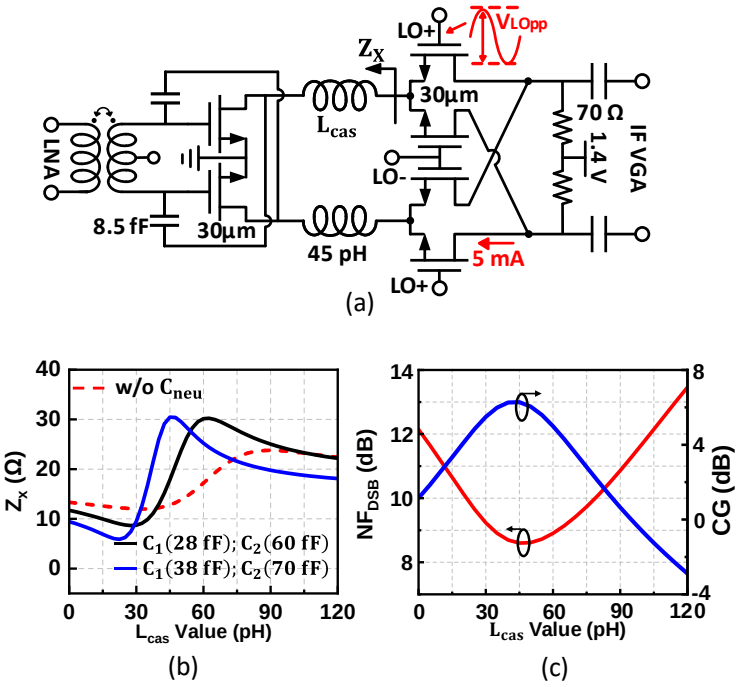


Figure 2.8: (a) Mixer schematic. (b) Calculated Z_x shown in (a) with and w/o C_{neu} with different L_{cas} values based on (2.19). (c) Simulated mixer NF_{DSB} and conversion gain with different L_{cas} values.

2.8(a), is:

$$Z_x = \frac{1}{sC_1} \parallel \left(sL_{cas} + \frac{1}{sC_2 + g_{ds}} \right) = \frac{\left(1 - \omega^2 L_{cas} C_2\right) + sL_{cas} g_{ds}}{s\left(C_1 + C_2 - \omega^2 L_{cas} C_1 C_2\right) + g_{ds}\left(1 - \omega^2 L_{cas} C_1\right)} \tag{2.19}$$

where g_{ds} is $\frac{1}{r_{ds}}$ (g_m stage), C_1 is the parasitic capacitance seen into the switching quad source, and C_2 is the total capacitance seen into the g_m stage drain, which approximately equals to the summation of C_{gd}, C_{neu} and C_{ds}. Z_x can be made high enough compared to the impedance looking into the switching quad by choosing an optimal series inductor value, and thus the noise from the switching quad will not appear at the output. Fig. 2.8(c) presents the calculated Z_x versus L_{cas} at 140 GHz, with L and C components Q factors assumed to be 10 and 30, respectively. The C_{neu}, as part of the C_2, increases the effective value of C_2, and helps increase the LC resonator Q and reduce the optimal L_{cas}. The mixer conversion gain and NF_{DSB} at 140 GHz are simulated

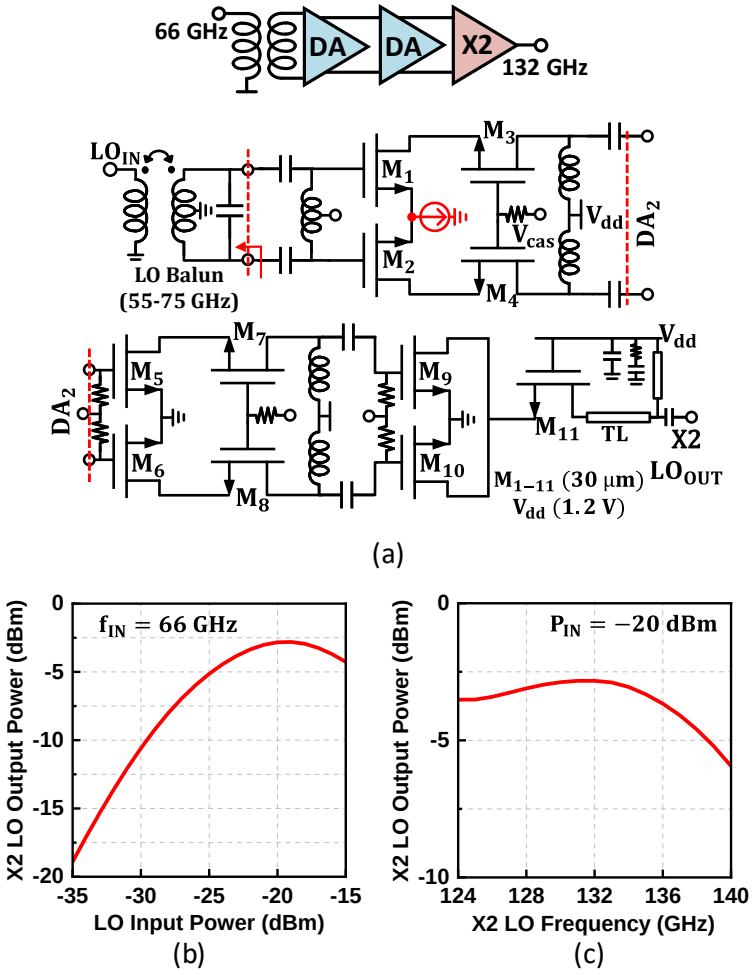


Figure 2.9: (a) Channel LO chain schematic. Simulated LO output power versus (b) input power level and (c) output LO frequency.

versus L_{cas}, and 6 dB conversion gain and 8.8 dB NF_{DSB} are obtained for L_{cas} = 45 pH [Fig. 2.8(d)]. An optimal L_{cas} helps resonate out the parasitic capacitance. In this case, the drain current from the mixer g_m stage will flow primarily into the switching quad, resulting in a peak mixer conversion gain [46]. The mixer output is a resistive load with no inductive termination for compact layout. It has a low pass-response, and the conversion gain is 5-6 dB at 0.1-15 GHz (IF) and drops to 3-4 dB at 20 GHz.

2.5 LO Chain, IF Beamformer and Combiner Design

2.5.1 Channel LO Chain

The 21-24 GHz LO (-5 dBm) first passes by an amplifier/tripler/amplifier chain and the 63-72 GHz signal is distributed using a standard Wilkinson network to local $\times 2$ amplifiers/multipliers at each mixer (Fig. 2.9). The $\times 2$ LO chain consists of a balun, two cascaded driver amplifiers and a D-band doubler. The 63-72 GHz signal level is -3 dBm on after the tripler unit and is distributed to 8 channels with a loss of 14 dB (9 dB division loss and 5 dB ohmic loss), resulting in an input power of -17 dBm for each doubler chain. Therefore, two amplifiers are needed before the doubler stage to result in enough drive power. The simulated output LO power at 124-140 GHz is $>$ -6 dBm for an input power level of -20 dBm at 62-70 GHz [Fig. 2.9(c)]. Another LO driver at 130 GHz is used before the mixer. Its transistor core topology is based on a NDP (similar to the LNA) and has a simulated gain of 6-7 dB. The output power of the LO driver is $>$ 0 dBm at 124-140 GHz and it consumes 11 mA DC current from a 1 V supply.

2.5.2 IF Beamformer and Combiner

The IF beamformer is designed at 9-14 GHz and consists of a variable gain amplifier (VGA) with 4-bit gain control and a vector modulator (VM) with 5-bit phase control. The 4-bit VGA is a single-stage cascode amplifier, and employs the current steering topology, resulting in 10-dB gain control with invariant input P1dB [Fig. 2.10(a)]. An extra feedback path is introduced using a 40 fF capacitor in parallel with the cascode common gate (CG) transistor to reduce the phase variance of different gain states. The simulated VGA maximum phase variance with and without C_{fb} for different gain states is presented in Fig. 2.10(b). The VM is based on two variable gain stages and a type I poly-phase filter (PPF) to generate I and Q vectors [47]. I and Q vectors are then selected and scaled by a 2-bit switch and 5-bit current DACs with a decoder and summed in the current domain at the output [48] [Fig. 2.10(c)]. The VGA and VM are biased at 8 mA and

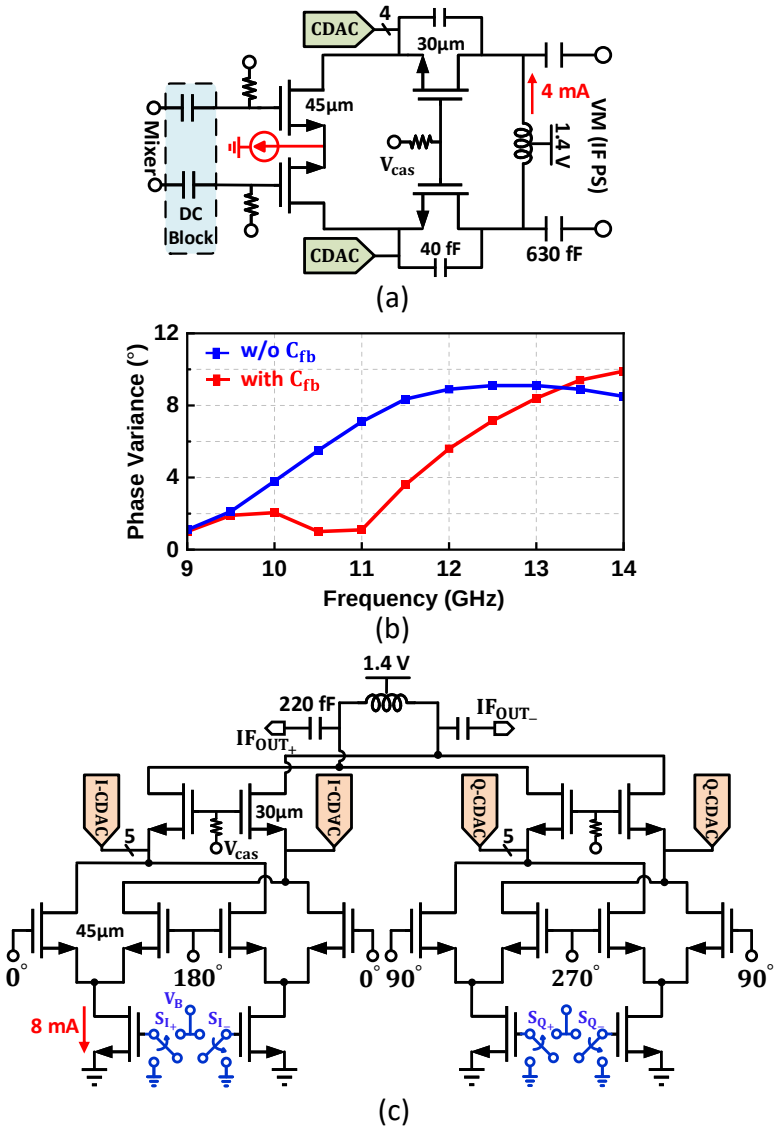


Figure 2.10: (a) Schematic of the IF 4-bit VGA. (b) Simulated VGA maximum phase variance for 10-dB gain control versus frequency. (c) Schematic of the vector modulator with 5-bit phase. control.

15 mA, respectively from a 1.4 V supply. The measured average peak gain of the IF beamformer breakout is 9.6 dB with a 3-dB bandwidth of 9.3-14.3 GHz. The input and output P_{1dB} are -11 and -2 dBm at 11 GHz, respectively. Note that a high IP1dB is required since it is after the LNA/mixer gain of 23 dB. This results in a relatively high channel IP1dB and allows for wide bandwidth signal to be received with high SNR.

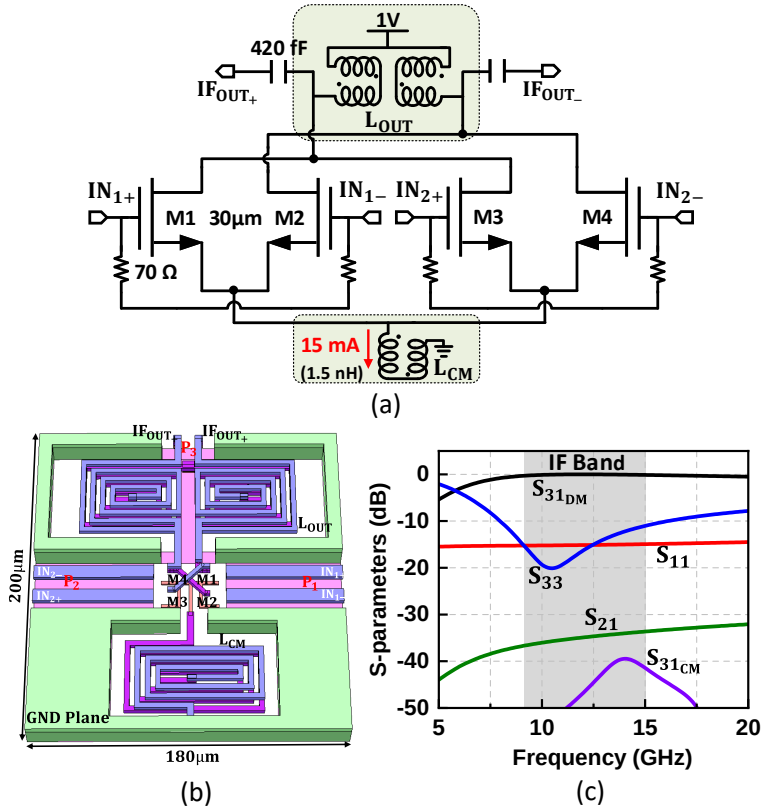
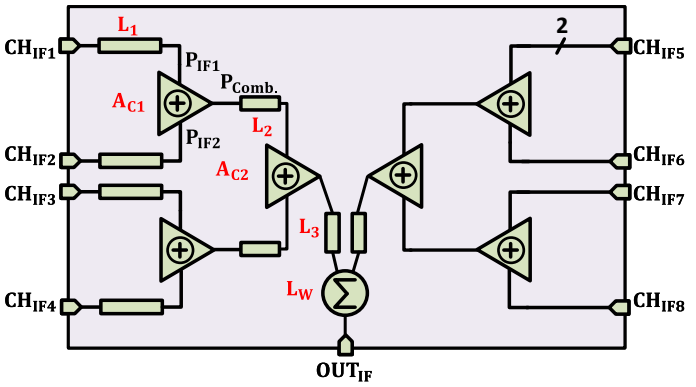


Figure 2.11: Wideband compact active IF combiner (a) schematic, (b) layout EM model and (c) simulated S-parameters.

An 8-to-1 combiner network is then implemented with a compact layout, high isolation and sufficient linearity. The first two stages are active combiners for compact size ($0.18\times0.2\text{mm}^2$), and are implemented using cascode amplifiers with merged outputs. A stacked inductor with low Q (9 at 11 GHz) is used for the output matching network to realize a wideband response. Also, L_{CM} is implemented for a higher common mode rejection ratio (CMRR). The simulated gain, defined as $Pout/Pin_{1Channel}$, is 0±0.2 dB at 9-14 GHz, due to the wideband resistive matching and low-Q load inductor. When both channels are energized, the gain, defined as $Pout/Pin_{1Channel}$ increases to 5.8-6.2 dB due to the coherent current addition at the output. However, in multi-port networks, it is best to define the gain as $Pout/Pin_{total}$, and in this case, the gain becomes 2.8-3.2 dB at 9-14 GHz. Note that a lossless Wilkinson combiner will have a gain of 0 dB under this definition. The simulated active combiner NF is 7.6 dB at 9-14 GHz. The return loss at each port



(a)

	L_1	A_{C1}	L_2	A_{C2}	L_3	L_W	Network
Gain (dB)	-1	+3.2	-1	+3.6	-1	-0.8	+3
IP1dB (dBm)	High	+1	High	+1.6	High	High	-4

(b)

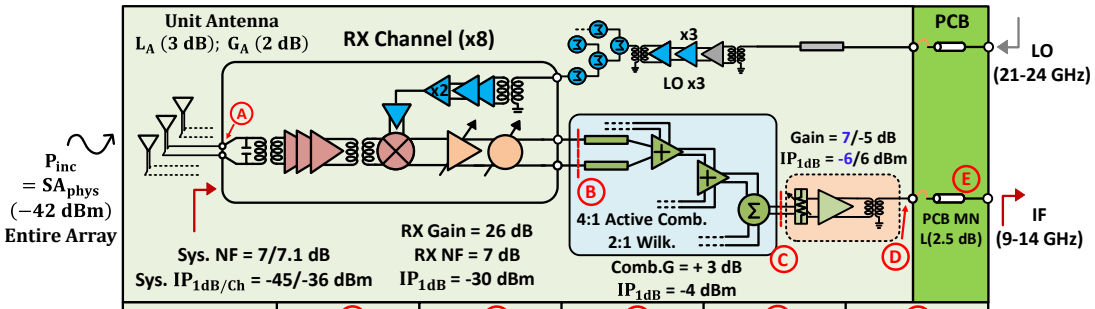
Figure 2.12: IF combiner network: (a) block diagram and (b) gain and linearity performance analysis (all ports and transmission lines are differential).

is <-10 dB with a >30-dB isolation and >40-dB CMRR [Fig. 2.11(c)]. The first and second stage active summers are biased at 14 and 20 mA from 1 V, and with a simulated OP_{1dB} of 6 and 7.2 dBm. The lumped-element Wilkinson combiner has much higher linearity, and is used in the last stage.

The differential 8-channel active/passive combiner is shown in Fig. 2.12 with a simulated gain ($Pout/Pin_{total}$) of 2.2-3 dB at 9-14 GHz. This takes into account the active combiner gain (two stages) and all the line loss connecting the different combiners. The combiner network IP1dB is limited by the second active combiner and is -4 dBm per input channel. The output P1dB is:

$$OP1dB = IP1dB_{Channel} + 10log\,(8) + Gain - 1 \tag{2.20}$$

and is 7 dBm. Based on the measured channel gain of 26 dB and $IP1dB$ of -30 dBm [**?**], the input P1dB of the phased-array channel referenced to the antenna 50-Ω port is therefore -33 dBm (including the channel and the active/passive combiner network).



	A	B	C	D	E
H. Gain Mode	$G_{RX} = -3 + 26 + 3 + 7 - 2.5 = 30.5$ dB				
Sig. P (dBm)	-54	-28	-16	-9	-11.5
N (dBm/Hz)	-167	-141	-138	-131	-133.5
N. P (dBm) BW = 1 GHz	-77	-51	-48	-41	-43.5

* $P_{/Ch} = P_{inc} - 10\log(N) - L_A$ ($N = 8$, $L_A = 3$ dB)

Figure 2.13: System-level calculation for the 8-element phased-array receiver at P_{inc} = -42 dBm.

An IF amplifier at 9-14 GHz (standard cascode with a low-Q load, I_{bias} = 10 mA) is used after the 8-channel combiner with a gain of 7 dB and an IP1dB/OP1dB of -6/0 dBm (Fig. 2.13). Knowing the OP1dB of the 8-channel combiner, it is clear that this amplifier limits the overall system linearity (Fig. 2.13). Therefore, a 2-bit passive attenuator with 0/4/8/12 dB attenuation states is used before this amplifier to increase the system IP1dB if needed at the expense of lower system electronic gain.

2.6 Phased-array System Analysis

Fig. 2.13 presents the system-level calculations for gain, noise, signal-to-noise ratio (SNR) and linearity for the 8-element phased-array receiver. Note that the channel gain measured value of 26 dB is used and not the simulated value of 30 dB.

The only two known power levels are the measured power at the IF connector (P_{IF}) and P_{inc}, which is the total incident power on the array aperture given by $P_{inc} = SA_{ph}$, where S is the incident power density from the transmit horn $S = P_T G_T/(4\pi R^2)$, P_T and G_T are the transmit power and gain of the horn antenna, R is the range, and A_{ph} is the physical area of the 4×2

antenna array given by $A_{ph} = 8A_{unit} = 8L_hL_v$, where L_h and L_v are the grid sizes on the array horizontal and vertical directions (both are 1.1 mm). The system receive electronic gain, $G_{RX_{el}}$, is defined as:

$$G_{RX_{el}} = \frac{P_{IF}}{P_{inc}} \tag{2.21}$$

and includes the antenna loss (3 dB), channel gain (26 dB), 8-channel combiner gain (3 dB), the final IF amplifier gain (7 dB), and the PCB loss (2.5 dB). This translates to a $G_{RX_{el}}$ of 30.5 dB for the phased-array. For completion, P_{inc} can also be calculated using the Friis transmission formula as:

$$P_{inc} = (P_T G_T)(SLF)(D_R) \tag{2.22}$$

where $SLF = (\lambda/4\pi R)^2$ and D_R is the directivity of the 4×2 antenna array, given by $D_R = 4\pi A_{ph}/\lambda^2$. Note that the D_R (and not the antenna gain, G_R) should be used for P_{inc} to refer the power level at the aperture (in air), since the antenna loss is already taken into the $G_{RX_{el}}$ in the gain lineup.

The system input P_{1dB} is determined by the last amplifier stage. The simulated system-level input P_{1dB} referenced to each channel input is -45 dBm/Channel in the high gain mode ($G_{RX_{el}}$ = 30.5 dB) and -36.5 dBm/Channel in the low gain mode ($G_{RX_{el}}$ = 18.5 dB) including the final attenuator/amplifier stage, and is limited by the final IF amplifier. Due to the Rx channel gain of 26 dB, the NF remains virtually the same for both the low linearity and high linearity modes. This means that it is best to operate the 8-element array at low electronic gain for high dynamic range. An external high-linearity IF amplifier (from 3.3 V) could be used if the IF signal needs to be amplified further while still keeping the same system linearity.

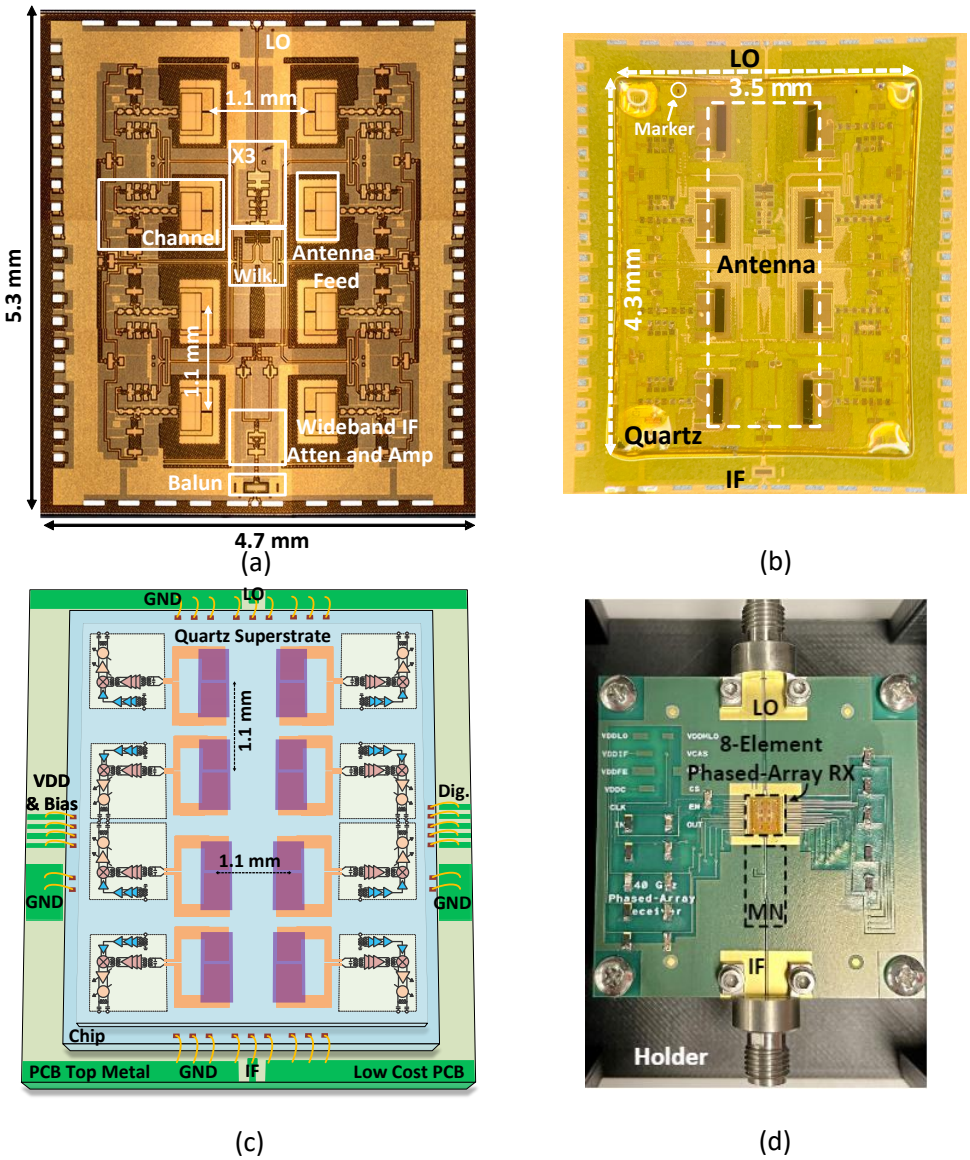


Figure 2.14: (a) 8-element phased-array receiver chip die photo. (b) Receiver chip with antenna and quartz (100 µm thickness superstrate) attached. (c) Block diagram of the 140 GHz phased array receiver system assembled on a low-cost PCB. (d) Photograph of the assembled PCB.

2.7 Phased-array Element and System Measurements

Fig. 2.14 presents the chip die photo of the 8-element wafer-scale phased-array receiver with a size of $4.7 \times 5.3\ mm^2$. The chip consumes 1.16 W and a detailed power breakdown table is presented in Table 2.1. The diced quartz wafer with the printed antennas is attached to the chip

Table 2.1: Phased-Array Receiver Power Breakdown

Total	8 Channels	LO Tripler	Combiners	Other
1.16 W	8×119 = 950 mW	50-60 mW	100 mW	50 mW

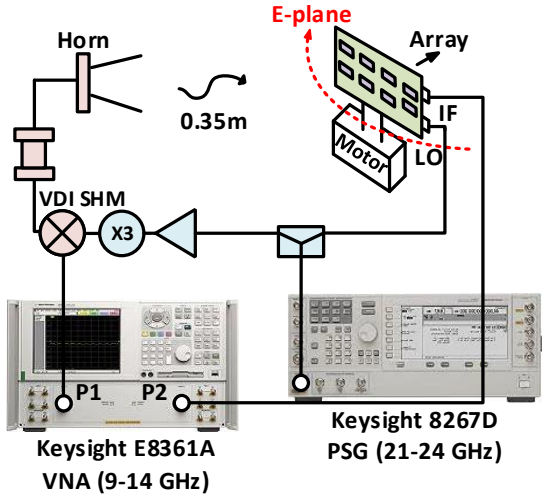
with a tiny dot of glue placed on the corners, and aligned under the microscope with the help of markers defined on the quartz superstrate. It occupies a smaller area than the chip so as not to cover the bonding pads. The chip supply, digital control and other bias pads are bonded on the PCB top metal. The LO input (21-24 GHz) and IF output (9-14 GHz) signals are bonded on the PCB, and matching networks are designed to compensate for the bonding inductance, reduce the transition loss and widen the IF bandwidth.

2.7.1 Receive Electronic Gain and Pattern

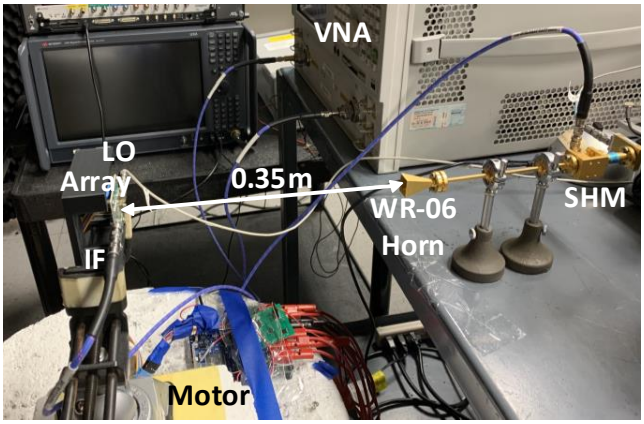
The phased-array measurements are done with a WR-6 standard gain horn antenna placed at a distance of 0.35 m [Fig. 2.15]. The far field of the 8-element array is 1 cm at 140 GHz. A Keysight 8267D PSG is used for the LO feed to the phased-array chip, and as an LO for the subharmonic mixer. After de-embedding the setup loss, a vector network analyzer (VNA) is used to measure the array and element electronic gain and phase.

First, the Rx channel breakout conversion gain with the LNA, mixer, IF stage (see Fig. 2.7(a)) was measured using GSG probes to have a conversion gain of 26-27 dB at 140 GHz and agrees reasonably well with the simulated gain of 30 dB [36].

The phased-array is then calibrated by turning on the antenna channels one by one and measuring the far-field amplitude and phase of each channel (Fig. 2.15). Since the phased-array is laid out symmetrically, there is only a maximum $\pm 12^{\circ}$ of phase variation across the array which is corrected using the IF phase shifters. Also, the gain variation was corrected using gain control in the IF VGAs. Note that the channel NF does not change versus gain control due to the high



(a)



(b)

Figure 2.15: (a) Measurement setup for the array small signal. (b) Photograph of the measurement setup.

channel gain of 26 dB.

The measured phased-array receive electronic gain, $G_{RX_{ele}}$, is 27.5 dB with a 3-dB bandwidth of 143.3-146 GHz (Fig. 2.16). The RF is swept with a fixed LO at 22.5 GHz and the IF signal is at 9-14 GHz. The phase-states are exercised for 5-bits/32-states with an RMS gain and phase errors of < 0.5 dB and $< 5^\circ$ at 9-14 GHz. The measured electronic gain compares well with a simulated Rx gain of 30.5 dB. The difference is due to a small biasing mistake in two edge channels which reduced their gain even after calibration.

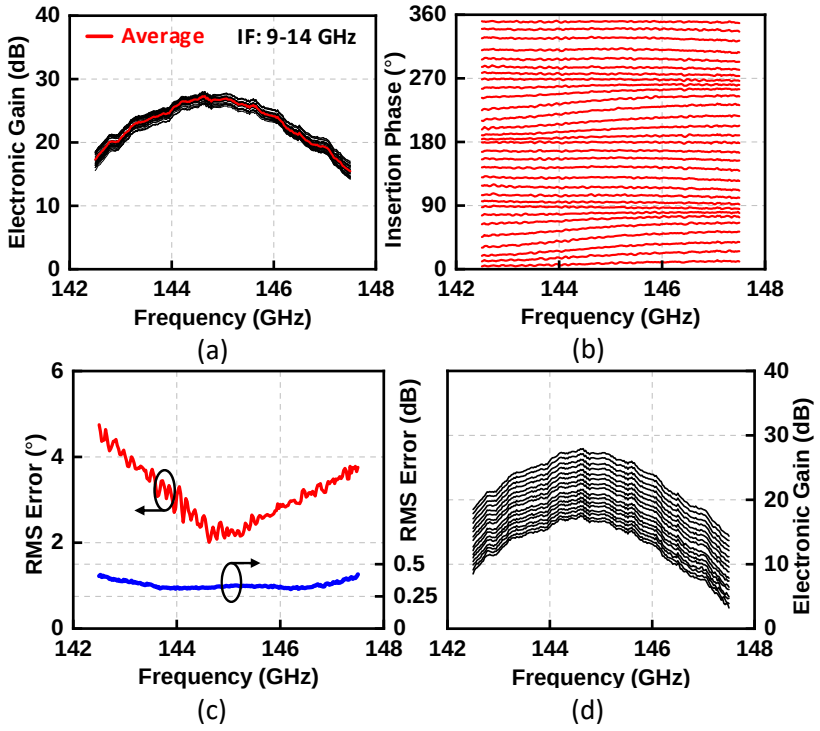


Figure 2.16: Measured 142.5-147.5 GHz element (a) phase states electronic gain, (b) phase states phase, (c) RMS errors and (d) electronic gain states tuned by 4-bit IF VGA.

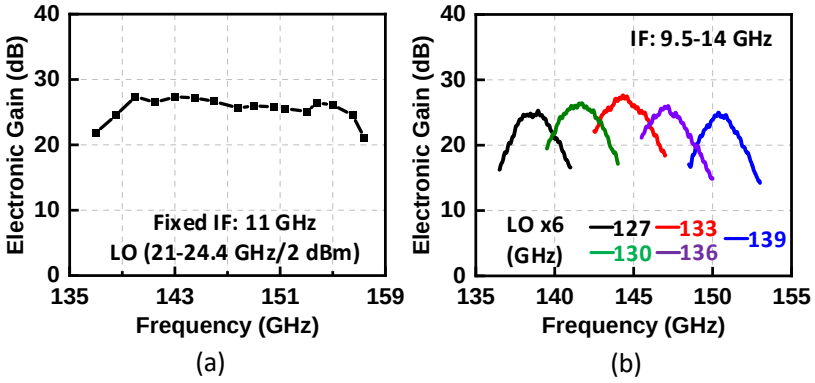


Figure 2.17: Measured array electronic gain with (a) a fixed IF frequency (11 GHz) and (b) different LO frequencies (carriers).

Fig. 2.17(a) presents the gain at broadside with a fixed IF frequency (11 GHz) and swept RF and LO frequencies. This measures the phased-array tuning range with a 3-dB bandwidth of 139-155 GHz, which is limited by the LNA and antenna gain response [see Fig. 2.6(e)]. Fig.

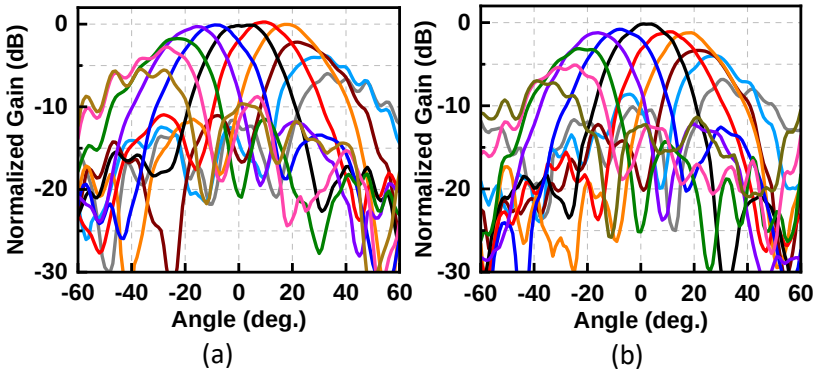


Figure 2.18: Measured E -plane beam patterns at (a) 140 GHz and (b) 150 GHz.

2.17(b) presents the measured electronic gain with different LO center frequencies. The RF input signal is swept with a frequency span of 4.5 GHz for each carrier. The measured peak electronic gain is 25-27 dB and the instantaneous 3-dB bandwidth is around 2-3 GHz for each LO. The narrower bandwidth is due to the gain response of the RF and IF chain, including the antenna response, LNA/mixer, the IF beamformer, combiner, attenuator, tuned wideband IF amplifier and PCB matching network. Note that the RF front-end bandwidth is 16 GHz, and it can be fully utilized by using different LO center frequencies of 21-24 GHz.

Fig. 2.18 presents the measured array beam patterns at 140 and 150 GHz. The 8-element phased-array is electronically scanned in the E-plane. The beam scan is $\pm 35^{\circ}$ with sidelobe levels $<$ -10 dBc. Compared to the finite array simulations at 150 GHz (presented in Appendix II), the measured gain drops quickly and is as expected. However, at 140 GHz, the gain drops after scan angle of 35° and does not agree with simulations (which predict a scan angle of 50°). The discrepancy is probably due to the underestimated TM0 mode surface-wave contribution in a small truncated thick substrate (0.09 λ_d at 140 GHz). The antenna frequency response also may have shifted down due to the fabrication and assembly errors.

There are solutions to surface waves issues. One is to use a cavity antenna, but this is hard to build at 140 GHz. Another solution is to use a 50-μm thick quartz superstrate at the expense of antenna bandwidth and a bit of efficiency reduction. Future work will employ 50-μm quartz

superstrate.

2.7.2 Channel IP_{1dB}

The linearity measurement setup is demonstrated in Fig. 2.19(a). In order to realize a high EIRP from the transmitter, an active multiplier (VDI-AMC-333) is used to drive the horn antenna. The system input P_{1dB} can be obtained based on the input and output power levels, and a power sweep to determine the 1 dB compression. The normalized receive electronic gain is shown in Fig. 2.19(b) and one can clearly see the 2-bit attenuator response. The channel IP1dB shows a 7 dB improvement (-44 dBm to -37 dBm), which is very close to the expected values [Fig. 2.19(c)].

2.7.3 Communication-links

To evaluate the phased-array over-the-air (OTA) performance, the measurement setup in Fig. 2.20(a) is used. A modulated signal from the arbitrary waveform generator (AWG) is upconverted to the RF band by a subharmonic mixer. The array downconverts the signal to the IF band, which is then demodulated by the Keysight DSO-Z series scope running the VSA9600 demodulation software with internal equalization.

Fig. 2.20(b) presents the measured array EVM_{RMS} values using 16/64-QAM 500-MBaud/s modulated signal versus P_{inc}. An α = 0.35 is used resulting in a PAPR of 6.6 and 7.7 dB for the 16-QAM and 64-QAM waveforms, respectively. The signal has a center frequency of 140 GHz and the array is at broadside in low gain mode. The system NF referenced to the antenna 50-Ω port is 7 dB, and is 10 dB when referenced to the air in front of the antenna. This results in a noise floor of -77 dBm for a 500 MHz bandwidth. This is clearly seen in the measured EVM, as it rises quickly to an EVM of 9.5% (20.5 dB SNR) for $P_{inc} = -55$ dBm on the array aperture. At P_{inc} of -47 dBm to -40 dBm, the EVM is limited by the setup and is 3-3.5%. Note that the integrated LO phase noise alone with the $\times 6$ multiplier contributes 2% to the system

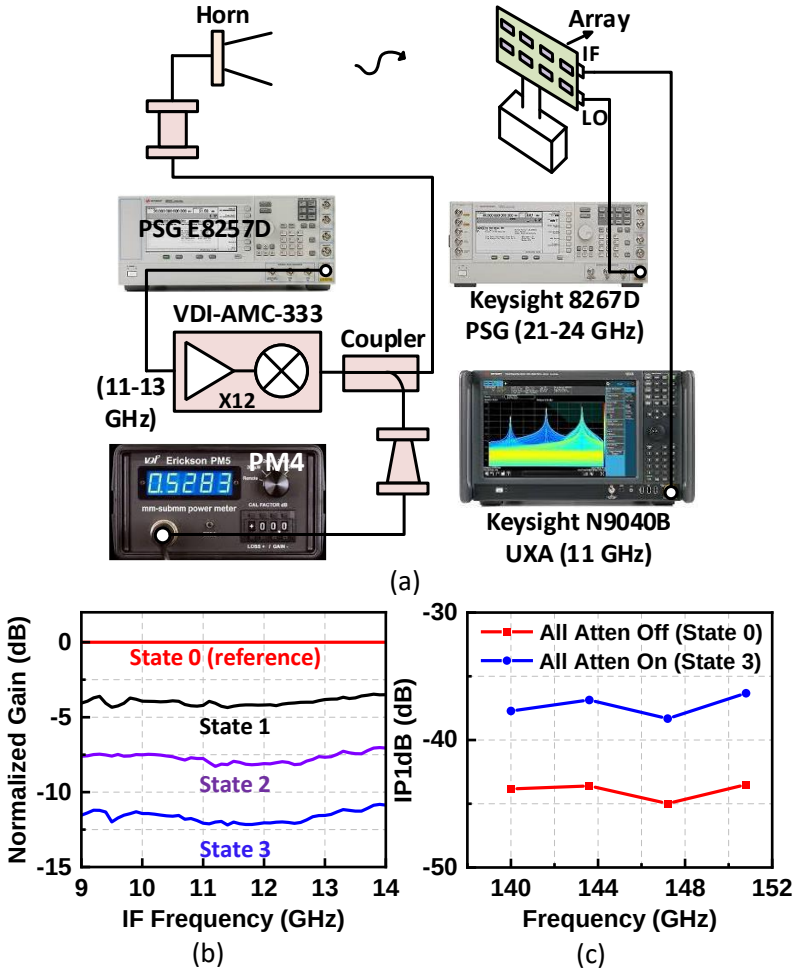


Figure 2.19: (a) Measurement setup for the array linearity. (b) Measured 2-bit IF attenuator states normalized gain. (c) Measured array input P1dB with attenuator fully on and off versus RF frequency.

EVM. At higher signal levels, the EVM is rising from the subharmonic mixer as it is approaching its output power limit. Note that the receive IP_{1dB} per channel of -37 dBm translates to -25 dBm at the aperture of the array (P_{inc} = -37 dBm +3+9), where 3 dB is the antenna loss and 9 dB is for the 8-element array.

Fig. 2.21 summarizes the measured constellations and EVM values of the array at different data rates, scan angles and center frequencies in 16 and 64-QAM for P_{inc} = -42 dBm. This power level is chosen to optimize the phased-array SNDR. At 0° scan, the measured maximum data rates are 10 Gb/s in 16-QAM and 9 Gb/s in 64-QAM. The achieved corresponding EVMs are

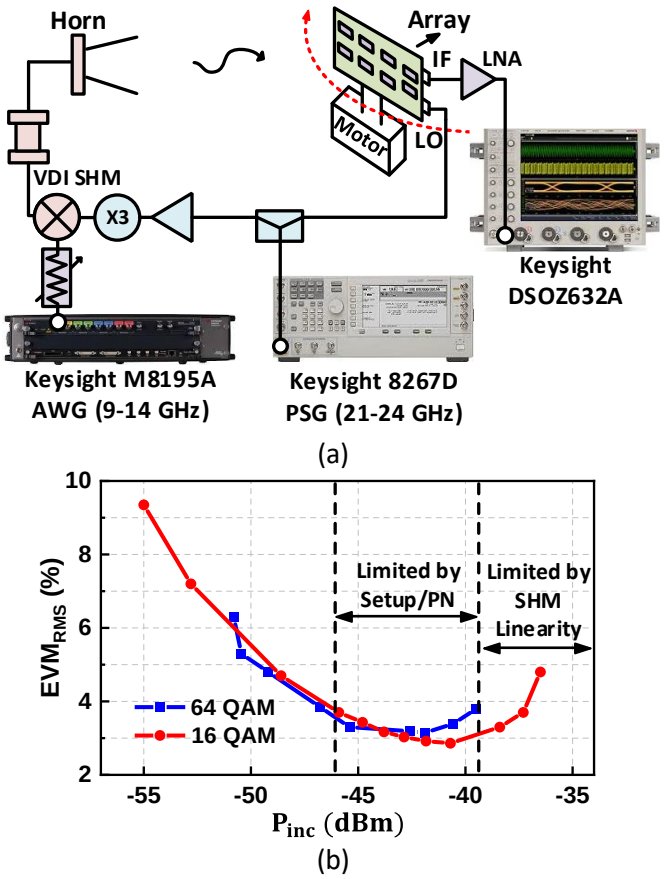


Figure 2.20: (a) Measurement setup for the 140-GHz communication link. (b) Measured EVM using a 16/64-QAM 500-MBd/s modulated signal at 140 GHz (center frequency) versus RF incident power level (P_{inc}).

6.6-6.8% for 16-QAM and 4.7-5.4% for 64-QAM. The EVM versus scan angle is also measured with a 64-QAM 3.6 Gb/s waveform. The EVM remains around 4% from -30° to +30°. Large angle scan EVM is slightly higher due to the lower antenna gain.

Tabel 2.2 and 2.3 compare the performance of the phased-array receiver with state-of-art D-band and G-band phased-arrays. It is hard to compare this work with other published ones, since most of them are only a single or two element phased-array receiver front-end without any system integration, such as frequency downconversion and chip-to-antenna packaging, except [29]. Compared to the phased-array receiver in [29], this work integrates the RF front-ends, RF-to-IF

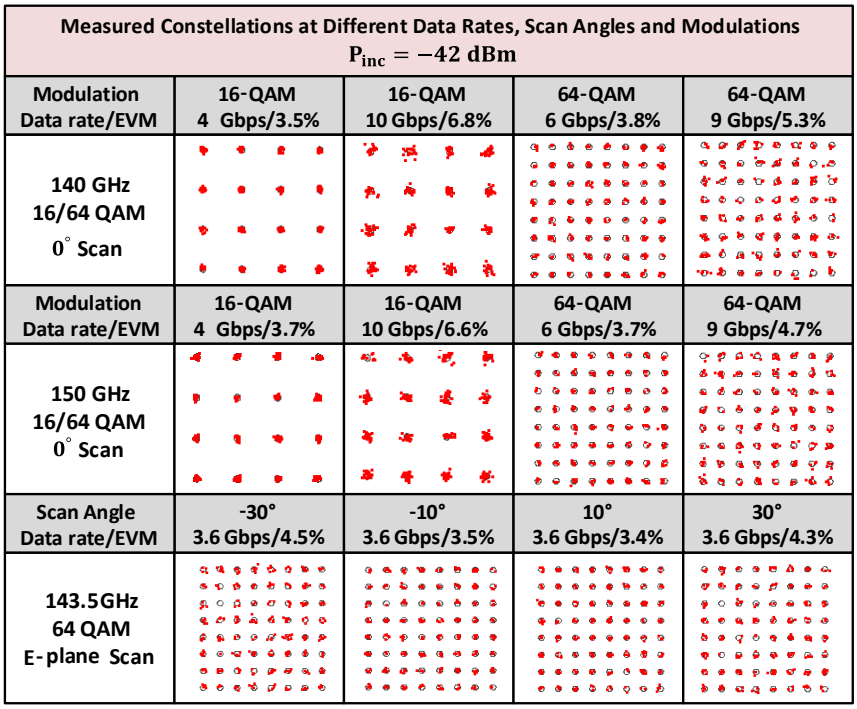


Figure 2.21: Measured constellations and EVMs of the array at different data rates, scan angles and modulations at P_{inc} = -42 dBm.

conversion and IF beamformers in a single chip. This paper also reports a low-cost assembly method at D-band, realizing a high efficiency antenna including the antenna-to-chip transition loss.

2.8 Conclusion

This chapter presented a 140-GHz 8-element wafer-scale phased-array receiver with an IF beamforming architecture and having very low RMS phase and gain errors. The phased-array receiver achieves 7 dB system noise figure on average when referenced to the channel input by implementing a low-noise RF front-end design. The array can receive 16 and 64-QAM waveforms at all scan angles and data rates up to 10 Gbps. To the author's best of knowledge, this is the first wafer-scale phased-array receiver with lowest noise figure at 140 GHz in silicon.

Table 2.2: Performance Comparison of D-band and G-band Phased-Array Receivers Part I

	This work	**RFIC'20** [29]	**MWCL'18** [31]
Process	45-nm CMOS-SOI	130-nm SiGe	130-nm SiGe
Frequency (GHz)	139-155[a]	130-170[b]	111-120
Element Number	8	8	2
Beamforming Architecture	RF Front-end + IF Beamforming	RF Beamforming	RF Beamforming
Size (mm^2)	25.38	1.97/element	2.1[d]
NF (dB)	6.4-7.5[g]	10[c]	11-12[c]
Peak Gain (dB)	27.5[e]	22	13
PDC/element (mW)	145	165[f]	53[f]
Gain Control	10	N/A	N/A
Scan Range ($^\circ$)	$\pm$35	Not specified	N/A
RMS Gain Error (dB)	$<$0.5	Not specified	$<$2
RMS Phase Error ($^\circ$)	$<$5	Not specified	$<$9
Chip-Antenna Packaging	Quartz Superstrate	Radio-on-glass	N/A
Over-The-Air Communication (Data Rate (Gb/s))	10 (16-QAM) 9 (64-QAM)	N/A	N/A

[a]System front-end BW. [b]Chip BW. [c]Simulated. [d]Without pads. [e]Electronic gain referenced to the antenna aperture. [f]RF front-end only. [g]Measured channel NF using GSG probes, noise source and waveguide passives.

2.9 Appendix I

To simplify the F_{min} derivations, an assumption of $C_{gd} = C_{neu}$ is taken in section IV. To further analyze the differential pair (DP) without any neutralization, the two-port noisy network theory is used to calculate the input refered equivalent noise voltage $\bar{v_{eq}}$ and current $\bar{i_{eq}}$ as:

$$\bar{v_{eq}} \cong \bar{v_g} + \frac{\left(g_m + \omega^2 r_g C_T C_D\right)\bar{i_d}}{g_m^2 + \omega^2 C_D^2} + j\left(\frac{r_g g_m C_T \omega + C_D \omega}{g_m^2 + \omega^2 C_D^2}\right)\bar{i_d}; \quad \bar{i_{eq}} \cong j\frac{C_T \omega}{g_m}\bar{i_d} \tag{2.23}$$

Table 2.3: Performance Comparison of D-band and G-band Phased-Array Receivers Part II

This work	**APMC'18**	**APMC'19**	**SiRF'17**
45-nm CMOS-SOI	130-nm SiGe	130-nm SiGe	130-nm SiGe
139-155[a]	170-200[b]	170-190[b]	118-132[b]
8	2	2	1
RF Front-end + IF Beamforming	RF Beamforming	RF Beamforming	RF Beamforming
25.38	1.89	4.7	0.44
6.4-7.5[g]	10[c]	24.5[c]	N/A
27.5[e]	13	19	13
145	16.6[f]	92.5	125[f]
10	N/A	N/A	N/A
±35	N/A	N/A	N/A
<0.5	<0.9	<0.9	Not specified
<5	<15	<15	Not specified
Quartz Superstrate	N/A	N/A	N/A
10 (16-QAM) 9 (64-QAM)	N/A	N/A	N/A

[a]System front-end BW. [b]Chip BW. [c]Simulated. [d]Without pads. [e]Electronic gain referenced to the antenna aperture. [f]RF front-end only. [g]Measured channel NF using GSG probes, noise source and waveguide passives.

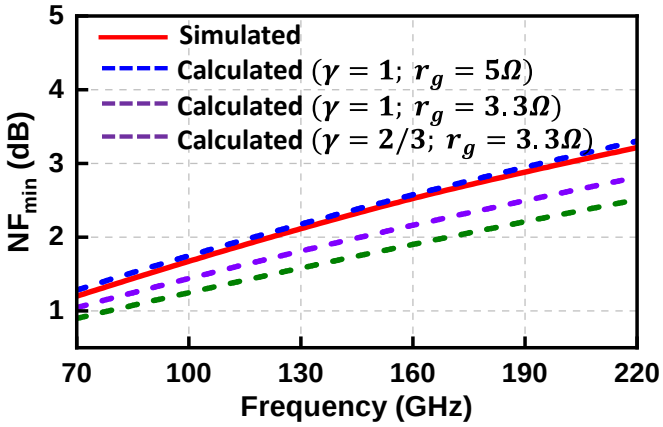


Figure 2.22: Simulated and calculated DP NF_{min} without C_{neu}.

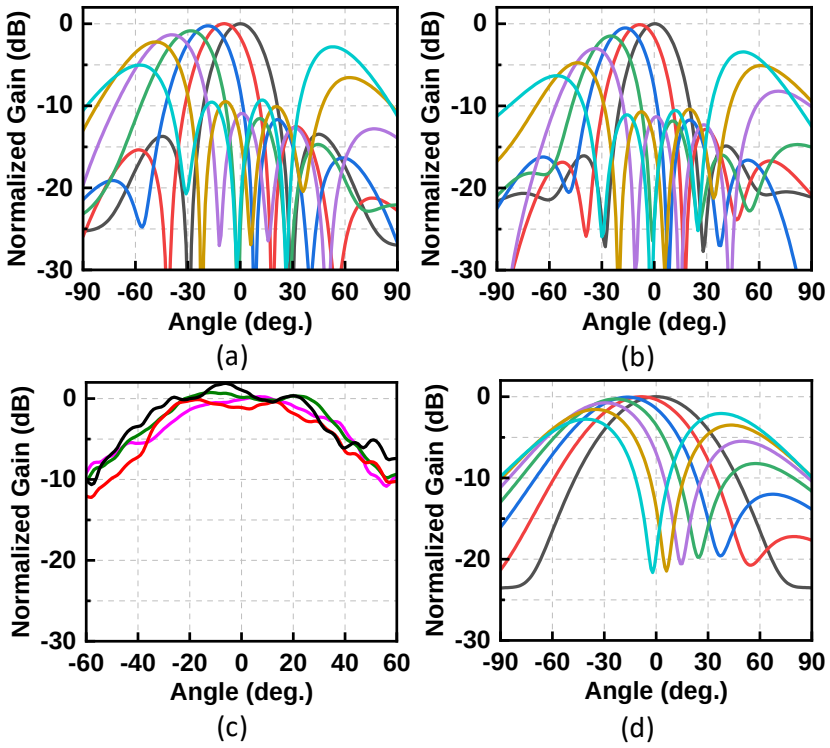


Figure 2.23: Simulated finite array E-plane scanning patterns at (a) 140 GHz and (b) 150 GHz. 140 GHz (c) measured array element patterns and (d) simulated finite array H-plane scanning patterns.

where $\bar{v_g}$ and $\bar{i_d}$ are the transistor gate noise voltage and the drain noise current. Y_c and G_u are then derived as:

$$Y_c = \frac{\bar{v_{eq}^*} * \bar{i_{eq}}}{\bar{v_{eq}^2}} \cong \frac{\omega C_T}{\beta} \frac{g_m \left(g_m r_g C_T \omega + C_D \omega\right)}{g_m^2 + \omega^2 C_D^2} + j \frac{C_T \omega}{\beta} \frac{g_m^2 + g_m \omega^2 r_g C_T C_D}{g_m^2 + \omega^2 C_D^2} \tag{2.24}$$

$$G_u \cong r_g \left(\left(\frac{C_T \omega}{\beta} \frac{g_m^2 + g_m \omega^2 r_g C_T C_D}{g_m^2 + \omega^2 C_D^2} \right)^2 + \left(\frac{\omega^2 C_T g_m \left(g_m r_g C_T + C_D\right)}{\beta \left(g_m^2 + \omega^2 C_D^2\right)} \right)^2 \right) \tag{2.25}$$

$$F_{min} = 1 + 2 \left(\frac{\omega}{\omega_T} \right) \left(\gamma A_1 + \sqrt{\frac{\gamma r_g \left(g_m A_2^2 + \omega^2 \frac{\left(g_m r_g C_T + C_D\right)^2}{g_m} A_3^2 \right)}{\beta} + \left(\gamma A_1\right)^2} \right) \tag{2.26}$$

where A_1, A_2 and A_3 are:

$$A_1 = \frac{g_m\left(g_m r_g C_T \omega + C_D \omega\right)}{g_m^2 + \omega^2 C_D^2} \tag{2.27}$$

$$A_2 = \frac{g_m^2 + g_m \omega^2 r_g C_T C_D}{g_m^2 + \omega^2 C_D^2} \tag{2.28}$$

$$A_3 = \frac{g_m^2}{g_m^2 + \omega^2 C_D^2} \tag{2.29}$$

Given that C_T and g_m are estimated to be 44 fF and 34.5 mS, NF_{min} of the differential pair without neutralization is calculated versus frequency for various γ and r_g values combinations [Fig. 2.22]. Based on the derivations presented above, The DP NF_{min} is lower due to the larger ω_T and smaller C_T, and to the higher denominators of both G_c and G_u. The uncancelled C_D term makes the summation of g_m^2 and $\omega^2 C_D^2$ larger.

2.10 Appendix II

The simulated E-plane patterns of the 4×2 finite array at 140 and 150 GHz are presented in Fig. 2.23(a) and (b). At 140 GHz, the scanning capability is 50° with a 3-dB gain drop. At 150 GHz, the simulated scanning capability is 40° with a 5-dB gain drop. This is similar to the measured results where 150 GHz has worse scanning capability than 140 GHz.

Fig. 2.23(c) presents the measured element broadside patterns at 140 GHz. The element gain on average drops to -5 dB and -10 dB at 40° and 60°, respectively. Fig. 2.23(d) presents the simulated finite array H-plane patterns for scan angles of $0-50°$ at 140 GHz.

2.11 Acknowledgment

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Chapter 2, in full, is a reprint of the material as it appears in: S. Li, Z. Zhang, B. Rupakula and G. M. Rebeiz, "An Eight-Element 140-GHz Wafer-Scale IF Beamforming Phased-Array Receiver with 64-QAM Operation in CMOS RFSOI", in *IEEE Journal of Solid-State Circuits*, doi: 10.1109/JSSC.2021.3102876.. The dissertation author was the primary investigator and author of this paper.

Chapter 3

An Eight-Element 136-147 GHz Wafer-Scale Phased-Array Transmitter with 32 dBm Peak EIRP and $>$ 16 Gbps 16QAM and 64QAM Operation

3.1 Introduction

Recent advancements in the $>$ 100 GHz millimeter-wave systems have enabled ultra-high data rate short-range communication [14–28]. Due to the wide unused bands with less interference at these frequencies, systems at these frequencies are good candidates to meet the increasing requirement of data consumption and less communication latency, creating an opportunity for high speed applications, such as wireless backhaul, Internet of Things (IoT) and virtual/augmented reality (VR/AR). An interesting band is D band (110-170 GHz) with a wide frequency spectrum (60 GHz). The 140-150 GHz frequency range, as one of the sub bands of it, is suitable for longer-range wireless broadband mobile, since it has less atmospheric absorptions (e.g., oxygen

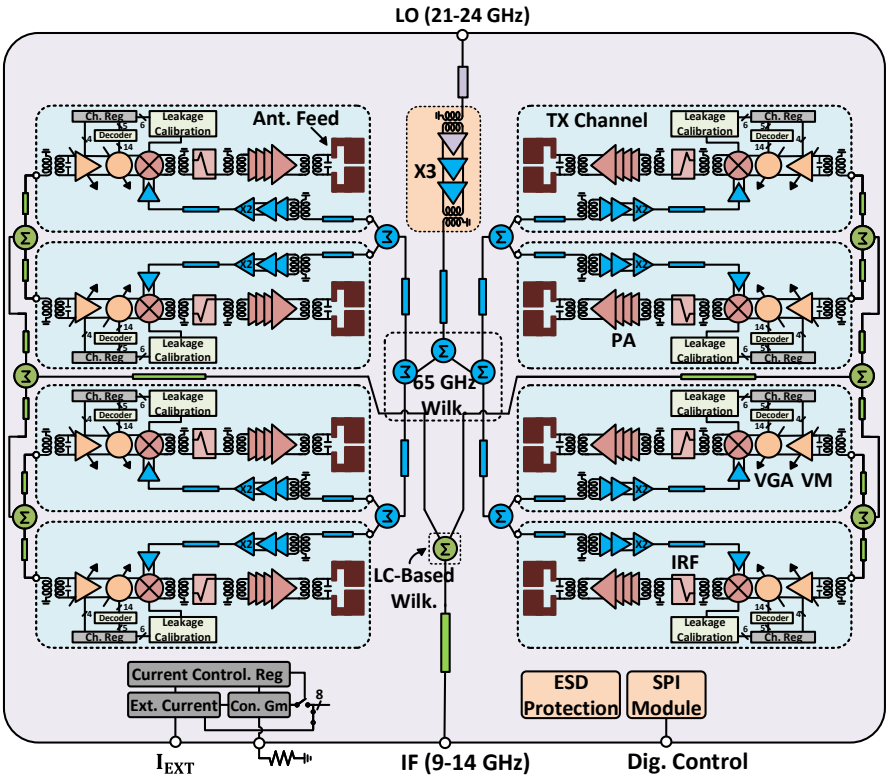


Figure 3.1: Block diagram of 8-element wafer-scale IF beamforming phased array transmitter chip at 140 GHz.

and water molecule absorptions) resulting in additional path loss than the 120-130 GHz range or the 170-180 GHz range. [3, 49, 50]. Also, in order to improve the system integration level and lower their cost, designs based on advanced CMOS processes are preferable. Transistors are capable of providing enough intrinsic gain at 140 GHz in these processes, since their associated f_t and f_{max} are $\sim$ 300 GHz [39, 51].

Compared to 60 GHz, 140 GHz has much higher free space path loss (FSPL). To overcome the space loss and maintain a high link budget over a wide angular region at 140 GHz, phased-array systems are desired. On the transmit side, the design target is to increase the phased-array effective isotropic radiated power (EIRP), which requires high output power for every transmit channels and also, antenna arrays with high radiation efficiency [9, 29, 52].

In order to build a large-scale phased-array at 140 GHz, a practical beamforming archi-

tecture is desirable. The conventional all-RF beamforming architecture is widely used at 6-100 GHz [6–8, 53–59]. However, at 140 GHz, it suffers from high phase shifter loss and variable gain amplifier (VGA) phase variation. Digital beamforming architecture is not practical due to much higher power consumption, which mostly comes from the I/Q quadrature LO paths to drive the mixers and analog-to-digital converters (ADCs) with high sampling rate and bandwidth. A high-IF beamforming architecture is therefore used at 140 GHz [Fig. 3.1], and this work presents a complementary chip to the 4×2 receive array presented in [60].

This chapter presents an 8-element 140-GHz phased-array transmitter with detailed circuit analysis and measurements, and is an expanded version of [61]. Section 3.2 presents the wafer-scale phased-array transmitter chip block diagram. Section 3.3 presents the 140 GHz power amplifier design. Section 3.4 focuses on other key circuit blocks design. Section 3.5 presents the phased-array system analysis. The phased-array channel breakout and system measurements are demonstrated in Section 3.6 and 3.7. Section 3.8 concludes this chapter.

3.2 Wafer-Scale Phased-array IF beamforming transmitter architecture

Fig. 3.1 presents the 140-GHz wafer-scale phased-array transmitter chip. The array is composed of 8-element IF beamforming transmit channels with 5-bit phase and 4-bit gain control, LC-based Wilkinson IF splitters, and a multiplier chain and distribution networks in the LO path to allow for an LO input frequency of 21-24 GHz. For lower LO distribution network loss, the input LO signal first passes by a tripler (×3) to 63-72 GHz and is then distributed using Wilkinson power dividers to the 8 channel LO chain blocks, each containing an LO doubler.

The IF signal in each channel is upconverted to the 140 GHz spectrum using a mixer and the 21-24 GHz (×6) LO. The mixer output spectrum has the fundamental RF signal at 140-150 GHz and the image signal at 120-130 GHz. A image rejection filter with 2 poles and a zero

at the image band is therefore implemented at the output of the mixer. Its frequency response, together with the tuned gain response of the PA driving amplifiers, realize a large enough image rejection ratio (IRR), and result in an efficient PA power stage. Note that image reject filter is not sharp enough to suppress the LO leakage. Therefore, the upconversion mixer in each channel is co-designed with current digital-to-analog converters (CDACs) to cancel the LO leakage.

The chip is designed in the GlobalFoundries 45RFSOI process. The floating-body thin-oxide RF 40-nm CMOS-SOI transistor is used for RF/LO/IF circuits design. Transistors designed for drivers and amplifiers have an associated f_t and f_{max} of 193 and 297 GHz (modeled to the top metal) at relatively low bias current density (J_{DC} of 0.17 mA/μm) [36]. Transistors designed for the power stage of the power amplifier are biased at 0.35 mA/μm (class A), and with associated f_t and f_{max} of 350 and 270 GHz.

3.3 140 GHz power amplifier

3.3.1 Transistor-Level Analysis with Neutralization

The capacitive neutralization technique has been widely adopted in D-band PA design [13], [62] and [42] [Fig. 3.2(a)]. Usually, it is used to improve both the transistor pair stability and the maximum available gain (MAG). The double-gate contact power stage transistor pair size is designed to be $30\times1.6\mu$m for compact layout and less interconnections, which are preferred at 140 GHz for accurate electromagnetic (EM) modelling. Relaxed poly pitch transistors are chosen due to less parasitics and enhanced stress response (higher gm) [39]. Due to their reasonable gate resistance r_g value (simulated to be 5-6 Ω), they are also capable of being stable themselves with enough gain when neutralization is used.

Fig. 3.2(b) presents the simulated f_T, f_{max} and the effective transconductance G_m of the power stage without neutralization versus transistor current density J_{DC}. The transistors are biased in class A mode with J_{DC} of 0.35 mA/μm for high G_m and gain. To analyze the neutralization

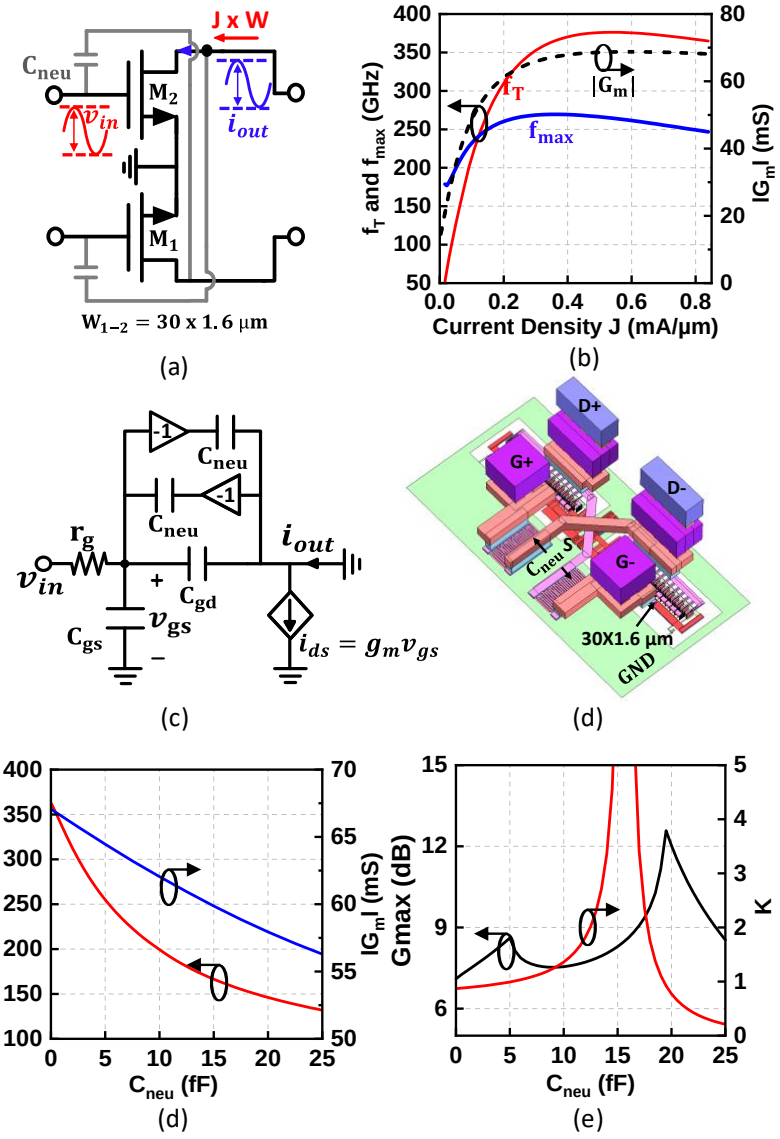


Figure 3.2: (a) PA power stage transistor pair schematic. (b) Simulated f_T, f_{max} and the effective transconductance G_m of the power stage without neutralization versus transistor current density J_{DC}. Power stage (c) effective half circuit small-signal model and (d) 3-D layout. Simulated (e) f_T, G_m, (f) Gmax and K factor of the transistor pair versus C_{neu} with J_{DC} of 0.35 mA/μm.

effect on the transistor pair G_m and linearity, the equivalent neutralized differential pair (NDP) half-circuit small signal-model and its layout are presented in Fig. 3.2(c) and (d) [43], The f_t, G_m

and $|G_m|$ are:

$$f_T \cong \frac{g_m}{2\pi\sqrt{C_T^2 - C_D^2}}; \quad G_m = \frac{g_m - j\omega C_D}{1 + j\omega C_T r_g} \tag{3.1}$$

$$|G_m| \cong \frac{\sqrt{(g_m + \omega^2 C_T C_D r_g)^2 + \omega^2 (g_m C_T r_g - C_D)^2}}{1 + \omega^2 C_T^2 r_g^2} \tag{3.2}$$

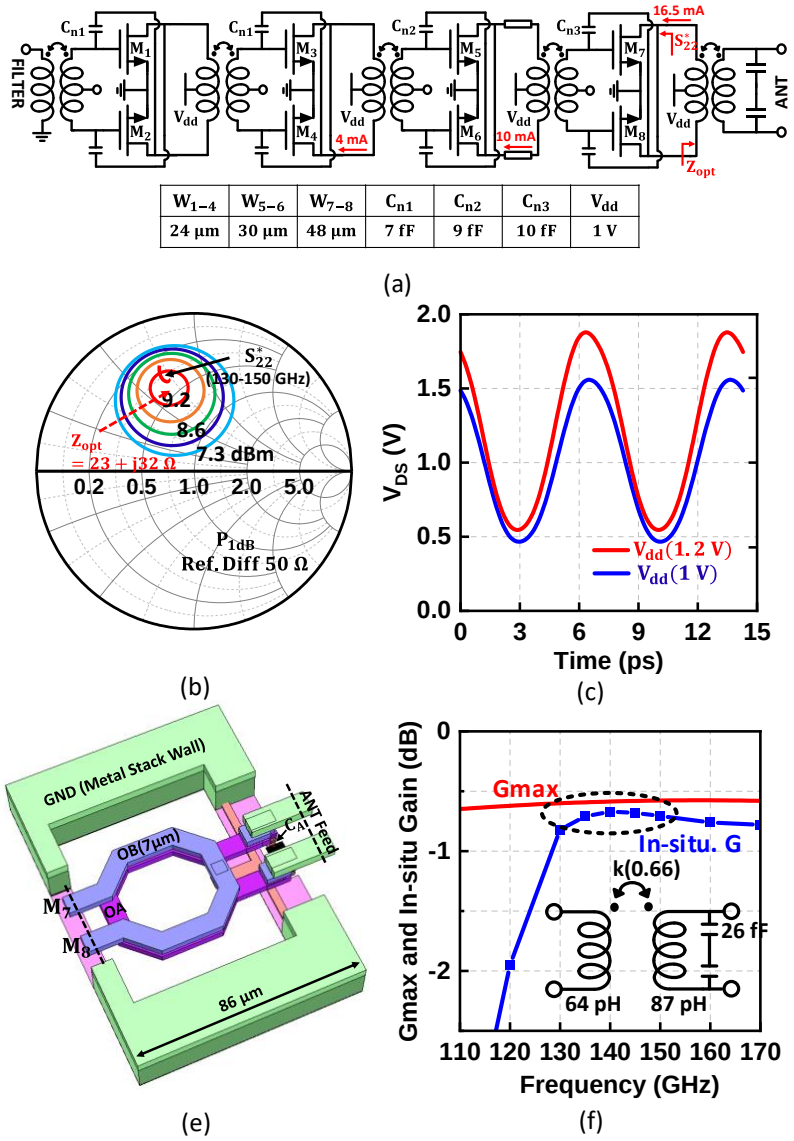
where C_T and C_D are given by:

$$C_T = \left(C_{gs} + C_{gd} + C_{neu}\right);\ C_D = \left(C_{gd} - C_{neu}\right) \tag{3.3}$$

When C_D drops, which means the value of C_{neu} increases, both f_t and $|G_m|$ (magnitude of G_m) degrade, and is verified in the simulation Fig. 3.2(d). However, neutralization capacitors with large enough values are required for the transistor pair input/output isolation, gain and stability [24] [Fig. 3.2(e)]. Therefore, 10-11 fF neutralization capacitors are implemented in this design for the power stage since they are able to stablize the differential pair and maintain high f_t and $|G_m|$.

3.3.2 PA Design

A 4-stage differential transformer-coupled PA is used with capacitive neutralization [Fig. 3.3(a)]. The first two stages serve as the pure amplifier stages, providing enough gain to lower the input power level requirement. These stages employ 24×1 μm transistors biased with J_{DC} of 0.17 mA/μm to save DC power and improve the efficiency. The 3^{rd} stage is designed to be the driver with enough output linear power to drive the last power stage. All interstage matching networks are designed using transformers for compact layout and low loss. The asymmetric transformer between the driver stage and the power stage, as an example, is achieved using a stacked structure for high coupling. Also, 25 pH in series with the driver stage realize an impedance transformation network (large transformation ratio) and conjugate matching with a simulated 1.5 dB loss (Gmax) at 140 GHz [42].



W_{1-4}	W_{5-6}	W_{7-8}	C_{n1}	C_{n2}	C_{n3}	V_{dd}
24 μm	30 μm	48 μm	7 fF	9 fF	10 fF	1 V

Figure 3.3: (a) 4 stage transformer-coupled PA. (b) Simulated load pull contours at 140 GHz and output S_{22}^* at 130-150 GHz. (c) Simulated V_{DS} of transistor M_7 at $\sim P_{1dB}$ and 140 GHz with different supplies. Output transformer (e) layout, and (f) simulated Gmax and in-situ (loaded) gain.

Fig. 3.3(b) presents the load pull simulation of the power stage. Given that the supply voltage (V_{dd}) is 1 V, the optimal loadline/Z_{opt} is $(23+j32)\Omega$. The S_{22}^* curve at 130-150 GHz is very close to the center of the loadpull power contours. This is also another important reason why a 10-11 fF (not 15-16 fF close to the intrinsic C_{gd} value) neutralization capacitors are chosen for

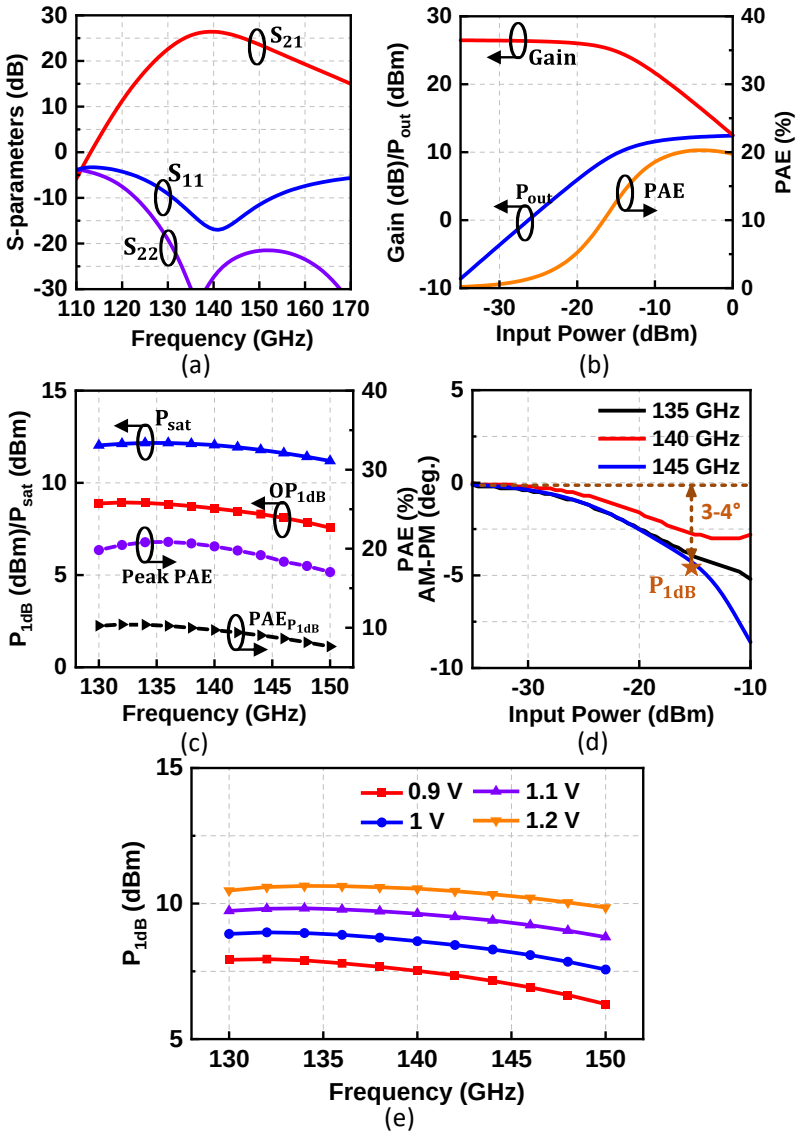


Figure 3.4: Simulated PA: (a) S-parameters and (b) gain, P_{out} and power added efficiency (PAE) versus input power level. (c) P_{sat}, P_{1dB}, peak PAE and PAE at P_{1dB} versus frequency. (d) AM-PM distortions and (e) OP_{1dB} with different supply voltages.

the power stage since they make the power and gain matching very close without any trade-off when designing the power stage output transformer.

Fig. 3.3(c) presents the simulated output V_{DS} waveform at P_{1dB} at 140 GHz. It can be observed that single-ended peak-peak voltage swings V_{pp} are 1.1 V (V_{dd} = 1 V) and 1.3 V (V_{dd}

= 1.2 V), respectively. The output matching network between the power stage and the antenna feed as the interface is designed with highly-coupled metal-stacked structure with low loss and high-pass response [Fig. 3.3(e)]. Fig. 3.3(f) shows that its simulated in-situ (loaded) gain at 130-150 GHz is greater than -0.8 dB.

The simulated PA small and large-signal performance are presented in Fig. 3.4 with a peak gain of 26.5 dB at 140 GHz and a 3 dB bandwidth of 131-150 GHz. The input is well-matched at 130-150 GHz with S_{11} is $<$ -10 dB. The output is also well-matched to differential 50 Ω with S_{22} $<$ -20 dB at 130-170 GHz, since the power and gain matching impedances are very close. Fig. 3.4(b)-(e) presents the large-signal simulations with P_{sat} and OP_{1dB} of 11.2-12.2 dBm and 7.6-8.9 dBm, respectively, at 130-150 GHz. The corresponding peak PAE and PAE at OP_{1dB} are 17-20.8% and 7.6-10.4%, respectively [Fig. 3.4(c)]. Fig. 3.4(d) presents the AM-PM distortions at different frequencies and are $3-4^{\circ}$ even up to the P_{1dB} level since this PA is a class A design. About 3 dB power increase is observed when the supply voltage increases from 0.9 to 1.2 V at 140 GHz, as shown in Fig. 3.4(e).

3.4 Other Key Circuit Blocks Design

3.4.1 Upconversion Mixer

The upconversion mixer utilizes an active architecture for low LO voltage swing requirement. A double-balanced topology is used so that the mixer is less sensitive to the differential LO swing asymmetry. To reduce the LO leakage, a compact and centrosymmetric switching quad layout is implemented, as shown in Fig. 3.5(b) [11]. Also, two 5-bit fine-tuning current DACs are used to steer the current in the differential branches and used as the LO leakage cancellation circuitry [Fig. 3.5(a)]. The mixer consumes 14 mA from a 1.4 V supply in the small-signal mode, and results in a power conversion gain of 2-3 dB and an output P_{1dB} is -5 dBm at 140 GHz (LO: 129 GHz, IF: 11 GHz, RF: 140 GHz and image: 118 GHz). Both the RF and the image signals

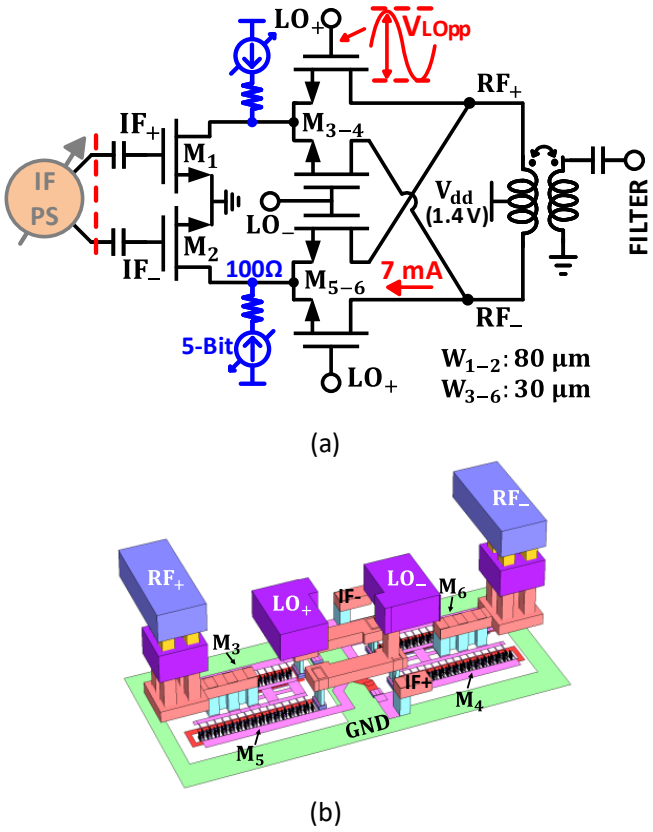


Figure 3.5: (a) Active mixer schematic. (b) 3-D layout of the mixer switching quad.

appear at the mixer output which limits its linearity.

3.4.2 Image Rejection Filter

Fig. 3.6(a) presents the elliptical image rejection filter (IRF) between the mixer and the PA. A series LC network is designed to create a zero in the filter response at 125-127 GHz to suppress the image signal power level. The filter response is critical to improve the PA linearity when the image signal is close or inside the PA working band. For example, as shown in Fig. 3.6(b), assuming a high-IF signal at 10 GHz and an LO at 138 GHz, the upconverted RF and image signals are at 148 and 128 GHz, respectively. In this case, the image signal is close to

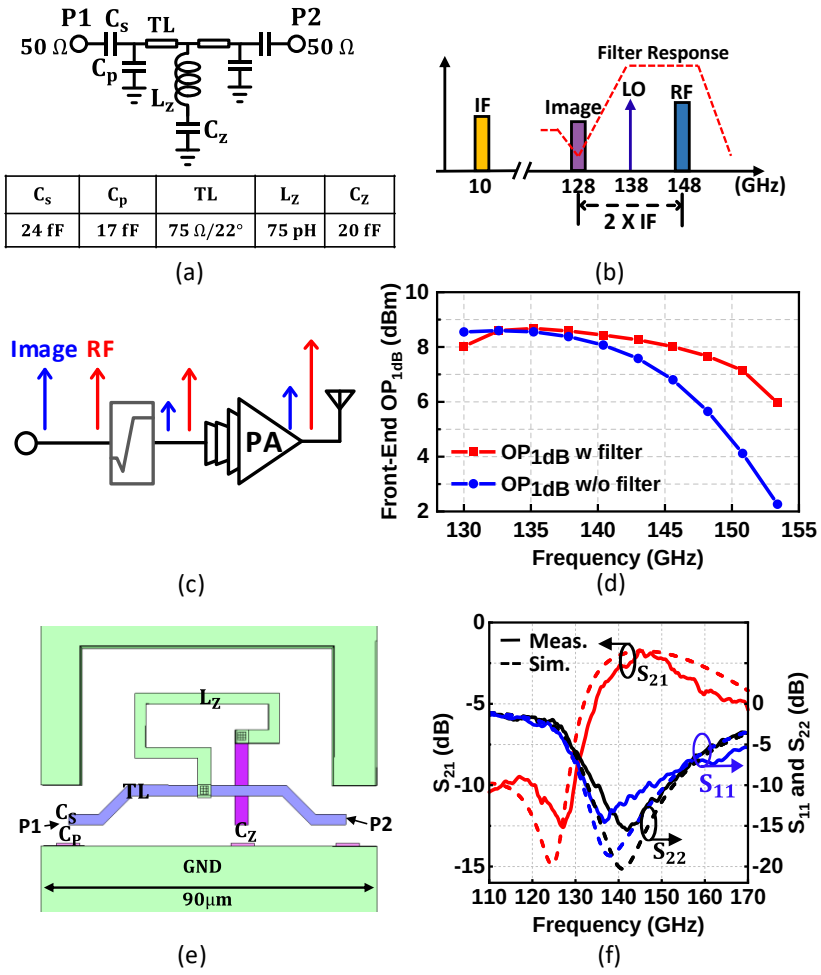
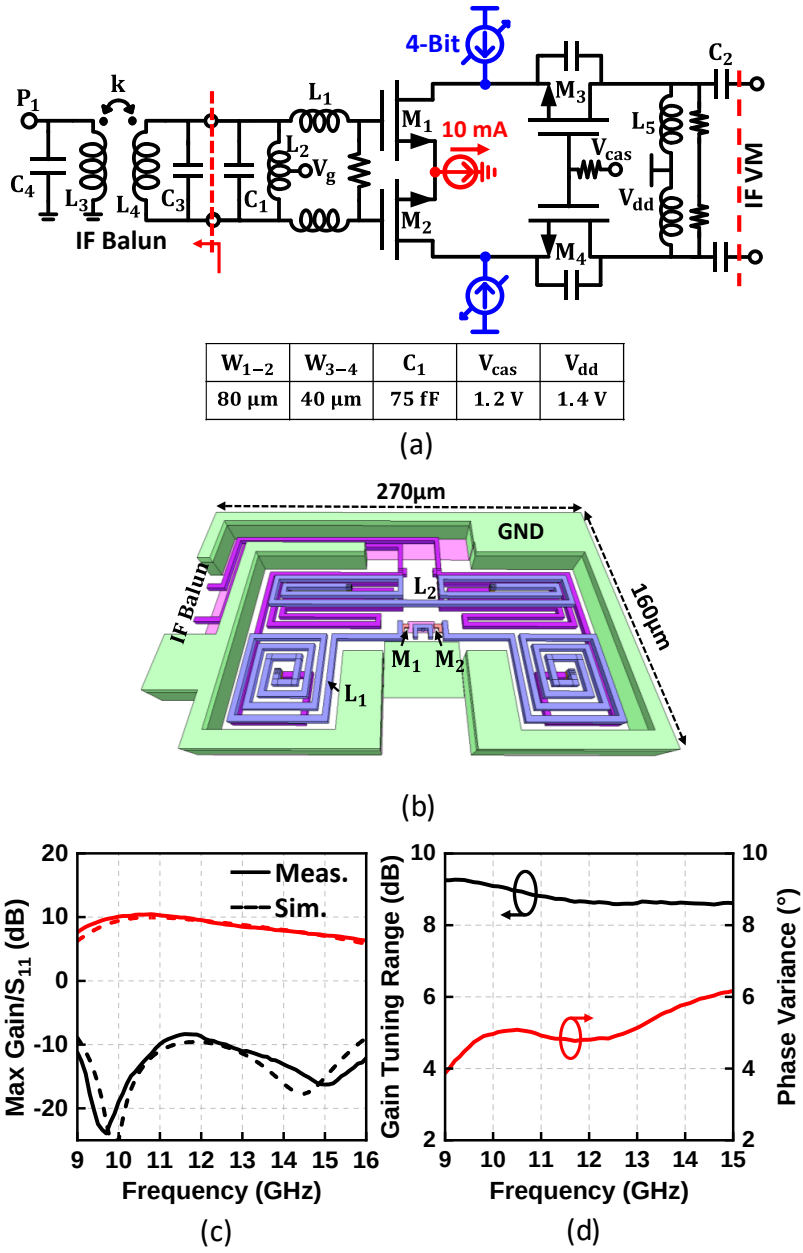


Figure 3.6: (a) Image rejection filter (IRF) schematic. (b) Frequency spectrum of the IF, RF, LO and image signals. (c) Filtering PA schematic. (d) Simulated front-end OP_{1dB} with and without filter versus frequency. IRF (e) layout 3-D view and (f) simulated and measured S-parameters.

the PA working band and is not suppressed by the PA gain response. Therefore, two signals are present at the PA power stage load and this limits the PA linearity.

Fig. 3.6(c) presents the filtering PA schematic and IRF is required, especially when the RF signal frequency is $>$ 140 GHz to maintain the PA linearity at the RF signal band [Fig. 3.6(d)]. Also, even though the on-chip IRF selectively is limited due to the low quality factor (Q-factor) of the passive filter, the image can still be suppressed by the filter since the frequency span between the image and the RF signal is 2$\times$IF and as high as 20 GHz. However, in this case, the LO



W_{1-2}	W_{3-4}	C_1	V_{cas}	V_{dd}
80 µm	40 µm	75 fF	1.2 V	1.4 V

Figure 3.7: (a) Wideband IF VGA schematic. (b) 3-D compact layout of the input matching network. (c) Simulated and measured input matching S_{11} and VGA maximum gain. (d) Measured VGA gain tuning range and maximum phase variance versus frequency.

leakage is close to the RF band, and LO leakage cancellation is needed in the mixer design.

Fig. 3.6(e) presents the IRF layout 3-D view (EM-model) with a measured in-band

insertion loss of 2 dB [Fig. 3.6(f)] and with S_{11} and S_{22} < -10 dB at 133-150 GHz. The measured image rejection ratio (IRR) is 10.5 dB and the null is at 128 GHz. The discrepancy between simulation and measurement (2.5 dB less IRR and a little frequency shift) is due to the Q of L_z being lower than expected.

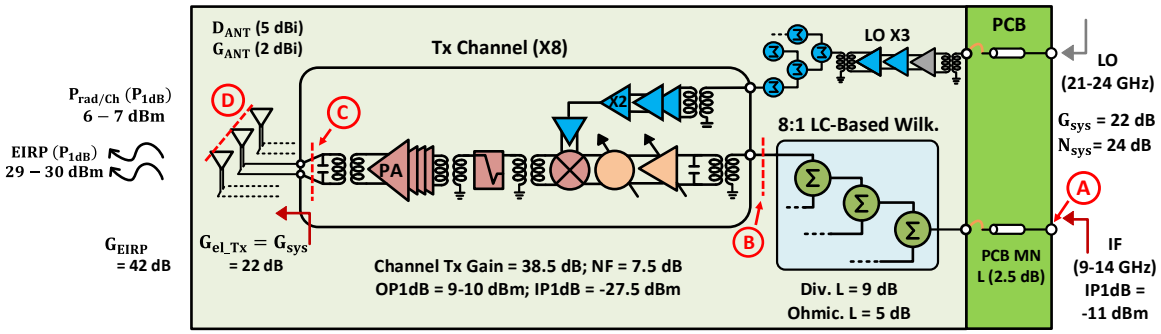
3.4.3 IF VGA with Wideband Input Matching

Fig. 3.7 presents the differential variable gain amplifier (VGA) at 9-14 GHz. The input matching starts from a wideband IF balun with dual resonance. Its minimum insertion loss is 1.3 dB and with a 1-dB bandwidth of 8.7-16 GHz. The balun input and output are matched to single-ended 50-Ω and differential 100-Ω, respectively, with both reflection coefficients < -10 dB at 9-15 GHz. The differential VGA input matching network is also designed with dual resonance for wideband performance matched to differential 100-Ω as the interface. Differential 100-Ω TL is implemented for the connection between the balun differential output and the VGA input. Fig. 3.7(b) shows a very compact VGA input wideband matching network layout 3-D view. As presented in Fig. 3.7(c), the measured VGA breakout maximum gain and S_{11} (including the balun) are 10 dB and < -10 dB at 9-16 GHz, respectively [Fig. 3.7(c)]. The VGA consumes 14 mW P_{DC} from a 1.4 V supply. It is based on current- steered topology with 4-bit gain control. The measured gain control range and maximum phase variance are ∼9 dB and < 6°, respectively.

3.4.4 Other System Blocks

The IF phase shifter is based on the active vector modulator and is similar to the design in [60]. The measured phase shifter RMS gain and phase errors at 9-15 GHz are <0.6 dB and <6°, respectively.

The ×6 LO chain, composed of a ×3 section with a 65 GHz distribution network, and then a ×2 section with a 130 GHz driver for the double-balanced mixer, has also been presented



	A	B	C	D
Sig. P (dBm)	-11	-27.5	10	30 (EIRP)
Noise (dBm/Hz)	-174	-166.5	-128	-117
P_N(dBm) BW = 1 GHz	-84	-76.5	-38	-27

Figure 3.8: 140 GHz 8-element phased-array gain, EIRP, linearity and noise analysis.

in [60]. The LO chain delivers > 0 dBm to the mixer with a total of 0.6 W of power consumption for the 8 channels.

3.5 Phased-Array Tx System Analysis

Fig. 3.8 presents the system-level analysis for gain, EIRP, linearity and noise for the 8-element phased-array transmitter. The system has two gain definitions: EIRP gain (G_{EIRP}) and Tx channel electronic gain (G_{el_Tx}) and are:

$$G_{el\_Tx} = \frac{P_{el}}{P_{in}} \tag{3.4}$$

$$G_{EIRP} = \frac{EIRP}{P_{in}} \tag{3.5}$$

where P_{in} is the system input power at the IF port and P_{el} is defined as the RF output power from each channel. G_{el_Tx} is also called system gain, G_{sys}, as it relates the RF output power to the IF

input power for each channel. The relationship between EIRP and P_{el} is given by:

$$EIRP = P_{el} + 20log(N) + G_{ANT} \tag{3.6}$$

where N is the number of antenna elements and G_{ANT} is the antenna gain

$$G_{ANT} = D_{ANT} + \varepsilon_{ANT} \tag{3.7}$$

The unit patch antenna directivity is given by $D_{ANT} = 4\pi A_{ph}/\lambda^2$ and is 5 dBi for A_{ph} = 0.5λ ×0.5λ. The simulated antenna radiation efficiency is ∼ 50% (-3 dB) leading to $G_{ANT} = 2$ dB. The Tx channel, including PA, filter, mixer and IF beamformer, has a simulated gain of $G_{ch} = 38.5$ dB. with an OP_{1dB} of P_{el} = 9-10 dBm and an IP_{1dB} of -27.5 dBm. Given that the 8-to-1 IF Wilkinson power splitter has a total loss of 14 dB (9-dB division loss and 5-dB ohmic loss), and the PCB wideband matching network and transmission line have another 2.5-dB loss, the G_{el_Tx} is calculated as:

$$G_{el\_Tx} = G_{sys} = G_{Ch} + L_{Wilk.} + L_{PCB} = 22\ dB \tag{3.8}$$

G_{EIRP} is then calculated using (4), (5) and (6).

$$G_{EIRP} = G_{el\_Tx} + 20log(8) + G_{ANT} = 42\ dB \tag{3.9}$$

The required input power at the connector is:

$$IP_{1dB_{sys}} = IP_{1dB_{Ch}} + L_{Wilk.} + L_{PCB} = -11\ dBm \tag{3.10}$$

Finally, the simulated EIRP is 29-30 dBm according to (3.6): The simulated channel noise figure NF_{Ch} is 7.5 dB, and the noise power in a 1 GHz bandwidth at the channel output P_{Ch_N} is:

$$\begin{aligned} P_{Ch_N} &= -174 + NF + 10log(BW) + G_{Ch} \\ &= -174 + 7.5 + 90 + 38.5 = -38\ dBm \end{aligned} \tag{3.11}$$

The array radiated EIRP noise power $EIRP_N$ adds incoherently and is:

$$EIRP_N = P_{Ch_N} + 10log(N) + G_{ANT} = -27\ dBm \tag{3.12}$$

The system radiated signal to noise ratio (SNR_{sys}) at $EIRP_{sys_{1dB}}$ is:

$$SNR_{sys} = EIRP_{sys_{1dB}} - EIRP_N = 57\ dB \tag{3.13}$$

This means that even if the input signal is at 20 dB back-off, the SNR_{sys} is still high enough for the Tx array to maintain a very low EVM for a 1 GHz bandwidth waveforms.

3.6 Phased-Array Tx Channel Measurements

Fig. 3.9(a) and (b) present the Tx channel breakout block diagram and die photo, respectively. For the test channel, a two-paths PA was used with a slightly different design and an output P1dB of 9.5 dBm at 148 GHz with a DC power consumption of $\sim$ 280 mW. The input IF signal is swept from 9.5-15.5 GHz with different LO frequencies (21.5-23 GHz), and the measured channel peak gain is 35 dB. The instantaneous bandwidths for different LO frequencies are measured to be 4-5 GHz and the Tx channel is capable of supporting high data rate communication [Fig. 3.9(c)]. Fig. 3.9(c) presents the 4-bit gain states of the IF VGA with 10-dB gain tuning range (IF:

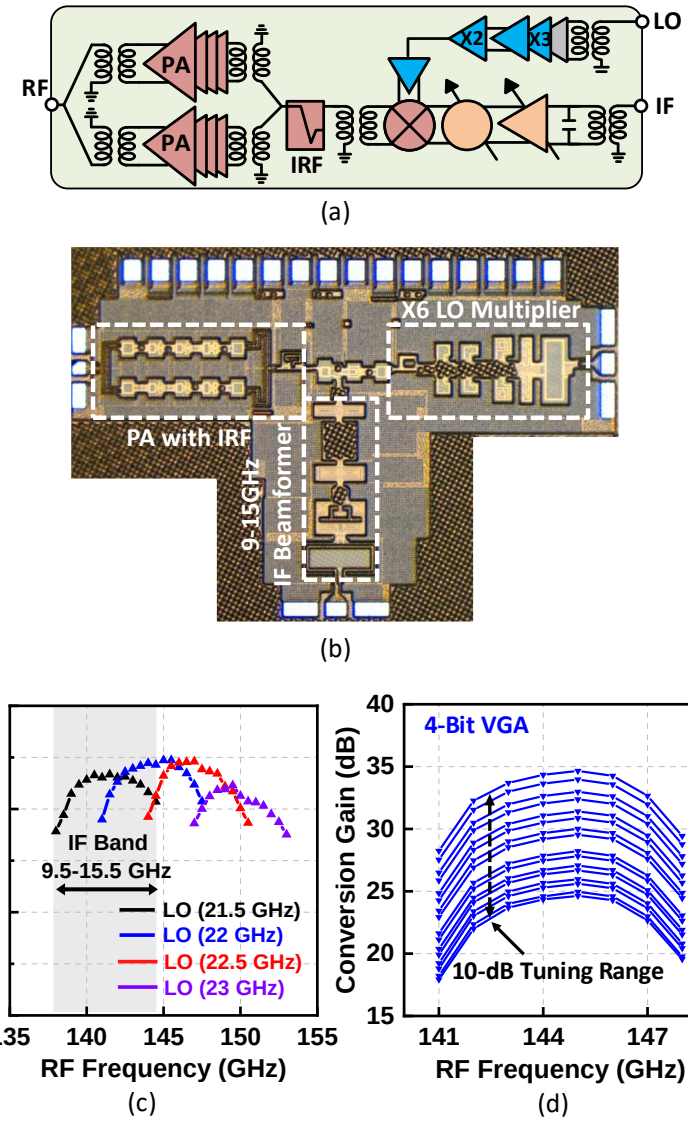
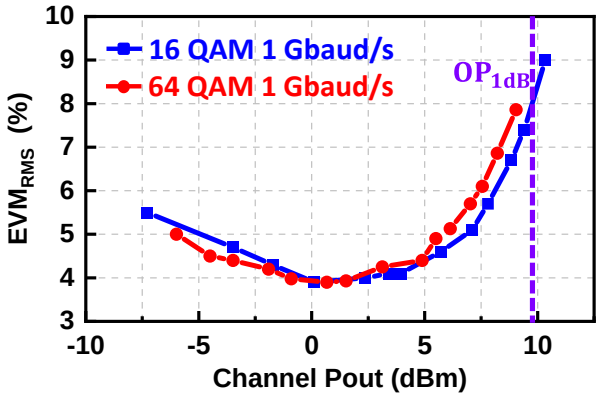


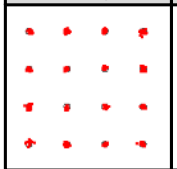
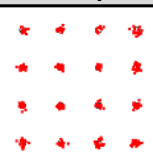
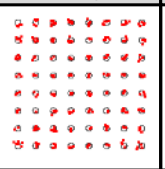
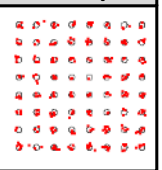
Figure 3.9: Tx channel breakout (a) schematic and (b) die photo. Measured channel (c) conversion gain with different LO frequencies and (d) 4-bit gain response.

9-16 GHz and LO: 22 GHz) and is designed mostly for element gain calibration. The IF phase shifter response at IF of 9-14 GHz is very similar to [60] and not shown for brevity.

Fig. 3.10(a) presents the measured channel EVM_{RMS} using QPSK and 16/64-QAM 1-Gbaud/s signals versus array EIRP at 148 GHz (center frequency). An $\alpha = 0.35$ is used resulting in a peak-to-average-ratio (PAPR) of 6.6 and 7.7 dB for the 16-QAM and 64-QAM waveforms,



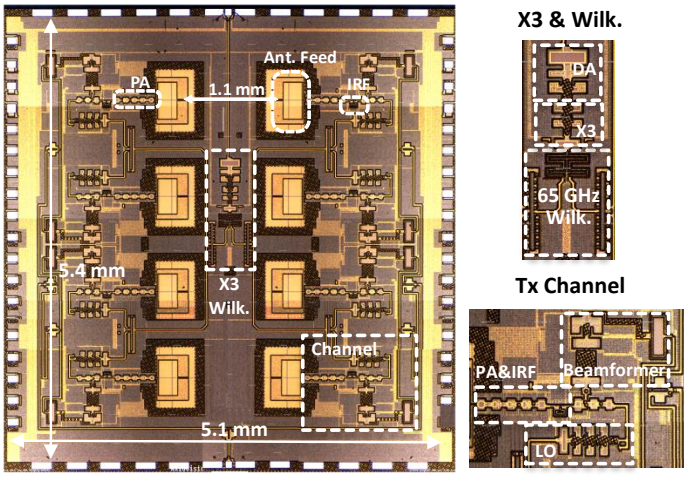
(a)

Pout: 3.5dBm /6dB BO		Pout: 1.5dBm /8dB BO	
4 Gb/s	16 Gb/s	6 Gb/s	21 Gb/s
			
4.1%	5.6%	3.9%	5.1%

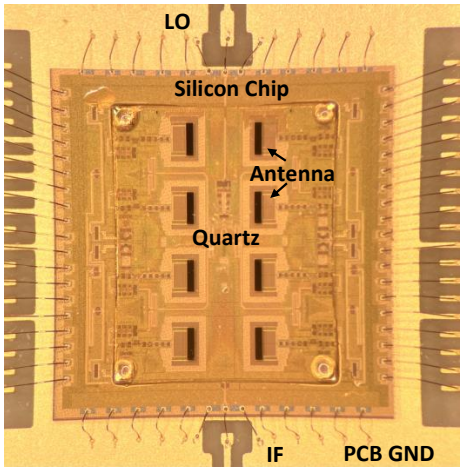
(b)

Figure 3.10: (a) Tx channel EVM using a 16/64-QAM 1-Gbaud/s waveforms at 148 GHz (center frequency) versus output RF power. (b) Measured constellations at 148 GHz with different output power and data rates.

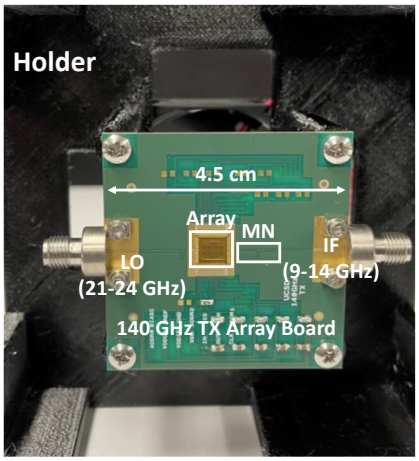
respectively. When the channel operates at 2-3 dBm (P_{out} 6-7 dB backoff from P_{1dB}), the channel EVM_{RMS} is $\sim 4\%$, which is mostly limited by the setup. Fig. 3.10(b) presents the measured constellations and EVM_{RMS} values at different data rates and EIRP. The measured maximum data rate is $\sim$ 21 Gb/s for 64-QAM waveforms at 148 GHz. The achieved EVM is 5.1% with 1.5 dBm channel.



(a)



(b)



(c)

Figure 3.11: (a) 8-element phased-array transmitter die photo. (b) Tx chip with antenna and quartz (100 µm thickness superstrate) attached. (c) Assembled PCB and holder for over-the-air (OTA) measurements.

3.7 Phased-array Measurements

Fig. 3.11 presents the 8-element phased-array transmitter die photo (size: 5.1 mm $\times$ 5.4 mm) including the PCB and holder. The antenna spacing is $\sim \lambda/2$ in the air at 140 GHz, which is close to 1.1 mm. The chip consumes 1.9 W from a 1.2 V supply (for the PA) and a 1.5 V supply for LO and IF circuits. The DC power is broken as: $\sim$156 mW/channel (total is 1.25 W

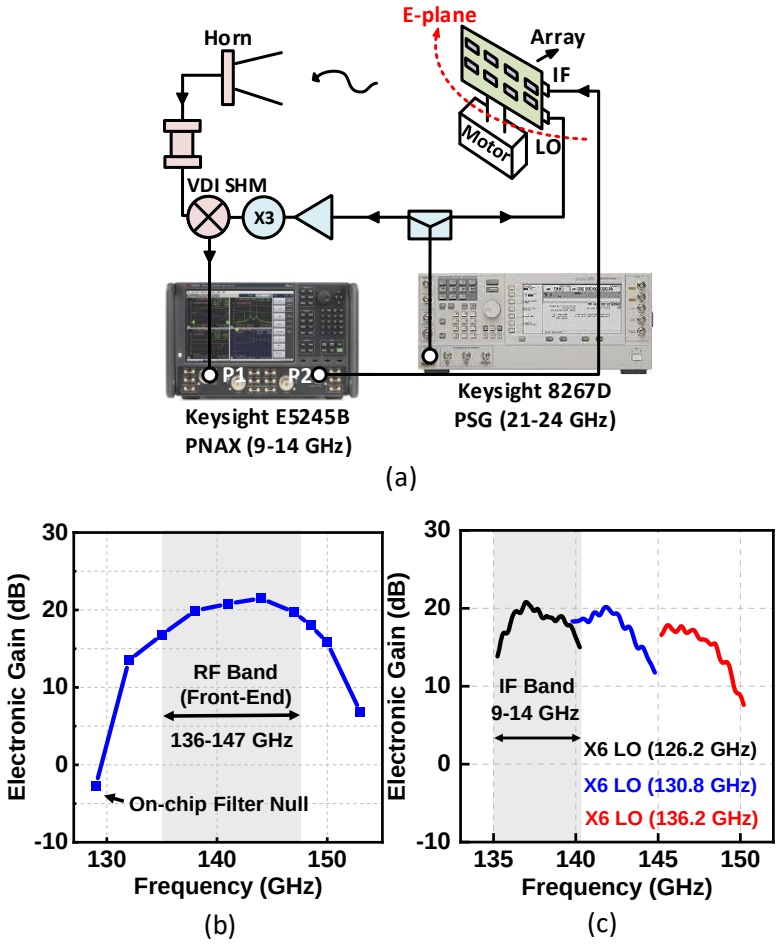


Figure 3.12: (a) Measurement setup for the array small signal. Measured array channel electronic gain with (b) a fixed IF (11 GHz) and (c) different LO frequencies.

for 8 channels (not including channel LO doubler chains)) and ∼0.6W for the LO multiplication and distribution. The IF division and distribution network is all passive and has zero power consumption.

3.7.1 Transmit Electronic Gain and Patterns

The phased-array Tx measurements are done using a WR-6 standard horn antenna [Fig. 3.12(a)]. A single external LO signal passes through a power splitter with one path feeding the

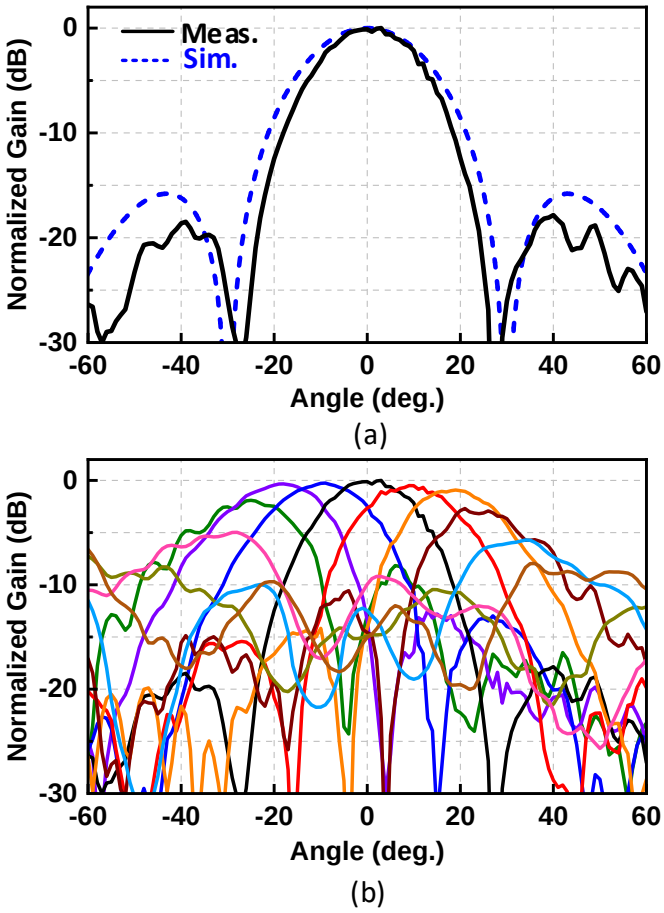


Figure 3.13: 138 GHz E -plane (a) measured and simulated broadside beam patterns and (b) measured beam patterns versus scan angle.

phased-array on-chip $\times 6$ multiplier, and the other path feeding an external $\times 6$ passive multiplier, including a passive tripler and a subharmonic mixer. This path is used to downconvert the received RF signal from the horn antenna to the IF spectrum. A PNA-X (Keysight E5245B) is used to measure the S_{12} at the IF band, and is critical to measure the channel phase states for calibration. After de-embedding the space loss, the horn gain and the setup loss, the EIRP gain G_{EIRP} is derived as:

$$G_{EIRP} = G_{S_{12}} - SLF + L_{Setup} - G_{Horn} \tag{3.14}$$

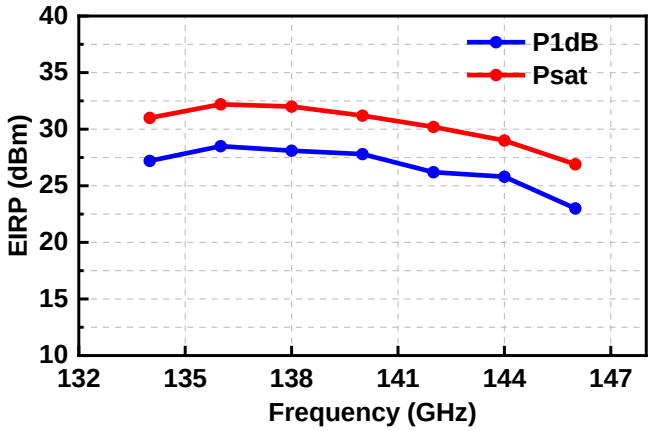


Figure 3.14: Measured array EIRP at P_{1dB} and P_{sat} versus frequency

where L_{Setup} includes the waveguide loss, external mixer loss and cables loss, and SLF is the space loss factor, $SLF = (\lambda/4\pi R)^2$.

The measured phased-array transmit channel electronic gain, G_{el_Tx}, is 21 dB with a 3-dB front-end bandwidth of 136-147 GHz and agrees well with the simulated value of 22 dB [Fig. 3.12(b)]. In this measurement, the LO is swept with a fixed IF at 11 GHz. The lower and upper bound of the bandwidth are limited by the on-chip filter response and the antenna response, respectively. To measure the instantaneous bandwidth of the array, the excited IF signal is swept from 9-14 GHz with different LO frequencies. The measured instantaneous 3-dB bandwidth is 3-4 GHz and is due to the IF beamformer and lumped-element Wilkinson combiner gain response.

Fig. 3.13 presents the measured patterns at 138 GHz. The broadside measured pattern compares well with the simulated pattern [Fig. 3.13(a)]. The 8-element phased-array Tx is electronically scanned in the E-plane with a beam scan range is $\pm 30^\circ$ and sidelobe levels $<$ -10 dB. It does not agree with simulations (which predict a scan angle of 50°). As mentioned in [60], the discrepancy is probably due to the underestimated TM0 mode surface-wave contribution in a small truncated thick substrate ($0.09\lambda_d$ at 140 GHz). The antenna frequency response also may

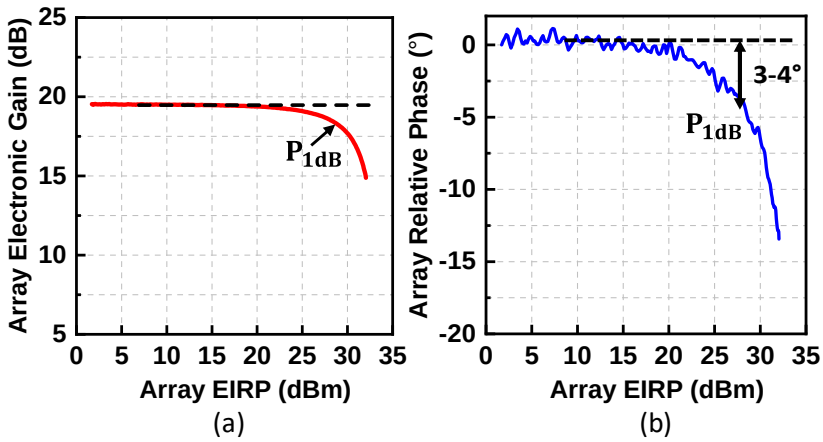


Figure 3.15: Measured array (a) AM-AM and (b) AM-PM distortions versus array EIRP at 138 GHz.

have shifted down due to the fabrication and assembly errors. In the future, it is best to use a 50 μm thick quartz superstrate at the expense of narrower operating bandwidth.

3.7.2 Array EIRP and Linearity

The array EIRP and linearity measurements use the same setup as Fig. 3.12(a). Fig. 3.14 presents the measured EIRP_{1dB} of 23-28.3 dBm and EIRP_{sat} of 27-32 dBm at 134-146 GHz, and agree well with simulations to within 1 dB.

The array AM-AM and AM-PM response at 138 GHz is presented in Fig. 3.15. There is no gain expansion in the AM-AM response versus EIRP, and the AM-PM distortion at the array OP_{1dB} is only 3-4° since the PA is biased in class A mode. This benefits the array transmit error vector magnitude (EVM) due to the low AM-PM distortion and array high $OIP3$ (simulated 10-11 dB higher than the OP_{1dB}).

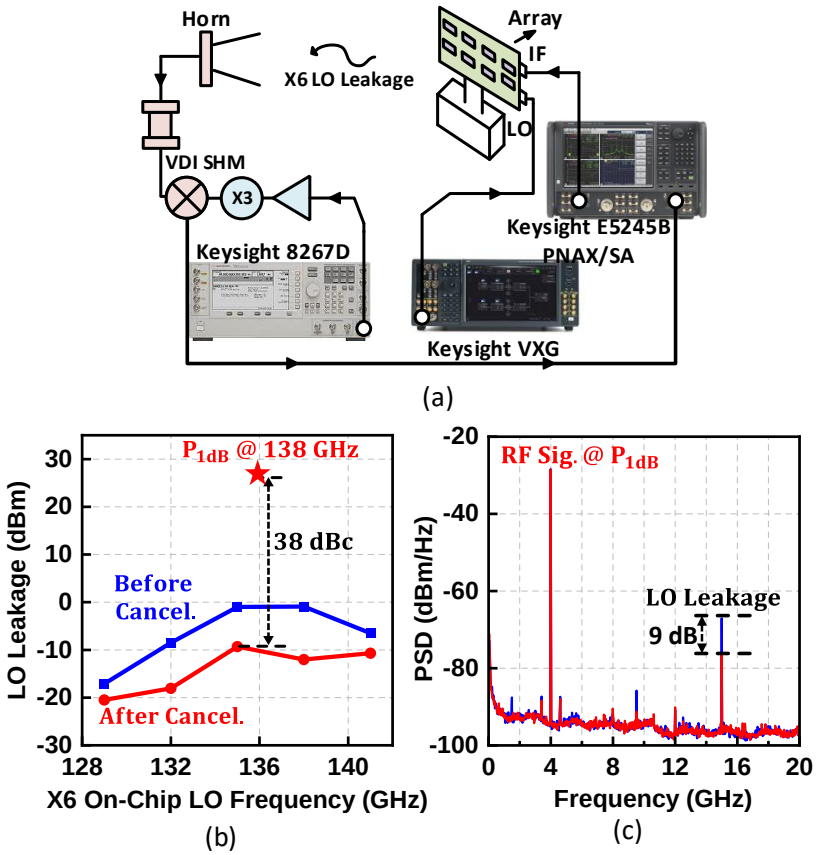


Figure 3.16: (a) Measurement setup for the array LO leakage measurements. (b) Measured LO leakage power level versus $\times 6$ LO on-chip frequency before and after LO leakage cancellation. (c) Measured frequency spectrum at the subharmonic mixer output with 9 dB LO leakage improvement (after the down-conversion externally).

3.7.3 Array LO Leakage

Fig. 3.16(a) presents the measurement setup for LO leakage measurements. Separate LO signals are used to feed the array and the external subharmonic mixer leading to a different IF on the receive path. The LO fed into the array is swept from 128 to 141 GHz ,and the downconverted LO leakage signal in the IF band is detected using the spectrum analyzer function in the PNA-X. The $\times 6$ LO EIRP leakage at 135 GHz is measured to be -1 dBm and -10 dBm before and after the LO leakage cancellation (DACs are used), respectively, showing a 9 dB leakage rejection improvement. The LO leakage at $<$ 135 GHz is much lower since it is suppressed by the on-chip

filter. Compared to the array $EIRP_{1dB}$ at 138 GHz (28 dBm), the LO EIRP leakage rejection after the cancellation is 38 dBc, as shown in Fig. 3.16(b) and (c).

3.7.4 Communication-links

The phased-array over-the-air performance is measured using the setup shown in Fig. 3.17(a). A modulated IF signal from the arbitrary waveform generator (AWG) is upconverted to 140 GHz on-chip and transmitted out from the phased-array. The received signal is downconverted to the IF band using a VDI subharmonic mixer, and demodulated by the Keysight DSO-Z series scope running the VSA9600 demodulation software with internal equalization. To evaluate the modulated signal EVM versus array EIRP, the array input power is swept using an external IF attenuator.

Fig. 3.17(b) presents the measured array EVM_{RMS} using QPSK and 16/64-QAM 200-MBaud/s signals versus array EIRP at 137 GHz (center frequency). An $\alpha = 0.35$ is also used. When the array operates with < 20 dBm EIRP (8 dB backoff from P_{1dB}), the array EVM_{RMS} is measured to be 2-2.5%, which is mostly limited by the setup. Note that the PSG integrated LO RMS jitter (offset frequency < 100 MHz) is around 23 fs (at 22 GHz), and the LO phase noise contribution alone to the EVM at 132 GHz (after $\times 6$) is calculated to be 1.9%. The 8-element phased-array is capable of delivering an average output power of up to 25 dBm for 16 and 64-QAM signals and with $< 5\%$ EVM_{RMS} (-25 dBc), which is only 3-dB bakcoff from P_{1dB} [Fig. 3.17(b)]. This is due to the class A design soft compression at high output power. The 200 MBaud 64-QAM downconverted spectrums in the IF band are presented in Fig. 3.17(c) and (d). The adjacent channel power leakage ratio is measured to be 33 dBc at a EIRP of 22 dBm.

Fig. 3.18 presents the measured constellations and EVM_{RMS} values of the array at different data rates and EIRP in QPSK, 16 and 64-QAM at 137 GHz (center frequency). The measured maximum data rates are > 16 Gb/s in 16-QAM and 64-QAM. The achieved EVMs are 6.2% for 16-QAM and 5.2% for 64-QAM with 22 dBm array EIRP. The EVM_{RMS} versus scan

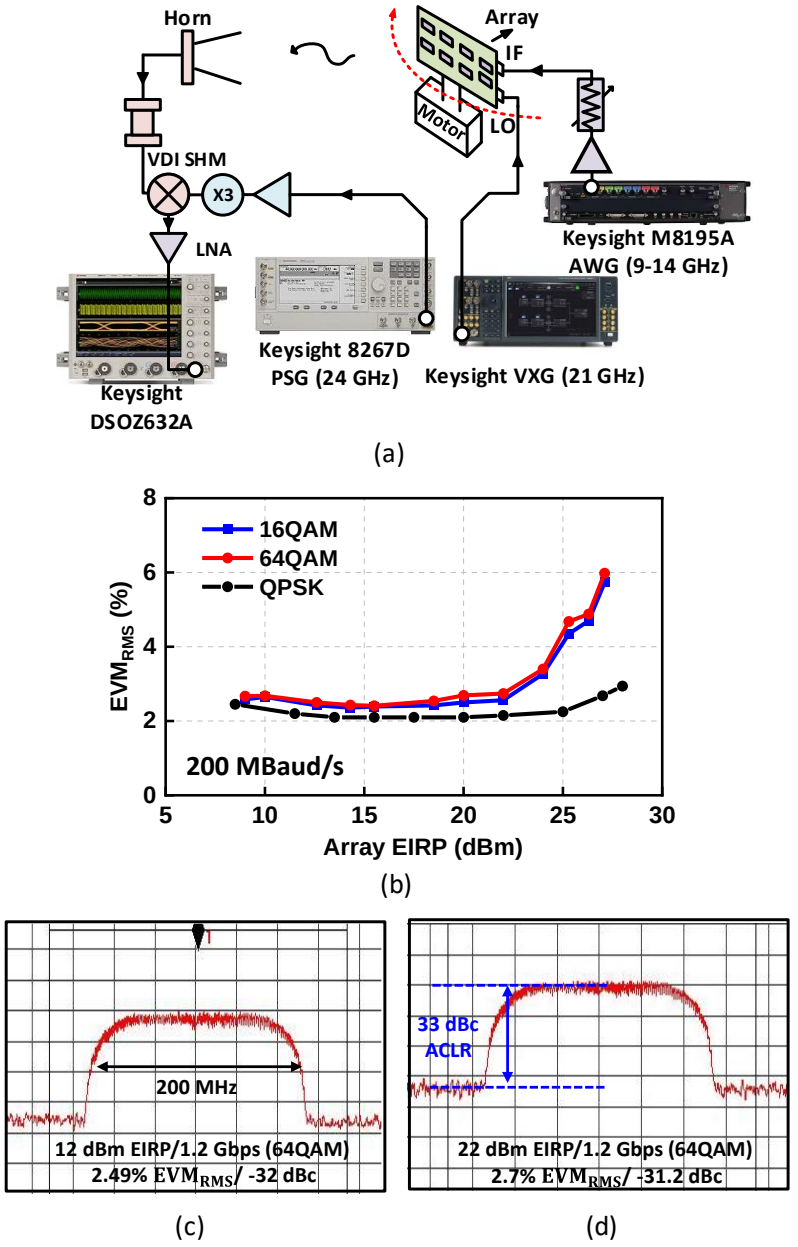
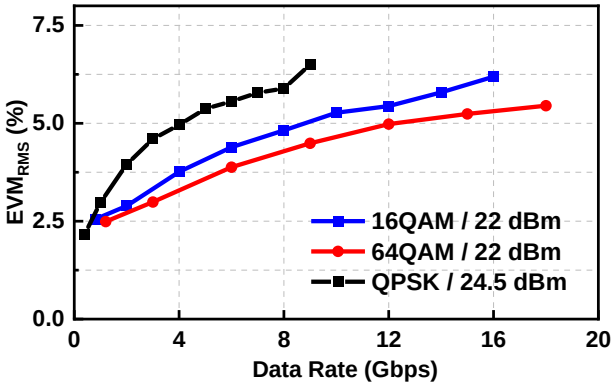
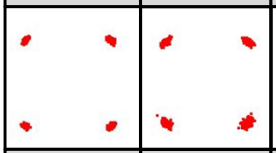


Figure 3.17: (a) Over-the-air (OTA) EVM measurement setup. (b) Measured EVM values using QPSK or 16/64-QAM 200-MBaud/s waveforms at 137 GHz (center frequency) versus array EIRP. Measured array output frequency spectrums (after down-conversion at the receive horn) in 64-QAM operation with EIRP of (c) 12 dBm and (d) 22 dBm, respectively.

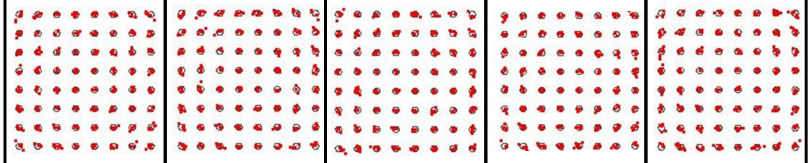
angle is also measured with a 64-QAM 1-GBaud waveform at a center frequency of 143 GHz. The EVM remains at 3.8-3.9% from -30° to +30° [Fig. 3.18(c)].



(a)

EIRP 24.5 dBm (QPSK)		EIRP 22 dBm (16QAM)		EIRP 22 dBm (64QAM)	
2 Gb/s	9 Gb/s	4 Gb/s	16 Gb/s	6 Gb/s	18 Gb/s
					
3.9%	6.5%	3.7%	6.1%	3.9%	5.4%

(b)

EIRP 20 dBm / 8dB BO (64QAM / 6 Gbps)				
-30°	-10°	0 °	10°	30°
				
3.92%	3.83%	3.83%	3.88%	3.94%

(c)

Figure 3.18: (a) Measured EVM using a QPSK/16/64-QAM modulated signal at 137 GHz (center frequency) versus data rate with 3.5 dB (QPSK) and 6 dB (QAM) backoff. (b) Measured constellations of QPSK/16/64-QAM modulated signals at 137 GHz with different array EIRP and transmitted data rates. (c) Measured EVM at different scan angles using a 64-QAM 1-GBd/s modulated signal at 8-dB BO (20 dBm EIRP) and 143 GHz.

Tabel 3.1 and 3.2 compare the performance of the phased-array transmitter with W-band and D-band phased-arrays. Compared to similar work, this paper reports a system-on-chip solution at D-band, realizing a record system EIRP and high data rates with modulated waveforms.

Table 3.1: Performance Comparison of W-band and D-band Phased-Array Transmitters Part I

	This work	**[29]**	**[9]**
Process	45-nm CMOS-SOI	130-nm SiGe	180-nm SiGe
Frequency (GHz)	136-147[a]	130-170[b]	108-114[a]
Element Number	8	8	16
Beamforming Architecture	RF Front-end + IF Beamforming	RF Beamforming	RF Beamforming
Die Area (mm^2)	33	1.97/element	27.5
Peak EIRP (dBm)	27-32	Not specified	24-24.5
Channel OP_{1dB} (dBm)	9-10	9.8	2.5[c]
Peak Gain (dB)	21[f]	16[e]	27[g]
PDC/element (mW)	231	330	212
Gain Control (dB)	10	N/A	N/A
Scan Range ($^\circ$)	$\pm$30	Not specified	$\pm$30
Gain Error (dB)	<0.5 (RMS)	Not specified	Not specified
Phase Error ($^\circ$)	<5 (RMS)	Not specified	Not specified
Chip-Antenna Packaging	Quartz Superstrate	Radio-on-glass	Quartz Superstrate
Over-The-Air Communication (Data Rate (Gb/s))	16 16/64-QAM	N/A	N/A

[a]System front-end BW. [b]Chip BW. [c]Single-ended OP_{1dB} +3 . [d]Psat. [e]Chip gain. [f]TX channel electronic gain. [g]Array EIRP gain.

3.8 Conclusion

This chapter presented a 136-147-GHz 8-element wafer-scale phased-array transmitter with an IF beamforming architecture and having very low RMS phase and gain errors. The phased-array transmitter achieves 32 dBm peak EIRP and 28 dBm EIRP at OP_{1dB}, respectively. The array can transmit 16 and 64-QAM waveforms at all scan angles and data rates up to 16 Gbps with 22-25 dBm EIRP (3-6-dB backoff from P_{1dB}). To the author's best knowledge, this is the first wafer-scale phased-array transmitter with highest EIRP at 140 GHz in silicon.

Table 3.2: Performance Comparison of W-band and D-band Phased-Array Transmitters Part II

This work	**[63], [64]**	**[65]**	**[52]**
45-nm CMOS-SOI	180-nm SiGe	130-nm SiGe	130-nm SiGe
136-147[a]	75-105[a]	84-102[b]	170-200[b]
8	16	16	1
RF Front-end + IF Beamforming	RF Beamforming	RF Beamforming	RF Beamforming
33	1.97/element	38.94	27.5
27-32	34	N/A	N/A
9-10	6-8[d]	-5[d]	-13[d]
21[f]	14[g]	13[e]	2[f]
231	300 (Tx)	137.5 (Tx)	41.3
10	Not specified	5.3	23
$\pm$30	Not specified	N/A	N/A
$<$0.5 (RMS)	$\pm$1.5	$<$1.2 (RMS)	$<$0.9 (RMS)
$<$5 (RMS)	$\pm$5	$<$5 (RMS)	$<$15 (RMS)
Quartz Superstrate	Antenna on PCB Die flip-chipped on PCB	N/A	N/A
16 16/64-QAM	30 Per Polarization 64-QAM	N/A	N/A

[a]System front-end BW. [b]Chip BW. [c]Single-ended OP_{1dB} +3 . [d]Psat. [e]Chip gain. [f]TX channel electronic gain. [g]Array EIRP gain.

3.9 Acknowledgment

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dBm Peak EIRP and $>$ 16 Gbps 16QAM and 64QAM Operation," presented at 2021 IEEE/MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, Jun. 10, 2021. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in full, has been submitted for publication of the material as it may appear in: S. Li, Z. Zhang and G. M. Rebeiz, "An Eight-Element 136-147 GHz Wafer-Scale Phased-Array Transmitter with 32 dBm Peak EIRP and $>$ 16 Gbps 16QAM and 64QAM Operation", in *IEEE Journal of Solid-State Circuits*, (submitted). The dissertation author was the primary investigator and author of this paper.

Chapter 4

D-Band Multi-Way Power Combined Amplifiers with 19-dBm Psat and 12% Peak PAE in 45-nm CMOS RFSOI

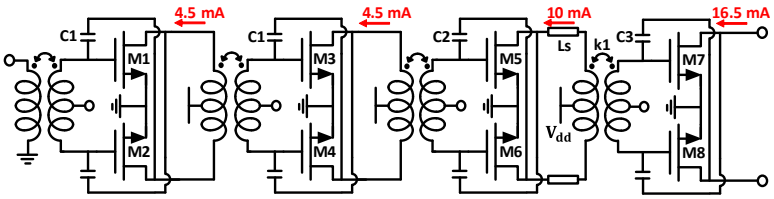
4.1 Introduction

In recent years, silicon-based millimeter-wave (mmW) and sub-THz systems operating in the D-band frequency spectrum (110-170 GHz) have become of increasing interest due to emerging applications, such as short-range high data-rate wireless communications [14–28], image sensing [66, 67] and radar [68–70]. Compared to the frequencies below 90 GHz, at D-band, the free space path loss (FSPL) is high, and a practical system requires a large transmit power with reasonable efficiency. This makes power amplifiers (PAs) as one of the most important and challenging blocks in transmitter designs. A high gain, high output power, linear and efficient PA is required to meet with the system design target. In order to improve the system integration level at low cost, advanced CMOS processes with low-cost and high-yield are preferable. However, the breakdown voltage of the MOS transistors is 1-1.2 V which is lower than III-V technologies,

such as InP [71–73] and GaN [74] or SiGe processes [75–81] and this limits the transistors linearity and maximum output power. Another drawback is that even though the advanced CMOS processes have an f_t and f_{max} of $\sim$ 300 GHz [39, 51], their intrinsic transistor gain is low at D-band (maximum available gain (MAG/Gmax) 6-7 dB at 140 GHz). This means that the driving capability before the power stage is required to be high. Drivers are designed with multi stages and enough gain to lower the input power requirement for system integration. They are implemented using large size transistors and therefore consume a lot of DC power, resulting in low efficiency PA designs.

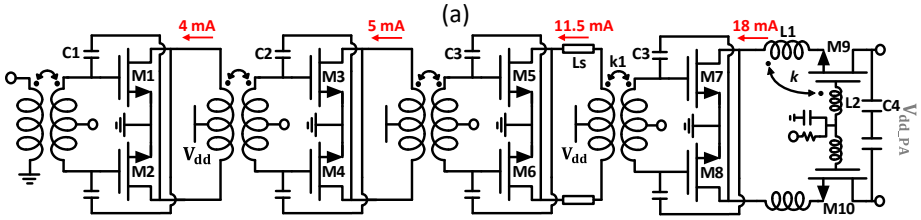
In the prior art, CMOS-based PA above 110 GHz report output powers between 8.6-15 dBm [13, 42, 62, 82–84]. Even though increasing the PA output stage transistors size indeed increase the maximum output power, too big transistors suffer from the interconnect parasitics and complex routing, resulting in low power gain and efficiency. Since the output power from a single MOS transistor is highly limited to $<$ 10 dBm at these frequencies, power combining techniques are implemented to deliver higher output powers and improve PA linearity and efficiency, including transformer-based differential two-way combining [13, 42, 62], direct power-combining [82] and device stacking [84]. Multi-way power combining topologies have additonal combining network loss and typically employ a large chip area. However, the passives size shrink versus frequency and the PAs at D-band are compact [77, 79, 82]. Therefore, in order to further push the output power at D-band, especially the P_{1dB} level, eight-way and beyond power combining with low loss is required.

This chapter expands on work originally presented in [85]. In addition to the eight-way (four-way differential) common source (C.S.) combined PA [Fig. 4.1(a) and (c)] of the original work, a new 130-150 GHz eight-way cascode combined PA utilizing gain boosting techniques [Fig. 4.1(b) and (c)] is also designed in the GlobalFoundries 45nm RFSOI. It is designed with larger saturated output power (Psat) and a higher supply voltage. Section 4.2 presents the technology GF454RFSOI and its performance, explaining why a multi-way combiner with ultra-low loss at



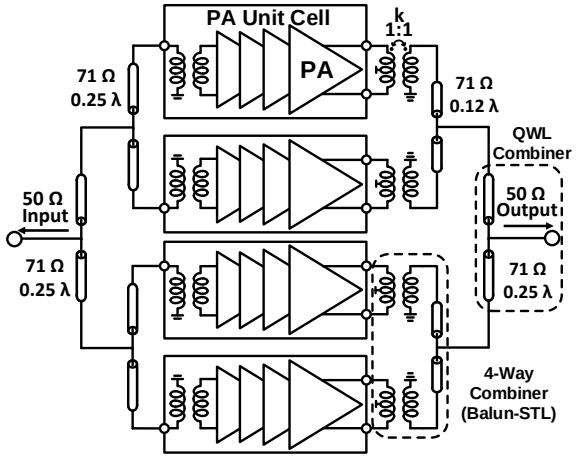
W_{1-4}	W_{5-6}	W_{7-8}	C1	C2	C3	V_{dd}
24x1 µm	30x1 µm	30x1.6 µm	7 fF	9 fF	10 fF	1/1.2 V

(a)



W_{1-4}	W_{5-10}	C1	C2	C3	C4	L1	L2	V_{dd}	V_{dd_PA}
24x1 µm	30x1.6 µm	7 fF	9 fF	10 fF	15 fF	28 pH	12 pH	1.1 V	2.4 V

(b)



(c)

Figure 4.1: Circuit schematics of (a) four-stage common source PA unit cell, (b) four-stage cascode PA unit cell and (c) eight-way combined PA using four-stage PA unit cells.

D-band is used. Device and circuit analysis and design details are expanded in Section 4.3. The methodology of taking measurements involving small signal, large signal AM-AM and AM-PM is expanded in Section 4.4. It is demonstrated that two eight-way combined PAs can deliver up to 17.5 and 19 dBm Psat with a peak PAE of 13.4 and 12.1%, respectively. Section 4.5 concludes this chapter.

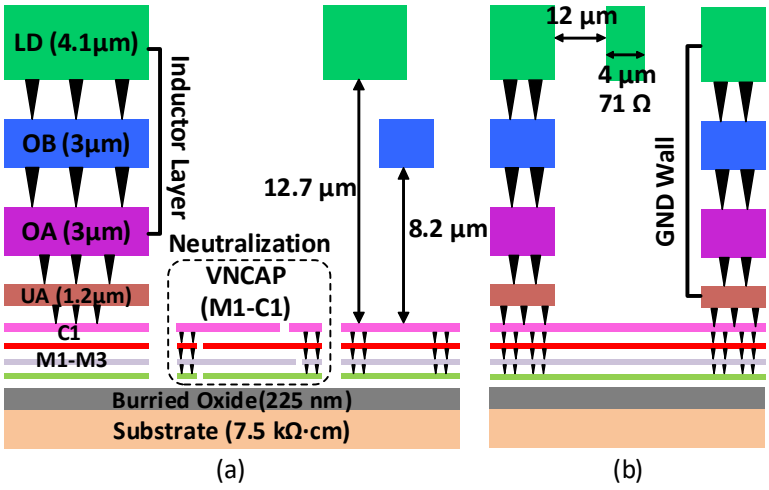


Figure 4.2: (a) GF45RFSOI technology stackup. (b) Top metal 71-Ω transmission line metal stackup.

4.2 Technology

The PAs are designed in the GlobalFoundries CMOS 45nm RFSOI (GF45RFSOI) process [Fig. 4.2(a)]. This process has eight metal-layer with three ultra-thick top-metal layers (OA-OB (Copper): 3-μm thick; LD (Aluminum): 4.1-μm thick), which are used for low-loss RF passives, including input splitter, balun, transformer and combiner. The top-metal 71-Ω transmission line structure is based on coplanar waveguide with lower ground plane (CPWG), and is 12.7 μm away from the ground plane [Fig. 4.2(b)], and with a measured insertion loss of 2 dB/mm at 140 GHz. Since the wavelength in the dielectric (λ_d) at 140 GHz is 1.1 mm, the quarter wavelength transmission line (QWL-TL) insertion loss is estimated to be 0.5 dB. Vertical natural capacitors (VNCAP) are provided and realized using metal fingers in a dense and stacked fashion with user-defined layers in the stack (M1-C1).

The differential transistor pair 3-D layout is presented in Fig. 4.3(a) using a floating-body thin-oxide RF NFET. Double-gate contact, multi-finger configuration and a relaxed-pitch layout are employed to reduce the gate resistance r_g and parasitic capacitance [39], and to improve the transistors intrinsic gain. At D-band, the transistor modelling with accuracy is critical and

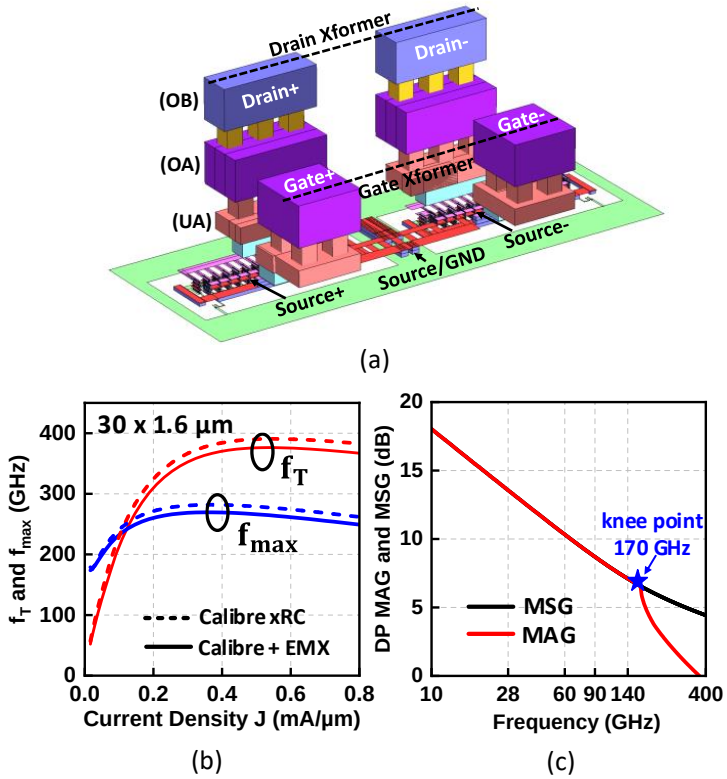


Figure 4.3: Differential transistor pair (a) 3-D layout, (b) simulated f_T and f_{max} versus bias current density and (c) MAG/MSG versus frequency.

includes two parts. First, the transistor itself with PC-M1 contacts, M1-C1 routing and vias are RC extracted using Calibre xRC. Second, the C1-OA/OB metal routing and vias are modelled by EMX, a full 3D electromagnetic simulator. For a multi-finger transistor, this methodology can simplify the EM simulation ports. After all the layout extraction, the 30×1.6 μm (30 fingers/1.6 μm per finger) transistor provides an f_T, f_{max} of 270, 350 GHz when biased at the current density of 0.3-0.4 mA/μm [Fig. 4.3(b)]. The simulated maximum stable/available gain (MSG/MAG) at 140 GHz is 6-7 dB [Fig. 4.3(c)]. The knee point occurs at 170 GHz, which means the transistor is not unconditional stable below 170 GHz due to the finite reverse isolation.

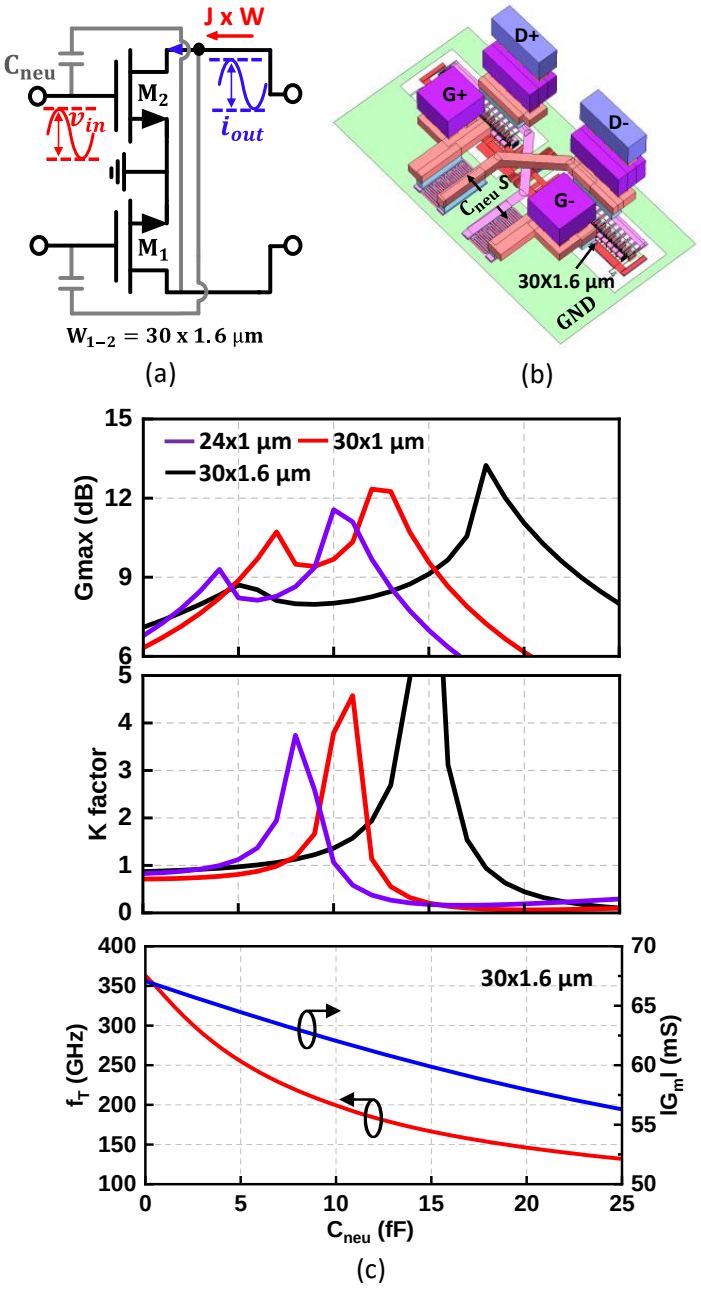


Figure 4.4: Neutralized differential pair (NDP) (a) schematic, (b) 3-D layout and (c) simulated Gmax, K factor, f_T and $|G_m|$ versus C_{neu}.

4.3 Design and Analysis

4.3.1 Neutralized Transistor Pair Analysis

The capacitive neutralization technique has been widely adopted in D-band PA design [13, 42, 62] [Fig. 4.4(a) and (b)]. It is used to decrease the knee point shown in Fig. 4.3(c) and make the neutralized differential transistor pair (NDP) unconditional stable. Also, neutralization can help increase the NDP's MAG. All amplifier stages in the PA designs are NMOS NDP with increased intrinsic gain, which reduces the input power level requirement and improves the PA overall efficiency. The simulated NDP's Gmax and K-factor for different transistor sizes are shown in Fig. 4.3. As derived in [60], the NDP's MAG when $(K > 1)$ is given by:

$$|MAG| \cong \frac{\sqrt{g_m + \left(\omega\left(C_{gd} - C_{neu}\right)\right)^2}}{\left|\omega\left(C_{gd} - C_{neu}\right)\right|\left(K + \sqrt{K^2 - 1}\right)} \tag{4.1}$$

The Gmax curve versus C_{neu} has dual peaks when $K = 1$ since the K factor relates the term in the denominator of the MAG is with the minimum value. Both 24×1 μm and 30×1 μm sizes NDP are implemented as the PAs three driver stages with 7 and 9 fF neutralization capacitors with C_{neu} values based on the NDP's stability and Gmax. A +/- 20% C_{neu} process variation is considered in the design, so the choice of the C_{neu} is in the middle of the two C_{neu} points when $K = 1$. The PA power stage size is 30×1.6 μm with 10 fF C_{neu}, which is chosen for the overall performance, including the power characteristics. A slight C_{neu} reduction helps improve the power stage linearity (0.5-1 dB increase in P_{1dB}) since the NDP's f_T and the effective transconductance G_m decrease versus C_{neu} [Fig. 4.3(c)].

4.3.2 Eight-way Common-Source Power Combined PA

The eight-way power combining (four-way differential) common source (C.S.) amplifier is implemented using four-stage differential PA (all stages with C.S structure) unit cells as building blocks. The first two stages serve as amplifier stages and are biasd at 0.17-0.18 mA/μm to save DC power consumption and improve the PA efficiency. The third is with higher bias and serves as the driver stage, for the output power stage. A conventional power combining design methodology used, and matches the power stage optimal loadline to the 50 Ω and employs λ_d/4 71-Ω transmission line in the T-combiner to realize the impedance transformation [Fig. 4.5(a)]. In our case, except for a 1:1 highly coupled balun, an extra 40 fF capacitor is used as part of the power matching. Also, the first stage 4-way combiner length is designed shorter than λ_d/4 (0.12 λ_d) and is incorporated into the power matching network together with the output balun [Fig. 4.5(b)]. This short length combiner is suitable for RF routing since the two adjacent PA unit cells are close in the layout. The power stage is biased in class A and Fig. 4.5(c) and (d) present the simulated power stage loadpull power contours and PAE contours at OP_{1dB}, respectively. The optimal loadline Z_{opt} for output power and PAE are differential (22+j32) Ω and (17+j35) Ω, respectively, which are close. The impedance transformation representations of Fig. 4.5(a) and (b) are shown in Fig. 4.5(c). The power stage output matching (reflection coefficient) S_{22}^* impedance is intrinsically close to the optimal loadlines of output power and PAE and there is no power/gain matching tradeoff. With a supply voltage of 1 V, the optimal output power and PAE at $\sim OP_{1dB}$ of both the driver and power stages are 9.2 dBm and 14.5%, respectively. Fig. 4.6(a) presents the simulated output stage transistor voltage V_{DS} and current I_{DS} swings at $\sim OP_{1dB}$ and 140 GHz. The transistor single-ended peak-peak voltage and current swings are observed to be 1.1 V and 40 mA at OP_{1dB}, respectively, and the combined node A_1 voltage peak-peak swing is simulated to be 2.4 V [Fig. 4.6(b)]. The first stage 4-way combiner EM model (3-D layout) is presented in Fig. 4.6(c). Two baluns are connected by the short TL-based combiner, resulting in a compact layout. The simulated Gmax and in-situ (loaded) insertion loss of the combiner

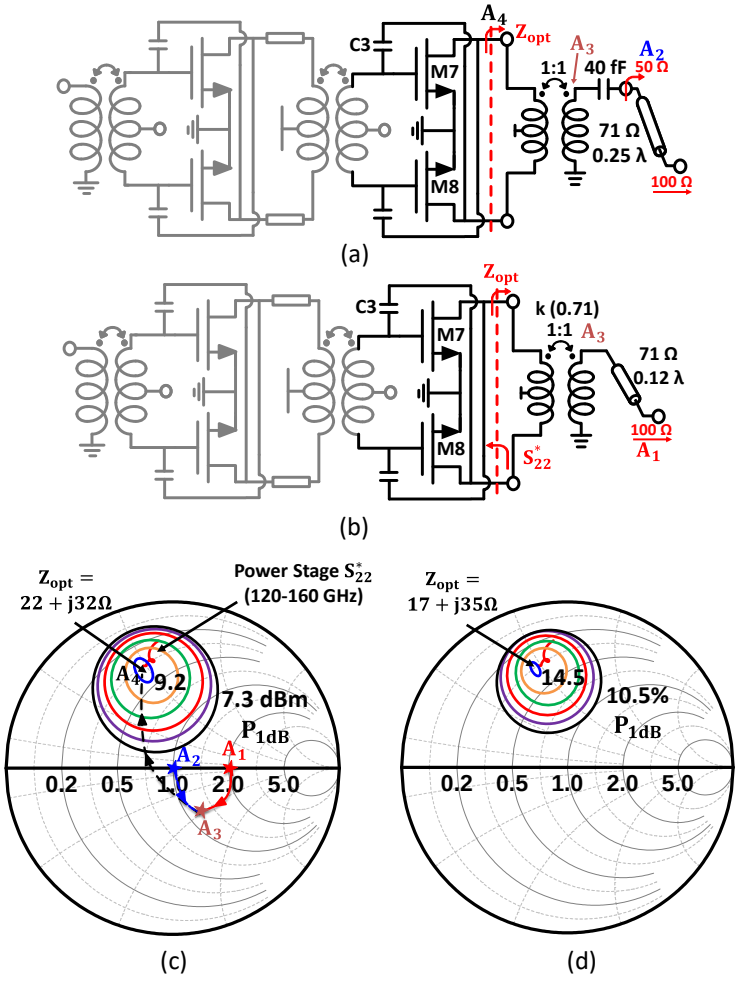


Figure 4.5: PA unit cell last stage (highlighted) schematic with (a) conventional quarter wavelength transmission line (QWL-TL) combiner and (b) highly-coupled balun-short transmission line combiner. Simulated loadpull (c) output power contours with load impedance transformation and (d) PAE contours at PA OP_{1dB}.

including the balun are only -0.7 dB and 0.9-1.2 dB, respectivley, at 130-150 GHz [Fig. 4.6(d)]. Since the second combiner is based on a $\sim \lambda_d/4$ transmission lines, the estimated ohmic loss is 0.5 dB and the combiner total ohmic loss is 1.5 dB at 140 GHz including the balun loss.

All the PA interstage matching networks are designed using transformers for compact layout and low loss. Fig. 4.7 presents the asymmetric transformer with intermediate-k before the last stage. A stacked structure transformer, with the help of small inductors Ls in series with

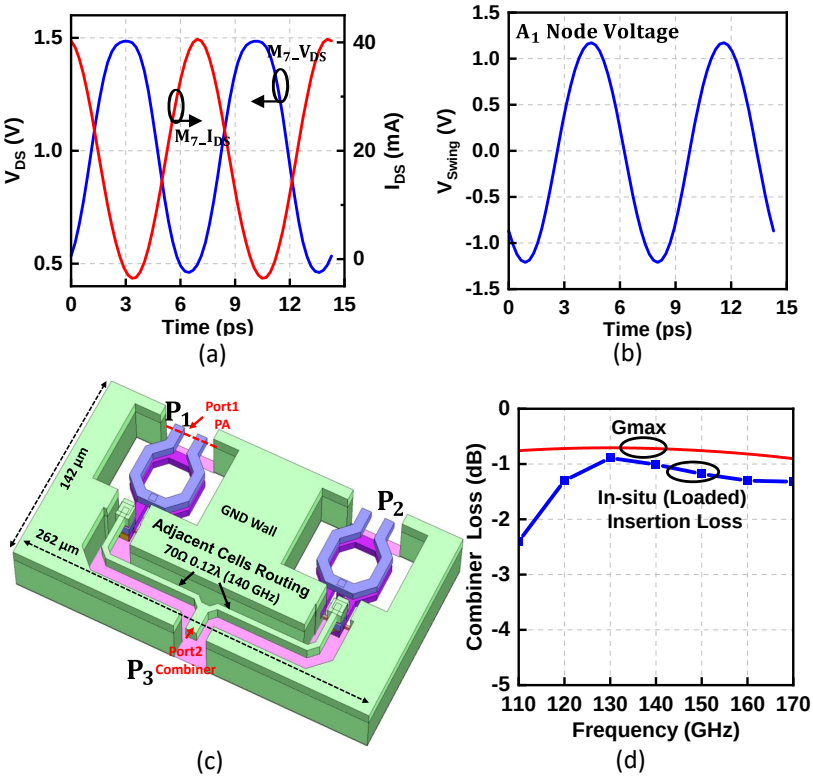


Figure 4.6: Simulated (a) transistor M7 (power stage) voltage and current swings and (b) combined node A_1 voltage swing. 4-way combiner (conneting two adjacent PA unit cells) (c) 3-D layout (EM model) and (d) simulated Gmax and in-situ (loaded) gain.

the driver drains, is employed to realize the wideband impedance transformation for conjugate matching [Fig. 4.7(b)]. The transformer 3-D layout is presented in Fig. 4.7(c) with a simulate Gmax and loaded gain of 1.3-1.5 dB and 1.8-1.9 dB, respectively, at 130-160 GHz [Fig. 4.7(d)].

Each stage of the PA is designed almost at the same center frequency [Fig. 4.8]. The last two stages gains are relatively flat versus frequency so that the PA is with wideband power performance.

4.3.3 Eight-Way Cascode Power Combined PA

Typically, the PA based on the cascode topology has higher OP_{1dB} and Psat since the supply voltage is doubled, resulting in larger available voltage swing at the output. However, at

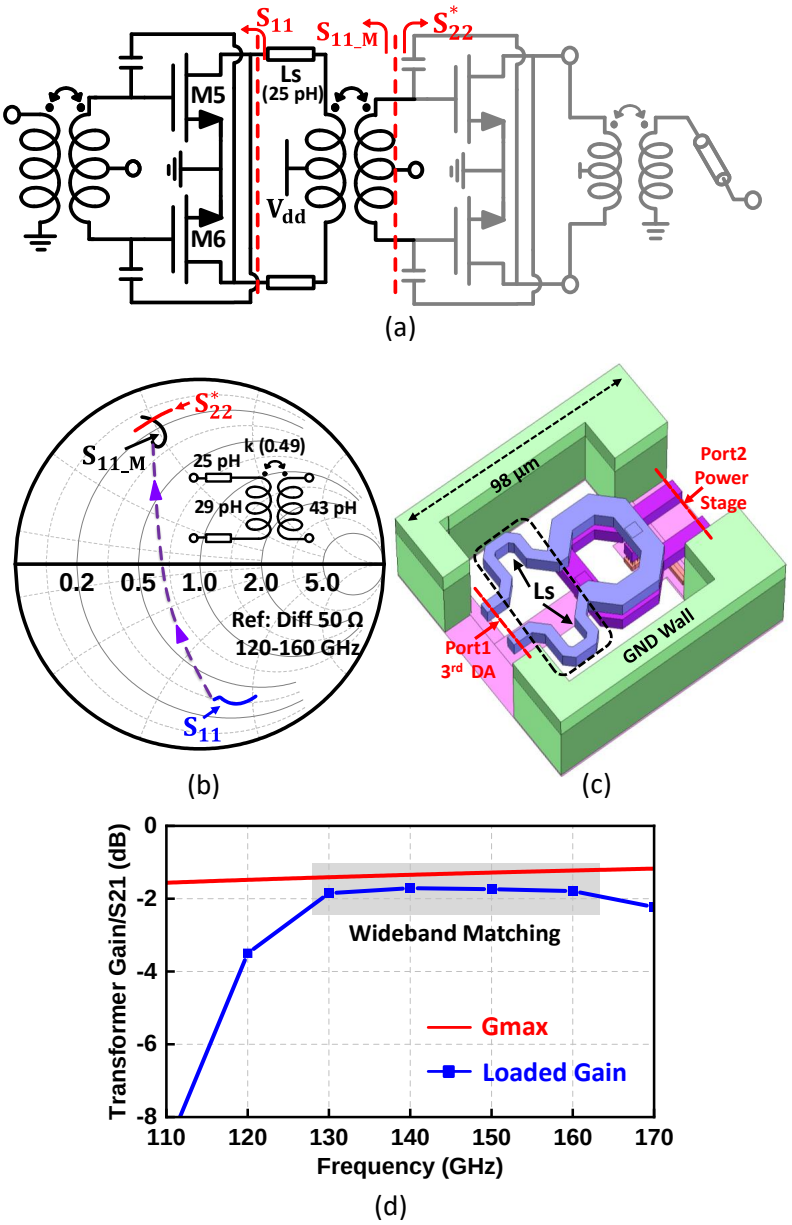


Figure 4.7: (a) PA unit cell driver stage (highlighted) schematic. Interstage transformer (b) equivalent model and impedance transformation, (c) 3-D layout and (d) simulated Gmax and loaded gain.

D-band, the cascode stage is struggle to achieve enough gain, especially in CMOS [86, 87], which means the input power level requirement from the driver stage should be improved simultaneously. However, this will lead to the design challenge in the driver design and low efficiency of the PA.

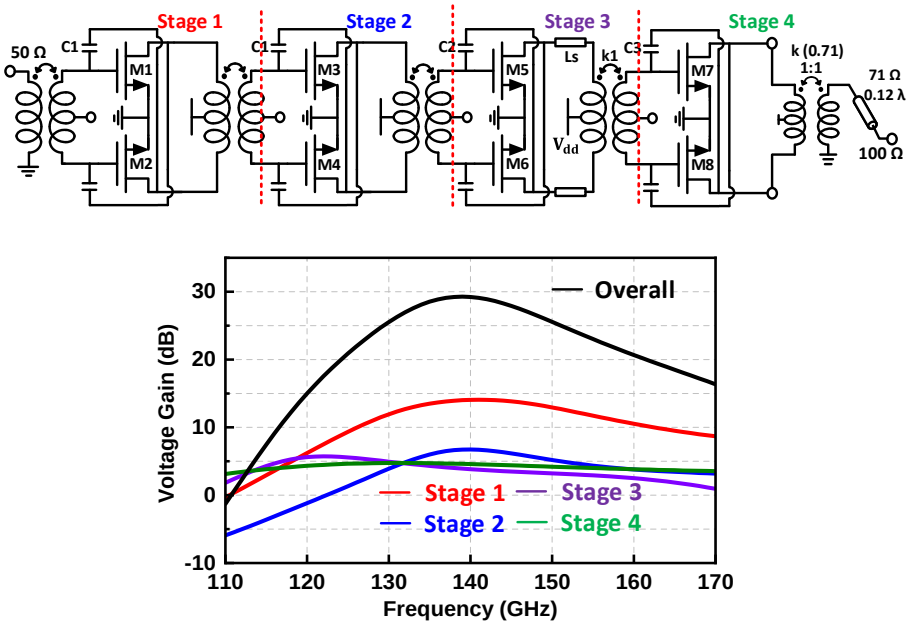


Figure 4.8: Simulated 4-stage PA unit cell voltage gain distribution.

Therefore, gain-boosting techniques are necessary in the D-band cascode PA design, which have been adopted and implemented in the prior art at lower frequency [88, 89].

Fig. 4.9(a) presents the cascode power stage simplified half circuit small-signal model. Assuming the gate and series inductor L_1 and L_2 are equals to 0, when the parasitic capacitors C_{p1} and C_{p2} exist at the C.S drain/C.G source nodes, part of the C.S drain current i_{CS} will flow into C_{p1} and C_{p2} as

$$\frac{i_{CG}}{i_{CS}} = \frac{g_m}{\sqrt{g_m^2 + (\omega(C_{p1}+C_{p2}))^2}} \tag{4.2}$$

The parasitic capacitance C_p $(C_{p1}+C_{p2})$ will greatly degrade the current conversion gain of i_{CG}/i_{CS}. To resonate out the C_p and suppress the gain compression effect, a series inductor L_1 is implemented between the C.S. and C.G. transistors. The current conversion gain A_i can be derived as

$$A_i = \frac{g_m}{\sqrt{g_m^2(1-\omega^2 L_1 C_{p1})^2 + \omega^2(C_p - \omega^2 L_1 C_{p1} C_{p2})^2}} \tag{4.3}$$

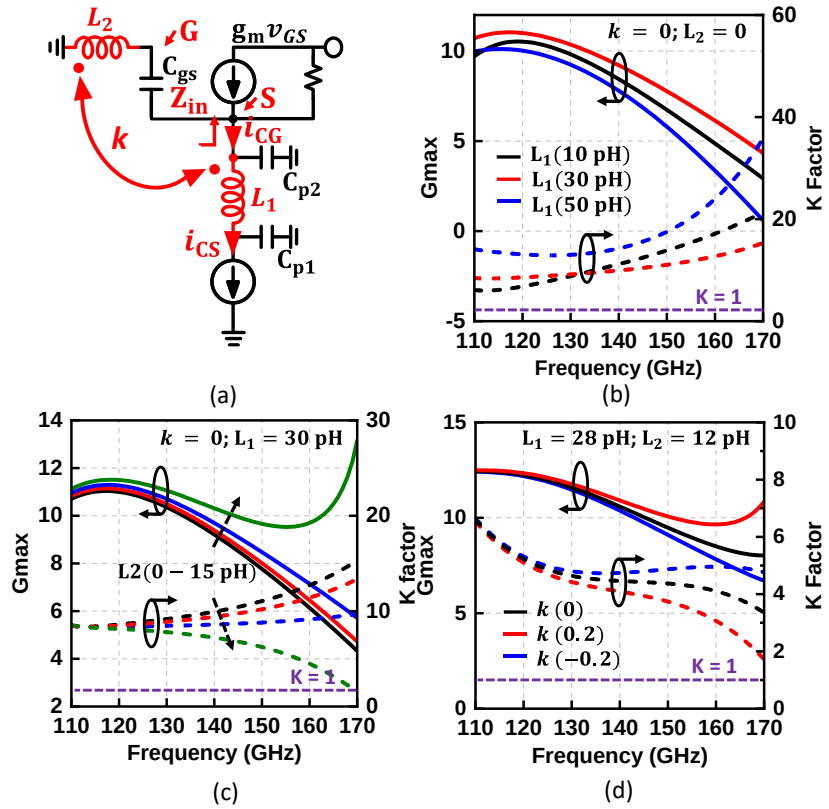


Figure 4.9: Cascode PA last stage (a) half circuit small-signal model. Simulated Gmax and K factor versus (b) cascode inductor (L_1), (c) common gate transistor gate inductor (L_2) and (d) the coupling coefficient k between L_1 and L_2.

When the denominator of A_i reaches the minimum, the current conversion gain A_i becomes the maximum, which helps improve the cascode stage intrinsic gain. Under this condition, the optimal L_1 is

$$L_1 = \frac{g_m C_{p1} + \omega^2 C_{p1} C_{p2} (C_{p1} + C_{p2})}{\omega^2 C_{p1}^2 (\omega^2 C_{p2}^2 + g_m)} \tag{4.4}$$

Fig. 4.9(b) presents the simulated Gmax and K factor of the cascode stage at different L_1 values with transistor $W = 30 \sim 1.6 \mu$m and biased at 0.37 mA/μm. The optimal cascode stage Gmax is simulated to be 9.2 dB at 140 GHz and achieved when $L_1 = 30$ pH. As indicated by (4.4), too large or small L_1 will degrade the cascode stage intrinsic gain performance.

An extra small inductor L_2, implemented at the C.G. transistor gate node, is used to boost

the cascode stage gain [88, 89]. The C.G. transistor gate and source nodes voltages relationship is calculated as [89]

$$V_G = \frac{-\omega^2 L_2 C_{gs}}{1-\omega^2 L_2 C_{gs}} V_S \tag{4.5}$$

The C.G. transistor gate-source voltage V_{GS} is boosted when node voltages V_G and V_S are out-of-phase, resulting in increased transconductance and then overall cascode stage gain. This happens when the denominator $(1-\omega^2 L_2 C_{gs})$ is larger than 0, which means $L_2 < 1/(\omega^2 C_{gs})$. Given that $L_1 = 30$ pH, the simulated Gmax at different L_2 values is presented in Fig. 4.9(c). At 140 GHz, the gain increases from 9.2 to 9.8 dB when L_2 increases from 0 to 12 pH. However, when L_2 is up to 15 pH, even though the gain increases a lot with wideband performance, the cascode stage K factor decreases quickly to be lower than 1 at 140-160 GHz, since the real part of the C.G. equivalent input impedance Z_{in} looking into its source node becomes negative [88, 89].

Usually, L_1 and L_2 are close in the layout for a differential cascode amplifier stage. Therefore, they will couple to each other and affect the stage gain and stability performances. Fig. 4.9(d) investigates the effects of different coupling coefficient k between L_1 and L_2. A slight negative coupling help with the cascode stage stability while maintain its gain. The cascode PA power stage schematic and layout are presented in Fig. 4.10(a) and (b), respectively. The inductor L_1 and L_2 are with a slight negative coupling. All the passives of the cascode stage, including inductors and the stacked balun, are EM modelled together for accuracy. Fig. 4.10(c) and (d) present the power and PAE contours at 140 GHz and OP_{1dB}. The simulated optimal loadline Z_{opt} for power and PAE are differential (17.5+j47.5) Ω and (18.5+j45) Ω, respectively. The optimal power and PAE level of the single cascode stage are simulated to be 12.1 dBm and 15.4%. Transient voltage swings of the C.S. transistor drain node A and the C.G. transistor source and drain nodes B and C are simulated and presented in 4.10(e). The single-ended peak-peak voltage swing of output node C is 1.8 V (supply voltage: 2.4 V).

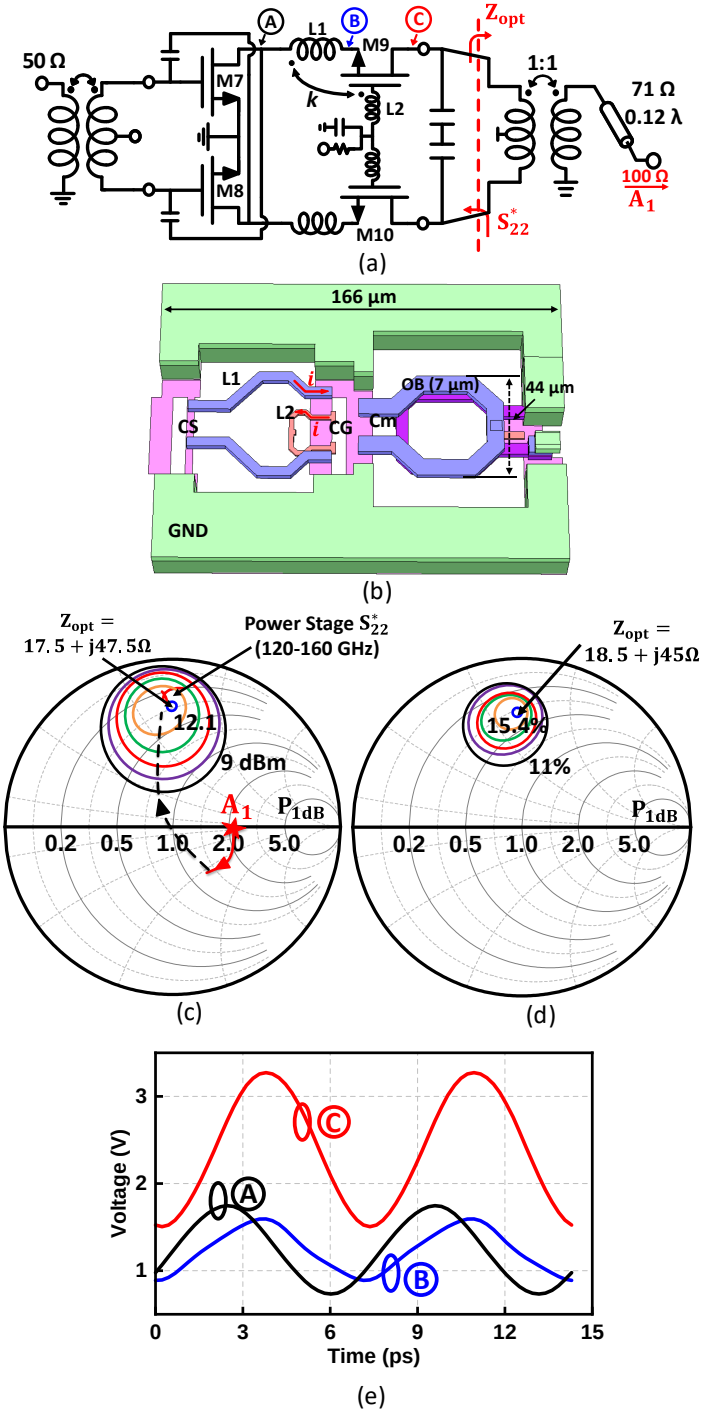


Figure 4.10: Cascode PA last stage (a) schematic and (b) 3-D compact layout. Simulated loadpull (c) output power contour and (d) PAE contour. (e) Simulated node A, B, C transient voltage swings.

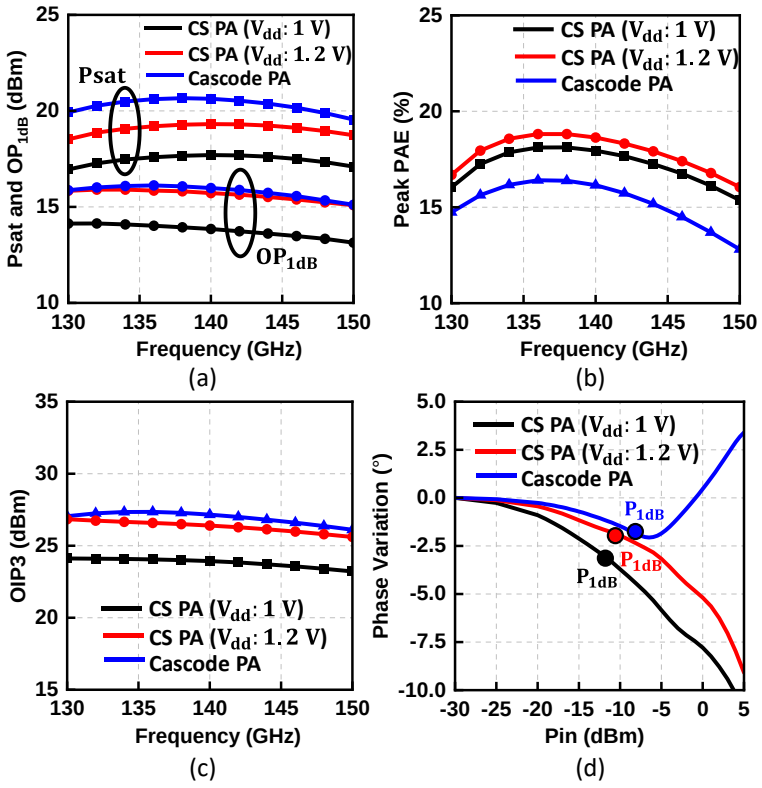


Figure 4.11: Simulated PA performance versus frequency at room temperature. (a) Saturated output power and output 1-dB compression. (b) Peak PAE. (c) Output third order intercept point. (d) AM-PM distortions.

4.3.4 PA Simulations

Fig. 4.11 presents the simulated PA performance for the two variants. The Psat and OP_{1dB} for the C.S. PA are simulated to be 18.5-19.3 dBm and 15.1-15.8 dBm, respectively, at 130-150 GHz, with a corresponding peak PAE of 16.8-18.8% (supply voltage: 1.2 V). For the cascode PA, the Psat and OP_{1dB} are simulated to be 19.6-20.6 dBm and 15.2-16 dBm, respectively, at 130-150 GHz, with a corresponding peak PAE of 12.8-16.4% (supply voltage: 2.4 V). The simulated OIP3 is $\sim$ 10-11 dB higher than OP_{1dB} for both PA implementations, and the AM-PM distortions are less than 4° even up to OP_{1dB} due to the class A bias and its soft compression characteristic.

Fig. 4.12 presents the simulated performance at 140 GHz of two PA variants versus

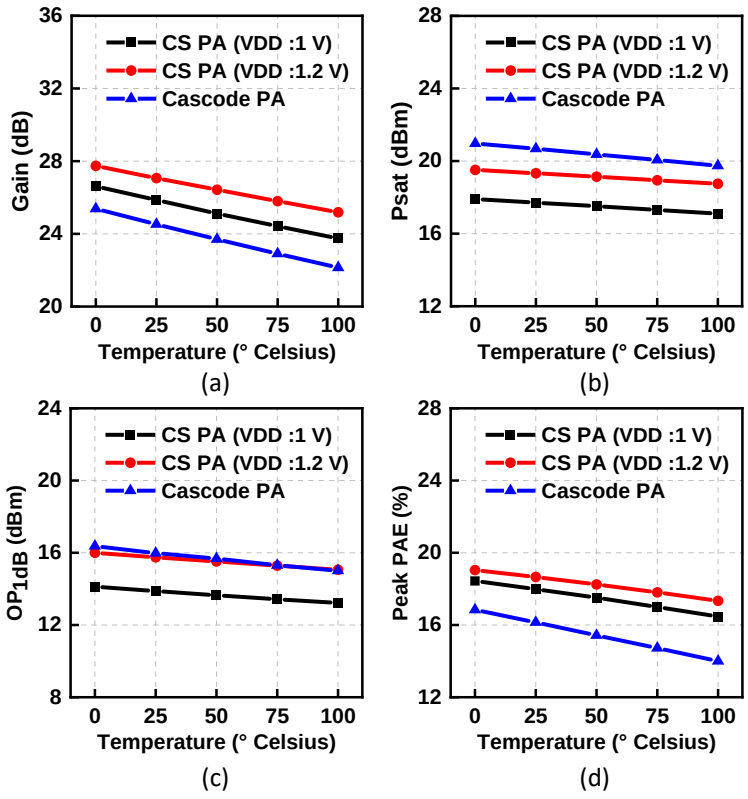


Figure 4.12: Simulated PA performance versus substrate temperature at 140 GHz. (a) Gain. (b) Peak PAE. (c) Saturated output power. (d) Output 1-dB compression point.

temperature. A temperature increase from 0 to 100°C also leads to Psat and OP_{1dB} drop of 1.3-1.4 dB which is expected at these frequencies.

4.4 Measurements

4.4.1 Small Signal Measurements

The eight-way power-combined PAs are implemented in the GlobalFoundries 45nm RFSOI process [Fig. 4.13]. The small-signal measurements are performed using GSG on-chip probing. A Keysight E8364B 50-GHz vector network analyzer (VNA) outfitted with Keysight mm-

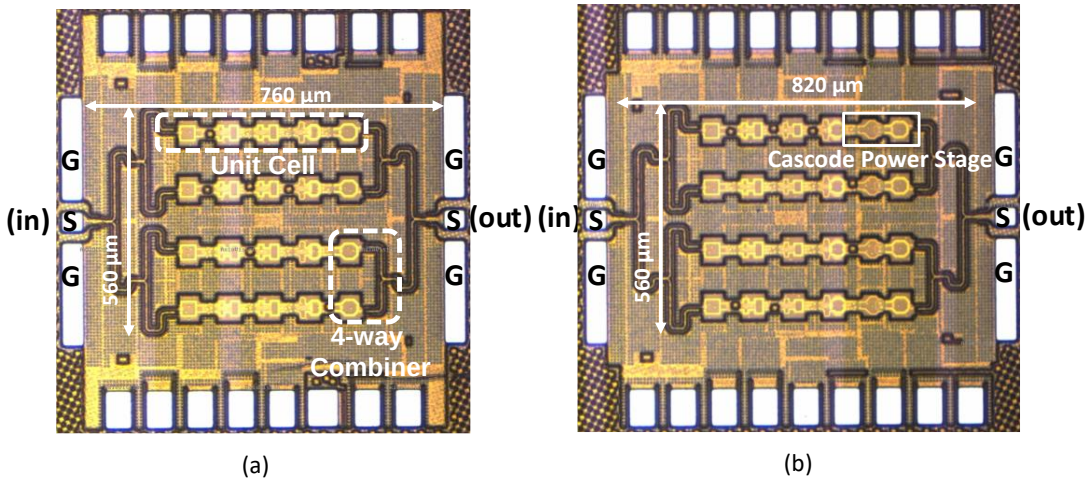


Figure 4.13: Chip micro-photographs of (a) eight-way C.S. power combined PA (core size: 0.43 mm^2), and (a) eight-way cascode power combined PA (core size: 0.46 mm^2)

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Wave head controllers and OML WR-6 waveguide extender modules were used for measurements from 110-170 GHz. On-chip TRL cells are used for the calibration and the measurement reference planes are the interfaces between the input/output GSG pads and the PA circuits (GSG pad loss is not included in the measurements). Fig. 4.14 presented the measured S-parameters and K factors of both PA variants. The eight-way C.S. PA has a peak S_{21} of 24 dB at 134 GHz with a 3-dB bandwidth of 130-151 GHz. The in-band gain ripple is +/- 1 dB. Both input and output reflection coefficients S_{11} and S_{22} are $<$ -10 dB across the bandwidth. The eight-way cascode PA measured peak S_{21} is 24.8 dB at 135 GHz with a 3-dB bandwidth from 133-148 GHz. Also, both input and output reflection coefficients S_{11} and S_{22} are $<$ -10 dB across the bandwidth. In both variants, compared to the simulations, the peak gain has 2-3 dB drop probably due to the underestimated gate resistance and capacitive parasitics of the device models and the metal-fill effects on the passive structures.

The probed K-factor measurements at D-band of two PA variants are presented in Fig. 4.14(c). Both PAs demonstrate $K > 1$ over the entire D-band frequency range suggesting that

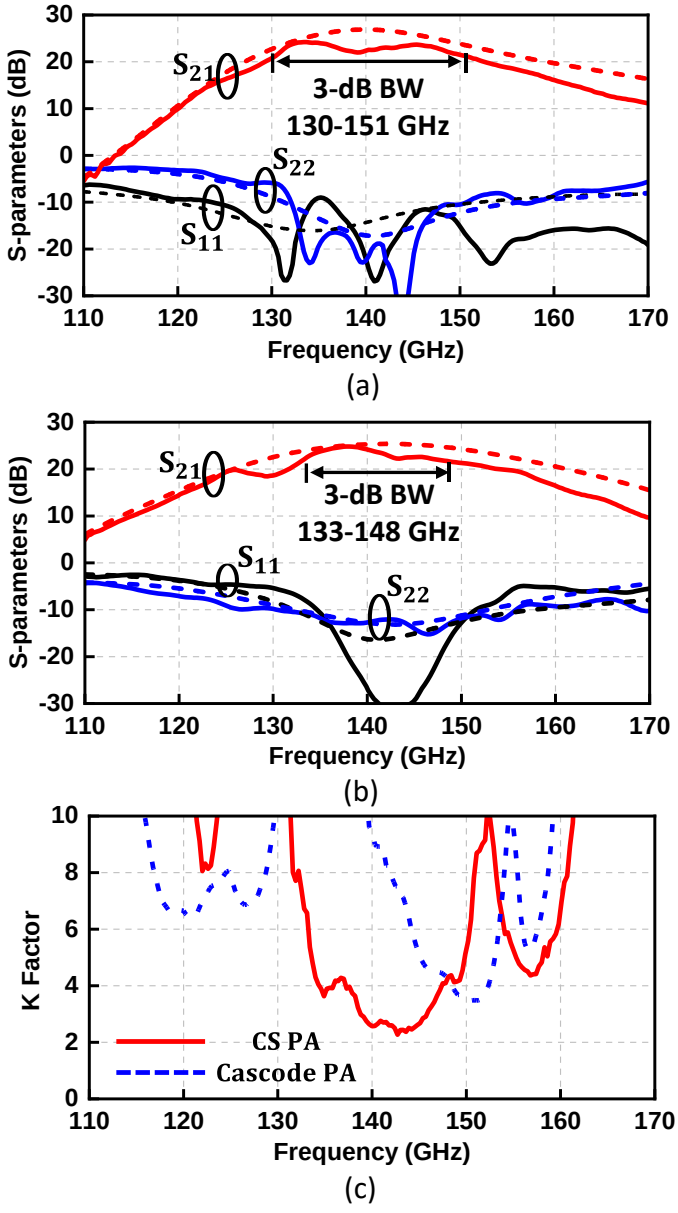
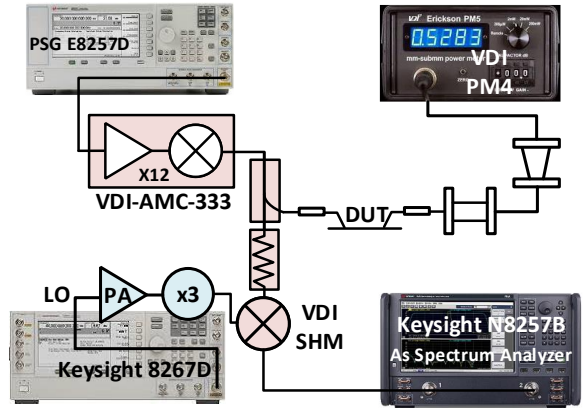
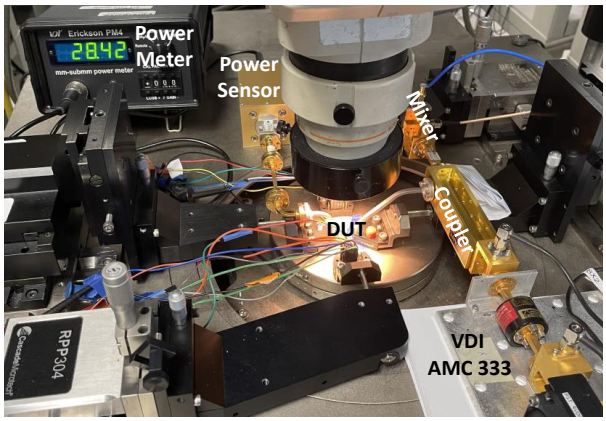


Figure 4.14: Measured and simulated S-parameters of the (a) eight-way C.S. power combined PA and (b) eight-way cascode power combined PA. (c) Measured K-factor of both PA variants.

they will be stable when integrated into a larger IC, such as a full transceiver system.



(a)



(b)

Figure 4.15: PA large-signal measurements (a) setup and (b) setup photograph.

4.4.2 Large Signal Measurements

Fig. 4.15 presents the setup for large signal measurements. The loss of attenuator, mixer and cable are de-embedded to calculate the PA input power level P_{in}. The WR6 probe loss is also measured using a back-to-back configuration and small-signal measurement setup and is $\sim$ 2.5 dB at 140 GHz. Similar to the small-signal measurement, the PA input/output power are calibrated to the PA circuits. Pads losses are de-embedded.

Large-signal measurements versus input power P_{in} are presented in Fig. 4.16. At 130/140 GHz, the eight-way C.S. PA ($V_{dd} = 1.2V$) achieves a peak Psat, OP_{1dB} of 17.3/17.5 dBm and

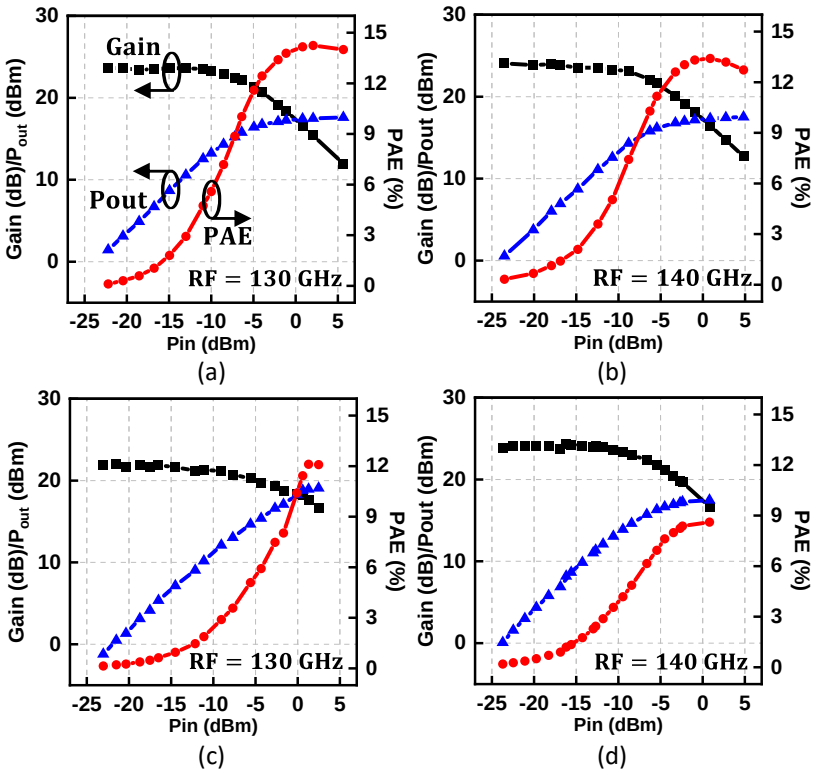


Figure 4.16: Measured gain, output power, and PAE versus input power for eight-way C.S. power combined PA at (a) 130 GHz and (b) 140 GHz, and eight-way cascode power combined PA at (c) 130 GHz and (d) 140 GHz.

13.2/14.2 dBm, respectively. The corresponding peak PAE and PAE at OP_{1dB} are 14.2/13.4% and 5.7/7.5%. The eight-way cascode PA has a peak Psat, OP_{1dB} of 19/17.5 dBm and 13/14.6 dBm, respectively. The corresponding peak PAE and PAE at OP_{1dB} are 12/8.7% and 3.7/4.9%.

The large-signal performance versus RF frequency are presented in Fig. 4.17. For the eight-way C.S. PA with a 1.2 V supply, Psat, OP_{1dB} and peak PAE are 16.8-17.5 dBm, 13.2-14.3 dBm and 11.2-14.2%, respectively, at 130-150 GHz. For the eight-way cascode PA with a 2.4 V supply, Psat, OP_{1dB} and peak PAE are 16.3-19 dBm, 12.8-14.8 dBm and 6.4-12.1%, respectively, at 125-150 GHz. The OP_{1dB} levels remain relatively constant with +/- 1 dB ripple, while the cascode PA P_{sat} drops at 140-150 GHz, resulting in lower peak PAE. This is probably due to the

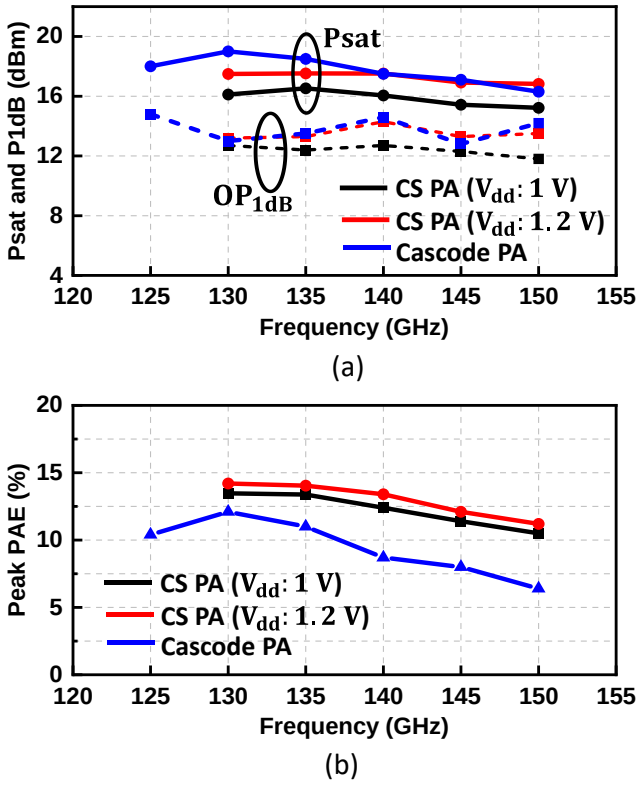


Figure 4.17: Measured Psat, OP1dB, and peak PAE versus frequency for (a) eight-way C.S. power combined PA and (b) eight-way cascode power combined PA.

slight gain drop, especially at the last cascode power stage.

The PA AM-PM distortion and OIP3 measurements are conducted using the setup presented in Fig. 4.18(a). Since the PA input P_{1dB} and IIP3 are $\sim$ -10 and 0 dBm (estimated), respectively, an external high linearity, high gain and narrowband PA (135-145 GHz) from VDI is placed right after the input subharmonic mixer (linearity limited) to make sure that the on-chip PA has enough input power level and dominates the whole setup linearity. A PNA-X (Keysight N8257B) is used to measure the S_{21} at the IF band for PA AM-AM and AM-PM distortion measurements. For PA OIP3 measurements, two tones (100 MHz span) at the IF band are generated from the PNA-X and feed the input mixe. The setup IIP3, including the on-chip PA under test

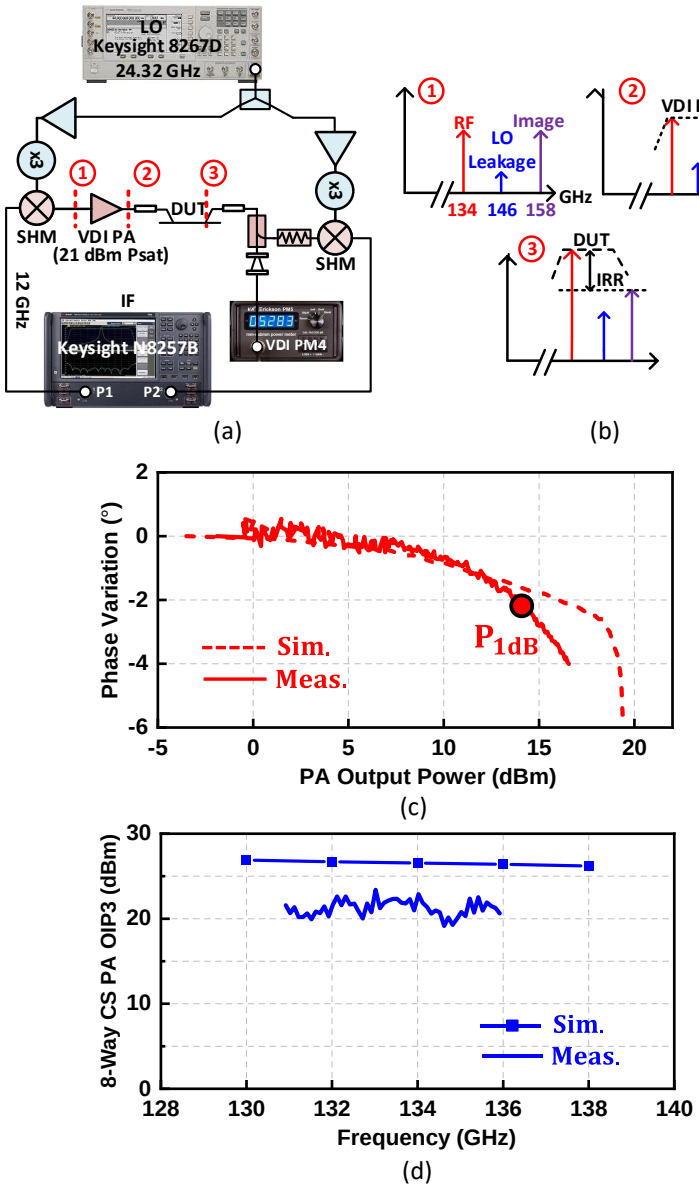


Figure 4.18: (a) Measurement setup for the PA AM-PM distortion and output third order intercept point (OIP3). (b) Frequency spectrum for RF, image and LO leakage. Eight-way C.S. power combined PA measured and simulated (c) AM-PM distortions and (d) OIP3.

(DUT), is measured and the PA OIP3 can be calculated as

$$OIP3_{DUT} = IIP3_{Setup} + G_{node_{3-P1}} \tag{4.6}$$

Table 4.1: Performance Comparison of D-band Power Amplifiers in CMOS and SiGe Part I

Ref.	Frequency (GHz)	Technology	Topology	VDD (V)	3-dB BW (GHz)
This work	**140**	**45-nm CMOS SOI**	**8-Way C.S. (4-Way Diff.)**	**1/1.2**	**130-151**
This work	**135**	**45-nm CMOS SOI**	**8-Way Cascode (4-Way Diff.)**	**2.4**	**133-148**
[13]	135	16-nm FinFET	4-Way C.S.	0.8/1	110-128
[62]	140	40-nm CMOS	4-Way C.S.	1	125-142
[42]	118	65-nm CMOS	4-Way C.S.	1.2	114-131
[82]	140	40-nm CMOS	8-Way C.S.	1	120-150
[83]	133	40-nm CMOS	Single-Way C.S.	1.1	125-138
[84]	128	45-nm CMOS SOI	Single-Way Cascode	4.4	128-150
[75]	130	90-nm SiGe	4-Way Cascode	4	110-145
[76]	116	90-nm SiGe	4-Way C.S.	1.6	110-134
[77]	120	90-nm SiGe	8-Way Cascode	3.7	107-142
[78]	135	90-nm SiGe	2-Way C.S.	2.2	114-131
[79]	133	130-nm SiGe	16-Way C.S.	1.1	75-157.4
[80]	160	130-nm SiGe	Single-Way Cascode	4	130-180
[81]	140	130-nm SiGe	Single-Way Cascode	3.3	110-170

where $G_{node_{3-P1}}$ is the conversion gain from PNA-X port 1 to node 3 shown in Fig. 4.18(a), with node 3 being the plane between the on-chip GSG pad and the PA circuits.

Fig. 4.18(b) presents the frequency spectrum of different nodes in the setup. For example, assuming an input IF signal at 12 GHz, a $\times 6$ LO signal at 146 GHz, the upconverted RF and image signal are at 134 and 158 GHz, respectively. At node 1, they are with almost equal power level but due to the external VDI PA narrowband performance, the image rejection ratio (IRR) at node 2 improves. Moreover, another IRR increase occurs in the PA chip under-test due to its

Table 4.2: Performance Comparison of D-band Power Amplifiers in CMOS and SiGe Part II

Ref.	Gain (dB)	Psat (dBm)	OP1dB (dBm)	Peak PAE (%)	Area (mm^2)	FoM[c]
This work	**22.2/24**	**16/17.5**	**12.5/14.2**	**12.5/13.4**	**0.43**[a]	**92.2/95.7**
This work	**24.8**	**18.5**	**13.5**	**11**	**0.46**[a]	**96.3**
[13]	19/20.5	13.1/15	7.1/9.2	11/12.8	0.062/0.041[b]	85.1/89.2
[62]	20.3	14.8	10.7	8.9	0.125[a]	87.5
[42]	22.3	14.5	12.2	10.2	0.103[a]	88.3
[82]	15	13.2	9.9	14.6	0.38	82.8
[83]	16.8	8.6	6.8	7.4	0.3/0.11[a]	76.6
[84]	9.4	13.2	-	2.8	-	69.2
[75]	18.2	21.9	18.6	12.5	1.7	93.3
[76]	20	20.8	17	7.6	5	90.9
[77]	7.7	22	16	3.6	0.62	76.8
[78]	22.4	19.3	18.5	13	0.26	95.4
[79]	18	19.3	16.6	8.8	0.71[a]	89.2
[80]	27	14	12.5	5.7	0.49	92.6
[81]	21	12.1	10	5	0.19	83

[a]Core Size. [b]exclude RF pads. [c]FoM = Gain [dB]+Psat [dBm]+20*log(Fc (GHz))+10*log(peak PAE (%)).

tuned response (node 3). There is enough IRR to ensure that the PA linearity performance is not affected by the unwanted image signal.

Fig. 4.18(c) and (d) present the measured eight-way C.S PA AM-PM distortion and OIP3. The measured AM-PM distortion is less than 2.5° at OP_{1dB} at 134 GHz. The measured PA OIP3 is 22-23 dBm at 131-136 GHz, which is $\sim$ 3 dB less than simulations, and could be due to residual IP3 contribution from the setup.

Fig. 4.19 and tabel 4.1 and 4.2 summarize the CMOS D-band PAs in this work and compares with the state-of-the-art D-band CMOS and SiGe PAs. The 45RFSOI PAs demonstrate the highest reported Psat, OP_{1dB} and gain in CMOS processes, and some of the highest FoM at

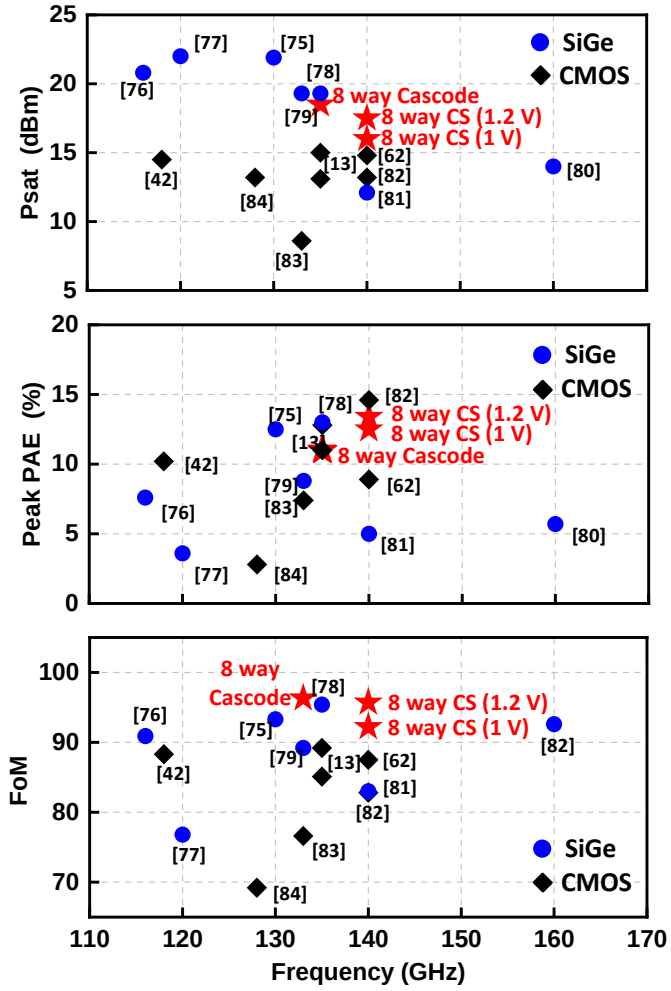


Figure 4.19: Performance comparison with previously published works at D-band in silicon.

these frequencies in both CMOS and SiGe processes. The FoM is previously defined in [13, 62]. The eight-way C.S. PA also demonstrates PAE which is comparable to the best published results using SiGe and CMOS technologies.

4.5 Conclusion

Eight-way common source and cascode combined PAs with high output power, linearity and efficiency utilizing ultra-low loss power combining techniques have been demonstrated in GF 45nm RFSOI process. The eight-way C.S. PA achieves a Psat of 17.5 dBm and peak PAE of 13.4%, while the eight-way cascode PA achieves a Psat of 19 dBm and peak PAE of 12.1%. To the author's knowledge, compared to the state-of-the-art, these PAs achieve highest Psat, P_{1dB} and gain as well as high efficiency in CMOS processes. Also, these PAs have highest FoM in silicon (both CMOS and SiGe). They are suitable to be used as part of D-band transceivers, due to their wideband high linearity and efficiency.

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Chapter 4, in part, is a reprint of the material as it appears in: S. Li and G. M. Rebeiz, "A 130-151 GHz 8-Way Power Amplifier with 16.8-17.5 dBm Psat and 11.7-13.4% PAE Using CMOS 45nm RFSOI," *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Atlanta, GA, USA, 2021, pp. 115-118, doi: 10.1109/RFIC51843.2021.9490507. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in full, has been submitted for publication of the material as it may appear in: S. Li and G. M. Rebeiz, "Design of D-Band Multi-Way Combined Power Amplifiers with 19-dBm Psat and 12% Peak PAE in 45-nm CMOS RFSOI", in *IEEE Journal of Solid-State Circuits*, submitted. The dissertation author was the primary investigator and author of this paper.

Chapter 5

Conclusion and Future Work

5.1 Dissertation Summary

At D-band in the mm-Wave spectrum, especially for wireless applications, the free space path loss (FSPL) is severe. To overcome the space loss and maintain a high link budget over a wide angular region at 140 GHz, high performance phased-array systems are desired. Also, in order to improve the system integration level and lower their cost, designs based on advanced CMOS processes are preferable.

This dissertation presented transmit and receive wafer-scale phased-array systems utilizing IF beamforming architecture for D-band applications, such as short-range communications with large data capacity (AR/VR, wireless backhaul), imaging and radar sensing. All the chips are developed in a CMOS SOI process with on-chip antenna feeds, and operate with high performance (NF, EIRP and data rates). The dissertation also presented high output power and efficiency CMOS PAs at D-band as the front-end circuits for D-band transmitters or phased-array transmitters. These works pave the pay of high performance and low cost phased-array systems in CMOS for beyond 5G/6G sub-THz communication.

In chapter 2, a 140-GHz 8-element wafer-scale phased-array receiver with an IF beam-

forming architecture and having very low RMS phase and gain errors was presented. The phased-array receiver achieves 7 dB system noise figure (NF) on average when referenced to the channel input by implementing a low-noise RF front-end design. Its noise model is analyzed in detail and the neutralization technique is implemented and useful to reduce the NF at D-band in CMOS processes. The array can receive 16 and 64-QAM waveforms at all scan angles and data rates up to 10 Gbps. To the authors best of knowledge, this is the first wafer-scale phased-array receiver with lowest noise figure at 140 GHz in silicon.

Besides the phased-array receiver, phased-array transmitter with high EIRP are also required to demonstrate a wireless link at D-band. In chapter 3, a 136-147-GHz 8-element wafer-scale phased-array transmitter with an IF beamforming architecture and having very low RMS phase and gain errors was presented. The phased-array transmitter achieves 32 dBm peak EIRP and 28 dBm EIRP at OP_{1dB}, respectively. The array can transmit 16 and 64-QAM waveforms at all scan angles and data rates up to 16 Gbps with 22-25 dBm EIRP (3-6-dB backoff from P_{1dB}). To the authors best knowledge, this is the first wafer-scale phased-array transmitter with highest EIRP at 140 GHz in silicon.

As an important block in transmitter designs, power amplifiers are important and challenging. In the prior art, CMOS-based power amplifier (PA) designs are usually with low output power, efficiency and gain due to the limited process f_T, f_{max} and breakdown voltage of the MOS transistors. However, in the advanced CMOS SOI process Global Foundries 45nm RFSOI, due to its excellent passives performances, a multi-way combiner network has been designed with a very low loss and compact layout, which makes the power combining a good approach to improve the PA output linear power while maintaining high efficiency. In chapter 4, eight-way common source and cascode combined PAs with high output power, linearity and efficiency utilizing ultra-low loss power combining techniques have been demonstrated in GF 45nm RFSOI process. The eight-way C.S. PA achieves a Psat of 17.5 dBm and peak PAE of 13.4%, while the eight-way cascode PA achieves a Psat of 19 dBm and peak PAE of 12.1%. To the author's

knowledge, compared to the state-of-the-art, these PAs achieve highest Psat, P_{1dB} and gain as well as high efficiency in CMOS processes. Also, these PAs have highest FoM in silicon (both CMOS and SiGe). They are suitable to be used as part of D-band transmitters or full transceivers, due to its wideband high linearity and efficiency.

5.2 Future Work

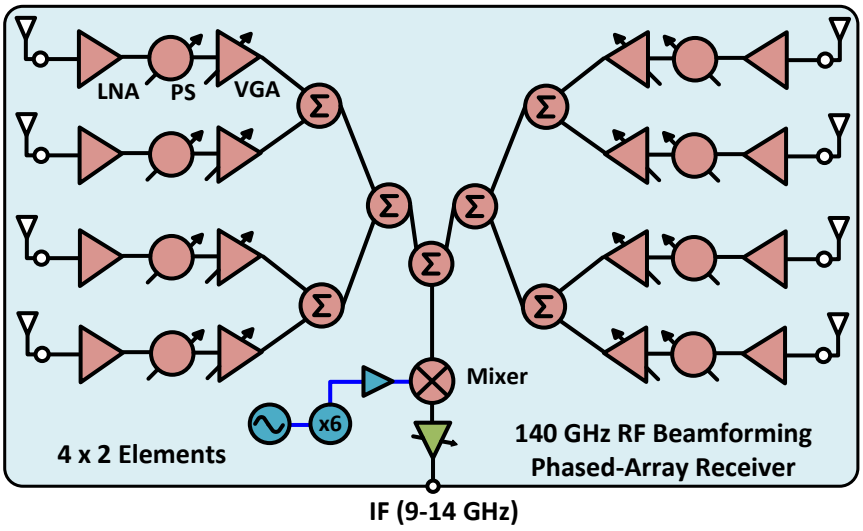
The D-band phased-array systems and PAs presented in this dissertation may be expanded and improved in a few aspects:

1) For the array beamforming architecture (see Fig. 5.1), the arrays presented in this dissertation employed the high-IF beamforming for low beamformer gain variation and gain and phase errors. To build a large-scale (64- or 256-elements) phased-array systems at D-band, RF beamforming architecture is also a candidate. TX and RX can be integrated together, and the chip size and total power consumption per element might be optimized and reduced, compared to the current version.

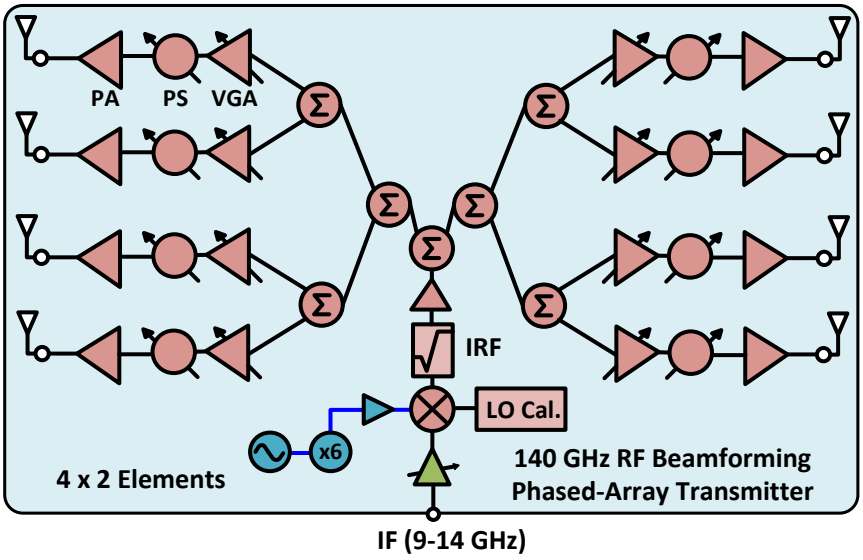
2) For the on-chip antenna, to resolve the surface wave issue, there are two solutions. One is to use a cavity antenna, but this is hard to build at 140 GHz (more investigations are needed in the future). Another solution is to use a 50-μm thick quartz superstrate at the expense of antenna bandwidth and a bit of efficiency reduction. Future work will employ 50-μm quartz superstrate for the wafer-scale on-chip antenna.

3) For both RX and TX arrays, PLLs (phase-locked loops) with low phase noise and high-IF in-phase quadrature (I/Q) up- or downconverters can be designed and implemented on chip. This will improve the systems integration level.

4) For the D-band PAs, more efficient power combining techniques, including multi-device stacking and power stage transistors sizing, can be investigated and possibly employed to further improve the PA performance. Also, the PAs' size can be reduced with more compact layout.



(a)



(b)

Figure 5.1: Block diagrams of 140 GHz RF beamforming phased-array (a) receiver and (b) transmitter.

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