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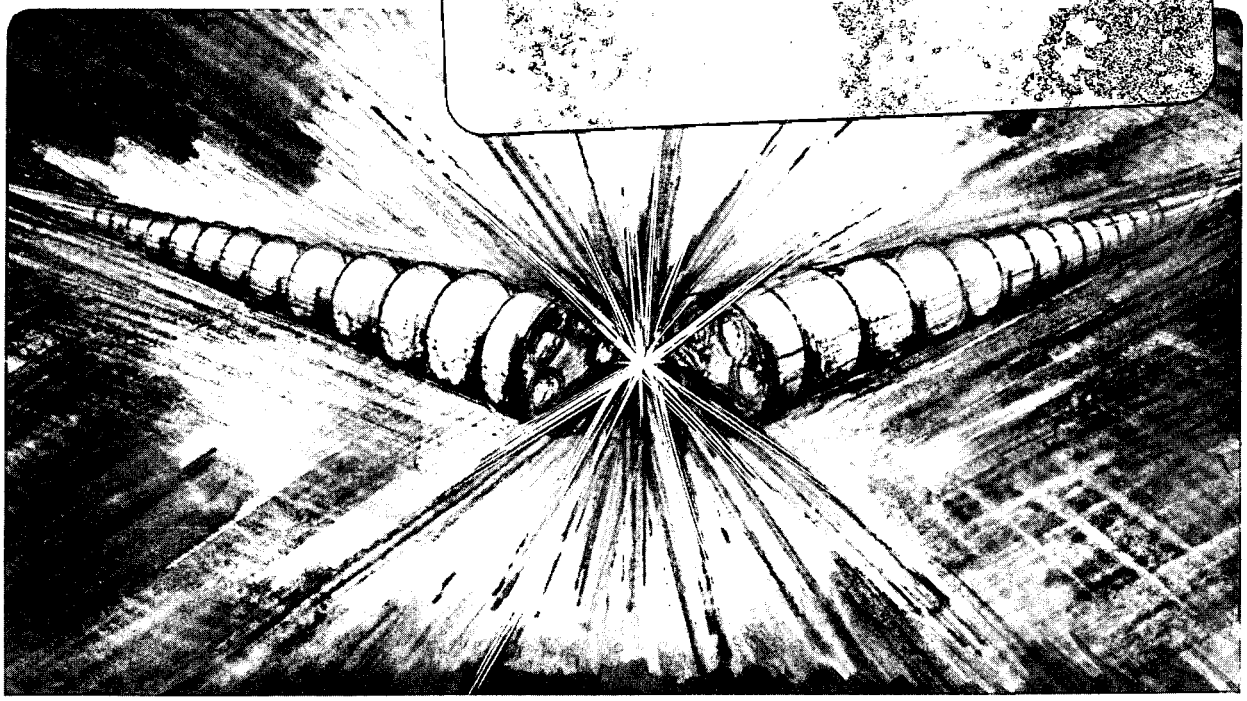

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DISCLAIMER

Quad Nanosecond Delay Module*

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Abstract

Four nanosecond (ns) delay units have been designed to fit in a single-width NIM module. This module is particularly suited for use in conjunction with quad constant fraction timing discriminators (CFTDs) since it has four delay units that can be placed adjacent to the four units of the CFTD. A series of different length cables connected via DIP toggle switches provide delays of 0-60 ns in 4 ns increments. Thus, the CFTD delay can be optimized for pulses of different rise times from ~10-100 ns. Design work for the PC board and silkscreening of the front panel were done with the MacDraw program on the Apple Macintosh computer and printed with the Laserwriter printer.

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I. Introduction:

The development of NIM electronics during the last decade has progressed toward greater packing densities. This has resulted in the replacement of many single unit modules with quad (4) and octal (8) unit modules. At present, most discriminators and logic modules come in at least a quad configuration. Although the octal units provide greater packing densities, the need for sufficient front panel space for the placement of connectors and controls has lead us to generally favor quad rather than octal units.

Specifically, our electronics pool now contains many of the quad constant fraction timing discriminators (CFTDs), both LBL # 21X4141-P2 and Tennelec TC-455, which require external cable delays. For a "fraction" setting of 40%, these CFTDs require a cable delay of about 60% of the rise time of the input pulse. For signals with very short rise times (<6ns), a short external delay cable may be attached directly to the CFTD. However, for longer rise times (10-100 ns), the delay cables become long and tend to be inconvenient. In addition, changing the delay time to optimize the timing resolution is awkward with external cables. Electronics set-ups, which require a large number of CFTDs, can be simplified by having variable-time cable-delay units built into a single width NIM module which can be placed next to the CFTD. We call this module, shown in Figure 1, the Quad Nanosecond Delay (QNSD). In our design, four toggle switches can be used to vary the delay between 0 and 60 ns in 4 ns increments. The maximum cable length of 60 ns and the 4 ns increments are dictated by both the physical amount of cable one can fit in a single width NIM module and the number of switches that can be placed on the front panel. Also, degradation of the signal amplitude and shape limits the maximum practical delay to about 60 ns.

II. Operation:

The quad ns delay has four identical units with 0-60 ns of delay between input and output connectors. Switches are used to add delay by adding additional lengths of cable in series. The insertion delay (the amount of delay with all switches in the "out" position) is ~ 1.7 ns. Throwing a single switch will provide delays of 4, 8, 16, or 32 ns by selecting cables of lengths 84, 168, 336, and 672 cm of RG-316 50 Ω teflon-insulated transmission cable. Additional switches can add delays up to the maximum of 60 ns in 4 ns increments. The accuracy of the delays is ~ 1% as is the unit-to-unit variation. One can obtain additional delay by cascading units, but at the expense of signal quality.

III. Design and Construction:

Several practical considerations went into the design and construction of this module. 1.) Only small diameter cable, such as RG-174 or RG-316 would allow us to fit 240 ns of cable delay into a single-width NIM module. RG-316 was chosen since its teflon insulation deforms less under the heat of soldering than does the PVC insulation of RG-174. The electronic performance of the two types of cable was found to be identical within the limits of our tests. 2.) 16 switches were needed on the front panel. The Grayhill 76STDO2 DIP double pole double throw toggle switch was chosen because of its small size and because it caused little degradation of signal shape in preliminary tests. The switches were mounted in sockets for ease of replacement in case of failure. 3.) Lemo type connectors were used to conserve front panel space and to be compatible with connectors on other modules, particularly those on the CFTDs. 4.) The construction was based on printed circuit (PC) board mounted components to minimize fabrication costs.

After preliminary decisions had been made regarding the switches, cables, and connectors; the MacDraw program on the Apple Macintosh was used to design the front panel and to determine the positions of the controls and the dimensions of the holes to be drilled and switch openings to be cut. A drawing of the front panel lay-out and assembly is shown in Figure 2. In order to improve unit-to-unit similarity and ease of construction, it was decided that all the switches and connectors should be mounted on a PC board. This board was designed with MacDraw, printed on the Laserwriter printer, and sent to the photography lab to generate a diapositive for the PC shop to use for circuit board fabrication Figure 3 shows both sides of the PC board and the master for silkscreening the front panel. Note that the back side of the board is a ground plane to shield the switches from the cables as well as to make the traces on the other side approximate a 50 Ω transmission cable. Figure 4 shows a circuit diagram and a parts list including prices as of March 1986. Besides the ~$130 for the parts listed in Figure 4, about 7 man hours per unit (based on a production run of 12 modules) were needed for assembly.

IV. Tests and results:

A one unit prototype was constructed and compared with a single length of cable as well as other delay boxes such as the Canberra 2058 and the Chronetics Model 21. Figure 5a shows a comparison between a 60 ns length of RG-316 and the QNSD with the full 60 ns of delay inserted. Note how the pulse shape is only slightly better for the cable alone. Figure 5b shows a comparison between the QNSD and the Canberra 2058. Note the poorer quality output signal shape for the Canberra 2058. This is presumably due to construction techniques since the Canberra unit uses the same RG-316 cable and similar quality switches. The center conductors of the connectors in the Canberra 2058 are connected to the switches by ~2 cm lengths of wire - not transmission cable - and each delay line is connected to the

switches by ~2 cm lengths of unshielded cable. This lack of attention to impedance matching and shielding presumably leads to the poorer signal quality. The QNSD is made with minimum lengths (<0.5 cm) of unshielded cables and the traces on the PC board were layed out to approximate a 50 Ω transmission line. Figure 5c shows a comparison between the QNSD and the Chronetics Model 21. This dual rack-mounted unit is built with slide switches and RG-58 cable and significant care was taken to limit unshielded cable lengths and reflections at the input and output connectors. Although this unit performs better than the QNSD (as expected from the RG-58 cable alone), it is bulky and requires inconvenient rack mounting.

Another concern in the design and construction of the QNSD was that there may be cross-talk between channels since the cables were so closely packed. No particular attention was made to separate the cables between different units. All the 32 ns lengths were first packed in the module, followed by the 16 ns, the 8 ns, and the 4 ns lengths. To check for cross-talk between channels, a NIM logic signal from a pulser was run at high rate into two channels of the module (#2 and #4), and the channel in between (#3) was examined with an oscilloscope. Figure 6a shows the results: The middle trace is the signal going through 60 ns of delay in channel 4, and the bottom trace is channel 3 with no input and all 60 ns of delay selected. Thus, there is maximum coupling between channels. The vertical scale of the bottom trace is more sensitive by a factor of 100. Thus, less than 0.1% of the input signal is picked up on this adjacent channel.

Figure 6b shows the signal from an ORTEC 474 timing filter amplifier configured with a rise time of 100 ns and a decay time of 50 μseconds, and the 60 ns delayed output from the QNSD superimposed on it. For the intended use as an external delay for CFTDs, where the signal rise times are much slower than for logic pulses, the deterioration in pulse shape is hardly noticeable, although the output signal is attenuated ~15% due to cable length. Note that the input and output signals are displaced by one division in the vertical scale.

V. Conclusions:

The construction and performance of a quad ns delay module has been described. This unit was specifically designed to provide the external delay for quad CFTDs. Thus, it was fitted into a single-width NIM module where is could be placed adjacent to the CFTD to minimize the lengths of connecting cables. It is equally suitable for other applications requiring logic or linear delays of less than 60 ns.

In this design project, we have also demonstrated the power of the Macintosh computer, when linked with the MacDraw program and Laserwriter printer, as a simple and effective computer aided design (CAD) tool. A disk with the PC artwork and front panel lay-out is available upon request from the authors.

Figure Captions

Figure 1. Picture of the QNSD module from the front (left picture) and from the side (right picture). One cover is removed to show construction details.

Figure 2. Assembly drawing of the QNSD module, showing, from left to right, an overall view of the final module, a dimensioned pattern for making the front panel, and the positioning of the circuit board.

Figure 3. Side one and side two of the circuit board, and the silkscreening pattern for the front panel. All of these were designed with the program MacDraw and printed on the Laserwriter Printer.

Figure 4. Circuit diagram (typical) and parts list with prices. Prices are total costs, that is: quantity x unit price.

Figure 5. a) Input pulse (top trace) and the delayed output pulse for 60 ns of cable delay (middle trace) and the delayed output pulse for 60 ns of cable delay in the QNSD (bottom trace). Vertical and horizontal scales are shown on the figure. b) Input pulse (top trace) and the delayed output pulse for 60 ns cable delay in the QNSD (middle trace) and for the Canberra 2058 (bottom trace). c) Input pulse (top trace) and the delayed output pulse for 60 ns cable delay in the QNSD (middle trace) and in the Chronetics Model 21.

Figure 6. a) Input pulse (top trace) and the delayed output pulse for 60 ns of cable delay in unit #4 of the QNSD (middle trace) and the output of unit #3 of the QNSD with no input (bottom trace). Note the factor of 100 difference in vertical scale between the middle and bottom traces (500 mV / division in the middle trace and 5 mV / division in the bottom trace.) b) Input pulse from an ORTEC 474 Timing Filter Amplifier with a 100 ns rise time and a 50 μsecond decay time and 60 ns delay in the QNSD. The scale is 0.1 V / division vertical and 100 ns / division horizontal. Note the 0.1 V offset between the input (lower trace) and the output (upper trace).

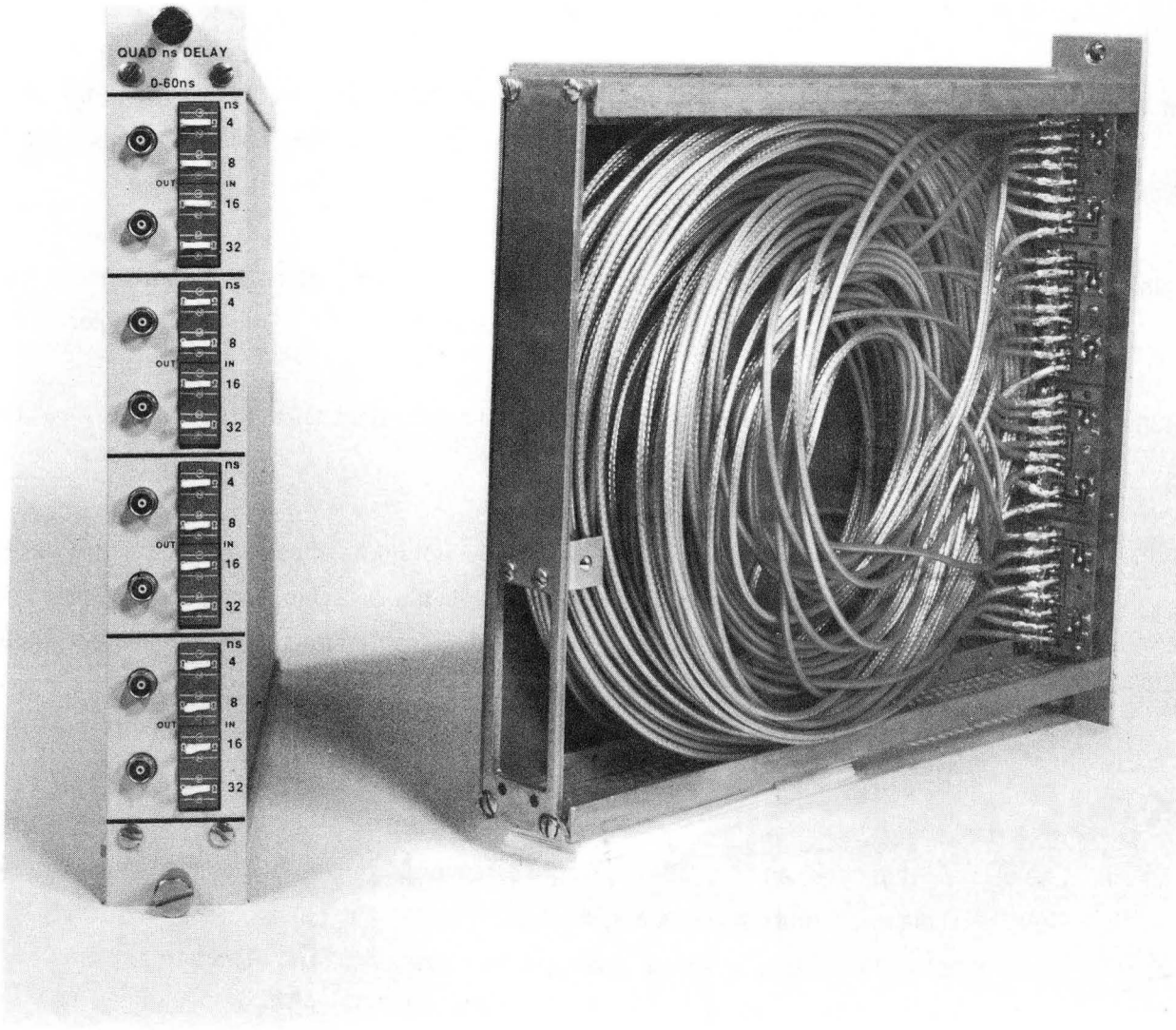

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Figure #1

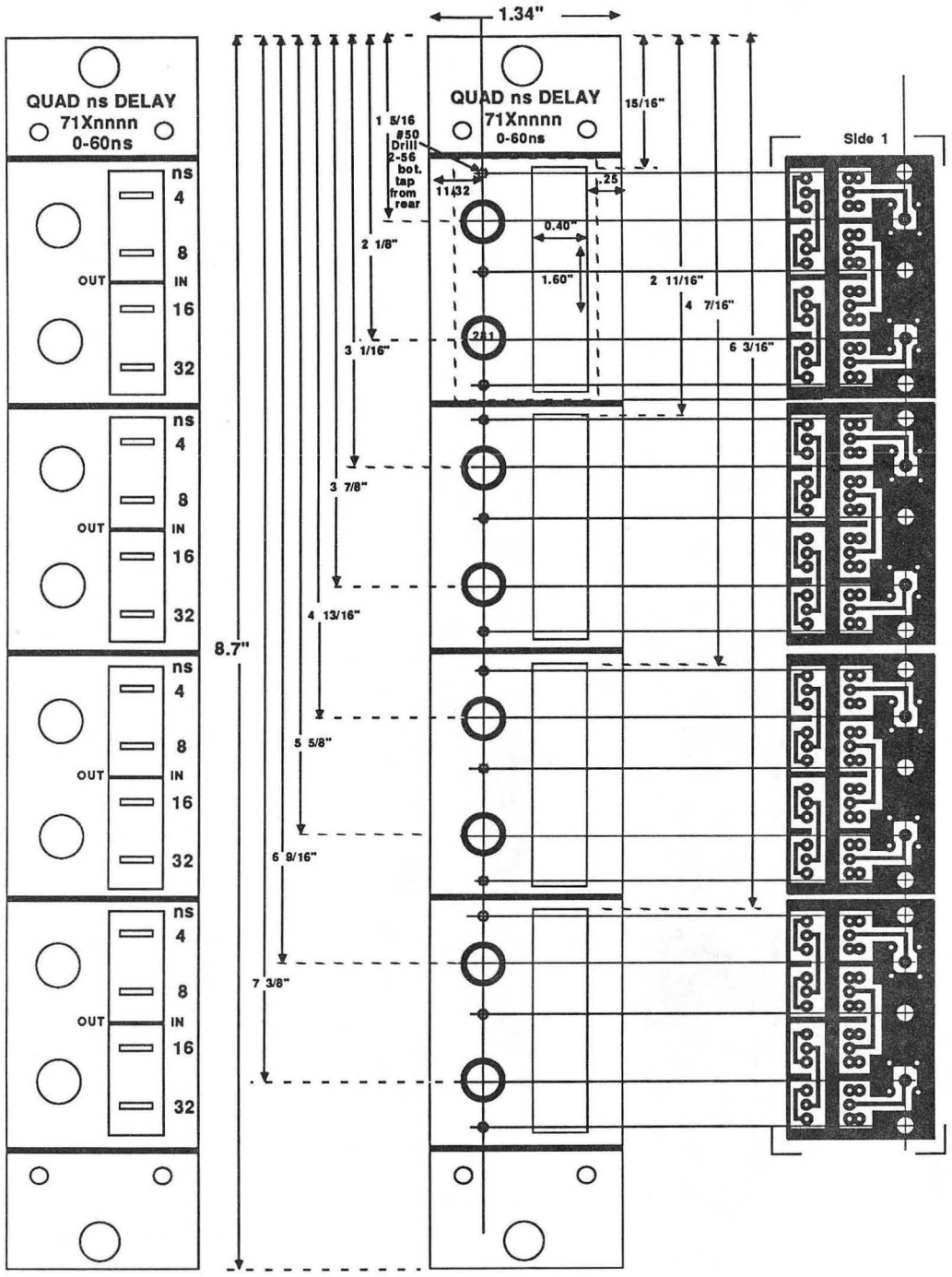

QUAD ns DELAY
71Xnnnn
0-60ns
ns
4
8
OUT
IN
16
32
1.34"
1 5/16
#50 Drill
2-56 tap
bot. from rear
11/32
.25
15/16"
0.40"
1.60"
2 1/8"
2 11/16"
4 7/16"
6 3/16"
3 1/16"
3 7/8"
4 13/16"
5 5/8"
6 9/16"
7 3/8"
8.7"
Side 1

Figure #2

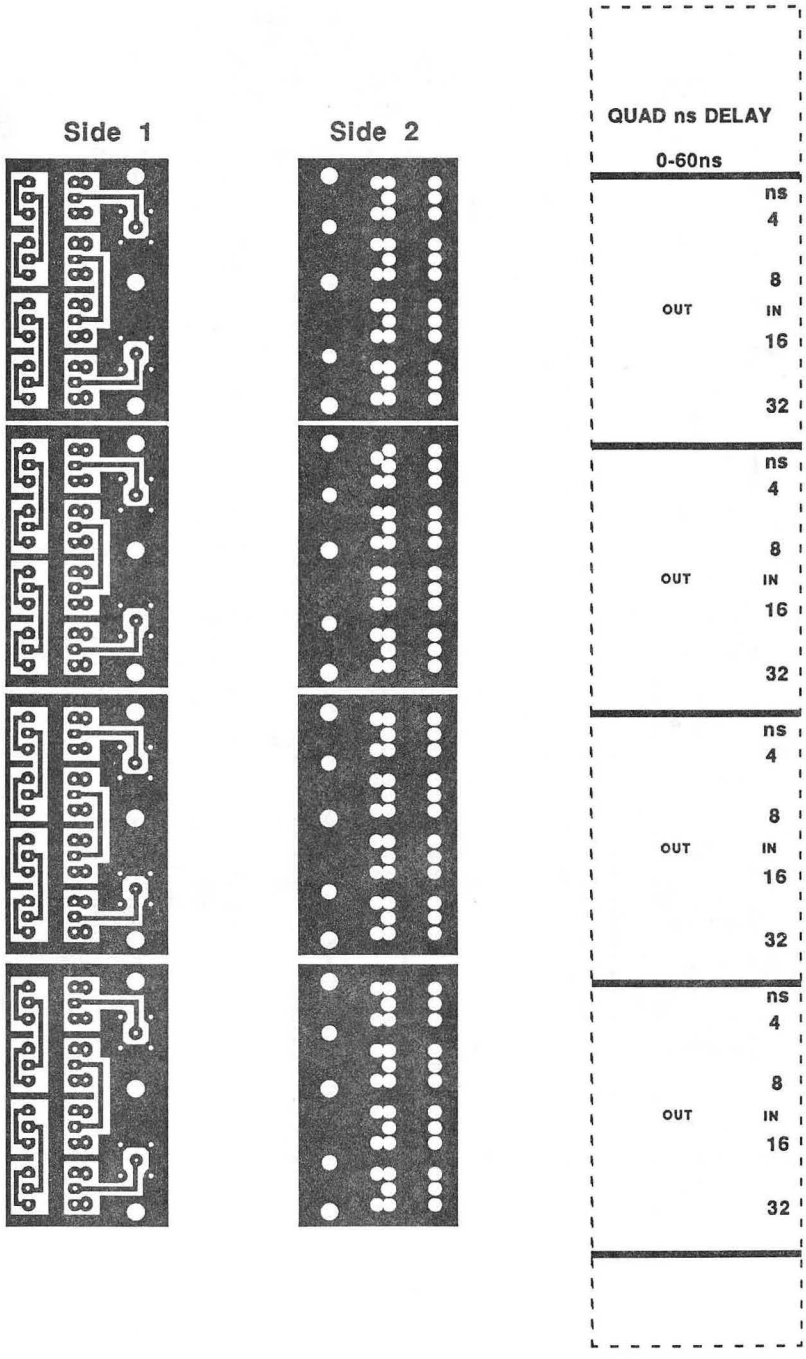
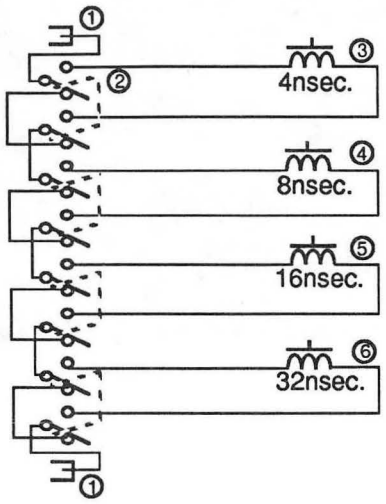

Side 1
Side 2
QUAD ns DELAY
0-60ns
ns
4
8
OUT
IN
16
32
ns
4
8
OUT
IN
16
32
ns
4
8
OUT
IN
16
32
ns
4
8
OUT
IN
16
32

Figure #3



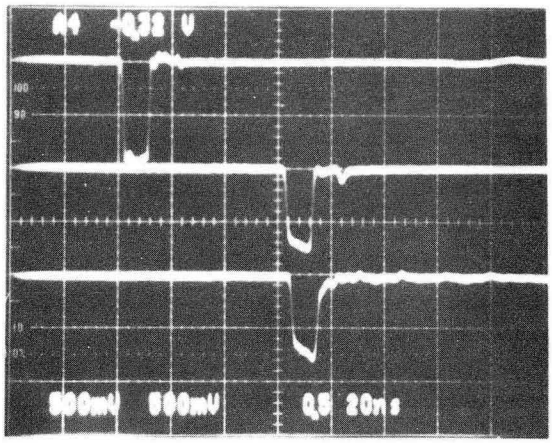
Parts List

		No. Required	Price 2/86
①	Lemo connector part # RP 00.250 TEF	8	39.68 *
②	Switches : Grayhill part # 76STD02	8	24.08 *
③	Delay line: 84 cm. RG 316/U: LBL # 6145-62775	4	2.42
④	Delay line: 168 cm. RG 316/U	4	4.84
⑤	Delay line: 336 cm. RG 316/U	4	9.68
⑥	Delay line: 672 cm. RG 316/U	4	19.36
7.	NIM single unit module kit: LBL # 5975-47926	1	21.65
8.	Printed circuit board	1	nil
9.	Screws : 2-56 3/8" long	6	nil
10.	Bussing strip: LBL Stock # 5975-58592	1	6.50
11.	I.C. Sockets, 14 Pin: LBL Stock # 5975-50977	8	3.12

* Quantities of 100+

Figure #4

a)



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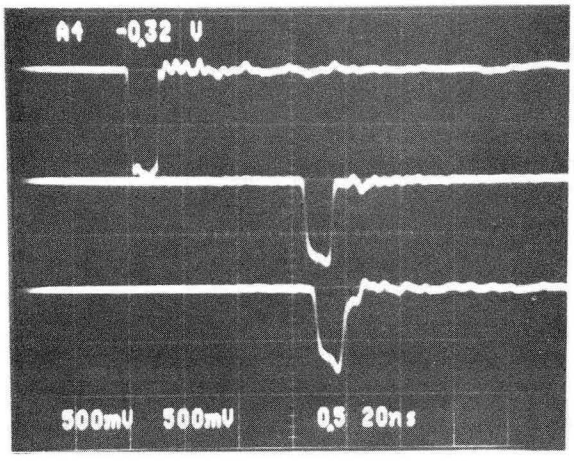

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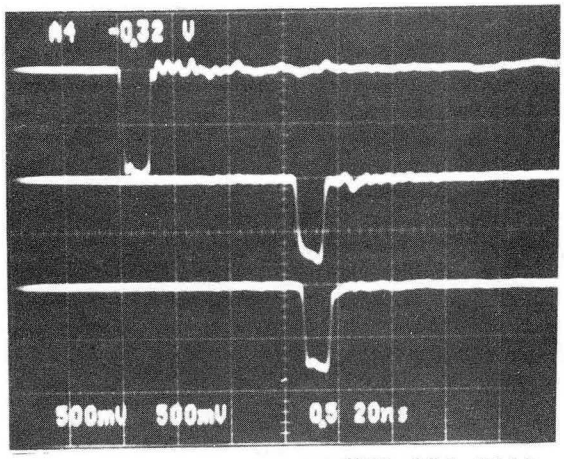

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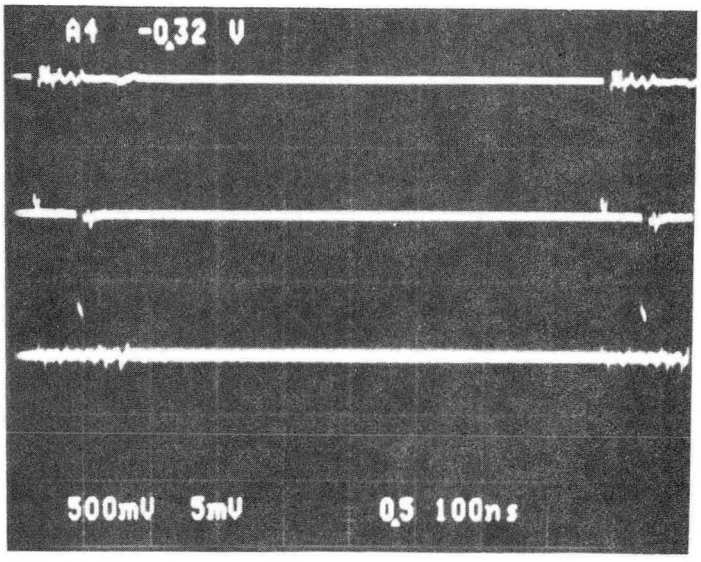
Figure #5

a)



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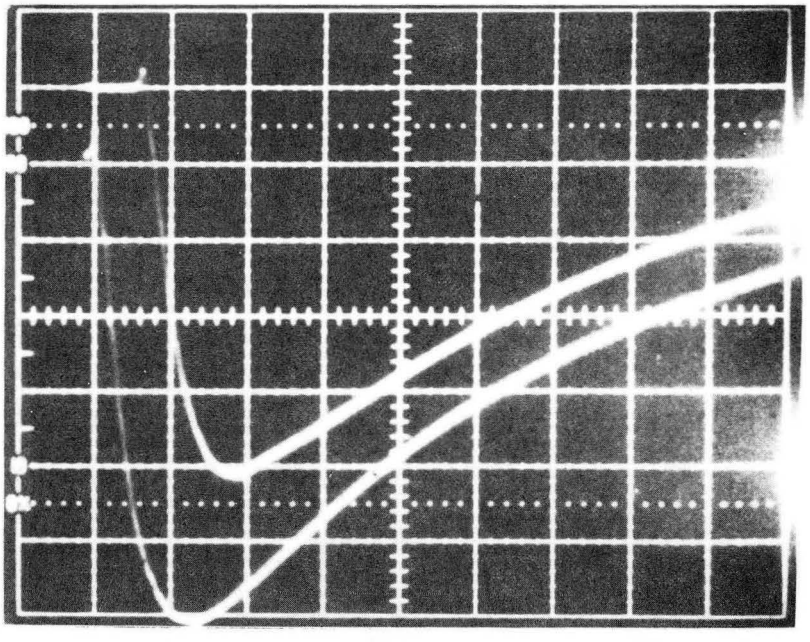

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Figure #6

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