## UC Berkeley UC Berkeley Previously Published Works

## Title

A Compact Model of Polycrystalline Ferroelectric Capacitor

**Permalink** <u>https://escholarship.org/uc/item/5j9121ws</u>

**Journal** IEEE Transactions on Electron Devices, 68(10)

**ISSN** 0018-9383

### Authors

Tung, Chien-Ting Pahwa, Girish Salahuddin, Sayeef <u>et al.</u>

**Publication Date** 

2021-10-01

**DOI** 10.1109/ted.2021.3100814

## **Copyright Information**

This work is made available under the terms of a Creative Commons Attribution-NonCommercial-NoDerivatives License, available at <u>https://creativecommons.org/licenses/by-nc-nd/4.0/</u>

Peer reviewed

# A Compact Model of Metal-Ferroelectric-Insulator-Semiconductor Tunnel Junction

Chien-Ting Tung, Graduate Student Member, IEEE, Girish Pahwa, Member, IEEE, Sayeef Salahuddin, Fellow, IEEE, and Chenming Hu, Life Fellow, IEEE

Abstract-In this paper, we present a compact model of metal-ferroelectric-insulator-semiconductor (MFIS) tunnel junction. Unlike the metal-ferroelectric-metal structure with only one insulator layer, MFIS-FTJ contains two insulator layers and a semiconductor electrode. The complex structure makes it difficult to self-consistently solve the Poisson and charge equations. We report the first compact model of MFIS-FTJ to our knowledge. Previous modeling studies focused on numerical simulation, which is time-consuming and not applicable to circuit simulation. The presented compact model is suitable for commercial SPICE IC simulation. It includes a ferroelectric model that can capture polarization switching under arbitrary applied voltage, an insulator-semiconductor model that calculates the potential profile of the MFIS stack, and an analytical tunneling current model. We demonstrate that this model can be used to simulate and fit both n-type and p-type MFIS-FTJs.

Index Terms— Compact model, ferroelectric, ferroelectric memory, hafnium zirconium oxide (HZO), ferroelectric tunnel junction (FTJ).

#### I. INTRODUCTION

**F**erroelectric tunnel junction (FTJ) is a nonvolatile memory first proposed by Esaki *et al.* in 1971 [1]. FTJ, due to its good scalability, low-power consumption and non-destructive reading [2], is a promising candidate for future nonvolatile memories. In 2011, discovering the ferroelectricity in HfO<sub>2</sub> [3, 4] made FTJ compatible with CMOS technology. The original FTJ is based on the metal-ferroelectric-metal (MFM) structure. The tunneling electroresistance (TER) ratio comes from the difference in screening lengths of two electrodes causing the variation of the barrier heights in different polarization states [5, 6]. Due to the limited change in barrier heights, this structure suffers from low TER ratio. To improve TER ratio, the metal-ferroelectric-insulator-semiconductor (MFIS) FTJ is developed. It has a much larger variation in the semiconductor

This work was supported by the Berkeley Device Modeling Center, University of California at Berkeley, Berkeley, CA, USA. The review of this article was arranged by Editor XXX.

(Corresponding author: Chien-Ting Tung.)

The authors are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA (e-mail: cttung@berkeley.edu). surface potential than metal. A TER ratio over 30 has been reported in an n-type MFIS-FTJ with 4nm-HZO [7]. A p-type MFIS-FTJ with 1nm-HZO has also been fabricated with the on-current up to 1 A/cm<sup>2</sup> [8]. With the growing interest in the FTJ device, a SPICE-compatible compact model of MFIS-FTJ is needed.

Although the compact model of MFM-FTJs has been studied [9, 10], there isn't a compact model of MFIS-FTJs. Unlike MFM-FTJ models that only need to consider the electron tunneling through one potential barrier, an MFIS-FTJ model needs to consider two potential barriers. Furthermore, due to the effect of the ferroelectric polarization on the band structure, the gate tunneling current model used for the HK-dielectric stack [11] cannot be applied in these devices. Previous modeling studies of MFIS-FTJs numerically calculate the energy band diagram and use the WKB approximation or the NEGF method to simulate tunneling current. This is not suitable in circuit simulations because of the significant computational time [12-15].

In this paper, we present and demonstrate a compact model of MFIS-FTJs. Starting with the polycrystalline ferroelectric capacitor model we previously developed [16], the present model calculates ferroelectric polarization and the potential profile of the entire MFIS stack self-consistently. The potential profile is then used to calculate the tunneling current. This model has good computational efficiency and models the experimental data of MFIS-FTJ well.



Fig. 1. Schematic band diagram of an MFIS-FTJ and its equivalent circuit.

#### II. Model

#### A. Ferroelectric model

An MFIS-FTJ can be seen as a ferroelectric (FE) capacitor in series with an insulator-semiconductor (IS) capacitor as shown in Fig. 1. To calculate the polarization of the FE capacitor, we start with the FE capacitor model developed in our previous work [16]. This FE model considers a polycrystalline FE material that has many crystalline grains or grain groups. Each group has a local field-dependent switching rate characterized by a material parameter  $\eta$ , which varies due to random variations of the local material properties such as crystal orientation, stress and stoichiometry. This local switching rate is shown in (1) known as the Merz's law [17], where  $E_a$  is the activation field,  $E_{FE}$  is the electric field,  $\tau_0$  is the characteristic time for a very large  $E_{FE}$ , and  $\alpha$  is a fitting parameter.

Under a positive  $E_{\rm FE}$ , the positively polarized area  $A_{\eta+}$  is assumed to increase according to (2) and  $A_{\eta+}$  has an exponential dependency of the accumulative time in a greement with previous experiments and models [18, 19] shown as (3).  $A_{\eta}$  is the total area of the specific  $\eta$  group,  $t_i$  is the time when  $E_{\rm FE}$  polarity changes, and  $\beta$  is a fitting parameter. By summing up the  $A_{\eta+}$  of all the  $\eta$  groups, we obtain the total positively polarized area  $A_{+}$  and calculate the polarization by (4), where  $A_{\rm T}$  is the total area of the device,  $f(\eta)$  is the probability distribution function of  $\eta$ , and  $P_{\rm R}$  is the remanent polarization.

$$\tau(t,\eta) = \tau_0 \exp\left(\left(\frac{\eta E_a}{|E_{\rm FE}(t)|}\right)^{\alpha}\right),\tag{1}$$

$$\frac{dA_{\eta_{+}}}{dt} = \frac{A_{\eta} - A_{\eta_{+}}}{\tau(t,\eta)}, \text{ if } E_{\text{FE}}(t) \ge 0,$$

$$= \frac{-A_{\eta_{+}}}{\tau(t,\eta)}, \text{ if } E_{\text{FE}}(t) < 0,$$
(2)

$$A_{\eta+}(t) = A_{\eta} - \left(A_{\eta} - A_{\eta+}\right)\Big|_{t=t_{i}} \exp\left(-\left(\int_{t_{i}}^{t} \frac{1}{\tau(t,\eta)} dt'\right)^{\beta}\right),$$
  
if  $E_{\text{FE}}(t) \ge 0,$  (3)

$$=A_{\eta+}\Big|_{t=t_{i}}\exp\left(-\left(\int_{t_{i}}^{t}\frac{1}{\tau(t,\eta)}dt'\right)^{\beta}\right), \text{ if } E_{\text{FE}}(t)<0,$$

$$A_{+}(t) = \sum A_{\eta^{+}}(t) \cong \int_{0}^{\eta^{\max}} A_{\Gamma} f(\eta) d\eta \times \frac{A_{\eta^{+}}(t)}{A_{\eta}}, \qquad (4a)$$

$$P(t) = P_{\rm R} \times \left(\frac{2A_{+}(t)}{A_{\rm T}} - 1\right),$$
 (4b)

The capacitor's total charge density is the sum of the polarization and the charge of background dielectric of the FE capacitor as (5). This is also the semiconductor charge density

(per area),  $Q_{\rm s}$ .

$$Q_{s} = -\left(P\left(t\right) + \varepsilon_{\text{FE}}V_{\text{FE}} / t_{\text{FE}}\right), \tag{5}$$

#### B. Semiconductor surface potential calculation

 $Q_{\rm s}$  can be used to calculate the semiconductor surface potential,  $\psi_{\rm s}$  using (6) [20].  $N_{\rm d}$  is the doping density and  $n_{\rm i}$  is the intrinsic carrier density.

$$Q_{\rm s} = \pm \sqrt{2\varepsilon_{\rm Si}k_{\rm B}TN_{\rm d}} \left[ \left( e^{\frac{q\psi_{\rm s}}{k_{\rm B}T}} - \frac{q\psi_{\rm s}}{k_{\rm B}T} - 1 \right) + \frac{n_{\rm i}^2}{N_{\rm d}^2} \left( e^{-\frac{q\psi_{\rm s}}{k_{\rm B}T}} + \frac{q\psi_{\rm s}}{k_{\rm B}T} - 1 \right) \right]^{0.5}$$
(6)

This equation has no explicit solution for  $\psi_s$  as a function of  $Q_s$  and must be solved iteratively. High computational speed is of prime importance for compact models for supporting the simulations of large memory circuits. Therefore, a good initial approximate solution for reducing the iteration cycles is of prime importance.

In the accumulation region, the initial approximation of  $\psi_{s0}$  is the following.

$$z = -\exp\left[-\left(\frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm si}k_{\rm B}TN_{\rm d}}}\right)^2 - 1\right],\tag{7a}$$

If z < 0 then

$$\psi_{s0} = -\frac{k_{\rm B}T}{q} \left[ W_{-1}(z) + \left( \frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm si}k_{\rm B}TN_{\rm d}}} \right)^2 + 1 \right] \times \left( 1 + e^{\gamma Q_{\rm s}} \right), (7b)$$
$$W_{-1}(z) \approx \ln(-z) - \ln(-\ln(-z)) + \frac{\ln(-\ln(-z))}{\ln(-z)}, \quad (7c)$$

If  $z \ge 0$  then

$$\psi_{s0} = \frac{k_{\rm B}T}{q} \ln \left[ \left( \frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm Si}k_{\rm B}TN_{\rm d}}} \right)^2 + 1 \right], \tag{7d}$$

In the depletion and inversion region, the initial approximation is the following.

$$z = \frac{n_{\rm i}^2}{N_{\rm d}^2} \exp\left[\left(\frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm Si}k_{\rm B}TN_{\rm d}}}\right)^2 + 1\right],\tag{8a}$$

If z < 2 then

$$\psi_{s0} = \frac{k_{\rm B}T}{q} \left[ z - \left( \frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm Si}k_{\rm B}TN_{\rm d}}} \right)^2 - 1 \right] \times \left( 1 - e^{-\gamma Q_{\rm s}} \right), \quad (8b)$$

If  $2 \le z < 10^{200}$  then

$$\psi_{s0} = \frac{k_{\rm B}T}{q} \left[ W(z) - \left(\frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm Si}k_{\rm B}TN_{\rm d}}}\right)^2 - 1 \right], \tag{8c}$$

$$W(z) \approx \ln(z) - \ln(\ln(z)) + \frac{\ln(\ln(z))}{\ln(z)}, \quad (8d)$$

If  $z \ge 10^{200}$  then

$$\psi_{s0} = -\frac{k_{\rm B}T}{q} \frac{N_{\rm d}^2}{n_{\rm i}^2} \ln\left[\left(\frac{Q_{\rm s}}{\sqrt{2\varepsilon_{\rm Si}k_{\rm B}TN_{\rm d}}}\right)^2 + 1\right],\qquad(8e)$$

W(z) and  $W_{-1}(z)$  are the lambert W functions.  $\gamma$  in (7b) and (8b) are used to tune the approximation at small  $Q_s$  and improve the convergence. The condition z < 2 is chosen to avoid the spike in (8c) if z is close to 1. The condition  $z > 10^{200}$  is introduced due to the numerical limitation of exponential in numerical computation. The value can also be adjusted depending on the simulator used. In Fig.2, the initial approximation is already very close to the  $Q_s$  obtained by (5) using  $\psi_s$  as the input. Halley's iterative method is used to solve (5) to get the surface potential [21]. In most cases, the iteration converges in 2 or 3 cycles. From the semiconductor surface electrical potential and field, the voltage drop across the insulator can be computed. Finally, the terminal voltage  $V_{\rm IS}$  of the insulator-semiconductor capacitor is the combination of the flat-band voltage  $V_{\rm FB}$ , the insulator voltage and the semiconductor surface potential. For p-type, the equations are similar with different signs

$$V_{\rm IS} = V_{\rm FB} - \frac{Q_{\rm s}}{C_{\rm IL}} + \psi_{\rm s}, \qquad (9)$$

#### C. Tunneling current model

To calculate the tunneling current in this compact model, we use an analytical equation. Previous studies of MFIS-FTJs often use numerical WKB approximation to simulate the tunneling current [13-15]. However, this method is not computationally efficient. Besides, WKB approximation does not consider the reflection of electron waves at the interfaces, and the band structure does not have the quantum mechanism correction. Therefore, even directly using the WKB approximation cannot produce accurate results, fitting parameters still need to be introduced. Furthermore, in addition to the conduction band electrons (CBE), valence band electrons (VBE) and holes (VBH) also need to be taken into account, which increases the computation time further [13]. In this work, we develop an analytical equation with several fitting parameters that can give the user enough flexibility to fit the experimental data of MFIS-FTJs with complex physics effects.

To simplify the model, we consider the semiconductor electrode as a metal, adapt the direct tunneling (DT) current equation from MFM-FTJ [22] to include the effect of two insulator layers. (10a) shows the barrier height relative to the Fermi level at the Insulator-Si and Metal-FE interfaces where  $\phi_{\rm IL/Si}$  and  $\phi_{\rm MFE}$  are the band-offsets at these interfaces, and  $V_{a2}$  is the modified applied voltage to restrict the applied voltage  $V_a$  to the region of DT. *a* and *b* are both theoretically 0.5 for CBE but we make them be fitting parameters to include the effect of VBE, VBH and other quantum mechanism effects. An empirical function  $g(V_{a2})$  is also added to fit the tunneling current. This is a standard practice in compact modeling, which requires high-speed computation and a greement to less than 1% with the measured device data.

$$\phi_{\rm IL} = \left[\phi_{\rm IL/Si} - \psi_{\rm s} + k_{\rm B}T\ln(\frac{N_c}{N_{\rm d}})\right] + q \cdot aV_{\rm a2}, \ \phi_{\rm FE} = \phi_{\rm M/FE} - q \cdot bV_{\rm a2},$$
(10a)

$$A_{\rm IL} = \frac{-4t_{\rm IL}\sqrt{2m_{\rm IL}^*}}{3\hbar V_{\rm OX}}, \ A_{\rm FE} = \frac{-4t_{\rm FE}\sqrt{2m_{\rm FE}^*}}{3\hbar V_{\rm FE}},$$
(10b)

$$T_{\rm I} = A_{\rm IL} \left[ \left( \phi_{\rm IL} \right)^{\frac{3}{2}} - \left( \phi_{\rm IL} - qV_{\rm OX} \right)^{\frac{1}{2}} \right] + A_{\rm FE} \left[ \left( \phi_{\rm FE} + qV_{\rm FE} \right)^{\frac{3}{2}} - \left( \phi_{\rm FE} \right)^{\frac{3}{2}} \right],$$
(10c)

$$T_2 = A_{\rm IL} \left( \sqrt{\phi_{\rm IL}} - \sqrt{\phi_{\rm IL}} - qV_{\rm IL} \right) + A_{\rm FE} \left( \sqrt{\phi_{\rm FE}} + qV_{\rm FE} - \sqrt{\phi_{\rm FE}} \right), (10d)$$

$$A_{\rm GW}^* \exp(T) = (3aT)$$

$$J_{\rm DT} = \frac{-4qm_{\rm FE}}{3\pi^2 h^3} \frac{\exp(I_1)}{T_2^2} \sinh\left(\frac{3qI_2}{4}V_{\rm a2}\right) \times g\left(V_{\rm a2}\right), \qquad (10e)$$

$$g(V_{a2}) = c \left[ dV_{a2}^{2} + 1 + e - \sqrt{\left( dV_{a2}^{2} + 1 - e \right)^{2} + e\left( dV_{a2}^{2} + 1 \right)} \right]$$
(10f)  
×(fV\_{a2}^{4} + 1),

We have verified this model with the simulated current using drift-diffusion and WKB approximation to calculate a bilayer MIS structure with a fixed polarization in the first layer for simplicity. Fig. 3 shows that this model can fit the WKB tunneling current through the bilayer structure with polarization accurately under different configurations. We can see that thinner FE, IL hyers and hrger polarization would give higher currents, which agrees with [12]. For different  $N_d$ , there isn't visible change in the positive on-current because the semiconductor is in inversion, which also agrees with [12]. The larger positive polarization will pull down the semiconduction potential more. However, for the high voltage region, the Fowler-Nordheim tunneling would appear as well as the space charge effect due to the transported carriers [23, 24]. Those effects are not considered by this compact model, which limits this model's accuracy at high voltage regions.

#### III. RESULTS

We have implemented this compact model in Verilog-A code, which is the most popular programing language for compact models, and test it on Hspice. We have modeled both n-type and p-type MFIS-FTJ experimental data using the presented MFIS-FTJ model. Fig. 4(a) shows the fitting of an n-type FTJ with  $t_{\rm IL} = 0.4$  nm,  $t_{\rm FE} = 4$  nm,  $N_{\rm d} = 3 \times 10^{19}$  cm<sup>-3</sup> and  $P_{\rm R} = 5\mu C / \text{cm}^2$  [7]; Fig. 4(b) shows the fitting of a p-type FTJ with  $t_{\rm IL} = 1$  nm,  $t_{\rm FE} = 1$  nm,  $N_{\rm a} = 1 \times 10^{19}$  cm<sup>-3</sup> and  $P_{\rm R} = 4\mu C / \text{cm}^2$  [8]. To fit these FTJ devices, the fitting parameters are treated as a function of polarization, where we use interpolation to generate the parameters between  $+P_{\rm R}$  and  $-P_{\rm R}$ . We use subscript + for the value at  $+P_{\rm R}$  and - for  $-P_{\rm R}$  in Fig. 4. This compact model can be used for both n-type and p-type MFIS-FTJ regardless of whether electrons or holes are the transport carriers.

We have tested this model for simulating MFIS\_FTJ in circuits. Fig. 5 shows a simple circuit. To demonstrate the ability to work with arbitrary input waveforms, we apply an unusual 100ns triangular positive voltage pulse to program the FTJ to its on-state followed by a read voltage of 0.2 V, then by a negative triangular pulse to program to off state followed by a read voltage of 0.2 V. Fig. 5 shows the device current vs time, the transient programming and read currents in the on and the off states. To further demonstrate the model's ability, in Fig. 6, we show the polarization switching and the tunneling current under triangular pulses of varying amplitude. The model keeps track of the polarization history well.

In addition, to test the simulation time efficiency of this compact model, we applied the waveforms of varying amplitude in Fig. 6a for 1000 cycles. The total runtime is only 52.27s on Intel Xeon Gold 5115 CPU. This speed is comparable to popular transistor compact models, such as BSIM\_CMG for FinFET IC simulation, and is, therefore, suitable for simulation large circuits involving MFIS\_FTJ. The 52ms simulation presented in Fig. 5a will take hours if it is performed with TCAD.

As shown in Fig. 5, the polarization does not remain at its maximum value when the voltage rests at 0. It is because there is still some depolarization field a cross the FE layer as shown in Fig. 1. This leads to the decrease in TER ratio. The design rule of MFIS-FTJs should choose the FE material with a larger coercive field than the depolarization field. Here, reducing  $t_{\rm IL}$  can help reduce the depolarization field and increase the tunneling current as shown in Fig. 3. The optimal design w.r.t the thickness, doping and polarization has been studied in [12]. To reduce the depolarization field and increase the on-current as well as the TER ratio, we should reduce both  $t_{\rm IL}$  and  $t_{\rm FE}$  at the same time.



Fig. 2. Comparison of our initial guess of  $\psi_s$  and the  $Q_s - \psi_s$  curve obtained from the analytical equation (5).



Fig. 3. Comparison of the tunneling current model and the WKB approximation. The symbols are the WKB approximation. The lines are the compact model. For the black line, the parameters are a = 0.52, b = 0.48, c = 1, d = 30, e = 1.8, and f = 0.008. For the red lines the following parameters are different: (a) d = 20, e = 1.2; (b) d = 20, and e = 2; (c) (d): All parameters are the same.



Fig. 4. Fitted results of (a) an n-type MFIS-FTJ [7] and (b) a p-type MFIS-FTJ [8]. Symbols are the experimental data and lines are the simulation. For n-type,  $a_+ = 0.6$ ,  $a_- = 0.5$ ,  $b_+ = 0.52$ ,  $b_- = 0.3$ ,  $c_+ = 1.2$ ,  $c_- = 0.7$ ,  $d_+ = 11$ ,  $d_- = 40$ ,  $e_+ = e_- = 3$ , and  $f_+ = f_- = 0$ . For p-type,  $a_+ = a_- = 0.5$ ,  $b_+ = -0.2$ ,  $b_- = -0.4$ ,  $c_+ = 0.8$ ,  $c_- = 0.22$ ,  $d_+ = 2$ ,  $d_- = 15$ ,  $e_+ = e_- = 1$ , and  $f_+ = f_- = 0$ .



Fig. 5. The write and read test of the FTJ. The inset is the sample circuit. We show the corresponding reading current and polarization to this read/write operation.



Fig. 6. Transient test of this model by applying triangular waveform with varying amplitude for 1000 cycles. The simulated polarization and tunneling current are shown in (a) the 1<sup>st</sup> cycle (b) the 1000<sup>th</sup> cycle.

#### IV. CONCLUSION

We have presented a compact model of MFIS-FTJ. It contains a time-dependent multi-grain ferroelectric model, a semiconductor surface potential model and a tunneling current model. Because good analytical approximations are used and iterative calculation cycles are kept minimal, the model is computationally efficient for the simulation of integrated circuits. This model can fit both n-type and p-type FTJ experimental data well. Finally, we implemented this compact model in Verilog-A, ran with a commercial SPICE simulator, and demonstrated simulation speed comparable to MOS transistors and, therefore, its suitability for simulating large memory circuits. For future work, we could further study tunneling current under high applied voltage and the temperature dependency of the FTJ compact model.

#### REFERENCES

- L. Esaki, B. B. Laibowitz, and P. J. Stiles, "Polar switch," *IBM Tech. Discl. Bull.*, vol. 13, no. 8, p. 2161, 1971.
- [2] A. Chanthbouala *et al.*, "Solid-state memories based on ferroelectric tunnel junctions," *Nat Nanotechnol*, vol. 7, no. 2, pp. 101-4, Dec 4 2011, doi: 10.1038/nnano.2011.213.
- [3] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide CMOS compatible ferroelectric field effect transistors," presented at the 2011 International Electron Devices Meeting, Washington, DC, USA, Dec., 2011.
- [4] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, 2011, doi: 10.1063/1.3634052.
- [5] M. Y. Zhuravlev, R. F. Sabirianov, S. S. Jaswal, and E. Y. Tsymbal, "Giant Electroresistance in Ferroelectric Tunnel Junctions," *Physical Review Letters*, vol. 94, no. 24, 2005, doi: 10.1103/PhysRevLett.94.246802.
- [6] J. Yoon, S. Hong, Y. W. Song, J.-H. Ahn, and S.-E. Ahn, "Understanding tunneling electroresistance effect through potential profile in Pt/Hf0.5Zr0.5O2/TiN ferroelectric tunnel junction memory," *Applied Physics Letters*, vol. 115, no. 15, 2019, doi: 10.1063/1.5119948.
- [7] M. Kobayashi, Y. Tagawa, F. Mo, T. Saraya, and T. Hiramoto, "Ferroelectric HfO2 Tunnel Junction Memory With High TER and Multi-Level Operation Featuring Metal Replacement Process," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 134-139, 2019, doi: 10.1109/jeds.2018.2885932.
- [8] S. S. Cheema *et al.*, "Enhanced ferroelectricity in ultrathin films grown directly on silicon," *Nature*, vol. 580, no. 7804, pp. 478-482, Apr 2020, doi: 10.1038/s41586-020-2208-x.
- [9] Z. Wang et al., "Compact modelling of ferroelectric tunnel memristor and its use for neuromorphic simulation," *Applied Physics Letters*, vol. 104, no. 5, 2014, doi: 10.1063/1.4864270.

- [10] D. Pantel and M. Alexe, "Electroresistance effects in ferroelectric tunnel barriers," *Physical Review B*, vol. 82, no. 13, 2010, doi: 10.1103/PhysRevB.82.134105.
- [11] J. C. Ranuárez, M. J. Deen, and C.-H. Chen, "A review of gate tunneling current in MOS devices," *Microelectronics Reliability*, vol. 46, no. 12, pp. 1939-1956, 2006, doi: 10.1016/j.microrel.2005.12.006.
- [12] F. Mo, Y. Tagawa, T. Saraya, T. Hiramoto, and M. Kobayashi, "Scalability Study on Ferroelectric-HfO2 Tunnel Junction Memory Based on Non-equilibrium Green Function Method with Self-consistent Potential," presented at the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2018.
- [13] P. Chang, G. Du, J. Kang, and X. Liu, "Conduction Mechanisms of Metal-Ferroelectric- Insulator-Semiconductor Tunnel Junction on N- and P-Type Semiconductor," *IEEE Electron Device Letters*, vol. 42, no. 1, pp. 118-121, 2021, doi: 10.1109/led.2020.3041515.
- [14] H.-H. Huang *et al.*, "A Comprehensive Modeling Framework for Ferroelectric Tunnel Junctions," presented at the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019.
- [15] P. Chang, G. Du, J. Kang, and X. Liu, "Guidelines for Ferroelectric-Semiconductor Tunnel Junction Optimization by Band Structure Engineering," *IEEE Transactions on Electron Devices*, vol. 68, no. 7, pp. 3526-3531, 2021, doi: 10.1109/ted.2021.3079881.
- [16] C. T. Tung, G. Pahwa, S. Salahuddin, and C. Hu, "A Compact Model of Polycrystalline Ferroelectric Capacitor," *IEEE Transactions on Electron Devices*, pp. 1-4, 2021, doi: 10.1109/TED.2021.3100814.
- [17] W. J. Merz, "Domain Formation and Domain Wall Motions in Ferroelectric BaTiO3Single Crystals," *Physical Review*, vol. 95, no. 3, pp. 690-698, 1954, doi: 10.1103/PhysRev.95.690.
- [18] C. Alessandri, P. Pandey, A. Abusleme, and A. Seabaugh, "Monte Carlo Simulation of Switching Dynamics in Polycrystalline Ferroelectric Capacitors," *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3527-3534, Aug. 2019, doi: 10.1109/ted.2019.2922268.
- [19] A. K. Tagantsev, I. Stolichnov, N. Setter, J. S. Cross, and M. Tsukada, "Non-Kolmogorov-Avrami switching kinetics in ferroelectric thin films," *Physical Review B*, vol. 66, no. 21, Dec. 2002, doi: 10.1103/PhysRevB.66.214109.
- [20] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2 ed. Cambridge: Cambridge University Press, 2009.
- [21] T. R. Scavo and J. B. Thoo, "On the Geometry of Halley's Method," *The American Mathematical Monthly*, vol. 102, no. 5, pp. 417-426, 1995, doi: 10.2307/2975033.
- [22] A. Gruverman *et al.*, "Tunneling Electroresistance Effect in Ferroelectric Tunnel Junctions at the Nanoscale," *Nano Letters*, vol. 9, no. 10, pp. 3539-3543, 2009/10/14 2009, doi: 10.1021/nl901754t.
- [23] P. Zhang, "Scaling for quantum tunneling current in nano- and subnano-scale plasmonic junctions," *Sci Rep*, vol. 5, p. 9826, May 19 2015, doi: 10.1038/srep09826.
- [24] S. Banerjee and P. Zhang, "A generalized self-consistent model for quantum tunneling current in dissimilar metal-insulator-metal junction," *AIP Advances*, vol. 9, no. 8, 2019, doi: 10.1063/1.5116204.