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Fabrication of Metal-Semiconductor Heterostructures in Silicon Nanowires

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Fabrication of Metal-Semiconductor Heterostructures in Silicon Nanowires

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE
in Materials Science

by

Luyun Yang

Thesis Committee:
Assistant Professor Allon Hochbaum, Chair
Associate Professor Daniel Mumm
Associate Professor Regina Ragan

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TABLE OF CONTENTS

LIST OF FIGURES

ACKNOWLEDGMENTS

This thesis represents not only my work, but also the guidance, encouragement, and support of many people who made it possible. Upon writing this paper, I realize that I am nearing the end of my journey as a Master of Science candidate. I still remember the first day I entered Engineering Hall 3121, how ecstatic I was when I got the keys for the laboratory, and how cautious and curious I was at the beginning. Gradually, I became familiar with fellow labmates and the workings of the laboratory. Now I can close my eyes and still hear the laughter of labmates, see the layout of the laboratory, and recall things being done there. One year is a short amount of time for research, but I have learned much during this short period.

First and foremost, I want to offer my sincerest gratitude to my advisor, Professor Allon Hochbaum, who has patiently guided and supported me through all my lab work and thesis preparation. I first met Professor Hochbaum when I took his class, Crystalline Solids, and I was captivated by his knowledge and enthusiasm. He always patiently answered our questions after class and during office hours. I am very thankful that Professor Hochbaum offered me the chance to join his lab. I thoroughly enjoyed this project assigned by him. I also discovered that Professor Hochbaum not only cares about his classroom and research, but also about our lives outside of class. He checked on my wellbeing when I broke my leg, assisted me with my job hunting, and help me navigate the road to graduation.

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ABSTRACT OF THE THESIS

Fabrication of Metal-Semiconductor Heterostructures in Silicon Nanowires

By

Luyun Yang

Master of Science in Materials Science

University of California, Irvine, 2015

Professor Allon Hochbaum, Chair

The increasing demand for fossil fuels and the need to reduce greenhouse gases require clean energy sources and more efficient utilization of energy. Thermoelectric materials provide a means toward achieving these goals since they convert heat, including waste heat, directly into an electric potential difference. Metal-semiconductor heterostructures can work as Schottky barriers in thermoelectric materials to increase thermoelectric efficiency.

In this project, nickel silicide phases were introduced into silicon nanowires (SiNWs) to build up the Schottky barrier. SiNW arrays were fabricated using a metal-assisted chemical process, creating SiNWs about 200 nm in diameter and 30µm in length. Different methods were adopted for nickel deposition: electroless nickel deposition, electro nickel deposition, E-beam deposition, and thermal evaporation. The samples were examined by X-ray diffraction (XRD) and scanning electron microscopy (SEM). The results show that depositing nickel on SiNWs in an aqueous solution without electricity is a simple way to deposit nickel particles, and the morphology of nickel particles depends on the concentration of the deposition bath. However, an aqueous solution will cause oxidation of the SiNWs and hinder the formation of nickel silicide. To solve this problem, depositing nickel on SiNWs in organic solutions inside an oxygen-free glove box is a way to prevent oxidation, and nickel can diffuse into silicon substrates easily via annealing when there no oxidation layer on the surface of SiNWs. The dominant phase formed in these samples is $NiSi_2$ after being annealed at 650°C for one hour in a tube furnace.

Key words: thermoelectric, heterostructure, nickel deposition, silicon nanowires

1. Introduction

The emerging global need for energy production, conservation, and management has intensified interest in more effective means of power generation. Enhancements to existing energy supplies must come from a variety of renewable sources including solar, wind, biomass, and others. Another potential source of energy is electricity from heat sources utilized by thermoelectric materials. Heat can come from the combustion of fossil fuels, sunlight, or as a byproduct of various processes (e.g., combustion, chemical reactions, and nuclear decay). Therefore, thermoelectric materials can play a role in both primary power generation and energy conservation. A hot topic of discussion is how big this role is likely to be and the answer to this question depends solely on how efficient these materials are [1].

By no means should it be expected that thermoelectric energy conversion will solve the world's energy problems. However, it is hoped and expected that it will play a more increasing role than it has in the past and will be one of several technologies working together with other solutions to address energy efficiency issues. Thermoelectric modules are solid-state devices that directly convert thermal energy into electrical energy. This process is based on the Seebeck effect, which is the appearance of an electrical voltage caused by a temperature gradient across a material. The opposite is the Peltier effect which is the appearance of a temperature gradient upon the application of voltage [2].

1.1 History

The term "thermoelectric effect" encompasses three separately identified effects: the Seebeck effect, Peltier effect, and Thomson effect.

The first discovery of thermoelectric effects was in 1821, by T. J. Seebeck. He showed that an electromotive force could be produced by heating the junction between two different electrical conductors. The Seebeck effect can be demonstrated by making a connection between wires of different metals. The other ends of the wires should be applied to the terminals of a galvanometer or sensitive voltmeter. If the junction between the wires is heated, it is found that the meter records a small voltage. Seebeck found that the magnitude of the thermoelectric voltage is proportional to the difference between the temperature at the thermocouple junction and at the connections to the meter as shown in Figure 1.1(a) [3].

Thirteen years after Seebeck made his discovery, J. Peltier observed the second of the thermoelectric effects. He found that the passage of an electric current through a thermocouple produces a small heating or cooling effect depending on its direction as shown in Figure 1.1(b). The Peltier effect is quite difficult to demonstrate using metallic thermocouples since it is always accompanied by the Joule heating effect. Perhaps, one can do no better than show that there is less heating when the current is passed in one direction rather than the other [3].

It seems that it was not immediately realized that the Seebeck and Peltier phenomena are related to one another. However, this relationship was recognized by W. Thomson in 1855. By applying the theory of thermodynamics to the problem, he was able to establish a relationship between the coefficients that describe the Seebeck and Peltier effects. His theory also showed that there must be a third thermoelectric effect, which exists in a homogeneous conductor. This effect, now known as the Thomson effect, consists of reversible heating or cooling when there is both a flow of electric current and a temperature gradient [4].

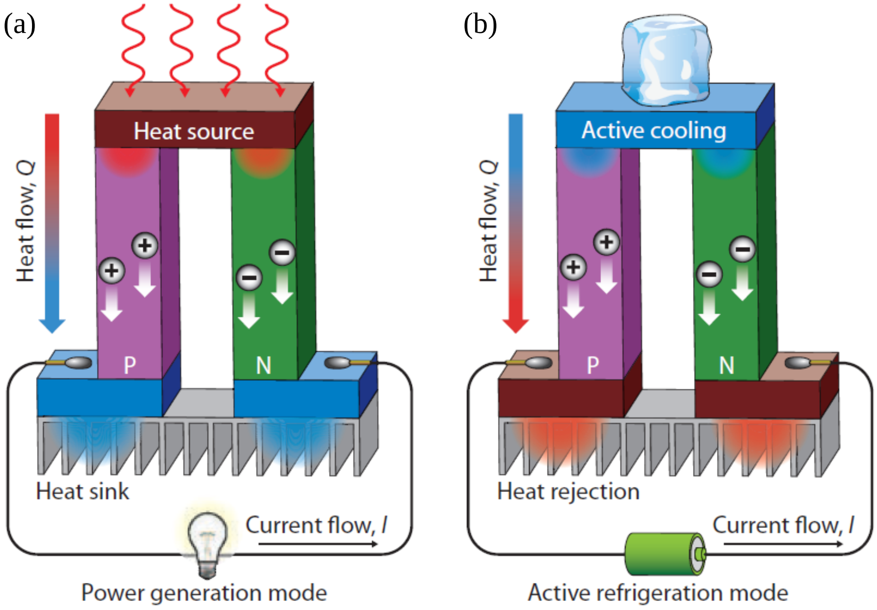


Figure 1. 1 Schematic illustrations of a thermoelectric module for (a) power generation (Seebeck effect) and (b) active refrigeration (Peltier effect). (a) An applied temperature difference causes charge carriers in the material (electrons or holes) to diffuse from the hot side to the cold side, resulting in current flow through the circuit. (b) Heat evolves at the upper junction and is absorbed at the lower junction when a current is made to flow through the circuit [5].

In the 1920s, Abram Ioffe introduced semiconductors as promising thermoelectric materials. Although metals show a high value of the ratio of electrical to thermal conductivity (σ/κ), the majority of them have a Seebeck coefficient S which does not exceed a few mV/K. In semiconductors S can reach values of up to one or more mV/K, but the ratio of the electrical to the thermal conductivity is smaller than in metals. However, this ratio can be easily manipulated by addition or removal of dopants. This implies that semiconductors are superior to metals in thermoelectric applications [6, 7].

1.2 Basic concepts of thermoelectricity

Thermoelectric device performance relies directly on the temperature gradient (ΔT) and an intrinsic material parameter, the thermoelectric figure of merit (zT). For power generation, the thermoelectric efficiency η is defined by combining the Carnot efficiency ($\Delta T/T_{hot}$) and the figure of merit zT as shown in Equation 1.1.

$$\eta = \frac{\Delta T(\sqrt{1+zT_{avg}}-1)}{T_{hot}(\sqrt{1+zT_{avg}}+\frac{T_{cold}}{T_{hot}})} \qquad (1.1)$$

where T_{hot} and T_{cold} are the temperatures of the hot and cold ends in a thermoelectric module and ΔT is their difference. The term $\sqrt{1+zT_{avg}}$ varies with the average temperature T_{avg}. This equation indicates that an increase in efficiency requires both high zT values and a large temperature gradient across the thermoelectric material. Thermoelectric devices currently available have a zT of 1 and will operate at an efficiency η of only about 5-6%. By increasing zT by a factor of 4, and depending on ΔT, the predicted efficiency η increases to 30%, a highly attractive prospect.

These properties define the dimensionless thermoelectric figure of merit zT:

$$\mathrm{zT} = \frac{s^2 \sigma\,\mathrm{T}}{k} \tag{1.2}$$

where T is the temperature. Producing high zT thermoelectric materials requires achieving simultaneously high electrical conductivity σ, high Seebeck coefficient S, and low thermal conductivity k in one solid [8]. These parameters are determined by the details of the electronic structure and scattering of charge carriers (electrons or holes), and thus are not independently controllable (ref. Figure 1. 2). The quantity $s^2\sigma$ is called the power factor (PF) and is the key to achieving high performance. A large PF means that a large voltage and a high current are generated. The thermal conductivity κ has a contribution from lattice vibrations, κ_{latt}, called the lattice thermal conductivity. Thus,

$$\kappa = \kappa_{\text{el}} + \kappa_{\text{latt}} \tag{1.3}$$

where κ_{el} is the carrier thermal conductivity. As κ_{el} is directly related to the electrical conductivity through the Wiedemann-Franz relationship ($\kappa_{\text{el}} = L_0\, \sigma\, T$), κ_{el} and PF cannot be varied independently. Intuitively, the thermal conductivity must be low as a large ΔT must be maintained; a large thermal conductivity will short the thermal circuit. zT also shows an opposing dependence on charge carrier density, while a large Seebeck coefficient also requires a high density of states at the Fermi level. As a consequence, the most promising thermoelectric materials are narrow bandgap semiconductors with charge carrier densities in the range of 10^{19}–10^{21} cm^{-3}.

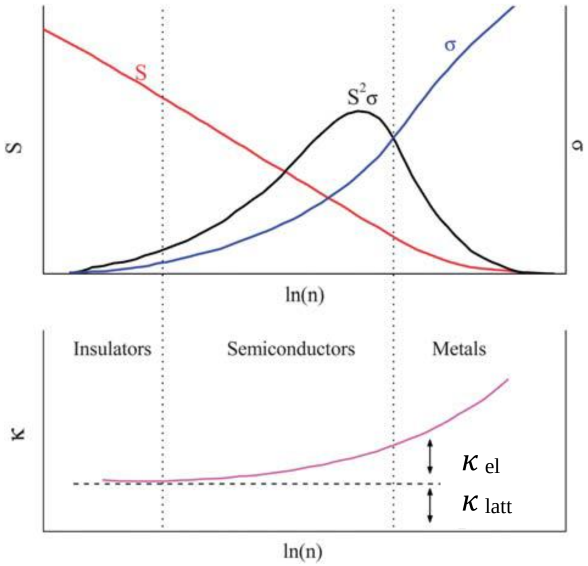


Figure 1. 2 Dependence of the Seebeck coefficient (S), electrical conductivity (σ), and the electronic (κ_{el}) and lattice (κ_{latt}) contributions to the thermal conductivity on the charge carrier concentration n, for a bulk material [9].

1.3 Theory of charge carrier and phonon transport at interface

Theoretical studies of phonon transport in superlattices show that reduction in lattice thermal conductivity does not need a well-defined geometry or a perfect interface at an atomic level. The only requirement is having a high density of interfaces, which is present in nano bulk structures. Therefore, to enhance the zT, the phonons have to be scattered more efficiently than charge carriers, which means the size of nanostructures should be smaller than the phonon mean free path and larger than the charge carrier mean free path. In practice, charge carriers have a narrower mean free paths than that of phonons. The interface spacing below which the electrical conductivity is reduced considerably can be estimated through the spectrum of the mean free path. Continued reduction in characteristic lengths in nanostructures has led to increasing importance of interfaces in transport properties of materials. In fact, a large portion of the advances in enhancing zT for nanostructured materials comes from the beneficial effects of the interfaces [10].

In a nano bulk material, grains and interfacial structures may have three distinct types as depicted in Figure 1.3. Type 1 (Figure 1.3a) is a nanocrystalline structure with a single material composition. Type 2 (Figure 1.3b) consists of embedded nanoparticles inside the lattice. Figure 1.3c is a nanocrystalline structure made from a mixture of two or more different materials or phases. In this structure the grains and/or the grain boundary regions are made from different materials. Experimentally, a nano bulk thermoelectric material may have a structure similar to any of these types or a combination of them [11]. For example, a peak zT of 1.4 at 100°C was achieved in a p-type nanocrystalline $Bi_{0.5}Sb_{1.5}Te_3$ bulk alloy using the type 1 methods to enhance the efficiency of thermoelectric materials 1 interface, which separates single phase crystallites [12]. Also, the p-type PbTe nanostructured bulk with SrTe precipitates, which demonstrated a zT value of 2.2 at 615°C, took advantage of the combination of Type 1 and 2 structures to more effectively scatter heat-carrying phonons across the integrated length scales [13]. A combination of Type 3 with 1 and/or 2 can make various other structures such as core–shell nanoparticle doped structures, or nanocrystalline structures with embedded nanoparticles [14].

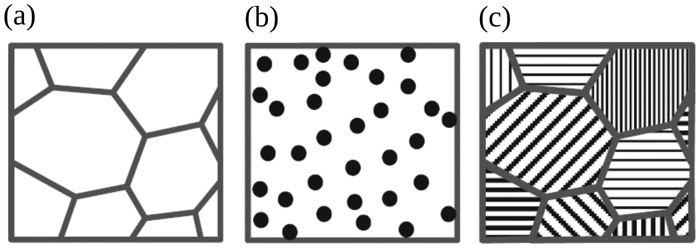


Figure 1. 3 Three types of nano bulk structures: (a) single component nanocrystalline material, (b) bulk material with embedded nanoparticles, (c) multicomponent nanocrystalline material [11]

The interface potential can also scatter only low energy carriers, which reduce their contribution. This phenomenon is called energy filtering [11]. The interface potential normally comes from the Schottky barriers between metal and semiconductor phases. In a sample, the minority carriers which have lower energy are affected by fabricating a nanostructure which scatters them more strongly than the majority carriers. The successful implementation of this strategy has been reported for InGaAs/InGaAlAs superlattice [15] and PbTe-based nanostructured materials [16, 17].

1.4 Thermoelectric materials

1.4.1 Bulk semiconductor alloys

Today, bulk semiconductor alloys are the most widely used thermoelectric materials and the materials with the highest efficiency, zT ≈ 1 [18]. Bulk semiconductor alloys are mainly found in three semiconductor compound families: (1) the V-VI compounds based mainly on Bi_2Te_3, which are used for applications in the room temperature range; (2) the IV-VI compounds based on PbTe, used in the 500 - 900K temperature range and (3) IV-IV compounds based on SiGe alloys. Neither Si nor Ge is a good thermoelectric material [19]. Although they have high electric conductivity, they also have high thermal conductivity, 113 and 63 W/mK at 300K for silicon and germanium, respectively [20], which leads to low zT. SiGe alloy has a high zT at high temperature (>900 K). Figure.1.4 shows the zT of typical n-type and p-type thermoelectric materials at different temperatures [16].

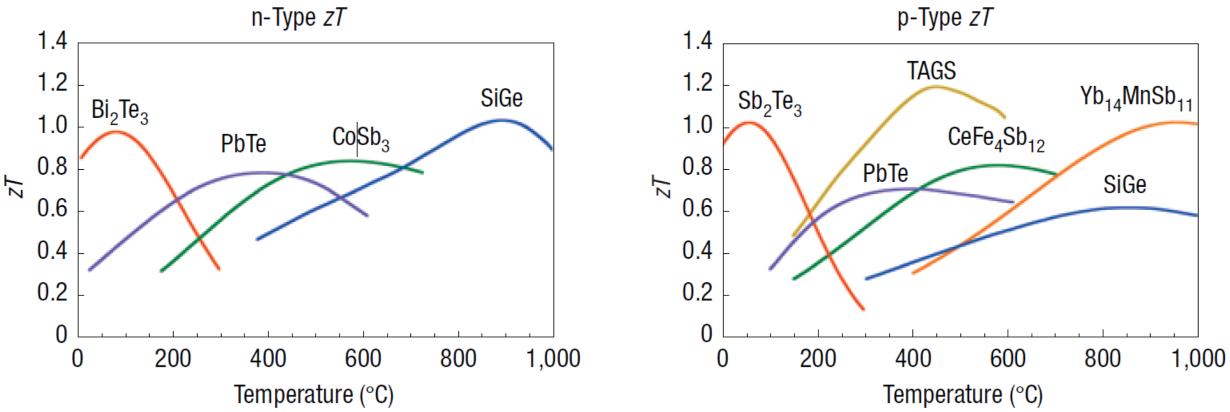


Figure 1. 4 zT of typical n-type and p-type thermoelectric materials at different temperatures [16]

By far the most widely used thermoelectric materials are alloys of Bi_2Te_3 and Sb_2Te_3. Bi_2Te_3 was first investigated as a material of great thermoelectric promise in the 1950s. For near-room-temperature applications, such as refrigeration and waste heat recovery up to 200 °C, Bi_2Te_3 alloys have been proven to possess the greatest figure of merit for both n- and p-type thermoelectric systems [21].

1.4.2 Nanostructured materials

The main advantage of low-dimensional materials is that their size can be made smaller than the mean free path of phonons, but larger than that of electrons and holes. This brings about a reduced κ, without compromising the other zT parameters [22]. These materials may be classified as nanotubes, nanowires, nanorods, nanoparticles, quantum well, super lattices, and ultra-thin films.

Carbon Nanotubes

A carbon nanotube (CNT) is composed of a graphene sheet formed into a seamless cylinder. There are two types of nanotubes, single-walled nanotubes (SWNT) and multi-walled nanotubes (MWNT), with the latter composed of concentric SWNTs. Carbon nanotubes are rich in charge carriers with $\sigma = 10^6$ S/m, S of 80 µV/K for single MWNTs at 300 K [23], and 40 µV for SNWTs

[24]. However, they exhibit extremely high κ, 3000 W/mK for MWNT and up to 10^4 W/mK for SWNT. This results in a very low zT of 6.4×10^{-4} for MWNTs and 4.8×10^{-4} for SWNTs. In order to decrease the κ, an approach to the nanotube composition has been considered. Introduction of C_{60} molecules within the core of SWNTs could act as a typical way to a reduced κ [25].

Superlattices

Superlattices consist of alternating thin layers of different materials stacked periodically. The lattice mismatch and electronic potential differences at the interfaces and resulting phonon and electron interface scattering and band structure modifications can be exploited to reduce phonon heat conduction while maintaining or enhancing the electron transport [19]. Superlattices are anisotropic. Different mechanisms to improve zT along directions both parallel (in-plane) and perpendicular (cross-plane) to the film plane have been explored. Along the in-plane direction, potential mechanisms to increase zT include quantum size effects that improve the electron performance by taking advantage of sharp features in the electron density of states [26], and reduction of phonon thermal conductivity through interface scattering [27]. Along the cross-plane direction, one key idea is to use interfaces for reflecting phonons while transmitting electrons (phonon-blocking/electron transmitting) [28], together with other mechanisms, such as electron energy filtering [29] and thermionic emission [30], to improve electron performance.

Several groups reported in recent years enhanced zT in various superlattices such as Bi_2Te_3/Sb_2Te_3, as well as Bi_2Te_3/Bi_2Se_3 [31] and PbSeTe/PbTe quantum dot superlattices [32] (ref. Figure 1.5). The large improvements observed in these materials systems, compared with their parent materials, are of great importance for both fundamental understanding and practical applications.

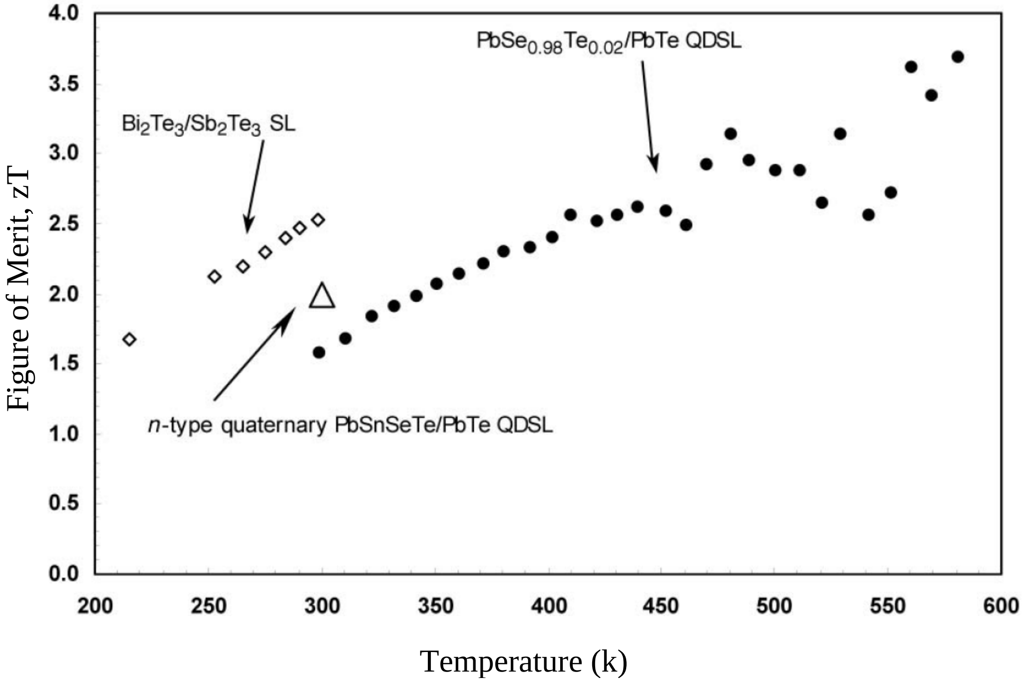


Figure 1. 5 Thermoelectric figure of merit zT for Bi_2Te_3 /Sb_2Te_3 superlattices (SL), PbSnSeTe/PbTe quantum dot superlattices (QDSL), and PbSeTe/PbTe quantum dot superlattices (QDSL) [31][32]

Layered Co oxides

Oxides seem hopelessly poor as thermoelectric materials. First, most of them show high lattice thermal conductivity due to a high sound velocity, because light oxygen ions are tightly bound. Second, the electrical conductivity is usually lower than that of other semiconductors [33]. However a new window has opened to oxide thermoelectrics since the discovery in 1997 of a large power factor in a single crystal sample of the layered cobalt oxide $Na_xCoO_2(NaCo_2O_4)$ [34]. The crystal showed a low resistivity of 200 μΩcm (5,000 S/cm) with a large thermopower of 100 μV/K at room temperature along the in-plane direction. The room-temperature power factor is as large as that of Bi_2Te_3, which clearly indicates that some oxides can be thermoelectric materials. Later, Fujita et al. [35] found a reasonably low thermal conductivity (50 mW/cmK at 800K) for a single-crystal sample, and evaluated zT to be unity at 1,000K. Ohtaki et al. [36] and Ito et al. [37] reported $zT \approx 0.8$ at 1,000K, even in polycrystalline samples of Na_xCoO_2.

Oxide thermoelectrics have been extensively investigated in the last decade, and a number of new oxides have been synthesized and examined as possible candidates for oxide thermoelectric materials [38]. Figure 1.6 shows the crystal structures of various layered cobalt oxides. All of them have in common the CdI_2-type CoO_2 block, which alternately stacks with various block layers along the c axis. The CdI_2-type CoO_2 block is hexagonal, whereas the various block layers, except for the Na layer, crystallize in the NaCl structure with tetragonal symmetry. Their crystal structure is an alternate stack of square and triangle sheets, which causes lattice mismatch at the interface between the blocks.

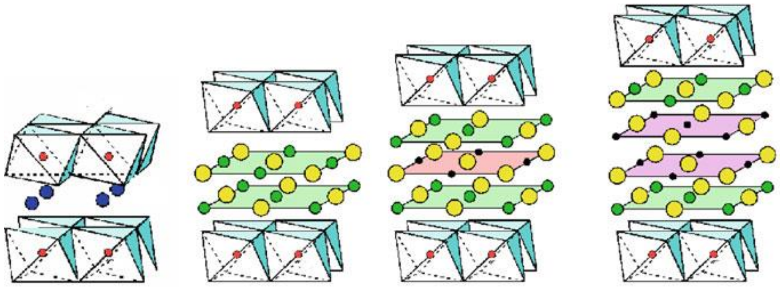


Figure 1. 6 Crystal structures of layered cobalt oxides. The CoO_2 block, common to each structure, is responsible for electric conduction. Except for Na_xCoO_2, the unit cell consists of the NaCl-type block and the CdI_2-type CoO_2 block [33].

Silicon Nanowires

Heavily doped bulk silicon, 10^{19} cm^{-3}, has a very poor zT value which approaches 0.01 at 300 K [39] due to a high thermal conductivity κ = 150 W/mK at room temperature [40]. However, with reduced dimensions, an increase in zT is expected because the mean free path is reduced due to phonon-boundary scattering.

Hochbaum et al. [41] obtained zT values of 0.60 at room temperature in wires that were approximately 50 nanometers in diameter. They synthesized p-type SiNWs by using a metal-assisted electroless etching method and a vapor-liquid-solid (VLS) grown gold-catalyzed method. The electroless etched SiNWs were rougher than the VLS grown SiNWs, with the former having an average surface roughness of the order of several nm (1-5 nm), which had a lower thermal conductivity κ. To measure the thermal conductivity, a single NW was suspended between two membranes, one acting as a heater and the other as a heat sink, as shown in Figure 1.7(a) According to Chen et al. [42], the thermal conductance of individual single crystalline silicon nanowires is related to the diameter of the nanowire, which can be explained by the fact that the mean free path is proportional to the diameter and is independent of the phonon frequency.

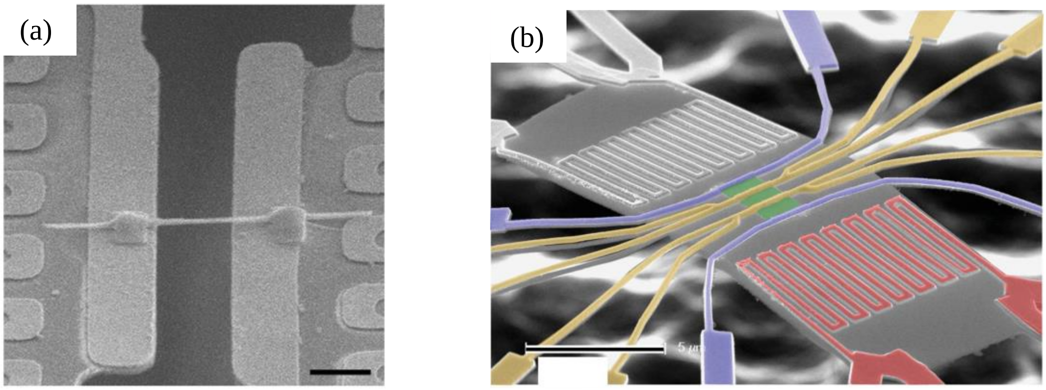


Figure 1. 7 (a) SEM image of a Pt-bonded EE Si nanowire (taken at 52° tilt angle). The Pt thin film loops near both ends of the bridging wire are part of the resistive heating and sensing coils on opposite suspended membranes [41].

(b) The central green area is the Si nanowire array, which is not resolved at this magnification. The four-lead yellow electrodes are used for thermometry to quantify the temperature difference across the nanowire array. The thermal gradient is established with either of the two Joule heaters (the right-hand heater is colored red). The yellow and blue electrodes are combined to carry out four-point electrical conductivity measurements on the nanowires [42].

Boukai et al. [8] measured the thermal characteristics of ~100 p-SiNWs in parallel. They reported a zT≈1 at 200 K, and their measured κ = 0.99W/mK is below the theoretical limit for silicon. NWs were fabricated by the superlattice nanowire pattern transfer (SNAP) method. The atomic control over the layer thickness of the superlattice allows manipulation in the spacing and width of the nanowires. NW arrays of several micrometers in length were prepared with lateral width × thickness dimensions of 10 nm × 20 nm and 20 nm × 20nm. Figure 1.7(b) shows a scanning electron micrograph (SEM) image of the suspended platform used to measure the thermal characteristics of the SiNWs. This is indicated in the figure by the green color.

Tang et al. [43] studied a different form of nanostructure, “holey” silicon. High density nanoscopic holes of p-Si with dimensions of 350, 140 and 55 nm were created in thin 100 nm single crystalline silicon membranes, either by nanosphere lithography or block co-polymer lithography. Holey silicon nanoribbons were characterized by a micro-electromechanical system device, shown in Figure 1.8(d). SEM images of the nanoribbons of 350 nm, 140 mm, and 55 nm are shown in Figure 1. 8(a) - (c). The temperature dependence of zT for the 55 nm ribbons achieved a maximum value of ~0.4 was achieved at 300 K. This corresponds to a 40 times increase in the zT compared to their parent bulk Si.

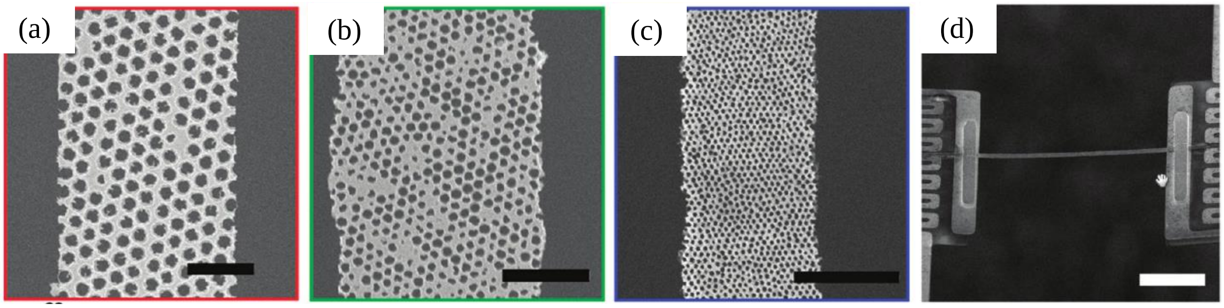


Figure 1. 8 SEM image of (a) 350 nm pitch, (b) 140 nm pitch, (c) 55nm pitch, (D) SEM image of a single electroless etched NW bonded to two platinum bridges that act as a heater [43]

1.5 Thermoelectric applications

There are mainly two types of commercially available multicouple thermoelectric devices. Type A was originally designed for cooling applications and possesses significant inter-thermoelement separation. In this type of device, n- and p-type semiconductor thermoelements are connected electrically in series by highly conducting metal strips and sandwiched between thermally conducting and electrically insulating plates. Type B has been developed more recently for power generation and is densely constructed with very small inter-thermoelement separation to increase the power-per-area. However, the conducting metal strips in the latter device are not insulated and the module cannot be attached directly to an electrical conductor, such as an aluminum heat sink [44].

Thermoelectric devices cannot be used independently. They should be connected to heat exchangers to dissipate heat, forming the basis of thermoelectric systems. The development of thermoelectric systems has been ongoing for many years. Thermoelectric systems are usually small heat pumps or power generators, which follow the laws of thermodynamics in the same manner as mechanical heat pumps, vapor compressors associated with conventional refrigerators, and other apparatus used to transfer energy [45].

Thermoelectric devices offer several distinct advantages over other technologies: Thermoelectric devices have no moving parts and, therefore, need substantially less maintenance. Life testing has shown the capability of thermoelectric devices to exceed 100,000 hours of steady state operation. Thermoelectric devices contain no chlorofluorocarbons or other materials that may require periodic replenishment. Also, the direction of heat-pumping in a thermoelectric system is fully reversible. Changing the polarity of the DC power supply causes heat to be pumped in the opposite direction - a cooler can then become a heater. Precise temperature control to within ±0.1°C can be maintained using thermoelectric devices and the appropriate supporting circuitry. Thermoelectric devices can function in environments that are too severe, too sensitive, or too small for conventional refrigeration. Thermoelectric devices are not position-dependent. Due to all the above advantages, thermoelectric devices have found very extensive applications in the past decade in wide areas, such as military, aerospace, instrument, industrial, and commercial products. These applications can be classified into three categories: coolers (or heaters), power generators, and thermal energy sensors [46].

Applications of thermoelectric devices as coolers

Thermoelectric coolers are widely employed in microelectronics to stabilize the temperature of laser diodes, to cool infrared detectors and charge-coupled devices, and to reduce unwanted noise in integrated circuits. In addition to cooling electronic devices, thermoelectric devices are widely used in other niche applications where the cooling demands are not too great (such as portable cooler boxes) or instances in which the energy cost is not the main consideration (such as military applications). However, their applications in cooling large thermal capacity components or spaces have been limited, due to the relatively low efficiency and high energy cost [45].

For commercial silicon chips, efficient hot spot removal is key for future generations of IC chips. Circulated liquid cooling allows for moving the heat sink away from the processor, thus allowing for a larger heat sink surface area [11]. However, reliability is a big concern, for example, if the system leaks coolant. The other widely used technology is thermoelectric module cooling. Thermoelectric cooling is a silent and environmentally-friendly solution. However, the hot spots in microprocessors are normally on the order of 300-400 μm in diameter, so even the smallest commercial cooling module is still too large to be used for spot cooling. In addition, the introduction of silicon stacked chips and three-dimensional (3D) chips can lead to even smaller and hotter spots. Nanoscale coolers with high efficiency will be key enablers for removing small hot spots in IC chips and for improving future IC thermal management [47].

Application of thermoelectric devices for power generation

Electrical power for small, independent and wireless systems for remote sensing, control, safety surveillance, and metering comes mainly from batteries. Since battery life is limited, battery-operated systems have to be maintained or replaced after a few years. Furthermore, batteries contain chemical substances that are harmful to the environment. For this reason, the disposal of battery-operated systems has to be controlled, which can be an expensive procedure. One common alternative is the use of solar cells, such as those used in calculators and watches. In low-light or no-light applications, small temperature differences which are present can be used to operate a small thermoelectric generator. Therefore, small, inexpensive, and efficient thermoelectric generators are gaining importance as replacements for batteries in many systems [48]. One actual example is a small preamplifier and a sensor control system powered by a thermoelectric generator generating an electrical power of 1.5 μW from a temperature difference of 10 °C [48].

For low power generation, the low efficiency of thermoelectric generators is not a main drawback. But for high power generation, low efficiency is a disadvantage and has limited its application to specialized areas. In recent years it has been realized that in situations where the supply of heat is inexpensive or free, as in the case of waste heat, efficiency of the thermoelectric generation system is not an overriding consideration. The use of waste heat as an energy source, particularly at temperatures below 140°C, substantially increases the commercial competitiveness of this method of generating electrical power [49].

Currently available is a standard device consisting of 71 thermocouples in a 75 mm^2 package, producing 19 W (www.hi-z.com). The world's largest supplier of thermoelectric generators, Global Thermoelectric Inc., provides thermoelectric generators ranging in output from 15 to 550 W, in module sizes from 508 mm × 279 mm × 483 mm to 1549 mm × 1549 mm × 1016 mm (www.globalte.com).

2. Methodology

In novel nanoscale thermoelectric materials, silicon nanowires (SiNWs) are appealing choices because of their small sizes and ideal interface compatibility with conventional Si-based technology [50-52]. In SiNWs, the electrical conductivity and electron contribution to the Seebeck coefficient are similar to those of bulk silicon, but they exhibit a 100-fold reduction in thermal conductivity [50], showing that electrical and thermal conductivities can be decoupled. Recent experiments have provided direct evidence that an approximately 100-fold improvement of thermoelectric figure of merit zT values over bulk Si is achieved in SiNWs over a broad temperature range. This large increase of zT is attributed to the decrease of thermal conductivity. This has raised the exciting prospect that SiNWs can be used as novel nanoscale thermoelectric materials [53, 54].

The intent of this project was to enhance the thermoelectric performance of SiNW arrays by introducing the heterogeneous silicide phase. The heterogeneous silicide phase acts as a phonon scattering interface to reduce the thermal conductivity of nanowires and increase zT.

2.1 Fabrication of silicon nanowires

In the bottom-up nanowire synthesis approach, the most common methods are vapor-liquid-solid (VLS) growth and, more recently, metal-assisted chemical etching. In the VLS method, a liquid-phase metal nanoparticle catalyst is used to form the SiNW. Silicon precipitation occurs in the nanoparticle, followed subsequently by SiNW growth [55]. The diameter of the nanostructures is a function of the diameter of the alloy droplet at its tip. In recent years, there has been interest in the metal-assisted chemical etching process because of its simplicity and low-cost, which allows control over different parameters, such as diameter, length, orientation, doping type, doping level, and cross-sectional shape.

A disadvantage of metal-assisted chemical etching is the rough surface of the nanowires. However, this may represent an advantage when used for thermoelectricity, due to increased surface scattering of phonons, leading to a reduced thermal conductivity [41, 56]. For this project, the metal-assisted chemical etching process was used.

2.1.1 Fabrication mechanism

In this project, the fabrication of SiNWs by metal-assisted chemical etching was based on a two-step process. In the first step, metal is deposited by electroless deposition or galvanic exchange. In the second step, SiNW etching or formation is achieved in a solution of HF, or a combination of HF and H_2O_2. Noble metal ions are reduced at the Si surface through a cathodic process and oxidation of Si atoms at the Si surface occurs, i.e., an anodic reaction. Typically, the metals used consist of Ag in a solution form ($AgNO_3$), Au, and Pt. They can be deposited on the Si substrate via various methods, including thermal evaporation, sputtering, electron beam (E-beam) evaporation, electroless deposition, electrodeposition, focused-ion-beam (FIB)-assisted deposition, and spin-coating of particles. Electroless deposition is a simple method that is usually utilized to deposit noble metals if there is no strict demand on the morphology of the resulting etched structures. In this project, the electroless deposition of silver was adopted. As the electrochemical potential of noble metals compared to Si is more positive, a galvanic displacement reaction occurs in Si by injection of holes into the valence band; ref. Figure 2.1(a). Metal ions are further reduced on the Si surface by electrons provided by the Si-Si bonds [57].

The cathodic and anodic reactions taking place on the surface of the Si can be highlighted in the following equations [57]:

$$Ag^+ + e^- \rightarrow Ag^0(0) \qquad (1)$$
$$Si(s)+2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \qquad (2)$$
$$SiO_2(s) + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad (3)$$

where Eq. (1) corresponds to the cathode reaction and Eq. (2) and (3) to the anode reaction. If H_2O_2 is added into the reaction solution, the cathodic reaction of H_2O_2 will occur on the Ag metal surface, with a reaction given by:

$$H_2O_2 + 2H^+ + 2e^- \rightarrow 2H_2O$$

When Ag is used as a metal, Ag^+ ions in the proximity of the silicon surface capture electrons from the valence band of silicon; ref. Figure 2.1(b). Meanwhile, holes are generated in the Si valence band when the Ag^+ is reduced to Ag nuclei. Deposition and growth of Ag nuclei facilitates the formation of SiO_2 underneath the silver nanoparticles; ref. Figure 2.1(c). SiO_2 is then etched away by HF, with the nanoparticles sinking into the silicon and forming SiNWs, as shown in Figure 2.1(d) [58, 59].

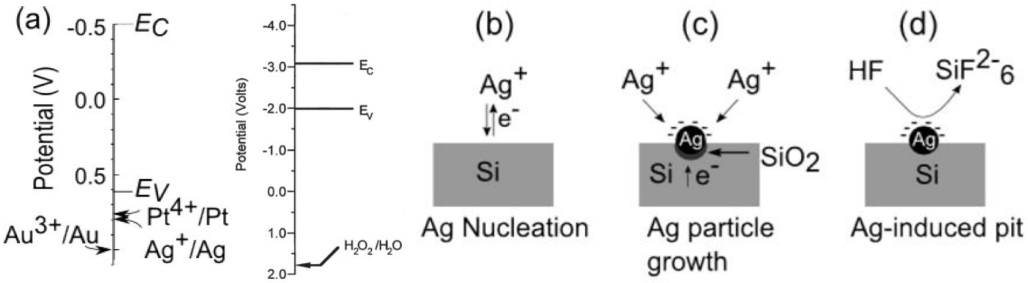


Figure 2. 1 (a) Qualitative diagram of the comparison of electrochemical electron energy levels of Si band edges and the redox systems, $AuCl_4^-$ /Au, $PtCl_6^{2-}$/Pt, Ag_4^+/Ag, H_2O_2 in HF solution. E_C and E_V are the conduction and valence band of Si, respectively. (b) - (d) Process of electroless silver deposition on a Si substrate immersed in HF/$AgNO_3$ solution. After Ag nanoparticles are deposited on the Si surface, HF starts to etch the silicon substrate [57].

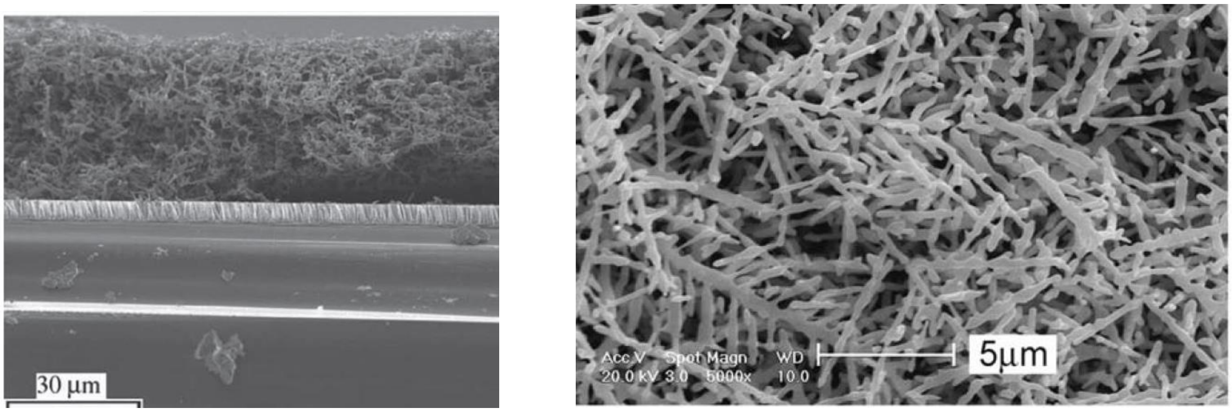


Figure 2. 2 SEM images of silicon substrates etched with HF/$AgNO_3$ with Ag dendrite structures [58, 60]

An important question is why lateral etching does not occur. According to Peng, Hu et al., the pore diameter is determined by the size of the metal particle. They suggest that the charge exchange and transport between the anodic and cathodic sites would be more favorable at the metal-Si interface than at the pit wall, because the metal-Si interface has the shortest charge-transport distance, and because of the unique catalytic property of the metal particle, which greatly decreases E_a for the cathodic reaction. Accordingly, oxide formation and the dissolution of silicon would more favorably occur at the pore tips (the metal-Si interface) than at the pit walls. That is, longitudinal etching would be more favored than lateral etching; thus, deep pores would finally be formed, owing to the prolonged longitudinal etching of silicon. However, a puzzling problem is that the pores generated with stable Pt particles are not as straight as those obtained with Ag and Au particles. Therefore, the nature and propagation of the metal-Si interface during Si oxidation and dissolution should be addressed to clarify this etching mechanism.

By varying the concentration of $AgNO_3$ and HF, the diameter of the resulting SiNWs (arising from overlapping pores) can be roughly tuned.

2.1.2 Influencing factors

Doping type and doping level

Different conclusions concerning the relationship between etching rates and doping types or doping levels of the Si substrate have been reported. Li et al. found that under identical conditions Au-covered regions on a p^+ (0.01–0.03 Ω cm) Si substrate and Au-covered regions on a p^- (1–10 Ω cm) substrate show only small variations in pore size and etching depth [61], while Cruz et al. reported that the etching depth in Au-covered regions of a p^- (10 Ω cm) Si substrate is 1.5 times larger than that of a p^+ (0.01 Ω cm) Si substrate, under identical conditions [62]. The reason for different etching rates for substrates with different doping levels remains unclear so far. Concerning the doping type, Zhang et al. found that a p-type (7–13 Ω cm) substrate is etched more slowly than an n-type (7–13 Ω cm) substrate. This relationship is valid for both (100) and (111) substrates [62]. Besides influencing the etching rate, the doping level of the Si substrate also influences the morphology of the etched structures. With increasing doping levels, Si nanowires resulting from metal-assisted chemical etching become rougher [63] and finally evolve into nanowires containing micro pores.

Orientation of silicon substrate

Experiments in early years showed that, indeed, in (100) and (111) substrates the etching proceeded along the vertical direction [57]. However, it was later revealed that non-vertical etching occurs in (111) and (110) substrates, resulting in slanting, aligned Si nanostructures, as shown in Figure 2.3 [64, 65]. The non-vertical, metal-assisted chemical etching (i.e., the anisotropic etching in certain preferred crystallographic directions) is ascribed to the back-bond breaking theory [66, 67], which has already been used to explain the anisotropy in the anodic HF etching of Si [68] and the etching of Si in an alkaline solution [69]. For the oxidation or dissolution of a Si atom on the surface of a substrate, it is necessary to break the back-bonds of the surface atom that connect to the atoms underneath. The stronger the back-bond strength, the more difficult it is to remove the surface atom. The number of back-bonds in a Si atom on the surface is determined by the crystallographic orientation of the substrate. Each atom on the surface of a (100) substrate has two back-bonds, while an atom on the (110) or (111) surface has three back-bonds [70]. Due to the different back-bond strength, the Si atom on the (100) surface plane is the most easily removed, and the etching occurs preferentially along the < 100 > directions.

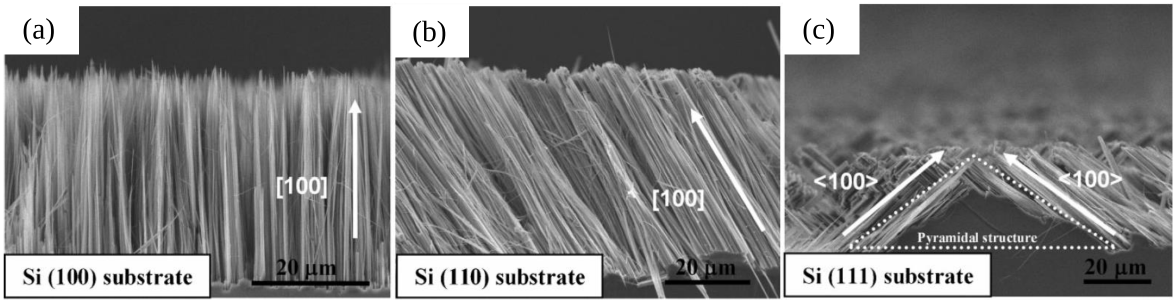


Figure 2. 3 Cross section SEM images of SiNWs formed on a Si (100) substrate (A), a Si (110) substrate (B) and a Si (111) substrate (C) [64, 65]

However, the influence of the etching anisotropy on the etching rate of a Si substrate (measured as the change in the etching depth vertically to the surface) remains puzzling. Huang et al. found that in the same etchant and for the same etching time, the etching depth of a (110) substrate etched along the < 100 > directions is almost the same as the etching depth of the same substrate etched along the [110] direction [71]. Zhang et al. found similar phenomena in the etching of (111) and (100) substrates with a different doping type, but the same doping level, despite the different etching direction [63].

Etching temperature

It has been reported that the length of Si nanowires fabricated by metal-assisted chemical etching in HF/$AgNO_3$ solution or HF/H_2O_2 solution increases approximately linearly with the etching time. Cheng et al [72] systematically studied the relationship between the etching time and the lengths of Si nanowires etched at different temperatures.

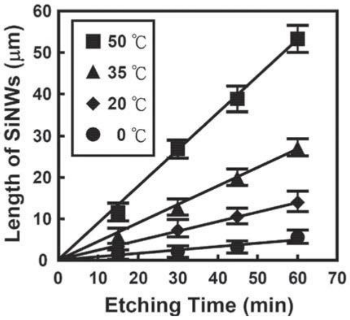


Figure 2. 4 Relationship of length of SiNWs and etching times at different temperatures [72].

With a temperature in the range of 0°C to 50°C, a linear relationship between the length of nanowires and etching time at all temperatures is confirmed (Figure 2.4). The observed etching rate increases with increasing etching temperature.

Type of metal

The morphologies of Pt and Cu electroless deposited from an HF-containing deposition solution look different from those of Ag and Au. With increased etching time, Pt and Cu tend to form a dense film on the surface of the Si substrate [73] rather than dendrite structures. The dense metal film further hinders the access of HF to the surface of the Si substrate and, therefore, blocks the further etching of the Si substrate [57].

The specific type of noble metal influences the etching rate. The rate of etching assisted by Pt is much faster than that assisted by Au [74]. Moreover, the pores in or wires on substrates etched in the presence of Pt are usually surrounded by a porous layer [75], while no observable porous layer is found about the pores or wires etched from Au-coated [65] or Ag coated [76] substrates under otherwise identical conditions. The difference in the etching rate and morphologies of the etched structures has not yet been well-explained. The difference in the catalytic activity of the noble metal for the H_2O_2 reduction might be a possible reason, although there is no literature directly comparing the catalytic activities of Pt, Au, and Ag particles on Si substrates for H_2O_2 reduction. As hole injection is necessary for the etching of Si, when more holes are injected, the etching is faster. When more holes are injected, the possibility that holes diffuse from the etching front to the sidewall of the etched structure (e.g., pores or wires) increases, favoring the formation of a microporous structure on the sidewalls of etched structures.

Concentration of etchant

Chartier et al. [77] systematically studied the influence of the HF/H_2O_2 ratio on the etching rate and on the etched morphologies of Si substrates (p-(100), 1–2 Ω cm) on which isolated Ag particles were deposited by electroless deposition. The morphologies of the etched structures are determined by the parameter ρ, defined as [78]/ ([78] + [H_2O_2]). With 100% > ρ > 70%, Ag particles induce straight cylinder pores, the diameters of which match well those of the Ag particles at the bottom. With 70% > ρ > 20%, cone-shaped pores form. The diameter of the pore tip is the same as the diameter of the Ag particle located there, while the opening of the pore at the surface of the Si substrate has a diameter larger than that of the Ag particle. For ρ below 30%, the cone-shaped pores are surrounded by microporous Si, which look similar to the structure etched with Pt particles in low HF concentration [65]. With 20% > ρ > 9%, Si evolves into crater-like structures with opening diameters of several micrometers. With 9% > ρ > 0%, neither porous nor crater structures form and a macroscopically smooth, but nanoscopically pitted surface, develops.

The relationship between etching morphologies and ρ is explained as follows [74]: For 100% > ρ > 70% (i.e., a high percentage of HF), the etching rate is almost completely determined by the concentration of H_2O_2 and nearly all holes generated at the Ag/Si interface at the pore tip are locally consumed because there is sufficient HF available to dissolve Si (or SiO_x, if this occurs as an intermediate reaction product). When ρ is less than 70%, the etching rate is determined by the concentration of HF. In this case, the consumption rate of the holes at the pore tip is lower than the generation rate. Accordingly, unconsumed excess holes can diffuse away from the tip to the side wall of the pore. Hence, microporous Si forms on the sidewall of the pore. With very small ρ, or very high H_2O_2 concentration, hole diffusion is pronounced and the diffused holes come to every exposed surface of the Si substrate. Consequently, oxidation and dissolution of Si occur everywhere and the etching is isotropic and independent of the location of Ag particles, resulting in a polished surface.

2.2 Silicide heterojunction

2.2.1 Mechanisms for increasing figure of merit (zT)

According to $zT=S^2\sigma T/\kappa$, there are two approaches to increase zT: the power factor ($S^2\sigma$), which includes the Seebeck coefficient S, is maximized and/or the thermal conductivity κ is minimized.

In this project a theoretical model of the thermoelectric properties of bulk semiconductors containing metallic nanoparticles is introduced. This model considers energy-dependent scattering of electrons and phonons on the band bending at the interfaces between the semiconductor hosts and randomly distributed metallic islands. This leads to an energy filtering effect that increases the Seebeck coefficient. This provides an explicit physical model for the proposed energy filtering effect [79].

While the role of metallic nanoinclusions may appear at first to be similar to that of point defects for which extensive work has been done, the physics is actually quite different. Indeed, in addition to electron scattering, phonon scattering on nanoinclusions occurs in a completely different regime than that on point defects [79].

The central idea of Faleev and Léonard is illustrated in Figure 2.5 [80]. There, spherical metallic nanoinclusions with radius R are randomly distributed in a bulk semiconductor material; ref. Figure 2.5(a). In general, at such metal-semiconductor interfaces, charge transfer between the metal and the semiconductor leads to bands bending away from the interface, which is called the Schottky barrier; ref. Figure 2.5(b). The presence of this potential causes energy-dependent scattering of electrons and phonons, as illustrated in Figure 2.5(c). The high energy electrons are unaffected by the potential, but the low energy electrons can be strongly scattered, resulting in decreased thermal conductivity.

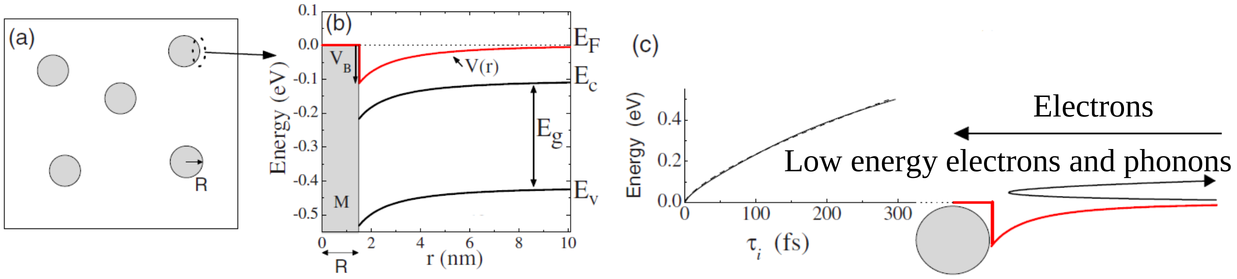


Figure 2. 5 (a) Schematic of the semiconductor host with metallic nanoinclusions. (b) Example of the calculated potential V(r) and the Schottky barrier. (c) Illustrates the concept of energy filtering: low energy electrons and phonons scatter strongly due to the potential barrier, but high energy electrons are unaffected [80]..

To explain the increase of the power factor $S^2\sigma$, the Mott relation for the Seebeck coefficient is used [81]. An electrical conductivity σ (E) is associated with the electrons that fill the energy levels between E and E+dE, irrespective of the mechanism that limits σ (E). The total electrical conductivity is then the integral of this over the entire energy range, moderated by the Fermi distribution function $f_0(E)$. Integrating by parts, the total conductivity is:

$$\sigma = \int_0^\infty \sigma(E)\left(-\frac{\partial f_0(E)}{\partial E}\right) \mathrm{d}E \tag{2.1}$$

Cutler and Mott [82] derive the Seebeck coefficient in this analysis to be the differential form of the Mott relation:

$$S = \frac{k_{\mathrm{B}}}{q}\frac{1}{\sigma}\int_0^{\infty} \sigma(E)\left(\frac{E-E_{\mathrm{F}}}{k_{\mathrm{B}}T}\right)\left(\frac{\partial f_0(E)}{\partial E}\right) \mathrm{d}E \tag{2.2}$$

In systems in which the Fermi statistics are degenerate, such as metals and degenerately doped semiconductors, Eq. (3.2) simplifies to the better-known form of the Mott relation:

$$S = \frac{\pi^2}{3}\frac{k_{\mathrm{B}}}{q}\, k_{\mathrm{B}}T \left\{\frac{\mathrm{d}[\ln(\sigma(E))]}{\mathrm{d}E}\right\}_{E=E_F} \tag{2.3}$$

This is generally valid, whether conduction is through band states, localized states, hopping or other mechanisms. In the particular case of band conduction, the differential conductivity can be expressed by the product of the density of carriers n(E), which is a function of the density of states g(E), and their differential mobility μ(E) or relaxation time τ (E):

$$\sigma(E) = n(E)e\mu(E) = n(E)e^2\frac{\tau(E)}{m^*} \tag{2.4}$$

where e is the free electron charge, and m^* the effective mass (in solids with non-parabolic bands, $m^* = m^*$ (E)). From Equations 3.3 and 3.4, the Seebeck coefficient becomes:

$$S \propto \frac{1}{n}\frac{\partial n(E)}{\partial E} + \frac{1}{\mu}\frac{\partial \mu(E)}{\partial E} \tag{2.5}$$

Thus, there are two ways to enhance S, namely enhancing $\frac{\partial n(E)}{\partial E}$ or enhancing $\frac{\partial \mu(E)}{\partial E}$.

Increasing $\frac{\partial n(E)}{\partial E}$ can be achieved by enhancing the dependence of the density of states on energy, $\frac{\partial g(E)}{\partial E}$. The size-quantization effect occurs only in low-dimensional structures, which should be 2-10 nm [83]. Figure 2.6 shows the energy dependence of the density of states in 3, 2, 1, and 0D structures [84].

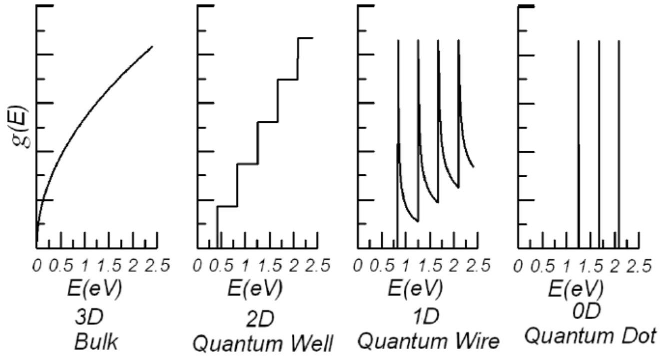


Figure 2. 6 Energy dependence of electron density of states in 3-, 2-, 1- and 0- dimensional crystals [84].

The density of states function results from a dispersion relation E(k) in which electrons have, as quantum numbers, a momentum k along 3, 2, or 1 axes of the crystal in 3, 2, or 1D, and a set of fixed quantum numbers (1, 2, 3. . .) along directions in which the motion is constrained (1 direction in 2D systems, 2 directions in 1D systems, all 3 directions in 0D systems). It is quite obvious that the sharp maxima in g(E) of quantum wires seen in Figure 2.6 will result in a large increase in the Seebeck coefficient via equations. (2.3) or (2.4). While the concept of thermoelectric transport in low-dimensions is quite old [81], and the diameter of SiNWs, which normally is about 200nm, is much larger than the requirement of quantum confinement, this theory cannot be applied on this project.

To enhance S by increasing $\frac{\partial \mu(E)}{\partial E}$, low energy electrons or phonons are scattered by a Schottky barrier. In the process, the electrons or phonons will lose some energy, resulting in an increase in the difference in mobility μ. Therefore, the differential $\frac{\partial \mu(E)}{\partial E}$ is increased. Overall, the power factor $S^2\sigma$ is increased.

2.2.2 Metal-semiconductor contacts

When metal makes contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. This barrier is responsible for controlling the current conduction, as well as its capacitance behavior. There are two types of metal-semiconductor contacts: rectifying Schottky barrier and low-resistance Ohmic barrier. To scatter low energy electrons and phonons, a Schottky barrier should be formed in SiNWs instead of an Ohmic barrier.

Schottky barrier formation

When an n-type semiconductor is brought in contact with a metal, electrons will flow from the semiconductor to the metal if the Fermi level of the semiconductor is higher than that of the metal. Such flow of electrons causes the Fermi levels of the metal and the semiconductor to align. The electrons moving from the semiconductor to the metal leave depleted donors in a region close to the interface that create an electric field in the semiconductor. This field causes band bending in the semiconductor close to the interface, leading to the formation of a Schottky barrier, as shown in Figure 2.7. This type is a rectifying barrier, allowing for electronic transport across the metal semiconductor interface.

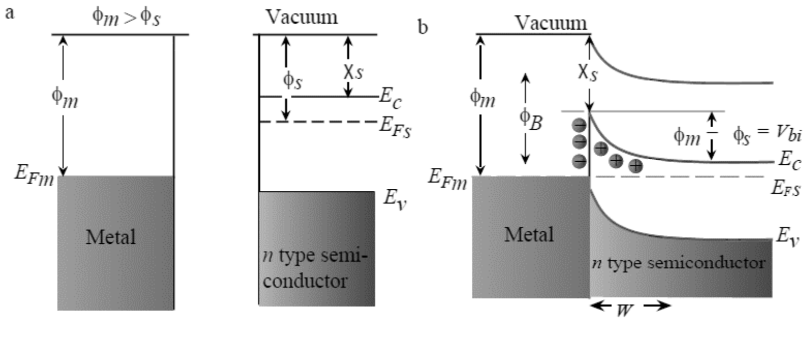


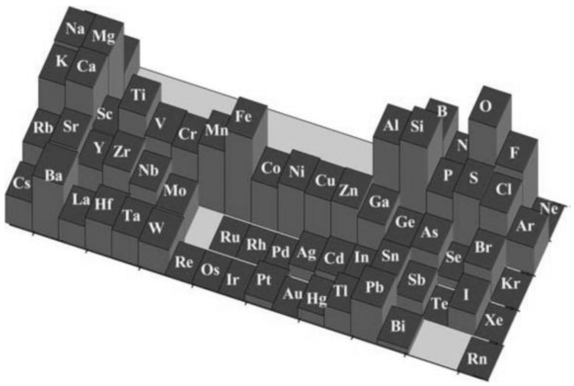
Figure 2. 7 Energy band diagram of formation of a metal-semiconductor (n-type) (M-S) contact. (a) before contact, (b) after the contact; the formation of a Schottky barrier for the case where $\varphi_m > \varphi_S$. The M-S interface shown in (b) is at equilibrium [86].

In Figure 2.7 (a) the conduction band, valence band, and Fermi level of the semiconductor are given by E_C, E_V, and E_{FS}. φ_m is the work function of the metal, which corresponds to the energy difference between the vacuum level and the Fermi level of the metal. χ is the electron affinity of the semiconductor, which is measured from the bottom of the conduction band to the vacuum level.

The obtained Schottky barrier allows electrons to flow from the semiconductor to the metal, but blocks it in the opposite direction, which makes it a rectifying barrier. In this project, the two most important parameters are considered to be the depletion layer width (W) and the Schottky barrier height (φ_B). The Schottky barrier height depends on the work function of the metal (φ_m) and the electron affinity of the semiconductor (χ) as described in the following equation:

$$\varphi_B = (\varphi_m - \chi) \tag{3.1}$$

To form Schottky barriers on n-type semiconductors, the metal work function (ref. Figure 2.9) should be larger than the affinity of Si. For this project, nickel was chosen as the contact metal for the following reasons: 1. Nickel is inexpensive and abundant on the earth; precious metals may have limited acceptance in the industry (ref. Figure 2.8); 2. Schottky barriers can form between nickel and silicon contacts; 3. Nickel is easily removed from silicon surfaces by using commercial etchants; 4. It is relatively easy to deposit and get Ni(0) on silicon surfaces, compared to other active metals. So although nickel is not the only metal that can be used in this project, it is relatively inexpensive, easy to obtain, and easy to work with.



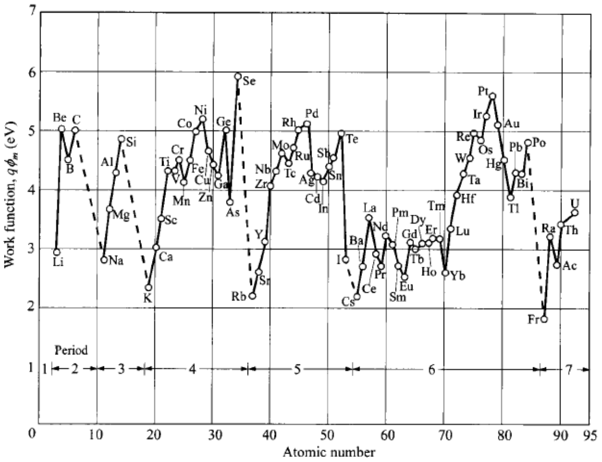


Figure 2. 8 Relative abundance of the principal elements in the earth's crust, presented using a logarithmic scale [85]

Figure 2. 9 Metal work function for a clean metal surface in a vacuum versus atomic number. Note the periodic nature of the increase and decrease of the work functions within each group [86]

2.2.3 Nickel deposition

In order to obtain metal-semiconductor interfaces on SiNWs, nickel needs to first be deposited on silicon. There are various ways to deposit nickel, such as electroless nickel deposition [87], electrodeposition [88], chemical vapor deposition [89], electron beam evaporation [90], and sputtering. Among these techniques, electroless deposition has been attracting attention because of its simplicity of operation and low cost.

Electroless nickel deposition in an aqueous solution

Electroless nickel (EN) deposition is an auto-catalytic reaction used to deposit a coating of nickel on a substrate. Unlike electrodeposition, it is not necessary to pass an electric current through the solution to form a deposit. The deposited nickel particles can be as small as 10nm in diameter [91].

In the semiconductor device industry, attempts have been made to utilize the electroless deposition method for delineating semiconductor junctions [92, 93], making Ohmic contacts [94], and micro-patterning integrated circuits [95].

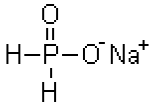
Electroless nickel deposition is undoubtedly the most important catalytic deposition process in use today. The principal reasons for its widespread commercial and industrial use are to be found in the unique properties of EN deposits. The chemical and physical properties of an EN coating depend on its composition, which, in turn, depends on the formulation and operating conditions of the EN bath. Typically, the constituents of an EN solution are: (1) a source of nickel ions; (2) a reducing agent; (3) stable complexing agents; (4) stabilizers/inhibitors; (5) energy [96].

(1) The nickel source

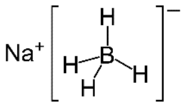
Sources of nickel cations include nickel sulfate, nickel hypophosphorus and nickel chloride. The use of nickel acetate does not yield any significant improvement in bath performance or deposit quality when compared to nickel sulfate. Any minor advantages gained by nickel acetate are offset by its higher cost over that of nickel sulfate and nickel chloride. In this project, nickel chloride was chosen over the poisonous nickel sulfate.

(2) Reducing Agents

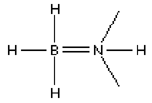
There are four common reducing agents used in the chemical reduction of nickel in an aqueous solutions: sodium hypophosphite, sodium borohydride, dimethlamine borane (DMAB), and hydrazine.



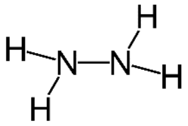
Sodium hypophosphite



Sodium borohydride



Dimethlamine borane (DMAB)



Hydrazine

The four reducing agents are structurally similar in that each contains two or more reactive hydrogens, and nickel reduction is said to result from the catalytic dehydrogenation of the reducing agents. Electroless nickel deposition can be viewed, in a very elementary manner, as the sum of two chemical reactions occurring in an electrochemical cell – a chemical oxidation reaction that liberates electrons and a nickel reduction reaction that consumes electrons:

Oxidation of reducing agent

$$\text{Red.} \rightarrow O_x + ne^-$$

Reduction of nickel ion

$$mNi^{2+} + 2me^- \rightarrow mNi^0$$

Overall reaction

$$mNi^{2+}\,\text{Red.} \rightarrow mNi^0 + O_x$$

In the reduction process, all reducing agents share some similar characteristics: 1. The reduction of nickel is always accompanied by the evolution of hydrogen; 2. The deposit is not pure nickel, but contains either phosphorus, boron, or nitrogen, depending on the reducing agent used; 3. The reduction reaction takes place only on the surface of certain metals, but must also take place on the depositing metal; 4. Hydrogen ions are generated as a by-product of the reduction reaction. 5. The utilization of the reducing agent for depositing metal is considerably less than 100 percent; 6. The molar ratio of nickel deposited to reducing agent consumed is usually equal to or less than 1.

In this project, hydrazine was chosen as the reducing agent.

Hydrazine is a powerful reducing agent in aqueous alkaline solutions. It has four reactive hydrogens:

$$N_2H_4 + 4OH^- \rightarrow N_2 + 4H_2O + 4e^-,\ E_b = 1.16\ V$$

$$2Ni^{2+} + 2e^- \rightarrow 2Ni^0,\ E^0 = -0.25\ V$$

Levy [97] proposed the following reduction reaction for nickel ions with hydrazine in an alkaline solution:

$$2Ni^{2+} + N_2H_4 + 4OH^- \rightarrow 2Ni^0 + N_2 + 4H_2O,\ E^0 = 0.91\ V$$

This reaction implies a reducing efficiency of 100 percent for hydrazine, since the hydrazine is involved in the reduction of nickel ions only. The above equation does not account for the hydrogen evolved during the nickel deposition reaction with hydrazine. The hydrolyzed nickel ion mechanism can be modified to represent the experimental observations made during nickel reduction with hydrazine:

$$Ni^{2+} + 2OH^- \rightarrow Ni(OH)_2^{2+}$$

$$Ni(OH)_2^{2+} + N_2H_4 \rightarrow Ni(OH)_{ad}^{1+} + N_2H_3OH + H^+$$

$$Ni(OH)_{ad}^{1+} + N_2H_3OH \rightarrow Ni + N_2H_2(OH)_2 + H^+$$

$$2H^+ \rightarrow H_2$$

Then the overall reaction can be written as:

$$Ni^{2+} + N_2H_4 + 2OH^- \rightarrow Ni^0 + N_2 + 4H_2O + H_2$$

The above mechanism does not account for the formation of hydrogen ions (H^+) during the course of the deposition reaction. In the reaction sequence given above, the hydroxyl ions (OH^-) in the first step are present in the solution through the addition of alkali metal or ammonium hydroxides. However, if the hydroxyl ions coordinated to nickel are generated by the dissolution of water molecules, a slightly different reaction mechanism results:

$$2H_2O = 2H^+ + 2OH^-$$

$$Ni^{2+} + 2OH^- = Ni(OH)_2$$

$$Ni(OH)_2 + N_2H_4 = Ni^0 + N_2H_2(OH)_2 + 2H^+$$

$$N_2H_2(OH)_2 + 2H^+ = N_2 + 2H_2O + H_2$$

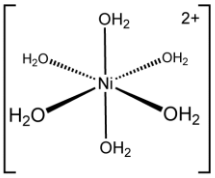
Then the overall reaction is given by:

$$Ni_2 + N_2H_4 \rightarrow Ni^0 + N_2 + 2H^+$$

(3) Complexing Agents

Additives referred to as complexing agents in electroless nickel deposition solutions are, with two exceptions, organic acids or their salts. The two exceptions are the inorganic pyrophosphate anion, which is used exclusively in alkaline EN solutions, and the ammonium ion, which is usually added to the deposition bath for pH control or maintenance. There are three principal functions that complexing agents perform in the EN deposition bath: (1) exerting a buffering action that prevents the pH of the solution from decreasing too fast; (2) preventing the precipitation of nickel salts, e.g., acidic salts or phosphites; (3) reducing the concentration of free nickel ions. In addition to these functions, complexing agents also affect the deposition reaction and, hence, the resultant nickel deposit.

Nickel ions in aqueous solutions interact with and are bound to a specific number of water molecules. Each water molecule is oriented so that the negative end of the dipole, oxygen, is directed toward the positive nickel ion. The number of water molecules that can attach to the nickel ion is called the coordination number. Divalent nickel has two coordination numbers, 4 and 6. Aqueous solutions of simple inorganic nickel salts, e.g., $NiSO_4 \cdot 6H_2O$, contain the green, octahedral hexaquonickel ion $[Ni(H_2O)_6]^{2+}$. A schematic representation of a 6-coordinate nickel ion in an aqueous solution is shown below:



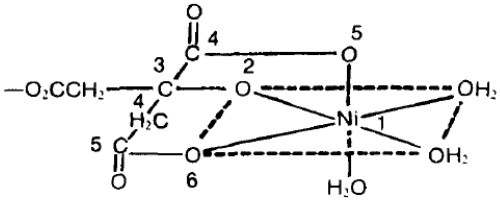
When water molecules coordinated to the nickel ion are replaced by other ions or molecules, the resulting compound is called a nickel complex and the combining, or donor, group is called a complexing agent or ligand. The chemical properties of nickel ions in an aqueous solution are altered when they are combined with complexing agents. Some common properties of solvated nickel ions that can be affected by complexing agents are color, reduction potential, and solubility.

Complexing agents can also separate nickel from an aqueous solution and lower the reduction potential for nickel, as shown in the following example [96]:

$$[Ni(H_2O)_6]^{2+} + 2e^- = Ni^0 + 6H_2O,\ E = -0.25V$$

$$[Ni(CN)_4]^{2+} + 2e^- = Ni^0 + 4CN^-,\ E = -0.90V$$

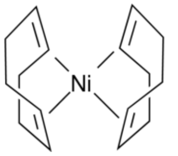
In this project, sodium citrate was chosen as the complexing agent because of its wide usage. The citrate ion, although tetradentate, can coordinate to the nickel ion with the formation of two chelate rings, a 5-membered ring and a 6-membered ring. If the complexing agent does not have a sufficient number of donor atoms to satisfy the coordination number (sites) of the nickel ion, the remaining sites may be occupied by other ligands and/or water molecules.



(4) Stabilizers
An electroless nickel deposition solution can be used under normal operating conditions over extended periods without adding stabilizers; however, it can decompose spontaneously at any time. Bath decomposition is usually preceded by an increase in the volume of hydrogen gas evolved and the appearance of a finely-divided black precipitate throughout the bulk of the solution. In this project, only a small amount of reaction solution was used each time and disposed of after deposition, so stabilizers were unnecessary.

Electroless nickel deposition in organic solvent

In this project, Bis(1,5-cyclooctadiene)nickel(0) (Ni(COD)$_2$) was used for the nickel source in the electroless nickel deposition in an organic solvent.



Nickel(0) bonds to alkene groups in two 1,5-cyclooctadiene ligands and is moderately soluble in benzene and THF [98]. In this project, toluene was chosen as the organic solvent to dissolve Ni(COD)$_2$ due to its higher boiling point, 111 °C, compared to that of benzene and THF which are 80°C and 66°C, respectively. The COD ligands easily break down at a low temperature because the melting point of Ni(COD)$_2$ is 60 °C. By breaking down the COD ligands, nickel can be deposited on the surface of SiNWs and form very fine nano particles. Deposition in an organic solvent is intended to prevent oxidation. The entire deposition process can be carried out in a glove box with an HPLC grade organic solvent.

There are other nickel(0) sources available, but considering decomposing temperature, molecular weight/efficiency, and solubility, Ni(COD)$_2$ appeared to be the best choice.

Electron beam nickel deposition

Electron beam physical vapor deposition (EBPVD) is a form of physical vapor deposition in which a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum. The electron beam causes nickel atoms from the target to transform into the gaseous phase. These nickel atoms then precipitate onto the SiNWs, coating the tip of the nanowires in the vacuum chamber. The vacuum chamber also prevents the oxidation of silicon and nickel.

Electrodeposition of nickel particles

In electrodeposition, nickel particles are deposited using the scanning electrodeposition/striping method pioneered by Sailor et al [99]. The SiNW array is immersed into a commercial nickel deposition solution (clean earth solution). The electrodeposition is potentiostatic at a suitable voltage versus saturated calomel electrode (SCE), using a potentiostat in conjunction with a one-compartment, three-electrode electrochemical cell with a Pt foil as a counter electrode, as shown Figure 2.10 [100].

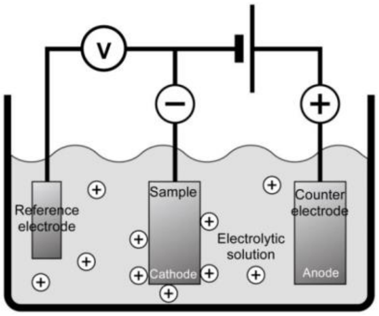


Figure 2. 10 Schematic of an electrolytic cell used in the electrodeposition of silicon nanowires [100]

2.2.4 Formation of nickel silicide

According to Lavoie et al., after a nickel film is deposited onto a silicon substrate and annealed, different phases will form depending on the temperature, as shown in Figure 2.11 [101].

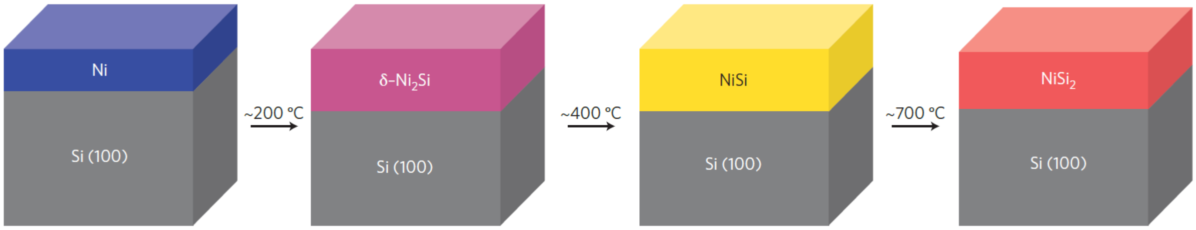


Figure 2. 11 Formation of the different phases of nickel silicide. Nickel silicide typically observed for a thin Ni film deposited on a (100) oriented Si wafer. As the annealing temperature is increased for a thin film on (100) Si, δ-Ni_2Si forms first, owing to its large interdiffusion coefficient; NiSi forms at a higher temperature when all of the δ-Ni_2Si is consumed, and remains stable up to ~700°C when the final phase, $NiSi_2$ begins to nucleate [101].

Nickel is the dominant diffusing species. If the temperature of formation is low enough that Si is not significantly mobile, the possibility of bridging is practically eliminated. With a low diffusivity for Si atoms, the formation of most silicide will be inside the silicon. Also, nickel diffusion is such that vacancies generated by the diffusion itself are mainly located in the metal layer instead of in the silicon layer when silicon is diffusing, which avoids creating many voids inside the material. In the case of metal diffusion, the vacancies are generated in the metal layer. The morphology of this layer after reaction is of little interest since it is removed by selective etching, as shown in Figure 2.12 [101].

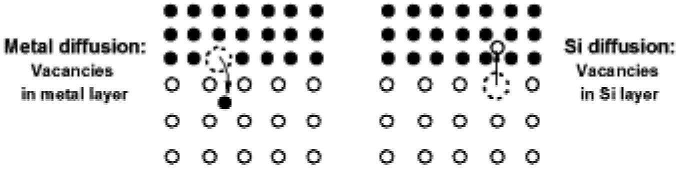


Figure 2. 12 Simple schematic of vacancy generation depending on diffusing species. Vacancies are located in the silicon layer if silicon diffuses and in the metal layer if the metal diffuses [101].

In the opposite case of a silicon film deposited on a thick nickel substrate, a similar sequential growth of silicides has been found to start with Ni_2Si, but followed by Ni_5Si_2 and Ni_3Si [102]. Combining these two subsequences, it is seen that the first phase is always Ni_2Si, but the subsequent ones, depending on the supply, are different; if the nickel supply is limited, the composition of the phases will increase in silicon, and vice versa, which is related to a Ni-Si phase diagram, as shown in Figure 2.13 [102].

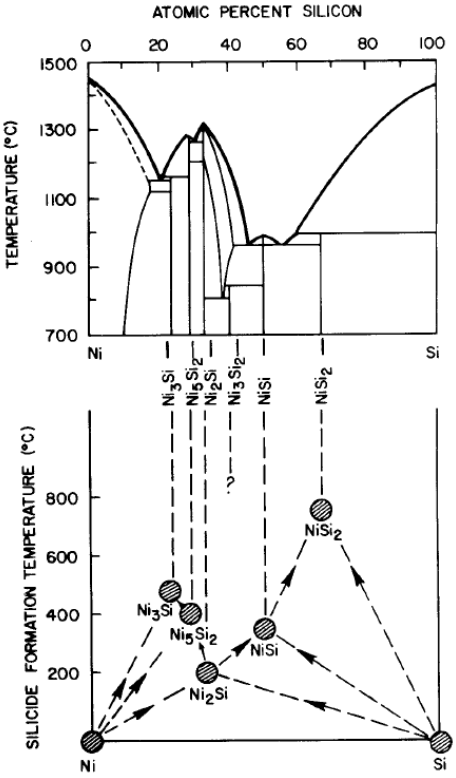


Figure 2. 13 Formation map of thin film nickel silidides which shows the sequence of phases against their formation temperature. The phase diagram of Ni-Si, as shown on top of the figure, is for comparison [102].

Studies have shown that the reactions of nickel with SiNWs may proceed differently than those with thin-film and bulk silicon. They mainly show that nanowire crystallographic orientation and the ability of the nanowires to better accommodate strain can lead to stabilization of silicide phases not normally observed in bulk or thin-film reactions under a similar heat treatment [78, 103-105]. In the above studies, all the nickel silicide phases can be obtained at temperatures between 250°C and 550°C. Tao et al. claim that Ni/SiNW composites can form at different temperatures ranging from 250°C to 550°C by using rapid thermal annealing (RTA) in an Ar atmosphere. Their nanowires are constructed by wet chemical etching, and then coated by electroless nickel deposition using the nickel bath $NiSO_4{\cdot}6H_2O$ as the nickel ion source, NH_4F as the reducing agent, $(NH_4)_2SO_4$ as the buffering agent, and sodium citrate as the complexing agent. All the steps conducted by them are similar to those on this project [106].

Effects of interfacial SiO_2 on nickel silicide formation

Scott and Lau reported on the effect of an interfacial SiO_2 layer between Ni, Pt, and Pd thin films and Si wafers on the solid-state reaction and formation of silicide. They found that the minimum temperature necessary for Pd_2Si formation is approximately 400°C for about 2.4nm of SiO_2 compared with 600°C for Pt_2Si and 650°C for Ni_2Si formation, as shown in Figure 2.14. It shows that even if there is only a very thin oxidation layer, it might be difficult for nickel silicide to form below 600°C. The metal deposited in their experiment was obtained by electron beam physical vapor deposition. The thickness of SiO_2 was 104nm with nickel 127nm with palladium, and 108nm with platinum [107].

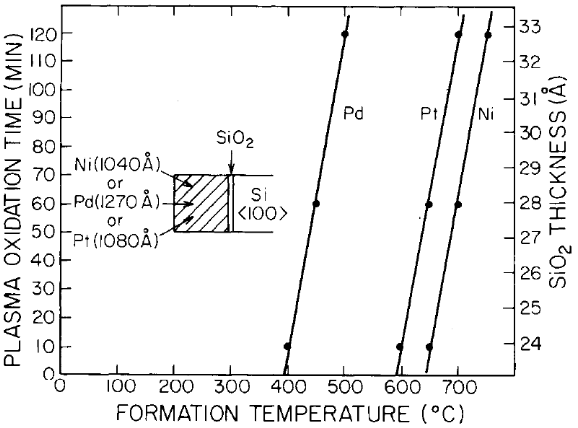


Figure 2. 14 Plot of plasma oxidation time vs. Ni_2Si, Pd_2Si and Pt_2Si formation temperature. The right hand scale shows the SiO_2 thickness corresponding to the oxidation time. All samples were annealed for 30 min [107].

It is known that SiO_2 does not react with nickel, palladium, or platinum up to 800°C [108]. Because of the very high stability of SiO_2, it is also very unlikely that an appreciable part of the SiO_2 layer will go into a solid solution with any of these metals at these temperatures. Thus, initial silicide formation does not depend on removing the SiO_2 barrier, but rather on the mobility of the reacting species in the SiO_2 layer itself.

It is known from radioactive tracer experiments that silicon is not mobile in SiO_2 at these high temperatures [109]. Thus, it is the relative mobilities of nickel in SiO_2 that most probably determine the initial silicide formation rates and, hence, the sensitivities of the respective silicide formations to the presence of an interfacial SiO_2 layer. Scott et al. [107] suggest that since Pd_2Si formation is insensitive to a thin interfacial SiO_2 layer, compared with Ni_2Si or Pt_2Si formation, palladium is mobile in SiO_2 at much lower temperatures than is either nickel or platinum. This conclusion is consistent with the results of experiments on high temperature electrolysis of vitreous silica [110]. These experiments have shown that palladium is indeed highly mobile in silica, and that substantial amounts of palladium can be introduced into the silica whereas platinum cannot be introduced into the silica at all.

According to Scott et al., the immunity of nickel silicide formation to silicon substrates through thin SiO_2 layers can be seen in Figure 2.15. Initially, SiO_2 is present as a layer between the nickel and the silicon. Upon annealing at a sufficiently high temperature, the nickel begins to diffuse through the SiO_2 layer to form silicide. This occurs at an initial rate which depends on the mobility of nickel in SiO_2. As nickel silicide continues to form, lateral non-uniformities in the silicide thickness act to break up the continuous interfacial coverage of the SiO_2, layer and the barrier fails. Therefore, the highly resistive SiO_2 would not get into the silicon substrate in the whole annealing process, which prevents the decreasing of electron mobility by hitting the SiO_2 spots. The decreasing of electron mobility can lead to the decrease of zT.

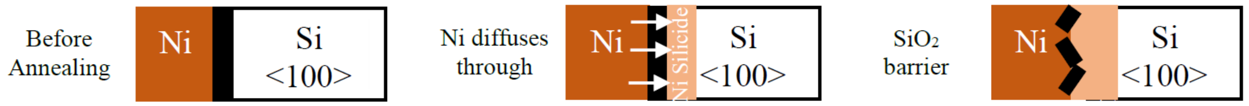


Figure 2. 15 Model of nickel silicide growth

2.3 Experiment process

The whole experiment process of this project can be divided into four parts: nanowire array synthesis, electroless nickel particles deposition, Schottky barrier formation (annealing), and etching extra nickel, as shown in Figure 2.16.

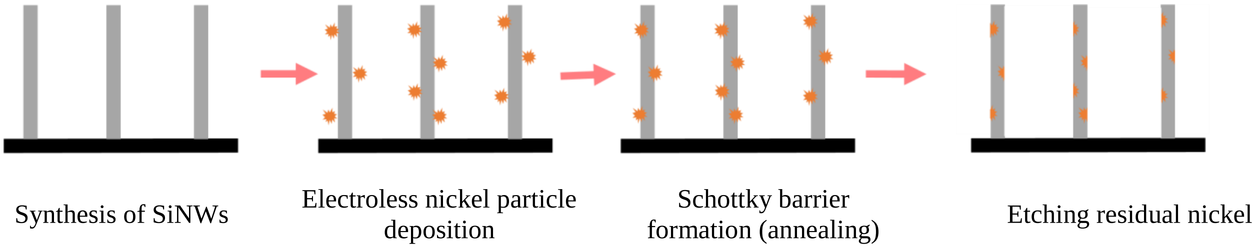


Figure 2. 16 Schematic illustration of the synthesis process of heterostructure SiNWs

2.3.1 Silicon nanowire array synthesis

The standard nanowire synthesis was conducted on boron doped p-type (100) silicon wafers with 10-20 Ω/cm resistance. The wafers were cut to 2 cm × 2 cm pieces to fit the quartz tube in the tube furnace. The cut wafers were sonicated for 5 minutes in acetone, followed by 5 minutes in methanol, and finally 5 minutes in Millipore water. The wafers were then dried with compressed air. The backside of the wafers was coated with nail polish and left to dry for 5-10 minutes. The backside of each wafers was coated with nail polish and adhered to the bottom of polyethylene beakers. In a separate polyethylene beaker, $AgNO_3$ (0.34g, 0.02 mol) was mixed with 80 mL of Millipore water, followed by the addition of 20 mL of 5M HF. The $AgNO_3$/HF solution was then transferred to the beakers containing the wafers. The reaction mixture was left to rest for 2 hours until 30 μm long nanowires developed. The $AgNO_3$/HF solution was decanted along with the silver dendrite cloud. The wafers were rinsed with Millipore water and IPA, then dried gently with compressed air. The wafers were then soaked with concentrated nitric acid for 30 minutes, nitric acid was then decanted. The wafers were rinsed with Millipore water and IPA, then dried with compressed air.

2.3.2 Electroless nickel deposition in an aqueous solution

A $4H_2O$:1HF solution was prepared in a polyethylene beaker. The SiNW array samples were placed in the HF solution for 5 minutes and then the HF solution was decanted. The SiNW array samples were rinsed with Millipore water and IPA, then dried with compressed air. Immediately, a scintillation vial was charged with nickel chloride hexahydrate (0.048g) and sodium titrate dehydrate (0.046g) and dissolved in 10 mL of 95°C Millipore water. Hydrazine (200 μL) was pipetted into the vial. The reaction mixture was then vortexed. The reaction mixture was then heated at 95°C for 5 minutes. The SiNW array samples were then transferred to the vial and heated at 95°C for 10 minutes. Then the solution was decanted. The SiNW array samples were rinsed with Millipore water and IPA, then dried with compressed air.

2.3.3 Electroless nickel deposition in organic solution

A $4H_2O$:1HF solution was prepared in a polyethylene beaker. The SiNW array samples were placed in the HF solution for 5 minutes, followed by a rinse with Millipore water and IPA, then dried with compressed air to remove the oxidized layer. The SiNW array samples were then placed into a nitrogen atmosphere. A 10 mL scintillation vial was charged with 0.025g $Ni(COD)_2$ and dissolved by agitation in 5 mL of dry toluene. The SiNW array samples were transferred to the organic solution. The vial was capped and the reaction mixture was heated at 90°C for two hours until the SiNW array samples were covered by nickel particles. The SiNW array samples were rinsed with dry toluene and stored in a nitrogen atmosphere to dry for at least three hours.

2.3.4 Schottky barrier formation (annealing)

The SiNW array samples were placed on a quartz slide which was then placed into the quartz tube of a tube furnace, as shown in Figure 2.17. Nitrogen gas was injected into the quartz tube for 10 minutes to purge oxygen from the tube. The SiNW array samples were annealed at 650°C for one hour. After annealing, the tube furnace temperature was lowered to 25°C. The SiNW array samples remained under the nitrogen purge until the tube furnace cooled to room temperature.

Note: The heating and cooling rates were not important for this process

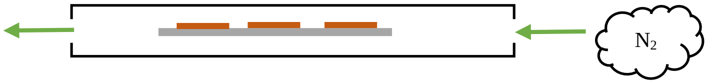


Figure 2. 17 Schematic illustration of annealing SiNW array samples in tube furnace

2.3.5 Etching away residual nickel

Nickel etchant was heated to 70°C and annealed SiNW array samples were placed into the solution. The mixture was heated for 1.5 hours. The nickel etchant solution was then decanted. The annealed and etched SiNW array samples were rinsed with Millipore water and IPA, then dried with compressed air.

2.3.6 Material characterization

The morphology of the SiNWs was checked by using an FEI Magellan 400 XHR SEM. The samples were cut with a diamond cutter to obtain a fresh cross-section, then mounted with conductive carbon glue on a 45º / 90º SEM mount. A through-the-lens detector (TLD), concentric backscatter electron (CBS) detector, and energy dispersive spectroscopy (EDS) system ($80mm^2$ detector with AZtec software) were used for morphology, phase, and element concentration identification.

Phase identification of silicide was performed by using a Rigaku SmartLab X-ray Diffractometer (XRD) with Cu Kα radiation. Both high resolution parallel beam and Bragg-Brentano para-focusing beam techniques were used in this project.

Mangelink et al. showed the XRD result of annealing (100) silicon with pure nickel films on top of the silicon substrate [111]. The NiSi phases appeared at angles of 31°, 36° and 56.5° when annealed at 700°C. When the annealing temperature was raised, the $NiSi_2$ phase appeared at about 33° and 43° (ref. Figure 2.18a). For sample annealing, rapid thermal annealing (RTA) was performed under a N_2 atmosphere.

Lee et al. showed the XRD result of annealing deposited nickel films on Si (100) after rapid thermal annealing at 300°, 500°, 700°, 750 and 900°C. The Ni_2Si and $NiSi_2$ phases appeared at angles of 45° and 48° after a 300°C annealing process. The NiSi phases appeared at angles of 36°, 46°, 47° and 56° when samples were annealed at 700°C (ref. Figure 2.18b) [112].

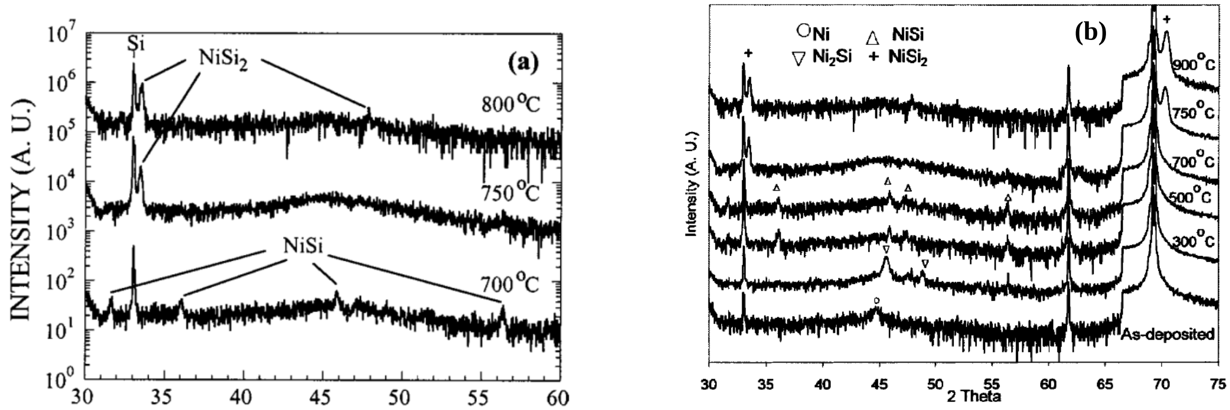


Figure 2. 18 XRD (Cu Kα) pattern of nickel silicide after annealing [111] [112]

3. Results and discussion

3.1 Fabrication of silicon nanowires

Figure 3.1 shows scanning electron microscopy (SEM) images of the silicon nanowire arrays which were created from a silicon substrate that was etched in a 100 mL etching solution. The low-magnification SEM images clearly show homogenously distributed nanowire arrays covering large areas.

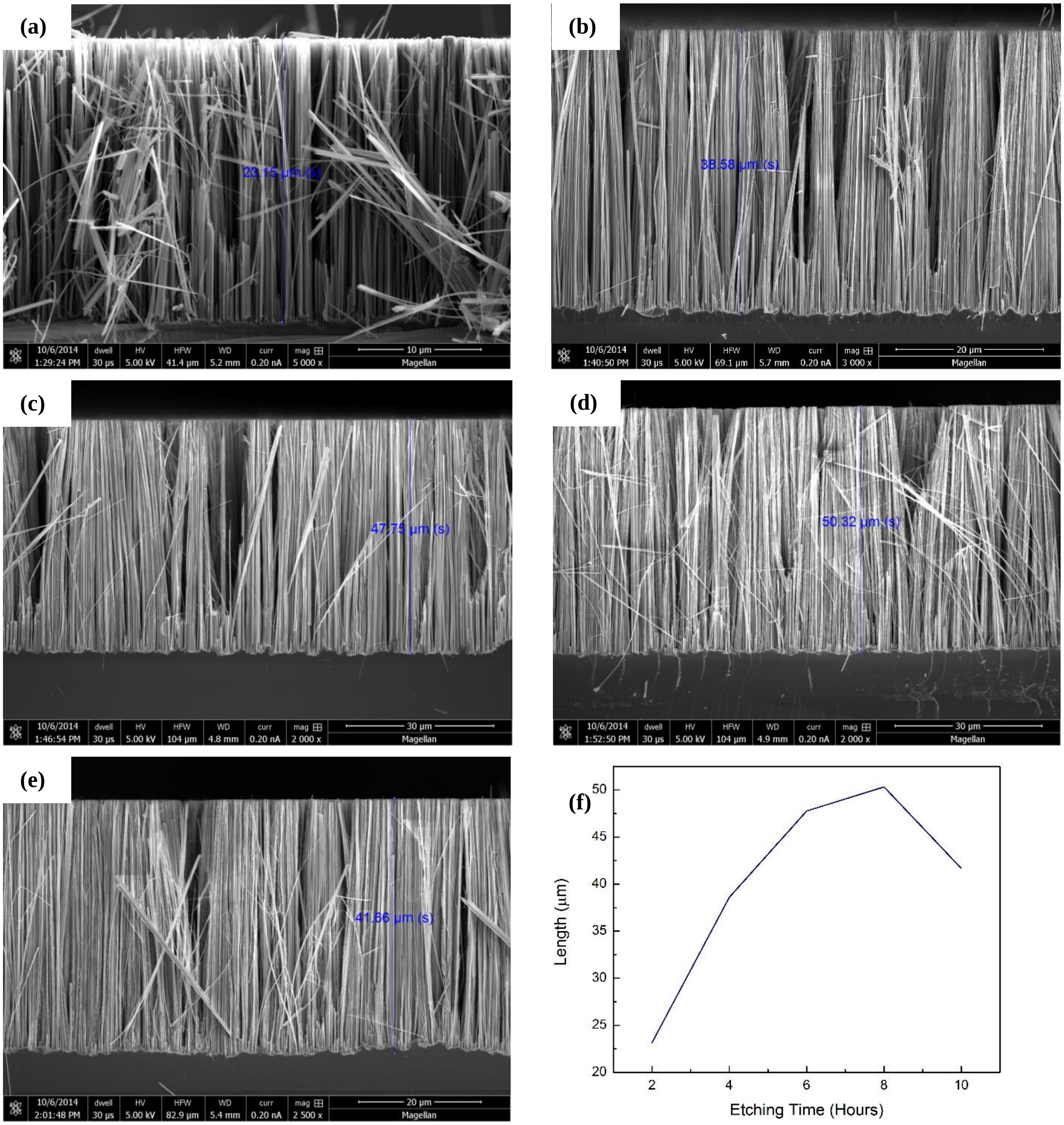


Figure 3. 1 (a) – (e) cross-section SEM images of SiNWs with different lengths under different etching times (2hrs, 4hrs, 6hrs, and 8hrs) in 100 mL 0.02M $AgNO_3$ + 0.5M HF; (f) length of various SiNWs with different etching time (100 mL solution).

Figure 3.1 (f) shows that silicon cannot be etched into nanowires of unlimited length. When silicon wafers are placed in the in 100 mL etching solution, the nanowires start to grow at a slower rate after six hours and actually become shorter after eight hours. This can be explained by the fact that etching of the tip of silicon nanowires and metal-assisted trench etching occur at the same time. The nanowires grow longer because the metal-assisted trench etching rate is faster than the tip etching rate, which depends mainly on the etching rate of HF on silicon. However, when the concentration of etching solutions is changed, the metal-assisted trench etching rate will slow down, making the nanowires grow at slower rate. The nanowires become shorter when the metal-assisted trench etching rate becomes slower than the tip etching rate.

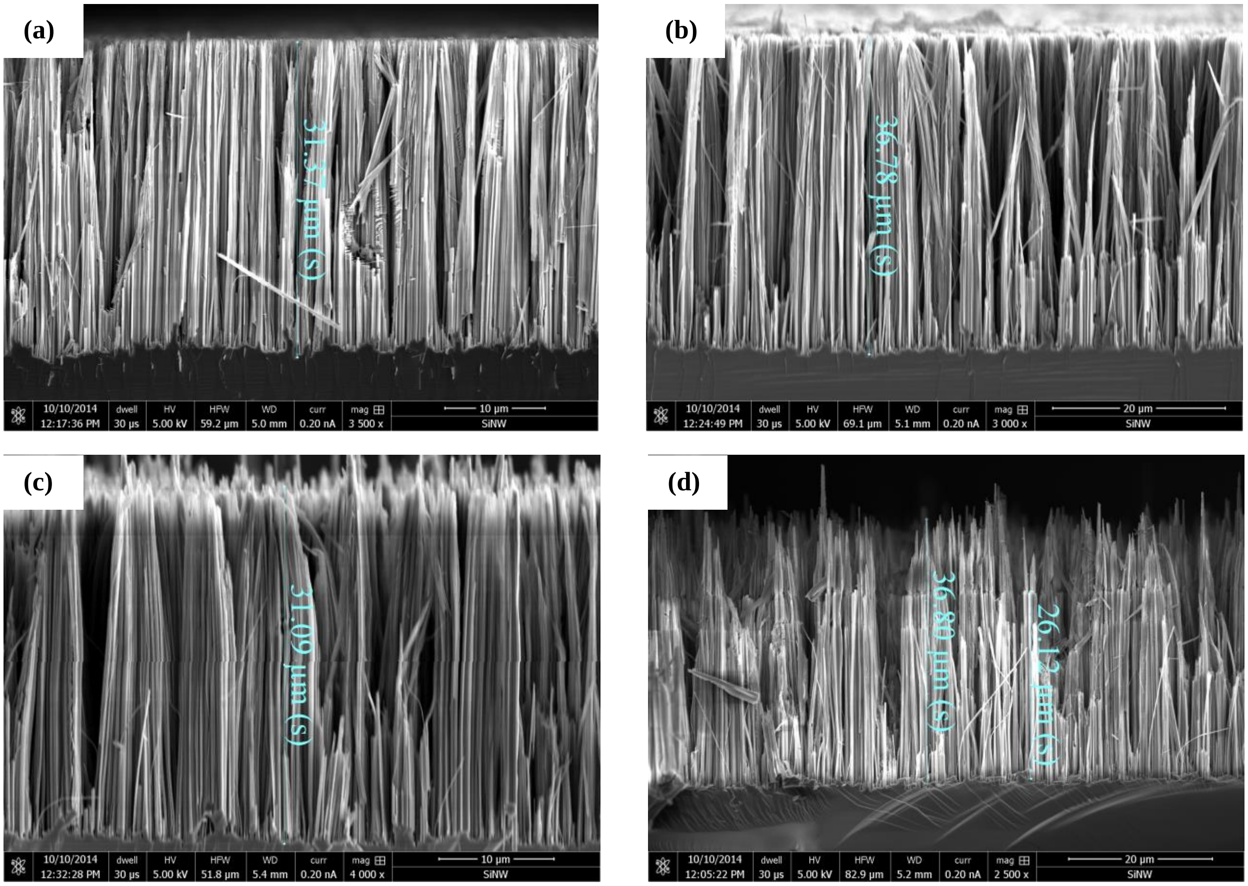


Figure 3. 2 (a) – (d) cross-Section SEM images after two hours of etching silicon substrate with different lengths under different etching solution concentrations: 0.03M $AgNO_3$, 0.04M $AgNO_3$, 0.05M $AgNO_3$, and 0.06M $AgNO_3$ (100 mL solution).

Longer nanowires are more desirable, because the goal is to produce as many nanowires as possible from a single silicon wafer. Initially the plan was to use spark plasma sintering to synthesize theremoelectric bulk materials, and measure its thermoelectric properties. This method was described by Zhang et al [113]. To achieve this goal, the concentration of $AgNO_3$ in the etching solution was changed to increase the trench etching rate, in hopes that longer wires could be etched before the metal-assisted trench etching rate slowed more than the tip etching rate. Figure 3.2 shows the morphology of SiNWs etched under different solution concentrations. The concentration of $AgNO_3$ was adjusted to 0.03M, 0.04M, 0.05M and 0.06M to determine if increasing the concentration of metal might increase the etching rate, resulting in longer nanowires.

However, according to Figure 3.2, increasing the concentration of $AgNO_3$ did not help to dramatically increase the length of nanowires when etched for two hours. The length of the nanowires could be increased by only about 10µm. Regardless of the length of the SiNWs, their morphology made them unusable after increasing the $AgNO_3$ concentration. The tips of the nanowires became sharper after increasing the $AgNO_3$ concentration, indicating that the wires were being over-etched. Nanowires with sharp tips tend to clump together, and they are hard to separate when trying to fabricate them into devices after sonication. Therefore, changing the concentration of $AgNO_3$ does not appear to be a promising way to increase the length of nanowires.

Increasing the amount of etching solution was also tried. Silicon substrates were etched in a 0.02M $AgNO_3$ + 0.5M HF 400 mL solution, instead of .02M $AgNO_3$ + 0.5M HF 100 mL solution. When the etching time went longer than 8 hours (10, 12 hours, 14, and 16 hours) the SiNWs kept growing much longer (Figure 3.3).

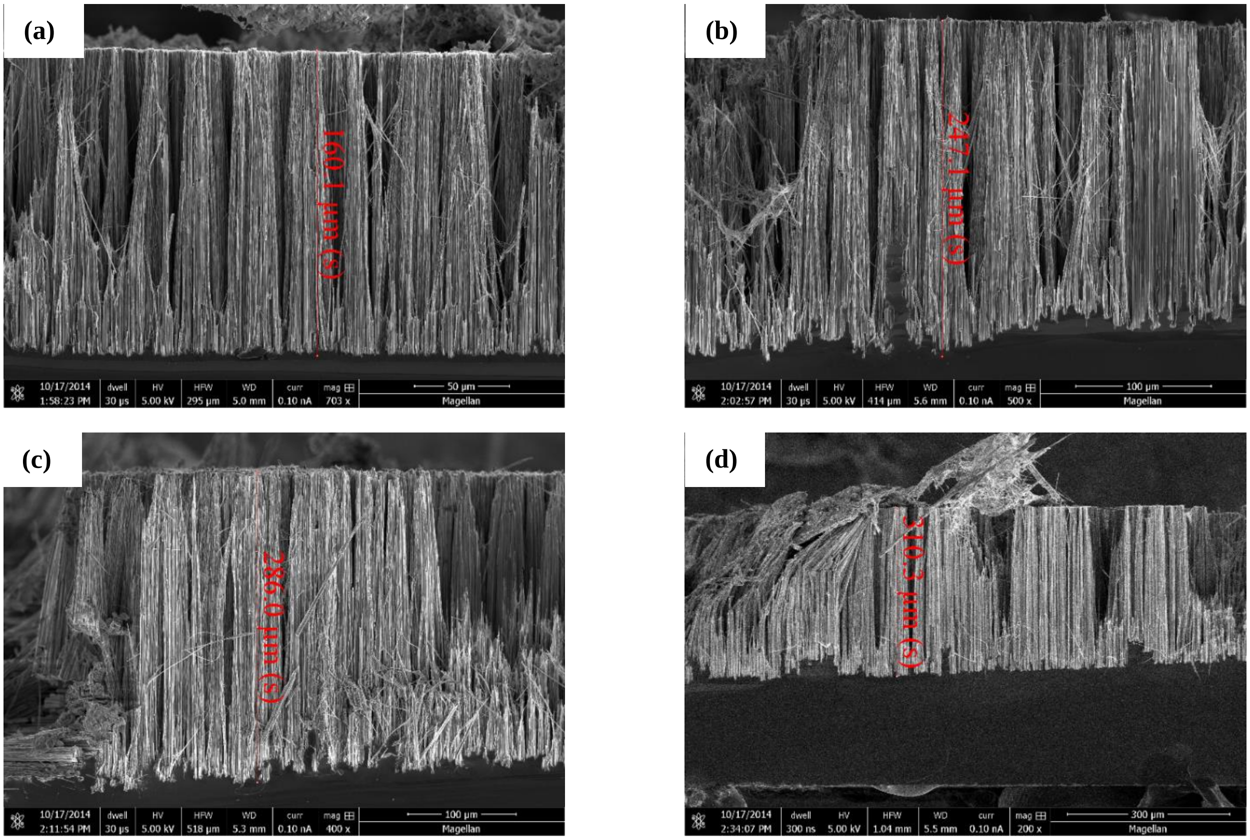


Figure 3. 3 (a) – (d) Cross-Section SEM images of SiNWs with longer length under varied etching time longer than 8 hours: 10hrs, 12hrs, 14hrs, 16hrs, in 400 mL 0.02M $AgNO_3$ + 0.5M HF (400 mL solution)

From Figure 3.3, we can see that the length of the nanowires increased by increasing the amount of etching solution while not changing its concentration. The length of the nanowires could grow to more than 300 µm after 16 hours of etching. Therefore, in this project the length of nanowires was controlled by the amount of etching solution.

From the SiNW fabrication mechanism illustrated in Section 2.1.1, it is known that dendrite silver will form on top of the silicon substrate, as shown in Figure 3.4. Since the formation of dendrite silver was thought to affect the etching of the silicon substrate, the dendrite silver was carefully removed by tilting the beaker after 10 hours of etching in 400 mL 0.02M $AgNO_3$ + 0.5M HF. The silicon substrate was still kept in the etching solution for another 6 hours.

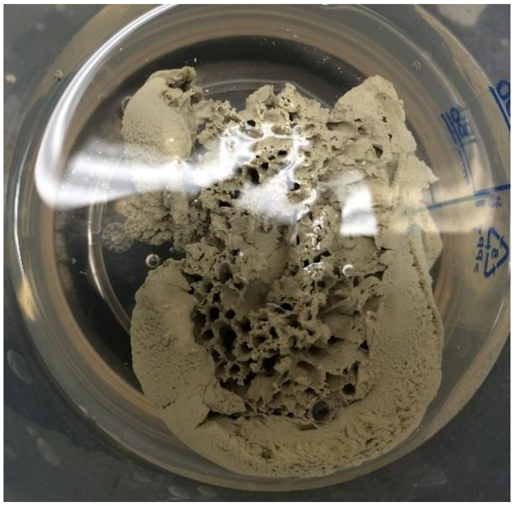


Figure 3. 4 Large chunk of dendrite silver cloud. The holes on the silver cloud were caused by H_2 produced during etching process

The morphology of the nanowires after 16 hours of etching, with the removal of the dendrite silver, is shown in Figure 3.5, which illustrates that the tips of SiNWs have irregular shapes due to the removal of dendrite silver. After removing the dendrite silver, the etching was no longer only extending vertically, but nanowires started to etch horizontally, which left many small dents on the tips of the wires. Clearly, the dendrite silver should not have been removed during the etching process.

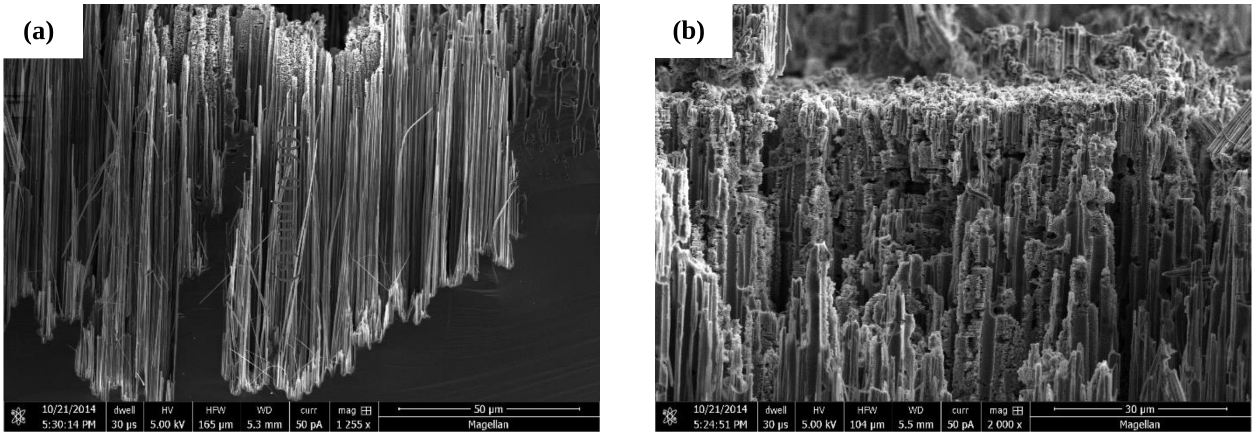


Figure 3. 5 Morphology of SiNWs after removing dendrite silver during etching process. The etching solution was 400 mL 0.02M $AgNO_3$ + 0.5M HF.

Regardless of the limited lengths of SiNWs that were controlled for purposes of this study, obtaining 1g of SiNWs will take about 10L HF to make the etching solution, because 400 mL HF can produce, at most, 0.71g SiNWs, even when all possible wires are removed from the substrate, as shown in Figure 3.6. Therefore, fabricating SiNW thermoelectric devices by spark plasma sintering is not considered very promising. Other ways to make SiNWs into devices for measuring thermoelectric properties are still under study in our lab.

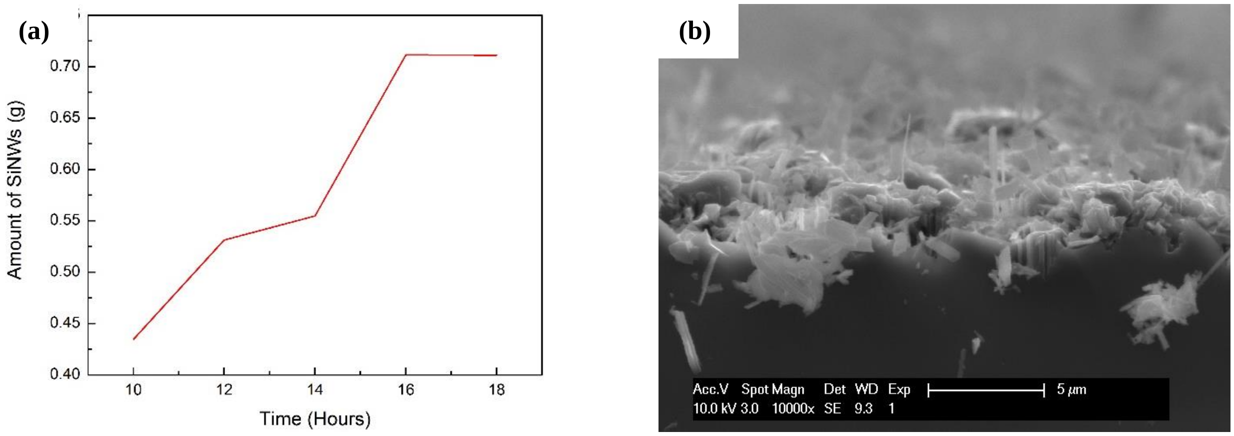


Figure 3. 6 (a) weight of SiNWs produced after different etching times; (b) substrate after removing SiNWs, showing that almost all nanowires were removed.

3.2 Approach of making metal-semiconductor heterostructures in SiNWs

3.2.1 Electroless nickel deposition in aqueous solution

The bath compositions for electroless nickel deposition were obtained from Schelesinger's "Electroless Deposition of Nickel" [114]. In order to determine conditions for optimal deposition, different bath composition concentrations and conditions were chosen as shown in Form 3.1.

Table 3.1 Different bath compositions and conditions for electroless nickel deposition in aqueous solution

Variable	Sample	Nickel chloride hexahydrate (g)	Sodium citrate dehydrate (g)	Hydrazine (μL)	Millipore water (mL)	pH
Hydrazine	1	0.048	0.046	150	10	10
	2	0.048	0.046	200	10	10
	3	0.048	0.046	250	10	10
	4	0.048	0.046	300	10	10
	5	0.048	0.046	500	10	10
	6	0.048	0.046	600	10	10
Nickel Chloride Hexahydrate	7	0.023	0.046	200	10	10
	8	0.036	0.046	200	10	10
	9	0.069	0.046	200	10	10
Sodium Citrate Dehydrate	10	0.048	0.024	200	10	10
	11	0.048	0.036	200	10	10
	12	0.048	0.06	200	10	10
pH	13	0.048	0.046	200	10	6
	14	0.048	0.046	200	10	8
	15	0.048	0.046	200	10	12

Figure 3.7 – 3.8 show how the nickel particles were deposited on the SiNWs.

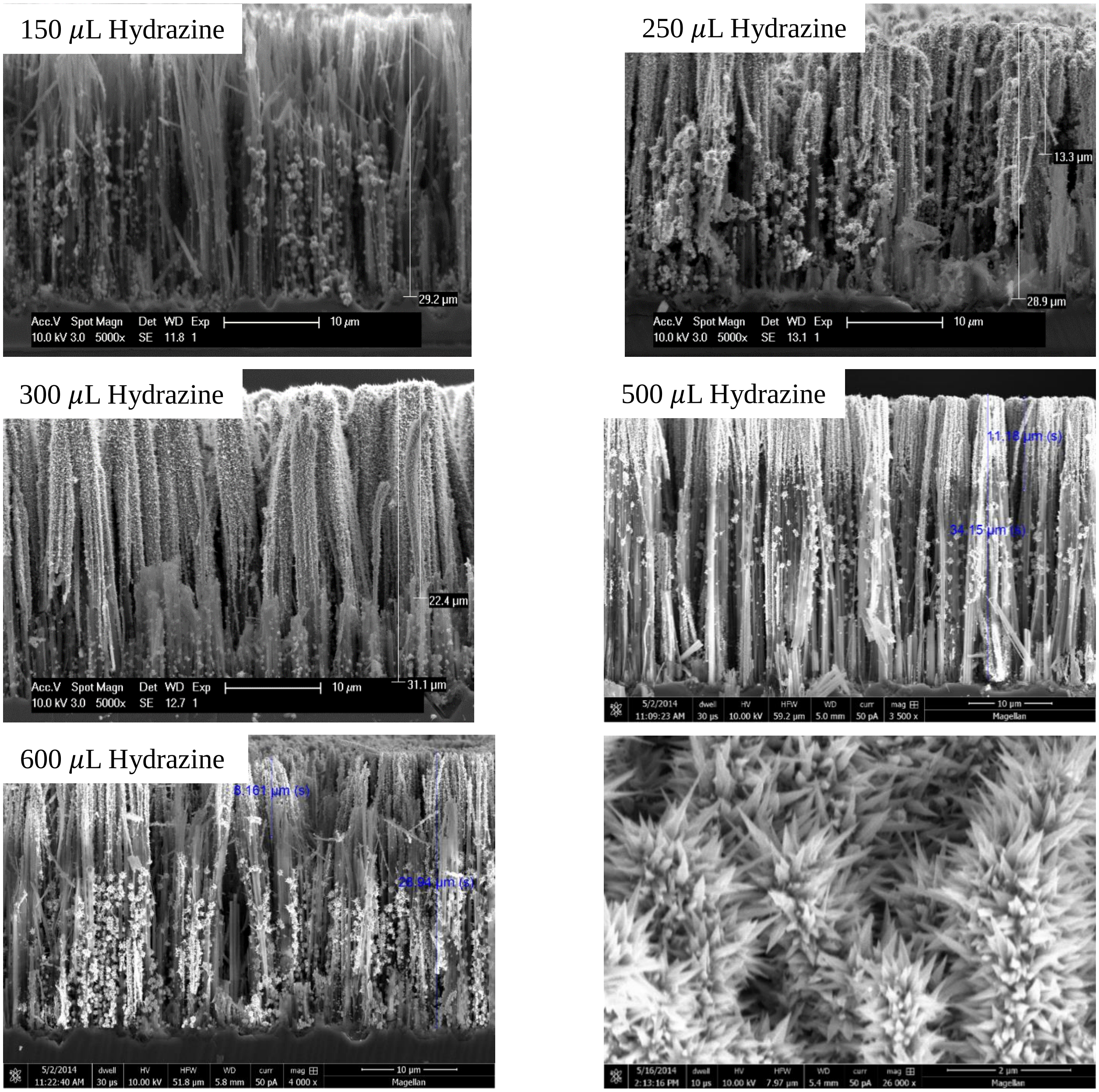
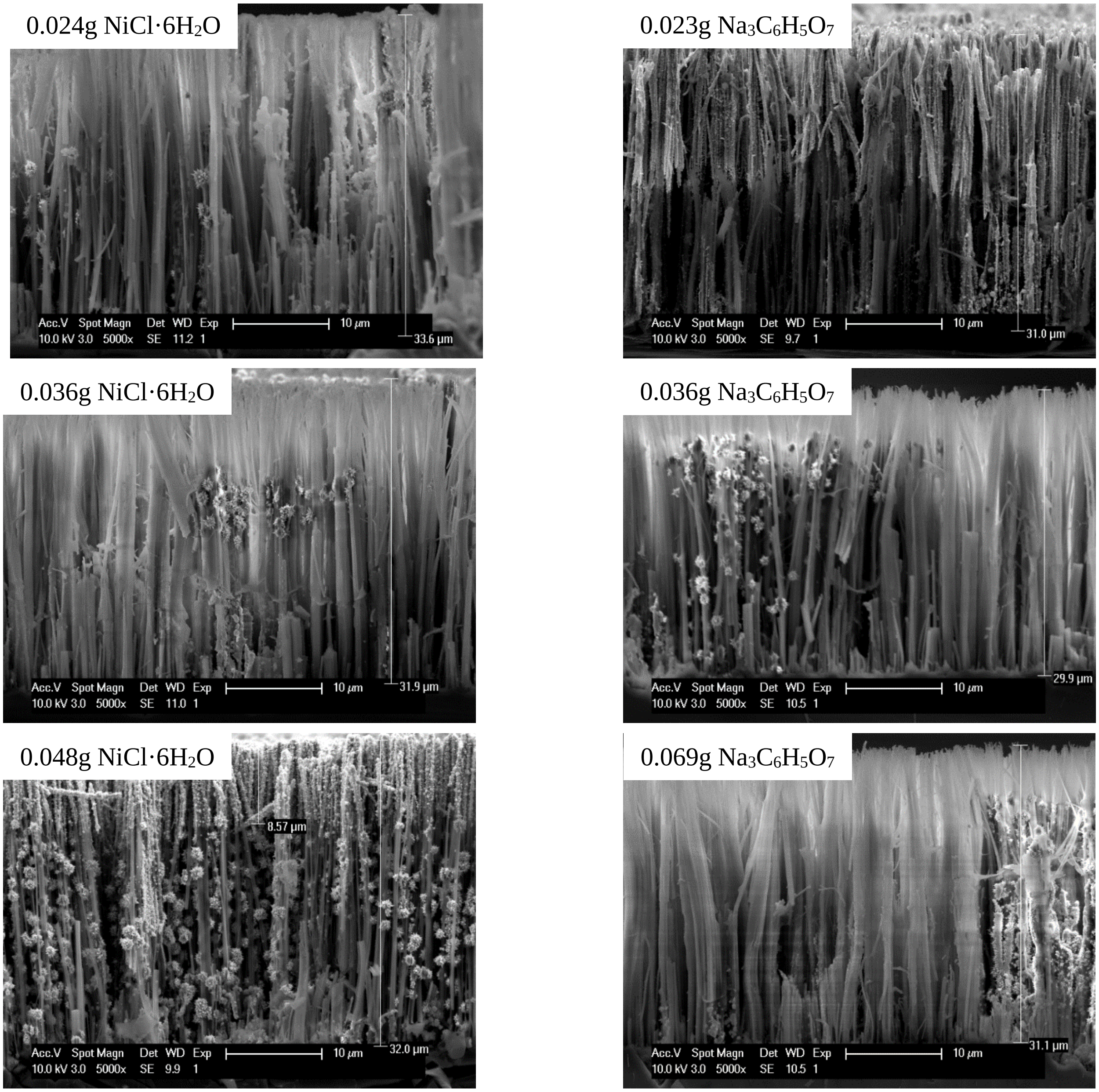


Figure 3. 7 Morphology of nickel particles on SiNWs when deposited in different concentrations of hydrazine (Table 3.1 #1, #3, #4, #5, #6)

Figure 3.7 shows that the coverage of nickel particles on the SiNWs changed with different hydrazine concentrations. The SiNWs could not be fully covered by nickel particles. When 250 - 600 μL of hydrazine were used for deposition, there were two kinds of coverage: the tips of the nanowires would be fully covered and nickel crystals formed as in the last image of Figure 3.7, while the lower section of the wires would not be covered by nickel crystals consistently. When 150 μL was used, nickel was not crystalized on the top parts of the nanowires. For this project, spotty nickel nanoparticle coverage is more desirable than full coverage, because spotty coverage can form the heterostructure in SiNWs after annealing. It is undesirable if all the silicon nanowires turn into nickel silicide nanowires, because that would decrease the efficiency of phonon scattering.

Figure 3.8 shows that the coverage of nickel particles on the SiNWs varied with different nickel chloride hexahydrate and sodium citrate dehydrate concentrations. If the nickel source, nickel chloride hexahydrate, is not adequate, there would not be enough nickel particles deposited on the SiNWs. Likewise, the concentration of sodium citrate dehydrate is very important: both increasing and decreasing the concentration of this complexing agent makes the nickel difficult to deposit on the SiNWs. Decreasing the amount of complexing agent leads to more $[Ni(H_2O)_6]^{2+}$ formation, which hinders the reduction of Ni^{2+}. It is still being researched why increasing the amount of complexing agent causes the same result as decreasing the amount of complexing agent.


0.024g $NiCl{\cdot}6H_2O$

0.023g $Na_3C_6H_5O_7$

0.036g $NiCl{\cdot}6H_2O$

0.036g $Na_3C_6H_5O_7$

0.048g $NiCl{\cdot}6H_2O$

0.069g $Na_3C_6H_5O_7$

Figure 3. 8 Morphology of nickel particles on SiNWs when deposited in different concentrations of nickel chloride hexahydrate and sodium citrate dehydrate (ref. Table 3.1 #7, #8, #9, #10, #11, #12)

From Figure 3.8, we can see that when 250µL - 600µL of hydrazine were used for deposition, there was a better coverage of nickel particles on the SiNWs, so those samples were used for further heterostructure formation studies.

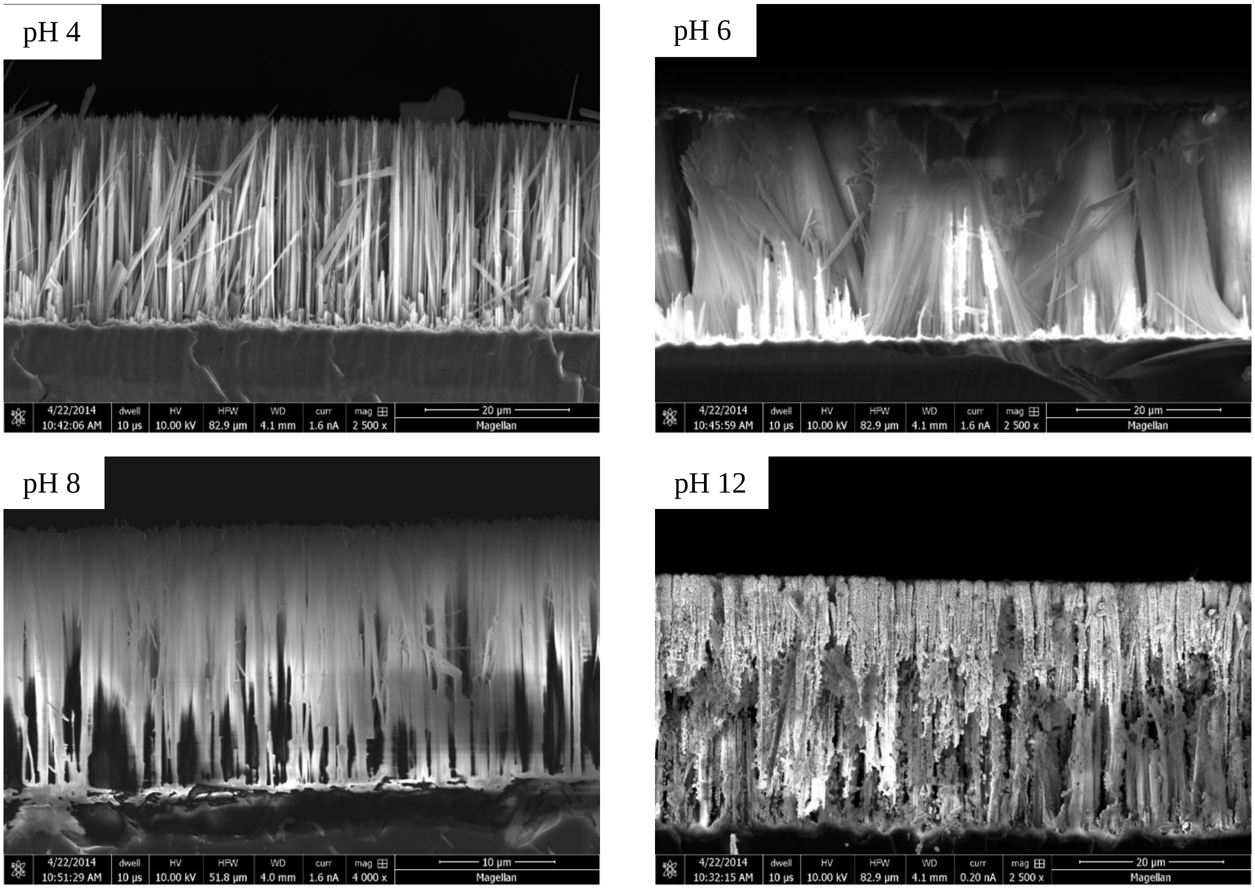


Figure 3. 9 Morphology of nickel particles on SiNWs when deposited in different pH values

For samples deposited under different pH conditions, the SEM results in Figure 3.9 show that the electroless nickel deposition reaction cannot occur in acidic conditions (pH<7). The sample used under pH of 6 deposition was synthesized unsuccessfully, whereby the wires could not be separated. Because of an unsuccessful synthesis, nickel particles were not formed on the sample.

In acidic solutions (pH>7), cloudy sediments form and the color of the solution changes from blue to green, which is shown in Figure 3.10. The green color in the acidic solution means that $[Ni(H_2O)_6]^{2+}$ was formed, which hinders the deposition reaction.

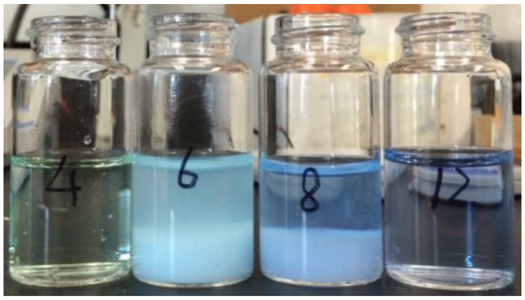


Figure 3. 10 Color of nickel deposition solution in different pH conditions. From left to right: pH of 4, pH of 6, pH of 8 and pH of 12.

After the deposition process, the samples were put in the tube furnace for annealing. In previous research, rapid thermal annealing (RTA) has been used for nickel silicide formation [106, 115], where silicon substrates were annealed for 3-5 minutes at about 500°C (mentioned in Section 2.2.4). The samples in this part of the project were annealed for 15 at 550°C in order to obtain the desired nickel particle coverage. The longer annealing time and higher temperature were chosen to ensure that nickel silicide would form in the nanowires.

Figure 3.11 shows the XRD pattern of the annealing results of samples #3 and #15 (ref. Form 3.1). The black lines show that nickel particles were deposited on the SiNWs. The red lines represent samples that were annealed and etched. However, no nickel silicide formed during the annealing process, which is indicated by the red lines. After 90 minutes the annealed samples were etched by the nickel removal etchant to remove nickel particles. NiO was left since it could not be removed by the nickel etchant. This explains the peaks on the XRD pattern red lines: NiO peaks appeared and nickel peaks disappeared after etching.

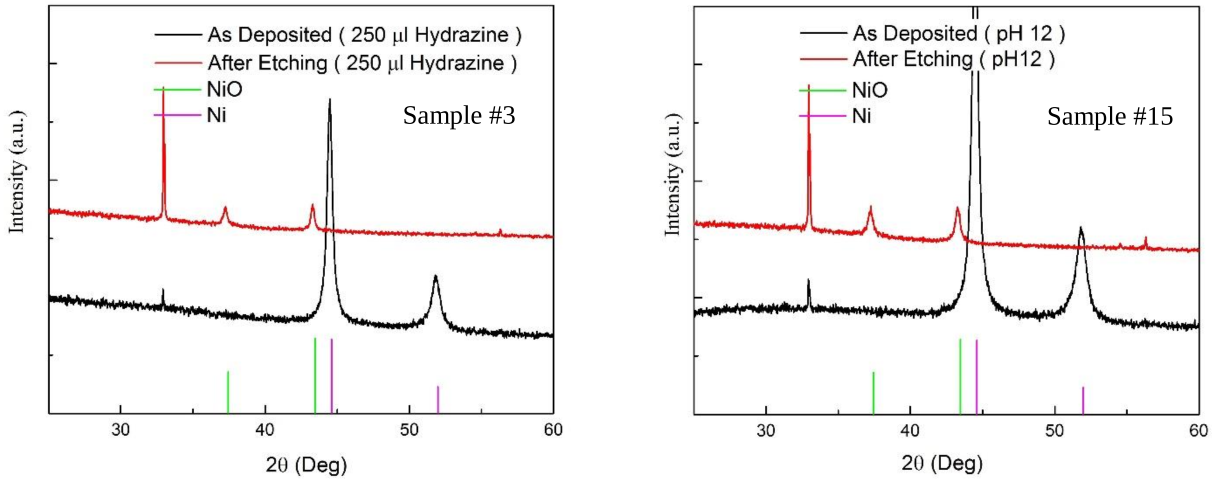


Figure 3.11 XRD (Cu Kα) pattern of SiNWs deposited with nickel particles; SiNWs after 550°C annealed for 15 min and etched for 1.5 hours in nickel etchant

The peak at 2θ = 33° is from Si (002) reflection [116]. For a (001) oriented silicon substrate examined with Cu Kα radiation, the only diffraction peak expected is (004) at 2θ = 69.1°. The XRD scanning for (001) SiNW arrays was stopped before 69.1° because the strong intensity from (004) would cover other peaks. The (002) peak is a forbidden peak, which should not appear. However, (002) may appear if the (004) is very strong, because strong (004) can cause multiple diffractions inside the samples.

It is possible that the orientation of single crystal (100) SiNWs might affect the results of silicide detection. If the silicide phase was formed epitaxially on the (100) substrate, it might be hard to match the nickel silicide XRD PDF cards when array samples are analyzed. Therefore, the silicon nanowires were scraped down to provide multiple orientation signals for XRD, as shown in Figure 3.12.

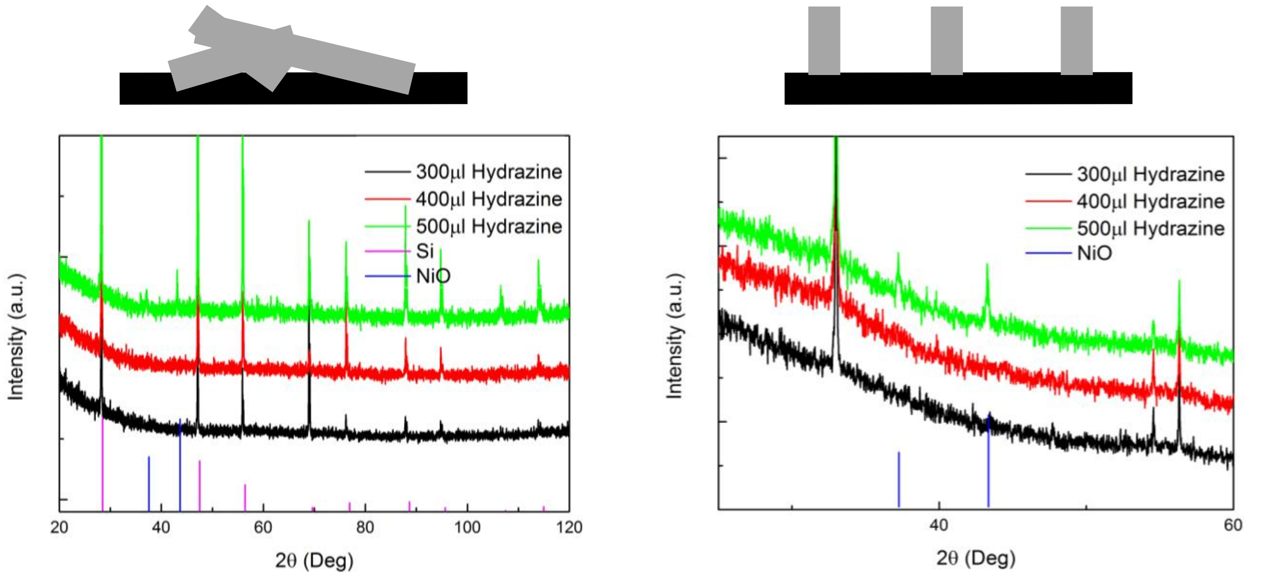


Figure 3. 12 XRD (Cu Kα) pattern of SiNWs from samples #4, #5, #6 (ref. Form 3.1). The patterns on the left are from SiNW powders which were scraped from a SiNW array substrate; the patterns on the right are from SiNW array samples before being scraped.

Figure 3.12 shows that NiO appeared in both powder and array samples. When powder samples were used for taking XRD patterns, silicon peaks appeared due to the random orientation of wires. The benefit of using silicon powders for XRD is that the strong (004) single- crystal silicon peak does not appear. However, many silicide peaks have 2θ angles similar to silicon peaks, so the silicon peaks might cover weak silicide peaks when using powder samples. When array samples are used for taking XRD patterns, the strong (004) peaks at 2θ = 69.1° need to be avoided, for the reason mentioned above. One observation regarding XRD patterns from array samples is that, sometimes, tungsten peaks next to 2θ = 69.1° (about 55°) will appear due to strong diffraction at (004).

As the XRD pattern of NiSi is almost the same as Si, it is possible that the formation of NiSi at about 500°C (mentioned in Section 2.2.4) will have the same orientation as a single crystal silicon, which means the weak silicide peaks would be covered by strong silicon peaks. Therefore, samples were annealed at 350°C to form a Ni_2Si phase, which has a different XRD pattern than silicon. The XRD patterns for samples annealed at different temperature are shown in Figure 3.13. Samples in the left image were annealed at 350°C and samples in the right image were annealed at 550°C. These samples were all deposited in the same condition, and they were etched for 1.5 hours to remove nickel after annealing. Samples were annealed for different time intervals to test their influence on phase formation. Figure 3.13 shows that a higher annealing temperature did not help the formation of the nickel silicide phase, but only caused oxidation.

Samples were tested using two different XRD detection techniques: PB (parallel beam) PSA and BB (Bragg-Brentano). All XRD patterns in this project were acquired by BB detectors unless specified. PB PSA is a technique used for thin film samples, while the BB technique is for bulk samples. The PB will only scan the very top layer of samples, which normally will take more time for the scanning due to lower intensity coming from samples. The reason for this is because the length of SiNWs (30 µm) is very short compared with the silicon substrate (550 µm), which can be viewed as a layer of thin film. If nickel silicide is formed in the SiNW array, by using the PB PSA, the signal of single crystal silicon may be lower. However, nickel silicide phases were not detected by the PB PSA detector, which is shown by the pink lines in Figure 3.13. Therefore, the BB detector was chosen for this project because it gives results faster.

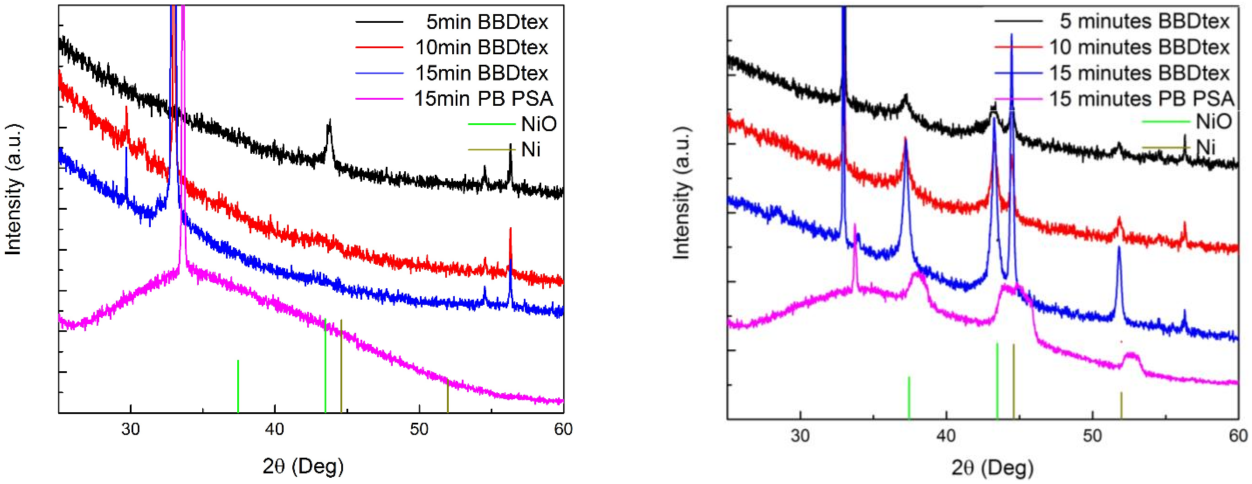


Figure 3.13 XRD (Cu Kα) pattern of SiNWs deposited under same condition but different annealing times and temperatures (left figure, 350°C, and right figure, 550°C)

The formation of green nickel oxide was very obvious, which was not only identified by XRD, but also visually. If the nickel oxide was not very thick, the sample color would only turn into gray (sample E). However, if the nickel oxide was thick enough, the whole sample would show a green color. Figure 3.14 shows that the color of the samples changed depending on the thickness of NiO. Samples A – C were deposited by E-beam (mentioned in Sec 3.2.2), where there was no oxygen contamination, so the samples still appeared dark black after two hours of annealing. Samples D - F were deposited in aqueous solutions and annealed for different times: 15 minutes, 60 minutes, and 2 hours. Their surfaces turned from gray to completely green, because the thicker NiO layers formed under the longer annealing time.

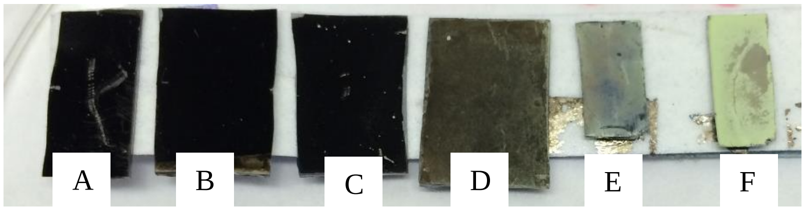


Figure 3. 14 Color of samples changed depending on the thickness of NiO

After changing annealing times, temperatures, and detection methods, it was still impossible to determine the existence of nickel silicide phases in the sample. Therefore, it was believed that oxidized layers formed outside the SiNWs during the deposition process, despite those wires being etched by HF before deposition. To avoid the formation of oxidized layers, other methods were tried in the remaining portions of this project.

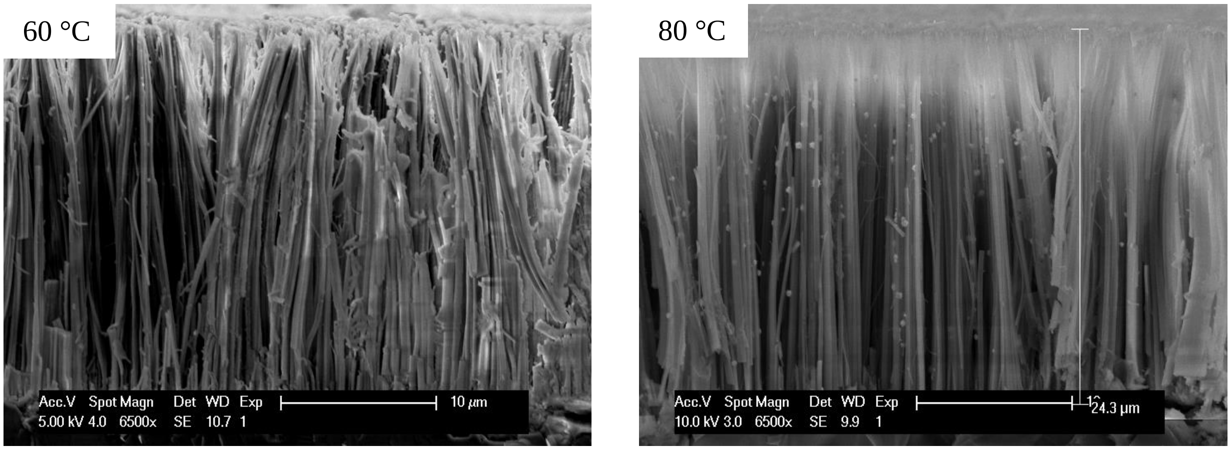


Figure 3. 15 SEM images of SiNWs after nickel deposition at temperatures lower than 90°C

It was first thought that samples would be more susceptible to oxidation in a basic solution than in an acidic solution, due to the existence of OH^{-}. However, as shown back in Figure 3.9, the nickel particles were not deposited on SiNWs in acidic solutions by using this method. It was also thought that heating samples in a solution at a temperature such as 95°C, would cause oxidation. Therefore, depositing at a lower temperature was attempted. The result, shown in Figure 3.15, suggests that lowering the deposition temperature hinders the deposition of nickel because the nickel reduction energy barrier cannot be overcome.

It was also found that the morphology of SiNWs would be degraded after being annealed and etched. Figure 3.16 shows the SiNWs' morphology changing from synthesis to deposition, then to the condition after being etched. When the final SiNW samples resemble Figure 3.16c, they cannot be separated and assembled on a device for measuring; as a result, other deposition methods were attempted to achieve the goal of forming nickel silicide phases.

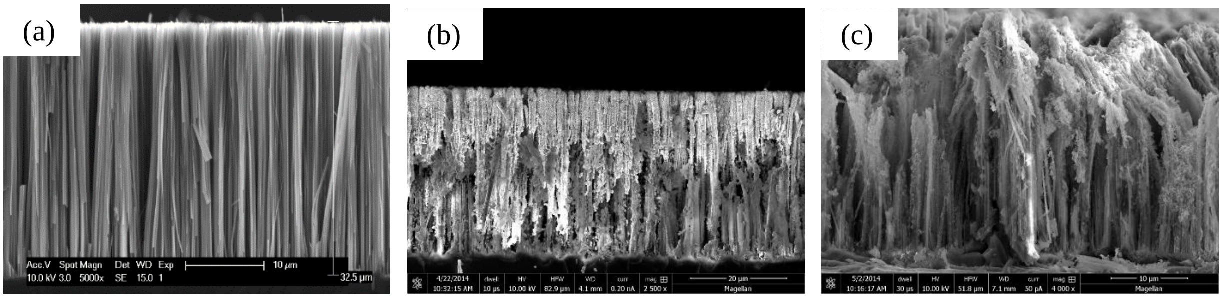


Figure 3.16 Morphology of SiNWs after different processes: (a) synthesis, (b) deposition in Sample #15 condition (ref. Form 3.1), (c) nickel etching

3.2.2 Other ways to deposit nickel particles on SiNWs

Electrodeposition was tried first, because it can be carried out at room temperature. Nickel particles were deposited on SiNWs at different time intervals from 100 seconds to 400 seconds. Figure 3.17a shows the XRD patterns of the electrodeposition samples, which were annealed at 700°C for 1 hour in case the nickel particles were too small to be identified by XRD, because small nickel particles crystalized into larger particles after annealing. The XRD pattern of the sample deposited for 400 seconds indicated the existence of nickel. However, nickel silicide was not formed and the energy dispersive spectroscopy (EDS) of those samples (ref. Figure 3.18) shows that all the nickel particles were deposited on top of the wires. The condition of nickel being deposited only on the top of SiNWs is related to the resistance of silicon substrate, which causing most of the electrons to gather on top of the wires during nickel reduction.

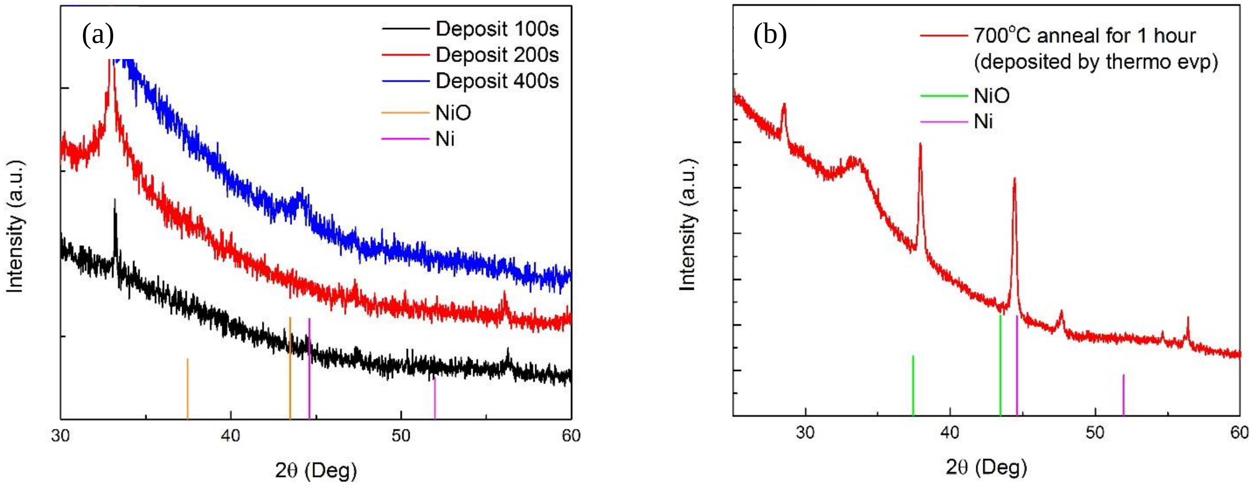


Figure 3. 17 (a) XRD (Cu Kα) pattern of SiNWs deposited by nickel electrodeposition at different time intervals (b) Nickel deposited by thermal evaporation. Both (a) and (b) samples were annealed at 700°C for 1 hour.

Since both electrodeposition and electroless deposition were unsuccessful in an aqueous solutions, it appeared that the oxidized layer formation was more related to an aqueous solution than to temperature. Therefore, thermal evaporation and E-beam deposition were tried next for nickel deposition. Both of these methods were carried out in a vacuum chamber without contact with an aqueous solution. Figure 3.17b shows the XRD pattern of thermal evaporation. In the XRD pattern, there were some other peaks detected besides Ni, NiO, Si and tungsten, such as the peak at 47°, which indicates the formation of nickel silicide. Although nickel oxide formed, it did not indicate that the oxidation layer came from the aqueous solution. The formation of nickel oxide may be related to the performance of the thermal evaporation device, because, in a later study, nickel oxide still formed with other deposition methods, when the annealing temperature was as high as 700°C. Figure 3.19 shows the EDS pattern of thermal evaporation on SiNWs. It shows that the deposition of nickel was not very uniform, with most of the nickel particles gathered on the tips of the wires.

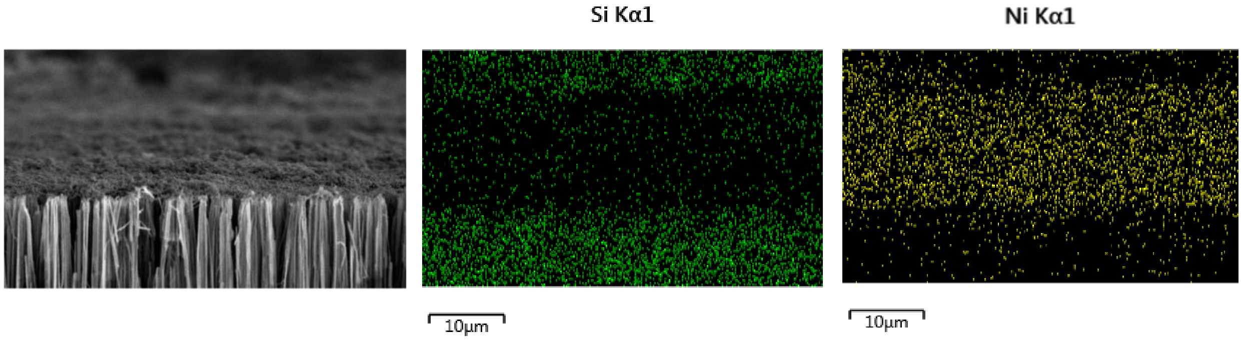


Figure 3. 18 EDS pattern of electrodeposition on SiNWs

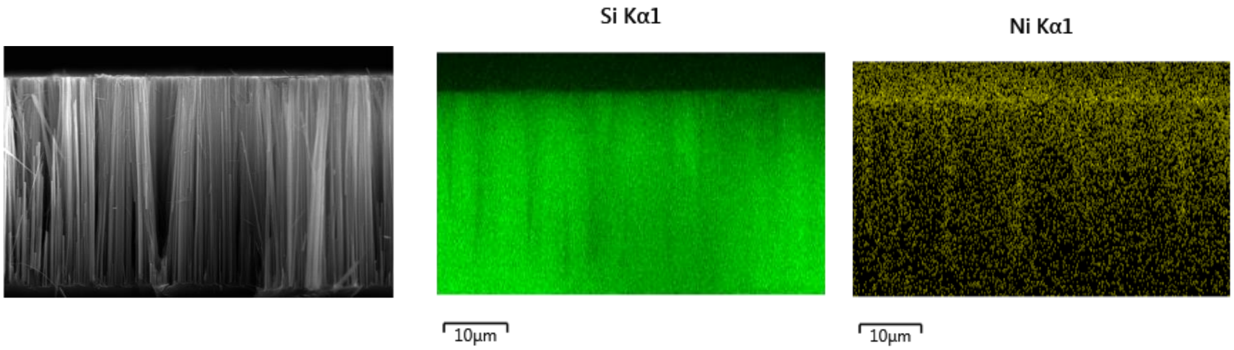


Figure 3.19 EDS pattern of thermal evaporation on SiNWs

The E-beam deposition method produced the same result: all the nickel particles being gathered on the tips of the wires. The electron beam could be tilted from 0° to 40° for deposition samples, so 0°, 15°, and 40° were used. However, the different angles produced no difference in the morphology under SEM. Figure 3.20 shows the SEM images of nickel particles deposited by E-beam on the tips of the SiNWs.

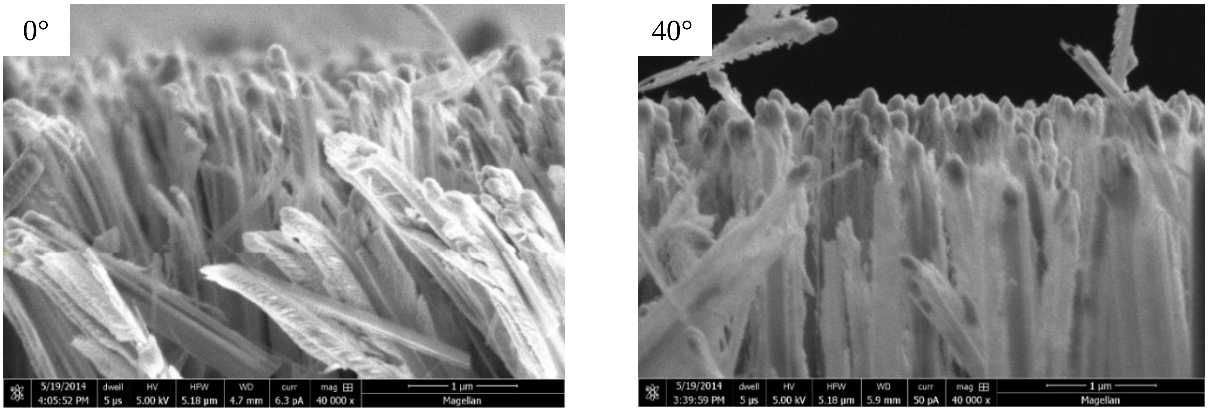


Figure 3. 20 SEM image of sample deposited by E-beam from different angles

Figure 3.21 shows the XRD patterns for E-beam samples. The black line indicates the successful nickel deposition by E-beam. Both the blue and red lines show that after 1 hour of annealing and 1.5 hours of etching, the nickel particles were removed. Other phases besides silicon and tungsten also appeared after annealing, which suggests that nickel silicide may have formed on the SiNWs. The red line, representing the sample after two hours of annealing, shows that the NiO phase formed. However, the blue line, representing the sample after one hour of annealing, shows that the NiO phase was not formed. The information suggests that there may be no benefit in annealing samples for prolonged times. It is suggested that a longer time interval could cause the NiO phase to form. The success of nickel silicide formation through E-beam also indicates that an aqueous solution can cause oxidation on a SiNW, which hinders the formation of nickel silicide.

The XRD pattern in Figure 3.22 shows that the results for different E-beam deposition angles are different. Only the sample deposited by electron beam at 40° shows the nickel silicide phase at 46°, but all the results show NiSi peaks at 36º. The peaks at 36º and 46° are mentioned in the references discussed in Section 2.3.6.

These samples were annealed for different times and etched for 1.5 hours. Regardless of the deposition angles, nickel gathered only on the tips of the SiNWs. Similar results, from different electron beam angles, support the belief that nickel silicide can form if there is no oxygen contamination during deposition. Considering that deposition in an aqueous solution can cover whole nanowires efficiently, compared to E-beam and electrodeposition methods (which deposit nickel only on the tip of the nanowires), depositing nickel in an oxygen-free solution was proposed for future investigation.

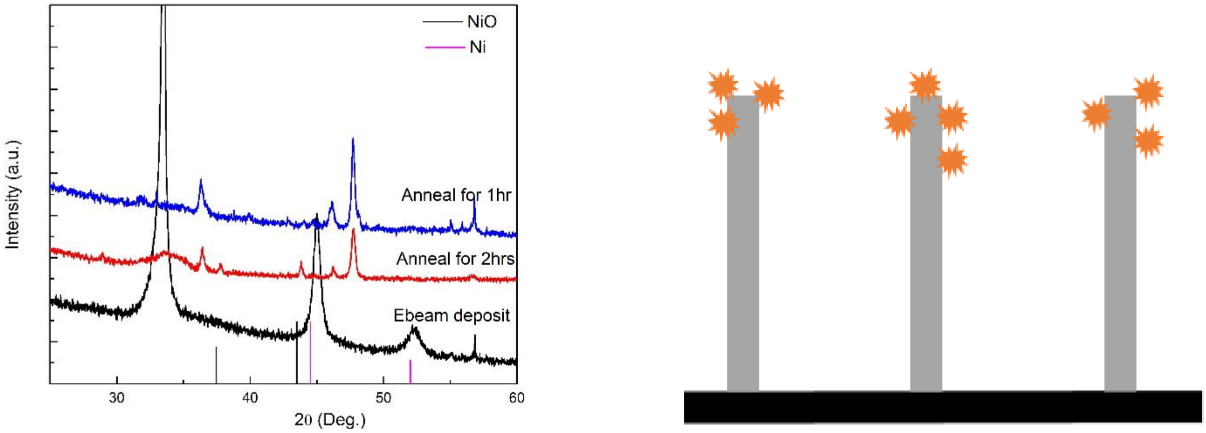


Figure 3.21 Left: XRD (Cu Kα) pattern of SiNWs deposited by E-beam. Right: schematic illustration of nickel being deposited on SiNWs by E-beam

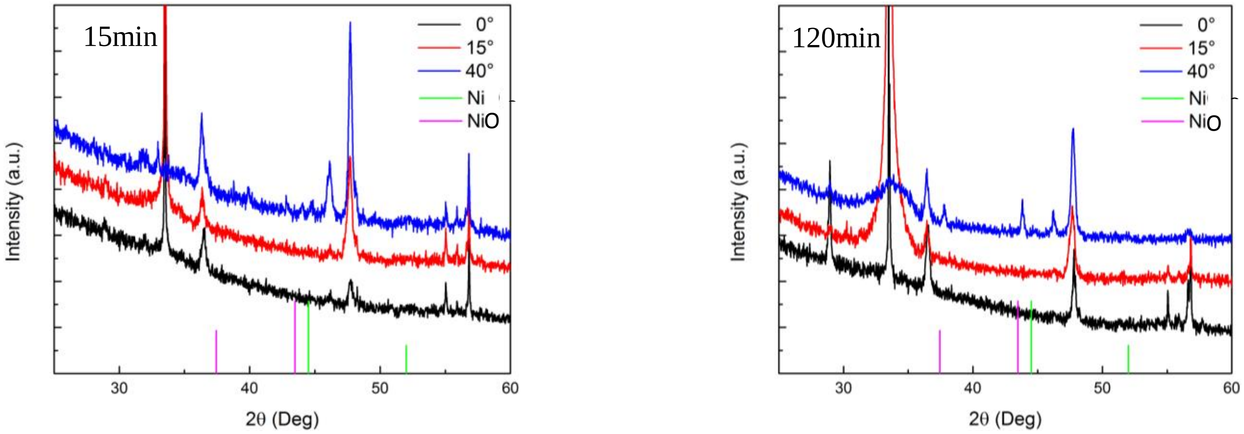


Figure 3. 22 XRD (Cu Kα) pattern of SiNWs deposited by E-beam from different angles and annealed for different times

3.2.3 Electroless nickel deposition in organic solution

In selecting an oxygen-free solution for deposition, HPLC dry organic solvent was considered first. As described in Section 2.3.3, Ni(COD)$_2$ was used as a nickel source and toluene as the solvent. The SiNW array chips were laid flat on the bottom of vials (ref. Figure 3.23 (a)), and after deposition there was a smooth nickel mirror formed on the wall of the vials, as shown in Figure 3.23 (c).

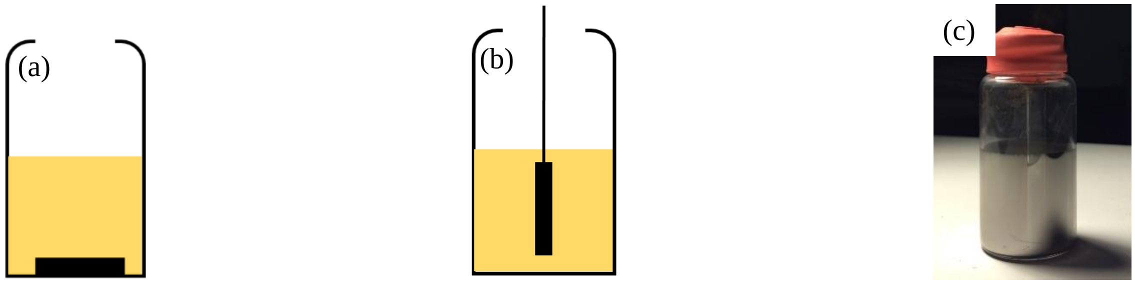


Figure 3. 23 (a) SiNW array chip lying flat on the bottom of a vial during deposition; (b) SiNW array chips suspended in the middle of vial during deposition; (c) Nickel mirror finish on the wall of vial.

Figure 3.24 shows the SEM images of SiNW array chip being deposited while lying flat on the bottom of a vial. There were more nickel particles that gathered on the tips of SiNWs than at the middle and bottom sections of the SiNWs. It was thought that this occurred because the vial was placed directly on the hot plate, making lower section of the vial hotter, causing the SiNW array chips to be heated unevenly. Therefore, the SiNW array chips were suspended in the middle of the vial, as shown in Figure 3.23b, but there were still more particles that gathered on the tips of the wires than at the middle and bottom sections of the SiNWs.

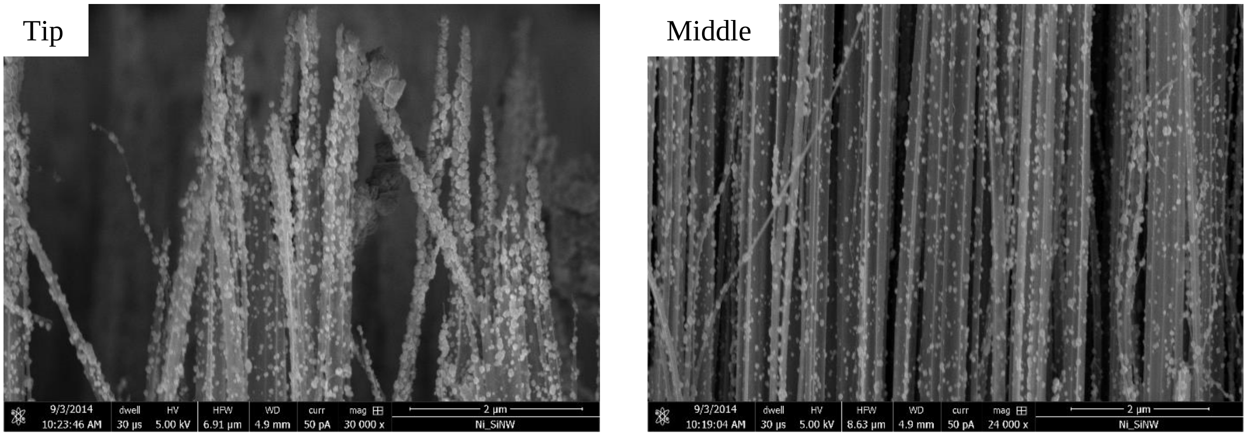


Figure 3. 24 SEM images of SiNW array with nickel particles deposited in organic solution

It was then proposed that if the temperature of the hot plate could be increased very rapidly, nickel particles might be deposited in the solution and fall on the tips of the wires quickly, providing more heterogeneous nucleation sites for nickel to deposit. An oil bath with a temperature control was chosen as the heat source. The temperature increasing rate of the oil bath was set at 0.6°C/min. Although the oil bath was placed outside of the glove box and the sample vial was sealed, the sample was found to be contaminated by atmospheric oxygen after nickel deposition, as shown in Figure 3.25. Also, the formation of nickel silicide was absent, as shown in Figure 3.25. As a result, it was decided that, for future nickel deposition experiments, samples would be suspended in the vials as shown in Figure 3.23b above.

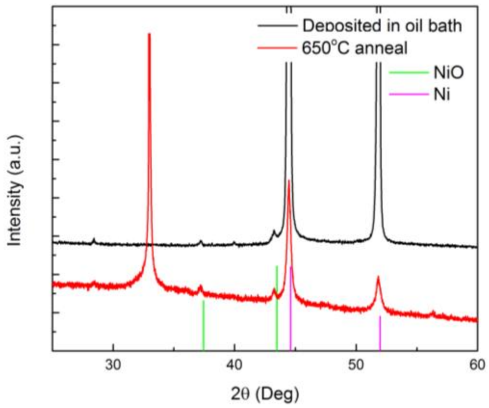


Figure 3. 25 XRD (Cu Kα) pattern of SiNWs deposited in organic solution using oil bath as the heat source

Figure 3.26 shows the XRD pattern of the SiNWs deposited in an organic solution inside the glove box, using a hot plate as the heat source. Figure 3.26a illustrates the phase change in the SiNWs from the newly synthesized SiNWs to SiNWs with a nickel silicide phase after the last etching step. The black line represents raw SiNWs, while the red line shows that nickel was successfully deposited on the whole nanowire. The blue line shows that after annealing at 650°C for one hour, the nickel silicide phase appeared. Although many other SiNW samples were annealed for 10 minutes, it was thought that the oxidized layer on the SiNWs may have hindered nickel from going into the silicon substrate, which was discussed in Section 2.2.4. Therefore, a longer time of one hour was used to anneal the SiNWs. The green line shows that all nickel particles were removed after being etched, and also no NiO was formed.

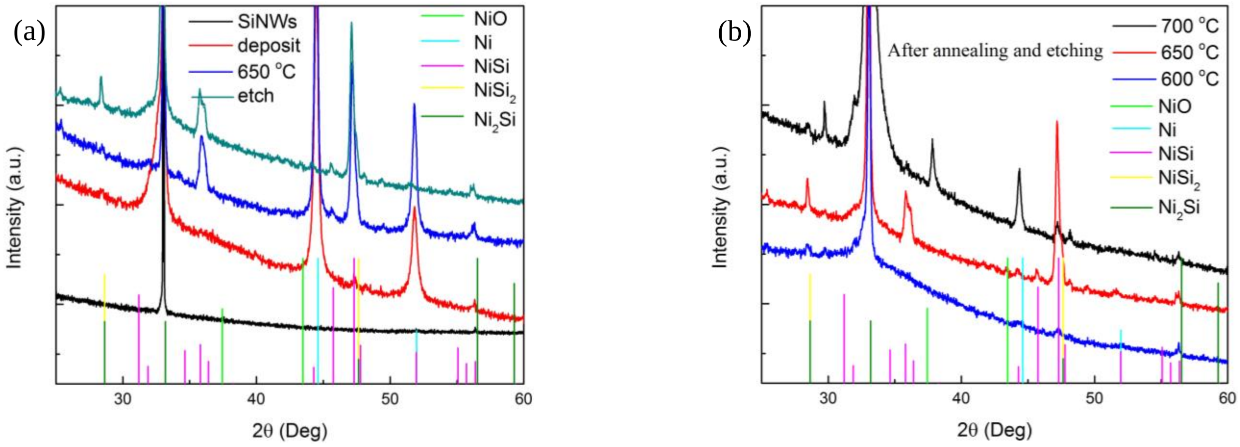


Figure 3. 26 XRD (Cu Kα) pattern of SiNWs deposited in organic solution inside glove box using hot plate as heat source

Figure 3.26b shows the effect of different temperatures on nickel silicide formation. 600°C, 650°C, and 700°C conditions were tried to determine the ideal temperature for a more apparent nickel silicide phase formation. Annealing at 600°C did not have an apparent nickel silicide phase formation and annealing at 700°C caused the formation of NiO. From the observed results, annealing at 650°C was considered the optimal annealing temperature. The sequence for nickel silicide phase formation by using an organic solution to provide the nickel source is shown in Figure 3.27.

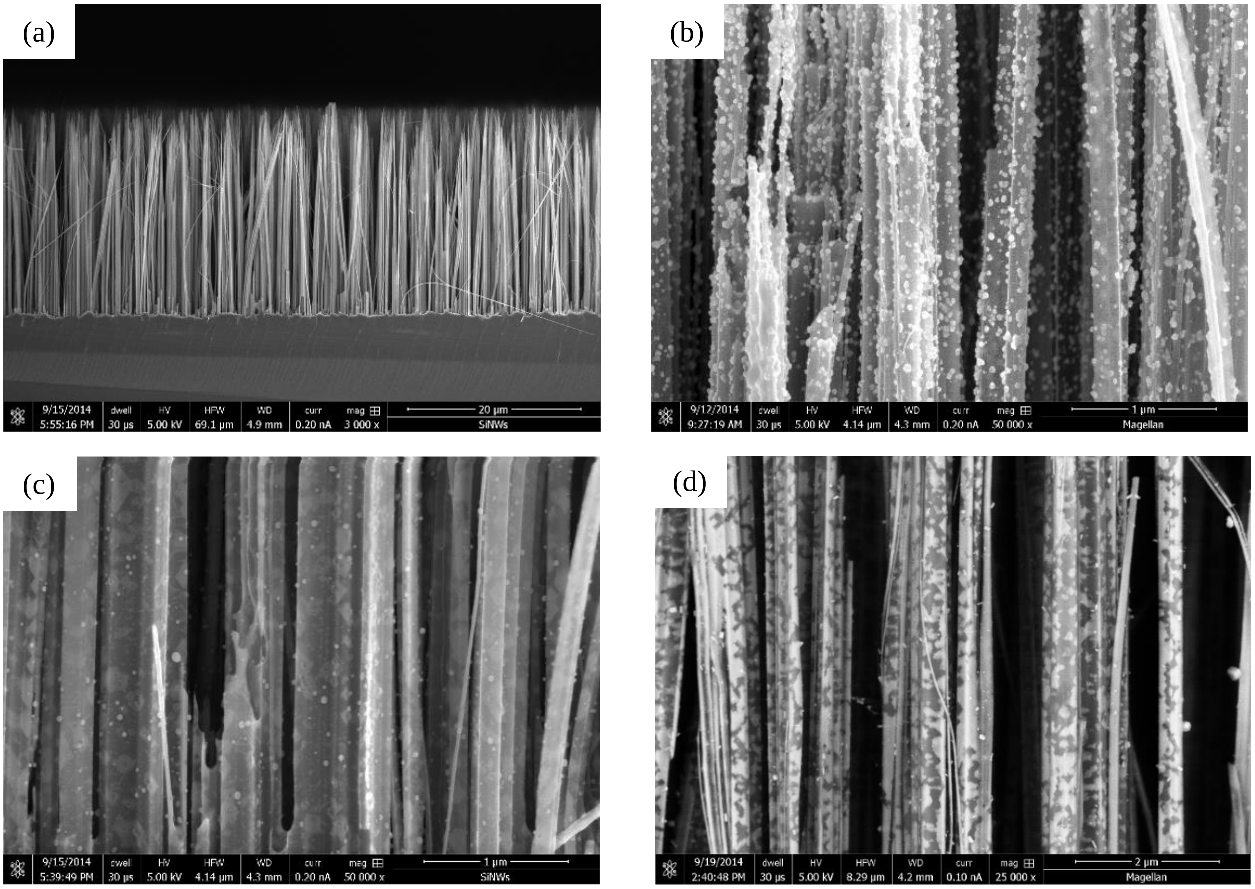


Figure 3. 27 Sequence for nickel silicide phase formation by using organic solution to provide nickel source. (a) SiNWs before deposition; (b) nickel particles deposited on SiNWs; (c) SiNWs annealed at 650°C for one hour; (d) SiNWs with nickel silicide phase after etching for 1.5 hours (back scattering electron).

To better analyze the nickel silicide heterostructure, the single crystal silicon substrate peaks in XRD were removed by tilting the SiNW array sample toward a certain angle, illustrated in Figure 3.28a schematically. This technique is called GIXRD (Grazing Incident X-Ray Diffraction). After tilting samples at right angles, all silicon peaks were removed, as shown in Figure 3.28b. However, it was still difficult to identify what kind of silicide phase was produced in the SiNWs, due to the complicated silicide heterostructure in the database.

Figure 3.28b shows that the strongest peaks of nickel silicide are associated with $NiSi_2$, NiSi, and $Ni_{31}Si_{12}$ which all appear at the same time, but it is difficult to find the matching peaks for Ni_2Si. This result matches the nickel silicide formation process shown in Figure 2.13 (Formation map of thin film nickel silidides). When nickel was annealed into a silicon substrate at over 400°C, the main silicide phase was $NiSi_2$. The lack of NiO and Ni peaks and presence of nickel silicide peaks are very promising results.

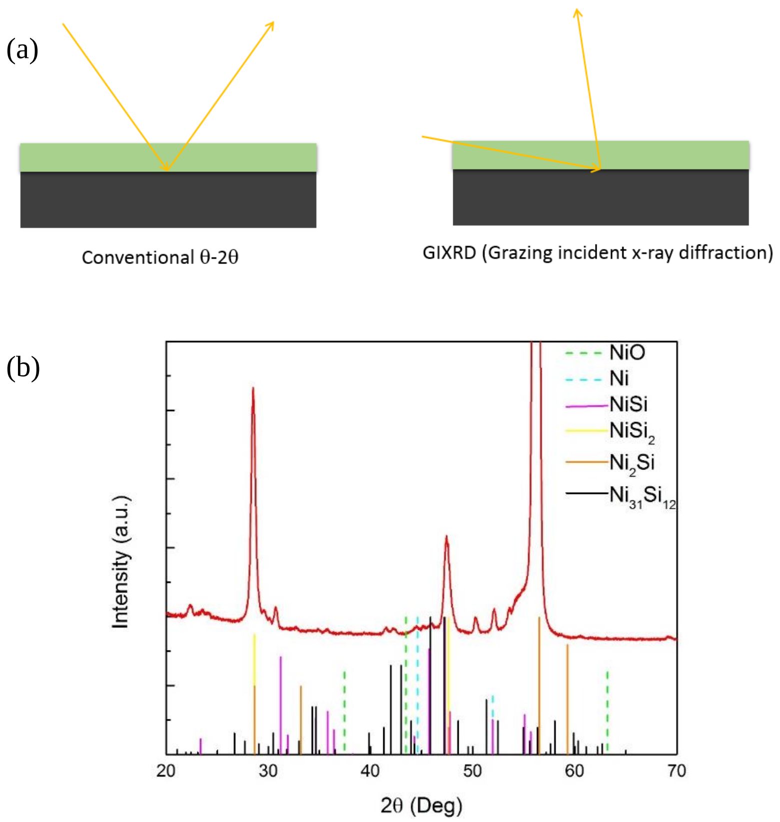


Figure 3. 28 Schematic illustration of the difference between conventional θ-2θ XRD analysis and GIXRD analysis

Besides XRD, the transmission electron microscopy (TEM) image also indicated the formation of nickel silicide heterostructures in Figure 3.29.

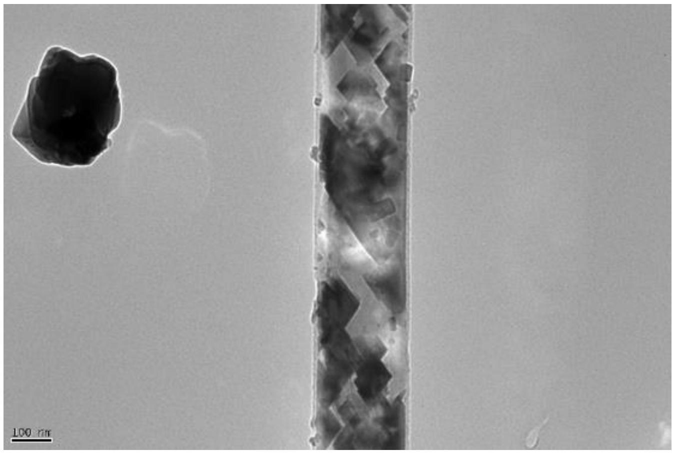


Figure 3. 29 TEM image of nickel silicide heterostructure on a single nanowire

4. Conclusions

This project has investigated the fabrication of metal-semiconductor heterostructures in silicon nanowire (SiNW) arrays. The heterostructures improve the figure of merit (zT) for thermoelectric materials by forming a metal-semiconductor interface, called the Schottkey barrier, to scatter phonons and to decrease their mobility (κ), thereby increasing the zT according to $zT=S^2\sigma T/\kappa$.

In this project, SiNW arrays were synthesized by metal-assisted HF etching. Different nickel deposition methods were tried to obtain diffusion of nickel through the process of annealing and the corresponding nickel silicide phase formation. The following conclusions are presented:

1) In the silicon nanowire synthesis process, the length of the nanowires is constrained by the amount of etching solution. Longer nanowires can be obtained by increasing the amount of etching solution and etching time. Changing the concentration of the etching solution will only deteriorate the morphology of wires.
2) Depositing nickel on SiNWs in a solution without electricity is a relatively simple way to deposit nickel particles, and they can cover whole nanowires, while nickel particles can gather only on the top when deposited by E-beam and electrodeposition. However, an aqueous solution will cause oxidation of the SiNWs and hinder the formation of nickel silicide.
3) Depositing nickel on SiNWs in an organic solution inside an oxygen-free glove box is the best way to prevent oxidation, and nickel can diffuse into the silicon substrate easily via annealing when there is no oxidation on the surface of SiNWs. Using the Ni(0) nickel source without a reducing agent also simplifies the process of deposition.
4) The dominant phase forming in SiNW samples is $NiSi_2$ after being annealed at 650°C for one hour in a tube furnace. Using grazing incident x-ray diffraction (GIXRD) to detect the nickel silicide phases can avoid the influence of silicon peaks compared to using the Bragg-Brentano (BB) detection method.

The obtained nickel silicide nanowire heterostructures should exhibit ideal zT based on the energy filtering theory provided.

5. References

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