UNIVERSITY OF CALIFORNIA, SAN DIEGO

# X- to W-Band Phased Arrays and Wafer-Scale Transmitters using Silicon Integrated Circuits

A dissertation submitted in partial satisfaction of the
requirements for the degree
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by

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2011

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University of California, San Diego

2011

DEDICATION

To my parents, Sebahattin and Nevin

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- B. Cetinoneri, Y.A. Atesal and G. M. Rebeiz, A two-channel Ku-band BiCMOS digital beam-forming receiver for polarization-agile phased-array applications, IEEE Radio Frequency Integrated Circuits Symp., June 2009, pp. 127-130.

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ABSTRACT OF THE DISSERTATION

**X- to W-Band Phased Arrays and Wafer-Scale Transmitters using Silicon Integrated Circuits**

by

Yusuf A. Atesal

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Professor Gabriel M. Rebeiz, Chair

The thesis presents X- to W-band arrays implemented in silicon technologies for different phased-array applications. An 8-20 GHz two-channel dual down-conversion receiver with selectable IF for interference mitigation is presented for digital beamforming applications. The receiver is fabricated using a 0.18-$\mu$m SiGe BiCMOS process and results in a channel gain (I and Q paths) of 46-47 dB at 11-15 GHz and $>$ 36 dB at 8-20 GHz with an instantaneous bandwidth of 150 MHz. The measured NF is $<$ 4.1 dB (3.1 dB at 15-16 GHz). The measured OP1dB is -10 dBm and the input P1dB is -56 to -40 dBm at 15 GHz depending on the gain, which is sufficient for satellite applications. The on-chip channel-to-channel coupling is $<$ -48 dB. The measured EVM is $<$ 3% for a 1 Msps QPSK modulation at 8-20 GHz, and $<$ 1.8% for a 0.1, 1 and 10 Msps QPSK, 16QAM and 64QAM modulations at 15 GHz. The chip has ESD protection on the RF and DC pads, consumes 70 mA per channel from a 3.0 V power supply and is 2.6$\times$2.2 mm$^2$,

including all pads. A 15 GHz 8-element phased array with a NF $<$ 3.9 dB is also demonstrated with multiple simultaneous beam performance using digital beamforming.

In another project, a silicon-based 8-element phased array based on an All-RF beamforming topology is integrated together with the antennas and digital control circuitry on a single Teflon board. The chip-on-board package, together with 8 X/Ku-band RF inputs and one RF output in a 2.2$\times$2.5 mm$^2$ area, and the appropriate grounding and Vcc connections, are modeled using a 3-D EM solver. The design results in a low coupling between the different RF ports, and ensures stability even with a channel gain of 20 dB at 12 GHz. The measured patterns show a near-ideal performance up to a scan angle of 60$^\circ$ with an instantaneous scanning bandwidth of 11.4-12.6 GHz (limited by non true-time delay connections between the antennas and the chip). Temperature tests indicate that the silicon chip maintains excellent phase stability and rms phase error up to 100°C.

Finally, the first mm-wave wafer-scale silicon power amplifier array is implemented using 0.13 $\mu$m BiCMOS technology. The power combining is done in the free-space using the high efficiency on-chip antennas. First, a W-band SiGe power amplifier is designed and fabricated together with a high-efficiency on-chip microstrip antenna. The power amplifier consumes 120 mA from a 1.7 V supply and the antenna/amplifier results in an effective radiated power (EIRP=$P_tG_t$) $>$ 10 dBm from 88 to 98 GHz, with a peak of 14.6 dBm at 92 GHz. Then, a 3$\times$3 power amplifier array is demonstrated with an equivalent isotropic radiated power (EIRP) of 33-35 dBm at 90-98 GHz. This results in a total on-chip power of 21-23 dBm, and a total radiated power of 17.5-19.5 dBm. The our knowledge, this is the highest power (and EIRP) achieved from a single silicon chip at millimeter-waves. The measured patterns of the array show single-mode operation and $\sim$100% free-space power-combining efficiency with a 3-dB beamwidth of 28$^\circ$ and a directivity of 15.5 dB (gain of 12 dB). The total power-combining efficiency including the antenna losses is 45$\pm$10%. It is shown that by using this technique high power (1-2 W) millimeter-wave transmitters with phased array capabilities can be realized in silicon technologies which will be compatible with best III-V solutions. The application areas are in millimeter-wave transmitters and wafer-scale phased arrays.

# Chapter 1

# Introduction

## 1.1 Phased Array Systems

Phased arrays are an array of antennas which filters electromagnetic waves in the spatial domain ( [2, 2]) and are widely used in communication and radar systems [3–7]. The signals are received (or transmitted) in desired directions (peaks) by constructive interference between the signals at each antenna, and simultaneously blocked in undesired directions (nulls) by de-constructive interference. The spectral efficiency of the transmit/receive systems are increased by the spatial filtering of the phased arrays (interfere rejection, etc.) result in higher data-rate systems [8]. The total effective radiation pattern (scan angle, peaks, nulls, sidelobe levels, beamwidth, etc) of the antenna array is determined by the signal amplitude and phase (time delay) weighting at each antenna. For electronically scanned arrays, the phase and amplitude weighting is done electronically and hence, the beam steering and beam-forming are much faster than mechanical systems (nearly instantaneous) [8, 9]. Fig. 1.1 shows the basic concept of a phased array system with 8 antenna elements in the receive mode. The incoming signal from an angle $\theta$ arrives at each consecutive antenna pairs with a time difference of $\triangle$T, resulting in a phase difference of $\triangle\phi$, where

$$\triangle T = \frac{d\cos\theta}{c}, \quad \triangle\phi = kd\cos\theta, \quad k = \frac{2\pi}{\lambda}, \tag{1.1}$$

and $d$ is the distance between the antenna elements.

The antennas are followed with variable time delays and variable attenuators (or variable gain amplifiers), in order to compensate for phase and amplitude difference between the antenna elements so as to have constructive summing in desired directions while having de-constructive summing in undesired directions. Note that transmit phased arrays operate on the

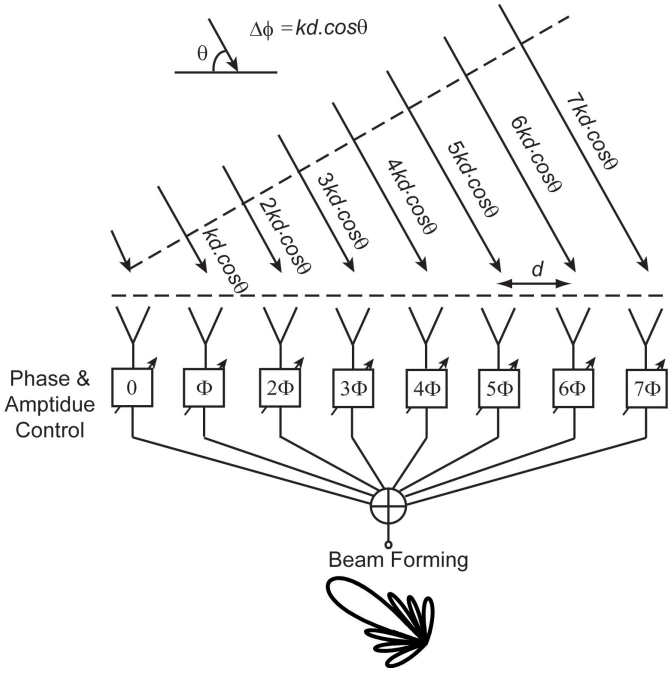



**Figure 1.1**: Block diagram of an 8-element phased array.

same principles. The variable time delays can be realized with variable phase shifters for narrow band applications or true-time-delay elements for wideband applications. Phased arrays based on silicon technologies have gathered particular interest, since both variable phase-shifters and variable gain control blocks are realizable together with complex transmitt/receive modules on a single silicon chip, and hence can replace complex III-V chipsets.

### 1.1.1 Phased Array Architectures and Previous Work on Phased arrays

The phase shifting can be realized in the RF, LO, IF or digital paths of the T/R modules (Fig. 1.2). The RF phase shifting topology (all-RF architecture) has been the most commonly used one since the invention of phased arrays due to high signal-to-interferer ratio (since the beamforming is done in the RF domain before the down-conversion, interferers are rejected before the non-linear mixers), lowest layout area, lowest power consumption (especially for large number of elements), and no need for LO distribution. Silicon phased arrays with all-RF architecture have been successfully demonstrated from X- to W-band with 4-16 elements, multiple beams, and multiple polarizations in transmit or receive configurations ( [10–16]). The LO and IF phase shifting architectures are also demonstrated using SiGe BiCMOS and CMOS processes [17–20].

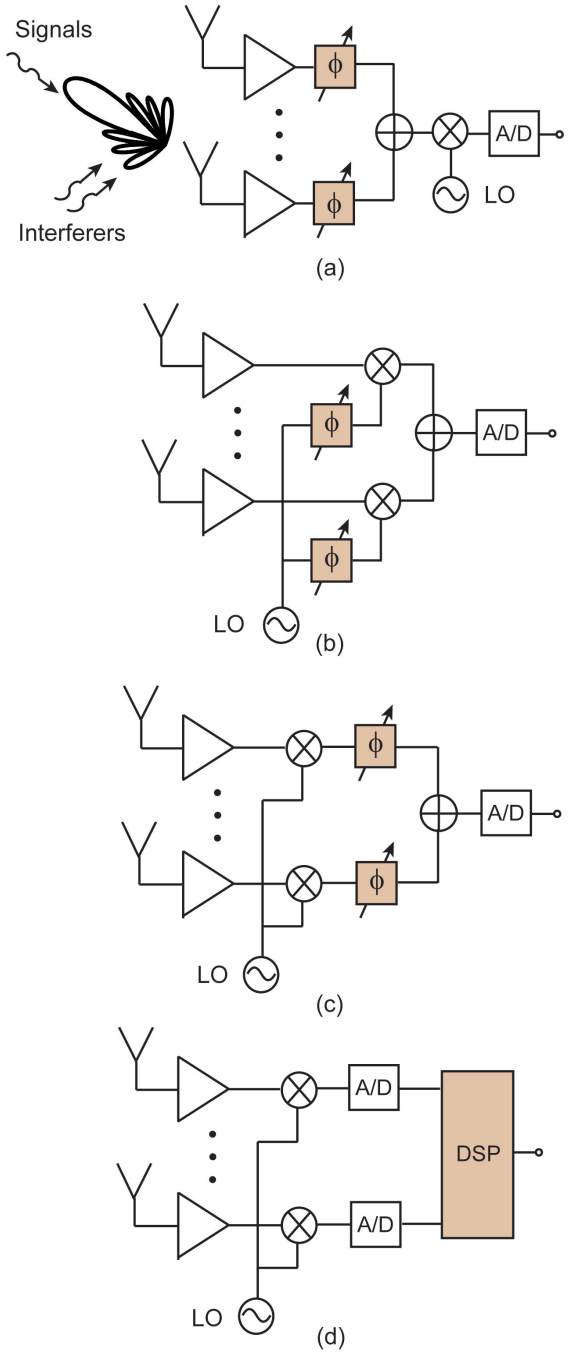



**Figure 1.2**: Block diagram of phased array architectures (a) RF phase-shifting, (b) LO phase shifting, (c) IF phase shifting, and (d) digital beam-forming.

### 1.1.2 Digital Beam-Forming Phased Arrays

In the digital beam-forming (DBF) architecture, the signals are first digitized, and then the phase shifting (time delaying) is preformed in the digital domain (Fig. 1.2d). The DBF applies the required amplitude and phase (time delay) weighting to each antenna element to result in a number of simultaneous patterns (typically 2-6), each with its own scan angle, side-lobe level and bandwidth [21, 22]. Furthermore, if the antennas are dual polarized, then each beam can have an independent polarization (linear or circular). DBF architecture results in the highest performance systems, especially for more than 4 simultaneous beams. A disadvantage of the DBF is relatively high power consumption.

The DBF architecture is ideal for satellite systems since the required S/N ratio for low bit-error-rate is 12-14 dB at the aperture level. However, at the element level, the S/N ratio is $< 0$ dB (for 16-32 elements and larger), and the number of bits in the baseband A/D converter is not limited by the S/N ratio but by the interference levels. Therefore, in order to use a low number of A/D bits and to reduce the computational complexity in the DBF, it is essential to employ a large degree of filtering at the element level (a sharp EVM filter is generally used).

The digital beam-former architecture has seen limited use due to the cost, size and power consumption of GaAs-based X and Ku-band down-converters. A two-channel SiGe-BiCMOS solution is presented in this dissertation with selectable IF frequencies and 8-20 GHz operation capability.

### 1.1.3 Packaging Issues for Silicon Phased Array Chips

The silicon integrated phased array circuits should be packaged for a complete product. A lot of work has been done on creating very high-performance microwave and millimeter wave silicon phased arrays, but packaging of these chips received comparatively little attention. Packaging environment can dramatically affect the RFIC performance, even can render the chip unusable. The degradation can be seen as excessive insertion loss, high return loss or low pin-to-pin isolation. As an example, for a single-ended high gain amplifier at 60 GHz (3-4 stages, 20dB gain), 80-100 pH ground inductance would be sufficient for oscillations.

The main challenge comes from the interface between the silicon chip and a board. Different techniques are used for chip-to-board interface (flip-chip, ribbon-bonding, etc) and bondwires are widely-used for connecting the chip to board (outside). A bondwire behaves as an inductor (or high-impedance transmission line) at millimeter-wave frequencies, and the inductance value depends on the diameter, length and shape (spacing to ground, etc) of the bondwire.

A widely used rule-of-thumb value for bondwire inductance is 1nH/mm. This inductance by itself degredates matching on the RF paths, which would cause reflections and loss. Therefore, a matching network should be carefully designed so as to compensate for the bondwire inductance.

In addition, on-chip measurements of silicon-chips provides an excellent ground (supply) to the chips through RF-ground pads (de-coupling capacitors). However, when a chip is mounted on a board, the on-chip ground (supply) will not be at perfect ground (supply), but will be an inductive ground (supply) due to the bondwire inductance. This inductance can affect the chip performance greatly: it can change the gain (magnitude and phase), noise-figure, matching and stability. In addition to the bondwire inductance, another issue is the coupling between the bondwires, which would deteriorate the isolation between different pins of the silicon chips.

In chapter 2, a low-cost 8-element phased-array board with a single silicon chip is demonstrated and the affects of packaging environment together with bondwires RF-transitions and matching networks are analyzed and addressed.

## 1.2 Power Amplifiers and Phased Arrays Transmitters

One of the most design-challenging components in transmitters is the power amplifiers. Fully-integrated SiGe (or CMOS) power amplifiers can replace complex GaAs-based transmit/receive modules and results in full system-on-chip solutions for phased-array or point-to-point communication systems. W-band power amplifiers (PAs) have been demonstrated using GaAs and InP-based HEMT monolithic microwave integrated circuit (MMIC) processes [23,24]. Recent works in silicon germanium technology have demonstrated the capability of generating significant millimeter-wave power within W-band (75 to 110 GHz) with reasonable efficiencies [25, 26]. However, generating high output powers is still a bottleneck for silicon designs due to low breakdown voltage limitations. The millimeter-wave designs also suffer from high on-chip losses due to low Q of the on-chip passive components. In addition, at millimeter-waves, transition between power amplifiers and the antennas are considerably lossy and challenging. This makes high-power SiGe amplifiers a crucial and challenging building block for many millimeter-wave systems. Recently published works show that 10-100 mW can be achieved using SiGe-BiCMOS, and CMOS processes (21 dBm [26], 19.6 dBm [25], 11 dBm [27], 10dBm [28]).

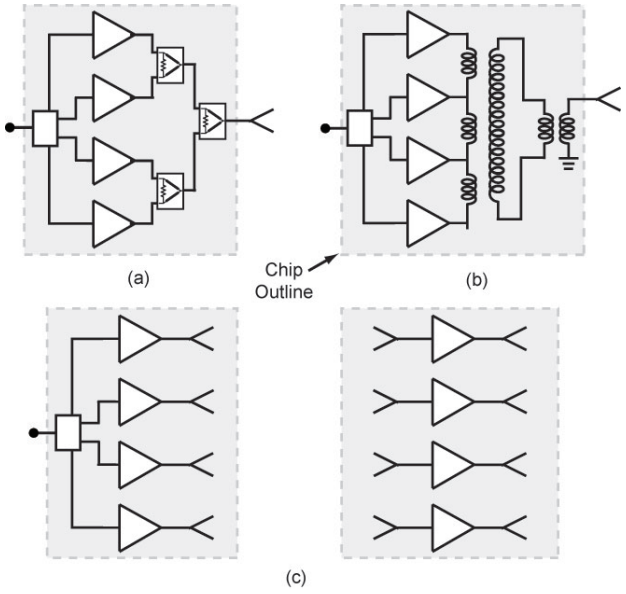



**Figure 1.3**: Block diagram of (a) Wilkinson, (b) transformer, and (c) quasi-optical power-combining techniques.

### 1.2.1 On-Chip Power Combining Techniques for High-Power Amplifiers

On-chip power combining and balanced device operation has been exploited for increased maximum available output power per chip. Balanced amplifiers result in higher power levels, and has been demonstrated [25], however, they suffer from large physical layout size and lossy couplers. In order to generate higher power levels, several on-chip power combining methods have been proposed and demonstrated using SiGe-BiCMOS and CMOS processes. Fig. 1.3 shows block diagram of three different power combining methods: Wilkinson based, transformer based, and free-space (quasi-optical). A 20 dBm (100 mW) power amplifier at 60 GHz is reported in [29] using Wilkinson couplers for power combining. Another Wilkinson-combiner based power amplifier is reported in [27] and achieved 12 dBm output power at 90-100 GHz. At 60 GHz, 14.5 dBm and 23 dBm power amplifiers with using distributed active transformers are reported in [30] and [31], respectively. The Wilkinson and transformer based approaches are adequate for 2-4 amplifiers, but still suffer from high on-chip combining losses especially for large number of elements (8-16 elements), and also from RF output transition losses. In addition, none of these techniques can be scaled to higher power levels, and on-chip designs achieving 0.1-1 W were not proposed or demonstrated.

### 1.2.2 Free-Space (Quasi-Optical) Power Combining

Quasi-optical (free-space) power combining was developed in the 1980s and is based on two different topologies: The grid and the antenna approach. Grid designs use an inter-element spacing of 0.1-0.2$\lambda_0$ and consider the transistor arrays as being imbedded in impedance sheets [32]. Antenna-based designs use an inter-element spacing of 0.5-1.0$\lambda_0$ and each amplifier/antenna element is designed taking into account the mutual coupling between the antennas [32–36]. Both the grid and the antenna approach have been demonstrated at Ka to W-band frequencies, and with excellent results using GaAs or InP components in a hybrid approach [33–42]. The antenna-based approach allows for a planar RF distribution network and is compatible with wafer-scale systems.

For silicon applications using antenna-based free-space power combining, a high-efficiency electromagnetically-coupled (EM) antenna can be designed directly on the silicon chip, and each SiGe (or CMOS) amplifier can be connected to the antennas. Unlike the Wilkinson and transformer based power-combining approaches, the free-space power combining has no limitation on the number of elements since the power combining is done in air and is 100% efficient (assuming equal amplitude and phase distribution to the elements, and no antenna losses). Therefore, applying this novel technique to the silicon designs (an NxM power amplifier array) allows for high power transmitters achieving 0.1-1 W at millimeter-waves (W-band and above). Furthermore, wafer-scale phased arrays (NxM, transmit or receive) can be designed by introducing phase shifters at each element together with the amplifier.

## 1.3 Thesis Overview

This thesis presents X- to W-band phased arrays and wafer-scale transmitters using SiGe BiCMOS techonologies. First, a two channel X- to Ku-band digital-beam-forming phased array receiver for satellite communications is demonstrated. For a complete phased array receiver, the silicon-chips should be packaged (connected to a board) together with radiating elements (antennas). Therefore, packaging affects are carefully analyzed, and as a demonstration an 8-element phased array is impelemented on a Teflon board by using an 8-element silicon phased array chip with All-RF phase shifting arhitecture. The chip-to-board transitions and raditating elements are designed in HFSS, and real-life pattern measurements of the complete system are presented. The chip-to-board transisitions are lossy, challenging and expensive, especially at millimeter-waves (90 GHz and above) where power generations is already limited by

breakdown-voltages and on-chip losses. By applying a very novel technique -free-space power combining- to silicon-chip design, the first millimeter-wave wafer-scale transmitters (power amplifiers) are implemented. This technique not only eliminates the need for output transitions, but also allows for 1-2 W millimeter-wave transmitters and phased-arrays that are compatible with best III-V solutions.

Chapter 2 presents the first fully integrated two-channel SiGe BiCMOS receiver, capable of operation in the 8-20 GHz, for digital beam forming phased arrays. The receiver is based on a dual-down-conversion architecture with selectable IF for interference mitigation, and the silicon chip is fabricated using a 0.18-$\mu$m SiGe BiCMOS process. The chip consumes 70 mA per channel from a 3.0 V power supply and is 2.6$\times$2.2 mm$^2$, including all pads. The receiver achieved excellent performance over the entire 8-20 GHz bandwidth, and theoretical and measurements results are presented. The receiver can be used with selectable IF frequencies from 1.8-3 GHz, and is also characterized versus temperature. An 15 GHz 8-element phased array with a diplexed LO distribution network was demonstrated at 15 GHz using four of these receivers, and achieved results are presented. The chip was also used in a real-time FPGA-based phased array system at 15 GHz to generate three simultaneous beams each with 10.7 Mbps links.

Chapter 3 presents a complete 8-element X/Ku-band phased array based on a single silicon chip. The phased array is built on single-layer Teflon substrate and contains an 8-element silicon phased array chip, the radiating elements, control circuits and all RF transmission lines. Packaging aspects of multi-element phased arrays, such as RF transitions and associated impedance matching networks, coupling between the different RF ports, Vcc decoupling and oscillations - especially in high gain designs, and the creation of a low-inductance ground between the chip and the antenna distribution board are carefully analyzed. It is shown that chip-on-board packaging results in high isolation (low coupling) between the different RF ports, and ensures stability even with a channel gain of 20 dB at 12 GHz. An 8-element phased array card with instantaneous bandwidth of 11.4-12.6 GHz, near ideal measured patterns and scanning up to 60$^\circ$ is successfully demonstrated. To the best of our knowledge, this is the first 8-element phased array based on a single silicon chip.

Chapter 4 presents the first wafer-scale power amplifier/combiner in silicon technology. A mm-wave wafer-scale power amplifier array implemented in a 0.13 $\mu$m BiCMOS technology fabricated together with high efficiency on-chip microstrip antennas is presented. The power combining is done in the quasi-optical domain using high efficiency on-chip antennas. A 3$\times$3 power amplifier array with 0.6$\lambda_0$ at 94 GHz spacing between the antenna elements is

demonstrated with excellent performance, an output power of 21-23 dBm and highest equivalent isotropic radiated power (EIRP) up-to-date from a silicon-chip (33-35 dBm at 90-98 GHz). The measured patterns of the wafer-scale array are presented and are in excellent agrement with simulations and show single-mode operation. The design is wafer-scalable and it is shown that applying quasi-optical design methodology to silicon-based designs would result in fully integrated millimeter-wave transmitters (with phased array capabilities) which are competitive with the best III-V solutions.

# Chapter 2

# A Two-Channel 8-20 GHz SiGe BiCMOS Receiver with Selectable Intermediate Frequencies for Multibeam Phased-Array Digital Beamforming Applications

## 2.1 Introduction

Satellite systems operating at the 8-21 GHz band and located in different earth orbits are used for communication data links with data bandwidths of 0.1-50 Mbps depending on the receiving aperture size [43]. This system is therefore well suited for a digital beam-forming array due to the low received power levels (Fig. 2.1a). In this architecture, each antenna element is connected to an I/Q down-converter, and the received I/Q signals are digitized and sent to a digital beam-former (DBF) [44]. The DBF applies the required amplitude and phase (time delay) weighting to each antenna element to result in number of simultaneous patterns (typically 2-6), each with its own scan angle, side-lobe level and bandwidth [21, 22]. Furthermore, if the antennas are dual polarized, then each beam can have an independent polarization (linear or circular).

The DBF architecture is ideal for satellite systems since the required S/N ratio for low

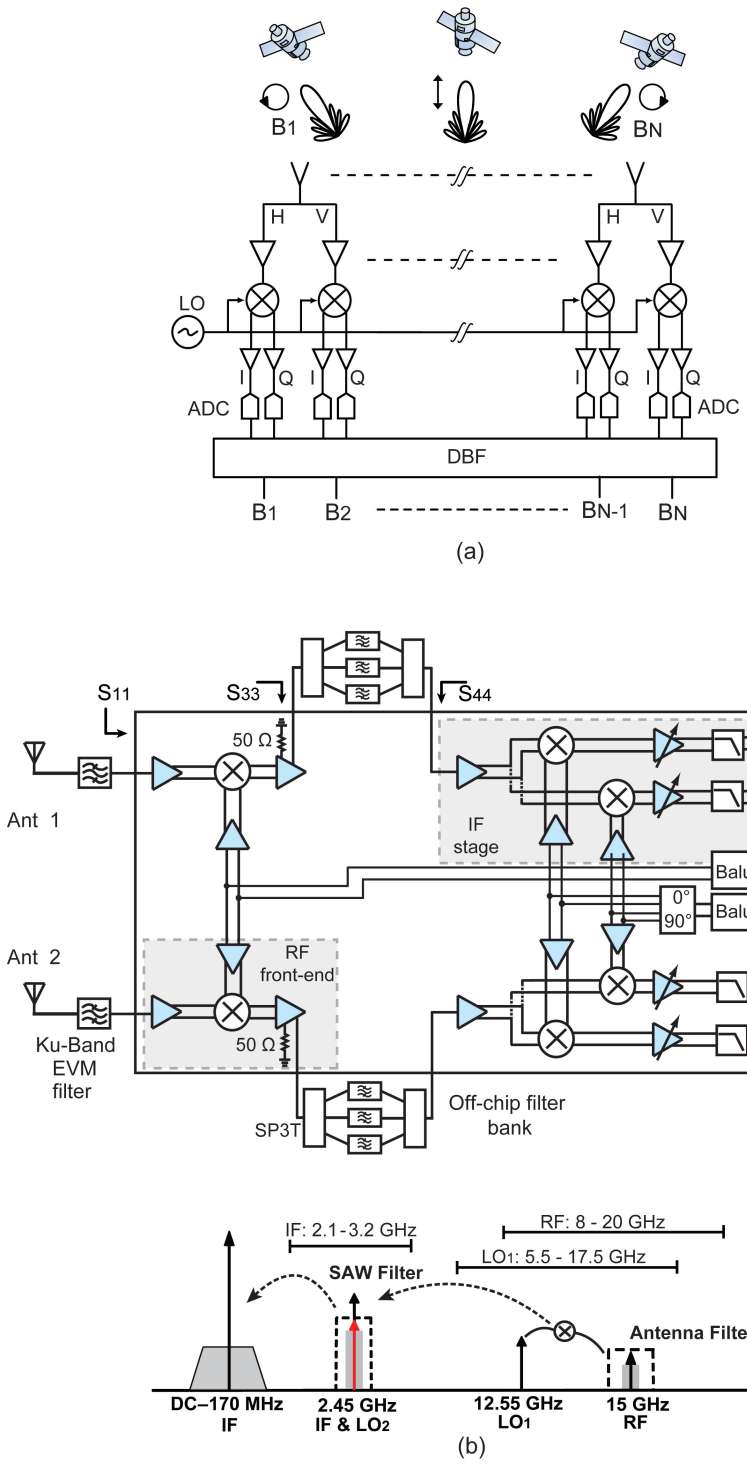



**Figure 2.1**: (a) Digital beam-forming system, (b) block diagram of the two channel receiver based on a dual-down-conversion architecture and frequency plan.

bit-error-rate is 12-14 dB at the aperture level. However at the element level, the S/N ratio is $< 0$ dB (for 16-32 elements and larger), and the number of bits in the baseband A/D converter is not limited by the S/N ratio but by the interference levels. Therefore, in order to use a low number of A/D bits and to reduce the computational complexity in the DBF, it is essential to employ a large degree of filtering at the element level. In this case, a narrow-band low-loss evanescent-mode (EVM) band-pass filter is placed at each antenna element [45, 46], and a dual down-conversion architecture with a high degree of IF filtering is required (Fig. 2.1b). Also, due to the very large interferers present on complex platforms, and which can change in frequency and time, a variable IF architecture should be used, and the system can select the most optimal LO frequencies and IF bands so as to minimize the interference levels at baseband frequencies. The phased array system can then employ 2-4 bit A/D converters at each element (depending on the residual interference levels), which greatly reduces the DBF complexity and power consumption. In most cases, the communication data rate is 0.1-10 Mbps, and a DBF connected to a 16-64 element array can synthesize 2-4 simultaneous beams using standard signal processing chips (FPGAs) [47].

The digital beam-former architecture has seen limited use due to the cost, size and power consumption of GaAs-based X and Ku-band down-converters. This chapter presents the first BiCMOS 8-20 GHz dual down-conversion chip with two independent channels, each with differential I/Q outputs (Fig. 2.1b). The chip can operate at a single frequency anywhere in the 8-20 GHz band. The operation of one channel is as follows (Fig. 2.1b): After the first down-conversion, the signal is filtered again using an off-chip filter bank. These filters are typically SAW devices with 4-6 poles, sharp rejection skirts and ultimate rejection of 50-60 dB [48]. The signal is then fed back to the chip for a second down-conversion which creates the I/Q outputs. A baseband VGA is placed before the I/Q outputs for linearity control as well as providing low-pass filtering with a cut-off frequency of 150-200 MHz at maximum gain. The I and Q outputs are then differentially fed into off-chip A/D converters for beamforming.

The LO inputs are single-ended and fed directly into passive baluns for differential on-chip distribution, and the two receiver channels share common LO busses. Both LOs are external due to stringent 1/f noise requirements for satellite communication systems (typically achieved with DROs at 8-18 GHz) [49]. Due to the low RF power per element and the sharp EVM RF filter on each antenna, the system can tolerate a low input P1dB, and a P1dB of -30 dBm per element for RF-front-end (LNA + mixer) is standard. The system-level P1dB can be as low as -60 dBm per element due to the additional filtering in the IF and baseband, and is mostly limited by the chip gain and the output P1dB of the baseband amplifiers.

## 2.2 Chip Design and Circuit Blocks

### 2.2.1 RF-Front-End Design

The chip is composed of an RF-front-end and an IF stage. The RF front-end is designed using 0.18-$\mu$m SiGe transistors with $f_t$=150 GHz for low noise figure (Jazz SBC18HX). The first stage is a cascode low-noise amplifier (LNA) with inductive degeneration and a tuned load providing simultaneous input and noise matching [11, 50] (Fig 2.2a). The second stage is an active single-to-differential converter with a differential cascode pair and a tuned load. A double-balanced mixer with a tuned load at 2.45 GHz is then used in order to prevent LO-IF feed-through (Fig. 2.2b). The mixer is followed by a differential CMOS buffer in order to isolate the mixer load from the external SAW filter and to ensure stability (the SAW filter impedance

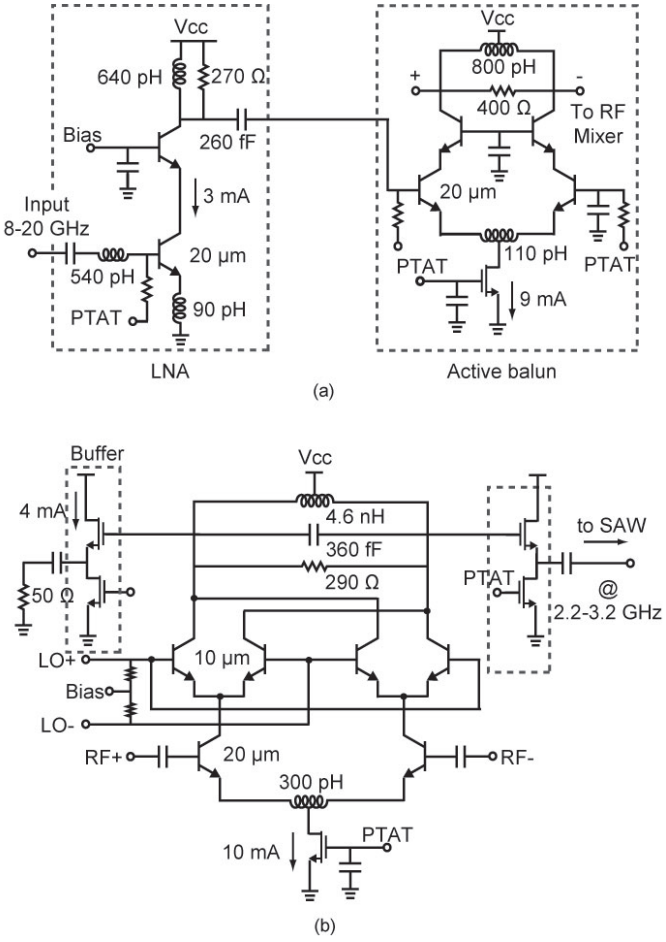



**Figure 2.2**: Circuit schematics of the RF-front end: (a) LNA and active balun, and (b) double-balanced mixer with a tuned load.

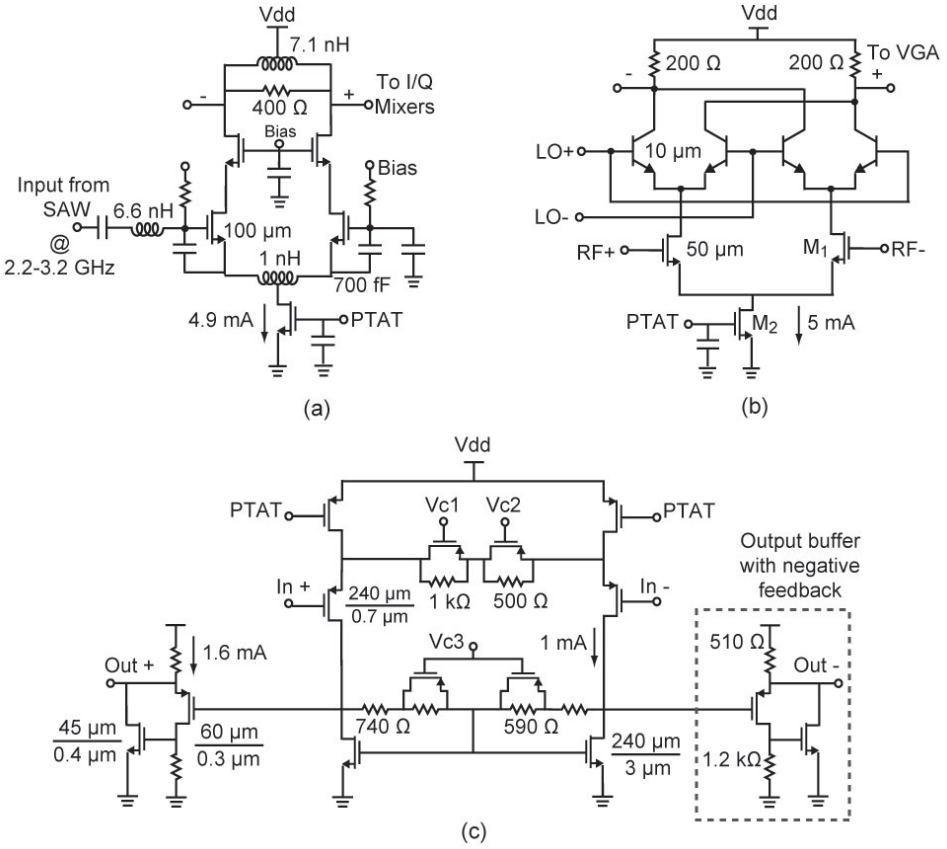



**Figure 2.3**: Circuit schematics of the IF stage: (a) Active balun, (b) resistive double-balanced mixer, and (c) baseband VGA with 9, 12 and 16 dB gain control.

is reactive for all rejection frequencies). The buffer is a CMOS source follower due to linearity considerations. In order to have a single-ended output for IF filtering, one of the mixer/buffer outputs is internally loaded with 50 Ω, while the other output is connected to the external filter bank. The RF front-end has a simulated gain of 25.0 dB at 15 GHz, with an input P1dB of -29.4 dBm, and a NF of 3.1 dB. The total current consumption is 37.7 mA from a 3 V power supply (including LO buffers).

### 2.2.2 IF-Stage Design

A CMOS active balun amplifier in a cascode configuration is used first in the IF stage (Fig 2.3a). In order to achieve wideband input matching and low noise figure at 2-3 GHz with a reasonable amount of current ($I_{\rm dc}$= 10 mA for the active balun), additional capacitance is employed between the gate and source of the CMOS transistors in the active balun [51, 52]. The differential signal at the output of the active balun is then fed to the I/Q mixers. Again, double-

balanced mixers are used for down-conversion to baseband frequencies. The I/Q mixers employ SiGe transistors in the switching core for lower 1/f noise and are resistively loaded for wideband operation (Fig. 2.3b). Fig. 2.4 presents the simulated noise figure of the IF stage and of the whole single-channel down-converter using MOSFET and bipolar switching cores. As seen, the 1/f noise corner frequency of single channel is reduced to 20 kHz using bipolar switching cores.

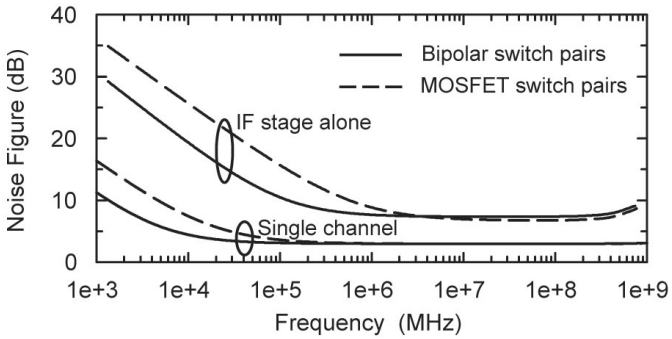



**Figure 2.4**: Noise figure comparison showing the effect of using bipolar (10$\mu$m/0.18$\mu$m) or MOSFET (25$\mu$m/0.18$\mu$m) switch pairs in the IF stage mixer core.

The I/Q mixers are followed by DC-coupled differential common-source variable gain amplifiers (VGA) and the gain is controlled by resistive degeneration using $V_{c1}$, $V_{c2}$ and $V_{c3}$ (Fig. 2.3c). The VGA's are designed using PMOS transistors with a large device length and optimized for lowest 1/f noise performance. The VGA is followed by a differential source follower with a negative feedback which sets the output impedance of the VGA to 100 $\Omega$ differential in order to drive high-speed off-chip A/D converters [53]. The IF stage has a simulated gain of 25.5 dB, with a simulated bandwidth of 200 MHz, an input P1dB of -34.5 dBm (output P1dB of -10 dBm in a 50 $\Omega$ load, single ended), and a noise figure of 7.2 dB at an input of 2.45 GHz, and consumes 31.2 mA from a 3 V power supply (including two $LO_2$ buffers).

### 2.2.3 LO Distribution Network

One of the key aspects of the design is the wideband on-chip LO distribution network for both $LO_1$ (5.5-17.5 GHz) and $LO_2$ (2.2-3.2 GHz). Two separate single-ended LO signals are fed into passive baluns and then routed differentially through the LO distribution network located in the middle of the chip (Fig 2.5 and Fig. 2.8). The $LO_1$ balun is two-layer design with primary turn implemented using M6 and the secondary turn implemented using M5. Both primary and secondary inductors are 3 turns with a metal width of 4 $\mu$m and a spacing of 3 $mu$m. The balun

results in 1.6 dB loss at 12.5 GHz [54]. The $LO_2$ balun is a single-layer standard library design with 2 dB loss at 2.5 GHz [55]. The LO signals for the I/Q mixers are generated using a one-stage differential R-C polyphase filter which provides a constant 90° phase versus frequency. The LO distribution is done using GSSG transmission lines (simulated loss using Sonnet: 0.62 dB/mm at 12.5 GHz), and the crossovers between $LO_1$, $LO_2$ and the I/Q paths are realized using ground islands between the signals for enhanced isolation (Fig. 2.5b).

The LO division between the two channels is done using T-junctions followed by differential amplifiers so as to enable operation at low LO powers. These LO drivers have a gain of 6 dB at 12.5 GHz, and 9 dB at 2.5 GHz (when loaded with the corresponding mixers), and are driven into saturation. The RF and IF mixers require $>$ -17 dBm ($\sim$200 $mV_{p-p}$) at the LO switching cores for a saturated gain, and this can be easily achieved with 5 mA drivers. The

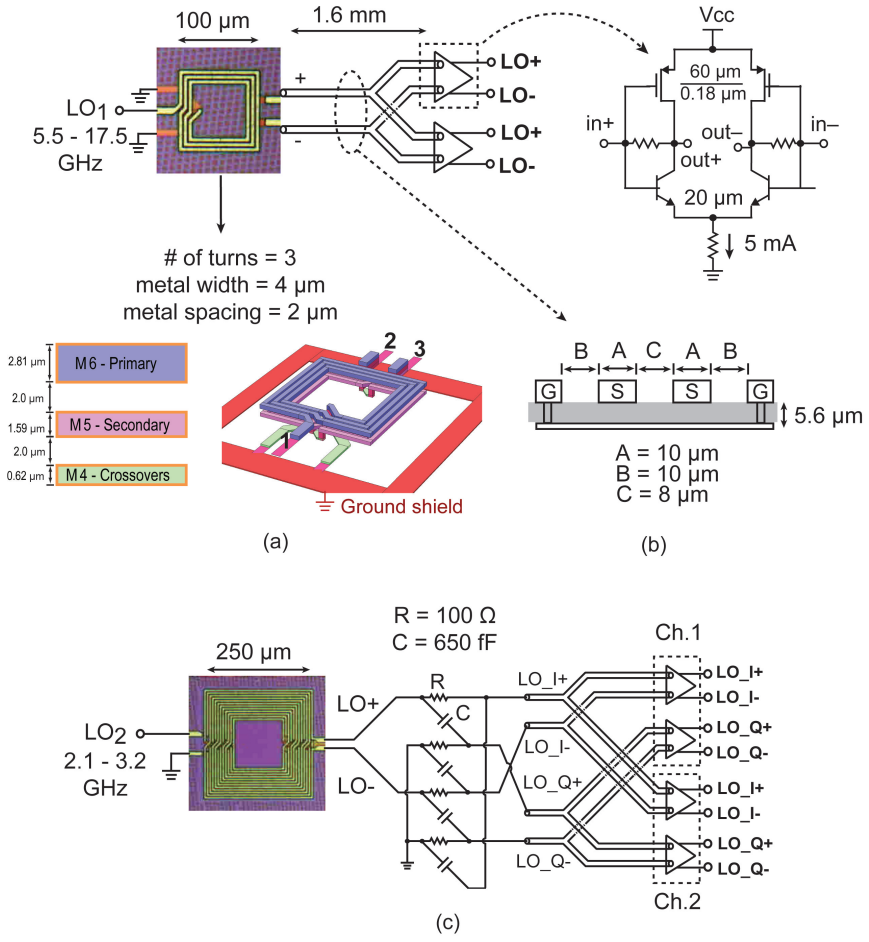



**Figure 2.5**: LO distribution networks: (a) $LO_1$ at 5.5-17.5 GHz, (b) differential LO driver, and (c) $LO_2$ at 2.1-3.2 GHz.

total distribution loss for $LO_1$ is 5.6 dB at 12.5 GHz including the 1:2 division, and is 11.0 dB for $LO_2$ including the polyphase network and 1:2 division. Therefore, for proper operation, an input LO power of $>$ -10 dBm is required for both $LO_1$ and $LO_2$. This means that an off-chip low phase-noise dielectric resonator oscillator (DRO) with an output power of 20 dBm can drive multiple elements without any additional LO distribution amplifiers.

The simulated LO differential phase errors at the input of RF ($LO_1$) and IF ($LO_2$) mixers are $< 10^\circ$ at 4-18 GHz and $< 5^\circ$ at 2.0-3.3 GHz. Since the RF and IF mixers and the baseband VGA are differential, the phase error at the baseband output port is reduced to $< 0.5^\circ$ over the 200 MHz bandwidth.

### 2.2.4 Biasing Network

Two PTAT circuits are implemented in order to generate reference currents: one for the RF-front-end, one for the IF-stage. The two channels share the reference PTAT blocks (RF and IF), and all amplifiers and mixers are biased from these reference currents. Shown in Fig. 2.6a and Fig. 2.7a are PTAT reference current generators for RF-front-end (100 $\mu$A) and IF-stage (50 $\mu$A), respectively. The PTAT reference current is calculated using:

$$I_{\mathrm{PTAT}} = \frac{\mathrm{kT}}{\mathrm{q}} \frac{\ln \mathrm{A}}{\mathrm{R_p}} \tag{2.1}$$

where $A$ is the ratio of emitter length of $Q_2$ to that of $Q_1$.

In addition to the PTAT current generator, another control path is included ($Vs$, $\overline{Vs}$) which can turn off the PTAT generator, and allows for external current control ($Vc$). PMOS transistors with large lengths (0.5-1 $\mu$m) are used for current mirroring. Furthermore, 1.6-10.1 pF de-coupling capacitors are placed at the bias sampling nodes for de-coupling the RF-stages from bias network effects. Detailed bias network circuits for RF-front-end and IF stages are shown in Fig. 2.6 and Fig. 2.7, respectively.

### 2.2.5 Technology and Chip Performance

The chip is fabricated on a 0.18-$\mu$m SiGe BiCMOS process (Jazz SBC18HX) with 6 metal layers. The 2.8-$\mu$m-thick top metal layer is used to implement inductors, transmission lines, and input/output pads (see Appendix 1 for detailed process parameters). Metal levels 4-5-6 are used to create a single continuous Vcc plane throughout the chip. A single ground plane for RF and DC ground is also employed on the chip (metal layers 1/4/6). All of the passive components and interconnections in the RF-front-end and the LO distribution network

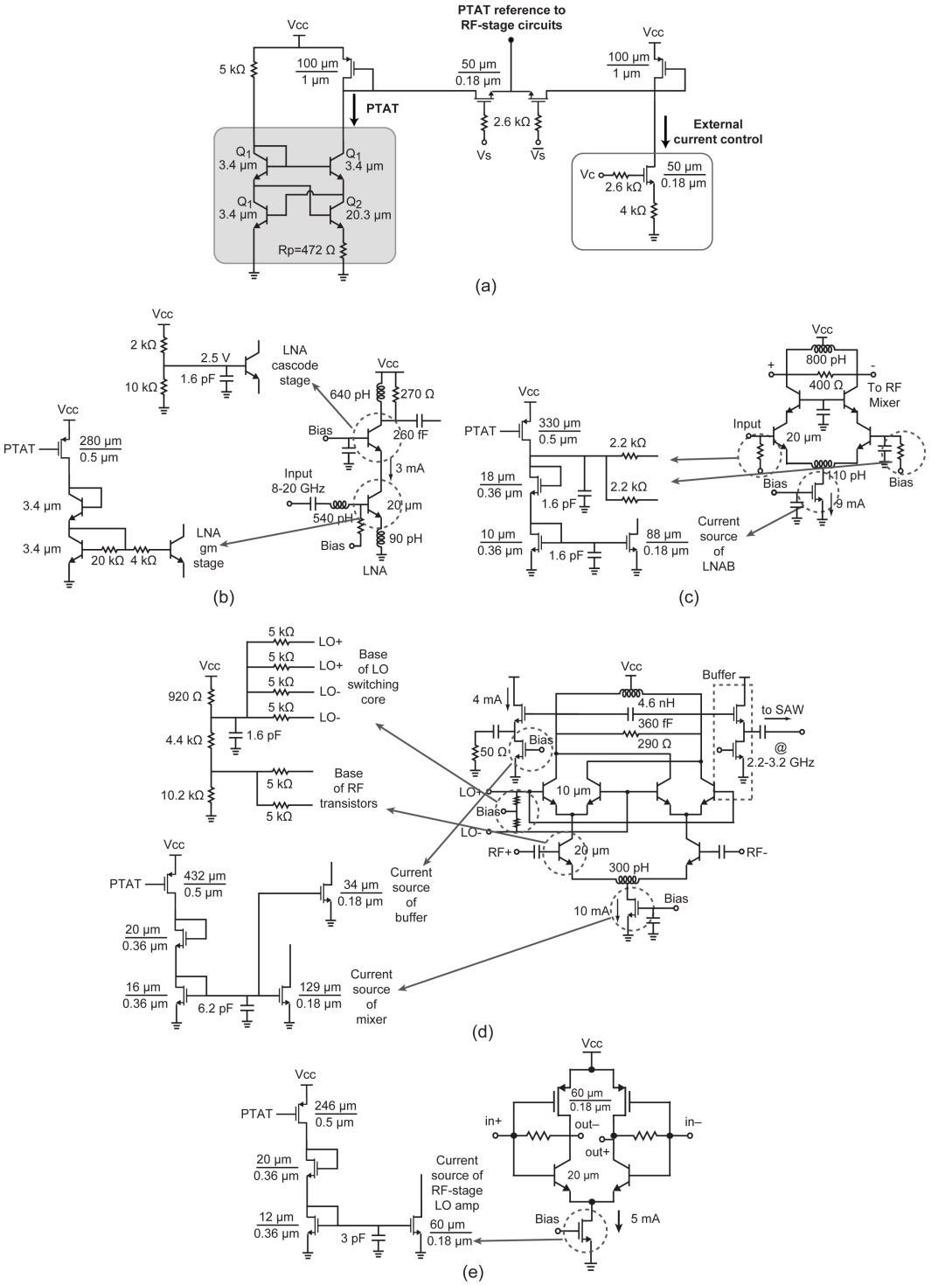



**Figure 2.6**: Bias networks of RF-front-end: (a) PTAT reference current source, (b) LNA, (c) LNAB, (d) DB-Mixer and (e) LO-amplifiers.

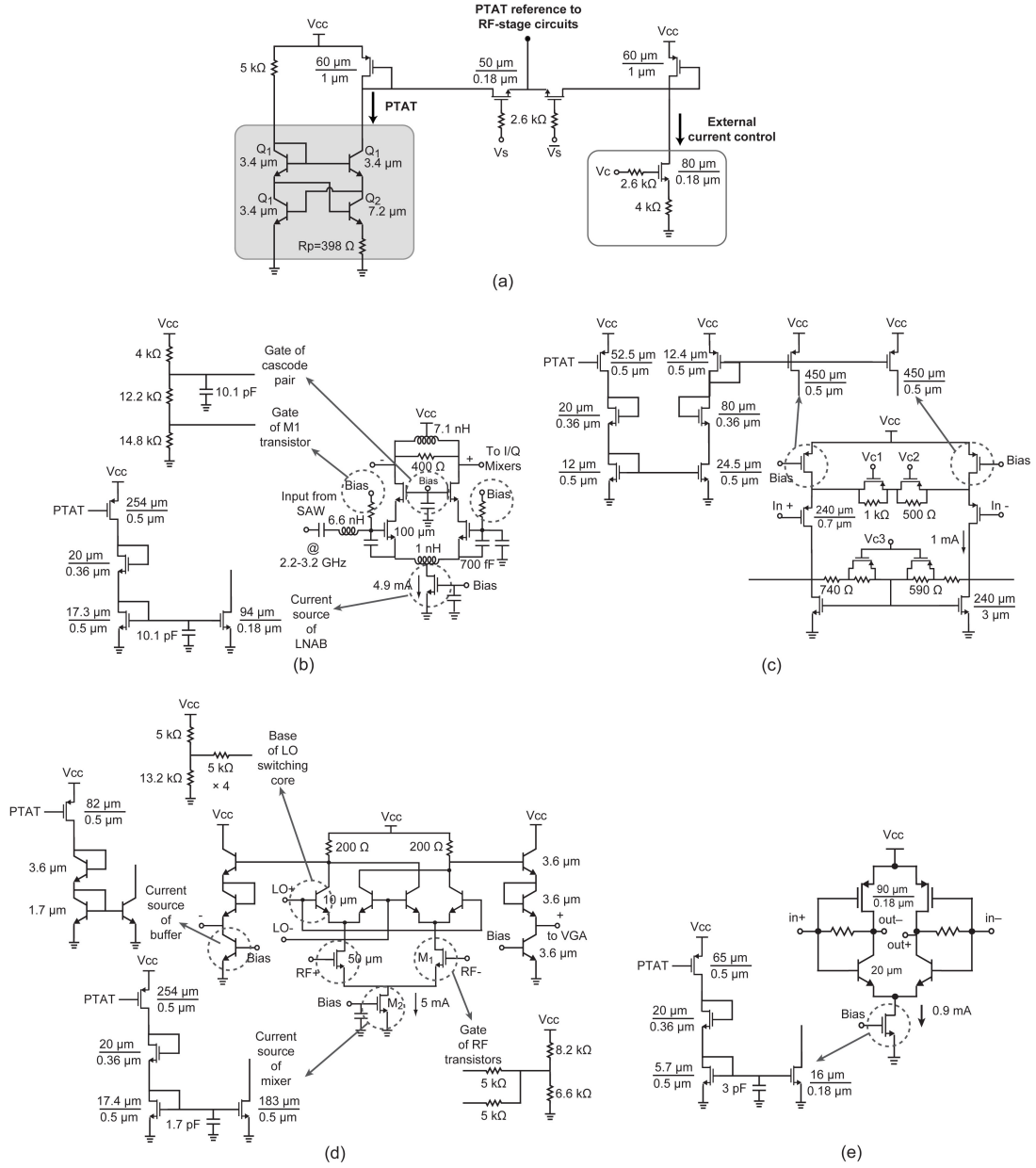



**Figure 2.7**: Bias networks of IF-stage: (a) PTAT reference current source, (b) Active balun, (c) VGA, (d) Mixer and (e) LO-amplifiers.

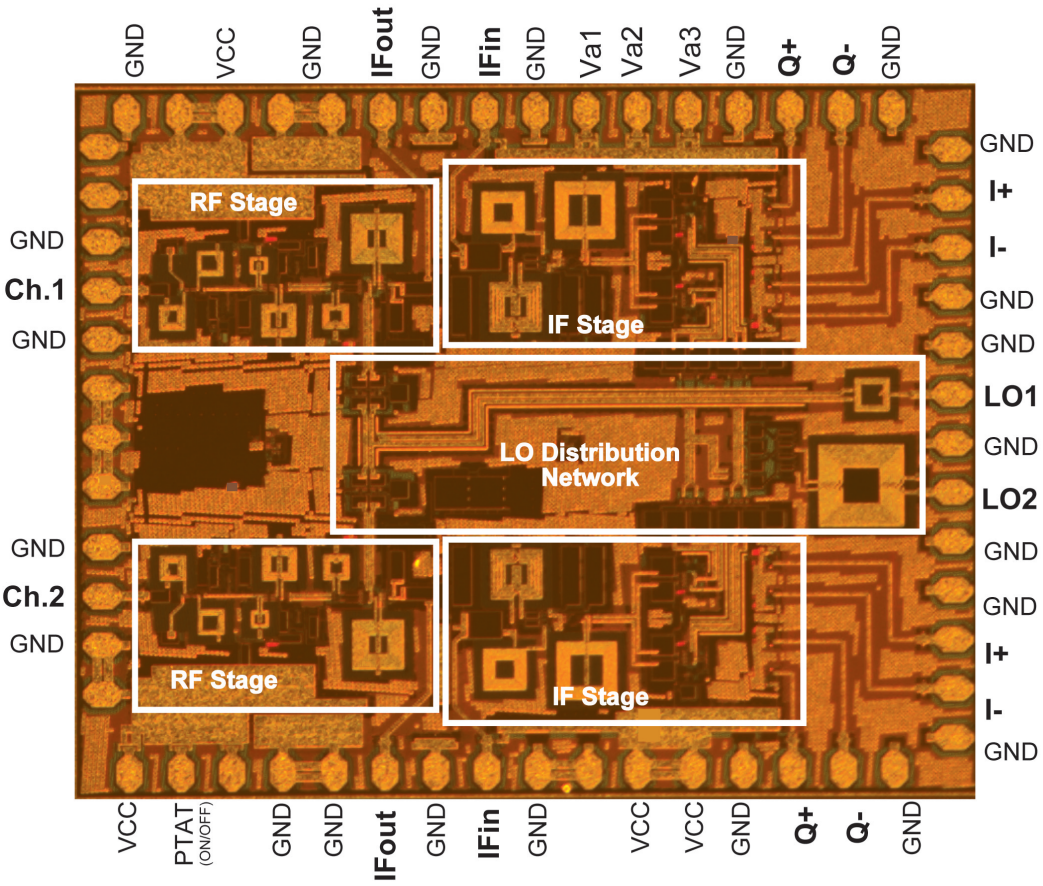
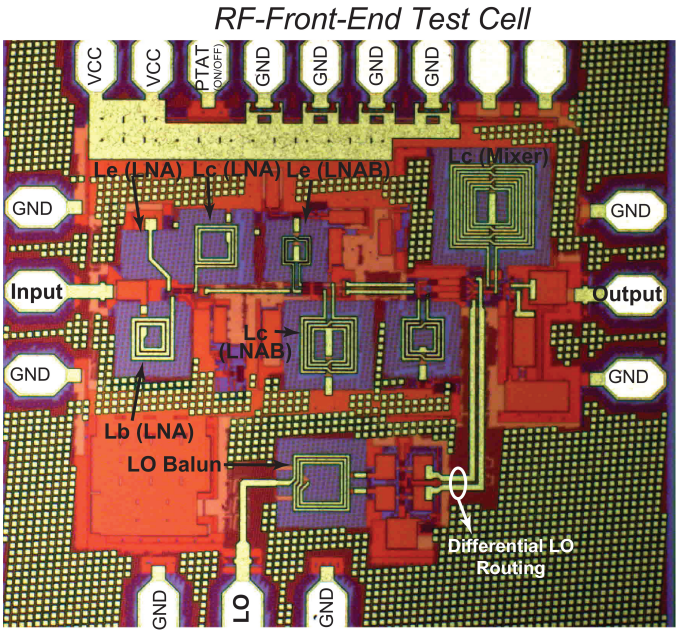
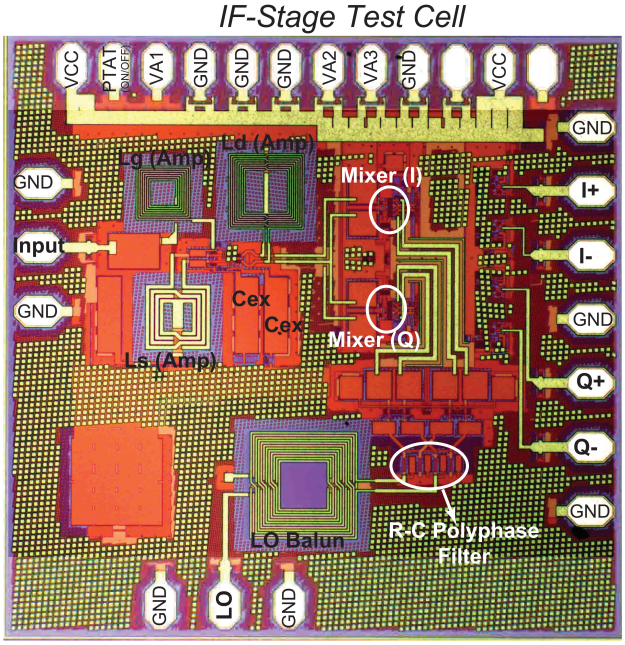



**Figure 2.8**: (a) Microphotograph of the 8-20 GHz two-channel down-converter (2.6×2.2 mm$^2$ including all pads).




(a)




(b)

**Figure 2.9**: Micrograph of the fabricated test cells: (a) RF-front-end ($1.25\times1.10$ mm$^2$ including all pads) (b) IF-stage ($1.40\times1.35$ mm$^2$ including all pads).

are simulated using a full-wave EM analysis software (Sonnet [56]). R-C parasitic extraction simulations are performed for the baseband circuitry. All RF and DC pads are ESD protected using 1.2 kV and 3.6 kV ESD diodes available in the Jazz library. The input and output matching circuits are designed taking into account the pad and ESD capacitance.

Each channel consumes $\sim$ 70 mA of current from 3 V power supply including the LO amplifiers. The simulated overall receiver shows a gain of 49 dB with a 3-dB baseband bandwidth of 200 MHz and a NF of 3.1 dB, all at 15 GHz, and with a very wideband performance (see Section 2.3). A microphotograph of the two-channel receiver (2.6$\times$2.2 mm$^2$) is presented in Fig. 2.8. Test-cells of RF-front-end and IF-stage are also fabricated for measurement purposes and are shown in Fig. 2.9a and b, respectively.

## 2.3 On-Chip Measurements

### 2.3.1 S-Parameter Measurements

The on-chip measurements are done using SOLT calibration to the probe tip and dedicated RF and DC probes. All measurements include the RF pad capacitance and the ESD diode loading effects. The measured input reflection coefficient ($S_{11}$) is shown in Fig. 2.10a. An excellent impedance match is achieved at 10-25 GHz, and the difference between the simulation and measurements is attributed to extra parasitics at the RF pad, which de-Q the reflection characteristics. The measured reflection coefficient at the I and Q outputs ($S_{22}$) are given in Fig. 2.10b, showing a good impedance match up to 1 GHz. Fig. 2.10c presents the measured reflection coefficients at the output of the RF stage ($S_{33}$) and at the input of the IF stage ($S_{44}$) agreeing well with simulations.

### 2.3.2 RF-Front-End Measurements

The RF and IF stages of the dual down-converter chip can be measured separately due to the IF filtering cut-out. The RF test cell (Fig. 2.9a) is characterized using CPW probes, Agilent network analyzers, signal sources (LO), and spectrum analyzers (NF measurements). Fig. 2.11a shows the gain and noise figure of the RF stage with a fixed IF output at 2.45 GHz (RF and $LO_1$ are scanned together). The measured gain is 23.5 dB at 15.0 GHz, with a 3-dB gain bandwidth of 9.2-16.2 GHz, and a NF of $<$ 3.7 dB at 8-20 GHz. The RF stage is also characterized with a fixed LO ($LO_1$= 12.55 GHz), and shows a gain and noise figure of 23.5 dB and 3.2 dB at 15 GHz, respectively (Fig. 2.11b). The input LNA and active balun designs are

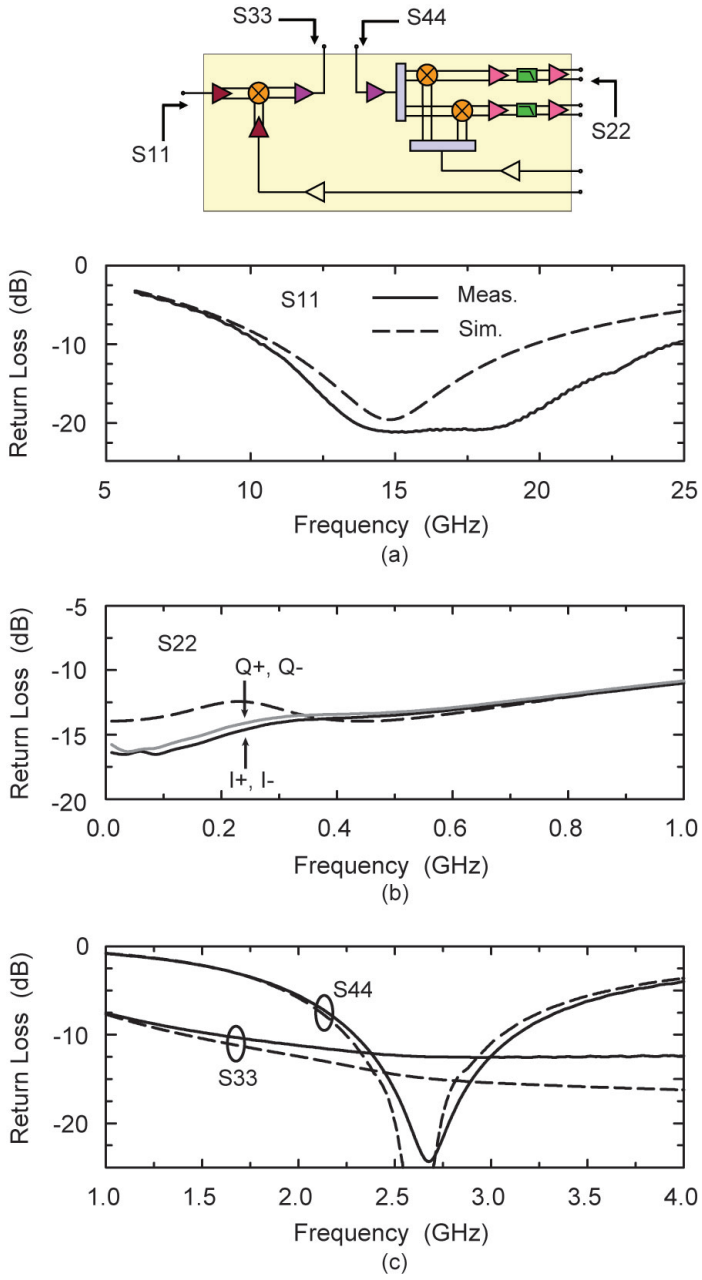



**Figure 2.10**: Measured return losses: (a) RF input ($S_{11}$), (b) baseband output ($S_{22}$), (c) IF output ($S_{33}$) and input ($S_{44}$).

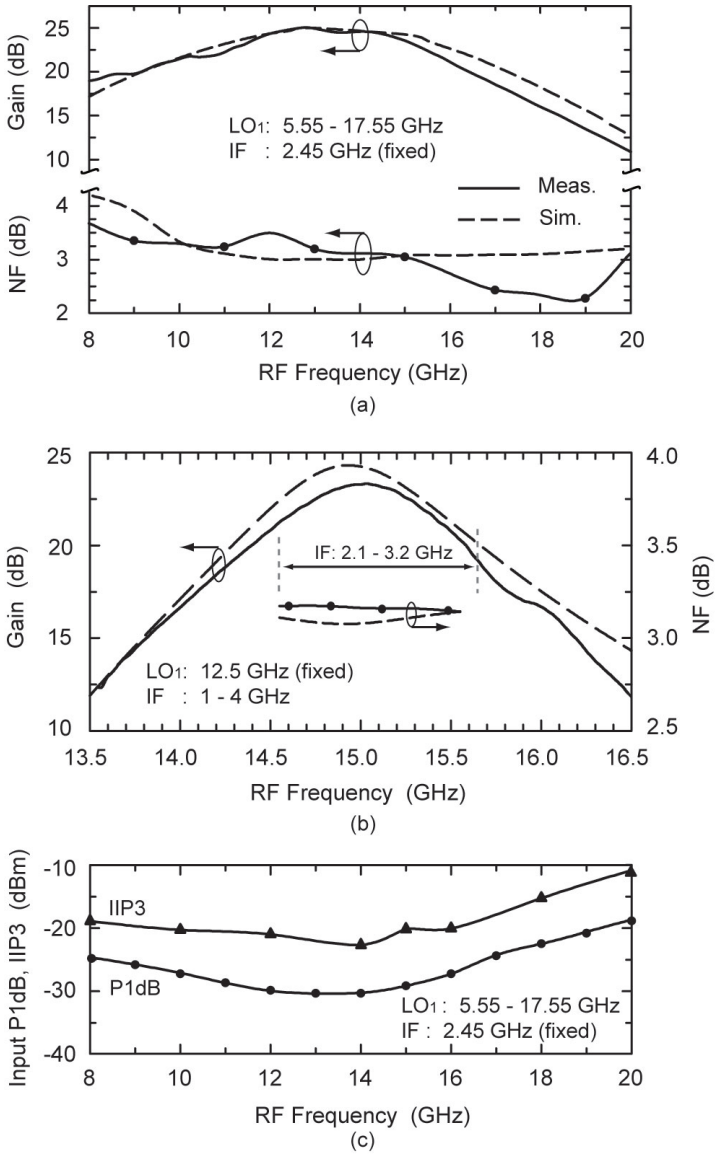



**Figure 2.11**: Measured gain and NF of the RF stage: (a) with fixed IF output at 2.45 GHz, (b) at 15 GHz vs. different IF. (c) Measured input P1dB and IIP3 with IF fixed at 2.45 GHz.

wideband and the gain curve is mainly shaped by the tuned IF response of the double-balanced mixer. The measured input P1dB and IIP3 are shown in Fig. 2.11c and are limited by the RF mixer.

### 2.3.3 IF-Stage Measurements

The IF stage is also separately measured with an input at 1.5-3.5 GHz using a test cell (Fig. 2.9b). For a fixed baseband frequency of 10 MHz, the measured gain and noise figure are shown in Fig. 2.12a. The gain is 20.5-24.5 dB and the NF is $<$ 11.5 dB at 2.1-3.2 GHz. The gain of the IF stage with an $LO_2$ of 2.45 GHz is shown in Fig. 2.12b for all the baseband outputs: I+, I-, Q+ and Q-. Note that the spikes around 100 MHz are due to the coupling of the FM radio stations to the test setup. The measured 3-dB bandwidth is 175 MHz with a gain of 24.5 dB, and is determined mostly by the baseband VGA. The measured P1dB is shown in Fig. 2.12c and is $\sim$ -35 dBm at 2.5 GHz, limited by the baseband VGA. Furthermore, the $LO_2$ power leakage at the baseband outputs is -53 dBm at 2.45 GHz for an input LO power of -5 dBm.

### 2.3.4 Channel Measurements

In order to fully characterize the on-chip channel response, the IF filters are replaced by short-circuit connections for both channels (in Fig. 2.8, IFout and IFin are shorted on the probe). The input RF frequency and $LO_1$ can be scanned together to tune the receiver to different RF frequencies without changing the IF. For a fixed IF of 2.45 GHz, the measured peak gain is $>$ 36 dB at 8-20 GHz ($\sim$47 dB at 11-15 GHz) with a NF of $<$ 4.1 dB at 8-20 GHz (Fig. 2.13a). The NF dip at 17-19 GHz was observed in three different chips and is believed to be due to the measurement setup. Another test is to fix the RF signal and change $LO_1$ and $LO_2$ so as to obtain different IF frequencies (Fig. 2.13b). This is required for interference mitigations. The results show that the overall gain is 47.6-42.6 dB for an RF at 15.01 GHz and IF from 2.0 to 3.0 GHz. The corresponding NF is $<$ 3.5 dB. The measured input P1dB and IIP3 of a single channel at 8-20 GHz with a fixed $LO_2$ are shown in Fig. 2.13c. The input P1dB is limited by the baseband amplifiers and is -40 dBm for the minimum gain setting (31 dB) at 15 GHz.

Fig. 2.14a presents the single channel receiver gain for all four I and Q outputs (each measured independently with other ports terminated by 50 $\Omega$) for an RF signal at 15-16 GHz. The measured gain is 47.0 dB with a 3-dB bandwidth of 150 MHz and shows identical results for all outputs (I+, I-, Q+, Q-). The baseband VGA has 9, 12 and 16 dB variable attenuation levels and the overall channel gain can be reduced to 31 dB with a 3-dB bandwidth of 380 MHz.

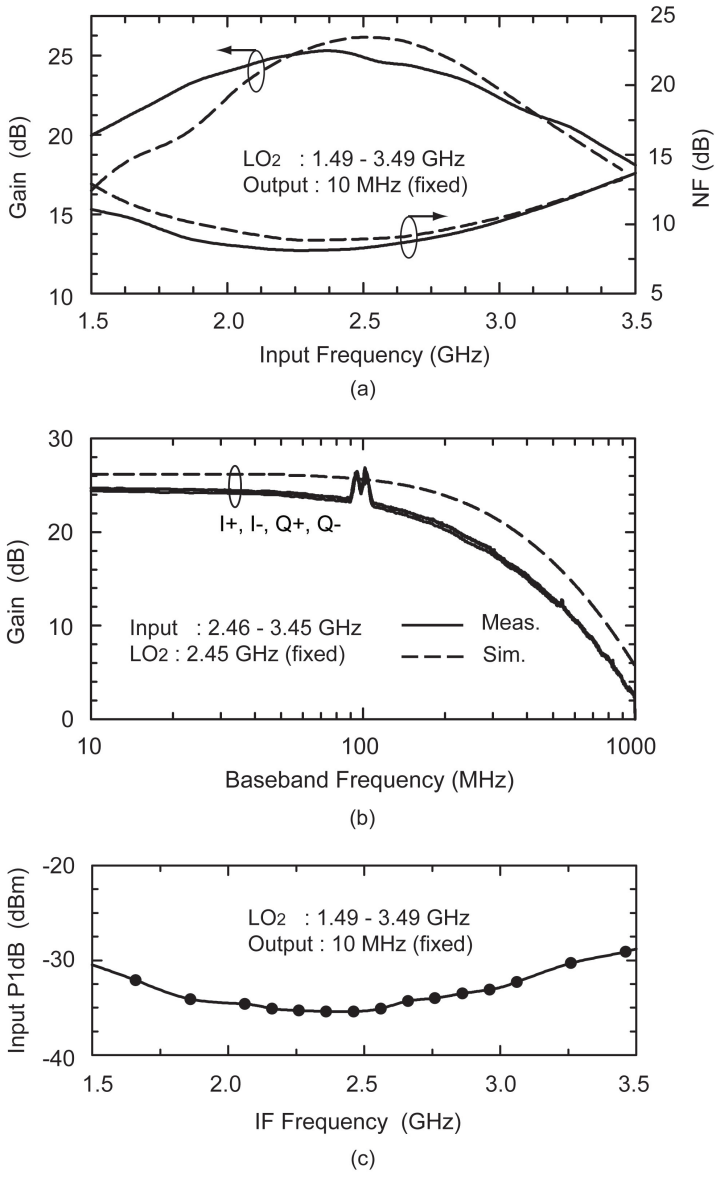



**Figure 2.12**: (a) Measured gain and NF of the IF stage with fixed baseband output at 10 MHz, (b) measured gain of the IF stage with fixed LO at 2.45 GHz.

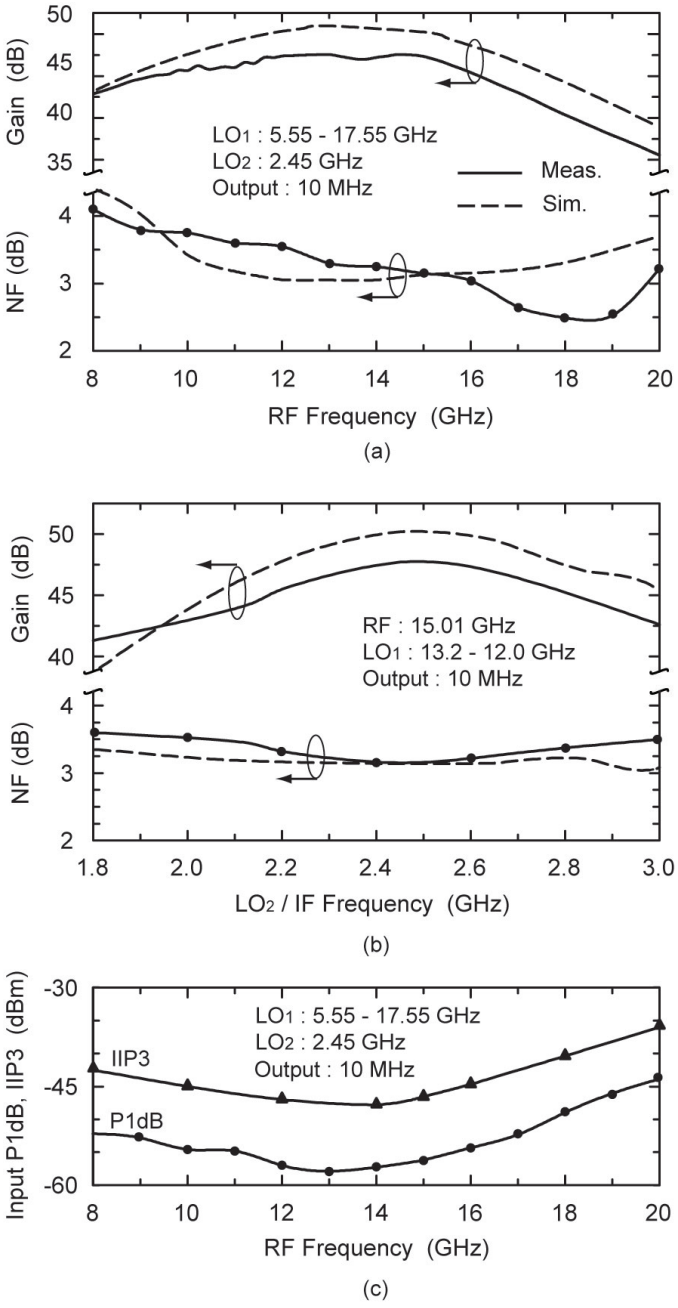



**Figure 2.13**: Measured channel gain and noise figure: (a) with IF fixed at 2.45 GHz, (b) at 15 GHz vs. different IF. (c) Measured input P1dB and IIP3 at maximum gain setting with IF fixed at 2.45 GHz.

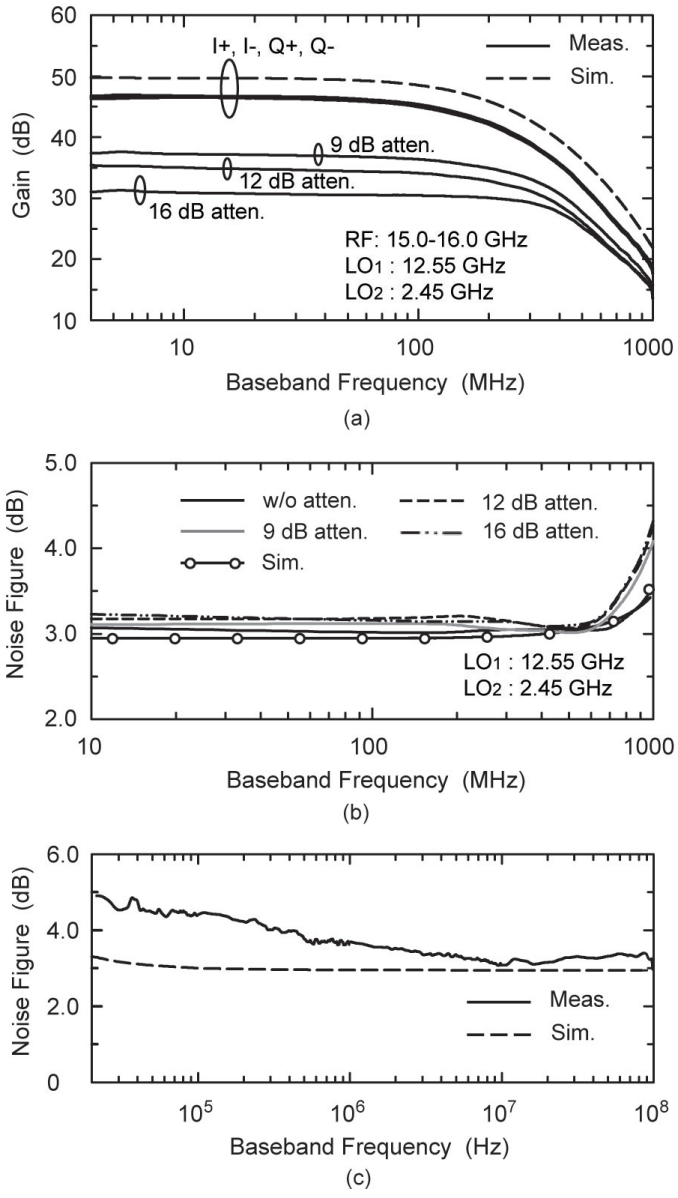



**Figure 2.14**: Measured (a) channel gain, (b) noise figure with $LO_1$ and $LO_2$ fixed at 12.55 GHz and 2.45 GHz, respectively. Gain is shown for different attenuation levels, and (c) noise figure below 100 MHz

The noise figure is 3.1-3.2 dB at 15-16 GHz and is not affected by the gain control (Fig. 2.14b). The effect of the LO power on system-level gain is also measured and the gain is flat for LO1 and LO2 power levels $>$ -10 dBm, as predicted by the simulations (Fig. 2.15).

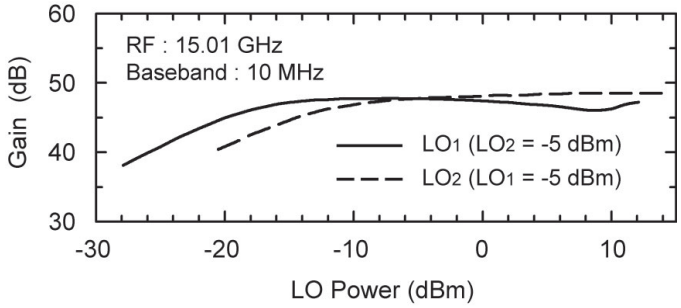



**Figure 2.15**: Measured channel gain versus LO power with $LO_1$ and $LO_2$ fixed at 12.55 and 2.45 GHz, respectively.

The two channels of the down-converter chip are identical to each other (gain, NF, P1dB, etc.), and the on-chip coupling between the channels was measured by injecting RF power to channel 1 and measuring the power at the I/Q outputs of channel 1 and 2. The input RF port of channel 2 was left open circuited (worst case condition), with the standard test conditions (RF=15.01 GHz, $LO_1$=12.5 GHz, $LO_2$=2.5 GHz, output=10 MHz). A coupling of $\sim$-48 dB was measured at the output of channel 2 with respect to the output level of channel 1, which is insignificant and does not distort the patterns.

The I/Q gain and phase imbalance and EVM measurements were also performed for the receiver using Agilent synthesizers E8267C (15.0 GHz), 83650B (12.5 GHz), E8257D (2.5 GHz) and Agilent Infinium DSO80654B oscilloscope with VSA 89600 software. These sources have $<$ -120 dBc/Hz phase-noise at 1 MHz offset from the carrier, and therefore have negligible effect on the output noise level. Fig. 2.16a-b presents the constellation and output spectrum for a 1 Msps QPSK modulation at 15 GHz. The receiver also resulted in $< 0.3^\circ$ and $<$ 0.1 dB I/Q phase and gain imbalance at an RF of 8-20 GHz, and also for the 2.1-3.2 GHz IF band (RF=15 GHz, $LO_1$ and $LO_2$ varying), all done under a 1 Msps QPSK modulation (Fig 2.16c-d).

The I/Q gain and phase imbalance are very low, and hence the EVM of the system is dominated by the signal-to-noise-ratio (SNR) at the output, which can be calculated using [57]:

$$EVM \approx \frac{1}{\sqrt{SNR}} \tag{2.2}$$

The EVM measurements are therefore done at the minimum gain state, which maximizes the output SNR since the NF of the system is not affected by the attenuation level (gain is reduced

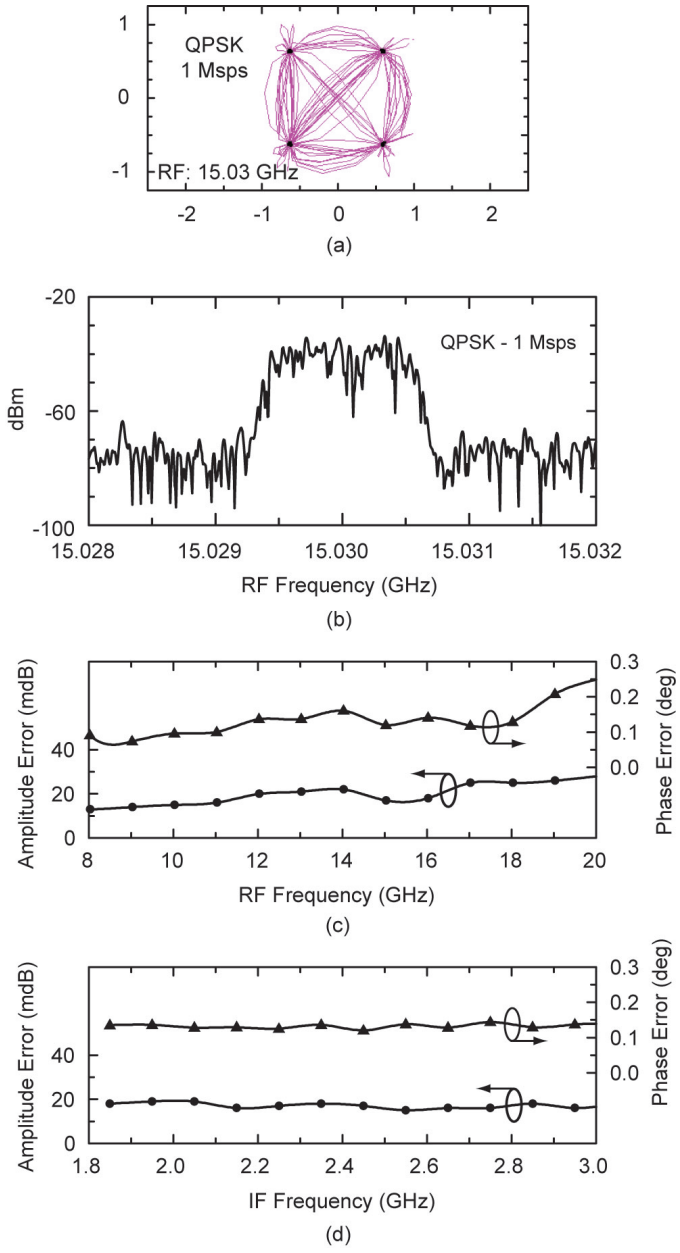



**Figure 2.16**: Performance of single-channel with 1 Msps QPSK modulation: (a) Constellation diagram, (b) Spectrum of the output signal, and I/Q gain and phase error (c) for IF fixed at 2.5 GHz, and (d) for RF fixed at 15.03 GHz.

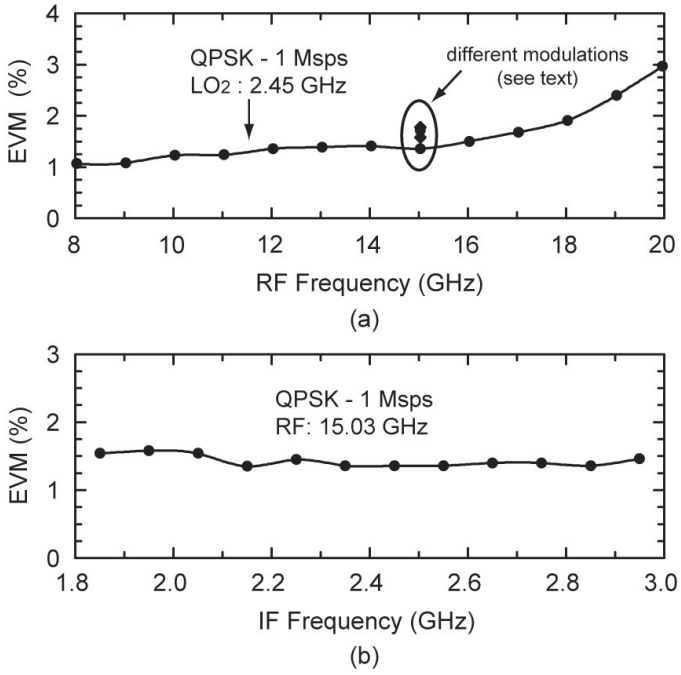



**Figure 2.17**: Measured EVM performance of the chip with 1 Msps QPSK modulation with (a) fixed IF at 2.45 GHz and (b) fixed RF input at 15.03 GHz.

by 16 dB while the bandwidth increases from 150 MHz to 380 MHz). The simulated SNR at the output of one channel is 37 dB with a gain of 31 dB, an input power of -45 dBm, a NF of 3 dB and an output baseband bandwidth of 380 MHz, and this results in an EVM of $\sim$1.4%.

The measured EVM is $<$ 1.35% for 1 Msps QPSK modulation at 15 GHz agreeing well with simulations. The measured EVM is also $<$ 3% for 8-20 GHz RF signals with 1 Msps QPSK modulation, and $<$ 1.6% for the 2.1-3.2 GHz IF band (RF at 15 GHz, $LO_1$ and $LO_2$ varying) (Fig. 2.17). Another EVM test was done at 15-16 GHz with an IF of 2.5 GHz using 0.5, 1 and 10 Msps QPSK, 16QAM and 64QAM modulations, and resulted in $<$ 1.8% EVM for all modulations (Fig. 2.17a). For the maximum gain state with a baseband bandwidth of 150 MHz, the output SNR is $\sim$27 dB and results in an EVM of 4.4%. Therefore, for low-level signals and maximum gain settings, the baseband bandwidth should be reduced off-chip to 20-30 MHz for best EVM performance.

### 2.3.5 Temperature Measurements

The two-channel chip is characterized from -40°C to 100°C and results in a channel gain of 42-47 dB and a NF of $<$ 5 dB over the whole temperature range (Fig 2.18). In this

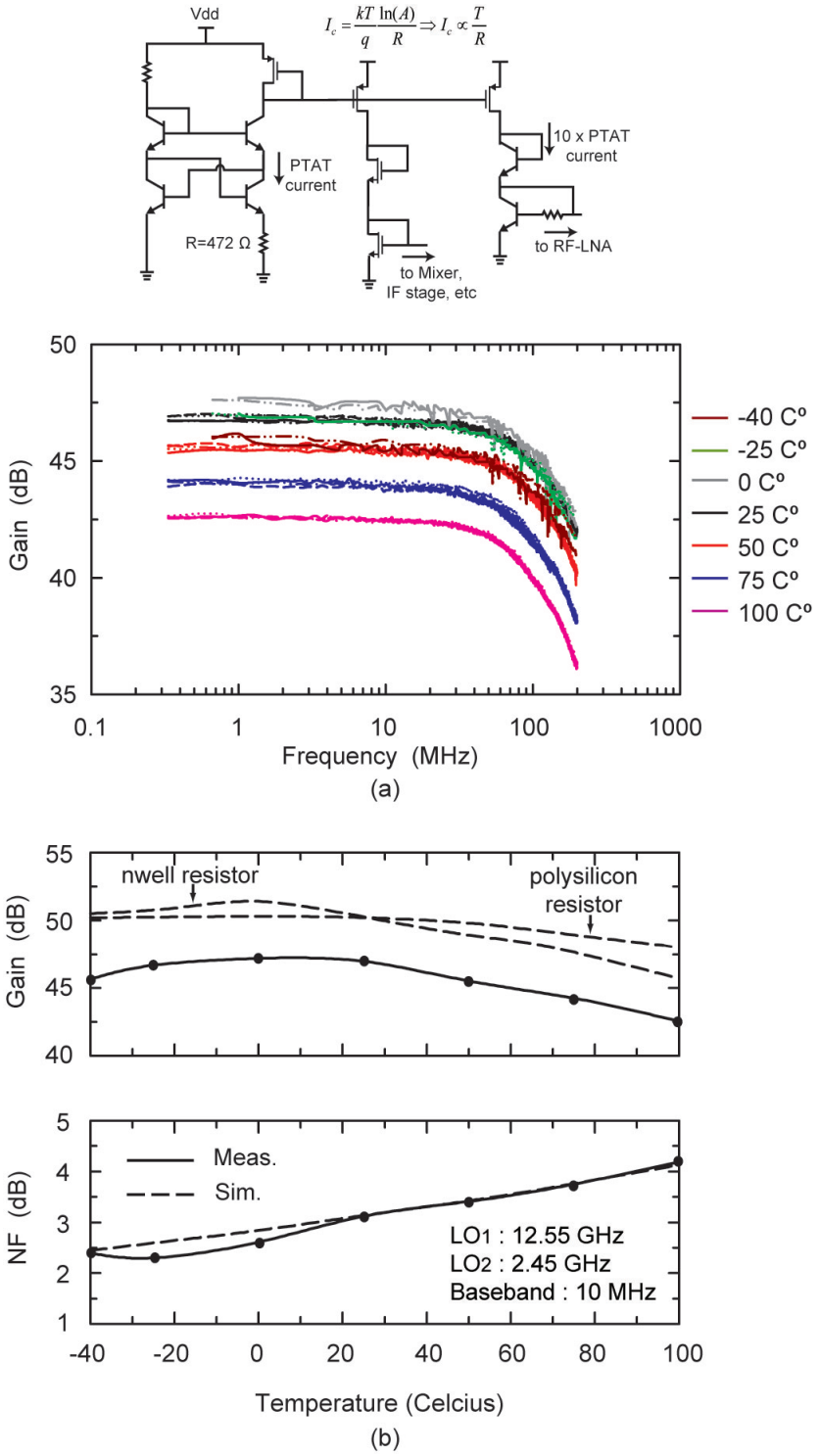



**Figure 2.18**: Measured channel gain and NF vs. temperature from -40°C to 100°C.

**Table 2.1**: Single-Channel Performance Summary (On-Chip)

| | | |
|---|---|---|
| **Gain** | 42-47 dB @ 8-20 GHz | |
| **Input Return Loss** | $<$ -10 dB @ 8-25 GHz | |
| **Output Return Loss** | $<$ -11 dB @ 0-1 GHz | |
| **NF** | 3-4 dB @ 8-20 GHz, IF=1.5-3.5 GHz | |
| **Gain Control** | 0-9-12-16 dB | |
| **Baseband 3-dB Bandwidth** | 150 MHz @ max. gain<br>380 MHz @ min. gain | |
| **IF Band** | 2.2 - 3.2 GHz | |
| **Input P1dB** | -58 to -45 dBm @ 8-20 GHz | |
| **IIP3** | -47 to -35 dBm @ 8-20 GHz | |
| **I/Q gain / phase imbalance** | $<$ 0.1 dB / $<$ 0.3° | |
| **EVM @ 8-20 GHz** | QPSK 1Msps | $<$ 3 % |
| **EVM @ 15 GHz (%)** | QPSK 1 Msps / 10 Msps | 1.4 / 1.7 |
| | 16QAM 1 Msps / 10 Msps | 1.6 / 1.8 |
| | 64QAM 1 Msps / 10 Msps | 1.6 / 1.8 |
| **Channel-to-channel Coupling** | $<$ -48 dB | |
| **Vcc** | 3 V | |
| **Power Consumption** | 210 mW / channel | |

design, PTAT circuits are implemented for both RF-front-end and IF stages which ideally have currents proportional to the temperature (Idc $\propto$ kT/R, where R is the resistance). However, N-well resistors were used which have a resistance proportional to temperature, and hence resulted in a current reduction at high temperatures. For future designs, polysilicon resistors with a constant resistance versus temperature will be used for improved gain with temperature.

The on-chip measurement results are summarized in Table 2.1.

## 2.4 8-Element Ku-Band DBF Phased-Array Receiver

### 2.4.1 Board Design

A 15 GHz printed circuit board is designed in order to combine 8 antenna elements (4 two-channel chips) for digital beamforming applications, and is measured using the setup shown in Fig. 2.19. The design is based on a Teflon board with $\epsilon_{\rm r}= 2.2$ and h=10 mils (Rogers RO5880) (Fig. 2.20). Routings for RF signals and the LO distribution network are performed using grounded CPW lines to insure high isolation, and shorted $\lambda$/4 stubs are placed on the RF lines for additional ESD protection. The differential I/Q outputs, and gain control lines are routed on the top layer to external DC supplies and an A/D sampling board on the top layer (Fig. 2.20). The DC supply is routed on the back layer using cutouts in the ground plane. This allows placement of 100 nF of bias de-coupling capacitors next to the silicon chip between the DC supply and the ground (Fig. 2.20). A total of 32 baseband output lines are present on the board. Due to the one-layer PCB implementation, the IF bandwidth is limited to 1 MHz which allows baseband extraction using simple unshielded wires. These are fed to $2\times16$-channel 12-bit A/D samplers (50 ksps for 2 channels, 10 ksps for 16 channels), and the digital data is read by a computer. The I/Q signals can also be fed to a 4-channel scope for real-time monitoring.

The silicon chip is placed on a grounded pedestal and is connected to the RF and DC lines using bondwires (Fig. 2.21a). A 3-D EM-simulator (HFSS [58]) is used to simulate the bondwire inductance, and the chip-on-board packaging environment. A CPW matching network is employed at each RF input in order to compensate for the bondwire inductance. The measured $S_{11}$ at the SMA connector is $<$ -10 dB at 12.5-15.5 GHz (Fig. 2.21b-c). The two RF inputs are separated by 800 $\mu$m on the board and the electromagnetic coupling between the two channels is also simulated in HFSS. The coupling between the channels is $\sim$-37 dB at 15 GHz including the bondwires (Fig. 2.22a), and is $\sim$-35 dB including the bondwires and the CPW matching networks (Fig. 2.22b).

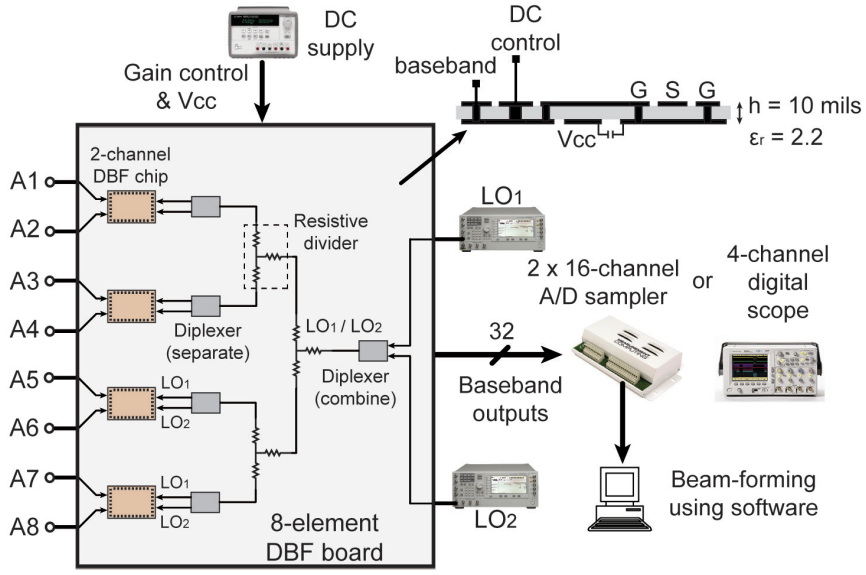



**Figure 2.19**: Layout of an 8-element digital beamformer measurement setup.

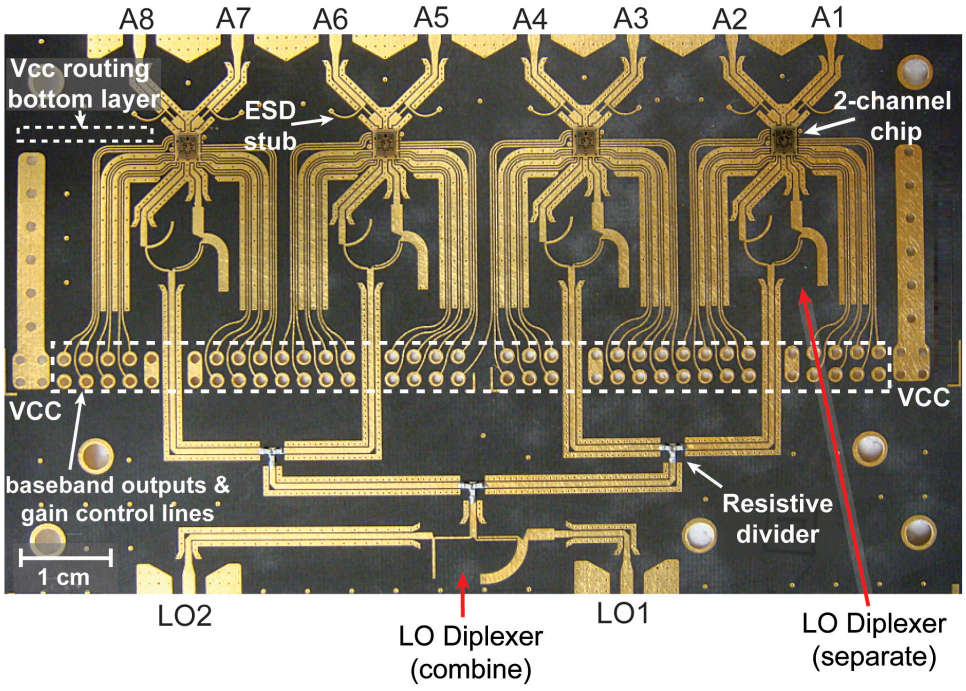



**Figure 2.20**: Picture of the fabricated 8-element Ku-Band DBF board.

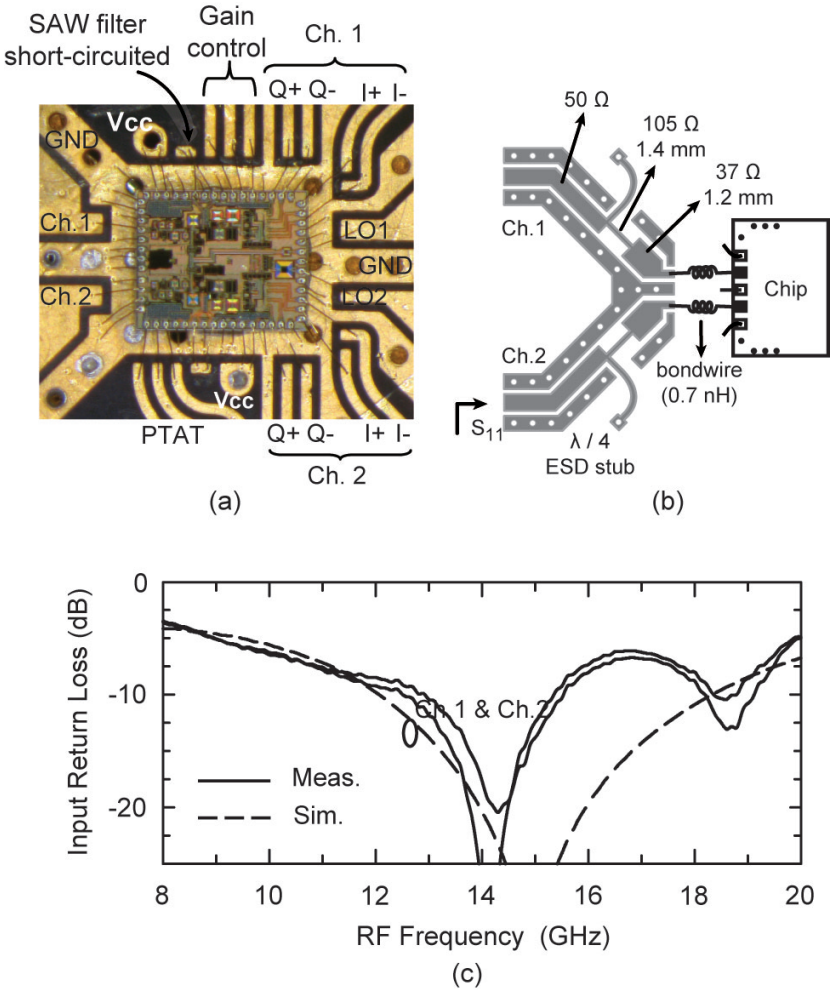



**Figure 2.21**: (a) Close-up view of the chip assembly, and (b) details of the input matching network and (d) measured S11 for A1 and A2.

The Vcc lines are routed to both sides of the dual-channel chip, feeding each channel with multiple bondwires so as to reduce the supply inductance. Also 31 bondwires to ground are used so as to result in a low-inductance RF ground. The silicon chip itself has 15 pF and 20 pF on-chip de-coupling capacitors between on-chip Vcc and ground planes for the RF-front-end and IF-stage, respectively. Therefore, at the design frequency the on-chip supply line is effectively shorted to the on-chip ground. For lower frequencies, 100 nF capacitors are placed on the board for Vcc de-coupling.

The effect of bondwire inductance on the receiver RF-front-end performance is presented in Fig. 2.23, where $Lvdd$ is the supply bondwire inductance, and $Lgnd$ is the total effective ground (bondwire) inductance. In the simulations, $Lvdd$ is assumed to be infinite and only $Lgnd$ is swept (since supply and ground are RF-shorted on the chip by de-coupling caps, sweeping only $Lgnd$ is sufficient). The receiver RF-front-end is mostly a differential design, except the first LNA stage, and maintains a good return loss, a gain of $\sim$20 dB for 0-100 pH effective bondwire inductance. The NF of the RF-front-end is dominated by the NF of the first stage (single-ended). Assuming that a simultaneous noise and input matching is achieved, the noise figure of an LNA can be calculated using [59]:

$$NF_{\mathrm{without-Lgnd}} = 1 + \frac{\mathrm{r_b}}{\mathrm{R_s}} + [(\mathrm{R_s}+\mathrm{r_b})^2 + (\mathrm{wL_b}+\mathrm{L_e})^2](\frac{\mathrm{I_{CQ}}}{2\mathrm{B_{DC}V_T R_s}}) \tag{2.3}$$
$$+\frac{1}{gm^2}[(1-w(L_\mathrm{b}+\mathrm{L_e})\mathrm{wC}\pi)^2 + ((\mathrm{R_s}+\mathrm{R_b})\mathrm{wC}_\pi)^2](\frac{\mathrm{I_{CQ}}}{2\mathrm{V_T R_s}}),$$

and replacing $L_\mathrm{e}$ with $L_\mathrm{e}$+$L_\mathrm{gnd}$ and

$$R_\mathrm{s} = \mathrm{r_b} + \frac{\mathrm{gmL_e}}{\mathrm{C}_\pi}, \quad \mathrm{w(L_b+L_e)} = \frac{1}{\mathrm{wC}_\pi} \tag{2.4}$$

gives

$$NF_{\mathrm{with-Lgnd}} = \mathrm{NF_{without-Lgnd}} \tag{2.5}$$
$$+[(wL_\mathrm{gnd})^2 + \frac{2\mathrm{L_{gnd}}}{\mathrm{C}_\pi}](\frac{\mathrm{I_{CQ}}}{2\mathrm{B_{DC}V_T R_s}}) + \frac{1}{\mathrm{gm}^2}(\mathrm{w}^2\mathrm{C}_\pi\mathrm{L_{gnd}})^2(\frac{\mathrm{I_{CQ}}}{2\mathrm{V_T R_s}}).$$

Note that this equation only takes in-to-account the effect of $Lgnd$ on the noise matching of the LNA (0.1-0.2 dB). In addition to this, there is additional noise loops between the stages through bias circuits, on-chip ground and Vcc supply (due to the non-ideal inductive ground) increasing the NF. The RF-front-end results in a simulated NF of $<$ 3.5 dB for 0-100 pH ground inductance (Fig. 2.23d). The estimated ground bondwire inductance is $\sim$50 pH (using HFSS [58]).

The effect of the ground bondwire inductance on the coupling between the channels is also analyzed (Fig. 2.24). Note that the coupling between the channels is ideally zero without

ground bondwire inductance (on-chip measurements, including probe coupling effects, results in ∼-50 dB coupling). The coupling increases to -47 dB ($S_{\mathrm{out2-ch1}} = -27$ dB and $S_{\mathrm{out1-ch1}} = +20$ dB) and to -44 dB ($S_{\mathrm{out2-ch1}} = -24$ dB and $S_{\mathrm{out1-ch1}} = +20$ dB) for an effective ground bondwire inductance of 50 pH and 100 pH, respectively (Fig. 2.24).

A single LO distribution network is employed on the PCB for both $LO_1$ and $LO_2$ in order to eliminate the multitude of cross-overs needed for two separate LO networks (Fig. 2.21). A diplexer is used to combine $LO_1$ at 2.45 GHz and $LO_2$ at 12.55 GHz, and the combined LO is distributed using a wideband 1:8 resistive divider network. As shown in Fig. 2.25, the two different LO frequencies enter the diplexer from port 1, and the diplexer performs frequency selectivity by presenting an open-circuit condition at the opposite output port, and using a combination of stubs and coupled lines which are $\lambda$/4-long at $LO_1$ (12.5 GHz). CPW-to-microstrip transitions are also designed since the diplexer is designed in microstrip. Independent measurements on the diplexers show excellent agreement with simulations (Fig. 2.25). At the chip side, another LO diplexer is used to separate the two frequencies and provide two LO inputs to the silicon chip. At 12.5 GHz, the LO distribution loss is ∼20 dB: 9 dB (1:8 division), 6 dB (2-stage resistive divider), 2.5 dB (two diplexers), and 2 dB (t-line loss). At 2.45 GHz the LO loss is ∼16.5 dB. Therefore, an input LO power of 10-13 dBm is required for $LO_1$ and $LO_2$, and we have used 20 dBm for both LOs.

### 2.4.2 Board Measurements

The 8-element board can be measured using 50 Ω coaxial ports (gain, NF, $S_{11}$, isolation), and can also be connected to 8 antennas and measured in an anechoic chamber. For the coaxial measurements, A1 and A2 were tested (Fig. 2.26a), and the measured performance is shown in Fig. 2.21c, Fig. 2.26b and Table 2.2, and includes an additional 0.6 dB loss due to the matching network and SMA connector. For the antenna measurements, endfire dipole antennas are used with a spacing of $0.5\lambda_0$ at 15 GHz (see [60, 61] for details on the antennas). The resulting 8-element patterns are synthesized in Matlab. In this case, no modulation is present on the RF signal, and the sampling is done at 10 ksps. Due to the non-real-time approach, one can synthesize any number of simultaneous patterns with any sidelobe level using software techniques. An example is shown in Fig. 2.26c with -23 dB sidelobes.

Rockwell Collins have also used the two-channel receiver chip in an FPGA-based real-time phased array, and synthesized three simultaneous beams for tracking three different transmitters located at different angles all at 15-16 GHz with a 10.7 Mbps O-QPSK modulation

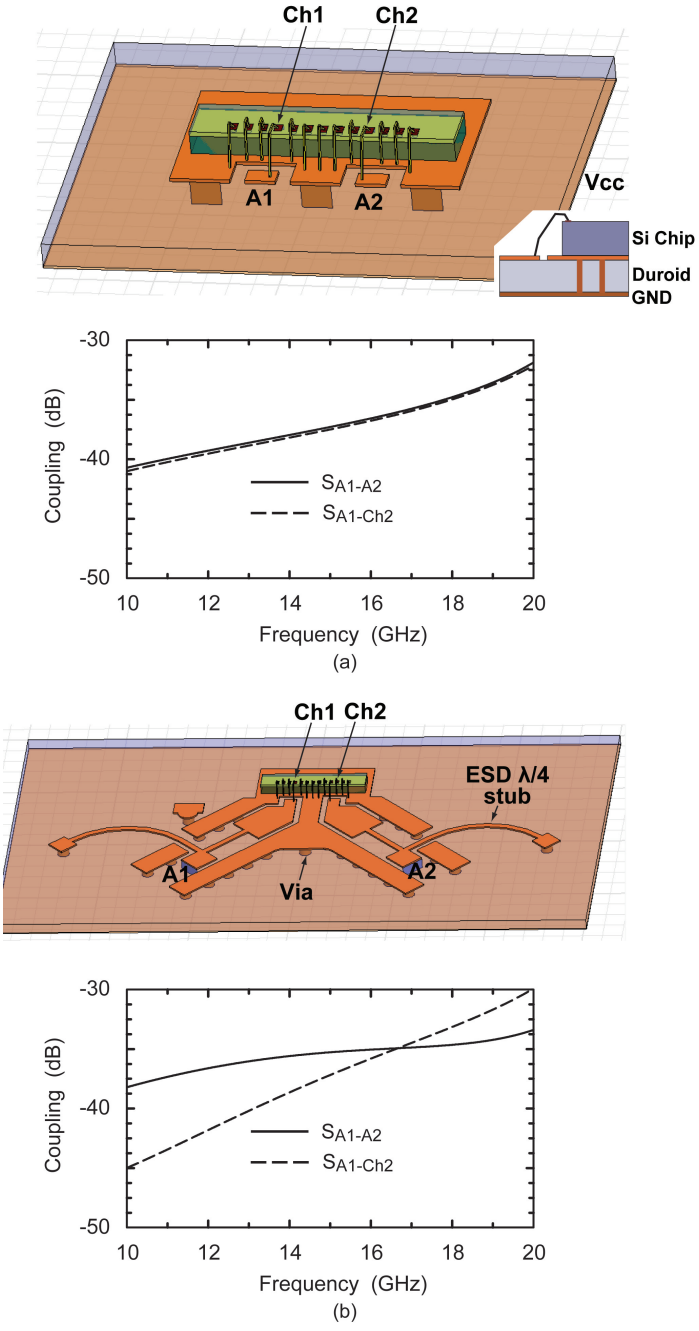



**Figure 2.22**: 3-D chip-on-board packaging model in HFSS: coupling between two channels (a) including bondwires, and (b) including bondwires and matching networks.

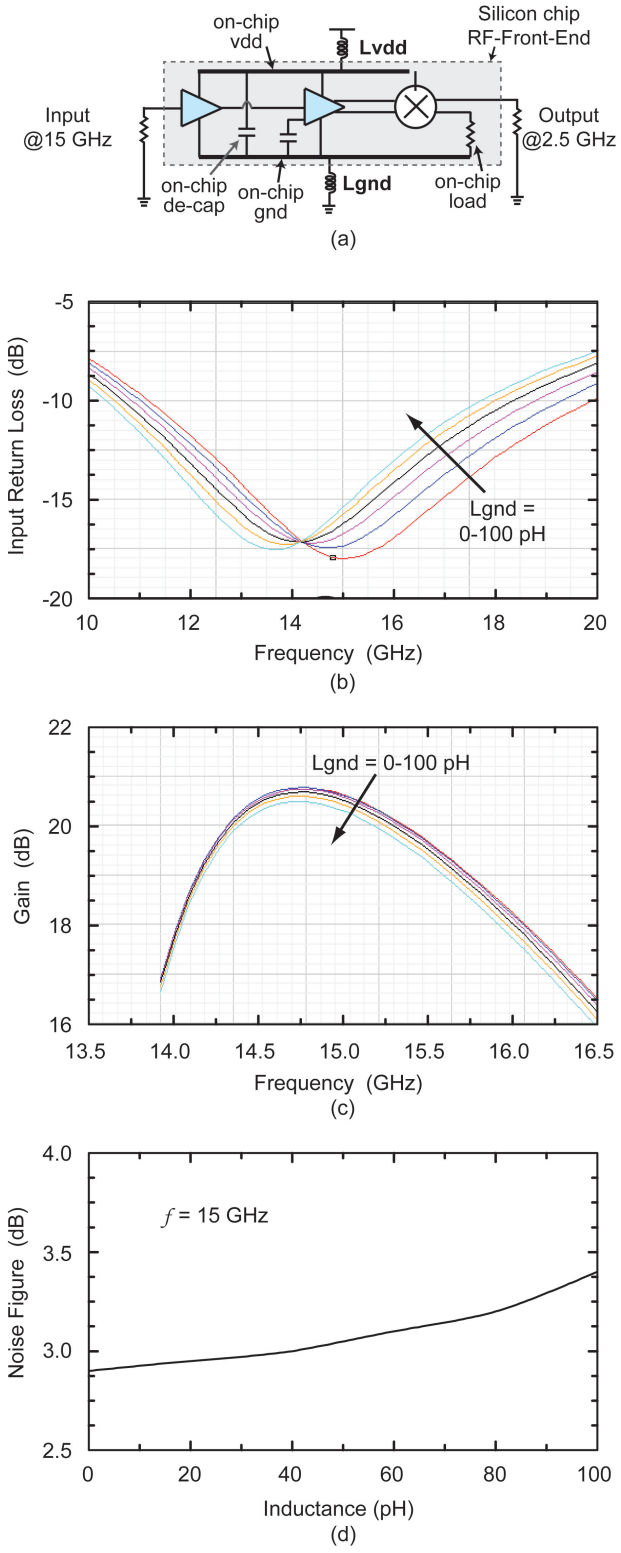



**Figure 2.23**: Effect of parasitic bondwire inductance on channel performance: (a) input return loss, (b) gain, and (c) noise figure.

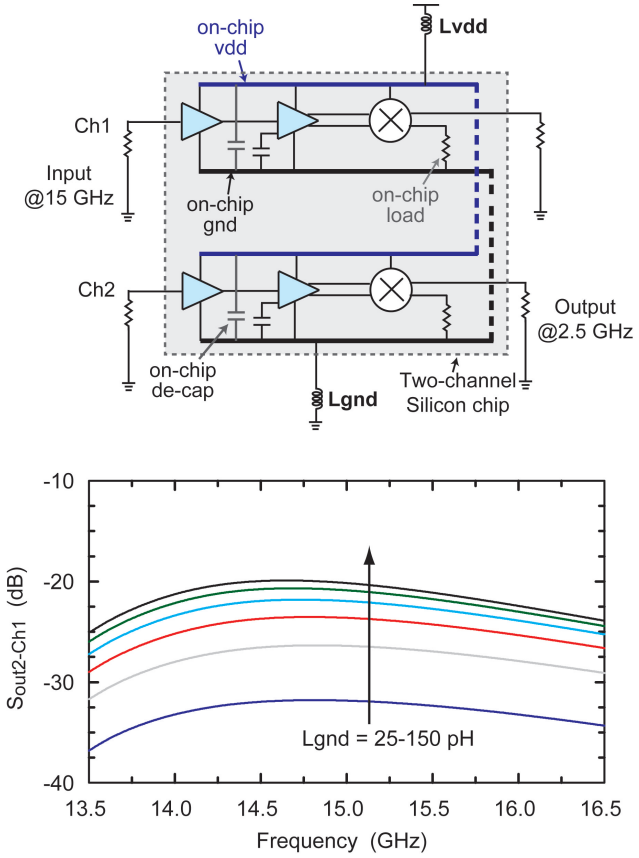



**Figure 2.24**: Coupling between channels with parasitic ground bondwire inductance. Coupling for Lgnd=0 pH is very low and is not shown.

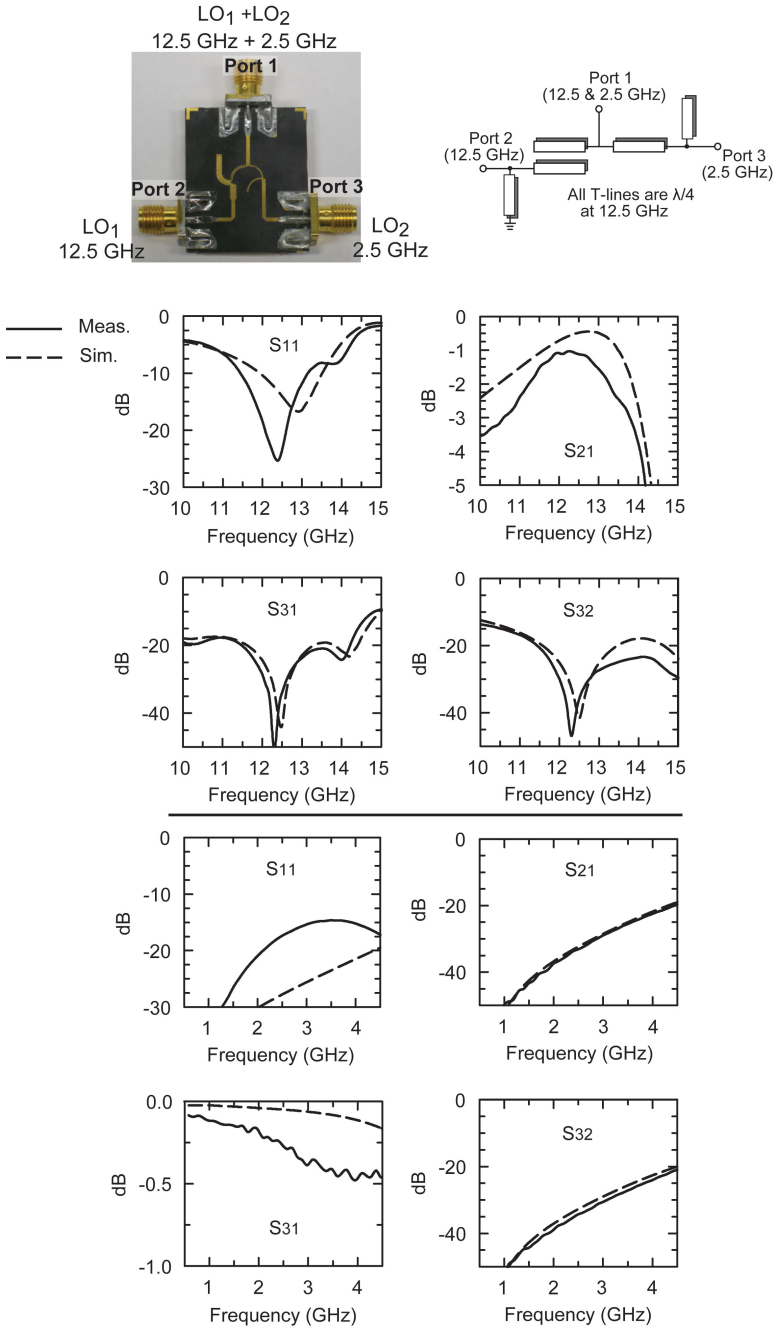



**Figure 2.25**: Measured and simulated S-parameters of the diplexer. Different frequency regions are shown for clarity.

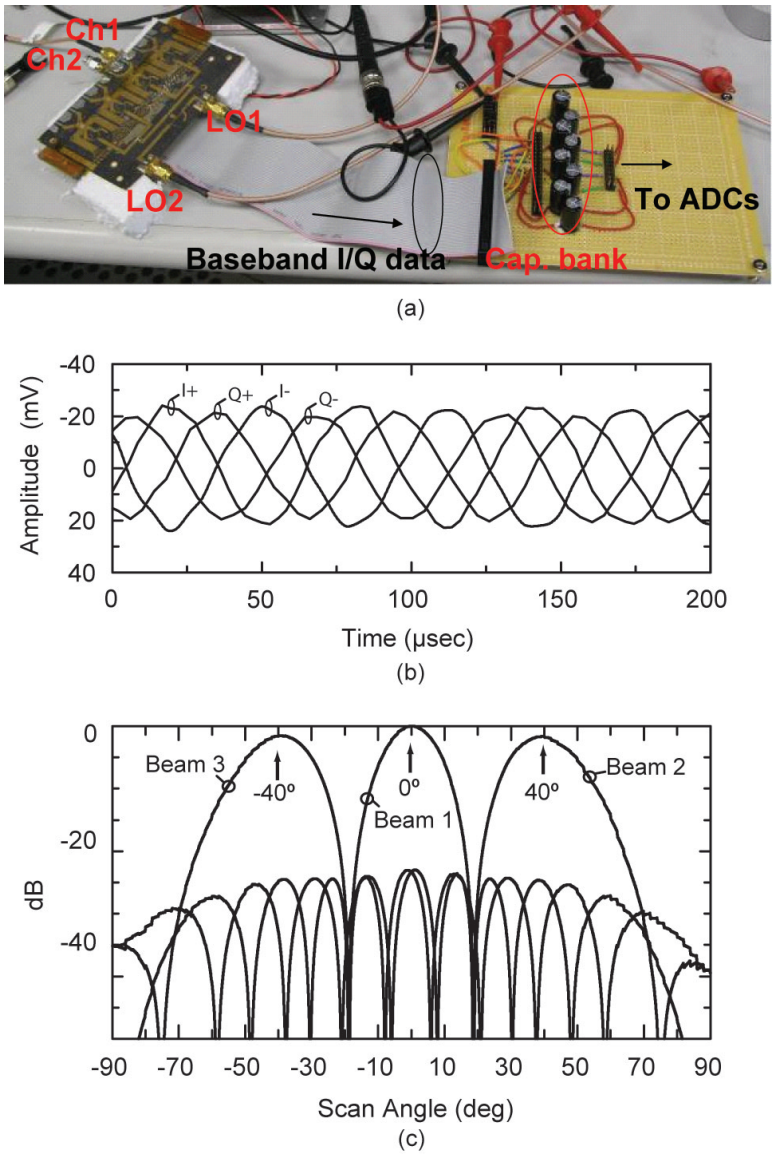



**Figure 2.26**: (a) Baseband waveforms at the output of the chip (I+, I-, Q+, Q-) in a system level configuration. The signals are measured using an ADC card at 10 ksps. (b) Synthesized patterns with Matlab for three different scan angles using a Dolph-Chebyshev distribution with -23 dB sidelobes.

**Table 2.2**: On-Board System Performance (A1 and A2)

| RF=15 GHz, $LO_1$=12.5 GHz, $LO_2$=2.45 GHz, Baseband=0.01-1 MHz | |
|---|---|
| **Gain** | 45 dB |
| **Input Return Loss** | < -10 dB @ 13-15.5 GHz |
| **NF** | 3.6 - 3.8 dB |
| **Channel-to-channel Coupling** | < -39 dB at 0.01-1 MHz |

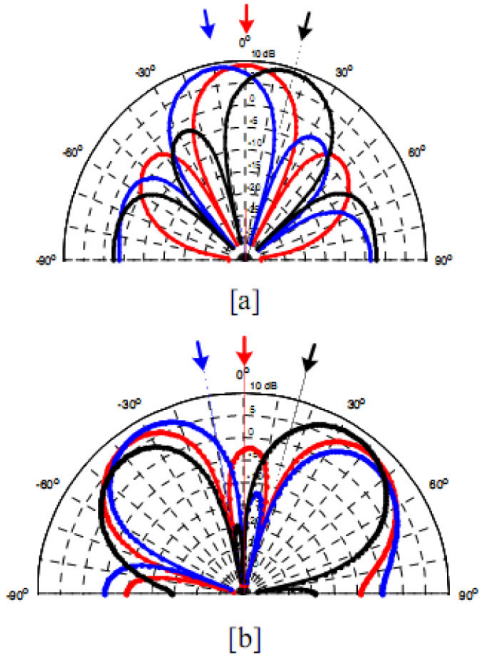



**Figure 2.27**: Rockwell Collins real-time digital-beam-forming array achieved three simultaneous beams tracking different angles: (a) without null placement, and (b) with null placement [1]

(Fig. 2.27). Furthermore, the Rockwell Collins digital beamformer synthesized two nulls in each pattern at angles corresponding to the other two transmitters. The reader is referred to [1] for details on this advanced Ku-band digital beam-forming phased array.

## 2.5 Conclusion

The first fully integrated two-channel SiGe BiCMOS digital beam forming phased array receiver capable of operation in the 8-20 GHz is presented. The receiver is based on a

dual-down-conversion architecture with selectable IF for interference mitigation, and the silicon chip is fabricated using a 0.18-$\mu$m SiGe BiCMOS process, has ESD protection on the RF and DC pads. The chip achieved excellent performance over the entire 8-20 GHz band with high gain, low noise figure, near-ideal I/Q balance and very low EVM. An 8-element array with a diplexed LO distribution network was demonstrated at 15 GHz and resulted in excellent performance. The chip was also used in a real-time FPGA-based phased array system at 15 GHz to generate three simultaneous beams each with 10.7 Mbps links.

## Acknowledgement

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# Chapter 3

# X/Ku-Band 8-Element Phased Arrays Based on Single Silicon Chips

## 3.1 Introduction

In the recent years, a lot of work has been done on silicon phased arrays, and silicon chips with many elements and multibeam capabilities have been developed []. Silicon-based phased arrays have now been demonstrated from X-band to V-band using RF beam-forming techniques [10, 11, 13–15, 62, 63]. The main advantages of the RF architecture are its simplicity, system-level linearity, low power consumption (no LO drivers, no LO distribution), and the use of a single high-performance transceiver.

There is an ongoing need for a low-cost scalable solution for silicon based phased array systems. A card based approach is shown in Fig. 3.1, where a silicon chip with 8 or 16 elements is placed on a board and connected to an antenna array. Optional GaAs LNA are placed for low noise receiver arrays. This board can be stacked in order to implement scalable N$\times$M phased array systems.

Most of the published work presents on-chip measurements using CPW probes, but this ignores the packaging aspects of multi-element phased arrays, such as RF transitions and associated impedance matching networks, coupling between the different RF ports, Vcc de-coupling and oscillations - especially in high gain designs, and the creation of a low-inductance ground between the chip and the antenna distribution board. These issues if not properly designed and mitigated, can degrade the phased-array chip performance and render it un-usable in practical implementations.

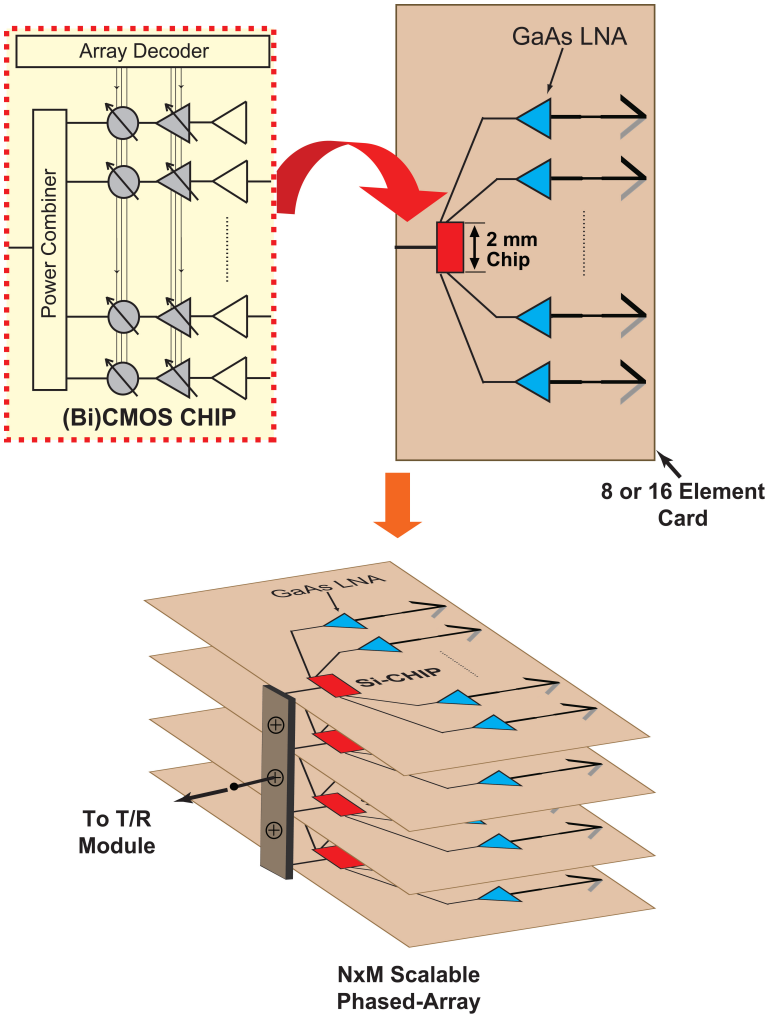


**Figure 3.1**: Low-cost scalable phased array system using silicon BiCMOS chips.

For the first time, a complete 8-element X/Ku-band phased array based on a single silicon chip is presented in this chapter. The phased array is built on single-layer Teflon substrate (Rogers RO3002) and contains the radiating elements, silicon chip, control circuits and all RF transmission lines.

## 3.2 Design

### 3.2.1 8-Element Phased Array Chip Design

The 8-element silicon phased-array chip is shown in Fig. 3.2 and has been presented in [11]. The chip results in an element gain of 20$\pm$1 dB and a NF of 4.5$\pm$0.5 dB at 10-14 GHz, and 4-bit phase control with an RMS phase and gain error of $< 6^{\circ}$ and $< 0.7$ dB at 6-18 GHz, respectively. The chip also contains all the digital control circuitry, with a 3-bit address decoder and a 4-bit shift register for setting the phase state at each element. ESD protection is also present at all RF and digital pads. The chip size is 2.5$\times$2.2 mm$^2$ with a current consumption of 170 mA from a 3.3 V supply (560 mW). The performance of the 8-element silicon phased-array chip is summarized in Table 3.1.

As shown in Fig. 3.2, the silicon chip is a nearly perfect symmetrical two-column design with four channels in each column. The sum-network is in-between the two-columns, and the line-lengths from channels to the output sum-node are equal. The input RF pads (8 of them) are located on the east (4) and west (4) side of the chip, and the output is taken out from the south side. The digital circuitry and associated control pads are located on the north side of the chip.

### 3.2.2 8-Element Phased Array Board Design

Fig. 3.3 shows the assembled 8-element phased array board. The linear phased-array is based on angled-dipole antennas on an $\epsilon_r$ = 2.2, h = 10 mils (0.25 mm) Duroid substrate, which result in a low-gain radiation pattern [60]. This allows for scanning up to 60$^{\circ}$ off broadside without excessive gain loss arising from the element factor (i.e., dipole pattern). The element-to-element spacing is 0.5$\lambda_0$ and the simulated coupling ($S_{21}$) between adjacent dipoles is -17 to -22 dB at 11.4-12.6 GHz. The antennas are resonant at 12 GHz with an $S_{11} <$ -10 dB between 10.5 and 14 GHz, and with a measured gain of 3.0 dB at 12 GHz. Also, two dummy elements are used at the edge of the array to enhance the scanning performance at wide angles.

The silicon chip is connected to 8 dipole antennas using matching networks and 50 $\Omega$

**Table 3.1**: Performance Summary of 8-Element Silicon Chip

| | |
|---|---|
| **Technology** | 0.18 $\mu$m SiGe BiCMOS (Jazz SiGe120, 1P6M) |
| **Frequency / Phase Resolution** | 6-18 GHz / 4-bit (accuracy $>$ 5-bit) |
| **Input Return Loss** | $<$-10 dB @ 11-15 GHz |
| **Input Return Loss** | $<$-10 dB @ 6-18 GHz |
| **Output Return Loss** | $<$ -10 dB @ 8-25 GHz |
| **Gain (average)** | 20.8 dB @ 12 GHz |
| **NF** | $<$5 dB @ 12 GHz, all phase states |
| **IIP3** | -31 dBm @ 12 GHz |
| **Group Delay** | 162.5$\pm$12.5 ps @ 6-18 GHz |
| **Phase Error (RMS)** | $<$ 5.7° @ 6-18 GHz, single-channel<br>$<$ 2.7° @ 6-18 GHz, all-channels |
| **Gain Error (RMS)** | $<$ 0.9 dB @ 6-18 GHz, single-channel<br>$<$ 0.4 dB @ 6-18 GHz, all-channels |
| **Channel-to-Channel Isolation** | $<$-43 dB @ 6-18 GHz |
| **Output to Input Isolation** | $<$-60 dB @ 6-18 GHz |
| **Array-Factor Directivity** | 9 dB (8-Elements) |
| **Area** | 2.2$\times$2.45 mm$^2$ |
| **Power Consumption** | 170 mA, 3.3 V |

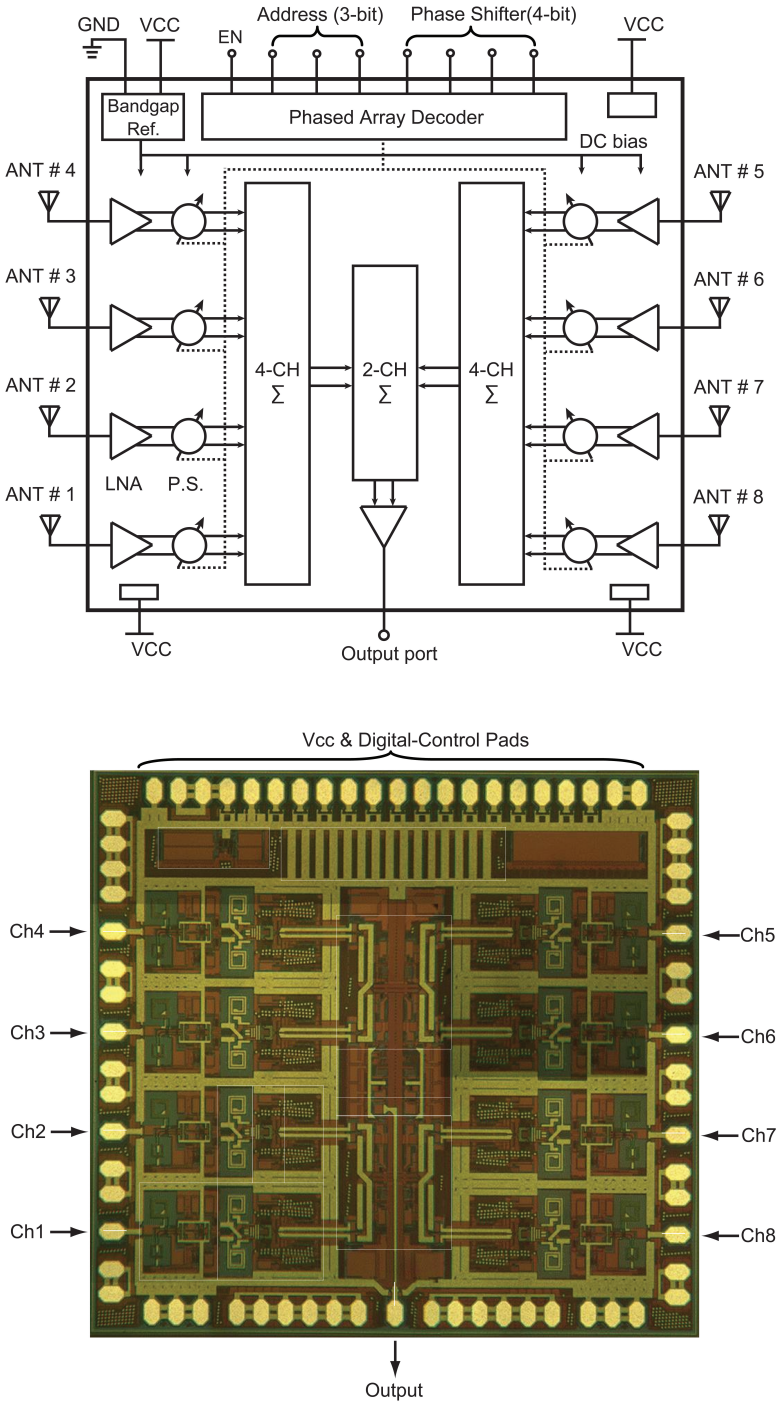


**Figure 3.2**: Functional block diagram of the 8-element silicon phased array chip (2.2×2.45 $mm^2$).

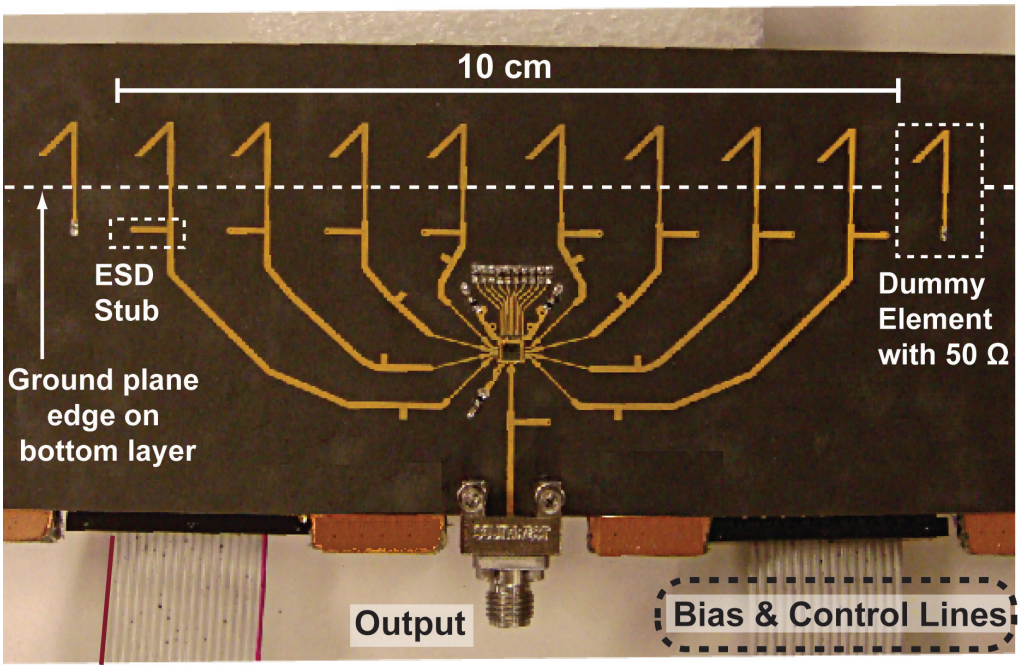


**Figure 3.3**: The 8-element X/Ku-band phased array with the silicon chip at its center.

transmission lines. The lines are not designed to be equal in time delay, and this limits the instantaneous bandwidth to 12 GHz$\pm$5%. In fact, the relative phase in the transmission-line lengths at 12 GHz is chosen to be 0°, -135°, -427.5° and -720° from the closest to the farthest antenna. This allows calibrating out the phase difference between the antenna elements using the on-chip 4-bit phase shifter without introducing any additional phase error. The transmission-line and matching network loss between the silicon chip and the radiating dipoles is 0.25/0.35/0.55/0.7 dB at 12 GHz from the closest antenna to the farthest one, and results in a natural taper of only 0.5 dB across the array.

A matching network is essential at each RF port due to the inductive effect of the bondwires (0.6-0.8 nH), and this is accomplished using the circuits shown in Fig. 3.4. The matching networks take into account the true impedance ($S_{11}$ or $S_{22}$) at the silicon chip GSG pads [11]. The input matching circuit in Fig. 3.4a is space limited due to the 4 RF inputs at one side of the chip and therefore uses a longer high impedance network. Both matching networks result in $S_{11}$ $<$ -10 dB from 10.5 to 14 GHz. Additional ESD protection is achieved using shorted $\lambda$/4 stubs

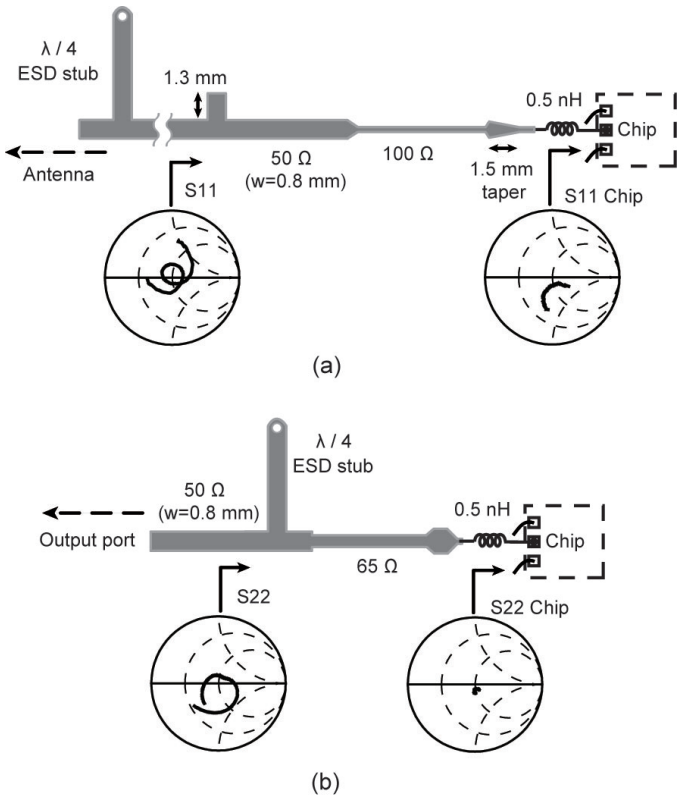


**Figure 3.4**: Matching networks for (a) input RF ports (8 of them) and (b) output RF port. The frequency span is 10-14 GHz.

on each transmission-line.

The silicon phased-array chip is placed on a grounded pedestal and the bond-wire coupling is minimized using several ground connections between the different RF inputs as shown in Fig. 3.5 and Fig. 3.6. Also, the input matching circuits are designed to quickly diverge so as to minimize the transmission-line coupling (see Fig. 3.5). Vcc is connected to the chip at three different corners using 100 nF bypass capacitors in series with 16 ohm resistors at each node (both capacitors and resistors are 0201 surface mount devices, Fig. 3.5). This results in a low inductance in the power supply line and excellent low frequency grounding. The digital and bias control lines are routed on the north of the chip, and then are connected to a ribbon cable connector on the bottom level of the board.

Ansoft HFSS, [58], is used to simulate the chip-on-board packaging structure in a 3-D environment, and includes the RF, grounding and bias effects, and the distributed coupling between the high impedance matching sections on the Duroid substrate. Shown in Fig. 3.6 is the 3-D model of the packaging structure. The simulated coupling between adjacent RF input ports, spaced at a center-to-center distance of 0.4 mm is $<$ -18 dB at 12 GHz (Fig. 3.6a). The coupling between the Vcc supply trace on the teflon board and the nearest RF signal line is $<$-40 dB at 12 GHz (Fig. 3.6b).

The signal lines in the proximity of the chip are 0.75 mm long, 0.2 mm wide, and are spaced with 0.2mm (0.4mm center-to-center), which results in $\sim$-23 dB coupling (Fig. 3.7a). This on-board coupling can be reduced to $\sim$-33 dB for a spacing of 0.5 mm.

The coupling between the adjacent elements (including bondwires, and RF-lines) can be further reduced by using 0.5 mm on-board spacing and extending ground (GND) traces (from the grounded pedestal) between the signal lines on the PCB board as shown in Fig. 3.6b. The coupling between adjacent elements is reduced to $\sim$-22 dB (was $\sim$-18 dB for 0.2 mm spacing) when the extended GND trace are left open on one side (ground extensions are acting as a open stubs from the reference ground pedestal). The coupling is further reduced to $\sim$-29 dB, when the extended GND traces are shorted to the bottom ground (reference ground plane). Therefore, in the future designs, CPW lines will be used (creating a low inductance ground plane on the top metal of the Teflon board) and the top-GND will be connected to the ground extensions for lower coupling (It is also important to have a continuous and short ground return path).

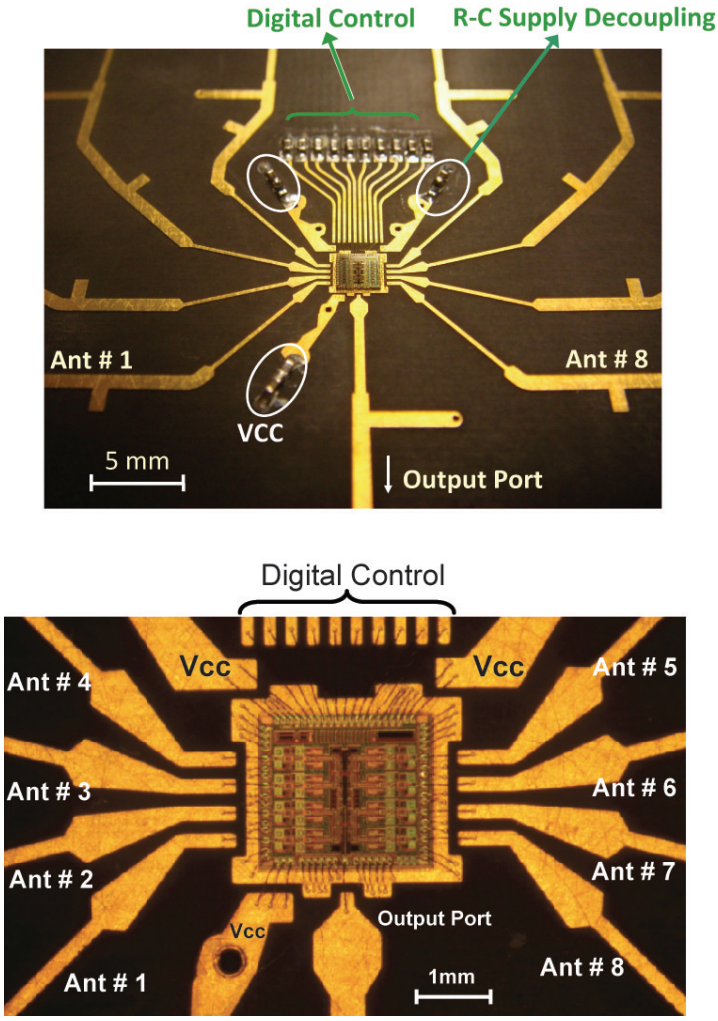


**Figure 3.5**: Input and output transmission lines around the silicon chip, and the chip-on-board packaging ($2.5 \times 2.2$ mm$^2$).

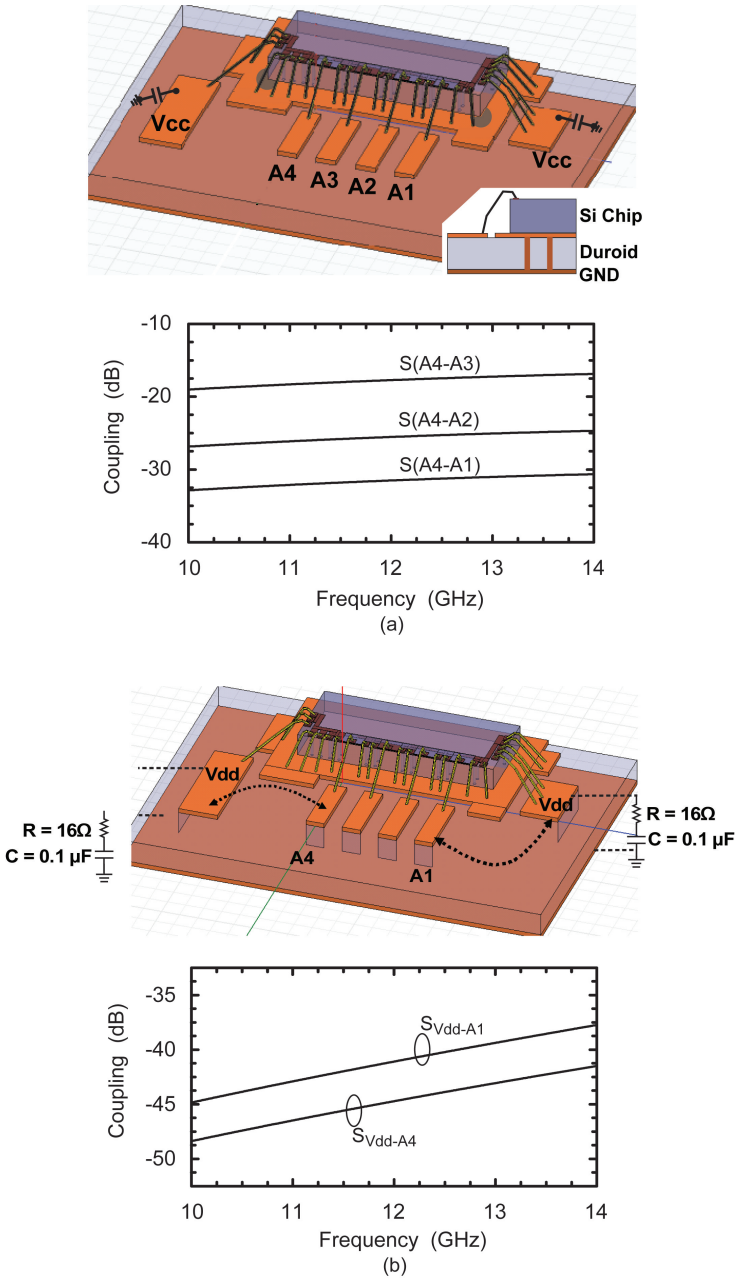


**Figure 3.6**: 3-D view of the silicon chip, bondwires, grounded pedestal and input RF transmission lines, and the simulated coupling between the input RF ports. Coupling (a) between elements (RF paths), and (b) between Vcc supply lines and the closest RF channel.

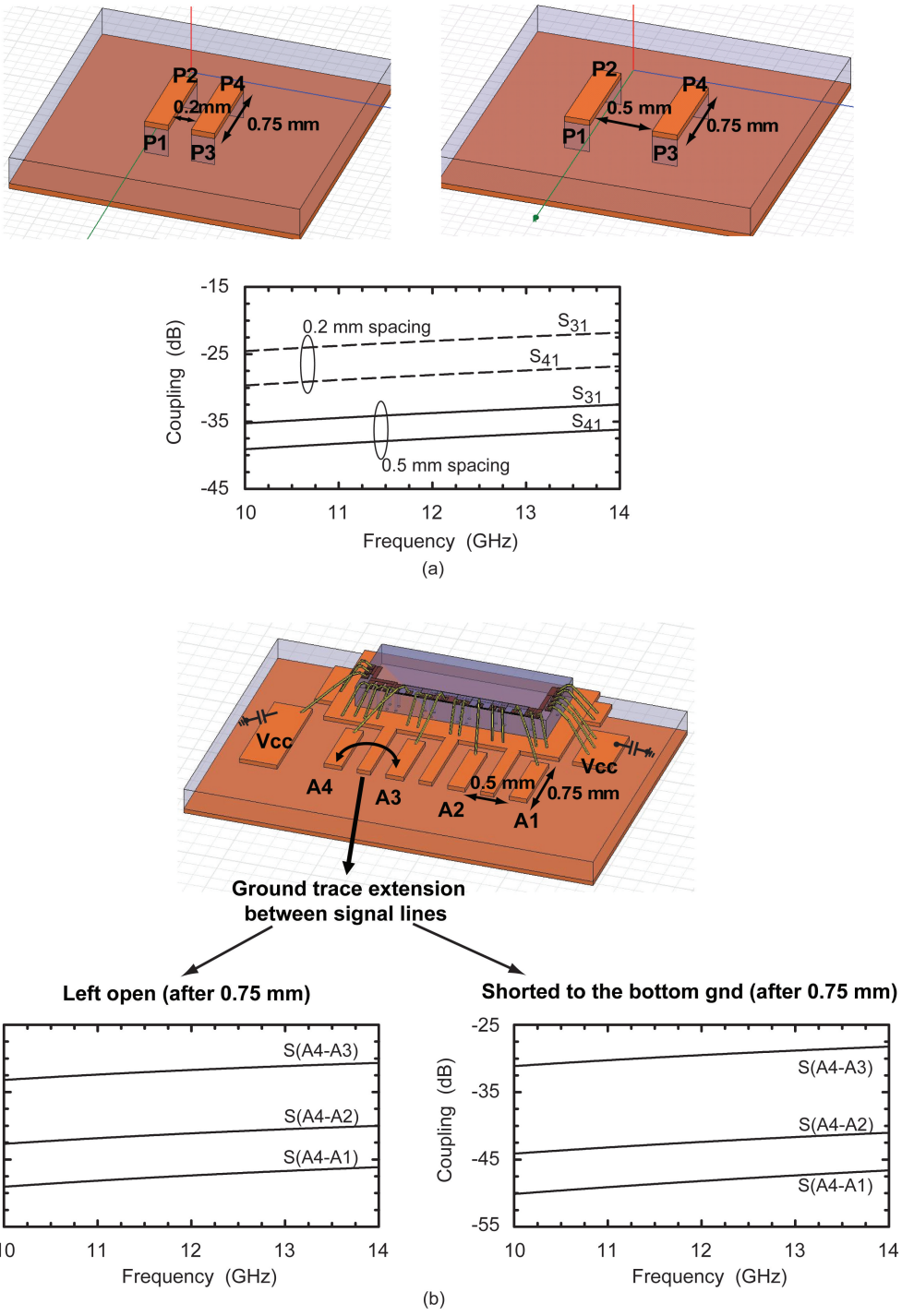


**Figure 3.7**: 3-D EM coupling simulations of (a) two RF lines separated by 0.2 and 0.5 mm, (b) chip-on-board packaging with 0.5 mm spacing between RF signal traces, and ground extensions (two cases are given: when the ground extensions are left open, or when the ground extensions are connected to the reference ground plane).

## 3.3 Measurements

### 3.3.1 S-parameter Measurements

The measured reflection coefficient at the output of the phased array board is shown in Fig. 3.8. An excellent impedance match is achieved at 11-13 GHz and the results agree well with simulations. The input reflection coefficient for the 8 RF input ports could not be measured since the ports are directly connected to the dipole antennas.

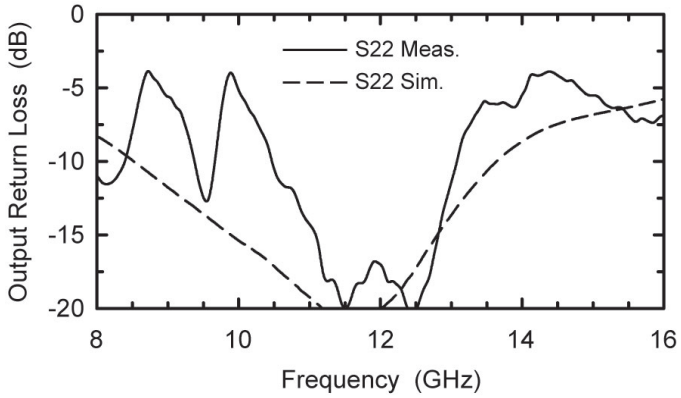


**Figure 3.8**: Measured output return loss. Measurements include the 3.5 mm connector effects.

### 3.3.2 Gain and Pattern Measurements

The Angled dipole antenna array is designed using Ansoft HFSS, and Fig. 3.9 presents the measured angled-dipole pattern at 12 GHz in a three element array. Measured and simulated input return losses are in very good agreement, and it is seen that the angled-dipole can be used to scan to 60° with ∼4 dB loss in the element factor. In addition, the simulated dipole pattern in an 8-element array (as opposed to a 3-element array) is even broader due to the mutual coupling between the elements.

The far-field patterns and gain were measured in an anechoic chamber using a standard gain horn transmitter and with an incident power of -65 dBm per dipole element (Fig. 3.10). The silicon chip phase states are controlled by using a computer, and the received power is monitored using a power sensor. The measured patterns at 12 GHz (Fig. 3.11a) show excellent scanning performance up to 60° with ∼ -13 dB sidelobes. The measured normalized patterns at 12 GHz are shown in Fig. 3.11b-d for 0°,30°, and 60° scanning and agree very well with simulations. The measured beamwidth is 15° for 0° scanned beam, and increases to 19° and 26° for 30° and

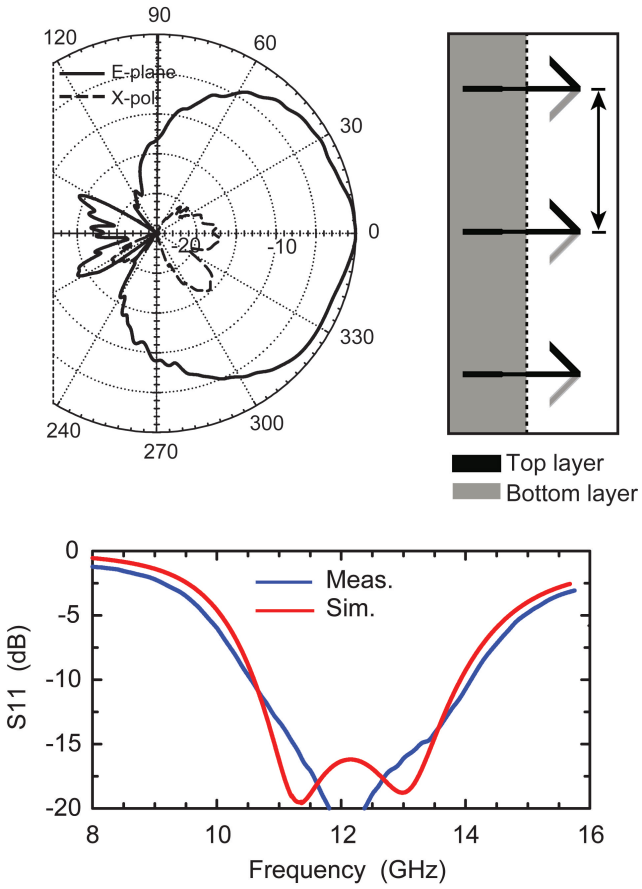


**Figure 3.9**: Measured angled-dipole antenna pattern at 12 GHz in a 3-element configuration (center element shown).

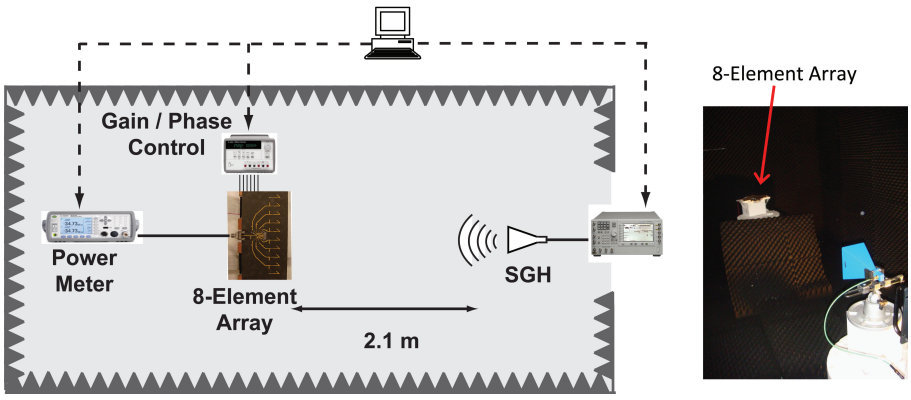


**Figure 3.10**: Block diagram and photo of the gain and pattern measurement setup.

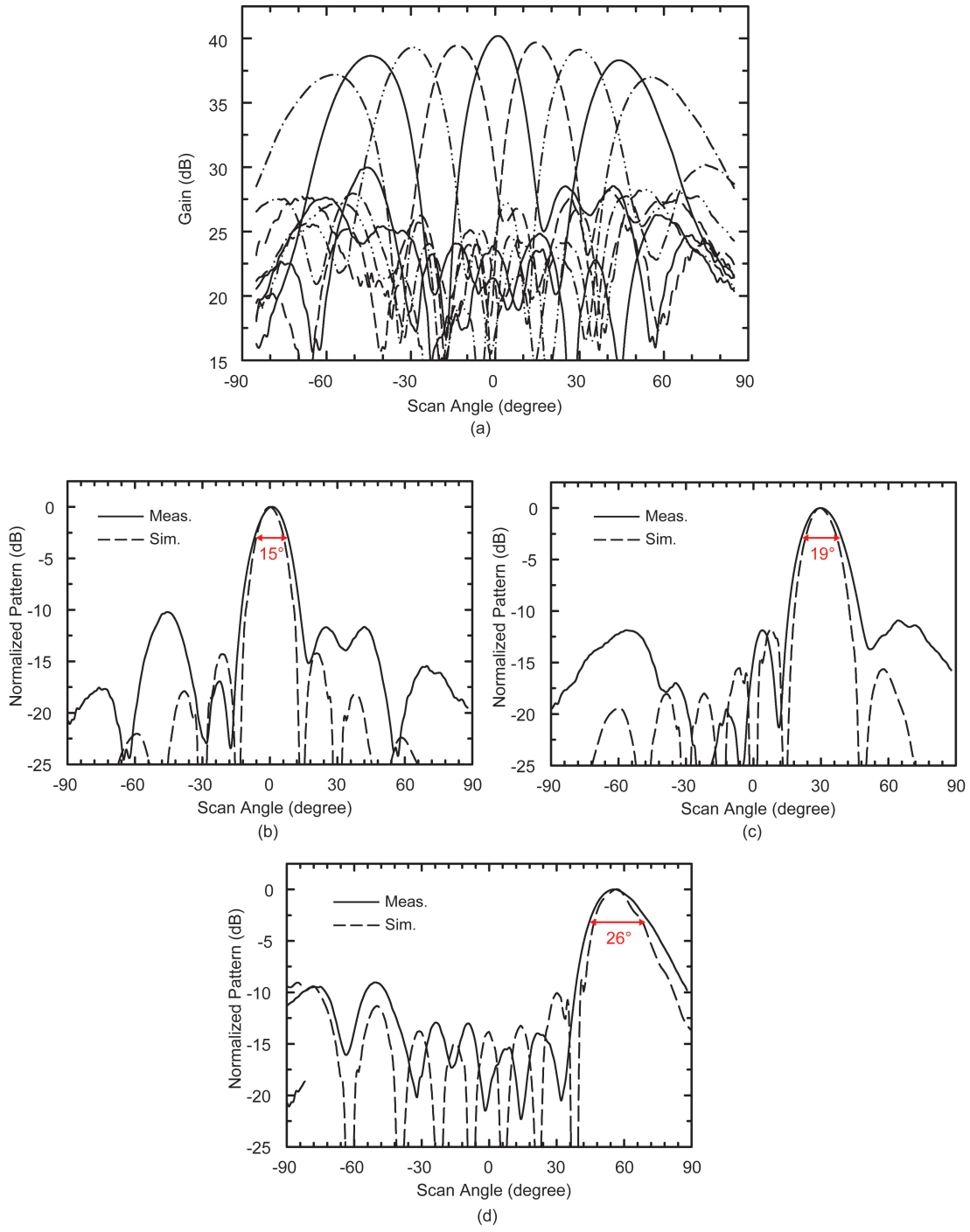


**Figure 3.11**: (a) Measured patterns at 12 GHz plotted on an absolute gain scale. Comparison between measured and simulated normalized patterns of (b) 0°−, (c) 30°-, and (d) 60°-scanned beams at 12 GHz.

60° scanning, respectively, as expected from an 8-element linear array.

The gain of the 8-element array, $G_{DUT}$, is measured in the receive mode and using the Friis transmission equation:

$$\frac{P_r}{P_t} = (\frac{\lambda_0}{4\pi R})^2 G_t G_{DUT} \tag{3.1}$$

The gain measurement is done at a system level, with $P_t$ and $P_r$ measured at the transmit and receive ports, and $G_t$=20.0 dB (horn antenna gain), R=2.1 m, and $\lambda$=2.50 cm. An RF power of -25 dBm ($P_t$) is radiated at 11-13 GHz using the signal source and the 20-dB-gain horn antenna. The space loss for a distance of 2.1 m is -60 dBm at 12 GHz. The received power at output SMA connector of the 8-element array is monitored by a power sensor and the measured gain includes the element factor, input and output transmission lines, matching networks and connector loss.

The silicon chip contains an active 8:1 current summer for channel combining. Therefore, the output power is proportional to $N^2$ and not to N as in standard Wilkinson-based phased arrays (Fig. 3.12a-b). This is contrary to the fundamental array principle (i.e., the total power cannot be greater than N×single-element), but it is important to note that in an active combiner, the additional RF power is delivered from the Vcc power supply. The current summer therefore results in an 8-element combined gain of 64 (18 dB) in addition to the electronic single channel gain of 20 dB. In addition, the angled-dipole (element factor) has a gain of ∼3.0 dB and the transmission-line and connector losses are ∼0.7 dB, which results in a total gain of ∼40 dB (Table 3.2).

**Table 3.2**: Gain of the 8-Element Phased Array

| | |
|---|---|
| **Silicon-Chip Channel Gain** | 20-21 dB |
| **Array Gain** | 18 dB ($\propto N^2$) |
| **Antenna Gain** | ∼3 dB |
| **Connector Loss** | ∼ 0.7 dB |
| **Total Phased Array Gain** | ∼40 dB |

The measured gain at 12 GHz is shown in Fig. 3.12c for -60° to 60° scan angles, and is in excellent agrement with simulations. Measured gain is slightly higher than the simulated gain at wide scan angles (-60°, 60°) due to the antenna pattern broadening in an 8-element environment which was not taken into account in the simulations. Note that this is the small-signal gain, and the measured output power is ∼ -25 dBm which is within the linear power region of the silicon chip.

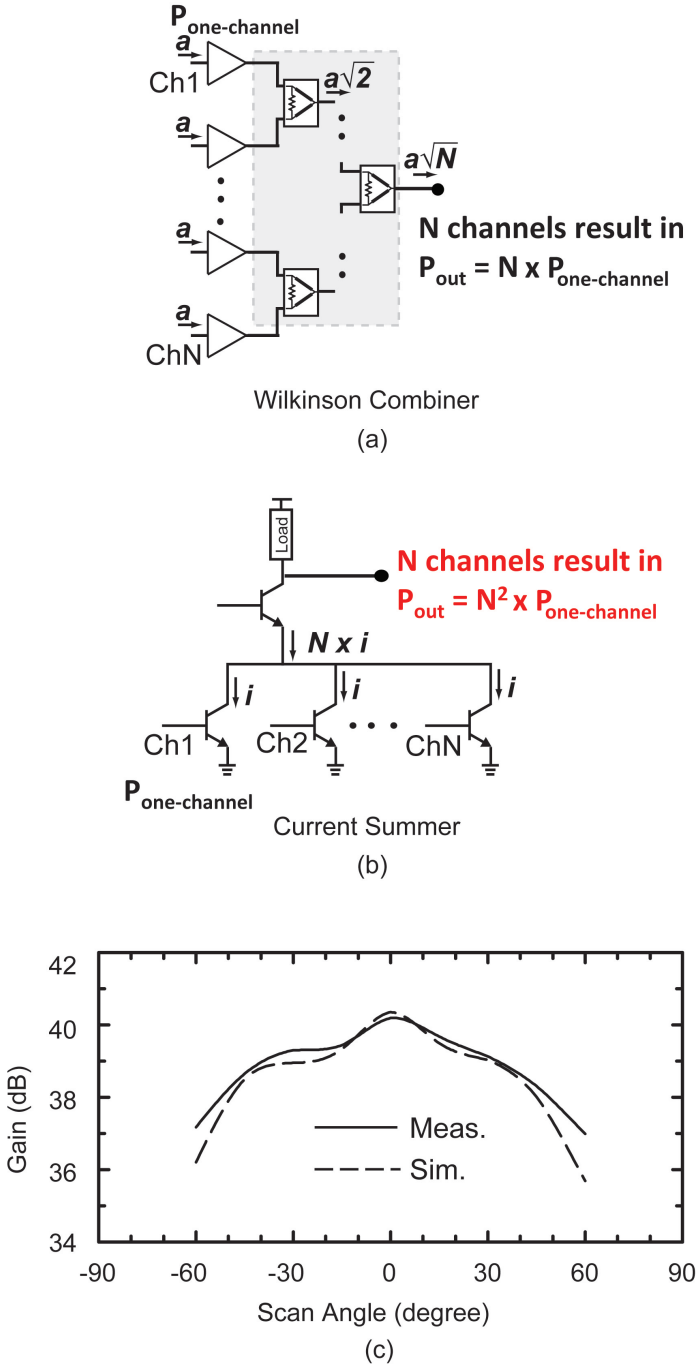


**Figure 3.12**: Phased array combiners: (a) Wilkinson based, (b) current-summing based. (c) Measured absolute gain vs. scan angle at 12 GHz.

Fig. 3.13 presents the normalized measured patterns at 11.4, 12 and 12.6 GHz superimposed on each other vs. frequency. It is clear that the non true-time delay transmission lines result in a slight "beam walk" at the 60° scan angles. Also, the high sidelobes are sidelobes of the 60° scanned beam. The phase settings were set at 12 GHz, and were kept identical at other frequencies, and therefore, these patterns represent the instantaneous scanning bandwidth performance. The phased array can operate over an instantaneous bandwidth of 1.2 GHz with no degradations.

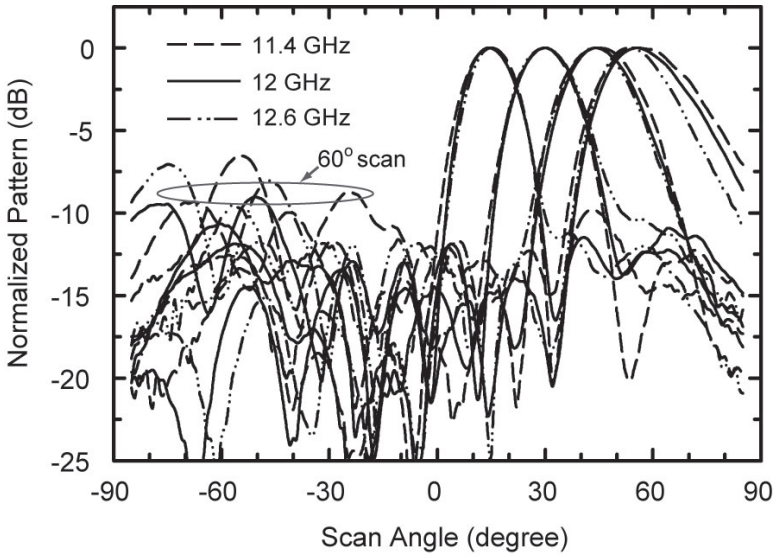


**Figure 3.13**: Measured patterns at 11.4, 12 and 12.6 GHz. The patterns are normalized and only positive beam scans are shown for ease of comparison.

### 3.3.3 Temperature Measurements

The silicon chip was also characterized vs. temperature in order to predict the phased array performance in various operation conditions. The chip contains 8 active phase shifters which are based on the vector modulator technique (Fig. 3.14a). In this case, the gain of the I and Q channels are controlled using 4-bit DACs, and are then summed together to generate 16 phase states in 22.5° steps. Since the quadrature all-pass network is passive and the amplifiers are biased using the same current source (PTAT [11]), the I and Q paths track each other vs. temperature. This results in virtually no change in the output phase vs. temperature. S-parameter measurements on the silicon chip indicate exactly this performance, as seen in Fig. 3.14b. The silicon solution with active phase shifters can therefore result in a very stable phase vs. temperature and minimal calibration vs. temperature.

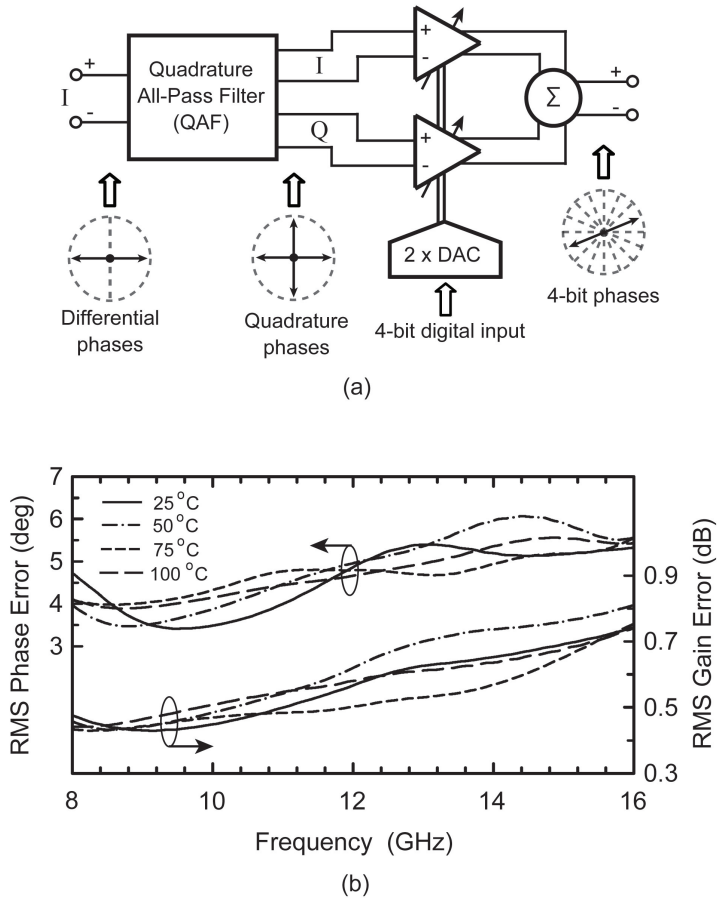


**Figure 3.14**: (a) Block diagram of the 4-bit active phase shifter, (b) measured RMS phase and gain error vs. temperature. An RMS error $< 6^\circ$ is maintained over temperature.

## 3.4 Conclusion

These results are, to the authors' knowledge, the first system level demonstration of an 8-element X/Ku-band phased array using a single silicon chip. Scanning up-to 60° is achieved. It is shown that chip-on-board packaging results in high isolation and <-10 dB returnloss even for 9 RF ports. In addition, true-time delay routing can be used for improved instantaneous bandwidth. In the future, GaAs LNAs will be placed at each antenna element so as to result in 1-1.5 dB NF. This design can be scaled to 8×8 or 16×16 elements using a "brick" ("card") architecture with minimal change in the layout.

Chapter 3 is mostly a reprint of the material as it appears in IEEE International Microwave Symposium Digest, 2010. Yusuf A. Atesal; Berke Cetinoneri; KwangJin Koh; Gabriel

M. Rebeiz. The dissertation author was the primary author of this material.

# Chapter 4

# Milimeter-Wave Wafer-Scale Silicon BiCMOS Power Amplifiers

## 4.1 Introduction

Millimeter-wave integrated circuits and systems based on CMOS and SiGe technologies are becoming much more complex with entire transceivers [64–72], large-element phased arrays [10, 11, 15, 16] and imaging systems [73–76] integrated on a single chip. Some systems are also coupled with high-efficiency on-chip antennas so as to eliminate the transition between the silicon chip and the external antenna and result in a system-on-chip solution [77–79]. Advanced CMOS and SiGe technologies deliver low noise amplifiers, high density of integration, and adequate phase noise at mm-waves but cannot deliver output powers greater than 15-20 dBm due to their low supply voltage requirements. One way to increase the RF power is to use on-chip power-combining based on Wilkinson couplers [27,29], transformers [30,31], or free-space (quasi-optical) techniques [32, 80] (Fig. 4.1). The Wilkinson and transformer-based techniques are adequate for 2-4 amplifiers but result in a large loss for 8-16 elements due to the limited Q of the on-chip passive components. On the other hand, free-space power combining has no limitation on the number of elements since the power combining is done in air and is 100% efficient (assuming no antenna losses, equal amplitude and phase distribution to the individual elements).

Quasi-optical power combining was developed in the 1980s and is based on two different topologies: The grid and the antenna approach. Grid designs use an inter-element spacing of 0.1-0.2$\lambda_0$ and consider the transistor arrays as being imbedded in impedance sheets [32].

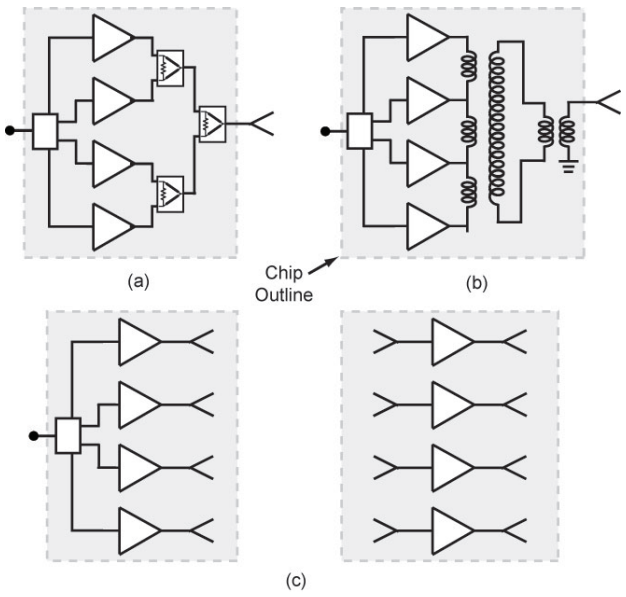


**Figure 4.1**: Block diagram of (a) Wilkinson, (b) transformer, and (c) quasi-optical power-combining techniques.

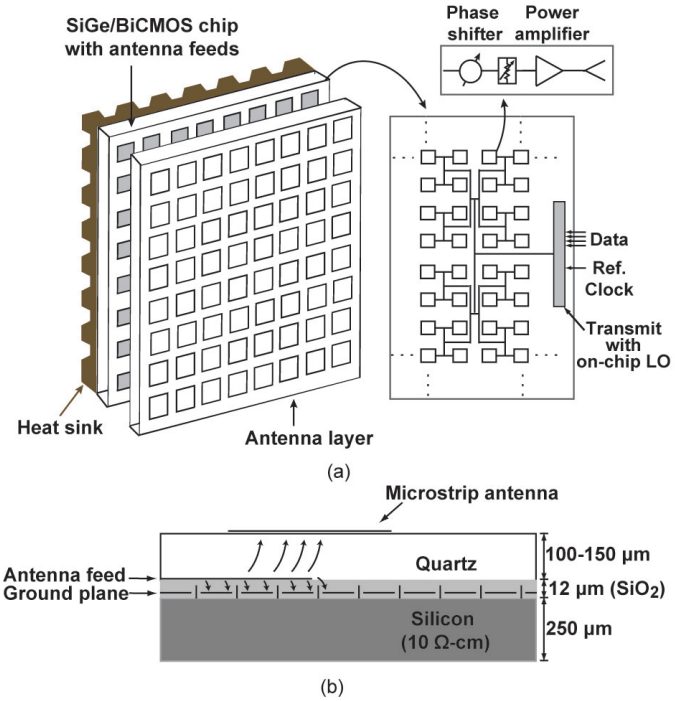


**Figure 4.2**: (a) Wafer-scale transmit phased array, and (b) electromagnetically-coupled on-chip microstrip antenna.

Antenna-based designs use an inter-element spacing of 0.5-1.0$\lambda_0$ and each amplifier/antenna element is designed taking into account the mutual coupling between the antennas [32–36]. In effect, a phased-array can be considered as a quasi-optical antenna combiner but with phase control on each element so as to scan the power-combined beam in different directions (this is valid for 0.5-0.65$\lambda_0$ spacing since the 1.0$\lambda_0$ spacing results in large grating lobes when the beam is scanned). Both the grid and the antenna approach have been demonstrated at Ka to W-band frequencies, and with excellent results using GaAs or InP components in a hybrid approach [33–42]. The antenna-based approach also allows that the RF feed distribution be planar, and is compatible with wafer-scale systems.

This chapter presents the first wafer-scale power amplifier/combiner in silicon technology. A power amplifier is placed at each on-chip antenna, and the RF distribution to the N×M elements is done using Wilkinson couplers and CPW transmission-lines. A high efficiency on-chip antenna ensures that most of the power generated by the N×M array is radiated to air. A 3×3 array is demonstrated in this work with an output power of 21-23 dBm at 90-98 GHz, and the design is scalable to 8x8 arrays generating watts of power at mm-wave frequencies. A heat sink is placed behind the silicon wafer and does not interfere with the RF distribution and radiation, thus ensuring low temperature operation (Fig. 4.2). In the future, this design can be extended to wafer-scale phased arrays (transmit or receive) using a phase shifter at each element together with the PA and/or LNA. Also, the design can be extended to 1-D or 2-D focal-plane imaging systems using a silicon receiver/radiometer unit at each on-chip antenna [81–83].

## 4.2 Design

### 4.2.1 3×3 Wafer-Scale Power Amplifier Array Silicon Chip

The 3×3 W-band power amplifier array is designed with 0.6$\lambda_0$ spacing between the array elements (Fig. 4.3). The input RF power is first divided into three different paths (rows) using a combination of unequal Wilkinson divider with 2:1 power ratio and a standard -3 dB Wilkinson divider. A driver amplifier (Gain = 15 dB, $P_{sat}$ = 13 dBm) is placed in each row and in turn feeds three power amplifier cells using another Wilkinson divider network. The driver design is identical to power amplifier design and is described in Section 4.2.2.

The Wilkinson dividers are realized using grounded CPW transmission lines; 12-10-12 $\mu$m (50 Ω), 15-6-15 $\mu$m (70 Ω) and 9-16-9 $\mu$m (40 Ω) over MQ ground plane, 9-13-9 $\mu$m (32Ω) over LY ground plane, and 20-4-20 $\mu$m (82 Ω) over M1 ground plane. The simulated

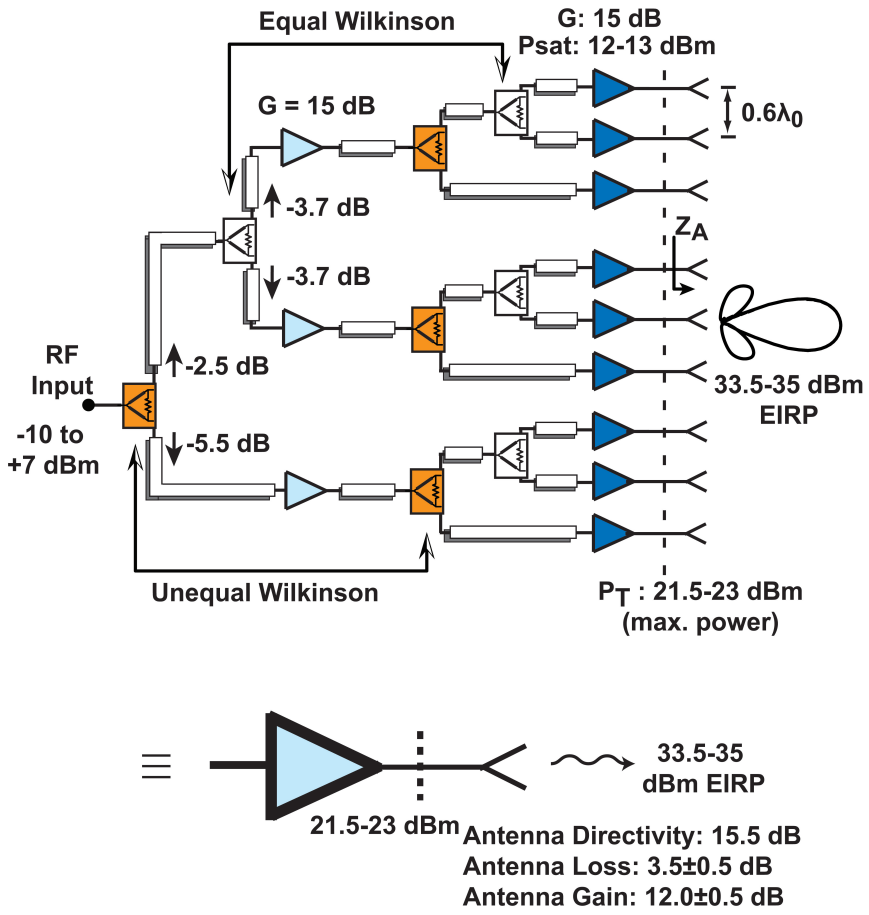


**Figure 4.3**: Block diagram of the W-band wafer-scale 3×3 power amplifier array.

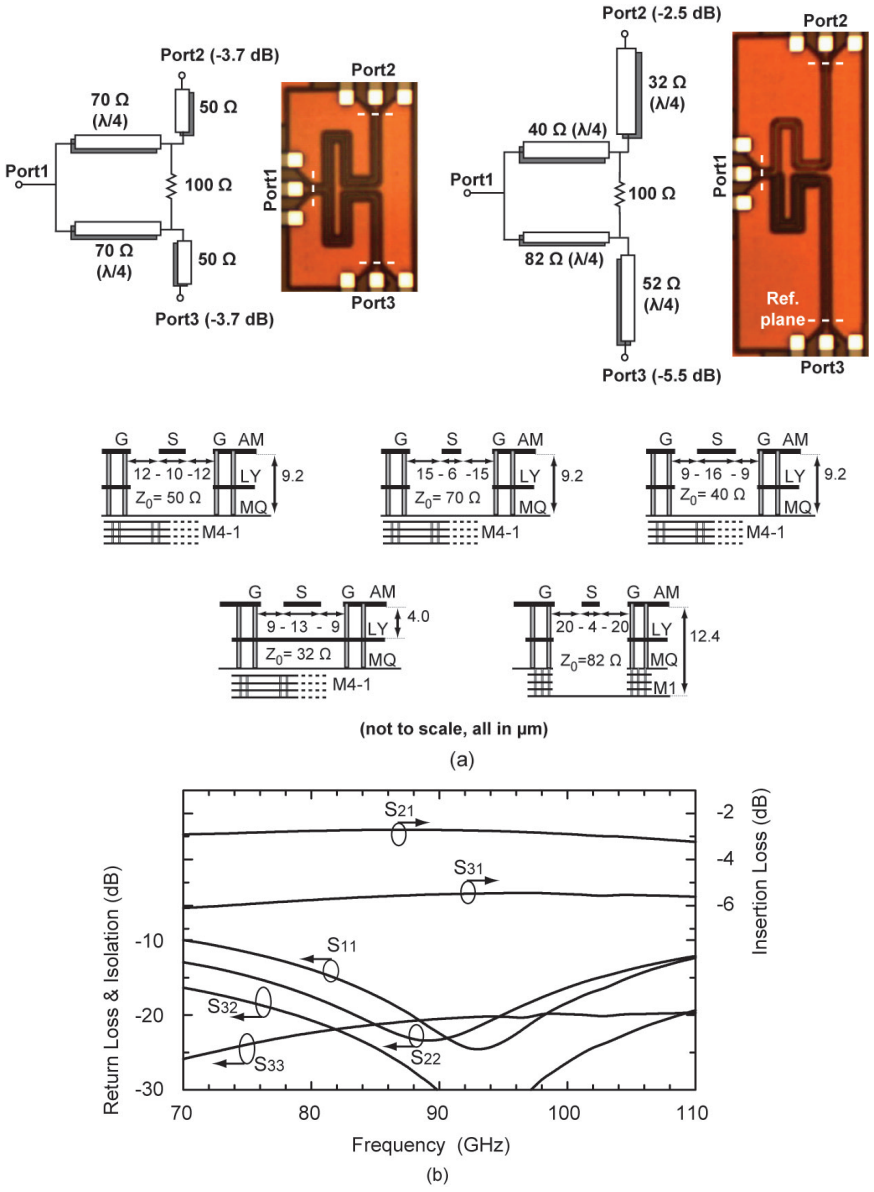


**Figure 4.4**: (a) Schematic diagram and microphotographs of the equal (-3.7 dB) and unequal (-2.5 dB / -5.5 dB) Wilkinson dividers with associated grounded CPW transmission lines ($Z_0 = 32 - 82\ \Omega$), (b) simulated S-parameters of the unequal Wilkinson divider.

$S_{21}$ and $S_{31}$ of the -3 dB Wilkinson divider are -3.7 dB at 94 GHz. On the other hand, the 2:1 Wilkinson divider results in an $S_{21}= -2.5$ dB and $S_{31}= -5.5$ dB at 94 GHz. The simulations include the CPW transmission line loss up to the reference planes shown in Fig. 4.4.

The layout of the 9-element silicon chip is presented in Fig. 4.5a,b, and the power amplifiers are located right at the microstrip antenna feed in order to minimize the large-signal interconnect loss. As seen in Fig. 4.3, paths have 2, 3, or even 4 Wilkinson dividers. However, the paths with less number of Wilkinson dividers have longer transmission lines in order to ensure equal insertion loss for all paths. The line lengths from the input port to each PA/antenna are also adjusted so as to have equal phase between all 9 elements, ensuring coherent summing in the spatial domain (Fig. 4.5c). The RF distribution on the silicon chip is realized using 50 $\Omega$ CPW lines with dimensions of 12-10-12 $\mu$m and a simulated loss of 0.65-0.75 dB/mm at 90-100 GHz. The total simulated line loss from the input port to each PA/antenna element (including both row and column distribution networks and Wilkinson dividers) is $\sim$9 dB at 94 GHz: $\sim$6 dB transmission line loss, and $\sim$ 3 dB Wilkinson loss. This loss does not include the 1:9 power division.

In order to facilitate the biasing of power amplifiers in a wafer-scale environment, amplifiers in each row (3 power amplifiers) are connected to a single Vcc and bias supply node (Fig. 4.5d). For measurement purposes, all of the DC bias pads are located on one side of the chip. The Vcc lines on each row are routed using stacked thick metal layers (AM and LY) with widths of 150-200 $\mu$m to minimize the line resistance and hence the voltage drop due to the high current levels (1.9 A for entire array). The base bias lines are routed using stacked low-level metals (M2-M4) taking into account the electro-migration design rules. In order to minimize substrate coupling and loss, a continuous ground plane (MQ) is used for both DC and RF, and is tied to large portions of the AM layer for the grounded CPW lines. Also, several 110 and 220 fF MIM capacitors are present between the Vcc supply lines and the ground plane for mm-wave decoupling. High value capacitor-resistor pairs are also used throughout the chip for RF decoupling at 0.5-20 GHz.

### 4.2.2 Power Amplifier Unit-Cell Design

A 4-stage power amplifier consisting of common emitter stages is designed using the IBM 8HP BiCMOS process with a bipolar ft of 200 GHz, and 7 metal layers including 4 $\mu$m and 1.25 $\mu$m thick aluminum top layers (Fig. 4.6). The transistors are biased in class A operation, and all biasing circuits, wideband capacitor bypass arrays, input, output, and interstage matching

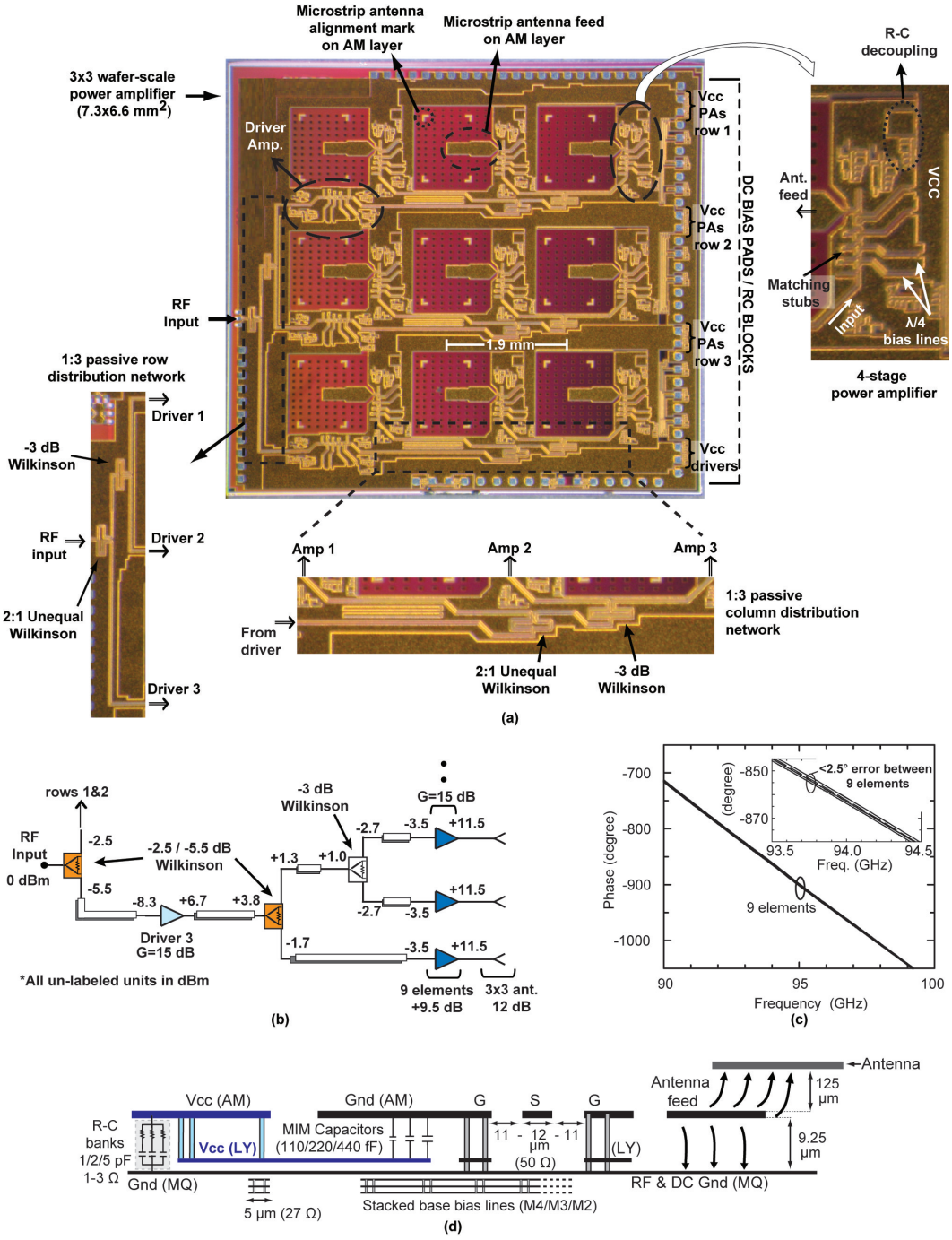


**Figure 4.5**: (a) Detailed microphotograph of the 3x3 power amplifier array chip without antennas ($7.3\times6.6$ mm$^2$ including all pads), (b) power division and amplification throughout the array in a small-signal regime, (c) simulated phase from the input port to the 9 antenna ports, (d) above silicon metal layers (M2-AM) with grounded CPW and microstrip lines, decoupling capacitors, and microstrip antenna feed.

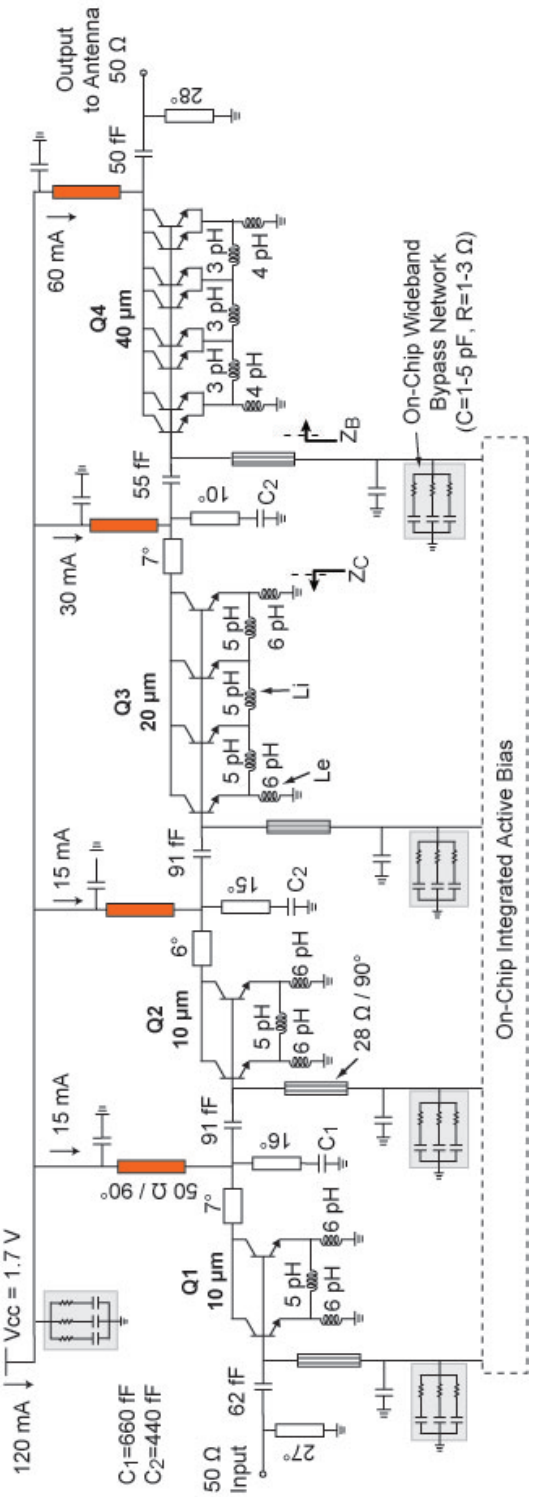


**Figure 4.6**: Circuit schematic of the 4-stage W-band power amplifier. Electrical lengths are given at 94 GHz and all non-labeled shunt capacitors are 440 fF.

networks are integrated on-chip. A power cell size of $5\times0.13$ $\mu m^2$ is used with a quiescent current of 10-12 mA/$\mu m^2$ for peak ft. The power cells are standard IBM kit designs with a single emitter finger, dual collector and base fingers (C-B-E-B-C), and each cell is surrounded by a deep-trench isolation ring. The first two gain stages consist of 2 aggregated cells ($10\times0.13$ $\mu m^2$), while the third and fourth stages are made from 4 ($20\times0.13$ $\mu m^2$) and 8 ($40\times0.13$ $\mu m^2$) cells, respectively. Scaling in the device size ensures that the large signal characteristics are limited by the last stage. The transistor collector nodes are connected to the matching networks using short sections of CPW lines (6°-7°, $Z_0$=10-15Ω). The emitters are directly connected to the ground plane on the top metal layer (AM) using via holes, resulting in 3-5 pH inductance to ground ($L_e$, $L_i$, Sonnet simulation [56]).

The collector and base biasing is done using $\lambda$/4 quarter-wave transmission lines followed by shunt 440 fF metal-insulator-metal (MIM) capacitors, operating near resonance at 94 GHz and providing an very low impedance at 85-105 GHz. The collector $\lambda$/4 sections (50 Ω, 90°) and matching stubs are realized using 11-8-11 $\mu$m grounded CPW lines with a Q of 11 at 94 GHz. The base bias feeds (28 Ω, 90°) are implemented beneath the RF ground shield (MQ layer) using low-Q quarter-wave microstrip lines (width = 5 $\mu$m, Q $\sim$ 3) created from stacked thin-metal interconnect layers (M2, M3 and M4 as signal, MQ as ground plane) and result in wideband RF chokes.

The $\lambda$/4 biasing scheme isolates the RF transistor and matching networks from biasing and supply de-coupling circuitry effects (self-resonances, inductance on Vcc lines, etc.). The base impedance seen by each stage ($Q_{1-4}$) is 300 Ω at DC and 15-20 Ω at W-band resulting in an emitter breakdown voltage of 4.2 V, a factor of 2.5× improvement over a standard design (technology $BV_{ceo}$ = 1.7 V) [84]. A broadband low impedance (low-Q) network consisting of different value capacitor-resistor pairs with C=1-10 pH and R=1-3 Ω is present after the $\lambda$/4 base bias lines, and also on the Vcc line (collector terminals). The resistor and capacitor values are adjusted so as to provide stability to each stage at all frequencies. Fig. 4.7 presents the simulated stability factor (k-factor) with and without the R-C banks.

The interstage matching networks are synthesized using shunt stubs and 50-91 fF series capacitors (Fig. 4.8a). The stubs are implemented using a short CPW transmission line ($Z_0$=50 Ω, Q=11 at 94 GHz) in series with an MIM capacitor, resulting in an equivalent 10-20 pH shunt inductor at W-band and an open circuit at DC. In order to prevent the stages from resonating together at a specific frequency, capacitors with different values ($C_1$, $C_2$) are used with the shunt stubs. The shorted matching stubs at the RF input and output ports provide ESD

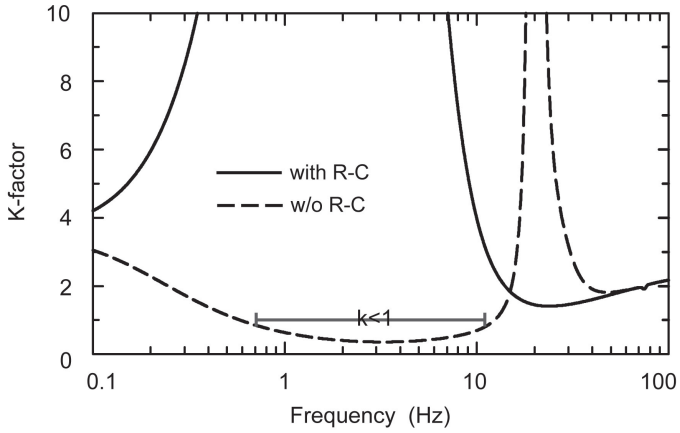


**Figure 4.7**: Simulated stability factor of the 4-stage power amplifier.

protection without performance penalties.

IBM MIM capacitors (1 fF/$\mu$m$^2$) are used for large capacitance values ($>$ 91 fF), while capacitors with $<$ 91 fF values are realized using metal-oxide-metal (MOM) capacitors. The MOM capacitors are implemented with MQ and M3 layers as one plate, and the M4 layer as the other plate, resulting in sizes of 20$\times$22 $\mu$m$^2$ to 25$\times$30 $\mu$m$^2$ and Q of 30-40 at 94 GHz (Fig. 4.8b). Deep silicon trenches are placed beneath the MOM capacitors to reduce the substrate coupling and maximize the quality factor.

All transmission lines, interconnects and MOM capacitors are modeled using a full-wave electromagnetic simulator, Sonnet [56], and taking into account the quartz substrate which

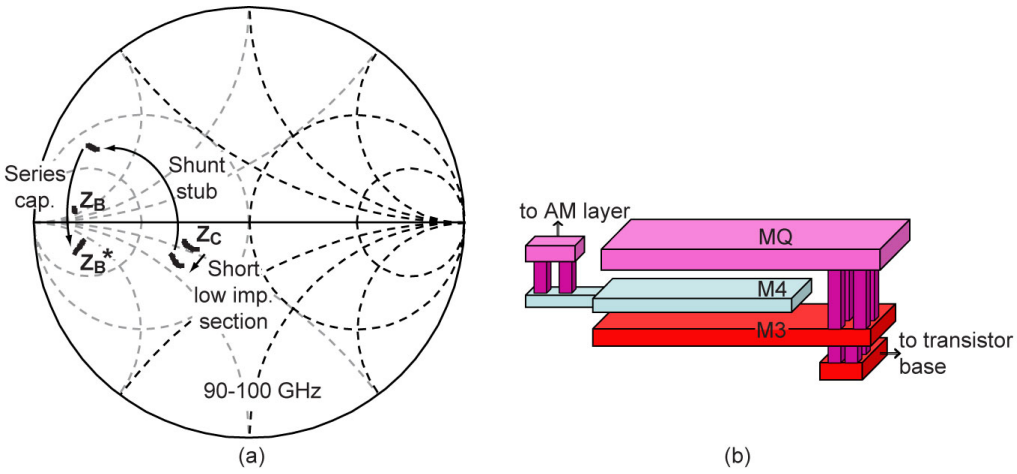


**Figure 4.8**: (a) Design of the interstage matching network between stage-3 (Q3) and stage-4 (Q4) at 90-100 GHz, (b) custom metal-oxide-metal (MOM) capacitor design.

will be placed on top of the silicon chip. Load-pull data is not available for the standard-cell transistors, but the wideband implementation of this design makes the power amplifier robust to modeling inaccuracies and process variations. Metal line widths and via arrays throughout the silicon chip are sized to be electromigration compliant and conform to the process reliability guidelines for 100 °C operation and 100,000 power-on hours.

Each common-emitter stage provides 3-5 dB of small-signal gain, resulting in a simulated overall gain of 14$\pm$2 dB at 90-99 GHz under nominal bias conditions (at 1.7 V, 120 mA). The simulated input and output return loss are $<$ -10 dB from 80-98 GHz. The power amplifier results in a saturated output power ($P_{sat}$) of 13.0 dBm at 94 GHz with a power-added-efficiency of 7.2% at 1.7 V, 160 mA biasing conditions. The amplifier can deliver $\sim$14 dBm of $P_{sat}$ at bias conditions of 2.0 V, 160 mA.

### 4.2.3 3×3 Antenna Array

Fig. 4.9a presents the layout of the 94 GHz electromagnetically-coupled on-chip microstrip antenna [77]. The microstrip antenna is integrated on a 125 $\mu$m quartz substrate ($\epsilon_r$= 3.8) placed on top of silicon RFIC. No via holes are used, and the feed between the silicon RFIC top-metal layer (AM layer) and the microstrip antenna is achieved by fringing-field coupling. The global ground plane (MQ) acts as the ground plane for the microstrip antenna and the feed-probe, and isolates the antenna from the lossy silicon substrate. Also, 40×40 $\mu$m metal squares are introduced on the LY layer to satisfy the IBM8HP design metal density rules. These metal squares are connected to the substrate using small reversed biased diodes.

The microstrip antenna is characterized on-chip, and the measured input return loss ($S_{11}$) agrees well with simulations with a -10 dB bandwidth of 91.7-98.5 GHz (Fig. 4.9c). The simulated directivity for a single element is D$\approx$6 dB and the simulated gain is $G$ =3$\pm$0.7 dB at 91-99 GHz ($G$ =$\epsilon D$, efficiency $\epsilon$=50$\pm$8%). It is hard to measure accurately on-chip antennas with low gain due to the wide radiation patterns and scattering from the measurement setup. An antenna gain of 2.5$\pm$1 dB is measured at 91-98 GHz, and corresponds to an antenna efficiency of 45$\pm$10% (Fig. 4.9d).

A 3×3 antenna array with 0.6$\lambda_0$ spacing at 94 GHz is fabricated on a single quartz substrate (Fig. 4.9b). The directivity is calculated using *Array Factor*×*Normalized Element Factor* technique [85], and is 15.3-15.6 dB at 90-100 GHz. The 3×3 gain is obtained by multiplying the array directivity with the microstrip antenna efficiency (*Array Factor*×*Element Gain*) and is 12$\pm$1 dB at 91-99 GHz.

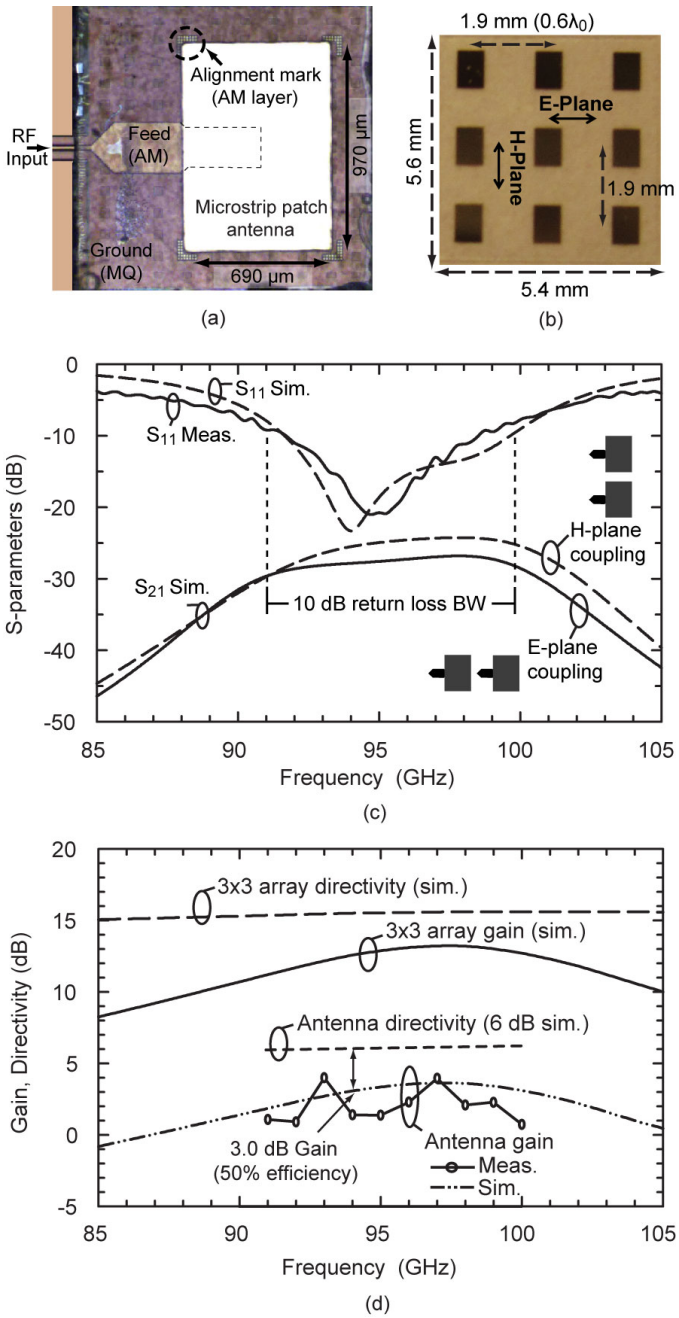


**Figure 4.9**: Micrograph of (a) electromagnetically-coupled microstrip patch antenna on a silicon chip, (b) quartz substrate with 3×3 antenna array, (c) input return loss on the microstrip antenna and the simulated E-plane and H-plane coupling between antenna elements, and (d) simulated (and measured) directivity and gain of a single antenna and the 3×3 antenna array.

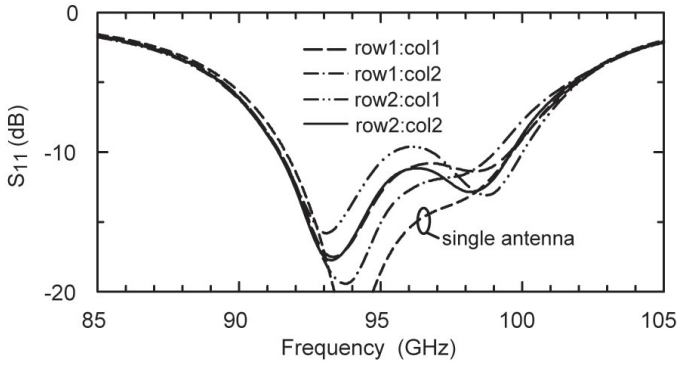


**Figure 4.10**: Simulated input return loss of four antennas in the 3x3 array environment including the mutual coupling between the elements. The other antennas have identical response due to symmetry.

The mutual coupling between the antennas is simulated using a 3-D electromagnetic simulator, HFSS [58], and is $<$ -25 dB and $<$ -27 dB at 91-100 GHz for H-plane and E-plane, respectively (Fig. 4.9c). The active antenna impedance in a 3$\times$3 array environment is calculated using:

$$Z_{\mathrm{A}} = \mathrm{Z}_{11} + (\frac{\mathrm{I}_2}{\mathrm{I}_1})\mathrm{Z}_{12} + (\frac{\mathrm{I}_3}{\mathrm{I}_1})\mathrm{Z}_{13} + ... + (\frac{\mathrm{I}_9}{\mathrm{I}_1})\mathrm{Z}_{19}, \tag{4.1}$$

$$I_1 = \mathrm{I}_2 = .. = \mathrm{I}_9$$

Fig. 4.10 presents the input return loss for the nine antennas in a 3$\times$3 array environment. The low mutual coupling between the antennas have a negligible effect on the active antenna impedance, which is important for wafer-scale power amplifier design.

### 4.2.4 3$\times$3 Power Amplifier Array

The 3$\times$3 silicon chip with the 9 power amplifiers results in a total simulated output power of 22.5 dBm at the antenna ports ($\mathrm{P_{on-chip}}$) at 94 GHz when the amplifiers are saturated (13 dBm + 9.5 dB). The small signal electronic power gain (total generated power ($\mathrm{P_{on-chip}}$) / input power ($\mathrm{P_{in}}$)) is 21 dB at 94 GHz: 15 dB driver gain, 15 dB power amplifier gain, and 9 dB CPW line and Wilkinson loss. The 3$\times$3 array has an equivalent isotropic radiated power (EIRP=$\mathrm{P_{on-chip}G_T}$) of 34.5 dBm at 94 GHz (22.5 dBm + 12 dB). The chip consumes 1.9 A from a 1.7 V supply and the simulated power-added-efficiency (PAE) is $\sim$5.8%. The simulated input return loss is $>$ 10 dB at 82-120 GHz. The chip size is 7.3 $\times$ 6.6 mm$^2$ including RF and DC pads.

## 4.3 Measurements

Three different W-band amplifiers were fabricated using the IBM 8HP process: A test amplifier chip with input and output CPW probes, a test amplifier with on-chip microstrip antenna, and a 3×3 amplifier wafer-scale array with on-chip microstrip antennas. Small-signal testing is performed with Agilent network analyzer (PNA E8361A) with a millimeter-wave controller (N5260A) and two 75-110 GHz extenders and a 1 mm coaxial system. The RF pad transition losses are not de-embedded from the results. The large-signal measurements are done using WR-10 waveguide components with transitions to the 1 mm coaxial probes (GSG 100$\mu$m pitch), mechanically-tuned Gunn-diode oscillators and variable attenuators, and the measurements were limited by the available source power above 98 GHz and below 88 GHz.

### 4.3.1 On-Chip Measurements of Test Amplifier with CPW Input & Output RF-Pads

The microphotograph of fabricated test power amplifier together with small-signal S-parameters is shown in Fig. 4.12a, and the amplifier results in a peak gain of 15.0 dB at 89-94 GHz, a 3-dB bandwidth of 85.5-101.5 GHz and $>$ 10 dB gain from 83-103 GHz, agreeing very well with simulations. Both input and output return loss are $<$ -10 dB at 80-100 GHz, and the measured reverse isolation ($S_{12}$) is $<$ -40 dB up to 110 GHz (not shown). The measured output $P_{1dB}$ and $P_{sat}$ at 94 GHz are 10 dBm and 13 dBm, respectively, and the measured power-added efficiency is 7.0% at 94 GHz (Fig. 4.12b). Fig. 4.12c presents the measured Psat versus collector voltage, and the test amplifier maintains a Pout $>$ 12 dBm from 1.6-2.1 V. The amplifier was tested using CPW probes and SOLT calibration, and the measurements include pad-losses.

### 4.3.2 Test Amplifier with On-Chip Microstrip Antenna

The W-band amplifier/antenna array is then measured using a far-field test set-up (Fig. 4.13). The silicon chip is placed on a standard W-band probe station and is fed using a GSG probe. A W-band standard gain horn antenna with a gain, $G_R$, of 22.0-23.0 dB at 85-105 GHz (22.9 dB at 94 GHz) is placed at $R = 25$ cm from the silicon chip (far-field) and the RF power is measured vs. frequency using an Agilent W8486A power sensor. RF absorbers are used around wafer-scale chip and the W-band horn so as to reduce the standing waves.

The amplifier with the on-chip microstrip antenna results in a wideband output power with $P_t t \times G_t > 10$ dBm from 88 GHz to ∼98 GHz, with a peak of 14.6 dBm at 92 GHz (Fig.

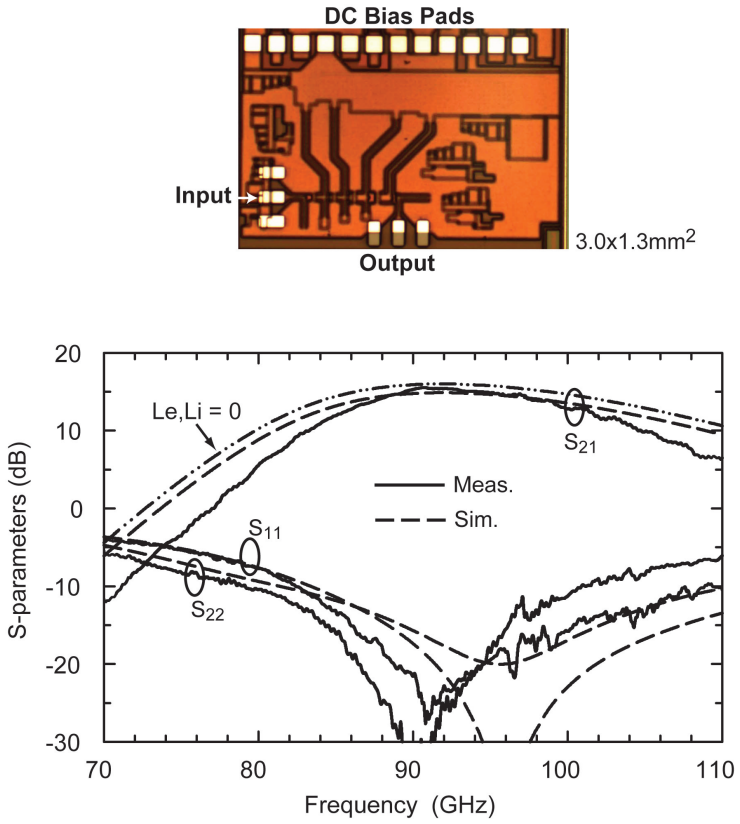


**Figure 4.11**: Measured on-chip S-parameters of the power amplifier unit cell.

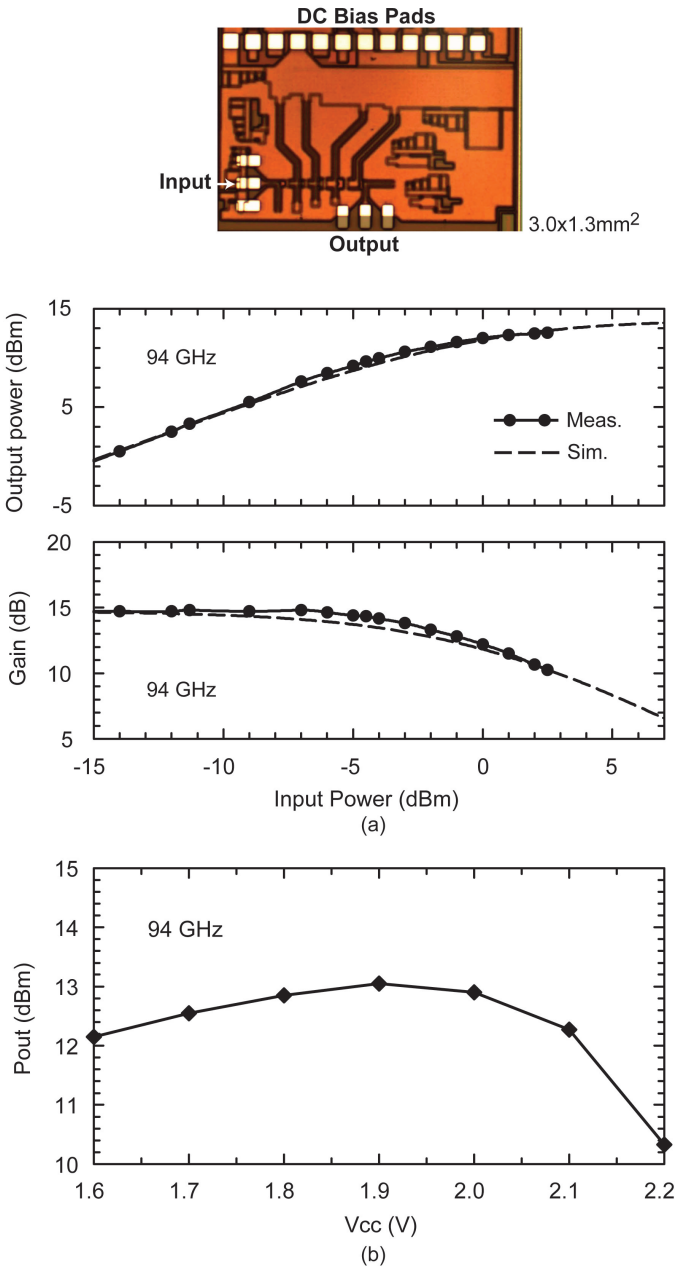


**Figure 4.12**: Measured unit-cell on-chip (a) output power and gain versus input power at 94 GHz, and (b) measured Psat vs. supply voltage.

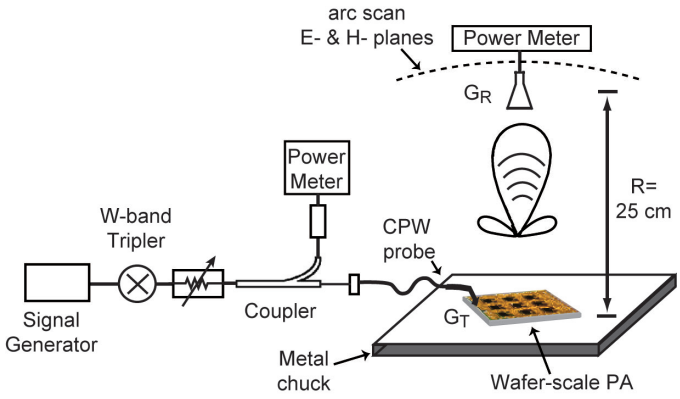


**Figure 4.13**: W-band EIRP and pattern measurement setup.

4.14a). The measured output power (Pt) from the on-chip antenna-amplifier also agrees with that of the test amplifier over a broad frequency range (Fig. 4.14b).

### 4.3.3 3×3 Power Amplifier Array with On-Chip Antennas

The fabricated quartz substrate with a 3×3 antenna array is placed on top of the 3×3 power amplifier chip using a dot of glue (Cyanoacrylate) at the corners (Fig. 4.15). Fig. 4.16 presents the measured input return loss ($S_{11}$) using probe-tip SOLT and on-chip TRL (through-reflect-line) calibration techniques. Both result in nearly same $S_{11}$ with -10 dB bandwidth of 85-104 GHz. This indicates that the GSG pad capacitance was well compensated using on-chip tapered grounded CPW transition (see [86] for details).

The setup shown in Fig. 4.13 with a custom circular arm is used over the probe station for pattern measurements, and the measurements were limited to ±40° in the E-plane and ±60° in the H-plane. The measured E and H plane patterns at 94 GHz are shown in Fig. 4.17a,b and are in excellent agrement with simulations with a measured half-power-beam-width (HPBW) of 28° in both planes and sidelobe level of -13 dB at 55° in the H-plane. The E-/H-plane patterns are also measured at 90 GHz and 98 GHz, and the HPBW is 35° at 90 GHz and 24° at 98 GHz, agreeing well with simulations (Fig. 4.17c-e). The measured cross-polarization levels are <-25 dB in the E- and H-planes at 90-98 GHz. These patterns clearly show that all 9 elements are radiating in phase in a single mode, and coherent summing is achieved in the spatial domain.

The Friis transmission equation between two antennas ($G_{\mathrm{T}}$, $G_{\mathrm{R}}$) separated by a distance $R$ is [85]:

$$\frac{P_{\mathrm{R}}}{P_{\mathrm{on-chip}}} = (\frac{\lambda_0}{4\pi R})^2 G_{\mathrm{T}}\mathrm{G_R}, \quad \frac{\mathrm{P_R}}{\mathrm{P_{radiated}}} = (\frac{\lambda_0}{4\pi \mathrm{R}})^2 \mathrm{D_T G_R} \tag{4.2}$$

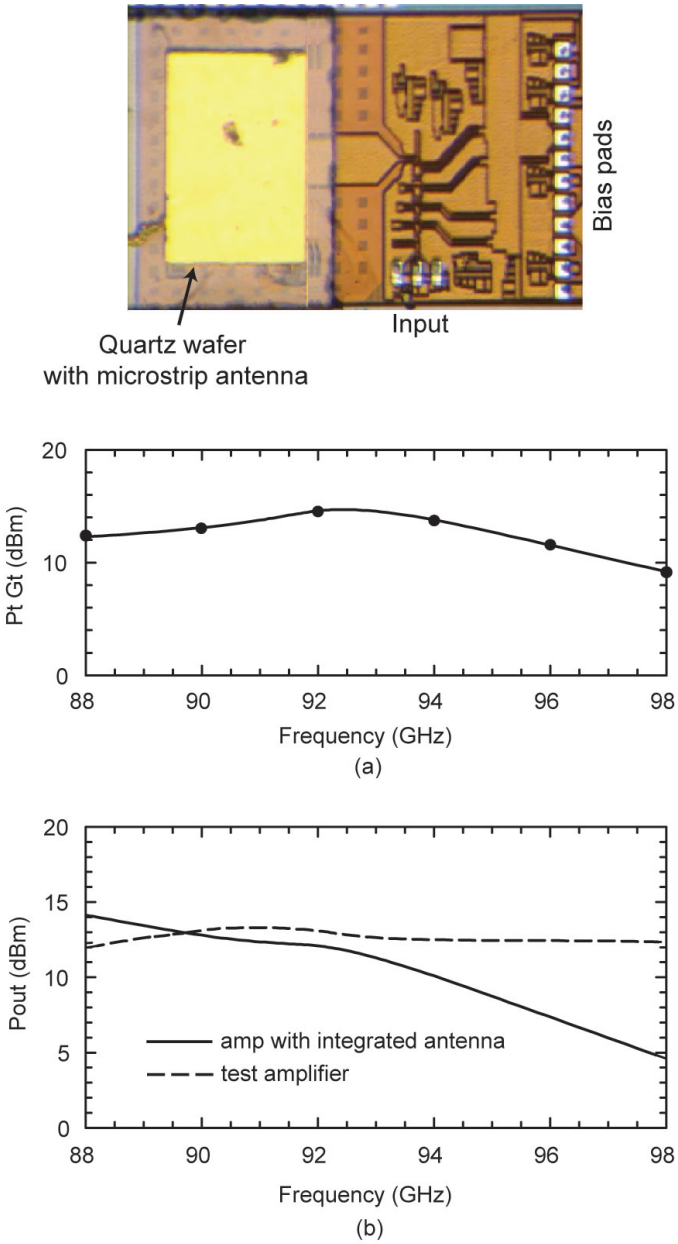


**Figure 4.14**: (a) Measured EIRP (PtGt) for the amplifier with on-chip antenna. (b) Comparison of measured Pout from the test amplifier and Pout of the amplifier with the on-chip antenna.

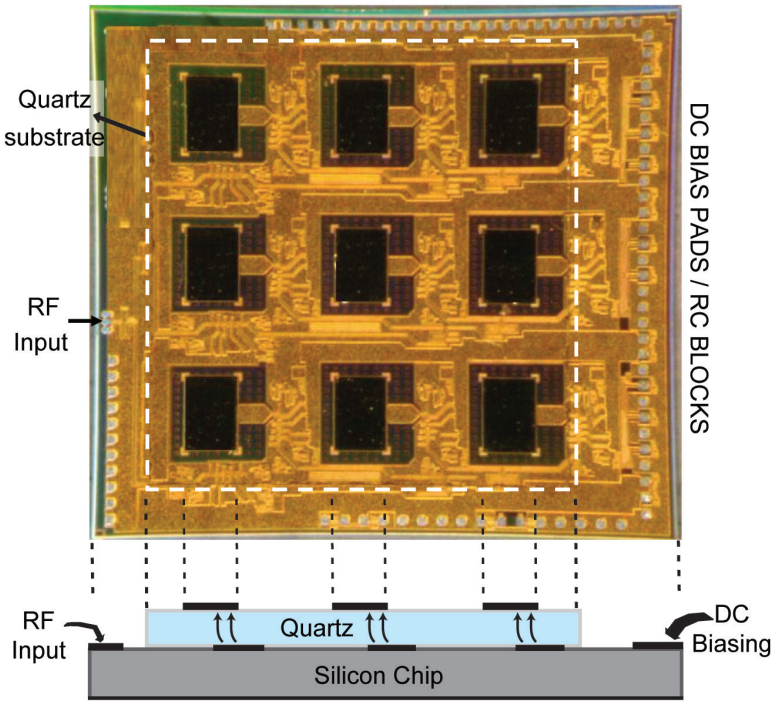


**Figure 4.15**: Microphotograph of the wafer-scale power amplifier array (7.3×6.6 mm$^2$). A quartz substrate with a 3×3 antenna array is placed on top of the silicon chip.

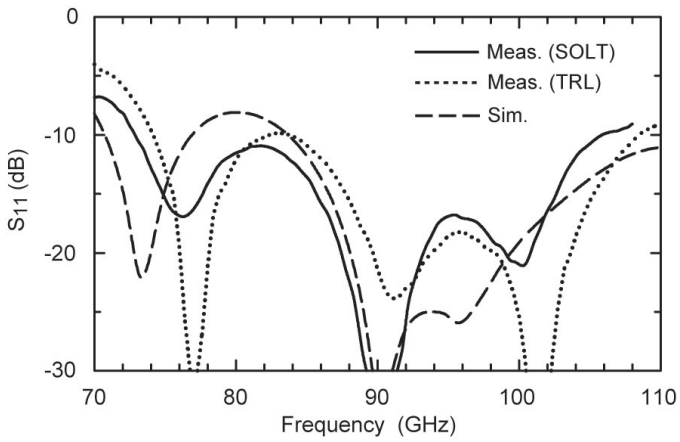


**Figure 4.16**: Measured input return loss of the wafer-scale 3×3 array.

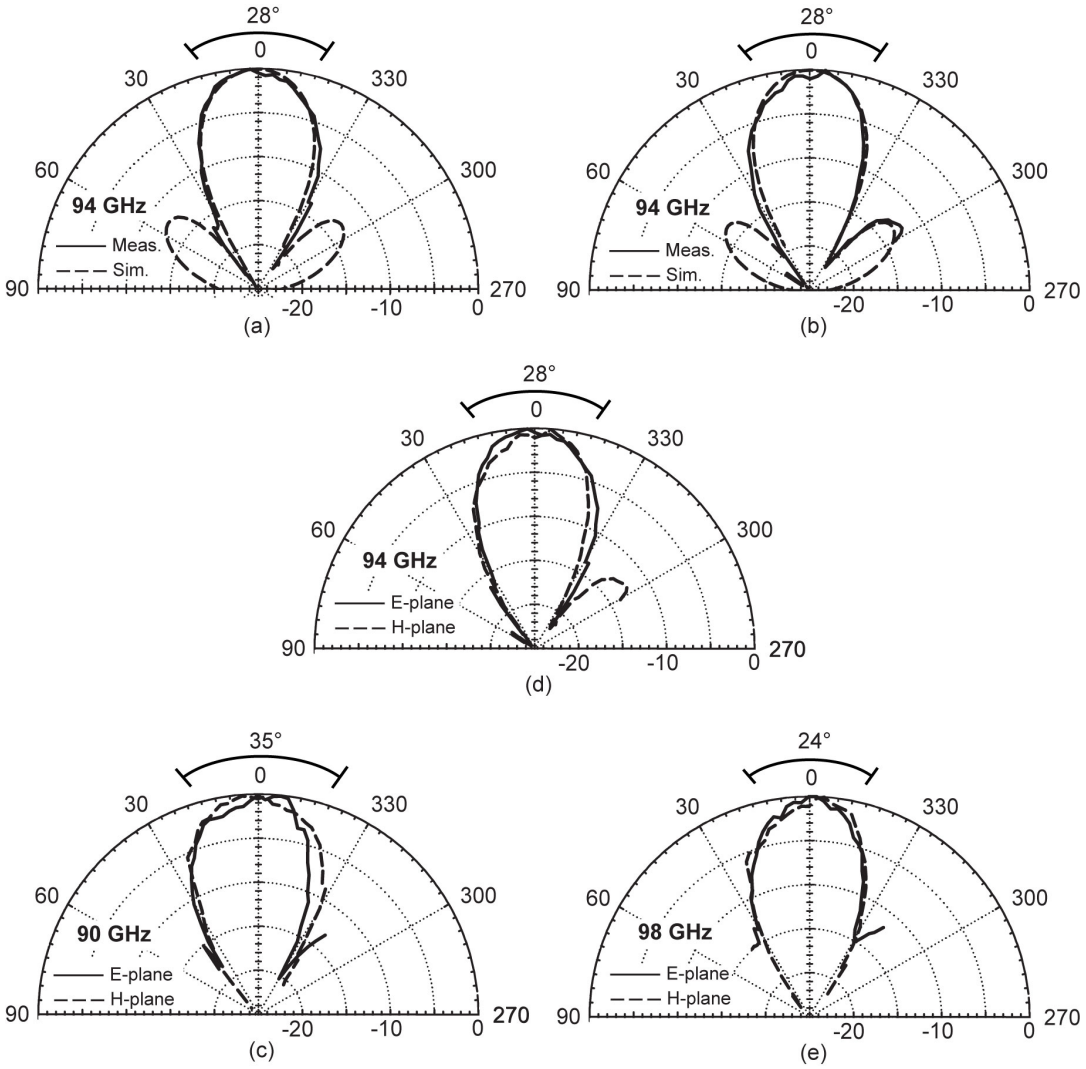


**Figure 4.17**: Measured and simulated array patterns at 94 GHz (a) E-plane, (b) H-plane. Measured E-/H-plane patterns at (c) 90 GHz, (d) 94 GHz (d) 98 GHz. The 3-dB beamwidth angle is also shown.

where $P_{\rm R}$ is the received power at the standard gain horn, and $G_{\rm T}$ (12±0.5dB),$D_{\rm T}$(15.5 dB) are the gain and directivity of the 3×3 microstrip antenna array. The equivalent isotropic radiated power (EIRP) is defined as:

$$EIRP = (\frac{P_{\rm R}}{G_{\rm R}})(\frac{4\pi R}{\lambda_0})^2 = P_{\rm on-chip}{\rm G_T} = {\rm P_{Radiatied}D_T}, \tag{4.3}$$

$$\text{and } P_{\rm on-chip} = \frac{\rm EIRP}{\rm G_T}, \quad {\rm P_{radiated}} = \frac{\rm EIRP}{\rm D_T}$$

Note that only the EIRP can be determined with accuracy using (4.3) since $P_{\rm R}$, $G_{\rm R}$, and $R$ are known quantities. Measurements of any on-chip power values ($P_{\rm on-chip}$) values therefore necessarily include any errors in $G_{\rm T}$.

The EIRP for two different 3×3 arrays is measured at 94 GHz with a bias voltage of 1.7-2.0 V (1.60 - 1.66 A), and a maximum EIRP of 33.5-35 dBm is achieved (Fig. 4.18a). The total on-chip power from the wafer-scale array, $\rm P_{on-chip}$, is 21.5-23 dBm at 94 GHz (33.5-35 dBm − 12 dB), and the total radiated power is 18-19.5 dBm (33.5-35 dBm − 15.5 dB). The measured maximum power-added-efficiency is 5.9%.

The free-space small-signal gain can be defined as:

$$Free - Space\, Gain = \frac{EIRP}{P_{\rm in}}, \tag{4.4}$$

where $\rm P_{in}$ is the power at the input port of the wafer-scale array. The measured free-space small-signal gain is 33 dB at 94 GHz and agrees well with simulations (Fig. 4.18a). The gain is divided as: 15 dB driver amplifier, 15 dB power amplifier, 12 dB antenna gain ($G_{\rm T}$), 9 dB CPW line and Wilkinson loss. The measured on-chip small-signal gain, $\rm P_{on-chip}/P_{in}$, is 21 dB (33 dB − 12 dB).

Fig. 4.19 presents the measured maximum EIRP versus frequency for the two different wafers. A measured EIRP of 33-35 dBm is obtained at 90-98 GHz with a corresponding total on-chip power of 21-23 dBm and total radiated power of 17.5-19.5 dBm. At 99 GHz, the EIRP is 32 dBm for all measurements and is limited by the available input power from the Gunn-diode source. The EIRP measurements agree well with simulations. The results are summarized in Table I.

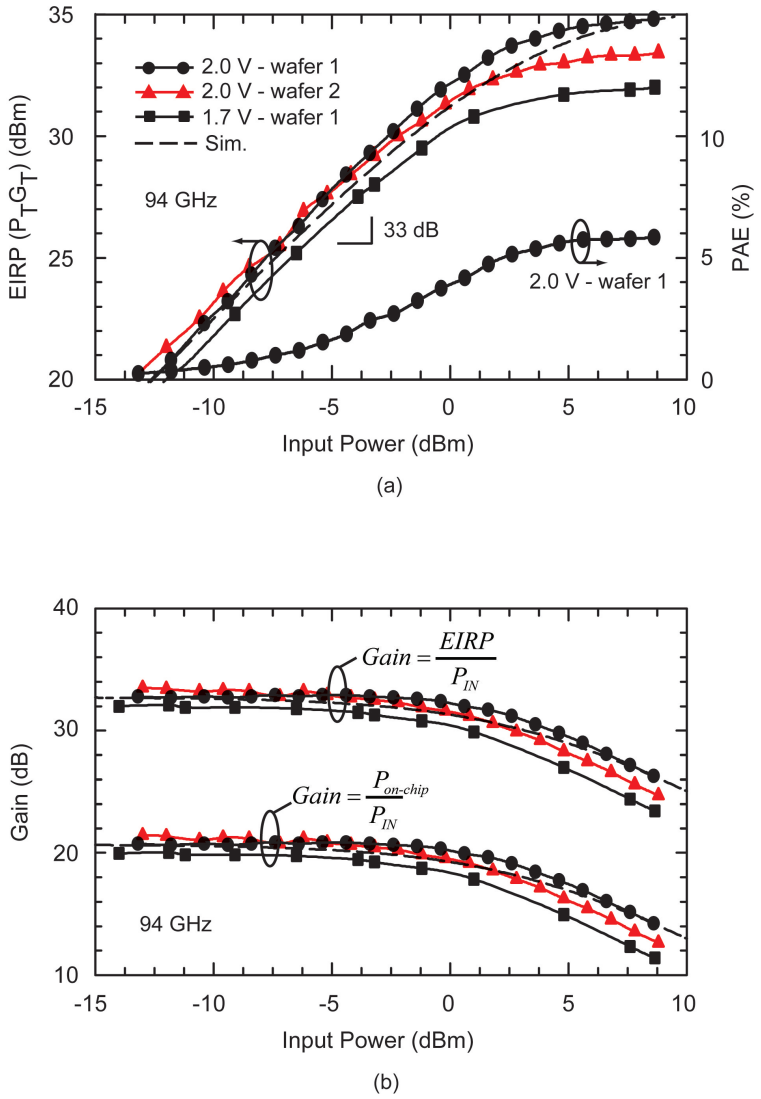


**Figure 4.18**: (a) Measured EIRP versus input power at 94 GHz, and (b) measured quasi-optical gain at 94 GHz. Measurements are shown for two different wafers.

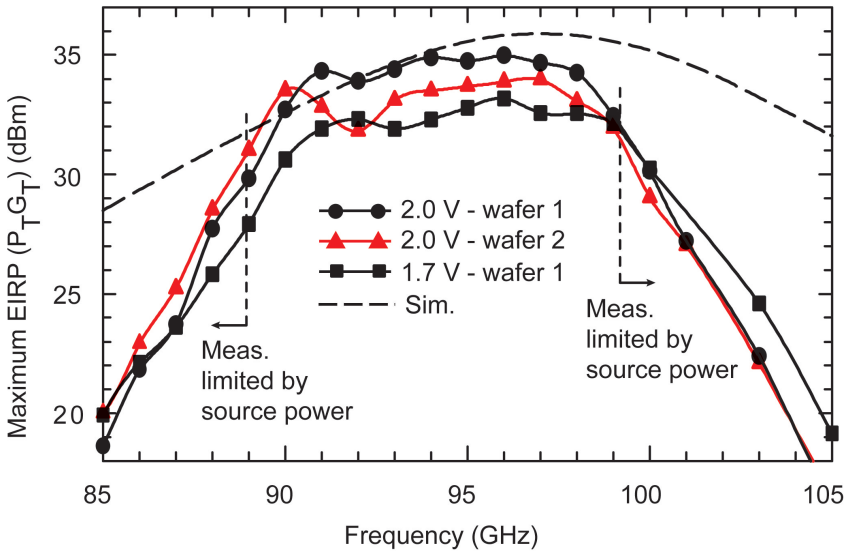


**Figure 4.19**: Measured maximum EIRP versus frequency. Measurements are shown for two different wafers.

## 4.4 Discussion and Conclusion

Table II and III compares this work with the state-of-the-art in power combining techniques using silicon and III-V transistors. Note that the 3×3 wafer-scale array shows the highest frequency operation so-far, but the power levels and the number of elements used in the III-V implementations are much higher, especially in the 30-44 GHz range.

The wafer-scale 3×3 array has a chip area of 48 mm$^2$ which is large knowing that it generates 200 mW of on-chip RF power (and 90 mW of radiated power). The advantage of wafer-scale integration – other than having an antenna directly integrated on-chip and eliminating the chip-to-board mm-wave transitions – lies in its scalability to large number of elements. A 8×8 array spaced at 0.55$\lambda_0$ at 94 GHz and with a 25 mW power amplifier at each element results in an output power of 1.6 W, an antenna directivity of 23.9 dB (a half-power beamwidth of 11.5°), an antenna gain of ∼20.5 dB, and an EIRP of 176 W (22.5 dBW), all in a 14×14 mm$^2$ of area. The 8×8 array would result in millimeter-wave transmitters that are competitive with the best III-V solutions. Furthermore, phase and amplitude control can be placed on each element leading to a phased array with controllable sidelobe levels. The design is also applicable to a variety of systems, such as focal plane imaging arrays (active and passive), and radars and

**Table 4.1**: Performance Summary

| **Single PA Element** | |
|---|---|
| Gain | 15 dB |
| Output power | 13.0 dBm @ 94 GHz |
| PAE | 7.0% |
| Vcc & Idc | 1.7 V, 120 mA |
| **3x3 Wafer-Scale Array** | |
| EIRP | 33-35 dBm @ 90-98 GHz |
| $P_{on-chip}$ | 21-23 dBm @ 90-98 GHz |
| $P_{radiated}$ | 17.5-19.5 dBm @ 90-98 GHz |
| $S_{11}$ | $<$-10 dB @ 84-105 GHz |
| Bias Conditions | 1.66 mA @ 2 V |
| $PAE_{on-chip}$, $PAE_{radiated}$ | 5.0-5.8%, 2.25-2.6% |
| Power Comb. Efficiency | 100% (45%, incl. ant. loss) |

**Table 4.2**: Performance Summary compared to single chips

| **Freq. (GHz)** | **Techn.** | **Topology** | **Gain (dB)** | **Psat (dBm)** | **PAE (%)** | **Area ($mm^2$)** | **Ref.** |
|---|---|---|---|---|---|---|---|
| 90-98 | SiGe 0.13 $\mu$m | Quasi-optical power comb. 4-stage CE | 21.5 | 21-23* | 5.8 | 48 | This work |
| 90 | SiGe 0.13 $\mu$m | 4-stage CE | 14.6 | 19.6 | 15.4 | 2.4 | [25] |
| 85 | SiGe 0.13 $\mu$m | Cascode×4 Power Comb. | 8 | 21 | 3.4 | 2.4 | [26] |
| 94 | CMOS 90 nm | 3-stage Power Comb. | 15 | 11 | 5.0 | 0.4 | [27] |
| 100 | CMOS 65 nm | 4-stage CS | 15 | 10 | 7.0 | 0.33 | [28] |
| 94 | InP HEMT 0.15 $\mu$m | 2-stage CS | 12 | 26.3 | 19.0 | 3.55 | [23] |
| 84-95 | GaN | 3-stage | 16 | 27.6-29.3 | 14.7 | – | [24] |

*: $P_{on-chip}$ used

**Table 4.3**: Performance Summary Compared to Free-Space (Quasi-Optical) III-V Designs

| **Freq. (GHz)** | **Techn.** | **Power Comb. Method** | **Number of Elements** | **$P_T$ (mW)** | **EIRP (W)** | **Ref.** |
|---|---|---|---|---|---|---|
| 90-98 | SiGe | Antenna/RFIC | 9 (3×3) | 90[1] | 3.16 | This work |
| 93 | InGaAs | Grid/Waveguide | 196 (14×14) | 684 | * | [42] |
| 79 | InP | Grid/Waveguide | 64 (8×8) | 264 | * | [41] |
| 44 | GaAs | Antenna/Hybrid | 256 (16×16) | 5,900 | 11,570 | [34] |
| 40 | GaAs | Grid/Space | 36 (6×6) | 670 | ** | [40] |
| 30 | GaAs | Grid/Waveguide | 242(11×11) 2-FETs per cell | 23,000 | * | [37] |
| 29 | GaAs | Antenna/Hybrid | 36 (6×6) | 8,000 | ** | [36] |

[1]: $P_{radiated}$ used

*: not applicable in a waveguide

**: not available in reference

communication systems with multiple simultaneous beams.

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# Chapter 5

# Conclusion

The thesis presented X- to W-band arrays, implemented in silicon technologies, for different phased array applications. The first 8-20 GHz two channel dual-down conversion receiver in a SiGe-BiCMOS process was presented for digital beam forming applications allowing for very high performance systems. In addition, chip on board packaging effects are analyzed and the first complete X/Ku-band phased array (8-element array) with a single silicon chip was presented with excellent patterns. This would allow low-cost highly scalable large arrays. Lastly, a W-band 3x3 wafer-scale array in a silicon implementation is presented by making use of quasi-optical power combining techniques and high efficiency on-chip microstrip antennas, leading to silicon transmitters (with phased arrays capabilities) that are competitive to best III-V solutions.

Chapter 2 presented the first fully integrated two-channel SiGe BiCMOS receiver, capable of operation in the 8-20 GHz, for digital beam forming phased arrays. The receiver is based on a dual-down-conversion architecture with selectable IF for interference mitigation, and the silicon chip is fabricated using a 0.18-$\mu$m SiGe BiCMOS process and has ESD protection on the RF and DC pads, consumes 70 mA per channel from a 3.0 V power supply and is 2.6$\times$2.2 mm$^2$, including all pads. The chip achieved excellent performance over the entire 8-20 GHz bandwidth, and results in a channel gain (I and Q paths) of 46-47 dB at 11-15 GHz and $>$ 36 dB at 8-20 GHz with an instantaneous bandwidth of 150 MHz. A 2-bit gain control (0-16 dB) is also provided at baseband. The measured NF is $<$ 4.1 dB (3.1 dB at 15-16 GHz) and is independent of the gain state. The measured OP1dB is -10 dBm and the input P1dB is -56 to -40 dBm at 15 GHz depending on the gain, which is sufficient for satellite applications. The on-chip channel-to-channel coupling is $<$ -48 dB. The measured EVM is $<$ 3% for a 1 Msps QPSK modulation at 8-20 GHz, and $<$ 1.8% for a 0.1, 1 and 10 Msps QPSK, 16QAM and 64QAM

modulations at 15 GHz. An 15 GHz 8-element array with a diplexed LO distribution network was demonstrated at 15 GHz and resulted in excellent performance. The chip was also used in a real-time FPGA-based phased array system at 15 GHz to generate three simultaneous beams each with 10.7 Mbps links.

Chapter 3 presented the first system level demonstration of a complete 8-element X/Ku-band phased array based on a single silicon chip. The phased array is integrated together with the antennas and digital control circuitry on a single Teflon board. The chip-on-board package, together with 8 X/Ku-band RF inputs and one RF output in a 2.2x2.5mm2 area, and the appropriate grounding and Vcc connections, are modeled using a 3-D EM solver. It is shown that chip-on-board packaging results in high isolation (low coupling) between the different RF ports, and ensures stability even with a channel gain of 20 dB at 12 GHz. The measured patterns show a near-ideal performance up to a scan angle of 60 with an instantaneous scanning bandwidth of 11.4-12.6 GHz. In the future, GaAs LNAs will be placed at each antenna element so as to result in 1-1.5 dB NF. In addition, true-time delay routing can be used for improved instantaneous bandwidth. A design that can be scaled to $8\times8$ or $16\times16$ elements using a "brick" ("card") architecture with minimal change in the layout is achieved.

Chapter 4 presented the first mm-wave wafer-scale power amplifier array implemented in a 0.13 $\mu$m BiCMOS technology fabricated together with high efficiency on-chip microstrip antennas. The power combining is done in the quasi-optical domain using high efficiency on-chip antennas. Beside a single W-band antenna/amplifier pair, a $3\times3$ power amplifier array with $0.6\lambda_0$ at 94 GHz spacing between the antenna elements is demonstrated. The 3x3 wafer-scalable array showed excellent performance with an output power of 21-23 dBm and an equivalent isotropic radiated power (EIRP) of 33-35 dBm at 90-98 GHz. The measured patterns of the array are in excellent agrement with simulations and show single-mode operation and $\sim$100% power combining efficiency with a 3-dB beamwidth of 28$^\circ$ and a directivity of 15.5 dB (gain of 12 dB). It is shown that with applying quasi-optical design methodology to Silicon-based designs, a $8\times8$ array would result in millimeter-wave transmitters which are competitive with the best III-V solutions. Furthermore, phase and amplitude control can be placed on each element leading to a phased array with controllable sidelobe levels.

# Appendix A

# JAZZ SBC18HXL and IBM 8HP Process Details and Pad Design

### A.0.1 JAZZ SBC18HXL Process

The circuits presented in Chapter 2 are implemented in Jazz Semiconductor 0.18 $\mu$m SBC18HXL BiCMOS process, which include high speed HBT with an $f_t$ of 155 GHz and an $f_{max}$ of 200 GHz. The process stack-up is given in Fig. A.1 and consist of 6 metal layers including a 2.81-$\mu$m-thick top metal (M6), which is used to implement transmission-lines and inductors. CPW transmission-lines with ground shields are implemented by using M6 layer as signal and side grounds, and the M4 layer as the bottom ground metal. The side-shields are connected to the M4-ground layer by using via holes. The process also has 0.18 $\mu$m CMOS transistors with an $f_t$ of 155 GHz. MIM capacitors with 5.6 fF/$\mu m^2$ are also available in the process.

### A.0.2 IBM 8HP Process

SiGe BiCMOS process (0.13 $\mu$m) of IBM is used for the W-band power amplifier design described in Chapter 4. The 0.13$\mu$m bipolar transistors have an $f_t$ of 200 GHz. The process has 7 metal layers, including a 4-$\mu$m-thick AM layer (aluminum) and 1.25-$\mu$m-thick LY layer (copper) (Fig. A.2). MIM capacitors with 1 fF/$\mu m^2$ are available in the process between QY layer (just above the LY layer) and LY layer, and are extensively used for RF de-coupling and matching networks. Minimum MIM-capacitor value is 64 fF, and capacitors with lower values are implemented using MOM structures shown in chapter 4. The AM layer is used for

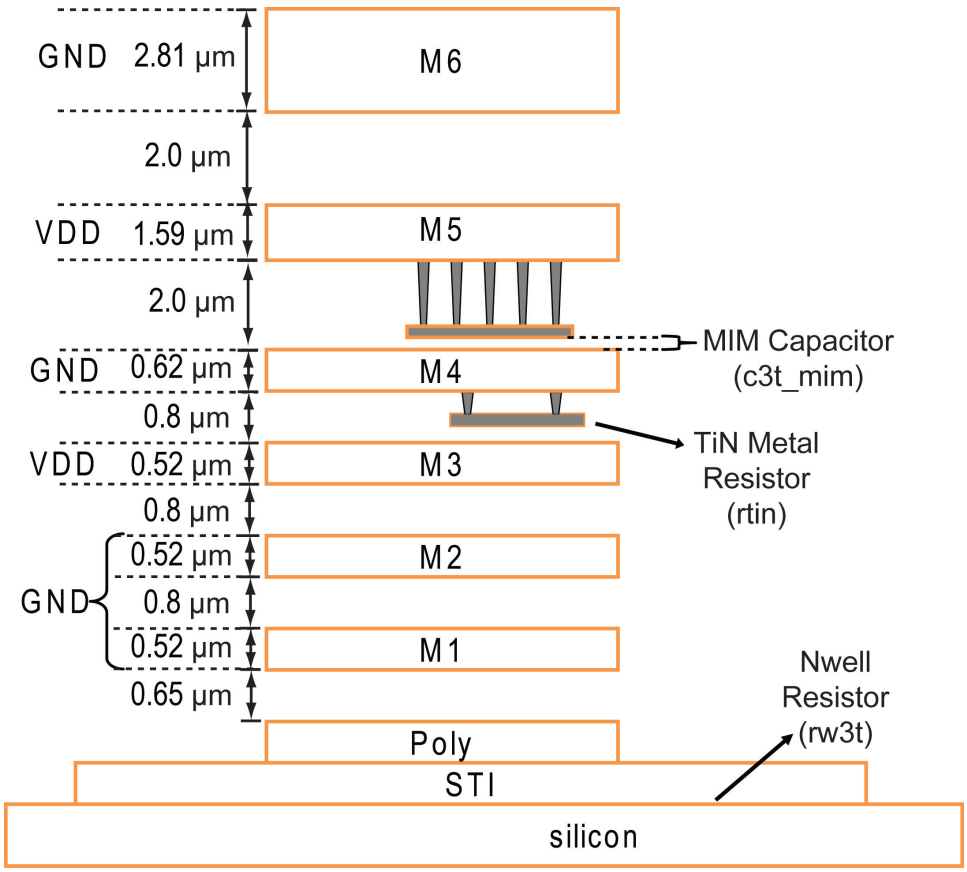


**Figure A.1**: JAZZ SBC18HXL process stack-up with 6 metal layers, MIM capacitors and TiN resistors.

transmission-lines and inductors. Grounded CPW transmission lines are implemented using AM (signal) and MQ (ground) layers. LY layer is extensively used for supply routing, and many decoupling MIM capactitors are placed between LY (supply) and AM (ground) layers.

### A.0.3 Pad Design

De-embedding pad capacitance is a very challenging issue especially for high frequency designs. Pad capacitances (shunt to the ground) are generally around 30-50 fF which is crucial at mm-waves, and should be included in the design. For the mm-wave work in this thesis, a tapered CPW to grounded CPW transition (GSG probe-tip to 50 ohm grounded CPW) is designed to be 50-ohm on both sides, compensating for the pad capacitance (Fig. A.3). The transition is simulated in a back-to-back configurations using Sonnet, and results in $<$ -25 dB return loss up-to 120 GHz. The transition results in $<$ 0.1 dB loss (per pad, 0.2 dB back-to-back) at DC-120GHz. The transition can be tuned for higher design frequencies by adjusting the ground extension underneath.

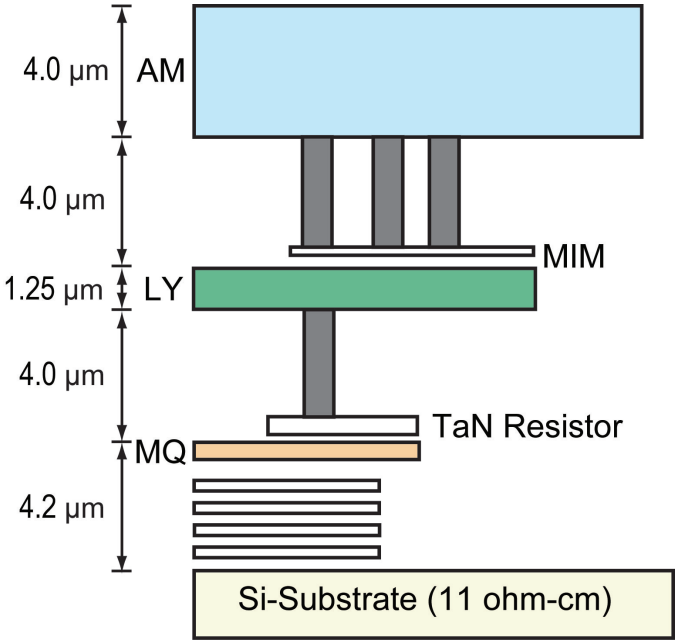


**Figure A.2**: IBM 8HP process stack-up with 7 metal layers, MIM capacitors, and TaN resistors.

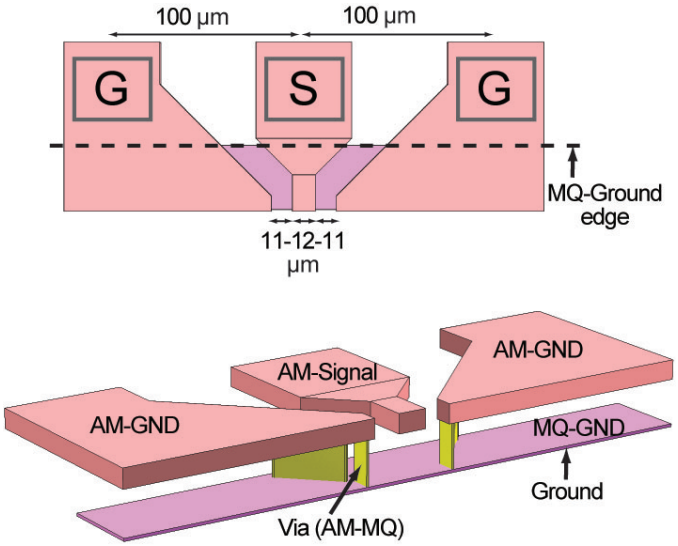


**Figure A.3**: CPW pad transition design in IBM8HP process.

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