Fabrication and performance of nanoscale ultra-smooth programmed defects for EUV Lithography

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Abstract

We have developed processes for producing ultra-smooth nanoscale programmed substrate defects that have applications in areas such as thin film growth, EUV lithography, and defect inspection. Particle, line, pit, and scratch defects on the substrates between 40 and 140 nm wide 50 to 90 nm high have been successfully produced using e-beam lithograpy and plasma etching in both Silicon and Hydrosilsequioxane films. These programmed defect substrates have several advantages over those produced previously using gold nanoparticles or polystyrene latex spheres_--most notabably, the ability to precisely locate features and produce recessed as well as bump type features in ultra-smooth films. These programmed defects were used to develop techniques for film defect mitigation and results are discussed.

I. Introduction

As devices sizes shrink into the nanoscale regime, the thin films used for these devices must be of the highest quality especially at thicknesses in the sub-10 nm regime. One of the questions in thin film growth and device technology is how small topographic variations affect film growth and morphology. These topographic variations may be the fabricated part of the underlying device structure or defects due to small particle contaminants, pits, and or scratches on the substrate.

Previously, Mirkarimi, et. Al [1,2] demonstrated that film growth properties could be studied using monodisperse gold nanospheres. With this technique, the authors demonstrated defect mitigation using the Ion Beam Thin-Film Planarization Process, which consists of a series of sacrificial film deposition and etching steps [3] [2,4]. Although the initial studies used the nanosphere technique, significant process advances were facilitated in the later studies using the programmed defects described here. Advantages include predetermined placement of defects, narrower defect size distributions, and the ability to study both pit and bump defects simultaneously.

In reflective diffractive optic devices for extreme ultraviolet (EUV) applications, the underlying film topography must be controllable at sub-wavelengths (13.5 nm for lithography). These optics work in a reflective mode where Mo/Si multlayers act as a Bragg mirror. Even nanometer topographical variations in the underlying substrate (a small particle for example) can cause detectable phase shifts in the reflected beam. In EUV lithography (EUVL), a promising next-generation lithographic candidate for the 32 nm node, mask blanks are fabricated by depositing reflective Mo/Si multilayer thin films

on glass substrates. Here, small topographical variations in the mask can translate to variations in image intensity on the wafer. Simulations indicate that substrate pits or bumps only several tens of nanometers in depth and width disturb multilayer film growth enough to result in a printable defect[5]As the simulations show that printability is a function of height and width thus, it is valuable to be able to study the defects of varying heights and widths simultaneously.

We have developed techniques to fabricate precisely placed nanoscale topography (both bumps and depressions) in extremely smooth films with well-controlled heights, widths, and size distributions to facilitate thin film growth studies and defect mitigation for EUV lithography. Features between 40 and 140 nm wide and 50 to 90 nm high have been produced and are described here. Performance of these defects in thin film defect mitigation will be discussed briefly.

II. Fabrication Techniques

For both pit and bump defects, multiple die were patterned on a single Si substrate. In each die, 40, 50, 60, 70, 80, 90, 100, 120, and 140 nm widths were targeted for raised and recessed programmed defects. We facilitated metrology of defects by patterning optically visible pointers at the bottom corner of each die with additional pointers located at each new defect size.

A. Particle-like defects

The simple yet effective sequences for producing particle-like defects is illustrated in Fig. 1. First, Si <100> wafers were spin-coated with hydrogen

silsesquioxane (HSQ, FOX product from Dow Corning) HSQ is a a spin-on-glass, which acts as a negative tone resist under e-beam exposure. Final defect thickness is dependent on the HSQ concentration and spin speed. For 70 nm high defects, 3.6% HSQ was spun at 4000 rpm, and oven-baked for 5 min on a copper plate at 170 °C for 30 minutes. Defect patterns were exposed using a modified[6] Leica VB6HR at 100 keV with 450 pA beam current and a 6.5 nm FWHM spot size at a nominal dose of 3000 uC/cm2 and developed for 60 secs using Shipley Corp. LDD26W. Dot and lines as small as 15 nm wide were fabricated with this process. With sequential spin-coatings and exposures, particles with different heights can be fabricated on one substrate.

B. Pit defects

Recessed topography representative of pits and scratch defects were fabricated by transferring e-beam defined programmed defect patterns into an underlying thin film using plasma etching (Fig. 2). Defect depths were determined by the film thickness and a 10-20 nm Cr etching stop was used to insure etching did not proceed into the silicon wafer (and thus change the defect depth). Both HSQ and poly-Silicon were used as defect materials. The HSQ was spun on the wafer and baked in 4 successive steps at 120 °C, 170 °C, 250 °C and 400 °C, each for 1 minute. For Silicon pits, very low roughness Silicon was sputter deposited. Techniques for producing these ultra-smooth films with heights and uniformity controllable in the sub-nm regime are described in a companion paper [7].

A positive e-beam photoresist, ZEP-520 (Zeon Corporation) at 140 nm thick (33% at 1000 rpm, 170 °C pre-exposure bake, 3 min xylenes development, IPA rinse) was lithographically patterned to define the defect pattern in the photoresist etching mask. Pit

and scratch defects ranging in size from 40-140 nm wide were exposed with a 50% negative feature bias. Electron beam exposure dose varied depending on feature sizes but were in the range of 150-200 uC/cm2. For the HSQ pits, the patterns were transferred into the cured HSQ (Oxford Plasmalab 300) using $CHF_3/Ar/CF_4$ plasma chemistry and a platen power of 275 Watts (Oxford Plasmalab 380). The defect pattern was transferred into the ultra-smooth silicon film using inductively-coupled HBr plasma chemistry. The photoresist mask was removed with an O_2 plasma strip.

III. Programmed Bump defects

Figure 1 shows a typical 4x4 array of bump defects. A 4x4 array of identical bumps are located between 2 μm pads for ease of location during metrological observations. The inset shows a 50 nm wide coded defect, 70 nm high.

Prior to using programmed defects, commercially available Au spheres deposited on Silicon was used to study to multi-layer film growth and planarization techniques.[1] The advantages electron-beam written defects have over the Au sphere technique in thin film growth studies are numerous. The obvious advantage is that the defect pattern locations are precisely determined relative to the center of the exposed substrate whereas the Au particles are distributed randomly across the wafer. In addition, with electron-beam patterns, multiple defect widths can be studied on a single substrate. The metrological issues with the Au sphere technique makes this much harder. In fact, the electron-beam can print patterns of arbitrary shapes allowing us to mimic a wide variety of real defects. Furthermore, the distribution of the AFM measured defect heights is quite narrow compared to previously studied Au particles (ref) -- 50.62 +/- 0.88 nm for nominally 50 nm programmed defects in HSQ and 50.9 +/- 7.8 for nominally 50 nm Au

spheres (95% confidence interval). However, a significant advantage of using electron-beam fabricated defects over Au particles is the ability to produce pit defects in addition to bumps.

IV. Programmed pit defects

Initially, pit defects were fabricated in a film of cured HSQ using plasma etching. Although height integrity was good these defects used for thin film defect studies, the roughness of the samples (~0.7 RMS) was prohibitive defect planarization abilitity below 1 nm. We thus focused on a new technique for producing ultra-smooth programmed pit defects.

The technique for fabricating ultra-smooth defects takes advantage of our ability to sputter the very low roughness Si used in multilayer coating technology (detailed elsewhere ref). Ultra-smooth films of silicon were sputter-depositied on ultra-smooth Cr. Figure 2 shows AFM roughness data for a typical Si programmed defect surface on Cr with root mean square (RMS) roughness of 0.233 nm, comparable to that for single crystal Si wafer.

During fabrication, we found the etching process played a critical role in maintaining the silicon smoothness. Initially, etching was done using HBr plasma, which has good selectivity to the photoresist masking layer and the underlying etching stop. After etching and oxygen plasma stripping of the photoresist, residue was found surrounding the pit-type defect that added 5-15 nm to the Si defect surface roughness (Fig. 5A). The residue is a byproduct of the etching process, sometimes called a fence

or veil, which forms on the sidewalls of the features and collapse after photoresist removal.

Residues could be removed using either dry or wet chemistry (Fig. 5B-C). The dry chemistry process employed 2 % CF_4 addition during the oxygen plasma photoresist strip. The veils were cleared but the Cr etching stop was also etched, albeit slowly (10 nm/min). This led to a loss of control in the defect depth (Fig. 3B). In order to achieve maximum selectivity to Cr, and precise control of the defect depth, we used EKC 270 (Dupont Corp., 70 °C for 30 minutes), a wet chemistry solution formulated to strip polysilicon etching residues (Fig. 5C).

To avoid the formation of these veils altogether, we investigated alternative dry etching chemistries. We chose a newly developed technique for etching nanofeatures that uses alternating steps of etching and deposition with very specific chemistries [8]With this novel etching technique, we fabricated defects with extremely vertical sidewalls and without veil formation (Fig. 6). Sidewall slope can be tailored by varying the relative times of etching and deposition step time throughout the process. This provides an opportunity to study the smoothing capability as a function of the defect's sidewall shape. In addition, this process has excellent selectivity to Cr and thus the etching stop is intact and the defect height integrity is maintained. This process is compatible with the production of programmed pit and bump defects on the same wafer.

V. Thin Film Growth and Planarization Studies of Programed Defects

Figure 7 shows a 70 nm HSQ bump defect planarized at the surface of the Mo/Si using an ion beam thin film planarization process.[9] Here, at each deposition cycle of the

Mo/Si multilayer, a sacrificial layer of Si (about 1-2 nm) is deposited and then etched away. Using this technique, the 70 nm bumps were planarized to below 1nm at the Mo/Si interface (non-printable in an EUVL mask).

Figure 8 shows a smoothed HSQ pit using the ion beam thin film process. Here a modified planarization process was used that is able to effectively smooth both pits and bumps. Here a thicker Si layer is used to planarize the substrate, before the reflective multilayer is deposited. This thicker layer of Si can be deposited and etched away without the drawbacks of interface roughening, argon incorporation, and the longer process time required when incrementally planarizing at each Mo/Si deposition cycle. Using this process,[10] 70 nm pits were smoothed to < 1 nm. Better smoothing could not be seen due to relatively high roughness of the HSQ layer (~.7 nm rms). The new process for producing programmed pit defects which utilizes ultra-smooth sputtered Si on ultra-smooth Cr low (~.2 nm RMS roughness) will allow more sensitive measurements of ultimate smoothing.

VI. Conclusions

Ultra-smooth programmed bump and pit type defects with precise width, height and narrow size distributions have been fabricated using ultra-smooth sputtered films, electron-beam lithography, and plasma etching. Compared to the Au nanospheres used previously for defect studies, these methods allow fabrication of *bump and pit* type defects, with accurately determined locations, and the potential, using a novel etching technique, to create programmed defect shapes with profiles mimicking actual defects. These programmed defects have already had significant impact in the field of EUV

lithography as they have facilitated development of techniques capable of bump and pit defect mitigation during Mo/Si multilayer film growth.

Acknowledgements

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Figure Captions:

1. Fabrication of particle-like defects.

2. Fabrication of pit defects. 1) Deposit Cr and spin-on HSQ or sputter amorphous Silicon. 2) Spin-on Zep-520 photoresist. 3) Expose and develop photoresist. 4) Transfer pattern into HSQ or silicon using plasma etching. 5) Strip photoresist.

3. Array of e-beam patterned HSQ particle defects (50 nm wide, 70 nm high). Inset is close-up of circled defect.

4. AFM measurement of recessed line defect. Roughness of surface is .23 rms. Low roughness allows good signal-to-noise in measurements of defect smoothing and thin film growth.

5. SEM cross-sections of recessed line defects in Silicon. A) HBr plasma chemistry for pattern transfer leaves etching residue. B) Removal of residue using a Oxygen plasma with the addition of 2% CF4. Cr underlayer is etched and changes height of defect. C) Removal of residue using commercially available EKC-270 for residue removal. Cr underlayer is left intact and defect height integrity is maintained.

6. SEM cross-section of recessed line defect in Silicon. Novel plasma etching technique using Fluorine chemistry produces defects with very straight sidewalls. Good selectivity to Cr underlayer maintains defect height integrity.

7. TEM cross-section of smoothed HSQ bump-type line defect using Ion Beam Thin Film Planarization process. Defect is planarized within 1 nm. Figure reprinted from Microelectronic Engineering.[9]

8. TEM cross-section of smoothed HSQ pit –type line defect using Ion Beam Thin Film Planarization process. Defect is planarized to below 1 nm. Better smoothing could not be discerned due to roughness of HSQ. New processes will employ ultra-smooth Silicon pits described here.

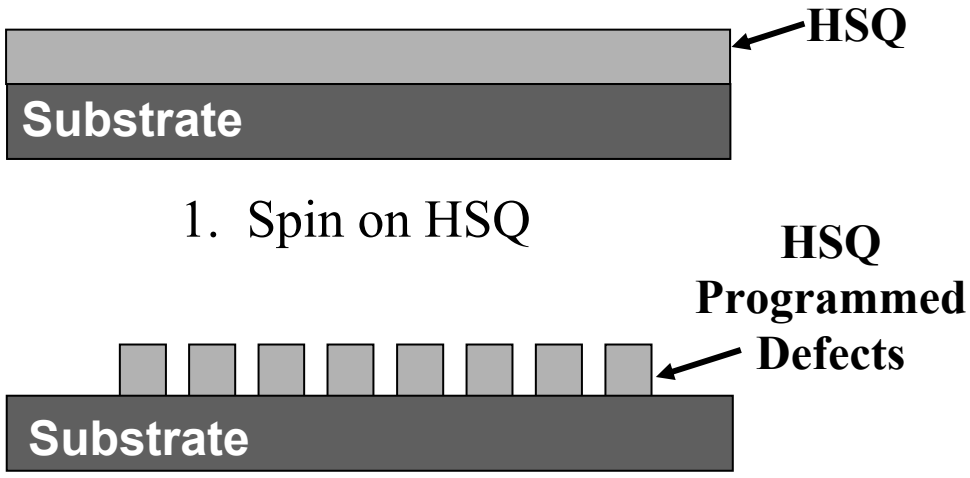

HSQ
Substrate
1. Spin on HSQ
HSQ
Programmed
Defects
Substrate
2. Expose and Develop

Fig. 1

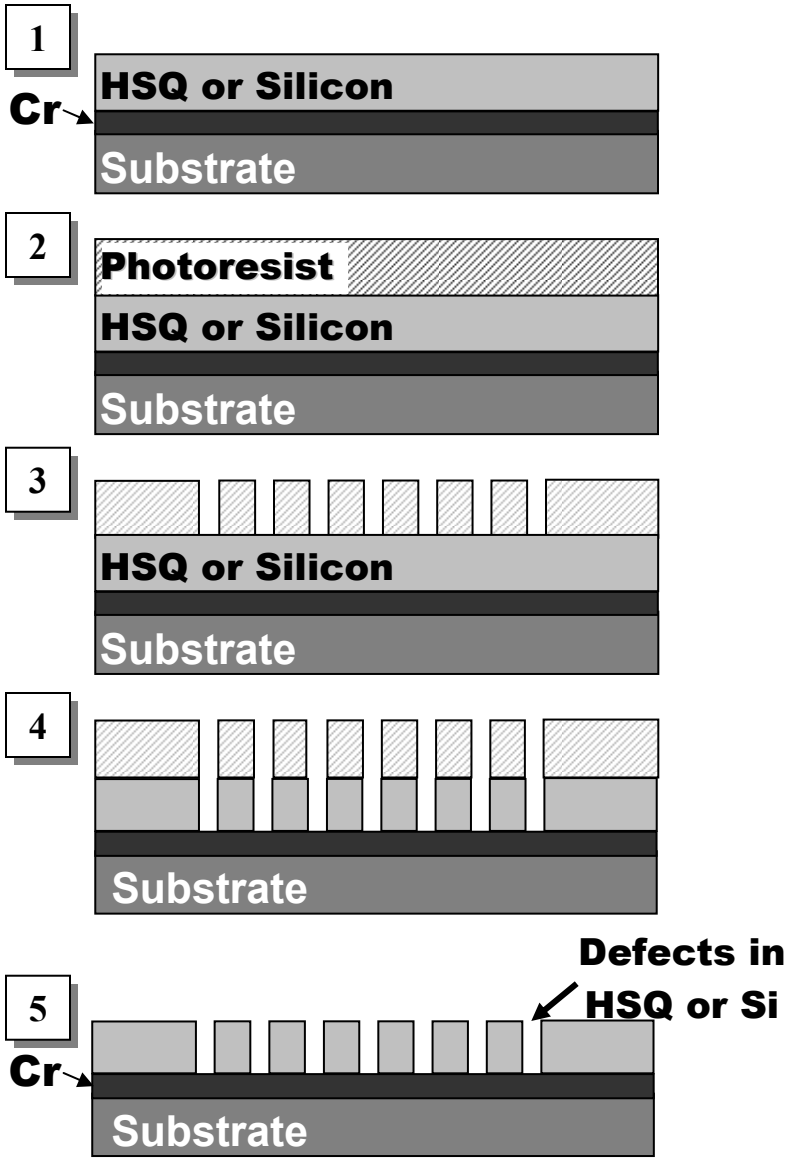

1
HSQ or Silicon
Cr
Substrate
2
Photoresist
HSQ or Silicon
Substrate
3
HSQ or Silicon
Substrate
4
Substrate
Defects in
HSQ or Si
5
Cr
Substrate

Fig. 2

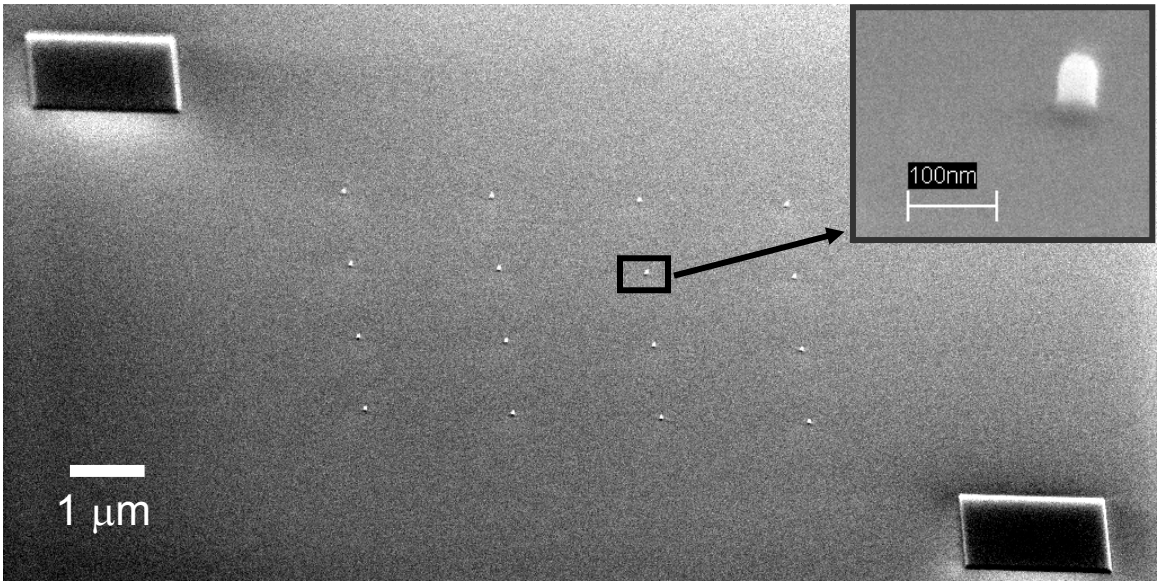


Fig. 3

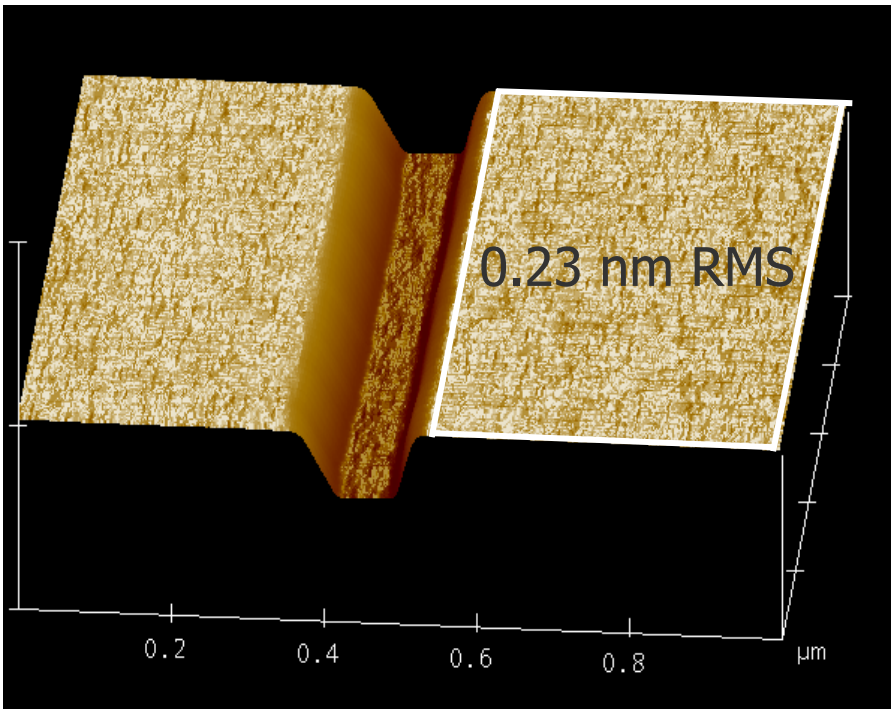


Fig. 4

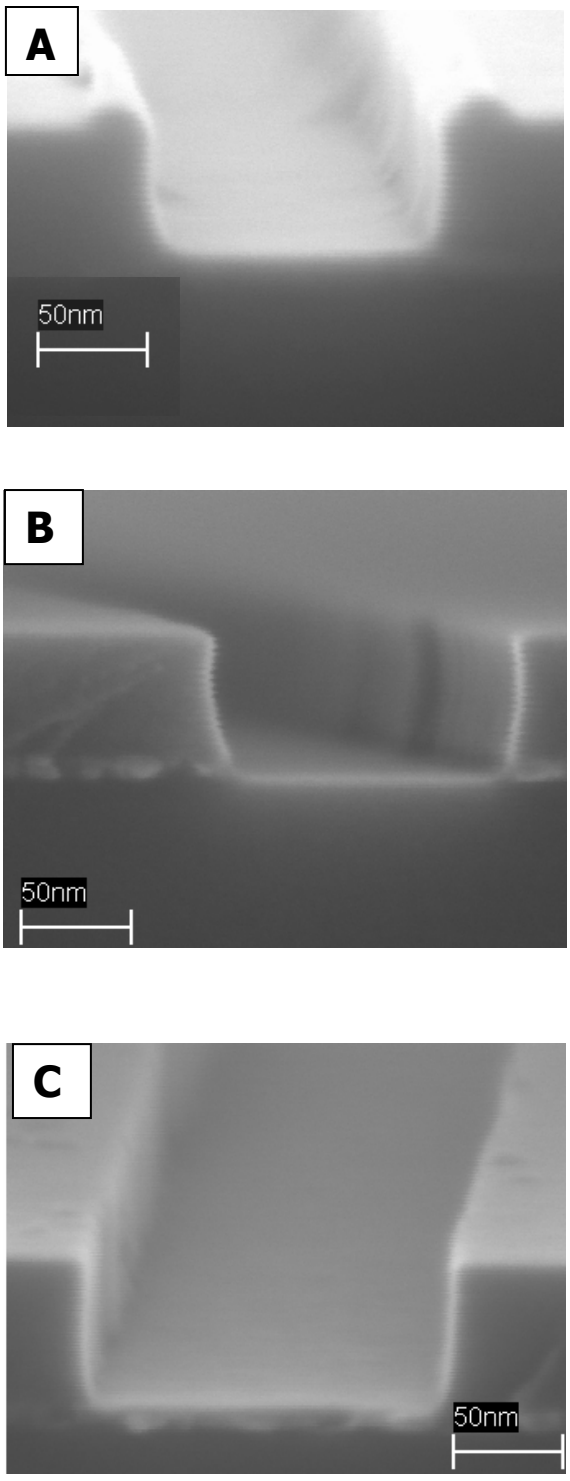


Fig. 5.

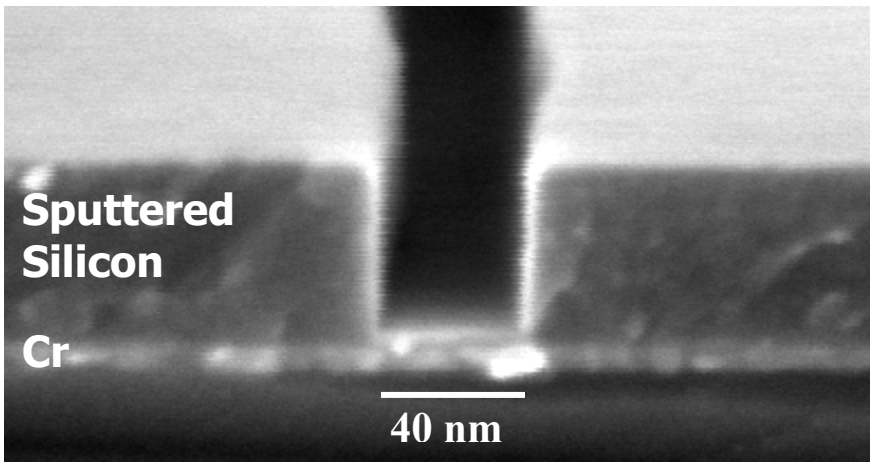


Fig. 6.

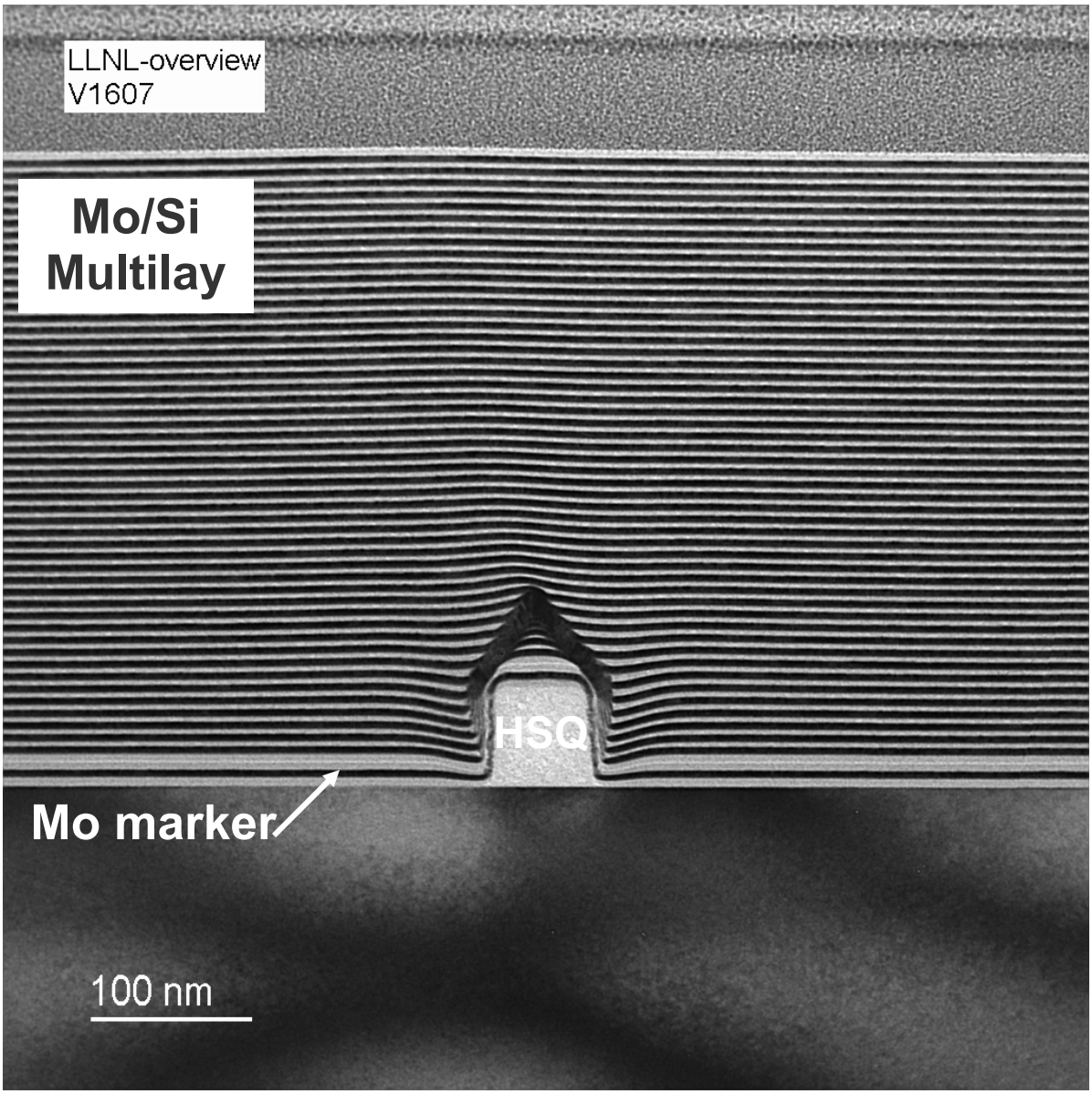
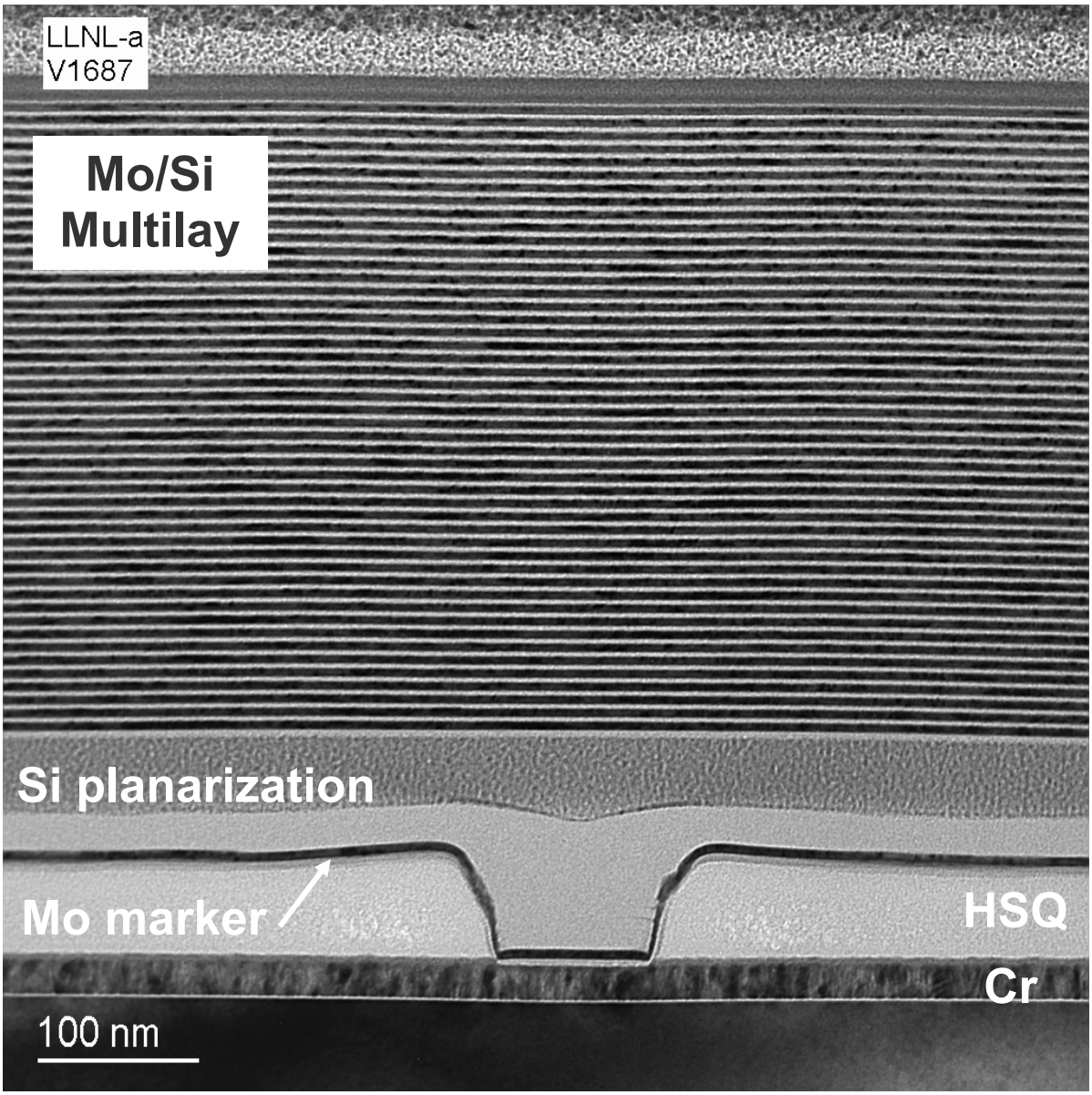


Fig 8.


LLNL-a
V1687
Mo/Si
Multilay
Si planarization
Mo marker
HSQ
Cr
100 nm