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Silicide/Silicon Heterointerfaces, Reaction Kinetics and Ultra-short Channel Devices

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Silicide/Silicon Heterointerfaces, Reaction Kinetics and Ultra-short Channel Devices

A dissertation submitted in partial satisfaction of the

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in Materials Science and Engineering

by

Wei Tang

2012

ABSTRACT OF THE DISSERTATION

Silicide/Silicon Heterointerfaces, Reaction Kinetics and Ultra-short Channel Devices

by

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Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2012

Professor King-Ning Tu, Chair

Nickel silicide is one of the electrical contact materials widely used on very large scale integration (VLSI) of Si devices in microelectronic industry. This is because the silicide/silicon interface can be formed in a highly controlled manner to ensure reproducibility of optimal structural and electrical properties of the metal-Si contacts. These advantages can be inherited to Si nanowire (NW) field-effect transistors (FET) device. Due to the technological importance of nickel silicides, fundamental materials science of nickel silicides formation (Ni-Si reaction), especially in nanoscale, has raised wide interest and stimulate new insights and understandings. In this dissertation, *in-situ* transmission electron microscopy (TEM) in combination with FET device characterization will be demonstrated as useful tools in nano-device fabrication as well as in gaining insights into the process of nickel silicide formation. The shortest transistor channel length (17 nm) fabricated on a vapor-liquid-solid (VLS) grown silicon nanowire (NW) has been demonstrated by controlled

reaction with Ni leads on an *in-situ* transmission electron microscope (TEM) heating stage at a moderate temperature of 400 ºC. $NiSi_2$ is the leading phase, and the silicide-silicon interface is an atomically sharp type-A interface. At such channel lengths, high maximum on-currents of 890 (μA/μm) and a maximum transconductance of 430 (μS/μm) were obtained, which pushes forward the performance of bottom-up Si NW Schottky barrier field-effect transistors (SB-FETs). Through accurate control over the silicidation reaction, we provide a systematic study of channel length dependent carrier transport in a large number of SB-FETs with channel lengths in the range of (17 nm – 3.6 μm). Our device results corroborate with our transport simulations and reveal a characteristic type of short channel effects in SB-FETs, both in on- and off-state, which is different from that in conventional MOSFETs, and that limits transport parameter extraction from SB-FETs using the conventional field-effect transconductance measurements.

In addition to application of silicide in Si NW devices, the fundamental materials science of Ni-Si reaction is also of interest, and *in-situ* TEM has been shown to be a useful tool in obtaining dynamical phase transformation information and therefore providing insights into the new phase formation process. By using in-situ TEM techniques, a new gold catalyzed solid-liquid-solid (SLS) silicide phase growth mechanism in Si NWs is observed for the first time, which shows the liquid mediating growth can be also used in synthesis of metallic silicide nanowires. SLS is analogous to the VLS in both being liquid-mediated, but is fundamentally different in terms of nucleation and mass transport. In our SLS growth at 700 ºC, the Ni atoms are supplied from remote Ni particles by interstitial diffusion through Si NW

into the pre-existing Au particle at the tip. Upon supersaturation of both Ni and Si in Au, octahedral shape of Ni disilicide phase nucleates in the middle of the Au liquid alloy, which thereafter sweeps through the Si NW and transform Si into $NiSi_2$. Dissolution of Si by Au(Si,Ni) liquid mediating layer and growth of $NiSi_2$ are shown to proceed in different manners.

Using *in-situ* TEM technique, we also have the chance to present direct evidence that Si (111) twin boundaries and Si grain boundaries on Si NW surface can be efficient heterogeneous nucleation site for the silicide growth. By analyzing the nucleation site favorability, unlike other typical FCC materials like Cu or Si, we infer (111) twin defects in $NiSi_2$ may have high interfacial energy. These results may provide valuable insights into the MOSFET source/drain (S/D) contact silicide formation process when defects are either unintentionally formed during the process or intentionally introduced to engineering the strain along the channel.

The dissertation of Wei Tang is approved.

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2012

This thesis is dedicated to my parents.

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PUBLICATIONS

JOURNAL PAPERS

1. Wei Tang, Shadi A. Dayeh, S. Tom Picraux, Jian Yu Huang, King-Ning Tu, "Ultrashort Channel Silicon Nanowire Transistors with Nickel Silicide Source/Drain Contacts", Accepted by *Nano Letters,* to be published ASAP
2. Wei Tang, Shadi A. Dayeh, S. Tom Picraux, Xiaohua Liu, Jian Yu Huang, King-Ning Tu, "Gold Catalyzed Ni Disilicide Formation in Si Nanowires: A New Solid-Liquid-Solid

(SLS) Phase Growth Mechanism", *in preparation*

3. Wei Tang, Shadi A. Dayeh, S. Tom Picraux, Jianyu Huang, King-Ning Tu, "Effect of defects on nickel disilicide nucleation in silicon nanowires", *in preparation*
4. Jinkyoung Yoo, Bonghwan ChonWei, Wei Tang, Taiha Joo, Dang Le Si, Gyu-Chul Yi, "Excitonic origin of enhanced luminescence quantum efficiency in MgZnO/ZnO coaxial nanowire heterostructures", *Applied Physics Letters,* **100***,* 223103 (2012)
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CONFERENCE PRESENTATIONS

1. Wei Tang, Shadi A. Dayeh, S. Tom Picraux, Xiaohua Liu, Jianyu Huang, King-Ning Tu, "Gold Catalyzed Ni Disilicide Formation in Si Nanowires: A New Solid-Liquid-Solid (SLS) Phase Growth Mechanism", Oral presentation, MRS Spring meeting, San Francisco, CA, April 2012
2. Wei Tang, Shadi A. Dayeh, S. Tom Picraux, Xiaohua Liu, Jianyu Huang, King-Ning Tu, "Gold Catalyzed High Temperature Silicide formation in Si Nanowires: A New Solid-liquid-Solid (SLS) Phase Growth Mechanism within a Solid Matrix", Oral presentation, Physics and Chemistry of Surfaces and Interfaces, Santa Fe, NM, Jan 2012
3. Wei Tang, Shadi A. Dayeh, S. Tom Picraux, King-Ning Tu, "Si Nanowire Schottky Barrier Transistors with Short Channels formed by Controlled Si/Silicide Interfaces

Movement", Oral presentation, Physics and Chemistry of Surfaces and Interfaces, Santa Fe, NM, Jan 2012

4. Wei Tang, Shadi Dayeh, Tom Picraux, King-Ning Tu, "FET devices with ultra-short channel length built on silicide/silicon/silicide heterostructures", Oral presentation, 2011 Materials Research Society Fall meeting, Boston, Massachusetts, December 2011
5. Wei Tang, Shadi Dayeh, Tom Picraux, King-Ning Tu, "Silicide/silicon/silicide nanowire heterostructures and devices", Oral presentation, 2011 Electronic Materials Conference, Santa Barbara, CA

Chapter 1 : Introduction

Nickel silicides have been a critical element in the microelectronic products because they forms the metal/semiconductor interface to semiconductor devices. Historically, silicide with low resistivity and high temperature stability has been examined as the metal-semiconductor contact materials. Silicide technologies have moved from Ti silicide, Co silicide and eventually to Ni silicide due to demands on increased process compatibility and decreased resistivity. This chapter aims at provide a general review of the silicide technology in modern VLSI device fabrication process, materials science in the silicide formation, and transits to application of silicide in Si nanowire (NW) devices.

1.1 Nickel silicide technology in VLSI devices

1.1.1 Self-aligned (Salicide) silicide process

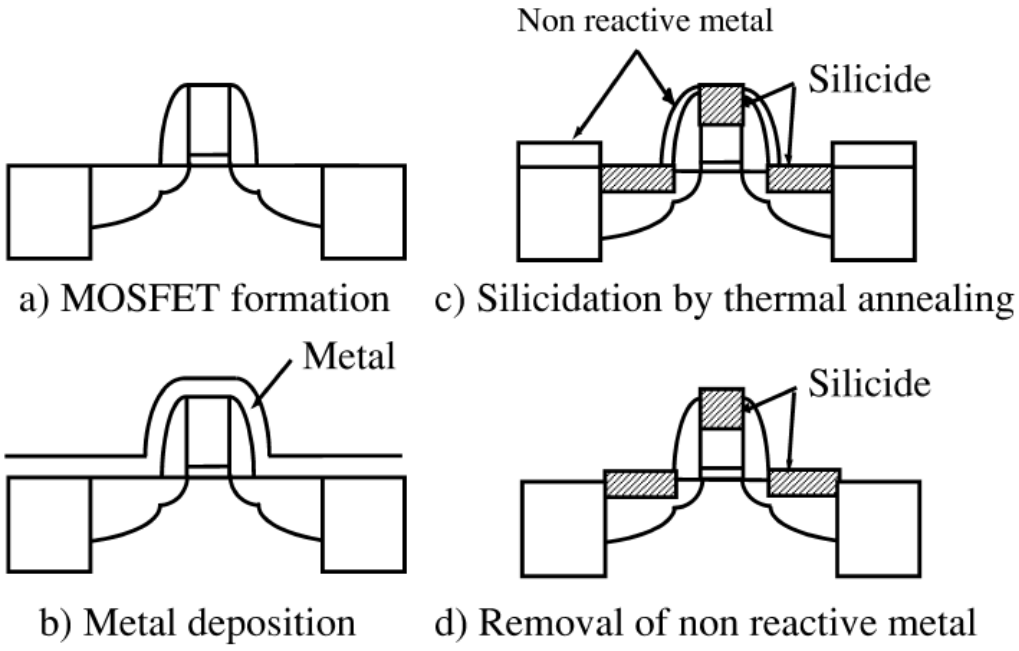

Figure 1.1 Schematics for salicide process [1].

We will first look at the role of nickel silicide in VLSI devices. Nickel silicide is used as the electrical contact material to both heavily doped source/drain (S/D) and gate through a self-aligned silicide process (salicide). After formation of MOSFET (Figure 1.1a), blanket Ni film is deposited on the Si wafer (Figure 1.1b). Nickel silicide is selectively formed in the contact openings during thermal treatment (Figure 1.1c) and unreacted Ni is removed (Figure 1.1d). Since Ni is the dominant diffusing specie in the Ni-Si reaction[2], the bridging effect that otherwise shorts the gate and S/D (e.g. in $TiSi_2$ case) is eliminated. Also, NiSi has the

advantage of low formation temperature (about 400 ºC). Compared with their counterpart C54-$TiSi_2$ (850 ºC) and $CoSi_2$ (800 ºC) in the previous technology generation[1]. Besides, with the downscaling of MOSFET channel length and therefore the contact line width, $TiSi_2$ and $CoSi_2$ contacts were subjected to sheet resistance degradation (narrow line effect) successively at the technology node 180 nm and 90 nm due to difficulty in nucleation of the low resistivity phase and grain agglomeration at high temperature [3]. The requirement of shallow junction formation also favors NiSi, because to form silicide line with the same resistivity, NiSi consumed the least Si. Therefore, nickel silicide is the choice of contact metal for current deep sub-100nm technology node. We explored the use of nickel silicidation reaction as an approach to form the contact to ultra-short channel Si NW transistor and the results will be discussed in details in Chapter 2.

1.1.2 Nickel silicide phase formation sequence

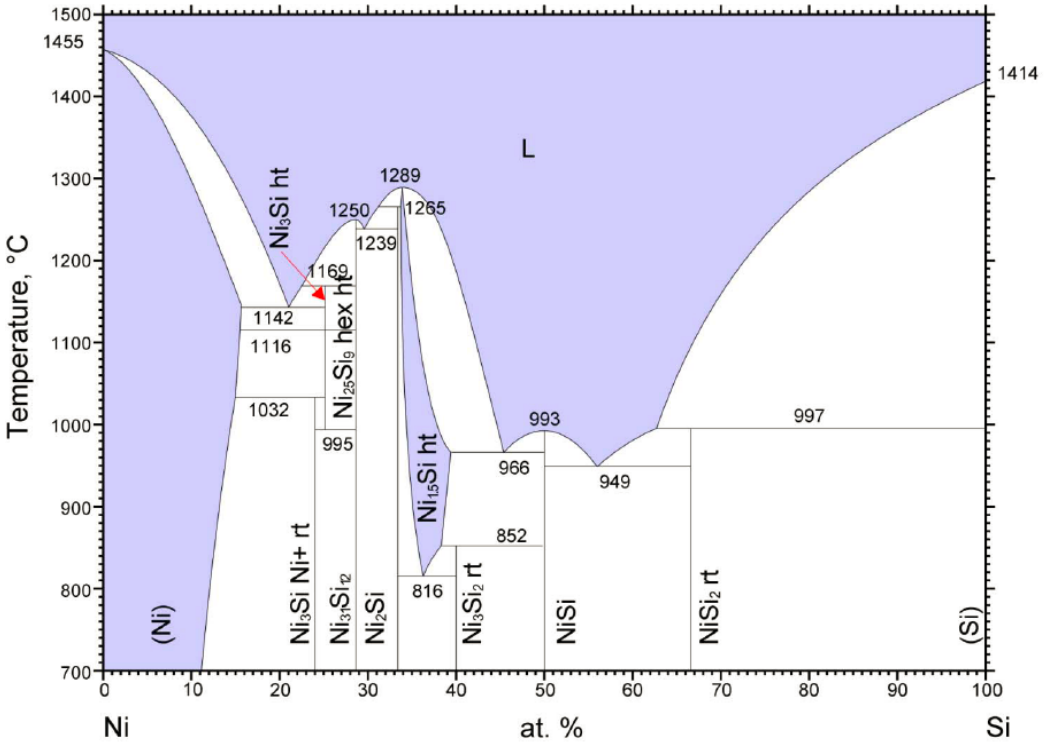

Figure 1.2 Ni-Si phase diagram

According to the phase diagram of Ni-Si system, multiple nickel silicide phases are stable at room temperature, including $NiSi_2$, NiSi, Ni_3Si_2, δ-Ni_2Si, $Ni_{31}Si_{12}$, Ni_3Si. In the reaction of bulk Ni-Si vertical[4] and lateral [5, 6] diffusion couple, multiple above phases are observed. However, in the reaction of Ni film (in the range of several hundred nanometers) with Si wafer, the resulted nickel silicide phase follows a well define phase sequence as temperature ramps up: δ -Ni_2Si is the first phase formed at a temperature as low as 200 ºC, and transformed to NiSi as the temperature is raised above 350 ºC, and finally converts to $NiSi_2$ at above 750 ºC [7].

To understand the absence of multiple phase formation in the thin film reaction, a comprehensive kinetic model for competing growth of multiple phase was proposed[8] In this model, after the first diffusion controlled phase (δ-Ni_2Si in the Ni-Si case) is formed, growth of the second phase does not start until the thickness of the first phase segment reaches a "critical thickness". This critical thickness was defined when the atomic fluxes of the dominant diffusion specie to and away from the interface between two competing phases are equal. In other words, regarding the growth of the first phase (diffusion controlled), it grows fast when its thickness is small and the growth rate gradually decreases as its thickness increases. Now consider the formation of a potential second phase (NiSi in the Ni-Si case). If it is interfacial reaction controlled and its growth rate is lower than the first phase, this potential second phase does not appear and there is only a single phase in this diffusion couple. When the growth rate of the potential second phase is higher than the first phase, the second phase will be observed, resulting in simultaneous multiple phase growth, which corresponds to a bulk diffusion couple case. The critical thickness was estimated to be about 2μm in the temperature range of 300 ºC to 430 °C. Since the thickness of silicide contact is much less than 2 μm, the kinetic reasoning explains the "single phase growth" phenomenon in contact reactions. Therefore, all the contacts on the Si chip are the same. This can also explain the multiple phase growth in a Ni pad to Si NW reaction, in which the reaction is closer to the thermodynamic limit. This will be discussed in details in Chapter 2.

It has been suggested [9-11] the selection criteria for the first phase is the one that degrades system Gibbs free energy at a maximum rate (i.e. maximize $-\frac{d\Delta G}{dt}$). Note the

relation $-\frac{d\Delta G}{dt} = -\frac{d\Delta G}{dX}\frac{dX}{dt}$, where $\frac{d\Delta G}{dX}$ is the driving force and $\frac{dX}{dt}$ is the growth rate of this phase. Therefore, the selection of the first phase is determined by both thermodynamic and kinetic factors.

1.1.3 Nickel silicide as fully silicide metal gate

Downscaling of effective oxide thickness (EOT) of the gate dielectric is critical in advancing technology node in improving the MOSFET performance and alleviating short channel effect. When SiO_2 is scaled down to a few atomic layer thick, direct tunneling from the gate to the channel will cause device failure. High-k dielectric materials such as HfO_2 has been used because to achieve a small EOT, the physical thickness of HfO_2 can be thicker due to its much higher dielectric constant (26) than SiO_2 (3.9). However, when poly-Si gate is used with typical high-k material, the channel is subjected to remote phonon scattering (RPS) [12] and carrier mobility is severely degraded, especially under high field. Metal gates have to be used with high-k dielectric materials because the high carrier density in metals will screen out RPS. Also, using metal gate can eliminate poly-Si depletion effect. [13]

The metals to be used for PMOS and NMOS should have different work functions to meet their different switching requirement. It has been found that the work function of NiSi formed after transforming poly-Si gate can be tuned by adjusting doping levels and dopant types in the original poly-Si gate. [14]

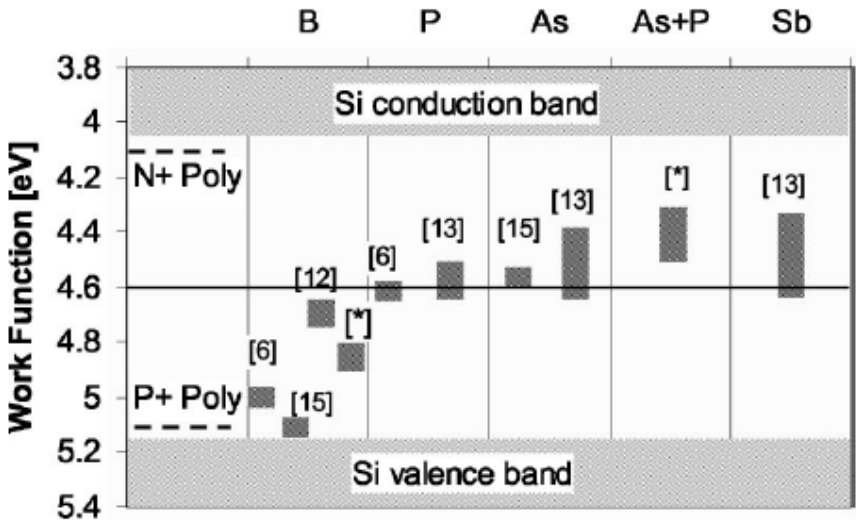

Figure 1.3 From Ref [14], work function tuning of NiSi formed on pre-doped poly-Si with different dopant types. Refer to Ref [14] for citation used in the figure.

Generally speaking, n-type dopant shifts NiSi Fermi level above Si midgap and p-type dopant shifts that below Si midgap, which tunes the work function of the NiSi to the same direction as doping poly-Si gate (Figure 1.3). The mechanism of this work function modulation by dopants was attributed to interfacial dipoles formed by dopants pileup (snow-plow effect) during NiSi formation process. However, there is a recent debate [15] arguing the work function modulation is a bulk instead of an interface effect.

1.2 Nickel silicide in Si nanowire devices

1.2.1 Nickel silicide as source/drain extension to nanowire FET device

Si NW FET fabricated by top-down [16-20] or bottom-up [21] method has been intensively investigated as alternative device structure to replace the traditional planar

MOSFET. Its advantage lies in that the nanowires are inherent 3D objects and Ω-shape gates or gate-all-around structures can easily form to maximize the gate control over the channel and relieve short channel effect. Due to superior property of nickel silicides (e.g. clean metal/semiconductor interface, reproducible electronic characteristics), they (or their counterpart germanide in Ge device) were also used in nanowire FET device [22-25].

One unique aspect of using silicide as the contact material is its formation process. A typical fabrication process of Si NW FET with nickel silicide as source/drain materials is described in Figure 1.4. After Ni contact annealing, nickel silicide S/D extension forms from Ni pad and grows into the Si NW (Figure 1.4c and Figure 1.5a). The channel length L_g can be tuned by controlling this reaction process. We utilized and monitored the reaction on an *in-situ* TEM heating stage and achieved a 17nm Si channel (Chapter 2). The silicide S/D contact formed in this way allows a metal top-gate to fully cover the Si channel and maximize the electrostatic gate control over the channel.

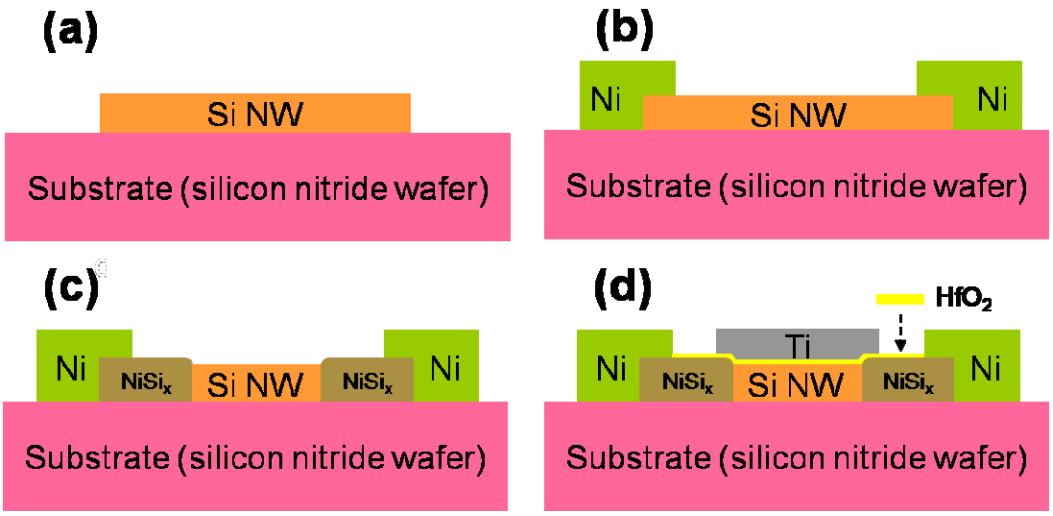

Figure 1.4 Nickel silicide source/drain Si NW FET fabrication process (a) Si NW dispensing (b) Ni contact definition (c) Nickel silicide formation at elevated temperature (d) Gate dielectric layer deposition and metal gate definition

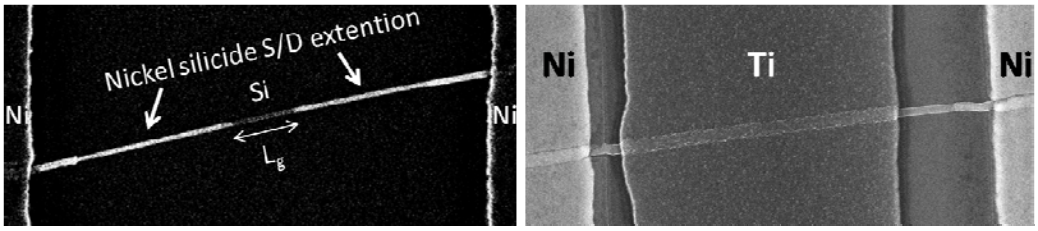

Figure 1.5 (a) Si NW channel with nickel silicide S/D extension (b) Ω-gate Si NW FET

1.2.2 Kinetics of nickel silicide growth in Si nanowire

It is important to understand the kinetics of nickel silicide growth in Si NW in order to achieve reproducible control over the contact and Si channel formation in Si NW FET device. The growth kinetics itself is also an interesting topic from the aspect of fundamental materials science. For studies of kinetic in phase transformation phenomena in NWs, *in-situ* TEM has

been a useful tool in capturing dynamical structure change information and providing insights into the phase transformation process. [26-29]

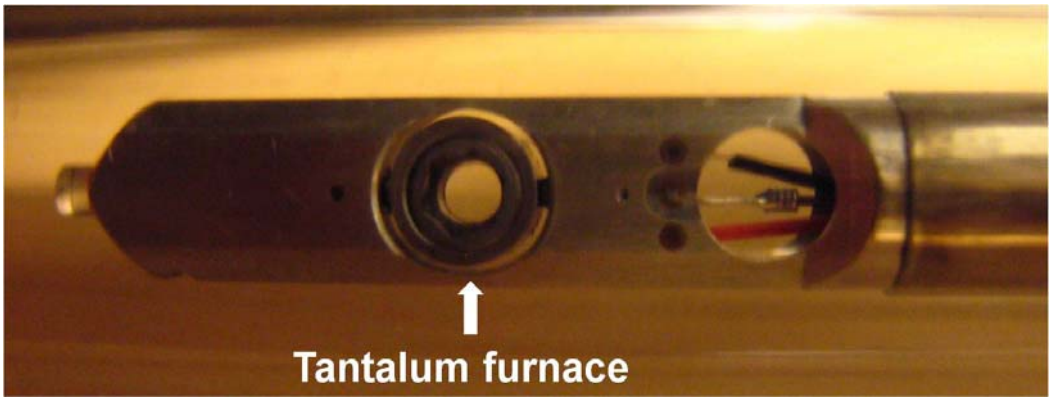

Figure 1.6 Gatan Single Tilt Heating Holder 628 with Tantalum furnace

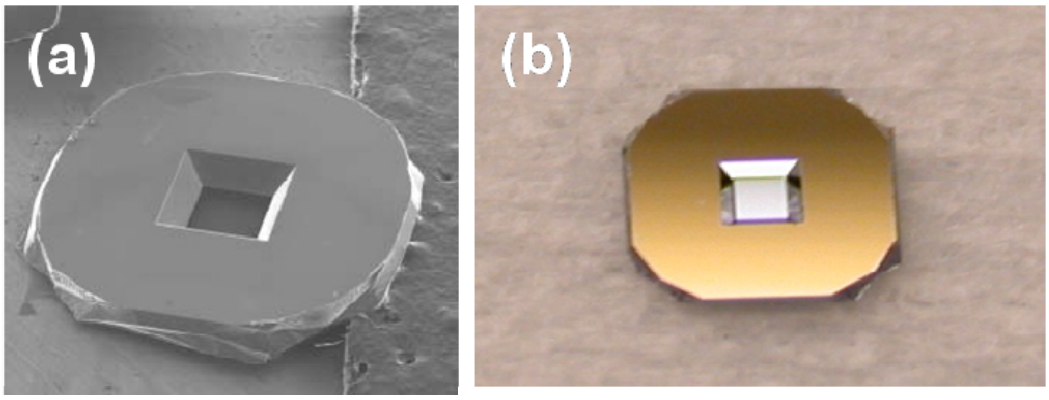

Figure 1.7 TEM silicon nitride membrane window (a) SEM image (b) optical image

The *in-situ* TEM is well-versed in investigation phase transformation under various external conditions, e.g. heating, mechanical stressing, electrical stressing etc, depending on the TEM holder used. In studies of Ni-Si reaction, we used a TEM heating stage (Figure 1.6, Gatan Single Tilt Heating Holder 628) to heat up Ni sources and Si NWs on silicon nitride

TEM membranes (Figure 1.7) and observe the nickel silicide formation process dynamically. Similar setups are also used by other investigators.

Lu *et al* first obtained HRTEM images of nickel silicide growth in Si NW on an *in-situ* TEM heating stage.[30] The Si NW is in contact with multiple Ni NWs and nickel silicide was formed from the two ends of the Si NW and gradually transformed Si NW into nickel silicide NWs. HRTEM imaging combined with temperature tuning of the heating stage allows for precise control of the reaction at atomistic scale, and a Si gap as short as 2 nm was achieved. Our approach to fabricate ultra-short channel Si NW FETs (Chapter 2) inherits and develops the methodology in this work.

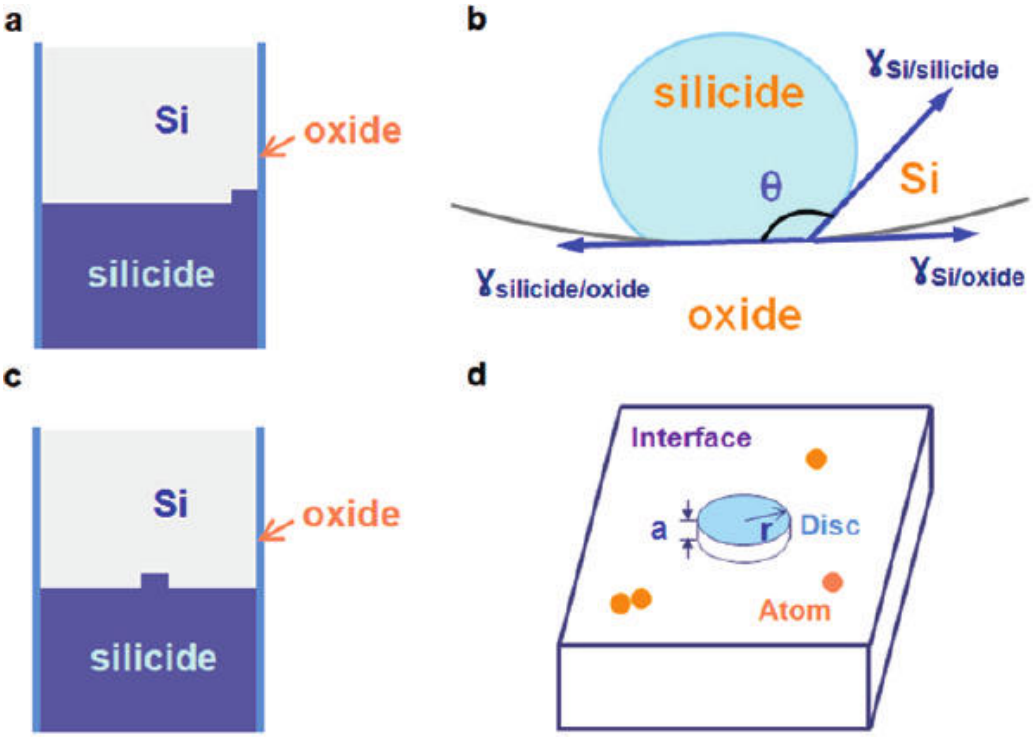

Figure 1.8 (a) Heterogeneous nucleation of a 2D silicide step at the Si/oxide interface (b) top-view of (a). (c) Homogeneous nucleation of a 2D silicide step in the center of the Si NW (d) schematics of a homogeneously formed disk.[31]

Chou *et al* found when $CoSi_2$ grows into Si NW, the reaction front proceeds in a stepwise manner. [32] *In-situ* HRTEM was used to track the step propagation, and emerging of each new step implies repeating 2D nucleation of a single $CoSi_2$ layer. Further investigation showed that the new silicide step nucleates homogeneously in the center of the Si NW and then propagates to the edge of it.[31] Homogeneous nucleation was very rarely observed because the nucleation barrier is high and usually new phase can first heterogeneously nucleate at certain interfaces in the system associated with a lower nucleation barrier. A comparison of homogeneous and heterogeneous nucleation of a 2D silicide step is summarized in Figure 1.8. The reason for absence of 2D heterogeneous nucleation here is that, to form a silicide step at the edge of the Si NW, a high energy Si/silicide interface will replace the low energy Si/oxide interface, which is energetically unfavorable. Therefore the new 2D silicide step has to nucleate homogeneously at the center of the Si NW. This result closely resembles our observation (to be discussed in more details in Chapter 3) that $NiSi_2$ nucleate homogeneously in the middle of Au-Ni-Si ternary alloy, due to a similar mechanism in selecting nucleation sites. Besides, in Chapter 3, change of 2D silicide nucleation site in Si NW, when defects are present, will be further discussed in Chapter 4.

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Chapter 2 : Ultra-short Channel Silicon Nanowire Transistors with Nickel Silicide Source/Drain Contacts

2.1 Introduction

Vapor liquid solid (VLS) grown semiconductor nanowires (NWs) have been intensively investigated as candidates of electronic devices due to their decent crystal quality[1], easiness of control over lateral confining dimension[2, 3], and potential for bottom-up self-assembled circuits[4-6]. Field-effect transistors (FETs) built on VLS grown Si, Ge and SiGe heterostructure NWs have shown high carrier motilities and excellent transistor characteristics comparable to or better than those fabricated by top-down processing approaches[7, 8].

Enhanced FET performance is enabled with ever-smaller channel lengths that can provide high on-current drives or reduced power consumption. The microelectronic industry has been pursuing smaller and faster devices since it was established half a century ago. The trend of devices miniaturization follows the prediction by Moore's law (Figure 2.1). Si NW FETs have been considered as a candidate structure for extremely scaled transistors. The primary advantages for using NWs are the fact that their gates can be formed in a Ω-gate or gate-all-around geometries, and therefore have superior electrostatic coupling between gate and channel over other device architectures and able to relieve short channel effect, including drain-induced-barrier lowering (DIBL) and degradation in sub-threshold slope [9].

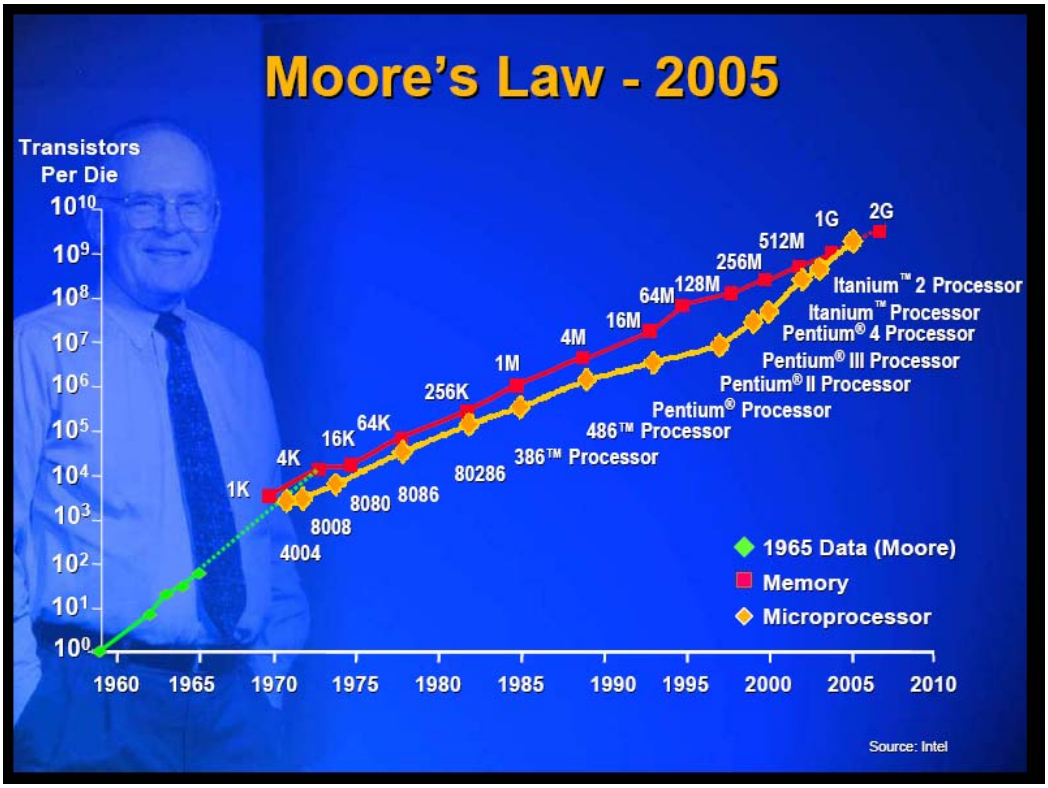


Figure 2.1 Moore's law showing the trend of device miniaturization

The NW transistor channel length is usually defined by the metal gate width, or the distance between its source/drain (S/D) electrodes, both of which are limited by lithography patterning tools. With continual transistor down-scaling, the demands on the critical dimension (CD) control in lithography tools steadily increases. For CD below 20nm, very expensive e-beam lithography tools or sophisticated photolithography technologies (extreme ultraviolet source, double patterning, etc) are needed[10].

By extending earlier works [11, 12] on controlled silicide formation in *in-situ* TEM experiments, we developed a process that can overcome the resolution limit posed by lithography technologies in defining transistor channels. Using this technique, we

demonstrate SB-FETs with ultra-short channel lengths down to 17nm on VLS grown Si NWs. Compared with the conventional MOSFET, a SBFET has naturally abrupt junctions and is not limited by lateral doping profiles, which are determined by the doping/activation techniques[13, 14] and become increasingly difficult for ultra-short channel devices. Our investigation also includes the silicidation reaction fundamentals (phase formation and growth kinetics), which is important to achieve a fine control over transistor channel lengths previously not achieved with VLS NW FETs. The controlled channel formation using this technique enabled us to access a new domain of SB-FET operation and to identify a performance transition between long channel and short channel regions in SB-FETs with an overall transport performance that is in excellent agreement with our transport simulations. This is because in NW FETs, the contacts are non-ohmic because the NW is undoped. Further, our systematic transport studies elucidates the essential role of Schottky barriers in charge transport in ultra-short channel FETs and demonstrate that transport parameter extraction using conventional transconductance methods from SB-FETs may not be accurate. The implications of this analysis can be generalized to other NW SB-FETs.

2.2 Material Considerations in Nanochannel Silicidation:

Nickel silicides are the standard metal contacts used in the semiconductor industry for both NMOS and PMOS devices and are regarded as 'mid-gap' metals with a hole Schottky barrier height (SBH) of ~ 0.4 eV on p-Si[15, 16]. Moreover, nickel silicides (or their counterparts, nickel germanides in germanium devices) have been extensively explored as nanoscale contacts for semiconductor NWs[17-21] and therefore our choice as the electrical contacts to

Si NW devices. In the Ni-Si reaction, Ni is the dominant diffusing species (DDS), and multiple nickel silicide phases could form[22]. Different nickel silicide phases have different Ni concentration and diffusivity[23], and growth of a more Ni-rich phase by consuming a less Ni-rich phase also needs Ni supplies from the metal contact reservoir. The phenomenon of simultaneous growth of multiple phases complicates the kinetics analysis that uses the data of silicided segment length versus time. To better understand and control the Ni-Si reaction kinetics for the fabrication of ultra-short channel FETs, we examine first the nickel silicide phases in our silicided NW segments and provide a detailed analysis on the silicide/silicon interface structure and quality that can have direct impact on formed silicide/silicon barrier heights and charge injection.

Our SB-FET devices were fabricated on 50 nm thick silicon nitride TEM membranes with a window size of 250 μm × 250 μm. Source/drain Ni contacts were defined by photolithography, followed by 100 nm e-beam evaporated Ni layer. The native oxide on the Si NWs at contact openings is removed before metallization. After S/D metallization, and to avoid creation of defects in the native oxide layer on the Si channel during the subsequent high energy electron radiation (300 keV) in TEM (Tecnai F30), we went through a special procedure[24] to remove this native oxide layer.

Annealing of the sample was performed on an *in-situ* TEM heating stage (Gatan 628 single tilt heating holder) at 425 ºC, and the reaction was monitored in real-time. Initially, nickel silicide formed at the source/drain Ni/Si contact, grew inward by transforming Si NWs. The remaining Si segment of the NW shrinks as the reaction proceeds.

Figure 2.2 (a-g) shows a series of TEM snapshots during the reaction process. If not interrupted, the whole Si NW would be fully converted into a metallic nickel silicide NW. However, we are interested in using this process to demonstrate that we can dynamically control the length of Si segment and use it as the channel in FET devices. When the length of the Si segment (referred as Si channel thereafter) reaches a desired length, we stop heating the sample, which thereafter cools down quickly (~10 ºC/s) and the interface is frozen. To fabricate ultra-short Si channel, very precise control of the reaction process or the silicide growth rate is required. In the final stage of Si channel length tuning, the silicide growth rate was reduced to about 0.05 nm/s at 375 ºC, which allows for sub-nanometer fine control over the channel length.

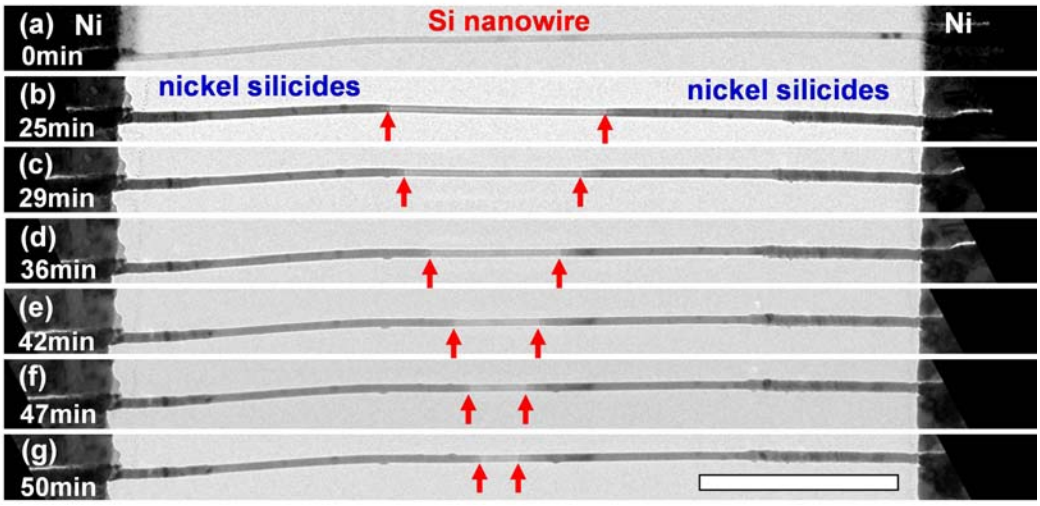


Figure 2.2 (a-g) Series of *in-situ* TEM snapshots showing the growth of nickel silicide from S/D Ni electrodes and narrowing of the middle silicon segment. The red arrows indicate the silicide/silicon reaction front. Scale bar is 1 μm.

We find that there are multiple phases formed on the Si NW as the reaction front swept through (Figure 2.3a). The phases are determined by electron diffraction patterns and fast Fourier transformation (FFT) of high resolution (HR) TEM images obtained from at least two different zone axes. The leading phase in direct contact with Si is $NiSi_2$, which is immediately followed by θ -Ni_2Si within a distance of 50 nm. Going further outwards in the direction to the Ni leads, the θ -Ni_2Si is followed by a δ -Ni_2Si segment. Then, a more nickel-rich phase $Ni_{31}Si_{12}$ follows in direct vicinity with the Ni leads. During the process of silicidation, Ni diffuses into the Si crystal, and the resulting Ni-Si compound volume is generally greater than the original Si volume, which appears with diameter expansion compared with the as-grown Si NW diameter (Figure 2.3a). The only exception of volume expansion resides in the $NiSi_2$ phase because of its close similarity in crystal structure and lattice parameter with Si. We observe diameter expansion when Si is transformed to θ -Ni_2Si, δ -Ni_2Si or $Ni_{31}Si_{12}$. This phase sequence is in contrast with the results obtained in a thin film reaction between planar Si and Ni thin films, which were established from in-situ XRD and resistance measurements during the temperature ramp up[25]. We recall that in thin film studies, δ -Ni_2Si is the first phase formed at a temperature as low as 200 ºC, and transformed to NiSi as the temperature is raised above 350 ºC, and finally converts to $NiSi_2$ at above 750 ºC[26]. The expected NiSi phase was not observed in our experiments, which corroborates with earlier results from the reaction between Ni pads and Si NWs at 550 ºC[27], 450 ºC[28] and 360 ºC[29], and from the reaction between Ni thin films and Si wafers at 450 ºC[30, 31], all of which showed $NiSi_2$ as the leading phase at temperatures well below 750 ºC. It has

been suggested that the interfacial oxygen may play a role in mediating $NiSi_2$ formation at low temperature[31], however, there is currently no definite explanation of the mechanism of low temperature formation of $NiSi_2$. Another silicide phase θ -Ni_2Si, which follows $NiSi_2$ in the upstream direction towards the Ni leads, has a hexagonal lattice structure (a=3.836 Å, b=4.948 Å). According to Ni/Si phase diagram, θ -Ni_2Si is a high temperature phase, which is stable above 825 ºC. However, recent studies on Ni and Si NW reaction have also found θ -Ni_2Si formed at a low temperature[32]. Moreover, in-situ X-ray diffraction studies of Ni-Si reaction shows that θ -Ni_2Si is a transient phase, which appears first at low temperatures, but disappears as the temperature is increased[33]. This is in good agreement with our results in that θ -Ni_2Si is also quickly consumed by δ -Ni_2Si after it forms. Another experiment[34] to test the stability of this phase shows that the θ -Ni_2Si phase formed at high temperatures transforms into δ -Ni_2Si and ε -Ni_3Si_2 as predicted by the phase diagram as it is cooled down below its stable temperature 825 ºC. On the other hand, θ -Ni_2Si formed at a low temperature (460 ºC) does not decompose during temperature cool down even to room temperature. These experiments suggest that although θ -Ni_2Si is a high temperature phase, it has certain type of stability at low temperatures, likely due to high kinetic barriers for phase transformation.

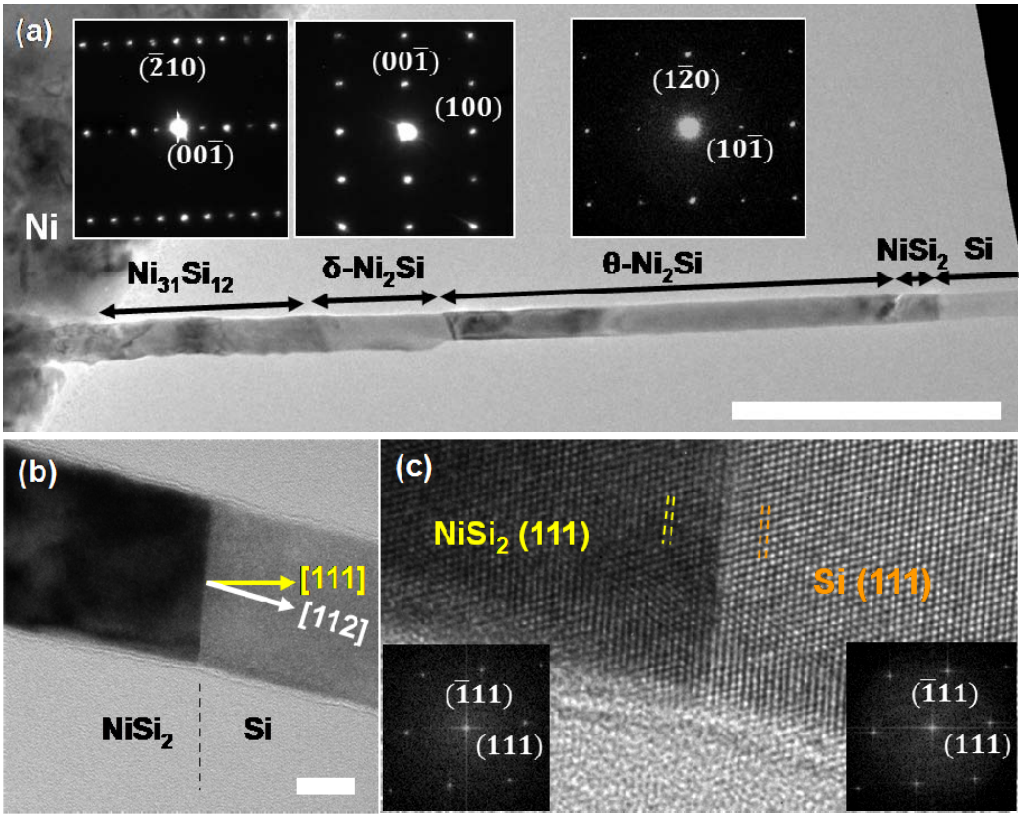


Figure 2.3 (a) TEM image with selected diffraction patterns that determine the nickel silicide phase sequence: Between Ni and Si, several phases are formed including $Ni_{31}Si_{12}$, δ -Ni_2Si, θ -Ni_2Si and $NiSi_2$. Zone axes for inset diffraction patterns from left to right are [120], [010], and [212], respectively. The scale bar is 400 nm. (b) Zoom-in TEM image of the $NiSi_2$/Si interface, showing the reaction front is Si (111) plane even in a <112> grown silicon NW. The scale bar is 20 nm (c) HRTEM image of the atomically flat $NiSi_2$/Si interface. The crystal orientation across the interface corresponds to a type A interface. The epitaxial relationship is established as $NiSi_2$ (111) // Si (111) and $NiSi_2$ [$\bar{1}$10] // Si [$\bar{1}$10].

Among all the phases and interfaces formed along the NW axial direction, the $NiSi_2$/Si interface is the metal-semiconductor contact interface. It is interesting to observe that the

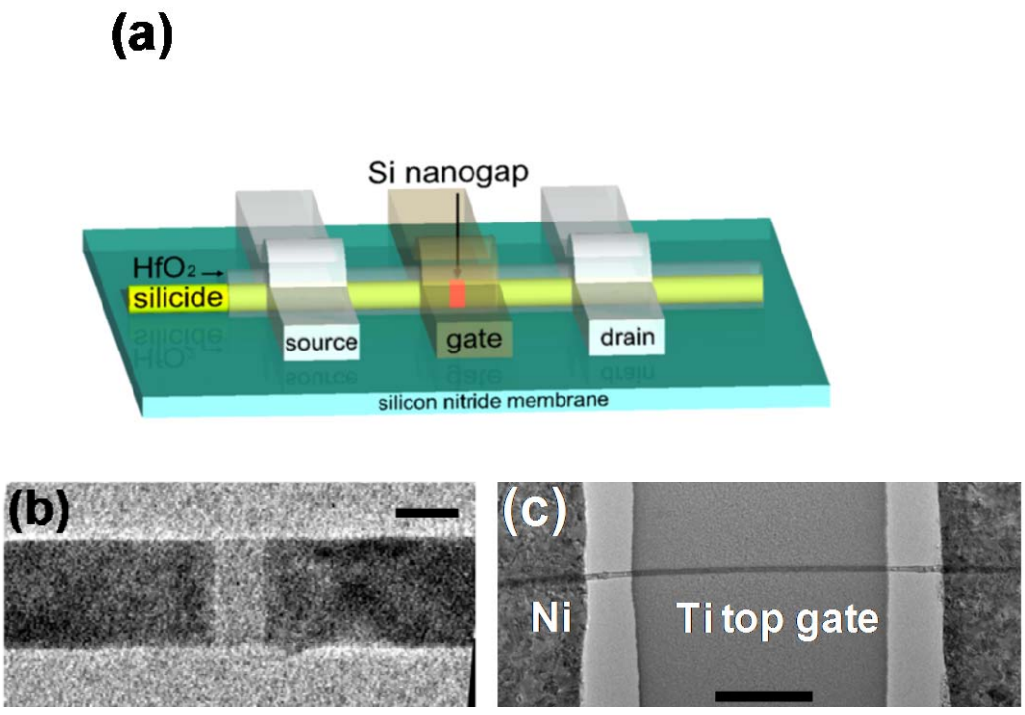
Ni-Si reaction front is Si (111) plane, even in a [112] grown Si NW (Figure 2.3b-c). The HR TEM image in Figure 2.3c shows that the interface is atomically sharp, and the epitaxial relationship established from the image is $NiSi_2$ (111) // Si (111) and $NiSi_2$ [$\bar{1}$10] // Si [$\bar{1}$10]. The slanted interface observed here has a larger area compared with a cross-sectional plane that is perpendicular to the NW growth direction. The fact that the silicide-silicon NW system chooses to form a larger interfacial area implies that the Si(111)/$NiSi_2$(111) interface has lower energy than that of all other possible interface configurations. In a reaction between Ni thin film and Si (001) wafer, inverted $NiSi_2$ pyramids[31, 35, 36] with {111} facets form inside the Si wafer, showing the same reaction front as we observe here. It is known that the $NiSi_2$/Si interface is among the best quality metal semiconductor interfaces[37], because the two crystals share the same cubic structure and a very close lattice constant (a_{Si}=5.430 Å, a_{NiSi2}=5.406 Å). The interfacial electronic properties are determined by the detailed structure of the $NiSi_2$/Si interface. Two types of $NiSi_2$/Si interfaces can form with a difference in their crystal orientations across the interface. $NiSi_2$ has the same orientation with Si in a type-A interface, while it is rotated 180º about the interface normal axis with respect to Si in a type-B interface. It is known [38] that these two interfaces have different SBH with n-Si (0.65 eV on type-A and 0.78 eV on type-B). In a large area thin film reaction [36], usually the $NiSi_2$/Si interface is a mixture of type-A and type-B. In contrast, throughout the high resolution transmission electron microscopy (HRTEM) characterization of our nanoscale contacts, we consistently observe atomically sharp type-A $NiSi_2$/Si interface, which guarantees the reproducibility of the electronic properties of the metal/semiconductor contact.

2.3 Device Analysis of Ultra-short Channel SB-FETs:

With this thorough understanding of formation, structure, and expected electronic properties of our silicide-Si NW interface, we are able to precisely scale down the channel length of a $NiSi_2$-Si NW transistor and explain its carrier transport characteristics. The silicide growth rate can be controlled by carefully tuning the temperature at the final stage of the silicidation reaction. Schematic of our top-gated Si FET device structure is shown in Figure 2.4a, with ultra-short channel (Si nanogaps) highlighted on the Si NW. We have obtained a 17 nm Si channel on a VLS grown Si NW (Figure 2.4b) at a temperature of 375 ºC. HfO_2 gate dielectric (10nm) was conformally deposited on the Si NW devices using atomic layer deposition at 200 ºC. At this temperature, no further silicidation was observed, and the Si channel length was retained at the desired value. Finally, 100nm Ti was deposited as the top-gate electrode. Figure 2.4c shows a TEM bright field image of the fabricated device on the 17 nm Si NW channel (Figure 2.4b). $NiSi_2$ is still the leading phase in such very short Si NW channels (Figure 2.7, supporting information). In our devices, the leakage current from gate electrode to S/D nickel silicide extensions is small (<1pA when V_g= -4 V) and we are only interested in DC characteristics of the device, so the gate-S/D overlapping was not of concern. To better gauge the characteristics of the Si FET with ultra-short channel, we have also fabricated devices with longer Si channels with the same gate dielectric layer. As suggested in ref. [39], we perform a post-metal-gate annealing step for 60 seconds in forming gas at 300 ºC to passivate the interface traps at the Si/HfO_2 interface. This treatment step consistently improves the gate control on the channel so that both the on current and inverse

subthreshold slope (SS^{-1}) were substantially improved (see supporting information Figure 2.10 for a comparison).

Transfer curves (both in linear scale and log scale) of Si NW FET with channel lengths, L_G=17 nm, 250 nm and 1.5 μm are shown in Figure 2.4d-f. As the transistor channel length is scaled down, the on-current I_{on} at V_{ds}= -1 V increases from 7uA (L_G=1.5 μm) to 23uA (L_G=250 nm) and finally to 27 uA (L_G=17 nm). This trend is intuitively expected, since we are measuring current from a shorter Si segment at the same bias; this trend however does not scale linearly as we will discuss below. The series resistance of the nickel silicide S/D extension can be neglected even in our shortest channel devices, based on electrical measurement of a fully silicided Si NW of the same length as well as calculation of the resistance using known resistivity values of nickel silicides from literature (see Table 2.1 and Figure 2.8 in supporting information for more details).



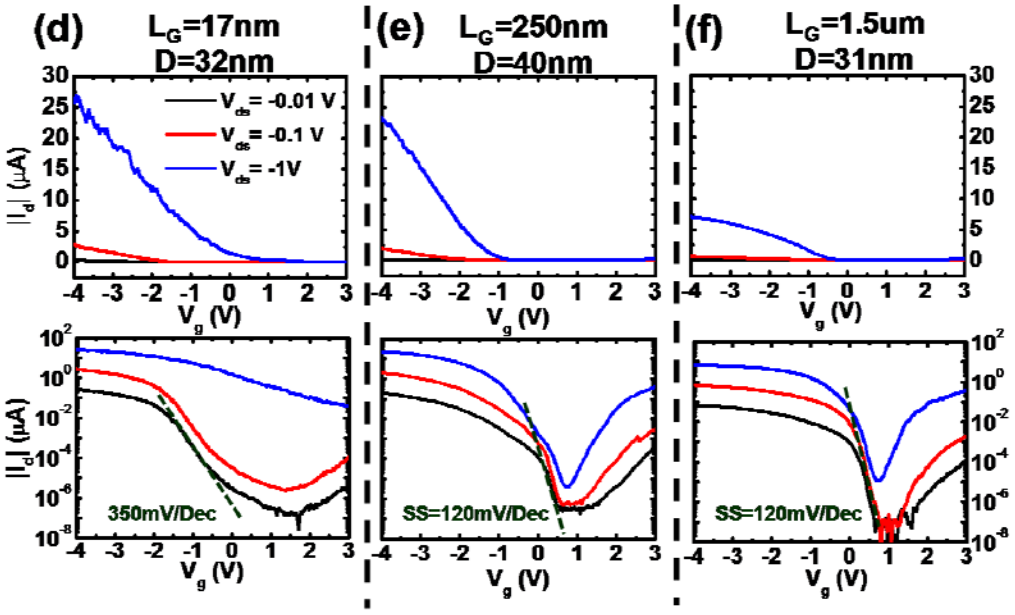


Figure 2.4 (a) Schematics of the top-gate FET device with ultra-short silicon channel (Si nanogap) (b) TEM image of a 17 nm silicon channel. Scale bar is 20 nm. (c) TEM bright field image of a top gate Si NW SB-FET fabricated on silicon nitride membrane. (d-f) Transfer curves with both linear (top panels) and log (bottom panels) for devices with channel length of 17 nm, 250 nm and 1.5 μm, and diameters of 32 nm, 40 nm and 31 nm, respectively. The V_{ds} in each plot from low to high are -0.01 V (black), -0.1 V (red) and -1 V (blue).

The increase in on-current is desirable because it allows faster operation of logic circuits (or lower power consumption if the current is held constant at a reduced supply voltage). On the other hand, the SS^{-1} degrades from 120 mV/Dec for L_G=250 nm channel device to 350 mV/Dec for L_G=17 nm ultra-scaled channel device. The off-state leakage current also increases in the 17 nm device. The I_{off} and SS^{-1} degradation are attributed to insufficient gate control over the NW channel electrostatics in such devices with close proximity of S/D when

switching the device off. We note here that our NW has a diameter of 30 nm. Both SS^{-1} and I_{off} are expected to be improved if a thinner NW (thin body) was used.

Higher on-state conduction is one of the motivations that drive the semiconductor industry to devote increasing endeavors in down-scaling of the MOSFET channels. To assess the on-state performance as a function of channel length, we use the maximum transconductance g_m (V_{ds}= -1 V) as a figure-of-merit and compare experimentally extracted values from 64 devices with those obtained from transport simulations. In long channel approximation, g_m is inversely proportional to L_G and is given by

$$g_m = \frac{\mu_h V_d C_G}{L_G^{\,2}} \tag{2.1}$$

where g_m is the maximum transconductance of an individual device, μ_h is the hole mobility, L_G is the channel length, V_d is the drain bias and C_G is the gate capacitance. To correlate the geometrical factors of the gate capacitance, we developed an empirical formula for Ω-gate capacitance, C_G^{Ω}, by curve fitting to capacitance values obtained from finite element simulations,

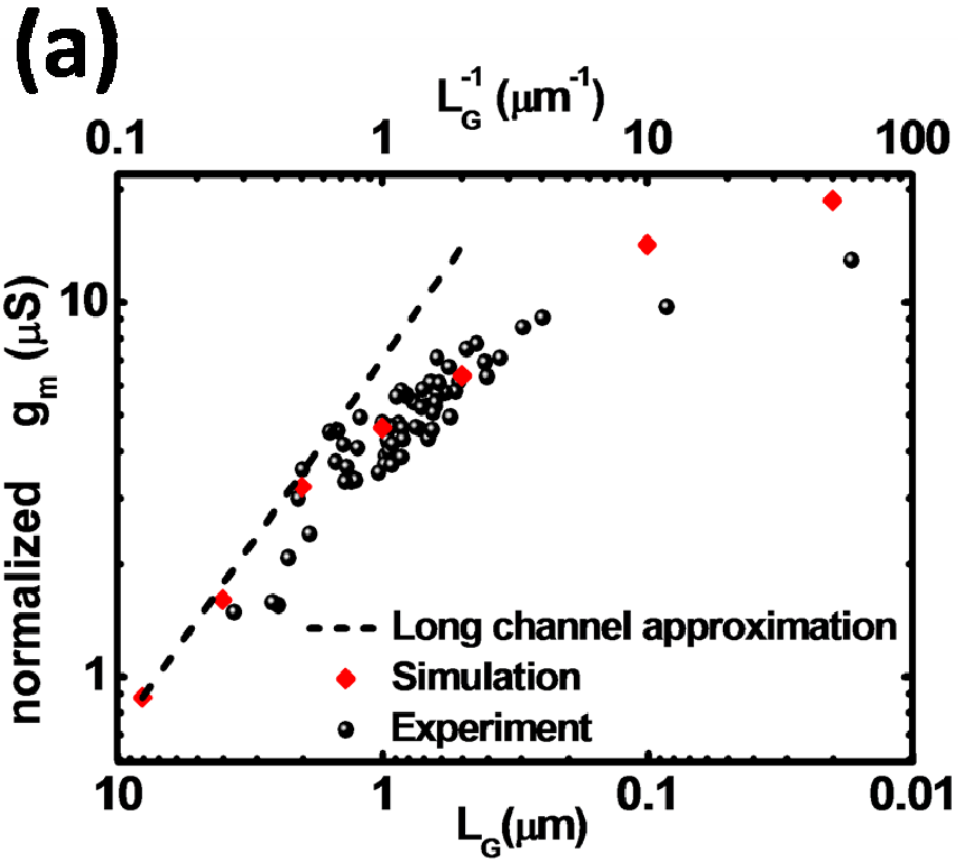
$$C_G^{\Omega}(h,r) = L_G\left[2\pi - 2\,\mathrm{acos}\left(\frac{1-h/r}{1+h/r}\right) + a\cdot(h/r) + b\cdot(h/r)^2\right]\varepsilon_0\varepsilon_r \,/\, \ln\left[1+h/r\right] \tag{2.2}$$

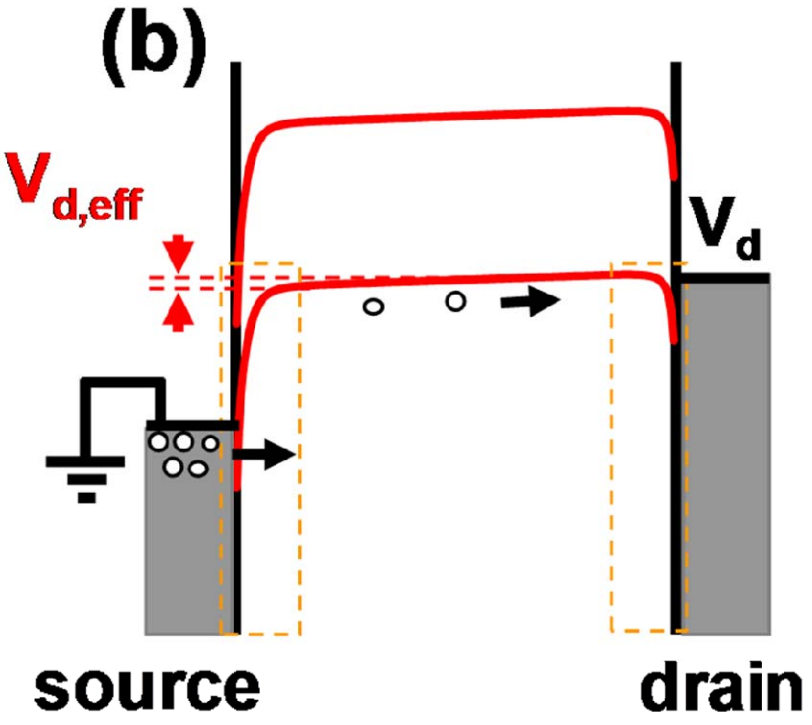
Here, r is the radius of the NW, h is the dielectric layer thickness, ε_r is the relative dielectric constant of the gate insulator layer. In a top-gated NW FET, the gate covers a portion of the surface of the NW. The term $2\mathrm{acos}\left(\frac{1-h/r}{1+h/r}\right)$ accounts for the central angle of the uncovered circular sector of the NW cross-section by the gate metal. $a\cdot(h/r)$ and $b\cdot(h/r)^2$ are first and second order correction terms of the tangential fringing fields.

Equation (2.2) reduces to the well known cylindrical capacitance $C_G(h,r) = 2\pi L_G \varepsilon_0 \varepsilon_r / \ln\left[1 + h/r\right]$ with a fully surrounded gate (first two terms in brackets of Equation (2.2)= 2π), and in the absence of asymmetric fringing fields (a=b=0). For the case of thin dielectrics in a Ω-gate configuration ($h/r < 1$), the fringing field parameters were found to be $a = 2.086$ and $b = 0.852$ which yields capacitance values that are within 2% error of those obtained from 2D simulations. In the extreme of $h/r \ll 1$, the gate capacitance can be approximated by a parallel plate capacitor with curved surfaces, and therefore the tangential fringing fields can be neglected. In the simulation, we found that the gate capacitance increases by only 2.6% when the substrate dielectric constant increases from 3.9 to 22, which implies that the substrate (nitride TEM membrane) stray capacitance is not important. The axial fringing fields may affect the gate capacitance when the channel is very short (or S/D electrodes are very close). However, the change of capacitance per unit length due to axial fringing fields is less than 3% even when the channel length shrinks down to 15 nm (Figure 2.9, supporting information). Therefore, our comprehensive simulations ensure a wide applicability of Equation (2.2). To compare different devices whose diameters vary in the range of 30 – 50 nm, we normalize our experimental transconductances with respect to the gate capacitance of a virtual reference device (40nm in diameter, top gate device with 10nm HfO_2 gate dielectric) using the formula:

$$g_m^{normalized} = g_m \frac{C_G^{ref}}{C_G} \tag{2.3}$$

where $C_G^{ref} = C_G^{\Omega}(h = 20nm, r = 20nm)$, and $C_G = C_G^{\Omega}(h,r)$.


(a)
L_G^{-1} (μm^{-1})
0.1
1
10
100
normalized g_m (μS)
10
1
Long channel approximation
Simulation
Experiment
10
1
0.1
0.01
L_G(μm)


(b)
$V_{d,eff}$
V_d
source
drain

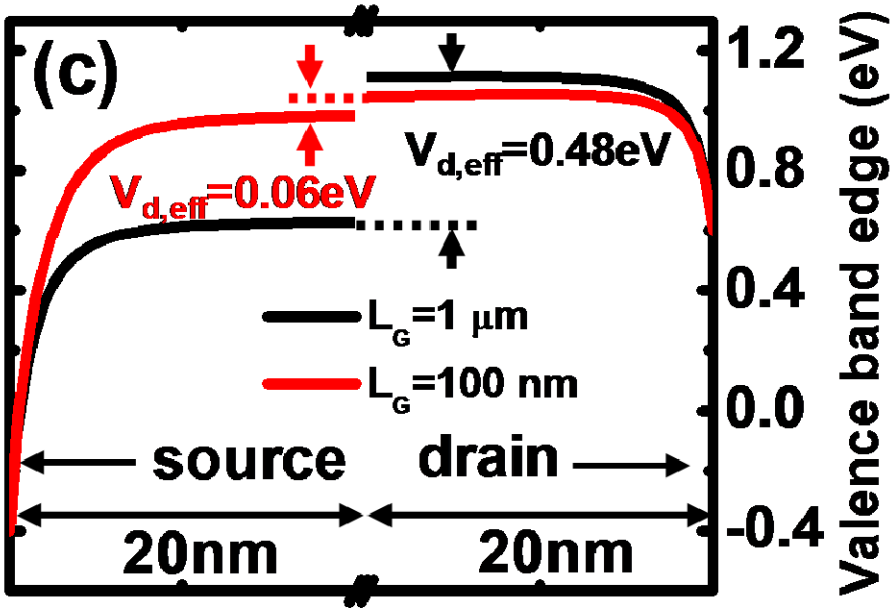


Figure 2.5 (a) Double log plot of normalized maximum transconductance as a function of channel length. Each black small circle represents measured transconductance from an individual experimental device, and large red diamonds represent extracted transconductance from simulated devices with different channel lengths. The dashed line describes the trend predicted by the long channel approximation from (Equation (2.1)). (b) Axial band diagram near the surface of a 100 nm channel device in the on-state. The valence band profile can be divided into 3 regions (from left to right): source SB region, channel region, and drain SB region. Both of the SB regions are highlighted by dashed boxes. The voltage drop across the channel region is denoted as $V_{d,eff}$ (c) Comparison of the valence band profile at the source/drain SB region (i.e., the part of the device highlighted by dashed boxes in (b)) of devices with 100nm and 1μm channel lengths during on-state operation (V_{ds}= -1 V, V_g= -4 V). $V_{d,eff}$ in the 100nm channel length device is a small fraction of the total source/drain bias.

To validate the on-state characteristic trend observed in the experimental devices, we

have performed device simulations for the same experimental channel length range using Silvaco Atlas software package. The transport model for Schottky contact is essential in this simulation, and it implements the model described in ref. [40], which treats the tunneling current through the Schottky barrier as carrier generation and recombination process in the barrier region, and the model can be extended for sub-50 nm channels. Diffusion-drift model, along with energy balance equations, which account for hot carrier effects, were solved for both carriers. The mobility model is taken after ref. [41], which accounts for velocity saturation at high parallel fields (along channel length), and surface roughness scattering as a function of perpendicular field, which was calibrated against the Si universal mobility curve. We assumed a gate-all-around geometry for gate capacitance in the simulation, and $C_G = \frac{2\pi\varepsilon_r\varepsilon_0}{\ln(1+h/r)}$ was used in Equation.(2.3) to normalize simulated devices to the reference device. The normalized maximum transconductance $g_m^{normalized}$ as a function of channel length for both measured and simulated devices is plotted in Figure 2.5a. Each black circle represents a $g_m^{normalized}$ for a single experimental device (in total 64 devices with different channel lengths), and the larger red diamonds are data points extracted from simulations. The trend predicted by the long channel approximation (Equation (2.1)) using $C_G^{ref} = C_G^{\Omega}(h = 20nm, r = 20nm)$, is represented by a dashed line in Figure 2.5a. Both of the experimental and simulated devices show deviation from the predicted enhancement of $g_m^{normalized}$ according to Equation (1), with shorter channel lengths. While this deviation is expected in conventional short channel FET devices (e.g. due to S/D series resistance), it manifests itself in a different and more significant physical behavior in SB-FETs.

To explain the origin of maximum transconductance deviation from long channel approximation in SB-FETs, we plot the energy band-edge diagrams along the NW axis in Figure 2.5b, extracted near the surface of devices under on-state bias. In Figure 2.5b, we divide the NW along the axial direction into 3 regions: source SB region, channel region, drain SB region, where the valence band part of the S/D SB regions are highlighted by dashed boxes. For these undoped NWs, the channel region is the part of the device where the potential drops almost linearly (in a band diagram, potential drop manifests in the way of band energy increase). This potential drop is defined as effective voltage drop (denoted as $V_{d,eff}$) across the channel, which maintains the channel field to drive carriers but is reduced to only a fraction of total S/D bias V_{ds}. Quantitatively, we plot in Figure 2.5c the valence band energy profile for devices with different channel lengths (1 μm and 100 nm) along the first 20 nm from both S/D SB regions at V_{ds}= -1 V and V_g= -4 V (on-state). The $V_{d,eff}$ for L_G=1 μm and 100 nm are 0.48 V and 0.06 V, respectively, with the latter only 6% of the applied V_{ds}. In contrast to the channel region, the majority of V_{ds} drops across the source SB for the short channel device, which implies that the contact resistance at the source is dominant in such a device. This is due to the fact that the source Schottky junction is under reverse bias. In the 100 nm channel device, only a small portion of the voltage drops across the channel while most of the voltage drops in the S/D SB region, which leads to a thinner SB compared to that of the 1 μm channel device.

Existence of both source and drain SBs poses a limiting factor on the on-current gain from scaled SB FETs. While the thickness of the SB might be controlled by doping, our

transport simulations showed that I_{on} or g_m can only be slightly improved at doping densities > 10^{18} cm^{-3} whereas the subthreshold characteristics would be degraded (see supporting information Figure 2.11a). In the on-state (V_{ds}= -1 V, V_g= -4 V), the SB depletion region thickness for the three doping concentrations considered here (10^{16}, 10^{18}, and 5×10^{18} cm^{-3}) remains essentially the same, about 7 nm. (see supporting information Figure 2.11b). This indicates that an increase in doping would not be effective in thinning the SBs to enhance I_{on}. On the other hand, increased channel doping is adverse in terms of incurring carrier scattering and difficulty in turning off the device (e.g. Figure 2.11a, 5×10^{18} cm^{-3} curve). There are generally other challenges associated with doping in ultra-short FET devices. One of these include random dopant fluctuation, which in the case of our 17 nm device would cause large device-to-device variation including threshold voltage shift, given that only 12 individual dopant atoms should exist in the channel at a doping level of 10^{18} cm^{-3}. On the other hand, the presence of a reservoir effect [42] in the liquid mediating growth seeds in VLS growth prevents realizing complex and sharp doping profiles. The difficulty to scale down the SB thickness becomes an issue in very short channel NW SB-FETs, which are the most common form of NW or nanotube FET devices [43, 44]. One possible solution is to utilize the 'snow plow' effect that piles up dopants at the silicide/silicon reaction front as the interface moves, to create a highly doped region only close to the contact [45, 46] while keeping the channel undoped for better transport characteristics and gate electrostatic control. However, this requires careful optimization of the silicidation temperature and the growth rate in order to maximize dopant solubility differences in silicon and in the silicide and

maintaining high dopant diffusivity in the silicide, which is yet to be accomplished.

With this comprehensive understanding on potential drops across SB-FET devices, we can now note that the use of Equation (2.1) or its similar forms to extract field-effect mobility from top-gate NW transistors is applicable only if the SB is low [7, 8, 47] or if the channel is long, when almost all of V_{ds} drops across the channel. If Equation. (2.1) is applied to short channel devices (<1 μm) with a moderate SBH, e.g. 0.47 eV for holes in our case, the field-effect mobility will be underestimated [48]. For an accurate mobility extraction, one needs to replace L_g and V_d with their effective values ($L_{g,eff}$ and $V_{d,eff}$) in Equation. (2.1) [49], where $L_{g,eff}$ is the length of channel region (the silicon segment excluding S/D SB region). Although the boundary of SB region may not be well defined, the factor $V_{d,eff}/L_{g,eff}$ in Equation. (2.1) is well defined as the average electric field in the channel, which is insensitive to the choice of SB region boundary.

2.4 Conclusions

This work presents an investigation of VLS Si NW transistors with channel length down to 17 nm, by utilizing controlled nickel silicide formation on an *in-situ* TEM heating stage. Multiple nickel silicide phases grow simultaneously with $NiSi_2$ as the reaction front. The $NiSi_2$/Si metal-semiconductor contacts are type-A interfaces, atomically sharp and therefore have reproducible electronic properties. By combining measured and simulated devices with different channel lengths, our transport analysis shows that the SBs take up the majority of the applied S/D bias when the channel length is scaled down to sub-100 nm region, and the on-state performance deviates from the trend predicted by long channel approximation. This

result implies that the Schottky barrier contact engineering is vital to best fulfill performance gains in short channel SB-FETs. In addition, analysis that follows long channel approximation may underestimate the field effect mobility in short channel SB-FETs.

2.5 Supporting Informations

Details on native oxide etching prior to silicidation experiments, HR TEM analysis on a 12 nm ultr-short channel device, evaluation of the silicide series resistance from known silicide values and from our experiment, comparison on full 3D simulations and 2D simulations for the Ω-gate capacitance, as well as effects of post-metal gate annealing on device characteristics, and simulated transfer curves for devices with various channel doping levels and their correspondent band-edge diagrams are described below.

Etching of native oxide on Si NW channel:

The native oxide on Si nanowire channel is subjected to 300 keV electron beam radiation in TEM, which may create defects in this dielectric layer or Si/oxide interface and degrade the gate control over the channel. We went through a special process to remove the native oxide on Si channel before introducing the sample into TEM chamber.

A straightforward dip in buffered oxide etch (BOE) will result in dissolution of Si nanowire (Figure 2.6a, supporting infromation) through the following two-step reaction[24, 50]:

$$Ni + 2H^{+} \rightarrow Ni^{2+} + H_2 \qquad (2.4)$$

$$2Ni^{2+} + Si + 6F^{-} \rightarrow 2Ni + SiF_6^{2-} \qquad (2.5)$$

To prevent supplying Ni ions from reaction (2.4) to reaction (2.5), we pre-coat an amorphous Si layer to protect Ni electrodes during the BOE etching (Figure 2.6b,d). The

BOE is diluted with 6 part water and the etch time is 20s, which is calibrated to remove about 3.5 nm of the thermal oxide. With a-Si protection layer, the Si NW is intact after BOE dip as demonstrated in Figure 2.6c.

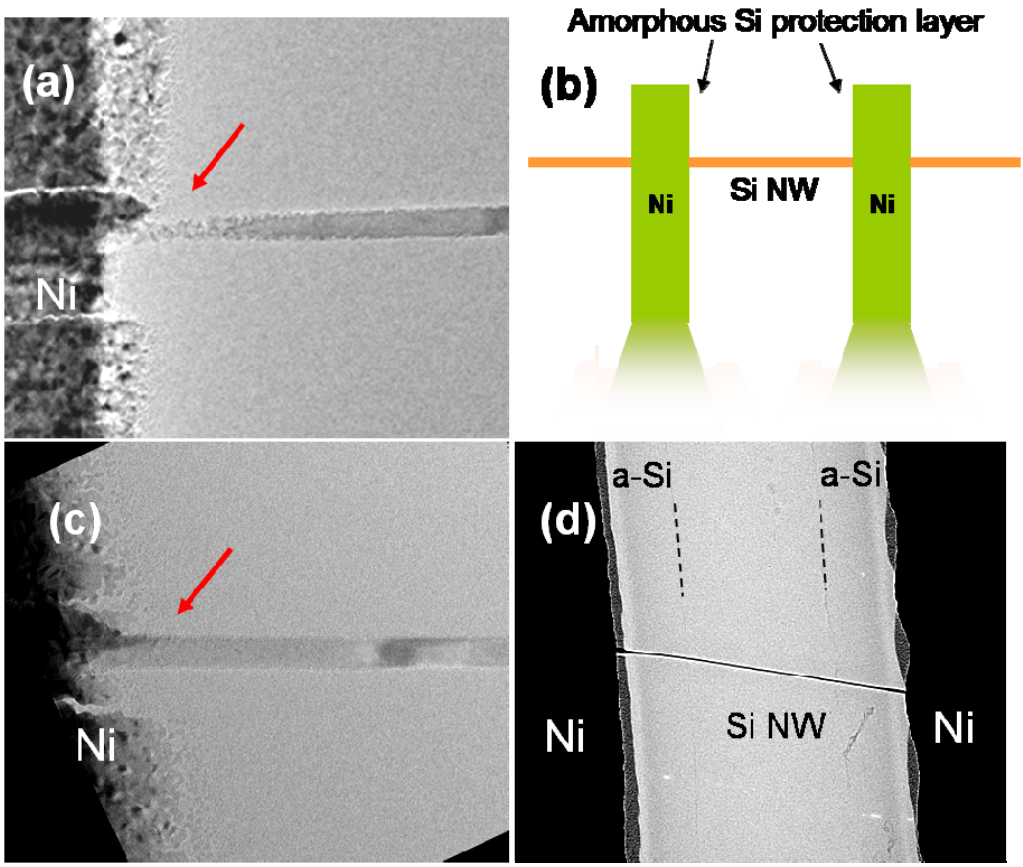


Figure 2.6 (a) The unprotected segment of the Si NW close to the Ni contact is etched during a BOE dip. (b) Top-view cartoon illustrating the use of a PECVD amorphous silicon layer to protect Ni from the BOE etchant. (c) With an amorphous Si protection layer, the Si NW remains intact after a BOE dip as highlighted by the red arrow, which contrasts the situation of the unprotected NW in (a). (d) A low magnification TEM image showing the a-Si protection layer whose boundary is highlighted with dashed black-lines.

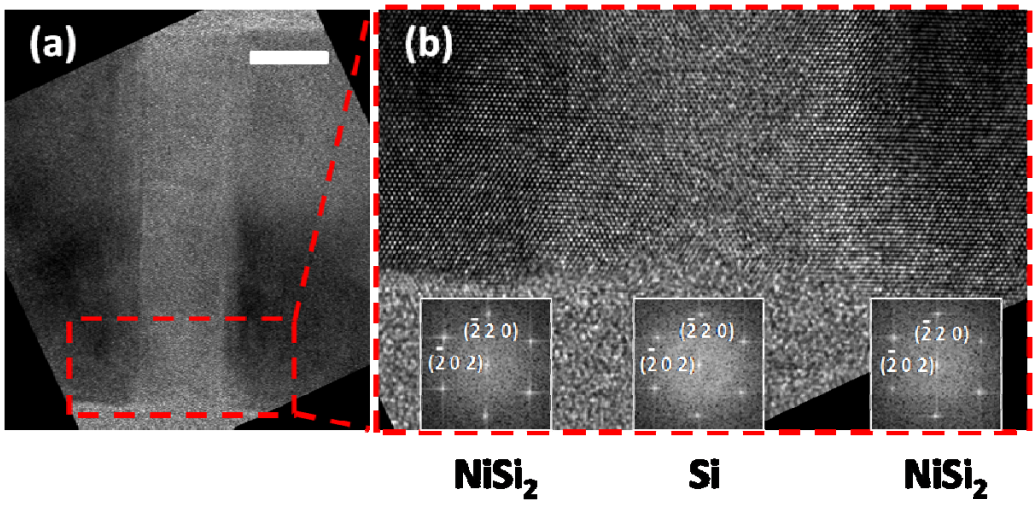


Figure 2.7 (a) a short Si channel. The scale bar is 10nm. (b) HRTEM image of the source/channel and drain/channel interface, showing the leading phase is $NiSi_2$ even when the channel is very short.

Evaluation of serial resistance of nickel silicide S/D extension segment:

In the on-state of our shortest channel (17 nm) device, and channel resistance translates to 37 kΩ. We experimentally determined the resistance of a fully silicided nanowire of the same length (Figure 2.8a,supporting information), as 1.3 kΩ, using two-terminal measurement. In addition, we combine the phase information obtained from TEM and resistivity value from Table S1 to calculate the total resistance of a fully silicided nanowire segment of the same length as 856 Ω. Both results imply that the S/D serial resistance is negligible compared with the channel resistance of all our devices investigated.

phases	crystal system	a/Å	b/Å	c/Å	density g/cm3	V per Si atom Å^3	Resistivity μΩcm
$Ni_{31}Si_{12}$	hexagonal	6.671	-	1.228	7.56	39.6	60*
δ-Ni_2Si	orthorhombic	4.99	3.72	7.06	7.37	32.8	25*
θ-Ni_2Si	hexagonal	3.836	-	4.948	7.88	30.7	25***
NiSi	orthorhombic	5.175	3.332	5.609	5.97	24.1	13*
$NiSi_2$	cubic	5.395	-	-	4.83	19.7	24**
Si	cubic	5.430	-	-	2.33	19.9	-

* values taken from reference [51]

** value taken from reference [52]

*** We did not find a resistivity value for θ-Ni_2Si. Therefore, we assume the resistivity of θ-Ni_2Si is the same as δ-Ni_2Si.

Table 2.1Structural data and electrical resistivity of various type of nickel silicide phase

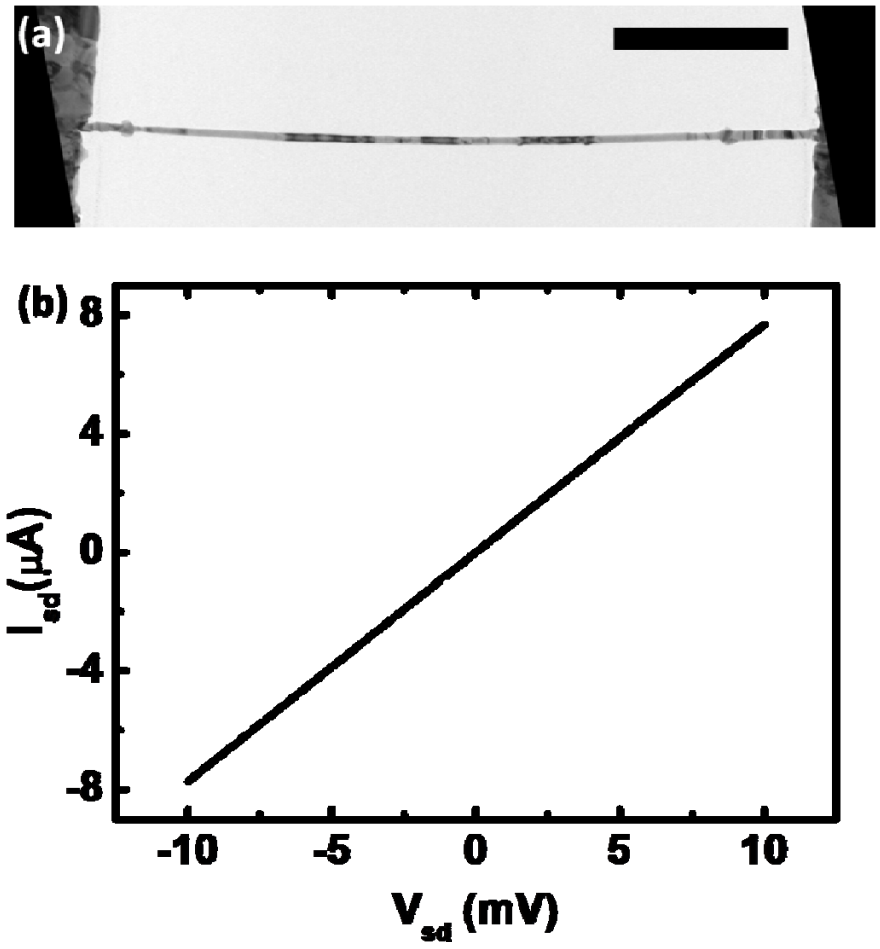


Figure 2.8 (a) a fully silicided Si NW. The scale bar is 1μm (b) Corresponding two terminal IV

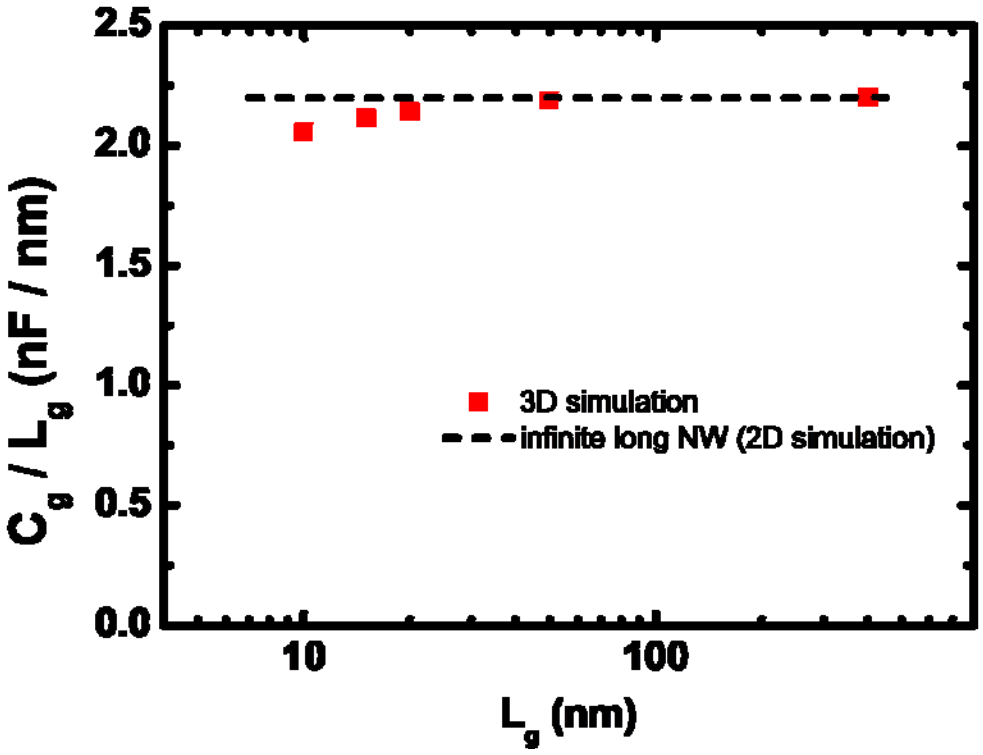


Figure 2.9 The gate capacitance per length obtained from full 3D simulation of NW with different channel lengths and the asymptotic limit of infinite long NW by 2D simulation.

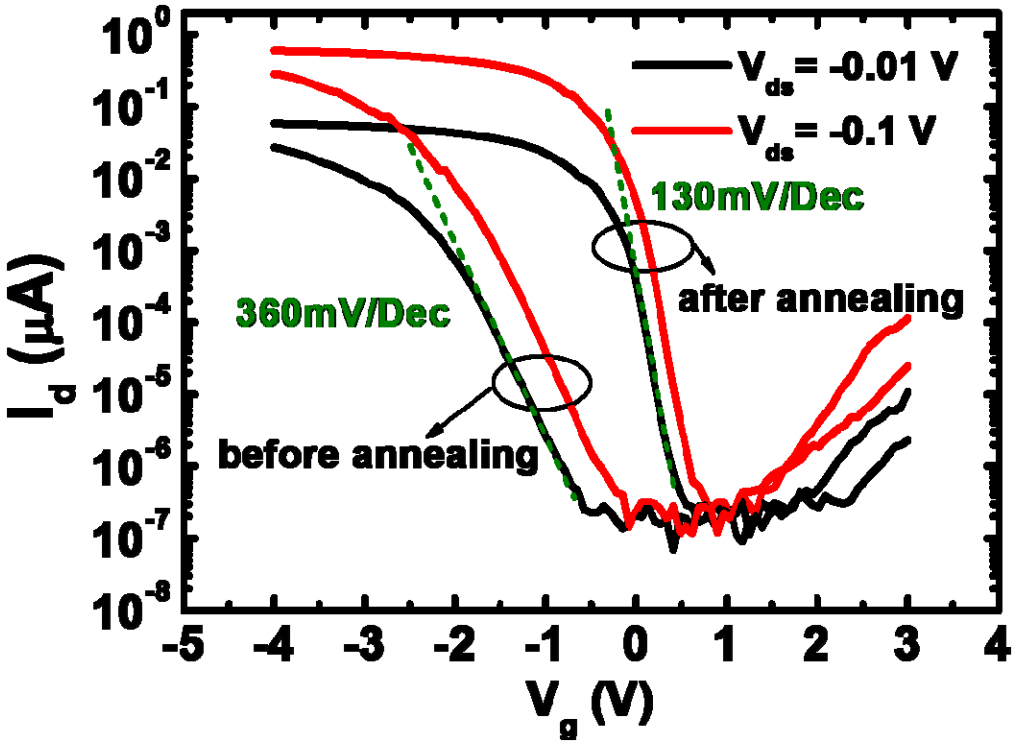


Figure 2.10 Post-metal-gate annealing in forming gas at 300ºC for 1min helps to improve on-current and inverse subthreshold slope. The channel length is 0.83 μm and the NW diameter is 35 nm.

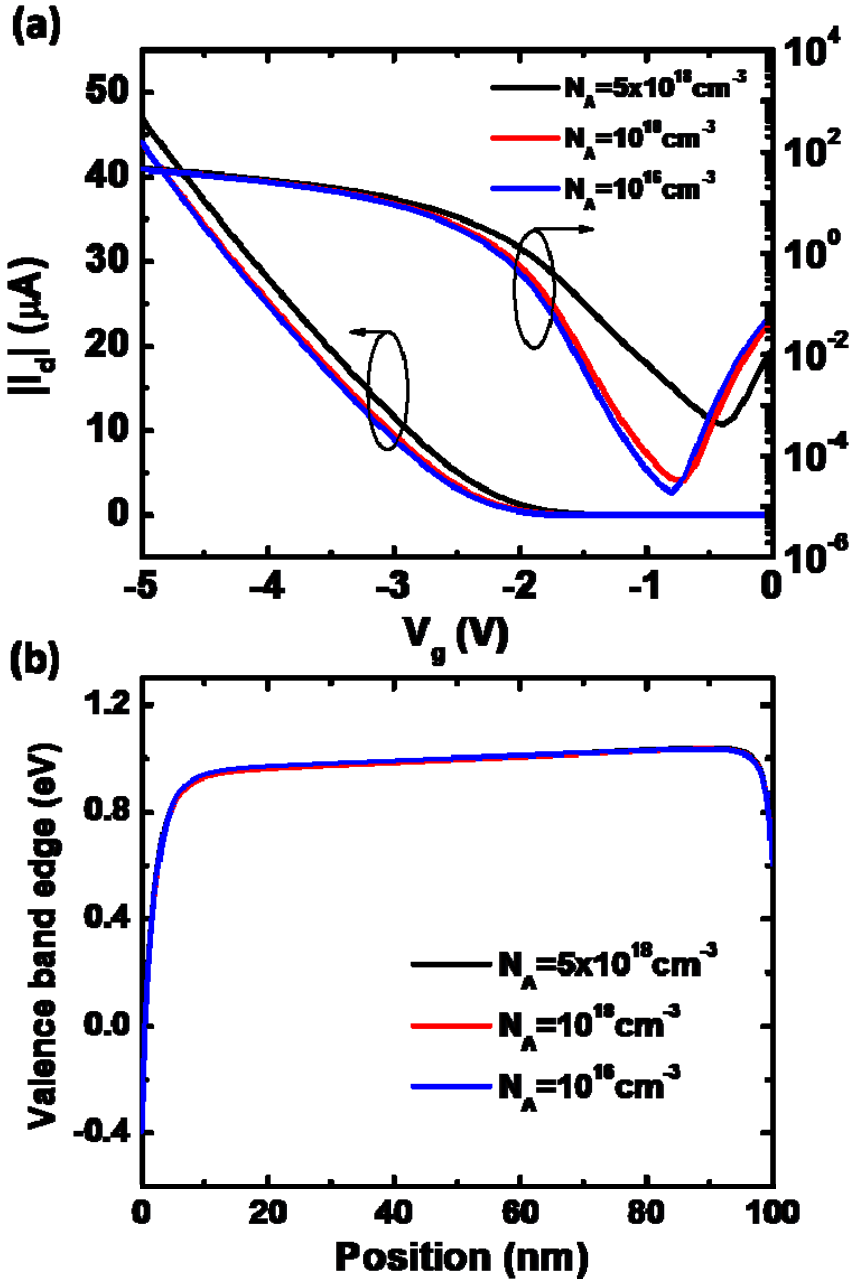


Figure 2.11 Comparison of simulated devices with 10^{16} cm^{-3}, 10^{18} cm^{-3} and 5×10^{18} cm^{-3} p-type doping densities: (a) Transfer curves, and (b) valence band-edge profiles in the on-state (V_{ds}=-1V, V_g=-4V).

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Chapter 3 : Gold Catalyzed Nickel Disilicide formation: A New Solid-Liquid-Solid Phase Growth Mechanism

3.1 Introduction

As demonstrated in the previous chapter, Si NWs grown by vapor liquid solid (VLS) growth mechanism can be used in fabrication of devices with very short channels. The NW device geometry has been intensively investigated because of the possibility to form gate-all-around structure so as to maximize the electrostatic control of gate to the channel, relieve the short channel effect and carry on the trend of transistor miniaturization. In addition to Si, VLS mechanism has been extensively used to grow Ge, III-V semiconductor NWs and hetero-structures, which has demonstrated potential wide applications in nanoscale electronic [1, 2] or opto-electronic device [3-6].

In VLS growth, gold is frequently used as the catalyst. To illustrate its importance, we use the growth of Si NW as an example. In order to grow a single crystal Si solid phase, an intermediate liquid phase is important to maintain Si atoms sufficiently mobile while finding their lowest energy crystal sites at the growth front. Introduction of gold can reduce the Si liquification temperature significantly from Si melting temperature (1414 ºC) to Au-Si eutectic temperature (363 ºC). In comparison, to grow defect-free single crystalline Si directly from gas phase (e.g. MBE growth), the substrate has to be substantially heated above 800 ºC [7] in order to maintain high diffusivity of Si on the surface of epitaxial layer.

In addition to the application of nickel silicide contacts in fabricating devices, we are also

interested in the fundamental material science in Ni-Si reaction. As-grown VLS Si NWs always have Au tips at one end of the NW (Figure 3.1)

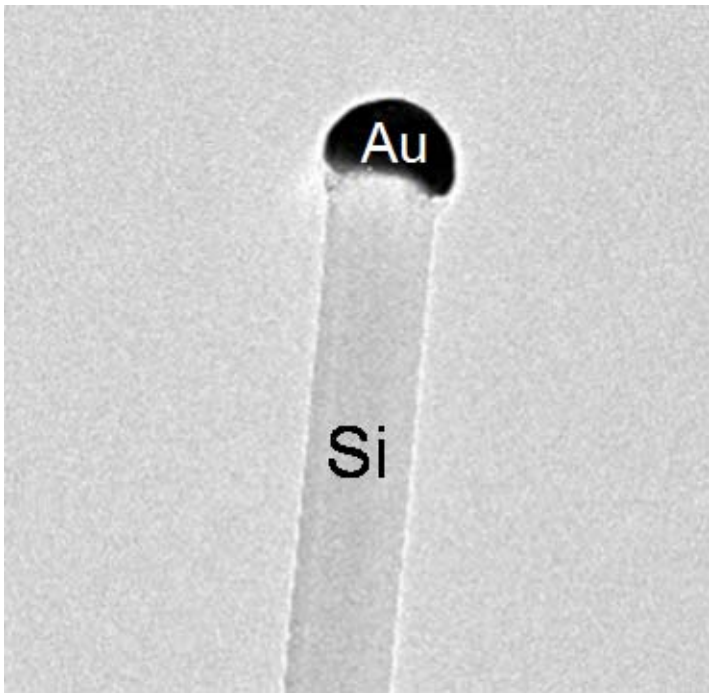


Figure 3.1 Gold tip on a VLS grown Si NW

. We are interested in the role of Au in the Ni-Si reaction. In this chapter, we report our detailed *in-situ* TEM studies on gold catalyzed $NiSi_2$ formation within Si NWs, which first demonstrates that the concept of catalytical liquid mediating growth (similar to VLS) is also applicable to metallic NW formation. The growth is well-attributed to a solid-liquid-solid (SLS) mechanism and it will be discussed in details later. The Au particles on the tip of Si NW are in-place catalysts for the subsequent SLS growth when Si NW reacts with Ni nano-particles (NPs).

3.2 Experimental

To enable *in-situ* TEM monitoring of the reaction, we use 30nm silicon nitride TEM membrane as the substrate, which is transparent to the electron beam. Figure 3.2 summarizes the sample preparation steps. A thin layer of Ni (6 nm) was deposited, followed by annealing at 650 ºC in forming gas for 2 min to break the film into Ni nano-particles (NPs), whose diameters are generally around 100 nm. VLS grown Si NWs were subsequently dispersed onto the membrane to make random contact to the Ni NPs. The whole substrate is then mounted on Gatan 628 single tilt heating stage and transferred into TEM (FEI Tecnai F30) chamber. The temperature of the heater is measured by thermo-couple and can be manually controlled by an external current source. Unless otherwise specified, the temperature of the heating stage was kept at 700 ºC as a isothermal treatment to trigger the reaction between Ni and Si. TEM images are continuously captured in real time and compiled into videos.

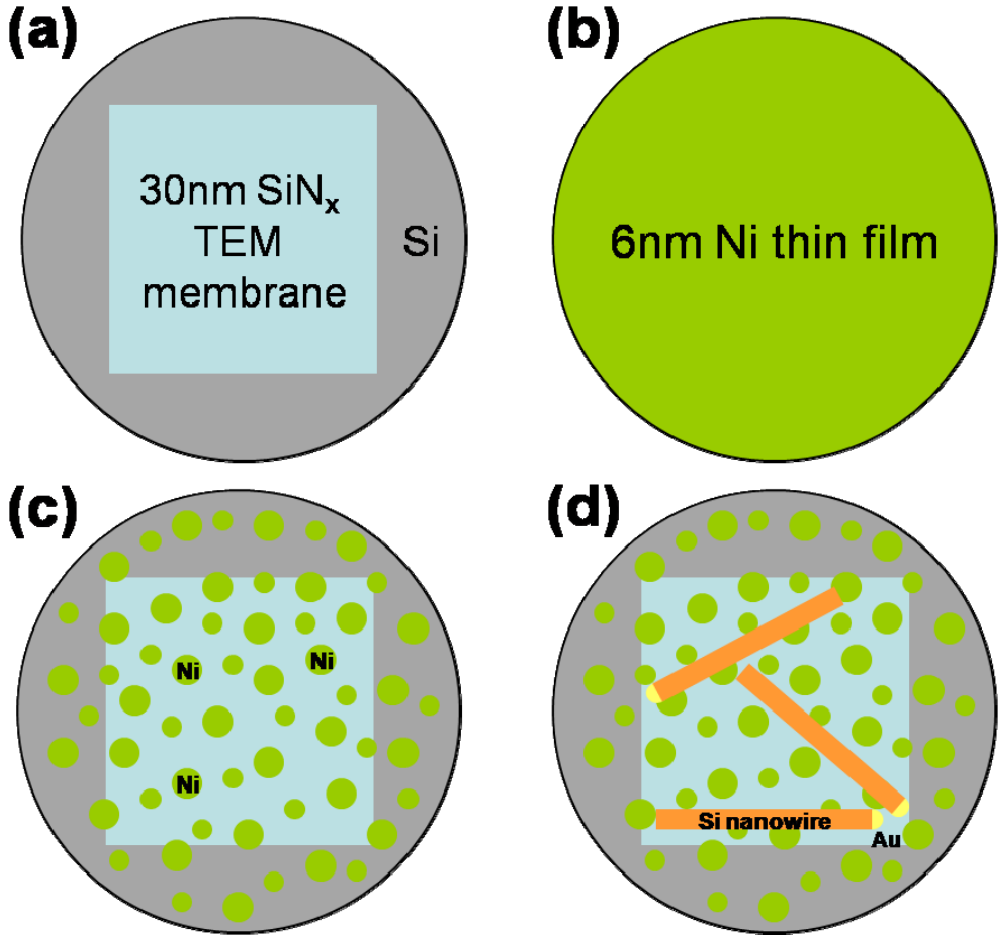
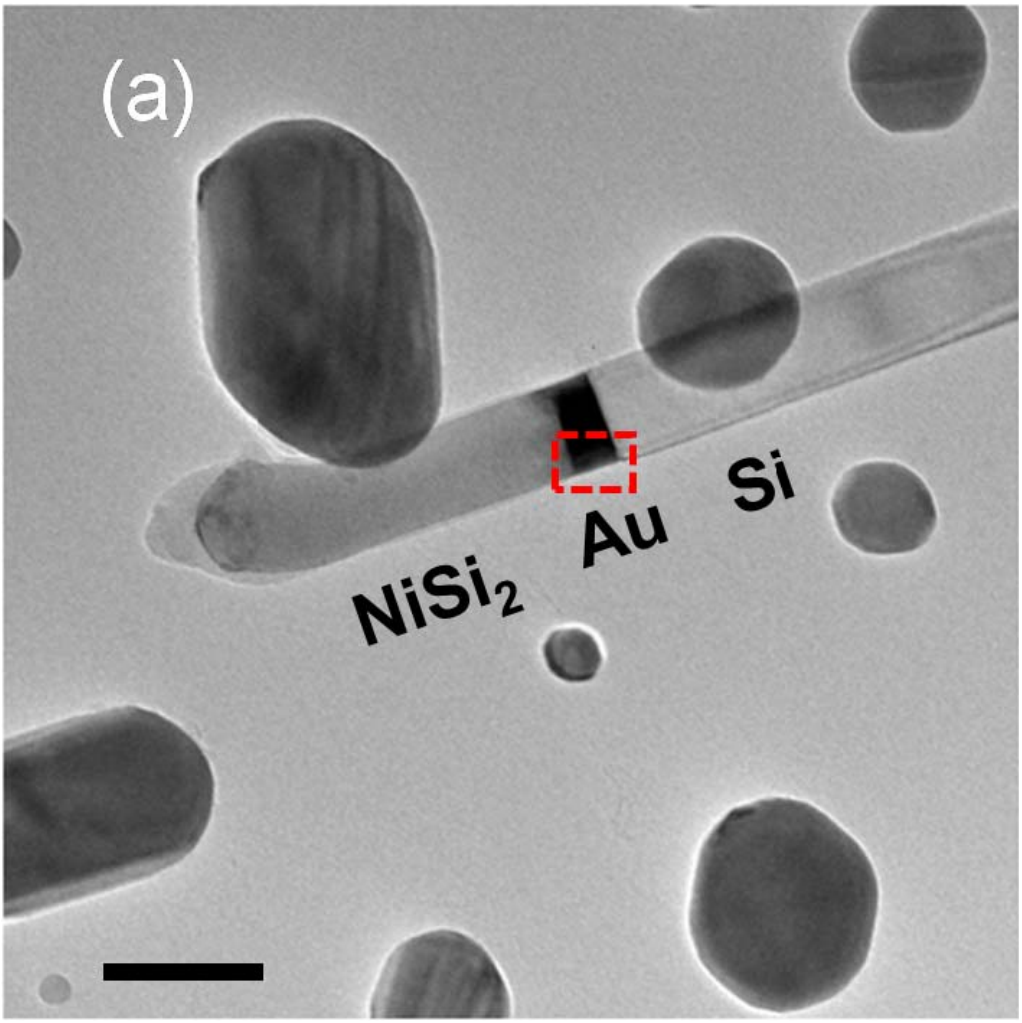


Figure 3.2 (a) 30 nm thick silicon nitride TEM membrane (b) Deposition of 6 nm Ni thin film by e-beam evaporation (c) Annealing of Ni thin film at 650 ºC and breaking it into Ni nanoparticles (d) dispensing Si NWs in random contact with Ni nanoparticles. The tip have a drop of Au

3.3 Results and discussion



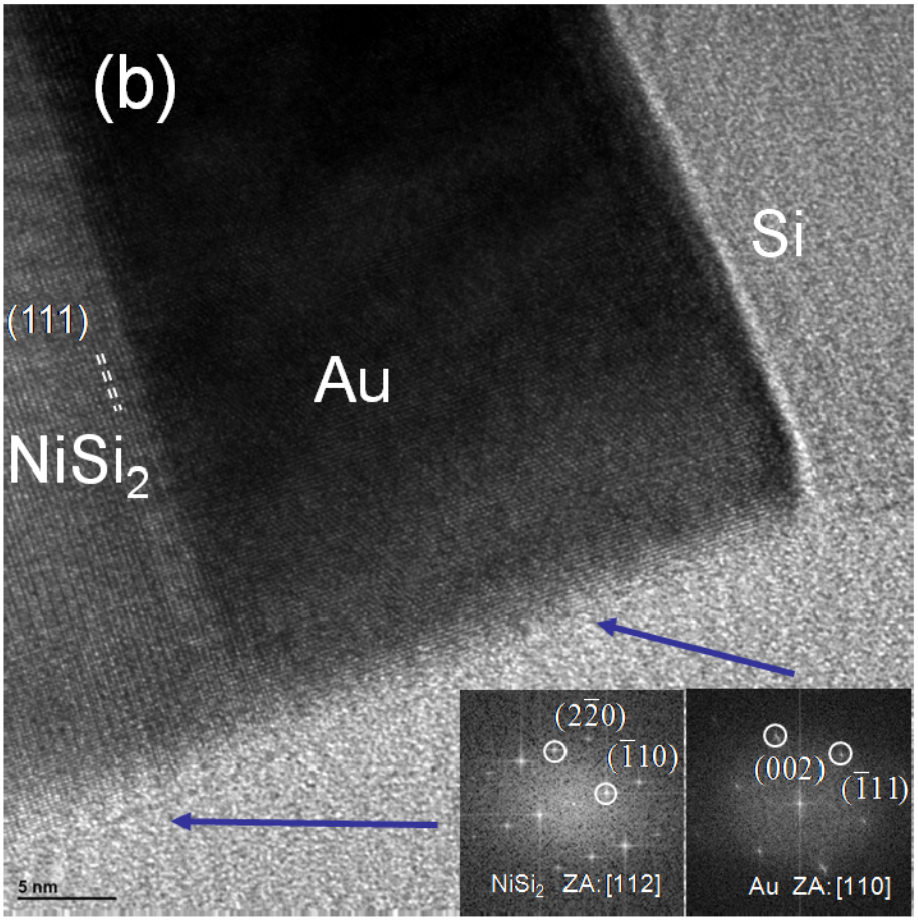
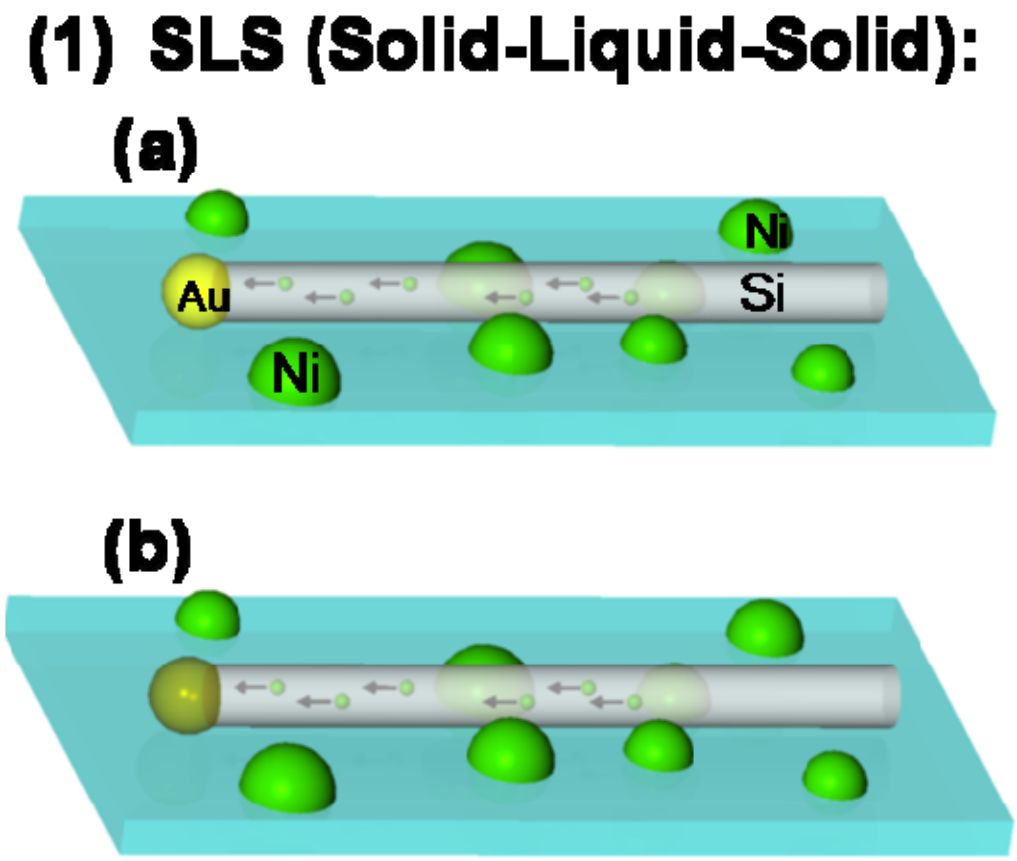


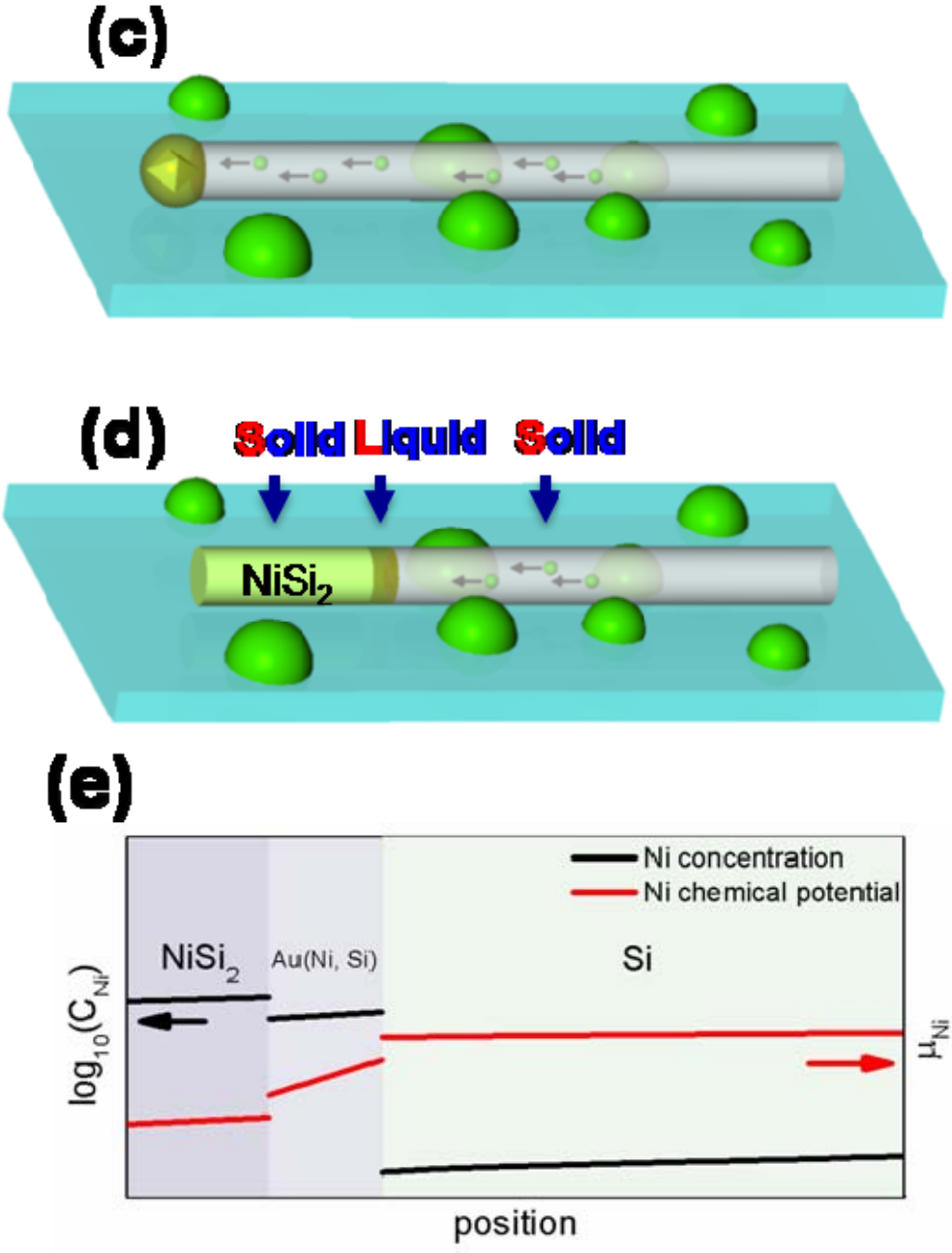
Figure 3.3 (a) TEM bright field image showing $NiSi_2$ forms from the tip of the nanowire with gold moving towards the opposite end. Scale bar is 100 nm (b) HRTEM image of the area around Au. The reaction front is $NiSi_2$ (111) plane

Figure 3.3a shows an example of a Si NW partially transformed to nickel silicide after being held at 700 ºC for 50 mins. Surprisingly, the silicide segment growth initiates from the tip of the NW, with the Au particle moves towards the other end of the NW at the same time. Here, nucleation of the silicide NW does not occur at the Ni/Si contact, which is similar to several recent studies on nanoscale silicide formation [8, 9]. High resolution (HR) TEM

image (Figure 3.3b) shows that the nickel silicide phase is $NiSi_2$, and $NiSi_2$ (111) plane is its growth front. Details about the initial stage of $NiSi_2$ formation and continuous growth of $NiSi_2$ in a steady state will be presented in later part of the thesis as supports to the above proposed process.

3.3.1 Solid-Liquid-Solid (SLS) $NiSi_2$ growth process




(c)
(d)
Solid Liquid Solid
NiSi2
(e)
Ni concentration
Ni chemical potential
NiSi2
Au(Ni, Si)
Si
log10(CNi)
μNi
position

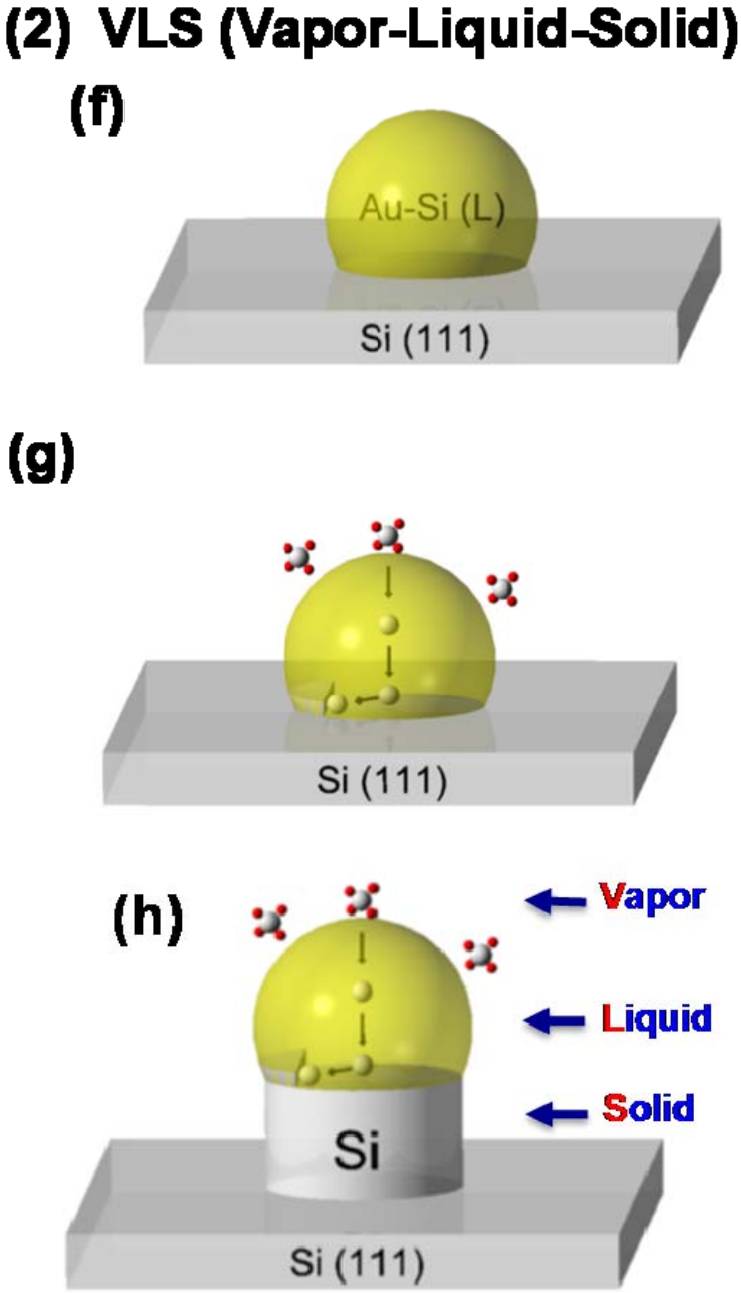


Figure 3.4. (1) SLS growth (a) Ni diffusion and accumulation in the Au-Si eutectic alloy. (b) Formation of a liquid Au-Ni-Si ternary alloy at the Si NW tip (c) Nucleation of a single $NiSi_2$ crystallite (d) Continuous growth of NiSi2 in a steady state (e) Schematics of Ni concentration and chemical potential when SLS growth reaches a steady state (2) VLS growth (f) Eutectic alloying

between Au particle and Si substrate (g) Supersaturation and nucleation of a Si step in Au-Si eutectic alloy (h) Continuous growth of Si NW in the steady state;

We attribute the gold catalyzed nickel disilicide formation as a solid-liquid-solid (SLS) mechanism. In SLS growth of $NiSi_2$, Ni atoms dissolved from Ni NPs into the Si NW and interstitially diffuse to and accumulate in Au tip of the NW (Figure 3.4a). Upon supersaturation of both Si (available from the Si NW itself) and Ni in the Au-Ni-Si ternary liquid alloy (Figure 3.4b), a single solid octahedral shape of $NiSi_2$ crystallite nucleates from the liquid alloy (Figure 3.4c). After that, the Au alloy continues to receive incoming Ni atoms from one end and precipitate $NiSi_2$ at the other end, when the growth reaches the steady state (Figure 3.4d).

Detailed understanding of this phase formation requires complete knowledge on the Au-Ni-Si system ternary phase diagram, which is still lacking in the literature. However, we can derive qualitative information from their binary phase diagrams. In the binary Au-Ni system, their solid phases are consolute above 816ºC and also appreciably soluable to each other at lower temperature, which implies a low enthalpy term for their solid solution. In contrast, Ni solubility in Si is negligible ($\sim 10^{15} cm^{-3}$ [10]) even at 700ºC, implying a high enthalpy term. Therefore, Au acts as a Ni getter in the Si NW and tends to absorb incoming Ni atoms supplied from remote Ni sources. Since Si is abundant, growth of $NiSi_2$ phase is therefore limited by Ni atom supplies. Figure 3.4e shows the schematics of chemical potential and Ni concentration profile along the axial direction of the NW when $NiSi_2$ grows with

continuous Ni supplies. To grow one layer of $NiSi_2$, in a NW with 100 nm diameter, it requires 6.2×10^4 Ni atoms. One the other hand, at 700 ºC the number of equilibrium Ni atoms dissolved in a 10 um long Si NW is ~800. The huge different between this two numbers implies that after growth of one $NiSi_2$ step, Ni is subsequently totally depleted in Si and it needs some time to restore supersaturation of Ni in Si and also Au liquid alloy. At this temperature, Ni diffusion in Si is very fast (several microns in one second [11]). At the Ni/Au interface, Au liquid alloy absorbs incoming Ni so that the latter is depleted in the part of Si NW close to Ni/Au interface, which creates a Ni concentration gradient in Si NW and maintain continuous delivery of Ni atoms. Although the Ni concentration increases when it enters Au, the chemical potential drops due to a reduced enthalpy term previously described.

It is interesting to compare the classic VLS mechanism to our new SLS growth mechanism. In VLS growth of Si NW, initially Au particle alloys with Si substrate to form a liquid alloy when the substrated is heated above the Au-Si eutectic temperature (363 °C). Additional Si atoms come from the vapor phase in the form of SiH_4. When Si becomes supersaturated in Au, solid Si phase nucleates (Figure 3.4g) and continues to grow with further SiH_4 supply (Figure 3.4h). VLS and SLS are both liquid mediating, and both precipitate out solid phases. To enable successful liquid mediated solid phase growth, the eutectic melt should have a lower temperature than the melting point of the solid phase that is intended to form. In VLS growth of Si NW, Si melting temperature is 1414ºC, and Au-Si eutectic temperature is 363ºC; while in SLS growth of $NiSi_2$, $NiSi_2$ melting temperature is 997ºC, and the Au-Ni-Si eutectic melt temperature should be below 700ºC, since 700ºC is our

annealing temperature and Au segment does not show any characteristic diffraction spot originated from a crystal at various tilting angles.

The only difference between VLS and SLS growth resides in the mass transport mechanism of source atoms. In VLS growth, the source atoms are supplied in gaseous phase and are driven by differentiated pressure. Usually, only a small portion of the source gases are reacted, while the majority of them are exhausted. In SLS growth, source atoms are delivered through a solid mass conducting media (Si NWs in our case), which occurs only within a very small confined volume and is robust to changes in the environment. In addition, the mass transport is highly directional, potentially improving the use ratio of source materials.

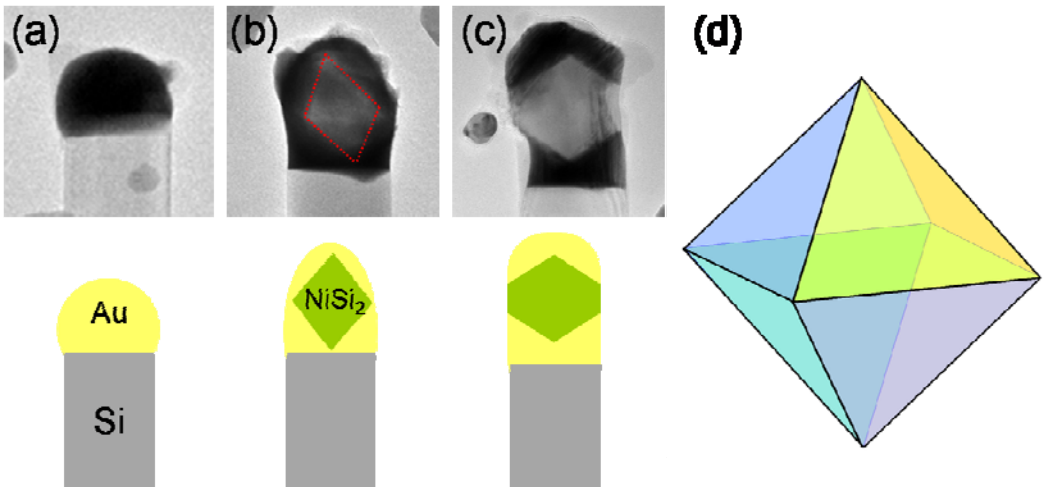


Figure 3.5. (a-c) Emerging and growth of octahedral shape of $NiSi_2$ crystallite from the Au liquid ternary alloy (d) Schematic of a octahedron bounded by 8 {111} facets

3.3.2 Nucleation $NiSi_2$ in Au (Ni,Si) ternary liquid alloy and initial growth stage

By using the *in-situ* TEM techniques, we are able to dynamically observe nucleation and early-stage growth of $NiSi_2$ phase from the Au liquid alloy. Initially, upon heating, the Au tip forms a eutectic liquid with Si NWs and continue to accept incoming Ni atoms (Figure 3.5a). When both Ni and Si reach supersaturation in the Au eutectic liquid, a $NiSi_2$ octahedral shape nucleus (or more accurately crystallite) emerges in the middle of the liquid Au (Figure 3.5b). The liquid state of the Au ternary alloy was confirmed by examining large amount of Au tips at different stages of incubation or nucleation, and no signs of solidification (no surface faceting or diffraction contrast) of the Au ternary alloy were observed. The $NiSi_2$ crystal continues to grow while retaining its octahedral shape until its size reaches the diameter of the NW. At this point, the originally suspended $NiSi_2$ is anchored (Figure 3.5c) at the boundary of the Si NW, and split the Au liquid into two parts (the part at the tip and the liquid mediating layer at the other side of the $NiSi_2$ crystal).

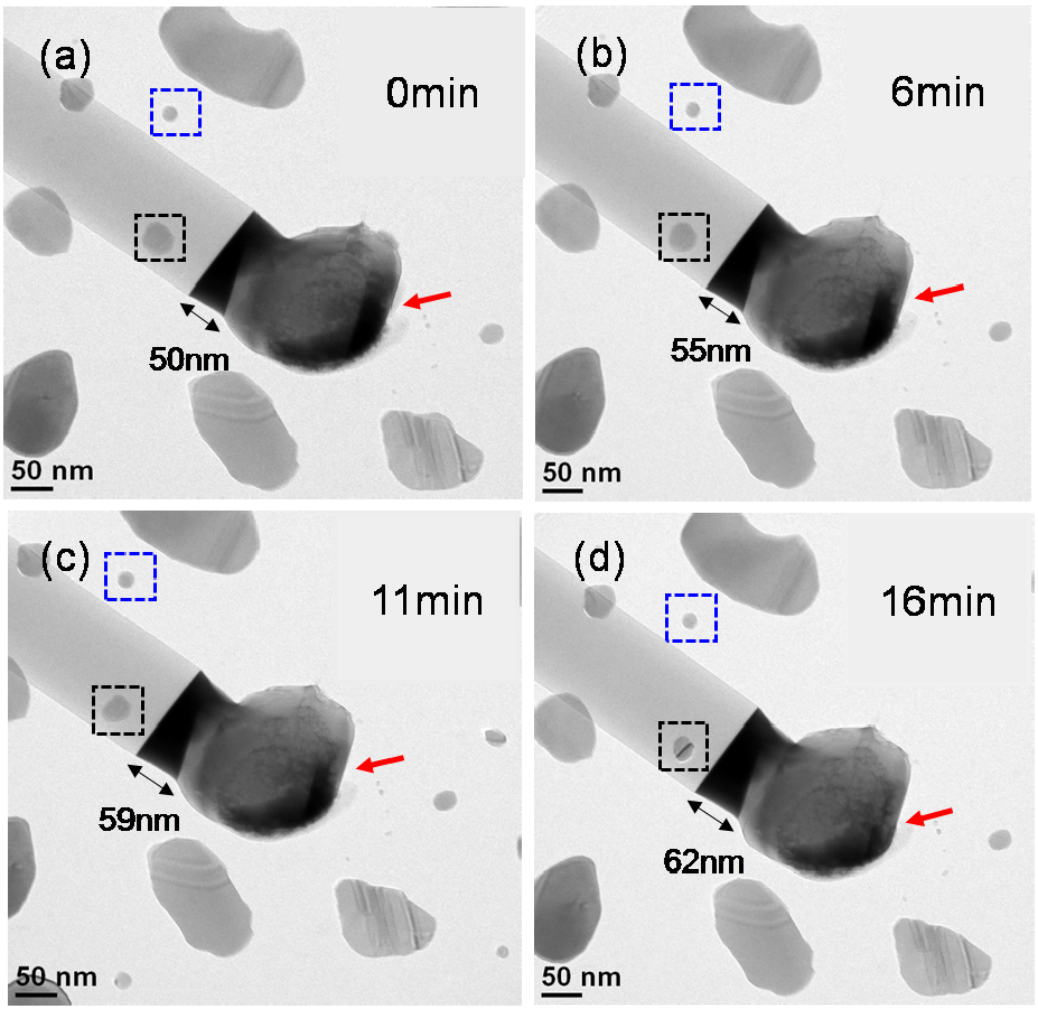


Figure 3.6. (a-d) *In-situ* TEM snapshots showing (i) Gradual disappearance of Au at the tip indicated by red arrow (ii) Growth of Au liquid mediating layer in length, marked by double-headed arrow. (iii) Shrinkage of Ni particle in contact with Si NW, which are marked by black dashed box. (iv) No size change for the Ni particle not in contact with Si NW, which are marked by blue dashed box.

In the later stage, the part of Au at the tip migrates back to the gold mediating layer (Figure 3.6a-d), as indicated by the growth of Au mediating layer and gradual disappearance

of Au at the tip end. Also, the Ni particle highlighted by dashed black box in (Figure 3.6a-d) gradually shrinks over the time period of observation, which implied that it is one of the Ni suppliers to the silicide growth. In contrast, Ni particle on the silicon nitride membrane highlighted by blue dashed box does not show a size evolution over time, and this rules out the possibility that the Ni sources needed for $NiSi_2$ formation are supplied by surface diffusion on the nitride membrane.

It is surprised to observe that the $NiSi_2$ crystallite nucleates homogeneously from the liquid. In general, it is well known that homogeneous nucleation requires very high supersaturation to overcome the nucleation barrier [12]. In reality, however, phase transformation is usually initiated by heterogeneous nucleation at a supersaturation much lower than that required for homogeneous nucleation. In heterogeneous nucleation, the new phase nucleates at certain boundary in this system if this can lower overall nucleation barrier. In VLS growth of Si NW, it has been experimentally demonstrated that Si crystal nucleates at the surface of the Au-Si eutectic liquid [13]. In contrast, in our gold catalyzed $NiSi_2$ growth, an octahedral shape of nucleus (bounded by {111} facets) emerges in the middle of the Au ternary alloy. Octahedral shape is believed to be Wulff shape of $NiSi_2$ crystal and similar octahedral precipitated has been observed in the reaction between amorphous silicon and implanted Ni [14, 15].

There are two possible heterogeneous nucleation interfaces (1) the Au ternary alloy and Si interface. (2) the Au alloy and its thin encapsulating SiO_2 interface (as-grown Si NW gold tip are usually encapsulated by a thin oxide layer (Figure 3.11), which may be due to

Au-catalyzed low temperature SiO_2 formation [16, 17]). As previously found, Ni is the dominant diffusion species in $NiSi_2$.[18] Therefore, heterogeneous nucleation of $NiSi_2$ at interface (1) is not likely, because $NiSi_2$ layer forming in this way will compromise and eventually rule out accessibility of Si NW to Au and consequently cut off the Si atom supply for the silicidation reaction. Besides, it does not happen in the way that $NiSi_2$ first heterogeneously nucleates at the boundary but is later detached and suspends in the Au alloy later, because those boundaries that enables heterogeneous nucleation implies this interface provide a low interface energy so that the chemical bonding strength is expected to be high. Absence of silicide nucleation and interface (2) implied that the $NiSi_2/SiO_2$ interface has high energy and therefore such interface is not favorable heterogeneous nucleation site. This observation is consistent with previous observation [19] showing stepwise growth of nickel silicide within Si NW proceeds through repeating 2D homogeneous nucleation, where the high energy oxide/silicide interface also hinders a heterogeneous nucleation.

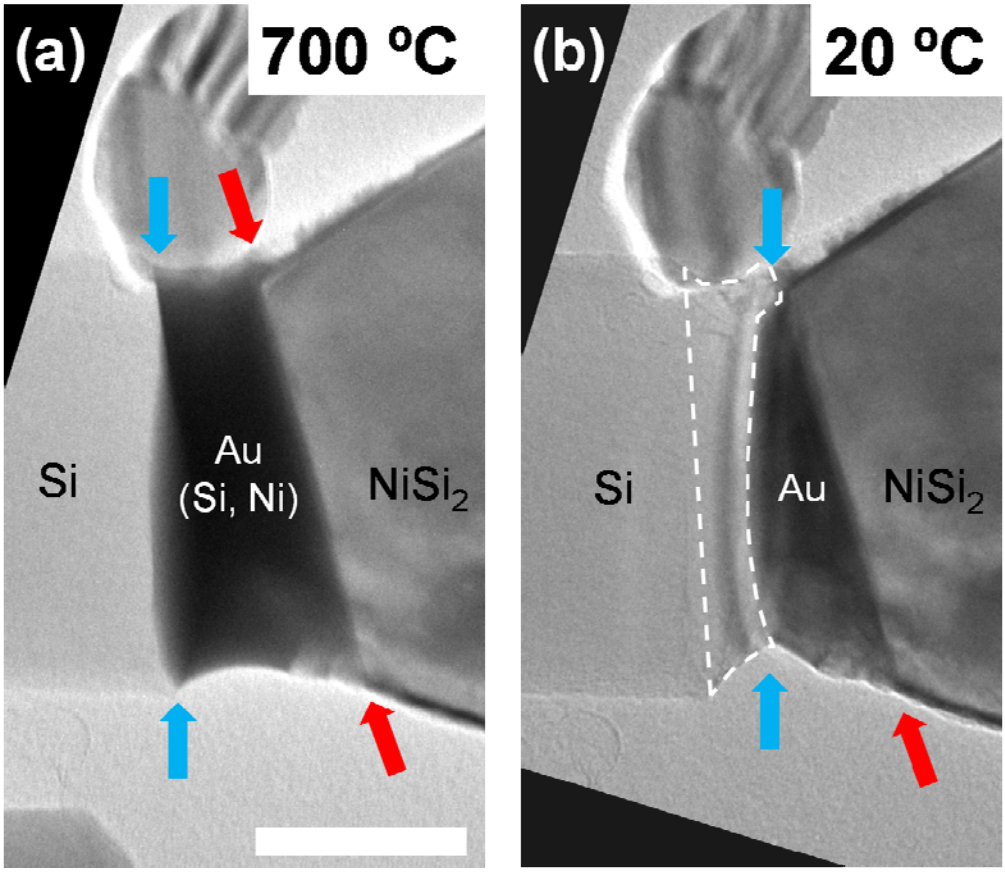


Figure 3.7. Au mediating layer before (a) and after (b) quenching from 700 ºC. The Au/$NiSi_2$ interface indicated by red arrow does not move, while the Si/Au interface marked by blue arrow contracts with Si (highlighted by white dash) precipitated out from Au. Scale bar is 50 nm.

We are interested in quantitatively how much Si and Ni are dissolved in Au, which are kept constant when growth of $NiSi_2$ reaches a steady state. As previously mentioned, there is no ternary phase diagram information available for Au-Ni-Si system. However, we can extract this information by quenching the mediating ternary Au-Ni-Si liquid alloy from 700 ºC to room temperature and measure the amount of Si and $NiSi_2$ precipitated out at both end of the Au alloy. We choose a quench rate (~1 °C/s) slow enough to ensure all Si and Ni are

rejected from Au, but still relative fast to avoid additional growth of $NiSi_2$ which may complicate the measurement of materials rejected from Au. Figure 3.7a-b show a comparison of the volume of Au mediating layer before and after quenching from 700 ºC. There is no observable $NiSi_2$ precipitated out from the Au mediating layer, which implies that the Ni supersaturation required for $NiSi_2$ growth is low (<1%). This is also consistent with previous discussion that Ni is the limiting source in $NiSi_2$ growth. By calculating the amount of Si precipitated out and the volume of remaining Au at room temperature, the Si/Au atomic ratio at 700 ºC in the Au-Ni-Si ternary alloy was determined as 0.53:1. According to the Si-Au binary phase diagram, the solubility limit of Si in equilibrium Au-Si liquid in contact with Si translates to a Si/Au ratio of 2.2:1 in such saturated liquid alloy (liquidus line to the Si side at 700 ºC). This observation implied that in the Au-Ni-Si ternary system, presence of small amount of Ni can reduce the solubility of Si in Au by roughly a factor of 4, because preferable precipitation of $NiSi_2$ rather than elemental Si. This result demonstrates that in-situ TEM heating technique can be very useful in extracting phase diagram information in a complex system not attainable by conventional methods.

3.3.3 Dynamical movement of Au/Si and Au/$NiSi_2$ interfaces

There are two interfaces moving at the same time during the $NiSi_2$ growth process, however, in different manners. Movement of Au/Si interface shows an interesting contact angle oscillation at the triple phase boundary when Au is progressively dissolving Si (111) planes. In contrast, growth of $NiSi_2$ at the $NiSi_2$/Au interface occurs in a stepwise manner. We will first discuss the moving of former interface and then briefly discuss the latter.

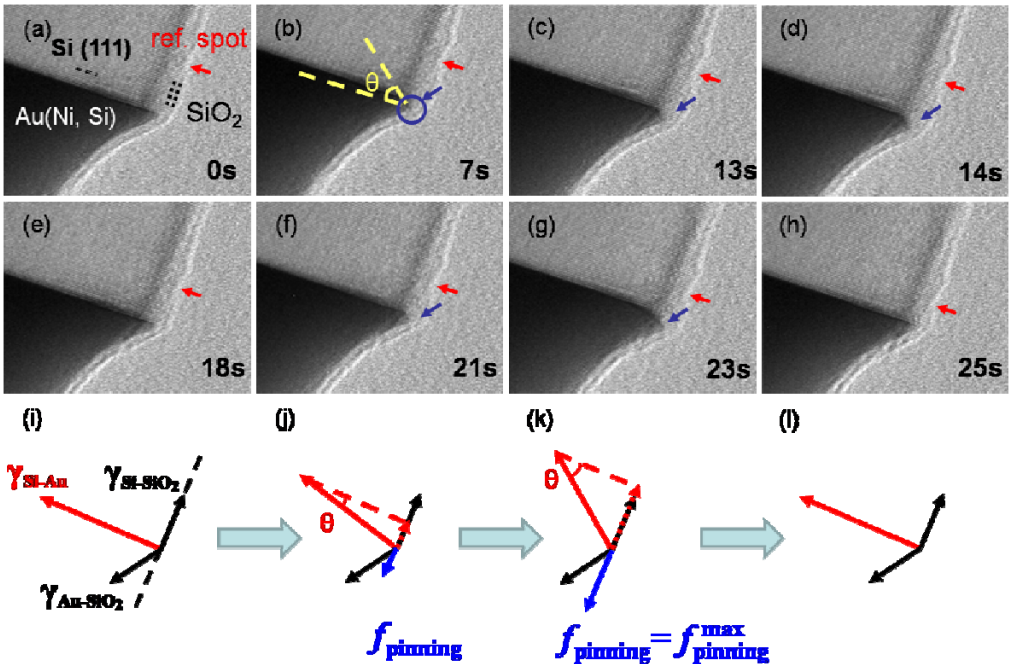


Figure 3.8. (a-h) *In-situ* TEM snapshots showing two cycles of contact angle oscillation at the triple junction point. Red arrow indicates a reference spot on the NW surface. Blue arrow indicates curvature develops at the triple junction point. (i-l) Force analysis of the mechanism of contact angle oscillation at the triple junction point, corresponding to the sub-panel images (e-h)

Figure 3.8a-h shows a series of TEM snapshots of Au/Si interface movement. We define the periphery where Si/Au/SiO_2 (native) meets as the triple junction point (TJP, shown in Figure 3.8a). When Si concentration in Au liquid alloy is below its saturation point, Au is able to dissolve Si from the NW. The interface, however, does not remain planar while it is moving. Au tends to dissolve Si in the center part of the NW first, while the movement of TJP is retarded. As a result, curvature at TJP develops and continues to increase as Au further dissolves Si in the center. We use the contact angle θ illustrated in Figure 3.8b as a measure of curvature. The TJP does not move forward until θ reaches a certain threshold value (Figure 3.8d), and the Au/Si interface becomes flat again after TJP movement (Figure 3.8e). The process described above constitutes one cycle of contact angle oscillation and 7 layer of Si (111) planes are dissolved. After that another cycle follows (Figure 3.8f-h). The contact angle oscillation behavior can be understood by analyzing the force at the TJP. Figure 3.8i-l corresponds to the sub-panel images from Figure 3.8e-h. Figure 3.8i shows surface/interface tension forces at the TJP when the Au/Si interface is flat. The force component along the dashed line direction should be balanced. When the contact angle θ increases, there is additional force component of the Au/Si tension that drops along the dashes line direction. A pinning force appears to balance this extra force component. The pinning force behaves like a macroscopic static friction force, and it may origin from microscopic heterogeneity at Si/SiO_2 interface. When θ increases, the force component along the dashed line direction increases, and the pinning force increases correspondingly until it reaches the maximum pinning force that can be exerted by the native oxide shell. After that, TJP movement can no longer be

constrained and the interface becomes flat again. This contact angle oscillation can also be understood from the view of interfacial energetics. As the TJP moves, the Si/SiO_2(native) interface is replaced by Au/SiO_2 interface. The Si/SiO_2 interface is well-known a stable interface and has a low interfacial energy, while the Au/SiO_2 interface has a higher interfacial energy. Replacement of a low energy interface by a high energy interface is energetically unfavorable, so the movement of the TJP is lagged. Similar TJP lagging phenomena has been observed in other system such as reaction between Co and Si NW, where the resulted $CoSi_2$ growth at the TJP is lagged behind the growth front in the NW center. [19]

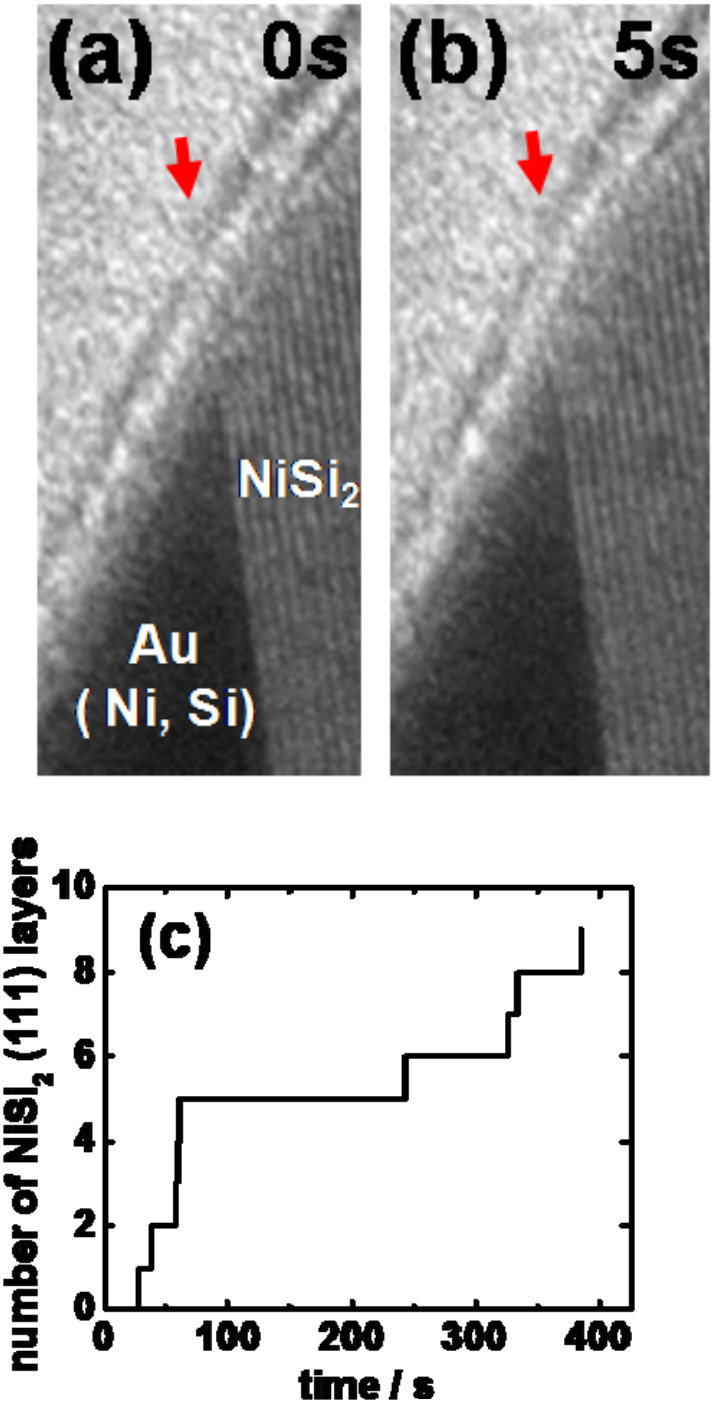


Figure 3.9. (a-b) Growth of a single $NiSi_2$ (111) layer. (c) Plane-wise growth of $NiSi_2$ (111) layer over time

In contrast of the contact angle oscillation behavior at Si dissolution front, the growth front of $NiSi_2$ proceeds in a layer-by-layer manner. Figure 3.9a-b shows growth of one (111) atomic plane of $NiSi_2$, and Figure 3.9c shows growth of NiSi2 (111) atomic plane over a longer period of time. The fast growth of three planes at about 60s may be an echo of previous result that Au can dissolve several layers of Si at a time.

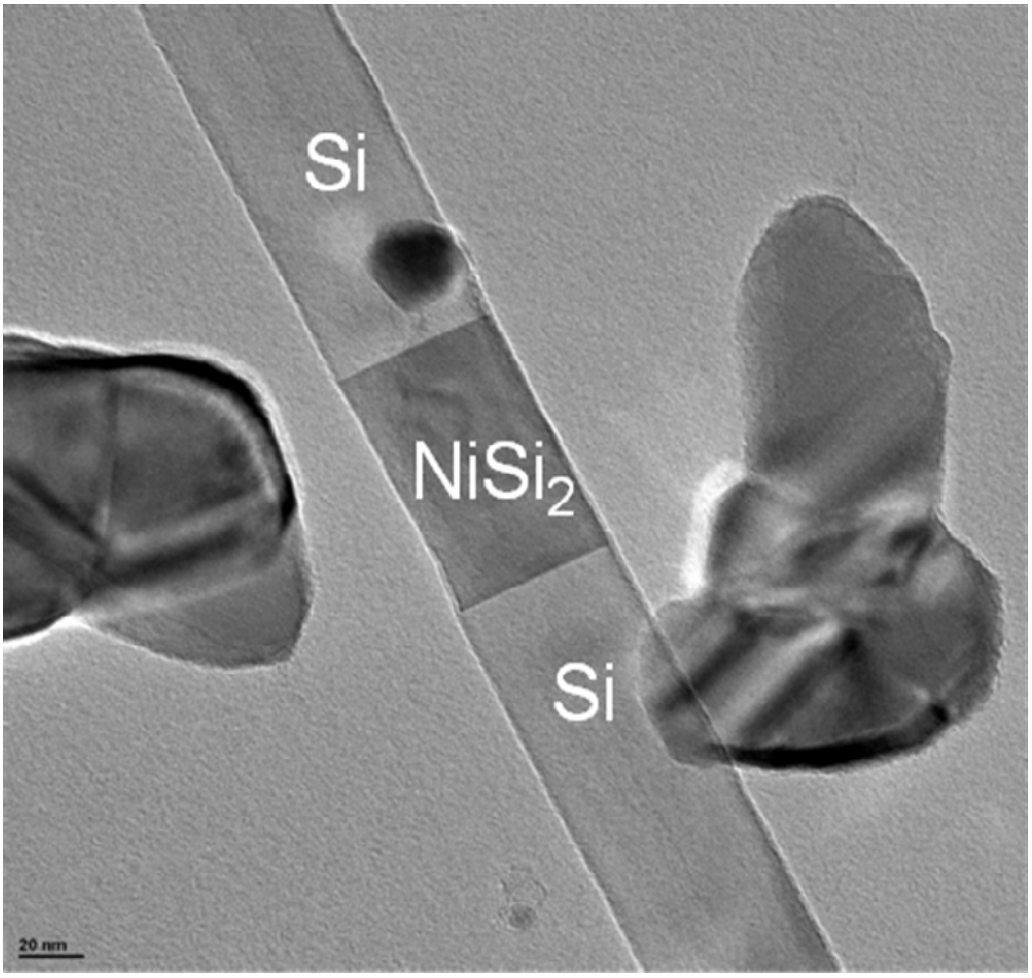


Figure 3.10. $NiSi_2$ homogeneously nucleates in Si NW at 800 ºC.

3.3.4 Reduction of $NiSi_2$ formation temperature by Au

Lastly, we are interested to see how effective Au can reduce the formation temperature of

$NiSi_2$ through a liquid mediating growth in our sample. To this end, higher temperature annealing was performed and it has been found that $NiSi_2$ homogeneously nucleates in Si NW on our sample when the annealing temperature is above 800 ºC (Figure 3.10), which implies that Au can catalyze the formation of $NiSi_2$ at a lower temperature (700 ºC). Although $NiSi_2$ can form in Si NW at a much lower temperature than 700 ºC such as in the reaction between Ni pad and Si NW [20, 21], we would like to emphasize that the formation temperature depends sensitively on the details of sample preparation process and initial Ni/Si interfacial condition. The catalytical effect of gold has been demonstrated and justified on our samples under the same sample preparation process. The high formation temperature observed in our sample is likely due to presence of native oxide at Ni/Si interface and the fact that the contact between Ni NPs and Si are point contacts, both of which limit Ni supplies for $NiSi_2$ formation.

3.4 Conclusion

In summary, we reported a detailed *in-situ* TEM study of gold catalyzed nickel disilicide formation process, for which we proposed a new solid-liquid-solid phase transformation mechanism. $NiSi_2$ was found homogeneously nucleates in the middle of the liquid Au(Ni,Si) ternary alloys. The steady state Ni and Si concentration in the Au ternary alloy was quantitatively measured by a quenching experiment. Movement of Au mediating layer was tracked by *in-situ* HRTEM videos. Si dissolution front moves with contact angle oscillation at the triple junction point, which was explained from the perspectives of both interface energetics and force balance. Precipitation of $NiSi_2$ proceeds in a layer-by-layer manner. With

Au catalyst, the formation temperature of $NiSi_2$ is reduced by 100 ºC.

3.5 Supporting information

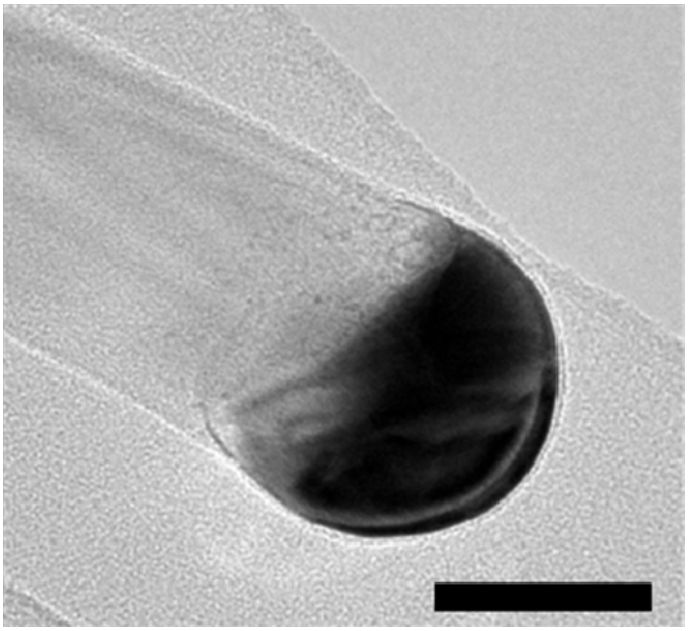


Figure 3.11 Si NW with oxide capsulated Au tip

3.6 References

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Chapter 4 : Defect induced heterogeneous nucleation of nickel silicide in Si nanowires

4.1 Introduction

In NW FET devices, nickel and other metal silicides have been actively explored as electrical contact materials, as demonstrated in chapter 2 of this dissertation and other investigations in the literature [1-4]. The nature of silicide (or their counterpart germanide in Ge devices) reaction allows formation of metallic S/D extension segment and therefore fully coverage of the NW channel by gate metal, which eliminates the serial resistance of the channel underlap region, maximizing the gate control of the S/D Schottky barriers and therefore improve the on-state drive current. [3] Ni-Si has been a model system to study the fundamental materials science of solid-state-reaction (e.g. competing growth of multiple phases [5]) due to the typicality and technological importance of nickel silicides. Recent rising interest in their application in NW device also stimulate studies on the reaction between Si NW and various Ni source, including Ni pad [6-8], Ni NW [9], and Ni nano-dots [10].

As reviewed in section 1.2.2, it has been found that nickel silicide grows by 2D repeating homogeneous nucleation in Si NW and featured a plane-wise growth when Ni sources are continuously supplied.[11] Generally speaking, homogeneous nucleation needs to overcome high nucleation barrier and therefore rarely happens in reality. Instead, heterogeneous nucleation can occur at a much lower temperature or supersaturation level if the nucleus finds

a low energy interface to attach to and therefore reduce the overall nucleation barrier. However, in the case of nickel silicide growth in single crystalline silicon NWs, formation of heterogeneous nucleus at the interface between Si and native oxide is energetically unfavorable, because in that case the original low energy Si/oxide interface is replaced by a high energy silicide/oxide interface. Therefore, concentration of Ni atoms in the NWs continues to soar until it reaches the level sufficient to initiate 2D homogeneous nucleation.

Previous studies on nickel silicide formation and growth in Si NW provides valuable insights into this reaction process. However, they mainly focus on studying single crystal or defect-free Si NWs, and little attention has been paid to the role of defects in such nano-scale phase formation process. In fact, defect may be present in Si NWs, when kinking [12], direct sidewall gas precursor (SiH_4) decomposition[13] or other instabilities during growth occur. In this work, we explored the effect of various types of defects on the nucleation and growth of nickel silicides in Si NWs. When nickel silicides are used as contact to Si NW FETs, usually silicide source/drain extensions are formed and the channel length of the device is further defined by the silicide reaction fronts [1, 2, 14, 15]. Therefore, understanding the effect of defects in Si NW in such source/drain extension formation is important to improve process reproducibility and control structure in such devices. Twin boundaries (TBs) and grain boundaries (GBs) are intentionally built into the Si NW using growth recipes featured fast growth rate. It is noted that Si (111) TB is a bi-layer interface. In-situ high resolution transmission electron microscope (HRTEM) was used to observe the silicidation reaction dynamically in real time. We provide in this chapter direct evidences showing TBs and

surface GBs are both preferred heterogeneous nucleation site. A unified model based on classic nucleation theory is proposed to demonstrate the effectiveness of nucleation barrier reduction by the defects discussed. A stochastic model was proposed to extract TB energy in $NiSi_2$ from the silicide growth curve, which provide otherwise not obvious information. In addition, our experimental observation has important implications to MOSFET S/D contact silicide formation technologies when defects are either unintentionally formed during the process or intentionally introduced to engineering the strain along the channel. Such effect will be discussed at the end of the chapter.

4.2 Experimental

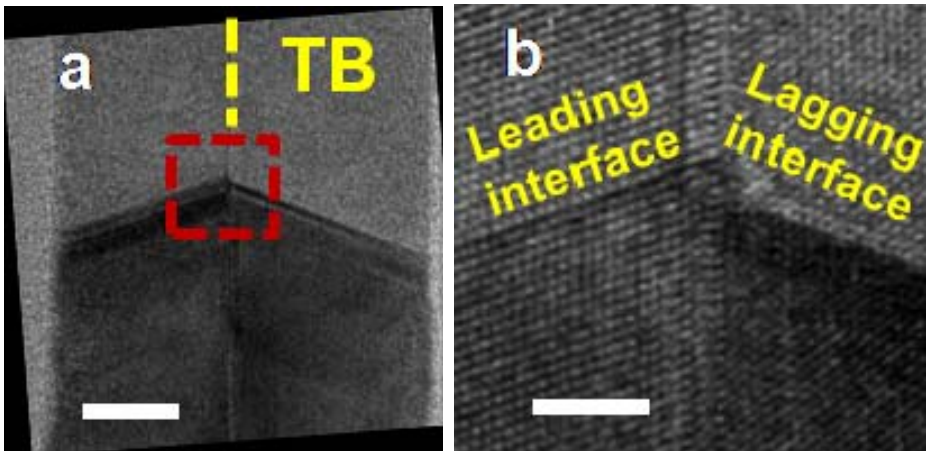
Silicon NWs are grown by Vapor-Liquid-Solid mechanism. The growth rate was intentionally tuned to induce kinetical instability and introduce twin defects in the NW. To further introduce GBs on the surface of the NW, growth temperature was carefully chosen so that it is high enough to facilitate silane sidewall decomposition but still lower than the temperature at which a single crystalline shell can form.

Our platform of in-situ TEM heating experiment was fabricated on 50 nm thick electron-beam transparent silicon nitride TEM membranes. Si NWs were ultrasonicated from the substrate and randomly dispersed on the silicon nitride membrane by a solution process. Chess board pattern with alternative contact pads openings are defined by photolithography. Native oxides on the Si NW at the contact areas are completely removed by dipping in diluted buffered oxide etch (BOE) solution (6 parts 40% NH_4F and 1 part. 49% HF) for 20s. Deposition of Ni film of 100nm then followed.

We use in-situ TEM heating stage (Gatan single tilt heating stage 628) to anneal the sample in a TEM (FEI Tecnai 300keV) chamber at a vacuum level of 10^{-7} Torr. The temperature is controlled by an external current source, and it allows isothermal thermal treatment of the sample after the initial temperature transient (about 2mins). HRTEM images are continuously updated by CCD scan, and frames were captured and compiled into videos to reveal the dynamic process of the silicide growth.

4.3 Results and Discussion

4.3.1 $NiSi_2$ growth in Si NWs with TB running in the center



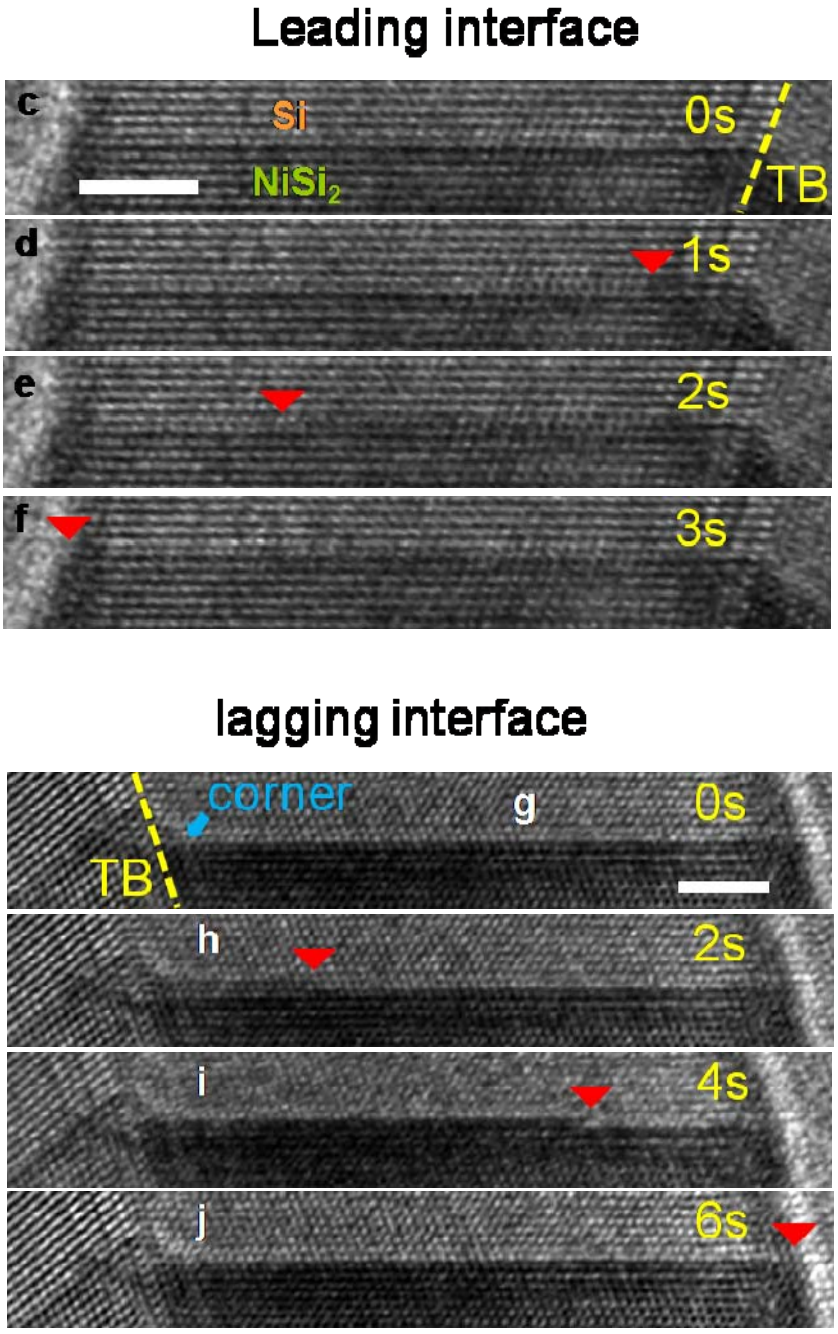


Figure 4.1 (a) Si NW with a TB running down its center. Scale bar is 10 nm (b) Zoom-in image of the dash box in (a) showing asynchronical growth of leading interface and lagging interface. Scale bar is 3 nm (c-f) Nucleation and propagation of a (111) $NiSi_2$ plane at the leading interface from the TB.

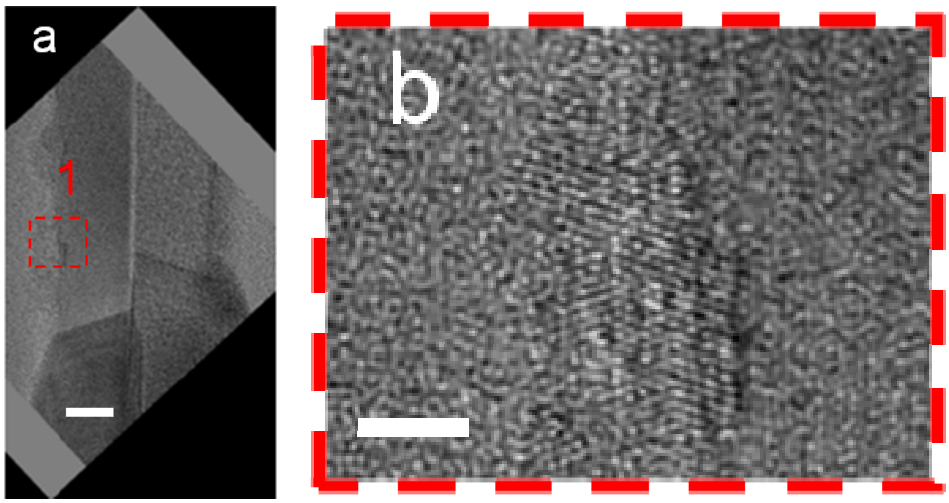
Scale bar is 3 nm (g-j) Nucleation and propagation of a (111) $NiSi_2$ plane at the lagging interface from the “corner”. Scale bar is 3 nm.

We will first look at the Si NW with a twin defect running along the axial direction of the NW, which is shown in Figure 4.1a. The NW is essentially a bi-crystal consisting of two portions of Si. The silicide growth front moves asynchronically in each of the bi-crystal, which we will elaborate shortly. We refer the fast growing interface as the leading interface and that grows slower as the lagging interface (Figure 4.1b). Figure 4.1c-f show a series of in-situ TEM snapshots that record a $NiSi_2$ (111) plane nucleates and propagates on Si (111) plane at the leading interface. It is notable that from both of the TEM snapshots and video clip that the $NiSi_2$ phase grows in a plane-wise manner. New $NiSi_2$ (111) plane nucleates at the TB and propagate to the edge of the NW. Also, it is interesting to note that the new step cannot directly propagate across the TB, and nucleus does not form across the TB either. The reason will be discussed later. As a consequence, the growth front of two halves of the bi-crystal move asynchronically, and there is a chance to develop steps with heights of a few $NiSi_2$ (111) planes.

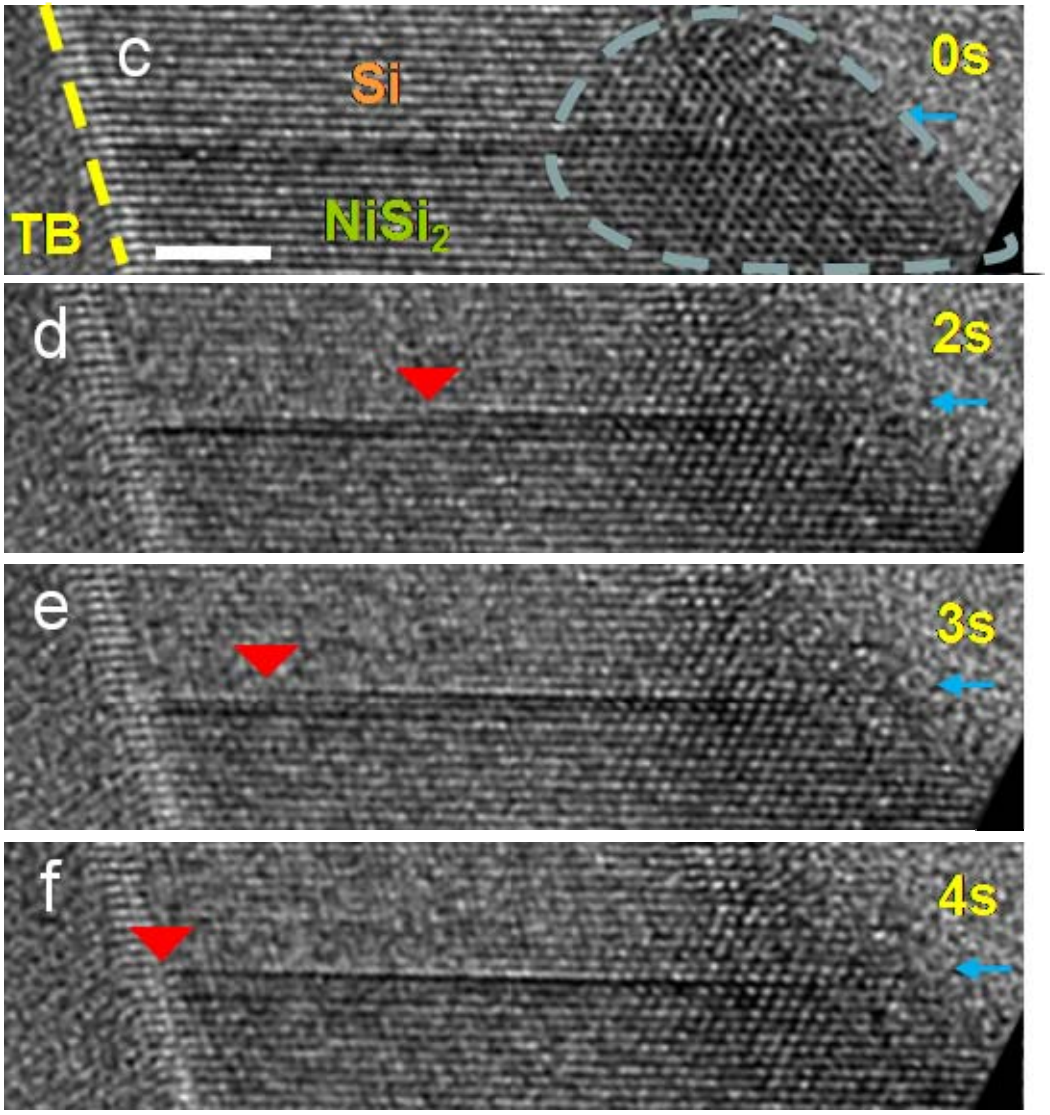
The key that initiates heterogeneous nucleation is that either the new phase ($NiSi_2$ in our case) can form a lower energy interface at certain boundaries or directly annihilate high energy boundaries in the system, compared with a homogeneous nucleation that initiates in the center of the matrix. In the case of 2D plane-wise nucleation, the interface becomes the edge that surrounds the nucleus with the height of one atomic layer. When $NiSi_2$ (111) plane nucleates at the TB, the interface facing the TB is essentially a type-B $NiSi_2$/Si interface, which is a low energy coherent epitaxial interface. Additional interfacial energy reduction is provided by annihilation of the twin defects.

For the lagging interface, growth of $NiSi_2$ (111) plane also proceeds in a stepwise manner. The location marked with "corner" at the original TB in Figure 4.1g is a preferable nucleation site. New plane nucleates at the "corner" and then propagates to the edge (Figure 4.1g-j). The nucleation at the lagging interface is much easier because it annihilates part of the high energy $NiSi_2$/Si interface. A detailed theoretical model of heterogeneous nucleation at the leading and lagging interfaces will be described later in this paper.

4.3.2 $NiSi_2$ growth in Si NWs with both TBs and surface GBs.



Leading interface



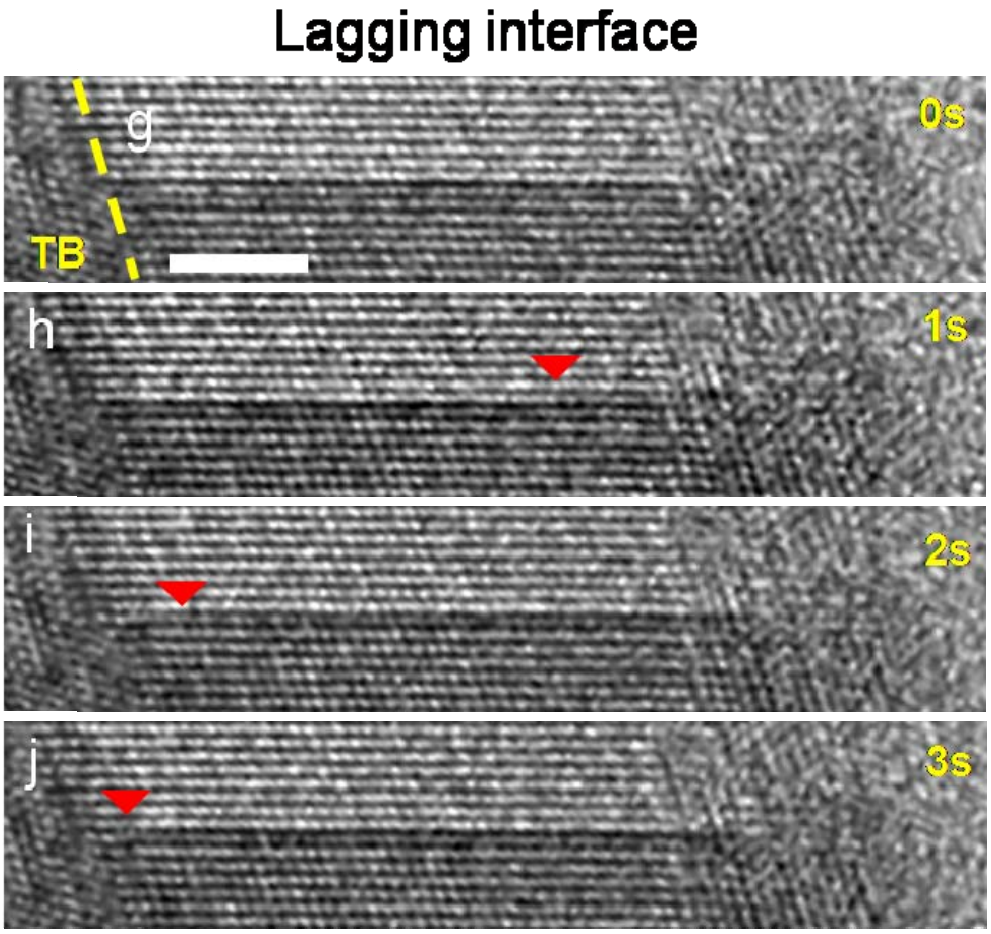


Figure 4.2. (a) Si NW with TB running down the center and surface GBs. Scale bar is 10 nm. (b) Zoom-in of several surface grains that have different orientation with respect to the NW stem. Scale bar is 3 nm (c-f) Nucleation and propagation of a (111) $NiSi_2$ plane at the leading interface from the surface GB. Scale bar is 3 nm. (g-j) Nucleation and propagation of a (111) $NiSi_2$ plane at the lagging interface from the surface GB. Scale bar is 3 nm.

If surface grains are intentionally introduced, heterogeneous nucleation is further facilitated and the corresponding nucleation sites change accordingly. Figure 4.2a show a twinned Si NW with surface grains, and Figure 4.2b highlights several surface grains with

different orientations with respect of the stem of the NW. In-situ TEM snapshots (Figure 4.2c-f) showing the lateral growth of a single silicide layer at the leading interface. A surface grain partially overlaps with the NW along the viewing direction (marked by light blue dashed enclosure), but it is readily distinguishable to have a different orientation with respect to the NW because the zone axis of this surface grain is better aligned to the viewing direction than the NW itself (the surface grain shows a clearer 2D lattice than the NW). Following Figure 4.2c-f, it is interesting to note that a single $NiSi_2$ layer first nucleates at the surface GB and propagate towards the center of the NW, which is along the opposite direction of the case when we do not have surface GBs (such as the process shown in Figure 4.1c-f). The TB in the center of the NW is still a heterogeneous nucleation site, but the probability of a new $NiSi_2$ layer to nucleate at a surface GB is much higher, as will be quantitatively demonstrated later.

The key for preferable nucleation at GBs is that they have much higher energies than TBs, because nearest neighbors chemical bonds are disturbed at GBs but not at TBs. At the lagging interface, it is surprised to see that the new plane does not always nucleate at the "corner". Figure 4.2g-j show an example that the new plane can still nucleate from surface GB and then propagate towards the center of the NW. The underlying assumption that the step should nucleate at the "corner" is that the new $NiSi_2$ nucleus will form a silicide twin with the existing $NiSi_2$ in the other half of the bi-crystal. $NiSi_2$ has a face-center-cubic (FCC) structure and, generally speaking, the energy of coherent TB in FCC materials (e.g. Cu, Si etc.) is much lower than GB energy or hetero-interface energy, because formation of a

coherent twin only involves alternation of the stacking sequence and the nearest neighbor coordination of interfacial atoms is not disturbed. However, a close look at the structure of twinned $NiSi_2$ crystal reveals that the nearest neighbor configurations of interfacial atoms are disturbed. Figure 4.9a (supporting information) shows the atom arrangement of a perfect $NiSi_2$ $(\bar{1}10)$ plane, and Figure 4.9b (supporting information) shows a possible configuration of a coherent (111) TB in $NiSi_2$. Si atoms (grey) highlighted by purple dash box are in close proximity to each other so that creation of new chemical bond or rearrangement of interfacial atom configuration should occur. In either case, nearest neighbor configurations of atoms at the interface are no longer the same as those in the bulk, so the TB energy in $NiSi_2$ is not negligible. This explains why $NiSi_2$ (111) planes do not nucleate or propagate across the TB. Therefore, the surface GB, depending on its energy, on the Si NW can be a more preferable heterogeneous nucleation site than the "corner".

4.3.3 $NiSi_2$ growth and step development between leading and lagging interfaces

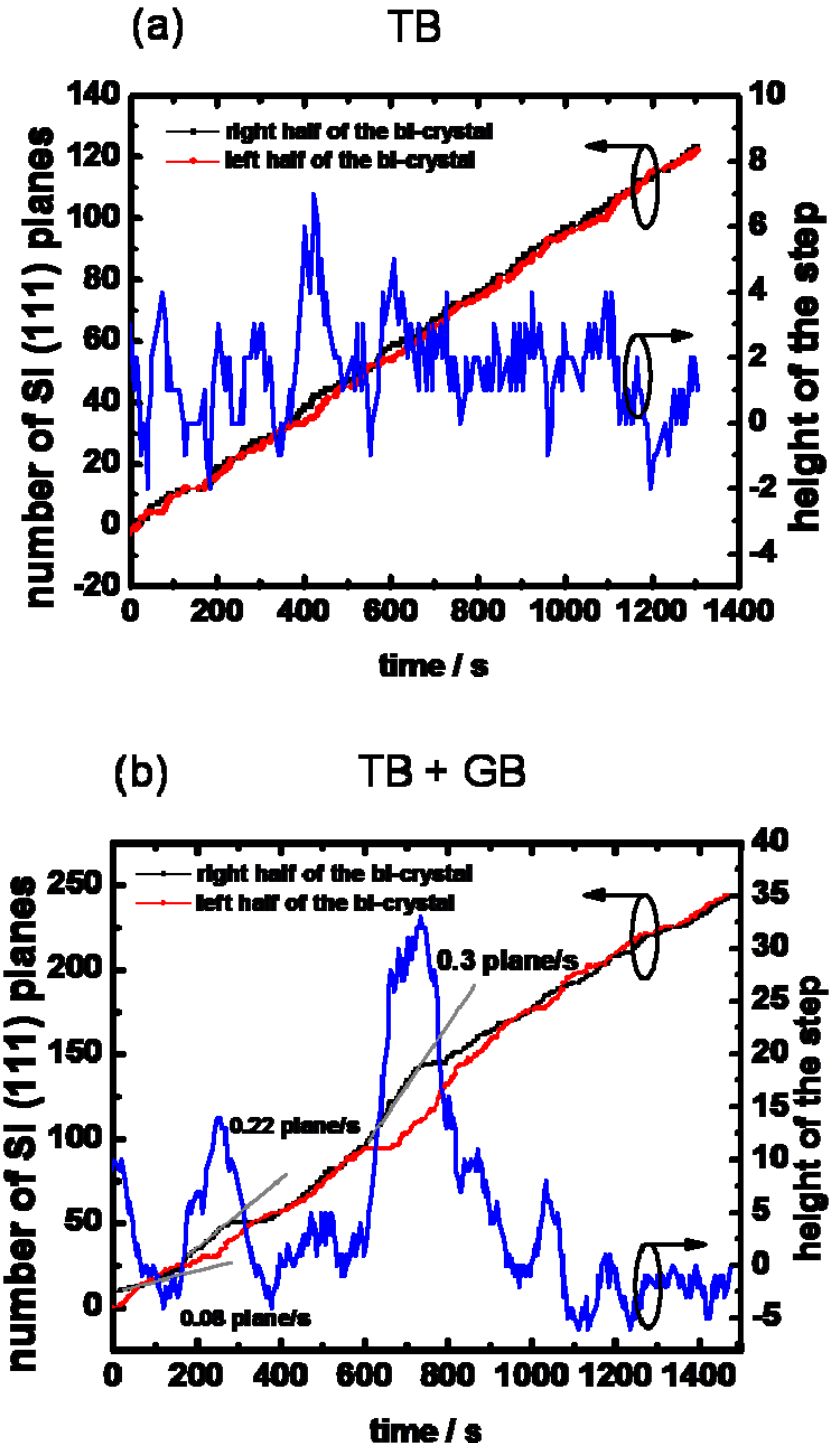


Figure 4.3. Growth of $NiSi_2$ (111) plane and step height between leading/lagging interfaces in Si NW with (a) TB and (b) both TB and GB

Plane-wise growth of $NiSi_2$ was tracked over an extended period of time when its (111) plane nucleation is assisted by TB alone (Figure 4.3a) and TB/GB combined (Figure 4.3b), and the growth behaves differently in these two cases. In Figure 4.3a, the growth (in both halves of Si bi-crystal) is almost linear over the period we tracked, which features a steady growth rate. This is because the Si (111) TB boundary energy is well-define and nucleation as well as growth rate, is roughly a constant within a time period observed. Over this time period, growth of silicide is about 39 nm, which is negligible compared with the already grown 547 nm nickel silicide segment on the same NW. Therefore, the signature of parabolic growth [8, 16] in a diffusion limited silicidation reaction does not show here, because the diffusion length from Ni pad to the reaction front changes only 7% over this period. The blue curves in Figure 4.3 measure the height difference (referred to step height hereafter) between the interface in each half of the bi-crystal. In Figure 4.3a, steps of several (111) plane height have chances to develop during the growth because new plane nucleation is a random effect. However, lagging interface can catch up with the front interface because the "corner" is a more preferable hetero-nucleation site, so the height of the step does not significantly grow.

On the other hand, when surface GBs are further introduced to the NW (Figure 4.3b), growth rate fluctuates and can change by a factor of 3.8 (from 0.08 plane/s to 0.3 plane/s) over a similar time period. The irregular growth behavior origins from the fact the nucleation barrier of $NiSi_2$ (111) plane depends on the energy of surface GBs, which is a function of relative orientation of the surface grain with respect to the NW as well as the details of the atoms arrangement at the GB. Those surface GB are incorporated by sidewall decomposition

of silane, so grains on the NW surface are randomly distributed. On the segment of the NW with high energy surface GBs, heterogeneous nucleation is more favored and $NiSi_2$ grows faster. It is noted that in the time period between 600 s and 630 s in Figure 4.3b, the leading interface (black curve, right portion in the bi-crystal) grows rapidly, while the growth of the lagging interface (red curve, left portion in the bi-crystal) ceases, and therefore a huge step (with a maximum height of 33 $NiSi_2$ (111) atomic layers) develops between these two interfaces. Rapid growth of the leading interface implies high GB energy at the surface, which promptly assists nucleation of $NiSi_2$, and therefore acts as Ni sinks and keeps Ni concentration lower than that requires to nucleate a $NiSi_2$ plane at the lagging interface. In this extreme case, $NiSi_2$ growth is completely dominated by nucleation at extrinsic surface GBs and shadow other intrinsic nucleation sites like the "corner" so that the lagging interface does not grow for an extended period of time. This result suggests that the defects can play a prominent role in the nickel silicide formation process. To use silicide as S/D extensions in Si NW FETs, controlled growth of nickel silicide into Si NW is required and NW-to-NW variation is undesirable, so twin and surface defects need to be avoided.

4.3.4 Models of the nucleation barrier at different nucleation sites

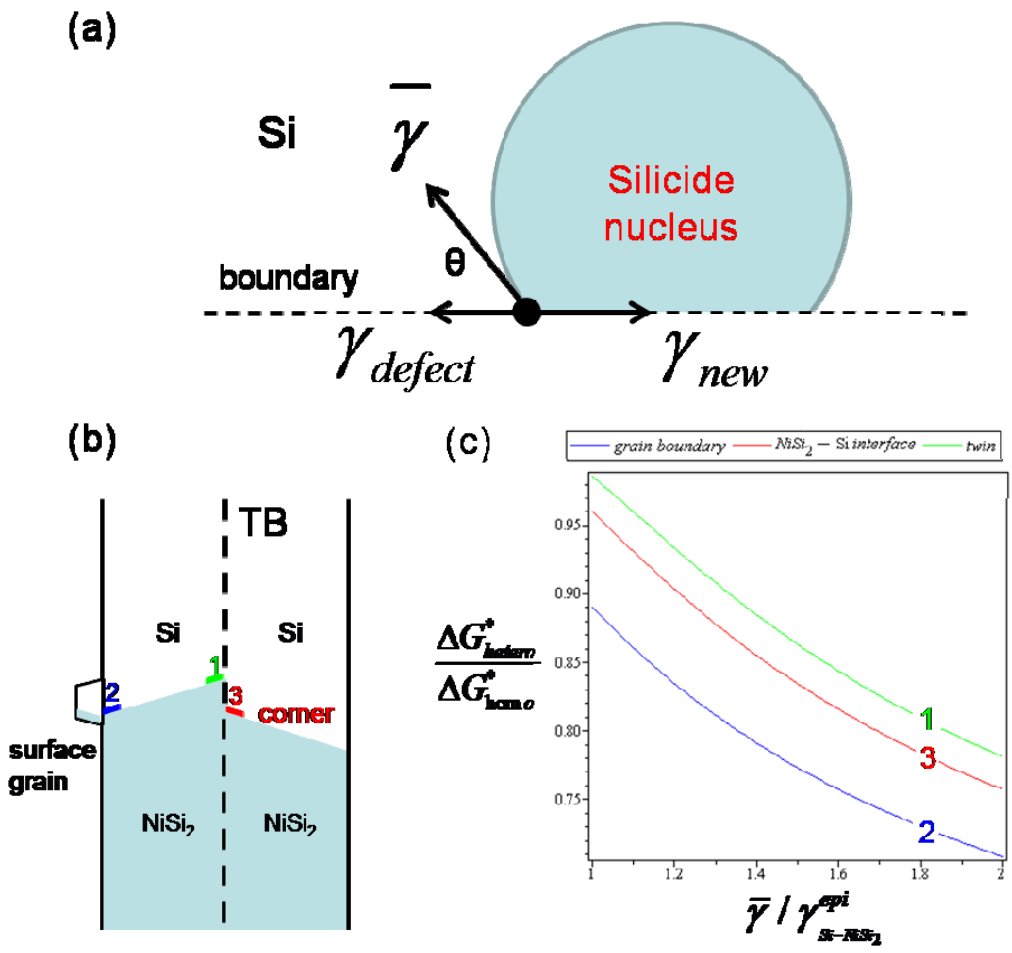


Figure 4.4. (a) Top view of a $NiSi_2$ 2D partial disk heterogeneously nucleate at certain boundary. (b) Schematics of three different heterogeneous nucleation sites (c) Reduction of nucleation barrier at different heterogeneous sites.

We developed a model to quantitatively depict the suppressing of 2D nucleation barrier at a heterogeneous site (including defects) based on classic nucleation theory. The nucleus is illustrated in Figure 4.4a. Assuming the 2D silicide partial disk nucleates at certain boundary

in the system, the change of free energy of the system is given by:

$$\Delta G_{hetero} = -\Delta g\left[\pi R^2(1-\theta/\pi) + R^2\sin(\theta)\cos(\theta)\right]h + \left(2\pi - 2\theta\right)Rh\bar{\gamma} + 2Rh\sin(\theta)\cdot\left(\gamma_{new} - \gamma_{defect}\right) \quad (4.1)$$

Where R is the radius of the disk, h is the height of the 2D partial disk, θ is the contact angle, $\bar{\gamma}$ is the average interface energy between $NiSi_2$ and Si over different orientations, γ_{defect} is the original defect energy in Si crystal, γ_{new} is the new $NiSi_2$ and Si interface energy at the original defect boundary. Both γ_{defect} and γ_{new} assumes different values for different defects, and their meaning will become clearer when we are discussing specific type of defects. The contact angle θ is given by the Young's equation, which assumes force balance at the triple phase point:

$$\bar{\gamma}\cos(\theta) + \gamma_{defect} = \gamma_{new} \quad (4.2)$$

The critical radius is solved by letting $\left.\frac{\partial \Delta G}{\partial R}\right|_{R=R^*} = 0$, and the nucleation barrier ΔG^* is given by:

$$\Delta G^*_{hetero} = \frac{\left[(\pi-\theta) + \sin(\theta)\cos(\theta)\right]\bar{\gamma}^2 h}{\Delta g} \quad (4.3)$$

Combine Eq. (4.2) and Eq. (4.3), the nucleation barrier can be evaluated. For a special case, when θ=0, Eq (4.3) gives the homogeneous nucleation barrier $\Delta G^*_{\text{homo}} = \frac{\bar{\gamma}^2 \pi h}{\Delta g}$. We are interested in how much defects can reduce the nucleation barrier, so we calculate the ratio:

$$\frac{\Delta G^*_{hetero}}{\Delta G^*_{\text{hom}o}} = \frac{\left[\left(\pi-\theta\right) + \sin(\theta)\cdot\cos(\theta)\right]}{\pi} \quad (4.4)$$

Note that θ is given by Eq.(4.2), and the above ratio only relies on $\gamma_{defect}/\bar{\gamma}$ and $\gamma_{new}/\bar{\gamma}$.

We will quantitatively consider nucleation of a 2D $NiSi_2$ partial disk at two previously mentioned types of defects (1) Si TB (2) Si GB, and a non-defect site (3) the "corner", and discuss the corresponding interface energy parameter separately. Three cases are schematically illustrated in Figure 4.4b. In case (1), γ_{defect} becomes Si TB energy and γ_{new} becomes the energy of type-B $NiSi_2$/Si interface, in which $NiSi_2$ is rotated by 180° about the interface normal. Si TB energy γ_{Si}^{twin} ranges from 38 mJ/m^2 to 71 mJ/m^2 in various theoretical investigations [17-19] and we take 50 mJ/m^2 as a reasonable estimation. The type-B $NiSi_2$/Si interface is roughly 0.6 J/m^2, and difference between type-A ($NiSi_2$ has the same orientation with Si) and type-B interface is as small as 12 mJ/m^2. [20] The average $NiSi_2$/Si interface energy $\overline{\gamma}$ (over different orientations) is not exactly known since the γ-plot of this interface is not available. The interfacial energy of high-index interface (curved part of the nucleus) can be much higher than low-index interface (e.g. epitaxial interface), so $\overline{\gamma} > \gamma_{Si/NiSi_2}^{epi}$. We plot in Figure 4.4c ("twin" line) $\Delta G_{hetero}^{*} / \Delta G_{\mathrm{homo}}^{*}$ versus a range of $\overline{\gamma} / \gamma_{Si/NiSi_2}^{epi}$ ratio to account for this uncertainty and the trend will be discussed with case (2) and (3) shortly. In case (2), when a 2D $NiSi_2$ partial disk nucleates at a Si GB, γ_{defect} becomes Si GB energy γ_{Si}^{GB}, and γ_{new} becomes incoherent $NiSi_2$/Si interface energy $\gamma_{Si-NiSi_2}^{inc}$, where the interface planes have different atomic configuration in the two adjacent phases. Si GB energy highly relies on the relative orientation between two neighboring grains. As a reasonable estimation [21], we choose the GB energy $\gamma_{Si}^{GB} = \frac{1}{3}\gamma_{Si(111)}$, where $\gamma_{Si(111)} = 1.23 J/m^2$ is the free energy of Si (111) surface. The incoherent $NiSi_2$/Si interface energy is expected to be higher than an epitaxial interface, so for simplicity, we

choose $\gamma^{inc}_{Si-NiSi_2} = 0.8\ J/m^2$. In case (3), when a 2D $NiSi_2$ partial disk nucleate at the "corner", γ_{defect} is essentially type-B $NiSi_2$/Si epitaxial interface energy $\gamma^{epi}_{Si-NiSi_2}$, and γ_{new} is the silicide twin energy $\gamma^{twin}_{NiSi_2}$. The interfacial energy parameter $\gamma^{twin}_{NiSi_2}$ is not available from the literature, we developed a stochastic model to derive its value as $\gamma^{twin}_{NiSi_2} = 1.14 J/m^2$, which will be described in details in section 4.3.5. Figure 4.4c shows effectiveness of nucleation barrier reduction $\Delta G^*_{hetero} / \Delta G^*_{\text{homo}}$ by nucleation at various types of defects. Table 4.1 summarizes the boundary energy parameters used in the nucleation model for all three cases. The ratio $\bar{\gamma} / \gamma^{epi}_{Si/NiSi_2}$ accounts for the uncertainty of $\bar{\gamma}$, i.e. the average Si/$NiSi_2$ interfacial energy on a curved interface. As a conservative estimation we choose $\bar{\gamma} = 1.2\gamma^{epi}_{Si/NiSi_2}$, and $\Delta G^*_{hetero} / \Delta G^*_{\text{homo}}$ values are 0.93, 0.90 and 0.83 respectively. Note that the nucleation rate is proportional to the factor $\exp\left(-\frac{\Delta G^*}{kT}\right)$, so a slight change in nucleation barrier can change the nucleation rate dramatically.

nucleation boundary type	γ_{defect}	γ_{new}
TB	$\gamma_{Si}^{twin}(0.05\ J/m^2)$	$\gamma_{Si-NiSi_2}^{epi}(0.6\ J/m^2)$
GB	$\gamma_{Si}^{GB}(0.4\ J/m^2)$	$\gamma_{Si-NiSi_2}^{inc}(0.8\ J/m^2)$
$NiSi_2$/Si twinned interface	$\gamma_{Si-NiSi_2}^{epi}(0.6\ J/m^2)$	$\gamma_{NiSi_2}^{twin}(1.14\ J/m^2)$

Table 4.1 Summary of interfacial energetic parameters used in the nucleation model for all three cases

There are two contributions to nucleation barrier reduction in a heterogeneous nucleation. (i) formation of a low energy Si/$NiSi_2$ interface at the defect plane (ii) annihilation of the defect itself. For heterogeneous nucleation at the TB, $NiSi_2$ nucleus can form epitaxial interface with Si, which has much lower energy than the curve interface of this two phases. The contribution (i) becomes more important when $\bar{\gamma}$ is higher (greater reduction at high $\bar{\gamma} / \gamma_{Si/NiSi_2}^{epi}$ end in Figure 4.4c). For nucleation at Si GB, although the $NiSi_2$/Si interface at the boundary is incoherent, reduction in energy are provided by annihilation of the Si GB. The contribution (ii) plays an important role here and the nucleation barrier is even lower than the nucleation at Si TB. A general criteria for heterogeneous nucleation is that $\gamma_{new} - \gamma_{defect} < \bar{\gamma}$, which combines both of the two contributions.

Although our studies focus on the Ni silicidation reaction in a NW system, they have general implications to the contact formation kinetics and device reliability in modern very

large scale integration (VLSI) technologies. In a CMOS fabrication process, the S/D region of MOSFETs needs to be heavily doped to achieve low contact resistance. This is achieved by dopant implantation and subsequent S/D activation annealing to recrystallize the damaged S/D area, and defects can form during annealing step. Tadashi *et al* [22] found that Si (111) stacking faults form at the trench edge after S/D activation annealing, and $NiSi_2$ whisker forms and elongate from those trench edge and pierce into the channel (Figure 4.5).

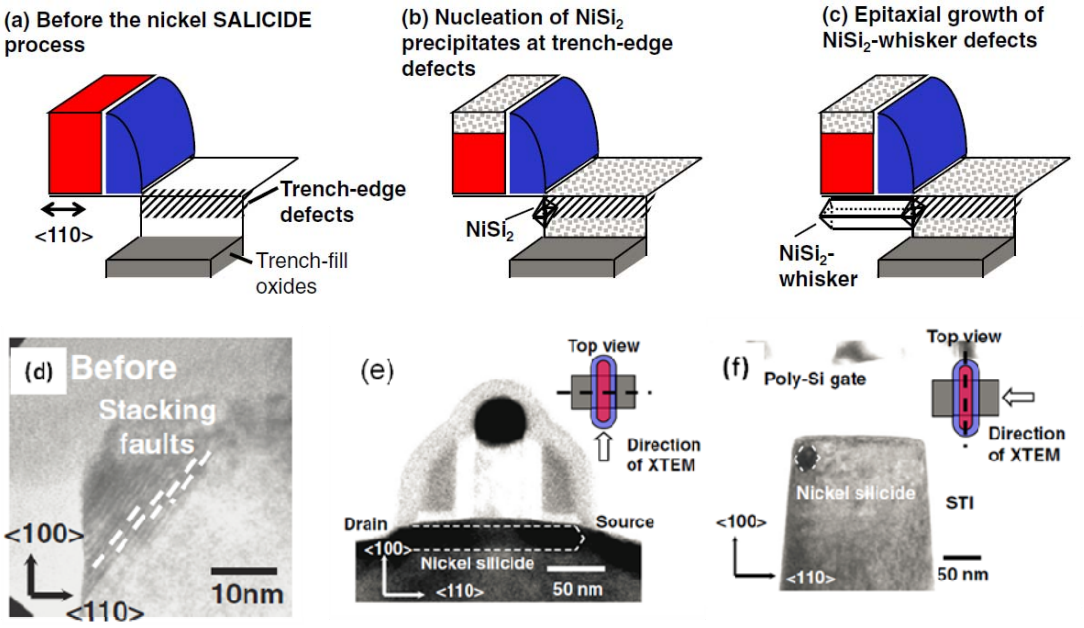


Figure 4.5 From Ref. [22]. (a) Trench edge defects formed after S/D dopant activation process when they are bounded by trench oxide fill. (b) $NiSi_2$ nucleation at those trench-edge defects (c) Growth of $NiSi_2$ whisker into the channel and failure of the device. (d) TEM images showing stacking faults as the trench-edge defects. (e-f) Cross-section TEM image along different direction showing $NiSi_2$ whisker grown into Si channel

The origin of observation is very similar to that of our result and can be explained by

enhanced heterogeneous nucleation of $NiSi_2$ phase at the stacking fault defects. In addition to the above mentioned unintentionally formed defects, defects are also intentionally introduced in the S/D region (Figure 4.6) to engineer strain in the channel to enhance carrier motilities. [23, 24]

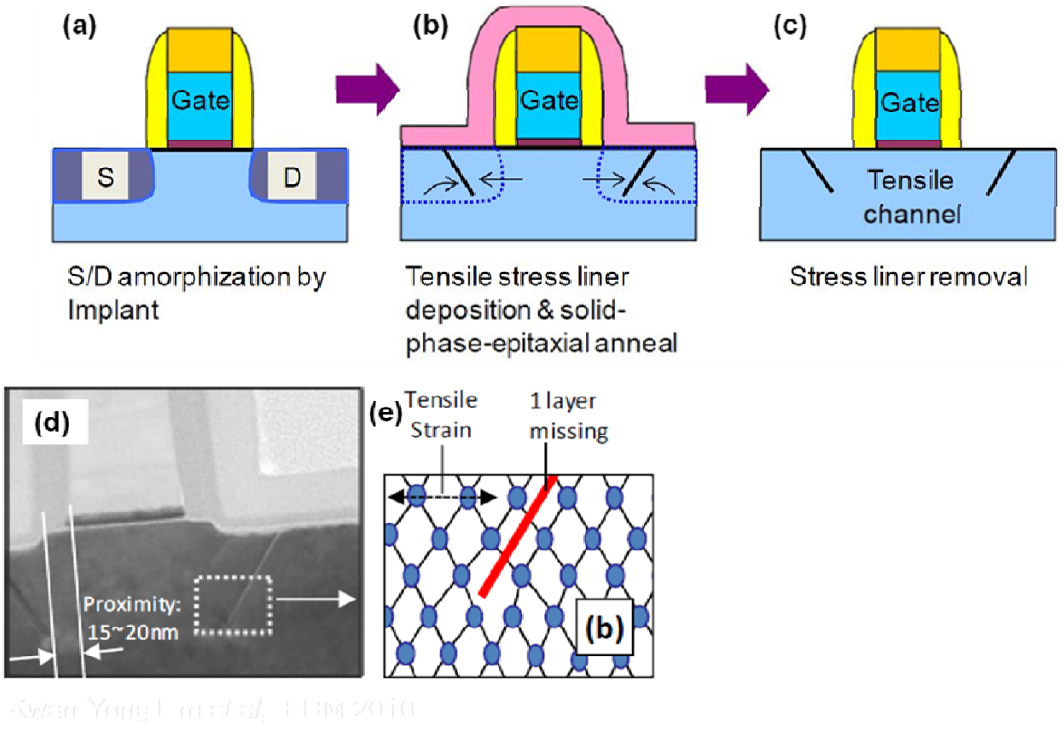


Figure 4.6 From Ref [24] (a-c) Stress memorization technology (d) TEM picture of stacking fault formed in S/D area. (e) Schematics of the mechanism of tensile strain in the channel induced by the stacking fault.

Presence of defects in S/D region may change the contact silicidation process and undesired silicide encroachment into the channel may occur when silicide formation is guided by those defects. Our in-situ TEM studies provide useful insights of how nickel silicide formation interacts with defects in Si, and it further impacts the contact formation technology in VLSI

device when intentional or unintentional defects are introduced.

4.3.5 Stochastic model of the silicide growth process in a twinned Si NW

In this section, we describe a stochastic model that utilizes the growth curve Figure 4.3 to extract the interfacial energy $\gamma_{NiSi_2}^{twin}$, which is otherwise not obvious but interesting because of coherency of the interface structure. When the silicide is growing into a twinned Si NW, growth of left and right half of the bi-crystal are statistically random events. We define the step height between the two interfaces in left and right crystals as H (Figure 4.7a). The evolution of the step height can be modeled as 1D biased random walk in the H space (Figure 4.7b). For example, when H is 1, if the left interface grows, H jumps to 2 with a probability denoted as ν_{lead}; similarly, if the right interface grows, H jumps back to 0 with a probability ν_{lag}. This type of random walk is biased, because the transition rates between two neighboring states are not equal, i.e. $\nu_{lead} \neq \nu_{lag}$, which will be later linked to the nucleation rate at their respective interfaces.

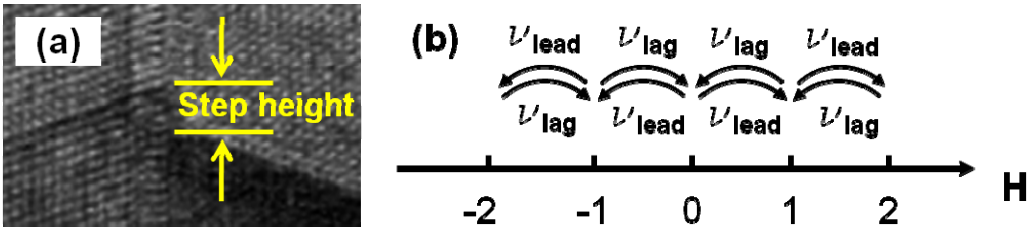


Figure 4.7 Biased random walk in H space

We further define f(H) as the probability function in the H space. When this random process reaches the equilibrium state, f(H) does not change over time, and the detailed balance

condition can be applied under this situation. If two states x and y are considered, the detailed balance condition can be expressed as:

$$f(x)\upsilon_{xy} = f(y)\upsilon_{yx} \tag{4.5}$$

By applying the above equation to all of the neighboring state, we obtain:

$$\begin{aligned} &f(0)\cdot\upsilon_{lead} = f(1)\cdot\upsilon_{lag} \\ &f(1)\cdot\upsilon_{lead} = f(2)\cdot\upsilon_{lag} \\ &\vdots \end{aligned} \tag{4.6}$$

To rewrite the above equation:

$$\begin{aligned} &f(1) = f(0)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right) \\ &f(2) = f(1)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right) = f(0)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right)^2 \\ &\vdots \end{aligned} \tag{4.7}$$

Similarly, for negative H, we have:

$$\begin{aligned} &f(-1) = f(0)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right) \\ &f(-2) = f(-1)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right) = f(0)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right)^2 \\ &\vdots \end{aligned} \tag{4.8}$$

To summarize:

$$f(\pm n) = f(0)\cdot\left(\upsilon_{lead}/\upsilon_{lag}\right)^n = f(0)\cdot q^n \tag{4.9}$$

where $q = (\upsilon_{lead}/\upsilon_{lag}) < 1$.

Using the above obtained probability function f(H), mean square step height can be evaluated:

$$\overline{H^2} = \frac{\sum_{n=-\infty}^{+\infty} n^2 f(n)}{\sum_{n=-\infty}^{+\infty} f(n)} = \frac{2\sum_{n=1}^{+\infty} n^2 q^n}{2\sum_{n=0}^{+\infty} q^n - 1} = \frac{q}{(1-q)^2} \tag{4.10}$$

Experimental mean square step height can be evaluated using the step height evolution curve (blue) in Figure 4.3 as 5.22. By solving Eq.(4.10), we obtained $q = 0.65$.

The growth rate of $NiSi_2$ is determined by two serial processes: Diffusion of Ni to the $NiSi_2$/Si reaction front, and nucleation of single $NiSi_2$ layer at the reaction front. However, Ni supply rates to both interfaces are the same, so the growth rates of both interfaces are only different in their nucleation rates. Therefore, q can be further simplified as the ratio of the nucleation at the leading and lagging interfaces. Quantitatively, it is given by:

$$q = \frac{\upsilon_0 \exp\left(-\frac{\Delta G^*_{lead}}{k_B T}\right)}{\upsilon_0 \exp\left(-\frac{\Delta G^*_{lag}}{k_B T}\right)} = \exp\left(-\frac{\Delta G^*_{lead} - \Delta G^*_{lag}}{k_B T}\right) \tag{4.11}$$

where ΔG^*_{lead} and ΔG^*_{lag} are the nucleation barrier at the leading and lagging interface respectively. Recall the formula of heterogeneous nucleation barrier in Eq.(4.4) and the schematic diagram in Figure 4.4b. Nucleus at leading and lagging interfaces are denoted as site "1" and site "3", respectively. The differences in their interfacial energy parameters (edges in the 2D case), when using Eq.(4.4) are summarized below:

Growing interface	γ_{defect}	γ_{new}
leading	$\gamma^{twin}_{Si}(0.05\ J/m^2)$	$\gamma^{epi}_{Si-NiSi_2}(0.6\ J/m^2)$
lagging	$\gamma^{epi}_{Si-NiSi_2}(0.6\ J/m^2)$	$\gamma^{twin}_{NiSi_2}$ (*unknown*)

Table 4.2 Interfacial energy parameters for leading and lagging interface growth in a twinned Si NW.

By solving Eq. (4.11) with $q = 0.65$, we obtained $\gamma^{twin}_{NiSi_2} = 1.14 J/m^2$. More strictly speaking, $\bar{\gamma}$ is another unknown. However, within its reasonable range (0.6-1.2 J/m^2), $\gamma^{twin}_{NiSi_2}$ does not vary appreciably (Figure 4.8).

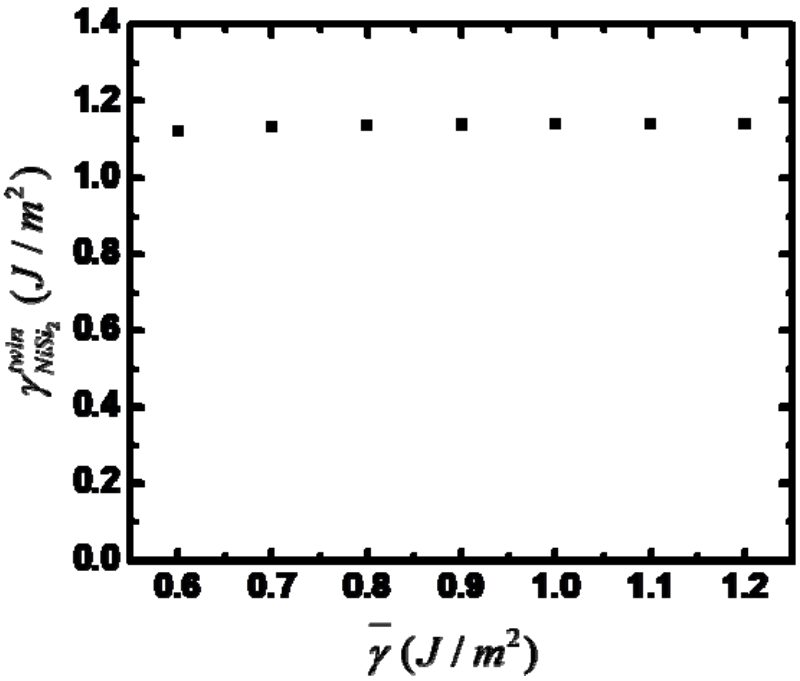


Figure 4.8 Dependence of $\gamma_{NiSi_2}^{twin}$ on $\bar{\gamma}$

If the twin boundary energy of $NiSi_2$ is close to that of Si (50mJ/m^2), using the above quantitative model, $\overline{H^2} = 10^{-32} << 1$. This result implies that under this assumption ($\gamma_{Si}^{twin} \approx \gamma_{NiSi_2}^{twin}$), step between leading and lagging interface should never form and new $NiSi_2$ plane can propagate across the twin boundary without delay. However, in experiment non-zero step heights are constantly observed, which implies that formation of a $NiSi_2$ twin is a much more energetically expensive process than formation of a Si twin and this result quantitatively echoes the discussion in the previous section.

4.4 Conclusion

In summary, we have investigated the effect of defects (including TBs and GBs) in Si

NWs on repeating nucleation of $NiSi_2$ (111) plane. *In-situ* TEM dynamical video recording technique was employed to track the initial formation of $NiSi_2$ (111) plane and its propagation direction, which provide direct evidence that both TBs and GBs can be preferred heterogeneous nucleation sites. A model based on classical nucleation theory was developed to quantify the amount of nucleation barrier reduction at these defects compared with a homogeneous nucleation case. In Si NWs with high energy surface GBs, nucleation at the GBs can dominate the growth of nickel silicide phase and giant step may develop between the leading and lagging reacting interfaces in a twinned Si NW. Therefore, surface GB need to be avoided in Si NW FET devices for better control of the S/D silicide extension formation process. Our results also provide insights into modern VLSI device contact silicide formation process when unintentional or intentional defects are incorporated.

4.5 Supporting information:

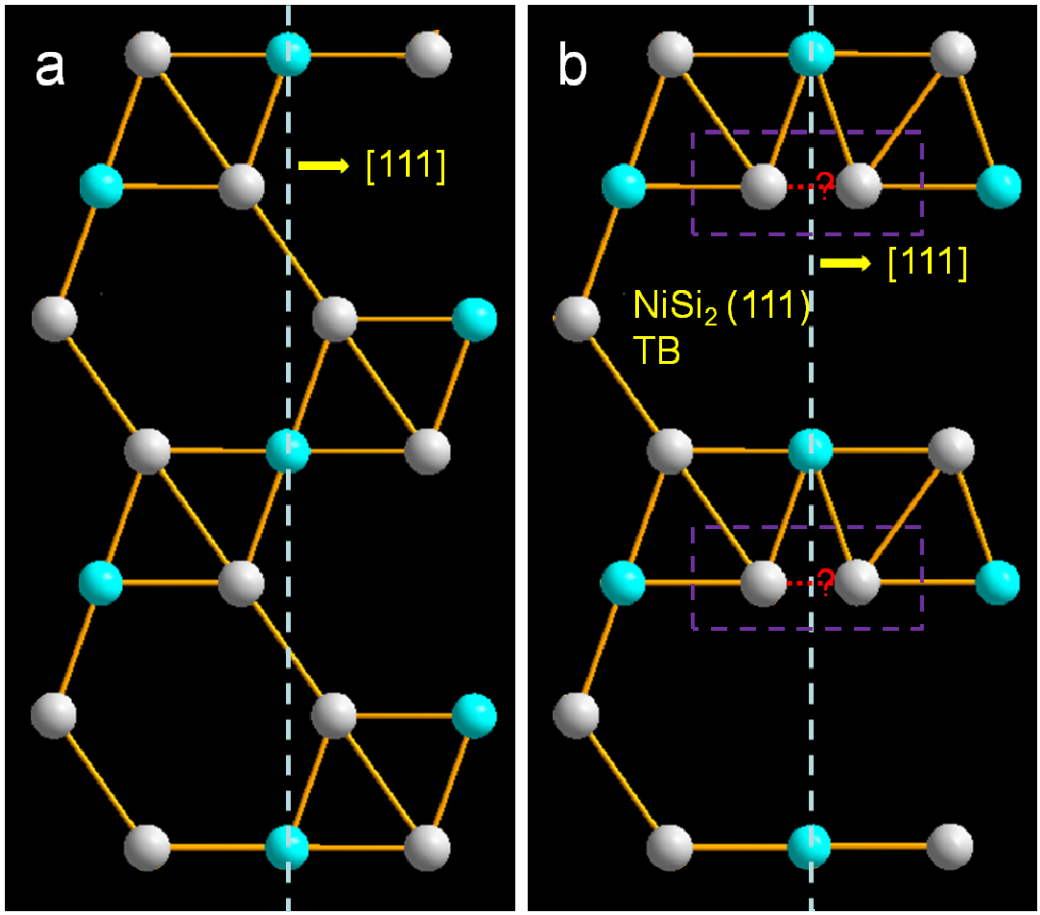


Figure 4.9. (a) $(\bar{1}10)$ plane in a perfect $NiSi_2$ crystal. Si atoms are grey and Ni atoms are green. (b) A possible structure of $NiSi_2$ $(\bar{1}10)$ plane when (111) twin is present. New chemical bonds across the TB may form between nearby Si atoms.

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Chapter 5 : Summary and future work

Since the introduction of salicide process, contact materials have transited from C54-$TiSi_2$ to $CoSi_2$ and finally to NiSi with downscaling of the width of the contact lines. There are more than billions of transistors made on a single chip and the electrical properties of the silicide contacts are highly uniform. This is due to thorough understandings of the solid state reaction between silicide-forming metals and Si, and therefore reproducible metal/semiconductor interface structure and electrical properties.

Si NW is one of the potential device geometries for an ultimately scaled MOSFET device within the physics limit, due to its possibility to form a gate-all-around structure and therefore the best gate electrostatic coupling and short channel effect control. In this thesis, we tried to explore the application of nickel silicide contacts to Si NW device with ultra-short channel length (17nm) and study Ni-Si reaction in the nanoscale. *In-situ* TEM techniques are important tools that enable fabrication of ultra-short Si gap on a Si NW, by monitoring the silicidation reaction in a highly controlled manner. Besides, the Au particles which were used to grow Si NW by VLS mechanism are later in-place catalysts for Ni-Si reaction when Si NW further reacts with Ni NPs. A new solid-liquid-solid growth mechanism was proposed to describe this phase transformation process. When defects, such as Si (111) TBs and GBs are present in the Si NW, the fundamental picture of how nickel silicide nucleate is then changed, and the silicide growth rate can be greatly affected by those defects. It suggests that special care has to be paid to the contact silicide formation process whenever defects are intentionally or unintentionally introduced in the Si crystal.

Recent studies of nickel silicide formation in Si NW have greatly advanced our understanding of this nanoscale phase transformation process. However, compared with Ni-Si bulk or thin film reaction, there are several questions about nickel silicide phase selection in this nanoscale Ni-pad/Si-NW reaction still open and deserve further investigation. For example, why $NiSi_2$ is the leading phase in the temperature range (350 ºC to 600 ºC) when formation of NiSi is expected in a thin film reaction? Why NiSi is never observed in the Ni-pad/Si-NW reaction? Why meta-stable θ-Ni_2Si phase (high temperature phase that is stable above 825 ºC) can form at a temperature as low as 400 ºC? Simultaneous multiple silicide phase growth is undesired because this introduces additional variability into the contact formation process. Is there any way to controllably form a single silicide phase and achieve highly reproducible growth rate, which is vital for a scaled up circuit on Si NW device? Different nickel and other metal silicide phases have different crystal structure and therefore can exert different type of strain into the Si channel, after contact formation, especially when the channel is very short. The S/D silicide induced strain effect on the channel mobility is another interesting subject to study in the future.