Title

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Journal

IET Microwaves, Antennas & Propagation, 10(10)

ISSN

1751-8725

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Publication Date

2016-07-01

DOI

10.1049/iet-map.2015.0818

Peer reviewed

A Fully Integrated Ka-Band Doherty Power Amplifier With 26.9 dBm Output Power, 42% Peak PAE and 32% Back-Off PAE

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Abstract: We present the design and development of a fully integrated, two stage Doherty power amplifier (DPA) in the Ka-Band. The amplifier is fabricated in a 0.15-μm Gallium Arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) process. The DPA has a center frequency of 26.6 GHz, a measured small signal gain of 10.5 dB, output power at 1-dB compression point (P1dB) of 26.9 dBm, maximum power added efficiency (PAE) of 42%, and PAE of 32% at 6 dB back-off power. To the best of the author's knowledge, this DPA is the first fully integrated millimeter-wave (mm-wave) power amplifier to achieve a record 32% PAE at 6-dB back-off power from 26.9 dBm at Ka-band.

1. Introduction

Mobile data traffic has undergone substantial growth in recent years and shows no signs of slowing down in the near future. This rapid growth has led to an increasingly crowded spectrum in the range of 300 MHz to 3 GHz, with today's cellular systems running at near theoretical capacity limit in given spectrum. The current 4G systems use advanced technologies such as Orthogonal Frequency Division Multiplex and Multiple Input Multiple Output to improve communication performance and achieve high data rates, but are reaching theoretical limits in terms of bit-per-second/Hz/cell. With limited bandwidth available in the currently used spectrum, many companies and research institutions have sought to develop mobile broadband systems beyond X-band into the mm-wave frequency spectrum [1].

An approach to building millimeter-wave mobile broadband systems is to use phased array antennas and beamforming techniques in order to reduce the peak power requirements of the power amplifier. Even with a reduction in peak power, the low efficiency of commercially available mm-wave power amplifiers is still a major challenge. Additionally, many mobile communication systems use signals with a high peak-to-average power ratio. Commercially available millimeter-wave PA's offer power added efficiencies in the range of 5% to 10% at 6-dB back-off power [2]-[3]. The low efficiency can lead to significant thermal management issues when a large number of these amplifiers are used in a beamforming system. Low efficiency PA's can also severely degrade battery life if used in a mobile device.

There have been several solutions developed to improve the efficiency of power amplifiers at back-off power, including the Chireix and Doherty architectures, as well as techniques such as envelope

tracking. A Doherty power amplifier is an attractive candidate for mm-wave implementation as it inherently supports large information bandwidth. Alternatively, envelope tracking technique requires a wideband DC-DC converter, which is difficult to implement with high efficiency. Doherty architectures have been a popular solution in the currently used mobile communication bands below 6 GHz [4]. Several Doherty PA's have been developed for millimeter-wave frequencies, but have low power and low efficiency. The mm-wave Doherty PA's reported in [5]-[8] have been built in Complementary metal oxide semiconductor (CMOS), Silicon on insulator (SOI), and GaAs for operation up to 76 GHz and achieve a maximum 6-dB back-off efficiency of 17% without linearization techniques [8] and 23% using post-distortion linearization [7].

In this paper, we present the design and development of a fully integrated Ka-Band Doherty power amplifier, fabricated in a 0.15-μm GaAs pHEMT process. An identical unit cell amplifier is used as the main and peaking amplifiers, and this unit cell amplifier was also fabricated as a standalone block to highlight the efficiency improvement of the Doherty PA. An on-chip asymmetric Wilkinson power divider is used at the input and an on-chip tee junction, a lambda/4 inverter, and an offset line are implemented at the output. The proposed Ka-band Doherty power amplifier achieves measured output referred one-dB compression point (OP_{1dB}) of 26.9 dBm and PAE of 32% at 6-dB back-off power at 26.6 GHz.

2. Circuit Design

2.1. Review of Conventional Doherty Power Amplifiers

The conventional, symmetrical Doherty power amplifier consists of two power amplifiers interconnected through a quarter-wavelength transformer as shown in Fig. 1. The amplifiers are represented by two current sources, I_1 and I_2. The main amplifier (I_1) is biased in Class AB so that it is "on" for all drive levels, whereas the peaking amplifier (I_2) is typically biased in Class C so that it is only "on" at drive levels above 6 dB back-off. The peaking amplifier serves to modulate the main amplifier load, ZM, from Ropt/2 to Ropt as the drive level is increased from 6 dB back-off to P1dB. This load modulation keeps the main amplifier in a high efficiency, compressed state over the 6 dB power range.

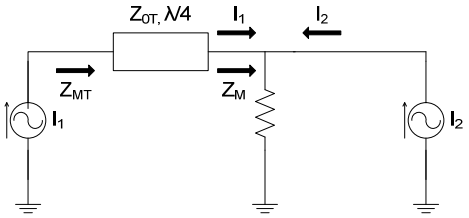

Fig. 1. *Doherty power amplifier concept diagram.*

2.2. MM-wave Doherty Power Amplifier Design

The proposed Ka-band Doherty power amplifier circuit schematic diagram is shown in Fig. 2. It is built in a 0.15-μm GaAs pHEMT process with a transition frequency (f_T) of 65 GHz and maximum oscillation frequency (f_{max}) of 100 GHz. The process offers depletion mode transistors with a pinch-off voltage of -1V and a breakdown voltage of 14V. The GaAs pHEMT process offers one thick RF interconnect layer and one thinner metal layer to make possible the layout of spiral inductors and MIM capacitors. There is an additional NiCR layer available for on-chip resistors.

All matching networks were realized through transmission line components. In our design, transmission line matching elements are used to generate capacitance on order of 100-200 fF. In order to realize these, we have employed open circuited stubs and short circuited stubs, with the latter being realized through quarter-wave transmission line chokes. A multi-band reject filter was included in the bias network to ensure that the amplifier was unconditionally stable at all frequencies. The DC gate connection also included an on-chip series resistor which played an important role in the large signal performance and will be discussed in Section 3. All passive structures were simulated using Agilent's Momentum electromagnetic simulator software [9], and the complete power amplifier non-linear simulation was done using Agilent Advanced Design System [9].

Referring to Figure 2, the main amplifier has two gain stages because the simulated maximum available gain of a single transistor is approximately 7 dB. The addition of a driver stage adds some gain and adds to the small DC power consumption, but should be designed with sufficient power margin such that it remains in its linear region of operation and has minimal impact on the load modulation action of the Doherty amplifier. The output stage device has a total gate width periphery of 600 μm and the driver stage device has a total gate width periphery of 300 μm, resulting in a gate periphery ratio of 2 to 1 between the output and driver stages, respectively. The gate periphery ratio was chosen to ensure sufficient power margin as previously mentioned. With a gate periphery double that of the driver stage, the output stage largely determines the overall efficiency of the amplifier and is biased in deep Class AB to maximize efficiency. The output stage was biased at a drain voltage of 5 V and a drain current of 10 mA, roughly 3% of the maximum current for the 600 μm device. Since the driver stage utilizes a smaller device and consumes less current at an equivalent gate voltage, it is biased at a higher Class AB condition to provide higher small signal gain with minimal penalty on the efficiency. The driver stage is biased at a drain voltage of 6 V and a drain current of 17 mA, roughly 10% of the maximum current for the 300 μm device. The drain voltages were chosen for optimal gain, power and efficiency performance between the two stages, while ensuring reliable operation with a nominal breakdown voltage of 14 V. The output

matching network was designed for an optimal power and efficiency match based on nonlinear load-pull simulation of the 600 μm device. Nonlinear load-pull simulation of the 300 μm device was also performed for the design of the interstage matching network to ensure that the driver stage could drive the output stage into compression. The interstage and input matching networks were designed for desired gain and input return loss performance using small signal S-parameter simulation.

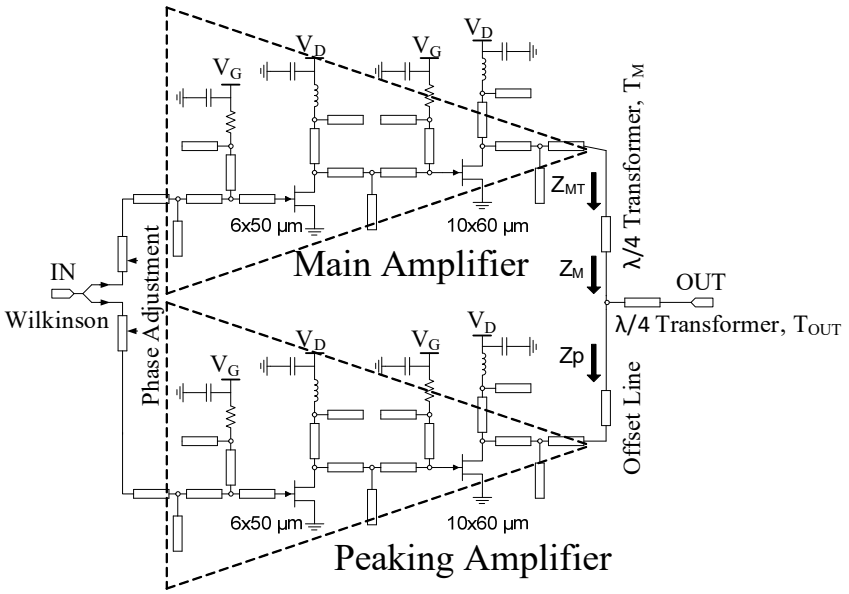

Fig. 2. *Doherty power amplifier circuit diagram.*

The peaking amplifier also consists of two gain stages with the same device sizes and is designed to operate in Class C so that it is off at low drive levels and turns on at 22 dBm output power, which is 6 dB below the maximum output power of the Doherty power amplifier. The matching networks for the peaking amplifier were similarly designed using nonlinear load-pull simulation to determine the optimal power match for the Class C device, as well as large signal S-parameter simulation to achieve the desired gain and return loss. Because the output matching networks for the deep Class AB main amplifier and Class C peaking amplifier were designed based on a load-line match and the V_{max} and I_{max} are the same between the two, we were able to use the same matching network topology.

The novelty of our Ka-Band Doherty amplifier is largely in the design of the transformer at the output of the main amplifier. Due to the additional parasitics and other nonidealities of transistors at mm-wave frequency range, the optimal back-off impedance at 22 dBm output power for the main amplifier departs from the $2*R_{opt}$ or 100 Ω used in an ideal Doherty architecture. For example, in our unit cell amplifier (used as the main amplifier), the optimal back-off impedance "Z_{MT}" for is roughly (59 – j*41) Ω in the band of interest. Our novel and simple solution to this problem is to design the transformer T_M at

the output of the main amplifier with a characteristic impedance of 50 Ω and an electrical length of 120 degrees to transform the $R_{opt}/2$ or 25 Ω load to (59 – j*41) Ω. Note that the characteristic impedance of the transformer T_{OUT} is 35 Ω so that its input impedance is 25 Ω. Since the transformer T_M has a characteristic impedance of 50 Ω, changing the electrical length from the standard 90 degrees to 120 degrees does not affect the impedance transformation at high drive levels where the main and peaking amplifiers see a R_{opt} or 50 Ω load. Figure 3 shows a comparison of the simulated PAE versus output power of the main amplifier alone for two cases: using the traditional quarter-wave transformer and the modified 120 degree transformer. A power sweep harmonic balance simulation was performed for each case to investigate the power and efficiency of the main amplifier from low drive levels to 22 dBm output power. As it can be seen in Figure 3, using the standard quarter-wave transformer results in a PAE of 30% at 22 dBm output power, whereas using the 120 degree transformer results in a PAE of 39% at 22 dBm output power. The 120 degree transformer ensures the main amplifier is driven into compression and reaches maximum efficiency at the same drive level that the peaking amplifier begins to turn on, a major improvement compared to the conventional transformer design.

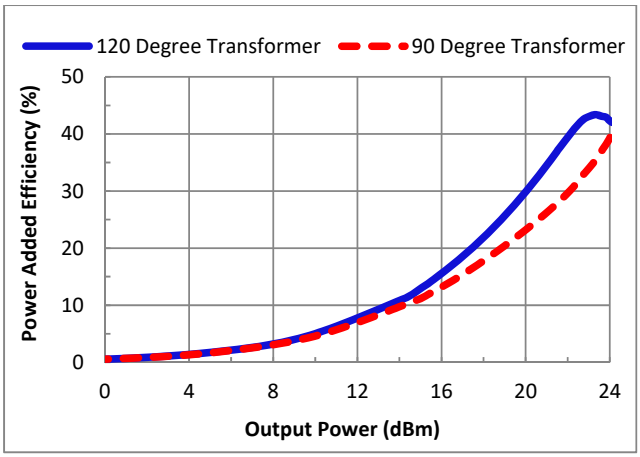

Fig. 3. *Simulated power added efficiency of the main amplifier alone at 27 GHz, Vds = 6 V, Ids = 27 mA.*

One of the challenges we addressed in implementing the Doherty architecture at mm-wave frequencies is achieving the open circuit condition required for the peaking amplifier in low power operation. The Class C peaking amplifier in our design had an output impedance "Z_P" of (16 + j*67) Ω, which leads to an output reflection coefficient magnitude of 0.8. We designed a 50 Ω "offset" line, shown in Fig. 2, with an electrical length of 35 degrees at the output of the peaking amplifier to rotate the impedance Z_P to (437 – j*19) Ω. We performed a harmonic balance simulation of the DPA where the input divider was disconnected and the main amplifier was driven directly. The Class C biased peaking amplifier output was connected at the node connecting the two quarter-wave transformers for both cases:

with and without the offset line. The simulated power added efficiency versus output power with and without the offset line is shown in Figure 4. The efficiency is slightly lower than what is shown in Figure 3 due to the power leakage into the peaking amplifier, even in the presence of the offset line. The offset line reduces the power leakage by more than 0.5 dB and helps to increase the PAE by more than 4% in the frequency band of interest.

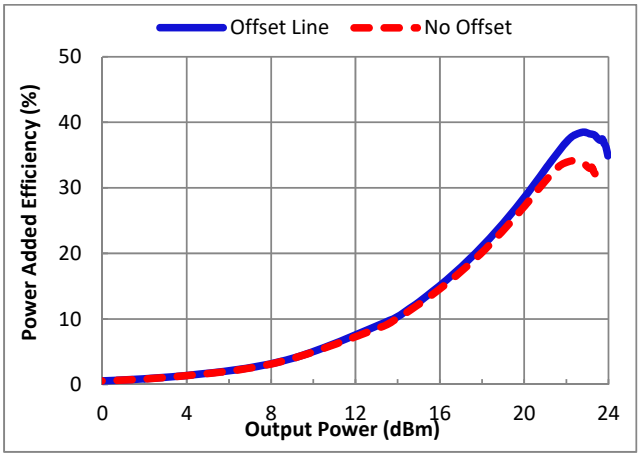

Fig. 4. *Simulated power added efficiency of the main amplifier with and without an offset line used in the peaking amplifier at 27 GHz, Vds = 6 V, Ids = 27 mA with the same bias as in Fig. 3.*

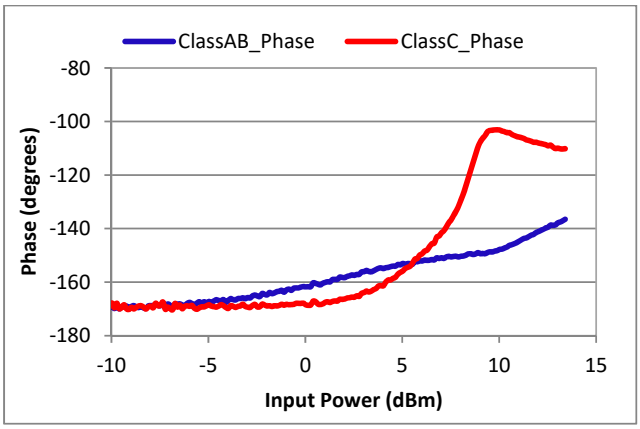

Fig. 5. *Measured phase of main amplifier alone in Class AB bias condition (Vdd = 6 V, Id1 = 17 mA, Id2 = 10 mA) and Class C bias condition (Vdd = 6 V, Vgg = -1.35 V).*

The phase adjustment lines at the input of the DPA in Figure 2 have a characteristic impedance of 50 Ω and the electrical lengths are designed to ensure the main amplifier and peaking amplifier output signals are in phase and add constructively. In the ideal architecture, the phase adjustment lines are designed to compensate for the difference between the quarter wave transformer T_M and the offset line. However, because the peaking amplifier is biased in Class C and the main amplifier is biased in Class AB, they have different AM-PM distortion characteristics as a function of drive level. Figure 5 shows the measured

phase versus input power of the main amplifier alone for a Class C bias condition and a Class AB bias condition. As seen from Fig. 5, the phase difference is around 40 degrees at a drive level of 11 dBm, which is approximately the input referred 1 dB compression point for the main amplifier. However, in the DPA, the 120 degree transformer T_M and the 35 degree off-set line will contribute additional phase differences to about 125 degrees. Therefore, the phase adjustment lines are designed to provide 125 degree phase compensation between the peaking amplifier and the main amplifier to provide optimal OP_{1dB} and PAE_{max}. The $PAE_{back\text{-}off}$ is unaffected since the peaking amplifier is nearly off at the 6 dB back-off drive level.

2.3. Asymmetric Wilkinson Splitter

As described in the previous subsection, we have designed the main and peaking amplifiers to have the same output stage gate periphery and OP_{1dB}. However, the Class C peaking amplifier only reaches 80% of the maximum drain current of the main amplifier if the input power is equally divided between the two branches. We have designed and employed an asymmetric Wilkinson splitter to deliver 1.6 dB more power to the peaking amplifier than the main amplifier. The unequal power split will ensure that the peaking amplifier is turned "on" to the same level as the main amplifier at the maximum drive level and fully modulates the load to 50 Ω. Using this approach, we can achieve the highest power and efficiency from the main amplifier and peaking amplifier. Fig. 6 shows the schematic diagram of the asymmetric Wilkinson splitter. The transmission lines are implemented with microstrip lines using the thick top metal layer and the resistor is implemented on chip with a NiCr layer. We have used well known methods as in [10] to design different sections of the transmission lines and the isolation resistor based on the desired power ratio.

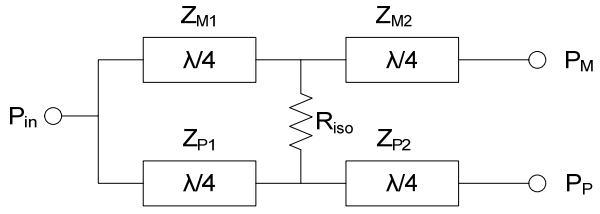

Fig. 6. *Asymmetric Wilkinson splitter circuit diagram.*

3. Experimental Results

The Doherty power amplifier was measured using on-wafer probing and on-die TRL calibration. Power and linearity measurements were taken using Agilent PNA-X N5247A Network Analyzer and Agilent PXA Signal Analyzer N9030A. The amplifier was measured under several bias conditions which

offer various tradeoffs in gain, OP1dB, PAE_{max} and $PAE_{back\text{-}off}$. A chip photograph of the Doherty power amplifier is shown in Figure 7.

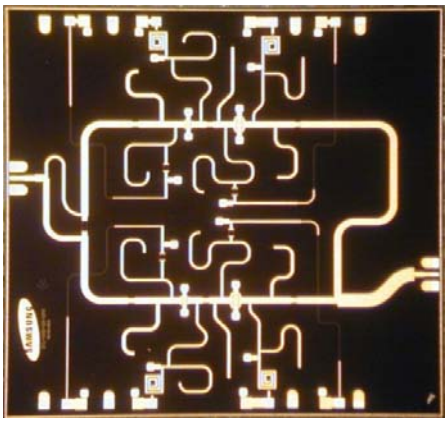

Fig. 7. *Chip photograph of the Doherty power amplifier. Chip size is 5x5 mm^2.*

The experimental results from this Doherty amplifier in its original condition with no chip modifications are reported in [11]. The amplifier achieved 25.1 dBm output power, 38% peak PAE and 27% back-off PAE at 26.4 GHz. We found that when the amplifier was driven close to compression there was a large enough DC gate current to cause a significant voltage drop across the series resistor described in section 2.2, thus limiting the maximum output power. We were able to use a focused ion beam to edit the chip and short circuit the resistor and prevent any voltage drop.

With the resistor short-circuited, the best bias condition tested for this Doherty amplifier is shown in Table I. The driver stage and power stage gate voltages of the peaking amplifier were set to -1.26 V and -1.22 V, respectively, so that the peaking amplifier turns on as the main amplifier begins to compress at 21 dBm output power. The drain voltages of the individual stages were individually tuned for the best power and efficiency. The output stage of the main amplifier was designed for a load-line match with a 5 V drain voltage, so the tradeoff between efficiency and power did not warrant increasing the drain voltage to 6 V. Additionally, since the peaking amplifier was biased in Class C, it required a higher drain voltage to reach the same output power as the main amplifier output and fully modulate the load to 50 Ω.

Table 1 Doherty amplifier bias condition

Main PA Stage 1	Main PA Stage 2	Peak. PA Stage 1	Peak. PA Stage 2
Vdd = 6 V	Vdd = 5 V	Vdd = 6.5 V	Vdd = 5 V
Idd = 17 mA	Idd = 10 mA	Vgg = -1.26 V	Vgg = -1.22 V

The design included an asymmetric Wilkinson splitter to address this problem as well, but during testing we observed an additional benefit from using asymmetric drain voltages. Figure 8 shows the small signal S-parameters of the Doherty amplifier. The small-signal input return loss suffers from the mismatch in the Class C peaking amplifier. The amplifier achieves a small signal gain of 9 –10.5 dB in the 26 – 27 GHz frequency band. There is a 1% frequency shift in the S_{21} trace, mainly due to errors in the extrapolation of the transistor model for use with larger gate peripheries. The gate peripheries of the transistor cells used in our design are 2 – 3 times larger than the transistor cells used by the foundry to develop the model. Figure 9 demonstrates the measured PAE, gain and output power versus input power at 26.6 GHz. The amplifier has a small signal gain of 10.5 dB, an output 1 dB compression point of 26.9 dBm, a maximum power added efficiency of 42% and a 6 dB back-off power added efficiency of 32%.

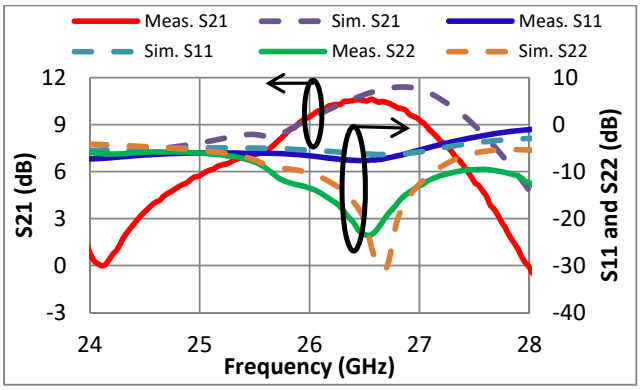

Fig. 8. *Measured S-parameters of DPA. V_{DM1} = 6 V, V_{DM2} = 5 V, V_{DP1} = 6.5 V, V_{DP2} = 5 V, I_{DM1} = 19 mA, I_{DM2} = 8 mA, V_{GP1} = -1.26 V, V_{GP2} = -1.22 V*

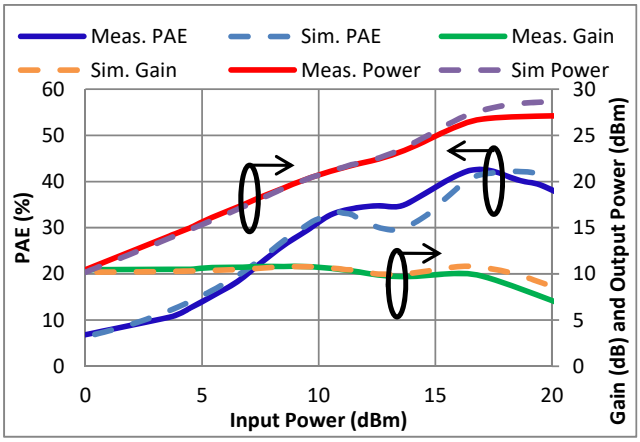

Fig. 9. *Measured output power and PAE of DPA at 26.6 GHz, simulated output power and PAE of DPA at 27.2 GHz. V_{DM1} = 6 V, V_{DM2} = 5 V, V_{DP1} = 6.5 V, V_{DP2} = 5 V, I_{DM1} = 19 mA, I_{DM2} = 8 mA, V_{GP1} = -1.26 V, V_{GP2} = -1.22 V*

The main amplifier was also fabricated separately for further testing and verification. Figure 10 shows the measured efficiency for Doherty amplifier and the main amplifier versus output power back-off

for comparison. The Doherty power amplifier was biased the same as in Figures 8 and 9. The driver stage of the individual main amplifier was biased at a drain voltage of 6 V and a drain current of 18 mA. The output stage of the individual main amplifier was biased at a drain voltage of 5 V and a drain current of 9 mA. The Doherty power amplifier has a 2% lower maximum efficiency due to the loss of the transformer and power combiner, but has a 10% higher efficiency at 6 dB back-off power and a 7% higher efficiency at 10 dB back-off power.

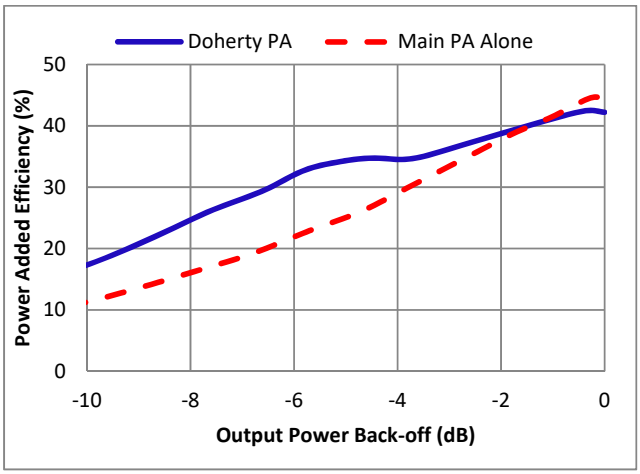

Fig. 10. *Measured PAE versus back-off level for DPA and individual main amplifier at 26.6 GHz.*

To illustrate the Doherty action, Figure 11 shows the drain currents of the main and peaking amplifiers as a function of drive level. At a drive level of 11 dBm, as the main amplifier begins to exhibit some gain compression as shown in Figure 9, the peaking amplifier begins to turn on. As the drive level is increased from 11 dBm, the peaking amplifier supplies more current to the output, and modulates the load of the main amplifier. This keeps the main amplifier in a high efficiency region, compressed state over this power range. At a drive level of 17.5 dBm, the main and peaking amplifiers have reached approximately equal drain currents in the output stage and the Doherty power amplifier is in its 1 dB gain compression.

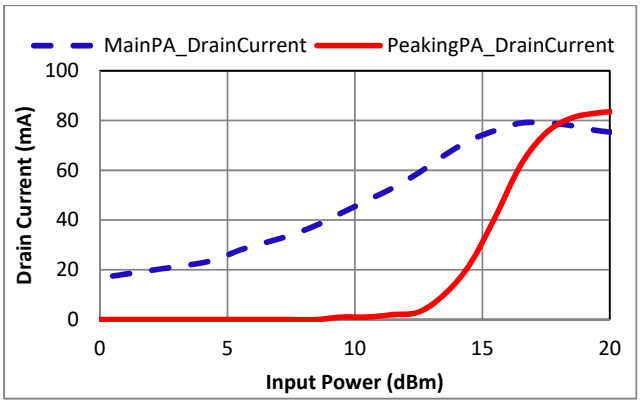

Fig. 11. *Measured DC drain current of main PA and peaking PA at 26.6 GHz.*

Figure 12 shows the performance of the Doherty power amplifier over a 1 GHz bandwidth, from 26 GHz to 27 GHz. The amplifier achieves an OP1dB of 26.3 – 26.9 dBm, a peak PAE of 30 – 42%, and a PAE at 6 dB back-off of 27 – 32%. Figure 13 shows the measured third order intermodulation of the DPA at a center frequency of 26.6 GHz and with tone spacings of 500 kHz and 50 MHz. The input power of each individual tone is swept to 15 dBm so that the total input power is 18 dBm and the DPA reaches saturation. Table II presents a comparison of our Doherty power amplifier with other reported mm-wave Doherty power amplifiers. Using a 0.15-μm GaAs process, our two stage Doherty power amplifier achieves the highest P_{sat}, PAE_{max} and $PAE_{back\text{-}off}$ in Ka-Band.

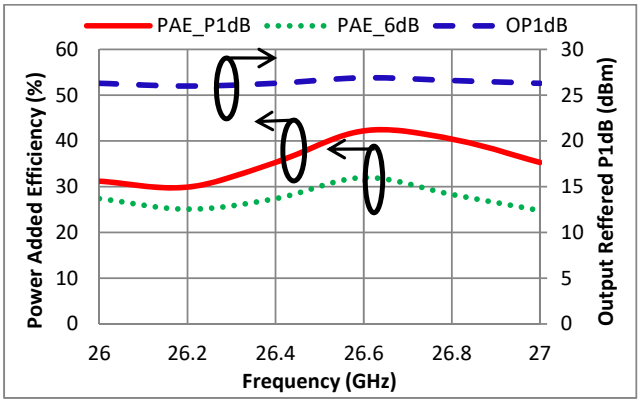

Fig. 12. *Measured OP1dB, maximum PAE and back-off PAE versus frequency of the DPA.* V_{DM1} *= 6 V,* V_{DM2} *= 5 V,* V_{DP1} *= 6.5 V,* V_{DP2} *= 5 V,* I_{DM1} *= 19 mA,* I_{DM2} *= 8 mA,* V_{GP1} *= -1.26 V,* V_{GP2} *= -1.22 V.*

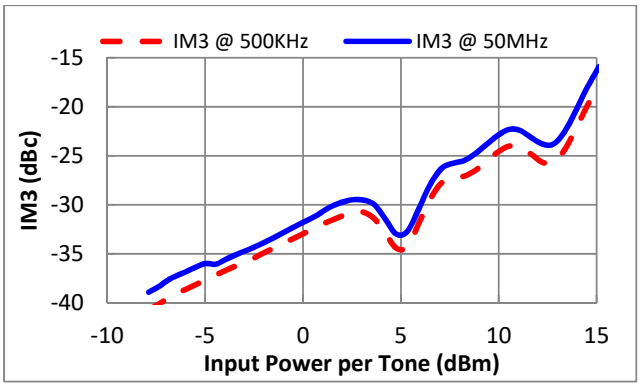

Fig. 13. *Measured third order intermodulation of the DPA with center frequency of 26.6 GHz, and with 500 kHz and 50 MHz tone spacing.*

4. Conclusion

We demonstrated a fully integrated Ka-band Doherty power amplifier for use in emerging wireless applications. The DPA was developed in TriQuint's 0.15-µm GaAs pHEMT technology and is comprised of two gain stages in both the main and peaking amplifiers. Our DPA achieves a measured output power of 26.9 dBm and a maximum PAE of 42% at 26.6 GHz. To the best of the author's knowledge, the PAE at 6 dB back-off power of 32% is the highest reported to date for a power amplifier in the Ka-Band.

Table 2 Comparison to previous results

Process	Ref.	Freq (GHz)	Supply (V)	Psat (dBm)	Peak PAE (%)	Back-off PAE (%)	Gain (dB)
45 nm CMOS SOI	[8]	42	2.5	18	23	17	7
GaAs HEMT	[5]	24	6	30.9	38	20	12.5
GaN HEMT	[6]	23	20	36.8	48	34	16
GaAs HEMT	[7]	42	5	21.8	25	23	7
GaAs HEMT	**This work**	26.6	5	26.9	42	32	10.5

5. Acknowledgement

We acknowledge the support of Samsung Telecommunications America in Richardson, TX.

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