UNIVERSITY OF CALIFORNIA,
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A Fully-Synchronous Multi-GHz Analog Waveform Recording And Triggering Circuit

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

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Dissertation Committee:
Professor Stuart Kleinfelder, Chair
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2017

DEDICATION

To the memory of Sabitha Puligundla,
my free spirited aunt.

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1. S.A. Kleinfelder, E. Chiem, **T. Prakash**. "The SST Fully-Synchronous Multi-GHz Analog Waveform Recorder with Nyquist-Rate Bandwidth and Flexible Trigger Capabilities," 2014 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Seattle, WA, 2014, pp. 1-3.

2. S.A. Kleinfelder for **the ARIANNA Collaboration** "Design of the Second-Generation ARIANNA Ultra-High-Energy Neutrino Detector Systems," Proceedings, 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC 2015): San Diego, California, USA pages 1-4, 2015

3. S.A. Kleinfelder, E. Chiem, **T. Prakash**. "The SST Multi-G-Sample/s Switched Capacitor Array Waveform Recorder with Flexible Trigger and Picosecond-Level Timing Accuracy," arXiv:1508.02460 [physics.ins-det], 2015.

ABSTRACT OF THE DISSERTATION

A Fully-Synchronous Multi-GHz Analog Waveform Recording And Triggering Circuit

By

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Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine, 2017

Professor Stuart Kleinfelder, Chair

The Antarctic Ross Ice-shelf Antenna Neutrino Array (ARIANNA) experiment is designed to detect ultra-high energy (UHE) neutrinos produced by the collisions of cosmic rays with the cosmic microwave background (CMB). A new single board data acquisition (DAQ) system was deployed as an instrumentation solution for the ARIANNA experiment and the heart of this new DAQ system is the Synchronous Sampling and Triggering (SST) integrated circuit. This dissertation focuses on the design and performance of the SST chip and a second experimental chip (SST0.18μ) in an attempt to scale down and investigate design techniques to reduce fixed pattern noise.

The Synchronous Sampling and Triggering circuit can be dubbed as an "oscilloscope on a chip with triggering capabilities". Fabricated in 0.25μ CMOS process, the SST contains 4 channels of 256 samples per channel. The chip has 1.9V input range on a 2.5V supply, 12 bits of dynamic range and an analog bandwidth of 1.5 GHz. The sampling clocks are generated synchronously via a circular array of high speed shift registers driven by an external LVDS oscillator. The SST can operate in wide range of sampling speeds with rates spanning over 6 orders of magnitude (2 k-samples/s to 2 G-samples/s). The SST was designed for simplicity of operation, only three active control signals are necessary for its operation. Each individual channel has a very sensitive real-time dual threshold triggering circuitry with windowed

coincidence features to detect very small and fast impulse signals. The circuitry is capable of discriminating signals with ∼1mV RMS resolution at >600 MHz bandwidth. Triggering options include, direct readout of comparator results or exclusive triggering on dual threshold crossing with adjustable time window. After calibrating for the fixed pattern timing noise, the SST achieves a timing resolution of 2.1 ps.

Fabricated in 0.18μ RF CMOS process, a second chip (SST0.18μ) was developed to reduce the fixed pattern sampling interval error. The SST0.18μ contains 4 channels of 512 samples per channel. The chip achieves a sampling speed of 3 G-samples/s with analog bandwidth of 1.2 GHz. It has a 900mV input range on a 1.8V power supply. The fixed pattern timing noise is characterized by stochastic zero-crossing method and the RMS value of the sample interval error is 8.28 ps.

Equipped with the SST analog waveform recording and triggering chip, the new data acquisition system has been successfully developed and deployed in the Antarctica's Ross Ice Shelf. The DAQ systems are actively monitoring for short radio Cherenkov pulses since 2014-15 austral summer.

Chapter 1

Introduction

The development of faster, cheaper and high precision analog waveform recorders has greatly benefited the high energy particle physics community. The Synchronous Sampling and Triggering (SST) circuit was designed as an instrumentation solution for the ARIANNA Ultra-High-Energy Neutrino Detector. Synchronous Sampling and Triggering circuit evolved from Switched Capacitor Array (SCA) circuits, first designed by Prof Stuart Kleinfelder for high-energy physics applications [38, 37]. SST can be used in wide variety of applications, they are especially good for applications which has low trigger rate and require excellent time resolution, for e.g., neutrino physics, Cherenkov telescopes in gamma-ray astronomy and medical imaging, specifically in Position emission tomography (PET) where time-of-flight plays an important role.

In this dissertation, the first Part discusses the custom micro-electronics developed for the ARIANNA experiment and it's performance measurements. The second Part presents the full-custom prototype chip developed in $0.18\mu m$ technology. The work aims to combine the reliability and speed of the previous design, while adding a novel FPN free sampling clock generation capability. Lastly, the third Part discusses the design and test results of the new

8-channel 2017 data acquisition system for the ARIANNA experiment.

1.1 Background

Most of the known universe is derived by observing photons across the electromagnetic spectrum. Complementary to this traditional approach, observation of charged cosmic rays has been embraced by astronomers to learn lot more about the cosmos beyond our solar system. The cosmic rays (mostly made up of atomic nuclei or protons) are positively charged particles and are deflected by magnetic fields in our galaxy, therefore their arrival directions do not necessarily point back to the source.

So, for a sharply focused examination of the universe; we need a telescope that can see a particle that is not much affected by the gas, dust, and magnetic fields it passes on its journey and the particle of interest is a Neutrino. This new field where scientists are using a neutrino to investigate the universe is called Neutrino Astronomy. This will hopefully open new horizons and revel unknown phenomena and help us answer several questions about our universe.

1.1.1 Neutrino Physics

In order to account for the missing energy in radioactive decays, Wolfgang Pauli in 1930 postulated an elementary particle (Neutrino) which he believed was carrying away the missing energy. Neutrinos were not discovered until 1956 when Frederick Reines and Clyde Cowan identified this particle [20]. Neutrinos are known to exist in three different states (electron neutrino (ν_e), muon neutrino (ν_μ) and tau neutrino (ν_τ)) as partners to the three heavier charged leptons (e, μ and τ). Much of the nature of the neutrinos are yet to be established.

Over the past couple decades several experiments [22] such as The Sudbury Neutrino Observatory (SNO) [5], Kamiokande [30], Super-Kamiokande[8] and K2K Long-baseline Neutrino Oscillation Experiment [6] have established, beyond any reasonable doubt that a neutrino produced in a particular flavor state (say for example ν_μ) has a finite probability of being detected in a different flavor state (say for example ν_e). This probability of flavor changing depends on the neutrino energy and the distance travelled between the source and the detector. The simplest and only consistent explanation of almost all neutrino data collected over the past two decades is a phenomenon referred to as neutrino mass-induced flavor oscillation. The existence of these oscillations imply that the neutrinos have non-zero mass, a very significant discovery. The origin of neutrino mass is one of the biggest puzzles in particle physics, we do not yet know the mechanism responsible for the generation of the neutrino mass. The answer to this question and few other questions such as *Are neutrinos Majorana or Dirac particles?* and *what is the absolute neutrino mass scale?* can only be revealed by additional information from plethora of particle physics research experiments.

1.1.2 Astrophysical Neutrinos

Neutrinos can be created in several different ways: beta decay of atomic nuclei, nuclear reactions inside stars and supernova and when a cosmic rays interact with atoms. Astrophysical sources can be as close as Earth and Sun and as far away as distant galaxies and even remnants of the Big Bang.

Only two sources of astrophysical neutrinos have been observed, the sun and supernovae. The solar neutrinos are ideal for studying neutrino oscillation properties. The supernovae explosions on the other hand are more interesting. In a core-collapse supernovae, a majority of the energy is directed into neutrino emissions. 99% of the neutrinos escape the star in the first few minutes. In addition, the shock waves from the supernovae explosions are ideal

conditions for the accelerations of cosmic rays.

The only neutrino observation from a supernovae till date is from SN 1987A (core-collapse supernovae). On 23rd February 1987 at 07: 35: 41 GMT two detectors, in USA (the IBM experiment) and Japan (the Kamiokande experiment) recorded a total of 19 neutrino interactions in a span of 13 seconds which occurred in the Large Magellanic Clouds at a distance of 50 Kiloparsecs (around 150,000 light years). Two to three hours later astronomers in the southern hemisphere saw the first supernovae visible to the naked eye. This observation of neutrinos from the sun and the supernovae represented a new kind of astronomy since the neutrinos give us the information about the processes not visible by photons.

1.1.3 Ultra-High Energy Neutrinos from Cosmic Rays

Victor Hess's [31] observation in 1912 of ionizing radiation whose origin was extra-terrestrial let to the birth of cosmic ray physics and in-turn astro-particle physics. It is known that the cosmic rays bombard Earth with energies higher than the most powerful man-made accelerator has been able to achieve so far. It is still unclear how or what sort of astronomical objects can accelerate these charged particles to $E > EeV$. The cosmic ray particles that have highest observed energies are assumed to come from unknown sources outside out galaxy. The highest-energy cosmic ray ever detected was observed on October 15th 1991 by the Flys Eye cosmic ray detector in Utah, USA. The researchers measured the energy to be $3.2X10^{20}eV$ [4]. The acceleration process giving the particles these extreme high energy is not known. In comparison, the energy of the highest cosmic ray particle is 10 million times higher than what Large Hadron Collider in CERN, Geneva can reach. Since the cosmic rays are electrically charged, they will be deflected by magnetic fields in our galaxy, therefore their arrival directions on Earth do not necessarily point back to the source. To detect the source, one needs an electrically neutral particle like the neutrino that is not influenced by

the magnetic fields.

In the 1960s, Greisen, Zatsepin and Kuzmin (GZK) [27, 56] first proposed that the ultra-high energy cosmic rays (UHECR) with energies more than $5X10^{19}eV$ will interact with the cosmic microwave background (CMB) from the big bang and rapidly lose energy given by equation 1.1, thus unable to travel long distances in the universe. The attenuation of the flux of the UHECRs is known as GZK process.

$$p + \gamma CMB \rightarrow \Delta^{+} \rightarrow n + \pi^{+} \tag{1.1}$$

Therefore the sources of ultra-high energy cosmic rays have to be close, not further away than 50 million light years [43]. The existence of these extreme energy cosmic rays ($E > 5X10^{19}eV$) is a real mystery. Three years after the GZK process was proposed, it was realized that when the cosmic rays interact with the cosmic microwave background (CMB), mesons are create which will produce high energy neutrinos via pion decay [15, 51]. These are called GZK neutrinos and almost certain to be extra-galactic.

$$\pi^{+} \rightarrow \mu^{+} + \nu_{\mu} \tag{1.2}$$

$$\mu^{+} \rightarrow e^{+} + \nu_{e} + \overline{\nu}_{\mu} \tag{1.3}$$

Neutrinos do no suffer from any of the aforementioned disadvantages. Some of the candidates for sources of high energy cosmic rays are super massive black holes, Galaxy clusters, Gamma Ray Bursts (GRB) and other violent objects in the universe. These neutrinos will travel, unaffected by the magnetic fields in space and if detected on earth, the will point back to the source of the cosmic rays.

1.1.4 Detection Methods of UHE Neutrinos of Cosmic Origin

Despite suggestions that there is a guaranteed flux of the particles, no detection of UHE neutrinos have been made as of 2016. A number of experiments designed for this purpose have been constructed, utilizing a range of detection concepts. Most of the detection techniques rely of Cherenkov radiation, either in the optical regime or radio regime. Dedicated high-energy neutrino telescopes based on optical Cherenkov techniques have been scanning the cosmos for about a decade. A large scale (km^3) optical detectors are designed to detect visible Cherenkov radiation using photo multiplier tubes. IceCube is one such detector currently operating in the South Pole [28]. These experiments primarily detect neutrinos of energies spanning form $10^{11}eV$ to $10^{15}eV$ range through Cherenkov light given off by the muons produced through a charged-current interaction of a muon-neutrino with nucleons in the ice. Optical Cherenkov experiments are also sensitive to energies greater than $10^{18}eV$ [45], however the size of the detectors are the limiting factors.

At energies $10^{18}eV$ and above, the expected neutrino flux if too small to be detectable in km^3 telescopes. On the other hand the most promising detection technique of UHE neutrino detection is that of coherent radio emission from neutrino-induced shower. This is called the Askaryan Effect. In the 1960s Gurgen Askaryan proposed that an ultra-high energy neutrino in a dielectric medium would give rise to coherent Cherenkov radiation in the radio regime [9, 10]. As a charged particle travels (with a speed of ν), it disrupts the local electromagnetic field and its medium. The electrons in the atoms will be polarized by the passing electromagnetic field of the charged particle. Photons are emitted as an insulator's electrons restore themselves to equilibrium after the disruption has passed, which is different from a conductor in which the EM disruption can be restored without emitting a photon. In normal circumstances, these photons destructively interfere with each other and no radiation comes out. However, when a disruption propagating through the medium with a speed faster than the local speed of light (c_n), the photons constructively interfere and

intensify the observed radiation. Figure 1.1 displays how the Cherenkov condition ($\nu > c_n$) is satisfied to create radiation. The left panel shows the field of a charged particle traveling with $\nu < c_n$. The right one is the field of a charge with a speed larger than c_n, which emits radiation with a strong peak at an angle θ_c from the moving axis. This angle is called the Cherenkov angle, given by the expression:

$$\theta_c = \cos^{-1}(c_n/\nu) \tag{1.4}$$

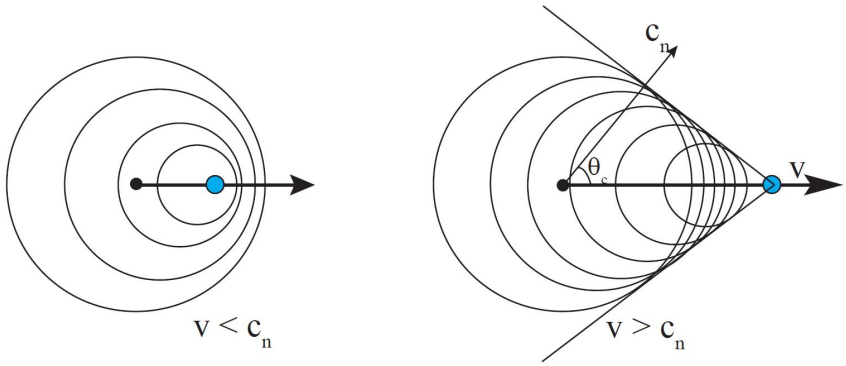


Figure 1.1: Schematic of Cherenkov Effect [23]. ν is the speed of a charged particle, c_n is the speed of light in a medium with a refractive index n and θ_c is the Cherenkov angle [1]

The Askaryan effect states that a charged particle traveling faster than the phase speed of light in dielectric media (such as water, ice, salt or lunar soil) creates a shower of secondary charged particles, which contains charge anisotropy and thus emits a cone of coherent radiation in the radio part of the electromagnetic spectrum [9]. The particle shower mostly consists of electron-positron pairs and photons. In the beginning the shower of charges has equal positrons and electrons, so there is no net charge and hence no Cherenkov radiation. As the EM shower progresses, the mutual conversion of particle into electromagnetic energy in the medium, combined with the available of atomic electrons which can be up-scattered into the shower by the Compton scattering, leads to a 20% excess of negative charges. Dur-

[1] figure originally published in [23]

ing the propagation of the extra charges, there will be a small transverse deviation for each individual particle, which causes the shower to have a transverse width in the order of few cm in dense media. At less than GHz frequencies the wavelength of the Cherenkov radiation of each negative charge exceeds the dimension of the compact charged-particle and photon bunch, and therefore the overall radiation of the particle shower is coherent in the form of impulses [23]. In a nutshell Askaryan recognized that the phases of all emitted photons are not random which means that the power of the coherent radio pulse is proportional to the square of the net charge in the shower and the net charge proportional to the primary energy of the initial particle.

Several experiments have been conducted to verify the Askaryan effect in laboratory settings. SLAC National Accelerator Laboratory experimentally verified the Askaryan effect in ice, salt and silica.

1.1.5 The ARIANNA Detector

The ARIANNA (Antarctic Ross Iceshelf ANtenna Neutrino Array) experiment, first proposed in 2005 by Dr. Steven W. Barwick, is designed to detect the neutrino flux in the ultra-high energy (UHE) range ($10^{17} - 10^{20}$ eV) [13, 11, 29]. The goal of the experiment is the detection of radio pulses initiated through Askaryan effect produced via neutrino-nucleon interaction in the ice of the Ross Ice Shelf.

The neutrino flux from the GZK effect is extremely low, typically in the order of 1 neutrino per km^2 per week arriving over 2π steradian at $\sim$EeV [24]. Therefore the neutrino detection in the ultra-high energy regime is extremely challenging. A very large target volume with low loss medium for converting the incoming neutrinos to RF signals is required. Ross Ice Shelf, by and large, Antarctica is an ideal target due to several crucial features. There is minimal human activity and relatively low anthropogenic noise levels. The ice shelf acts as a vast

and existing medium for neutrino detection. The ice is transparent to electromagnetic waves at radio frequencies and the ice-water interface behaves like a mirror for radio emissions, reflecting them towards the detectors array on the surface of the ice. Close proximity to the McMurdo base allows for a large array to be deployed and maintained.

The aim of the ARIANNA neutrino detector is to detect the coherent Cherenkov radio pulses generated by the neutrino-nucleon interactions in the ice through sets of radio antennas embedded just beneath the surface and hosted within independent stations installed in a hexagonal grid like fashion. When completed, the full detector will consist of 1296 autonomous surface stations separated by 1km. The experiment achieves a large aperture (effective volume $\times$ solid angle) by covering a vast area (900 km^2 over 500 m thick ice) combined with a larger than 2π steradian view of the sky. An illustration of ARIANNA station and the method by which it looks for UHE neutrinos is shown in Figure 1.2.

The initial prototype station with the first generation data acquisition system was deployed during the 2011/12 season. Almost a complete system redesign has been made and deployed during the 2014/15, 2015/16 and 2016/17 seasons. A complete system overhaul, updating the power and communications towers, a new single board 4-channel data acquisition system to replace the previous motherboard/daughter-card system, amplifier re-design has been made. The new system has improved physical and electrical robustness, better features and performances, consumption of substantially less power, cost effective and most importantly easier calibration features.

A photograph of the ARIANNA station is shown in the figure 1.3.

[2]Image created by Scott Brown, originally published in [17]

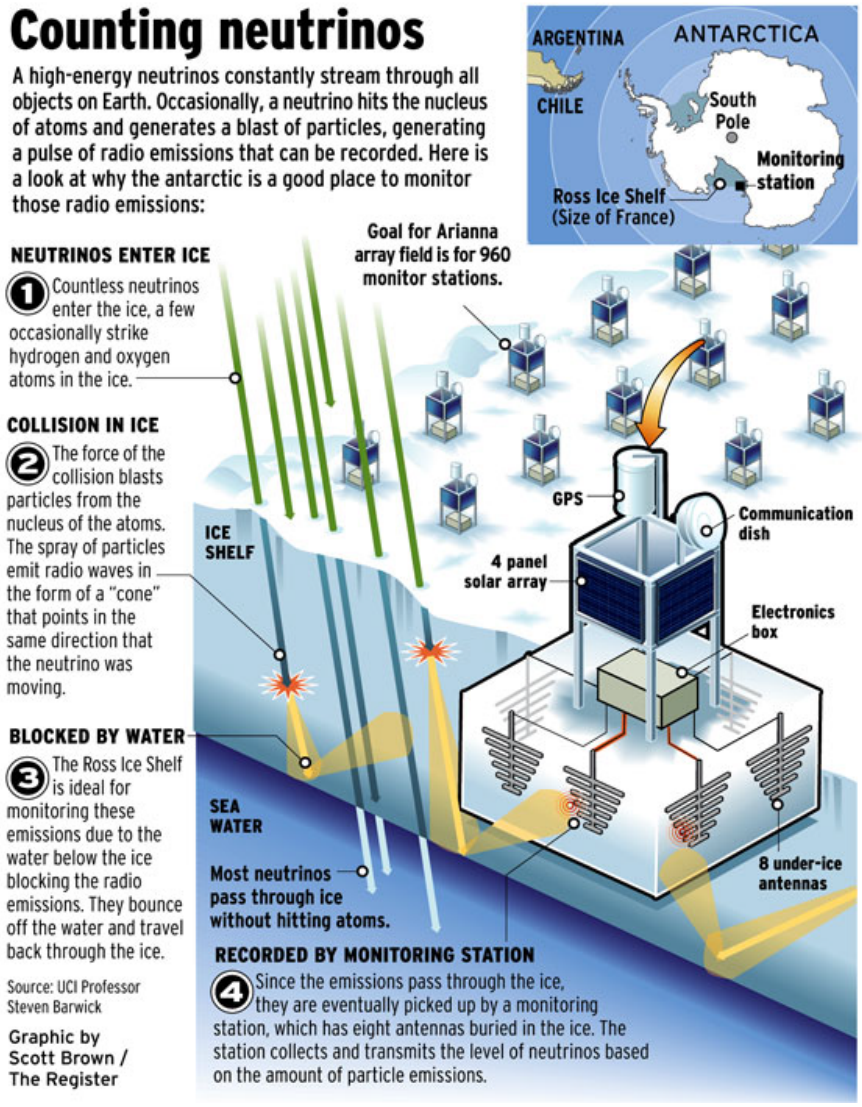


Figure 1.2: Illustration of ARIANNA Neutrino Detector [2]

1.2 Data Acquisition and Trigger System

This section provides an overview of the Data Acquisition (DAQ) System used in the ARIANNA experiment. A brief discussion about the first generation DAQ system (deployed during the 2011/12 Antarctic season), the rational behind the upgrade and an introduction to the second generation DAQ system (deployed during the 2014/15 Antarctic season), with emphasis on the switched capacitor array circuits is presented.

Figure 1.3: Photo of one of the ARIANNA stations taken during the 2015/16 season[3]

1.2.1 Overview

Each independent station of the ARIANNA experiment consist of four Log-Periodic Dipole Array (LPDA) antennas which are sensitive from 100MHz to 1GHz in air and down to 80 MHz when immersed in the firn [25]. Each antenna feeds a high-gain amplifier then an ant-aliasing filter which in turn feeds a custom designed Waveform Acquisition Chip with triggering capabilities. The firing of the trigger causes the sampled data from the chip to be readout and digitized by an analog to digital converter. The digitized data is stored in the SD card. An mbed microcontroller and a Xilinx Spartan 3 FPGA is used to perform all the housekeeping. Most of the electronics are housed in a metal box which is buried with its top flush with the snow level. The microcontroller also communicates with the outside word via the AFAR Wireless Ethernet Bridge and Iridium Short Burst Data (SBD) satellite communication module.

The detection procedure of the Data Acquisition System (DAQ) is as follows: Each LPDA antenna detects a radio frequency pulse (typically between 0.1 and 1 GHz) generated by a

[3]Photo courtesy Anna Nelles, picture originally published in [12]

UHE neutrino interactions with the hydrogen and oxygen nuclei in the ice. The pulse is fed to the amplifier box, where it is filtered through high-pass and low-pass filters in order to eliminate the aliasing noise and later amplified using the high-gain amplifiers designed for ARIANNA. The amplified pulse is sent out of the amplifier box through a limiter and two attenuators. The aim of the amplifier box is to produce a radio pulse with low noise and less distortion in the waveform acquisition circuit's dynamic range. This amplified pulse is fed into the waveform acquisition circuit through a Bias-Tee which shifts the voltage level of the radio pulse. The waveform acquisition circuit will be continuously sampling the incoming radio pulse until a neutrino event occurs, at which point the circuit will assert a trigger signal. This trigger signal is continuously monitored by the FPGA, after the trigger signal is asserted, the FPGA will generate a stop pulse which is sent back to the waveform acquisition circuit. This stop pulse halts the sampling on the chip and enables the data to be readout. The digitized data is temporarily saved on the FPGA, then transferred to the SD card through the microcontroller for further processing. During a communication window, the stored data is transmitted from Antarctica over Iridium satellite and high speed wireless internet connection.

Capturing an Askarayan radio pulse produced via neutrino-nucleon interaction is a challenging task. The design of a custom made waveform acquisition chip is of utmost importance to maintain high signal integrity. The Askarayan radio signals can span over large range of frequencies, so in addition to high sampling speeds the chip should also have broad and flat frequency response.

As mentioned in the subsection 1.1.5 a complete overhaul of the ARIANNA detector was performed during 2014 and 2015 campaigns. During this time a new synchronous sampling chip was developed to replace the old switched capacitor array based waveform acquisition circuit. In the following sections, the first generation DAQ system, its pitfalls and motivations behind developing a new DAQ system is discussed. Emphasis will be given to the waveform

acquisition circuits of both generations.

1.2.2 First Generation (ATWD) ARIANNA DAQ System

The first generation ARIANNA data acquisition system had a motherboard-daughter card configuration. The prototype stations were designed based on the Advanced Transient Waveform Digitizer (ATWD) [41, 32] chip designed Professor Kleinfelder and his research group. The ATWD was a single channel digitizing IC and it was part of a daughter card which was then installed on 4-channel motherboard. The ATWD data acquisition system is shown in the figure 1.4. The system found considerable success during the second deployment season in 2012, with a number of the systems deployed.

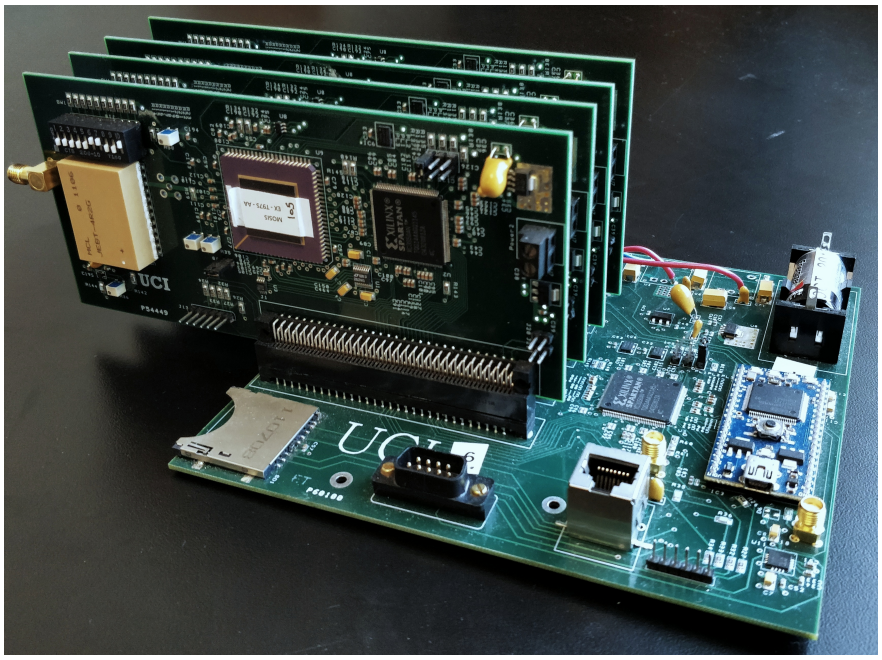


Figure 1.4: A four channel ATWD data acquisition system. The ATWD chip is mounted on the daughter card which is in-turn mounted on a motherboard (a square chip with a white label across it)

The ATWD data acquisition system was designed to improve the selectivity to detect the neutrino radio shower. The system contains four ATWD sampling chips that operate syn-

chronously with high timing precision, and also deliver real-time triggers based on waveform pattern matching.

The ATWD circuit contains a linear array of 128 sample and hold (S&H) circuits for sample storage, arranged as a circular buffer, and attains 2 GHz sample speeds. Sample clock generation is synchronous, combining a phase-locked loop (PLL) for high-speed clock generation and a high-speed fully-differential shift register for distributing clocks to all 128 sample circuits. This permits a low-frequency external reference clock to generate the 128 high-speed sample clocks. This semi-synchronous technique eliminates the need to supply and distribute very high speed system-level clocks. It also has the advantage that the timing jitter and drift in the internal high-speed clock is well controlled in comparison to previous techniques.

The ATWD chip is novel and greatly advanced, yet complications that degrade the system performance still persists. The designers of the first generation DAQ system identified three main issues with the ATWD chip (these issues are briefly discussed below) [57]. Despite, resolving few of the issues, a design change appears to be the best approach.

The designers identified that the sample and hold clock (pointer) in the ATWD chip either grows and/or shrinks over time. This behavior was called as the slippage issue. On many occations, pointer growth is more frequent in ATWD. The designers believed that the clocking was imperfect and in the presence of electronic noise, setup and hold times of the shift registers were violated.

The designers coped with the issue by periodically resetting the chip. The failure rate is exponential with time, therefore a brief but frequent periodic resets were used. The designers were able to effectively eliminate the issue by allowing the ATWD to run only during the initial narrow time period due to the probability of slippage is very low. Experimental results depict that a reset signal applied to the ATWD at a constant rate of 17μs [57] will result in the elimination of relatively all slippage.

ATWD has no direct read of the stop (pointer). As a result, analysis became more arduous. Therefore, for the second generation data acquisition chip a direct readout of the stop bits transpired.

Asynchronous stop is yet another issue with ATWD. Once the ATWD signals the trigger, the system should assert a stop signal to the ATWD. The arrival of the stop to the ATWD will halt the sampling process. This stop signal is asynchronous to the ATWD internal clock, which causes potential problems to the data acquisition system such as: Synchronization failure and improper sample and hold switch positions (i.e., intermediate voltages). These problems were never observed, but the second generation data acquisition chip was designed to be fully synchronous.

For the ARIANNA experiment target sample clock frequency is 2 GHz, the chip is designed to achieve close to the Nyquist-rate analog sampling bandwidth of 1 GHz in realistic system usage. The bandwidth of an entire system is inevitably lower than that of the Sample and Hold circuits. This is due to the totality of various bandwidth-limiting components such as the front-end amplifier characteristics, high and low-pass filtering, capacitance and inductance from chip packaging and wire bonds, etc. For the data acquisition system, the net 3-dB bandwidth was measured to be over 800 MHz. This bandwidth is less than the Nyquist rate. The second generation DAQ was designed to have Nyquist rate system bandwidth.

1.2.3 Second Generation (SST) ARIANNA DAQ System

A four-channel/single-board data acquisition system was developed for the ARIANNA experiment to replace the previous motherboard/daughter-card system. This new second generation system was designed based on the Synchronous Sampling and Triggering (SST) chip. The SST data acquisition system has an updated amplifier design, with new and better battery management units. The hardware upgrades improve the robustness of the complete

system. The second generation DAQ system is more cost effective, consumes less power and is much easier to calibrate compared to the first generation DAQ system. A photo of the SST data acquisition system is presented in the figure 1.5. As of 2016/17 Antarctic season, ten SST stations (7-HRA stations and 3 Cosmic-ray stations [12]) have been successfully deployed in Ross Ice Shelf and are currently collecting data.

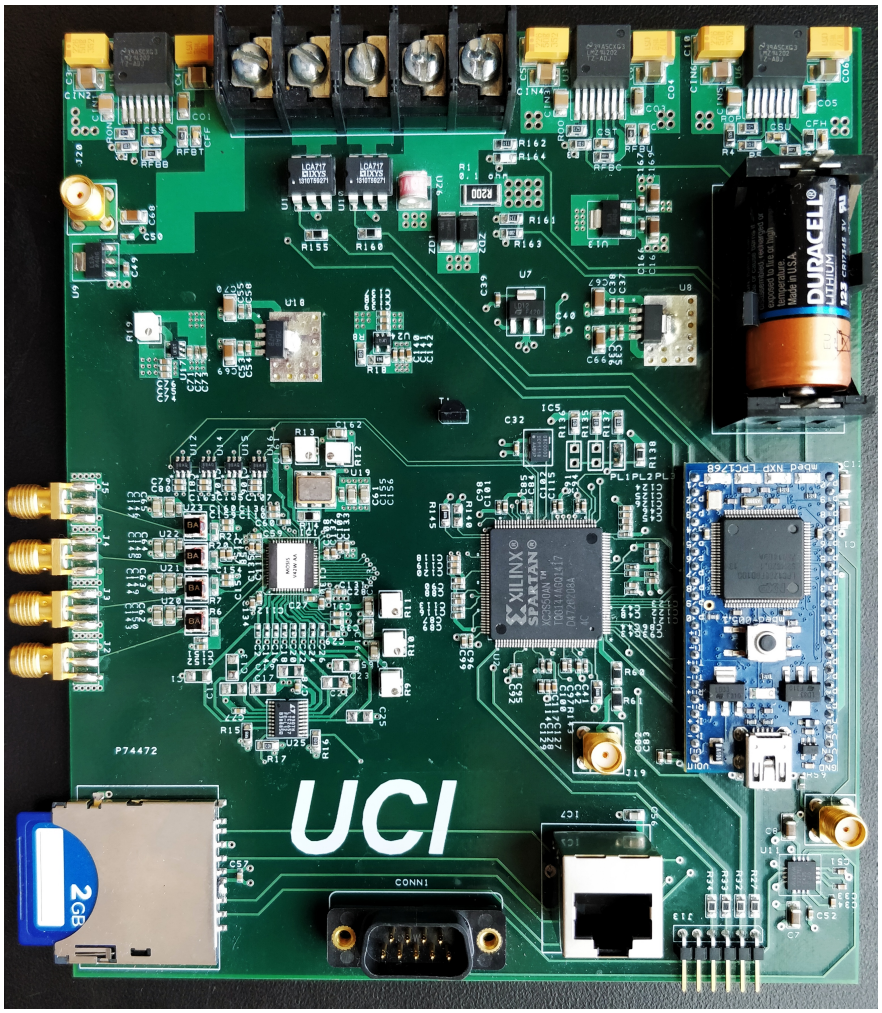


Figure 1.5: Second Generation Four Channel Single Board Data Acquisition System with the SST Chip (A Square Chip with a White Label Across it, Center-Left of the Board)

Synchronous Sampling and Triggering (SST) chip was designed to simplify the ATWD chip and achieve major improvements. The chip contains 4-channels instead of 1 and is housed in an extremely small package. A photo comparing both ATWD and SST packages are

presented in figure 1.6. The sampling in the new system is completely synchronous without the use of PLL or delays. The chip features stable working capacity with clock rates over 6 orders of magnitude. The SST was designed for simplicity of operation, and only three active controls are required for operation: a Start/Stop pin that starts and stops sampling for convenient common-start or common-stop operation, a Reset pin, and a Read-Clock pin. The SST achieves nearly flat frequency response out to ∼1.3 GHz and 1.5 GHz -3 dB bandwidth using a standard 50 Ohm input signal. It includes fast, flexible trigger capabilities with ∼1 mV RMS sensitivity in response to pulses of 500 ps full-width at half-maximum. A 0.25 μm CMOS process allows large input voltages resulting in considerable reduction in power usage. It also features 256 samples and hold circuits, double that of the ATWD. It supports both single ended as well as differential trigger outputs apart from multiple trigger voltage outputs. SST has the capability to read the position of the sampling pointer, a feature that greatly helps in debugging the readout data.

Figure 1.6: A Picture of ATWD Chip(Left) and SST Chip(Right) Placed Side-by-Side [4]

1.2.4 Third Generation 8 Channel (SST) ARIANNA DAQ system

After the incredible success of the second generation DAQ system, the next logical step for the ARIANNA engineering team was to see if the number of channels per board could

[4]Photo courtesy Dr. Stuart Kleinfelder

be doubled. For the 2017/18 Antarctic season, a new 8 channel DAQ system board was designed. The design of the new 8 channel system board was greatly inspired from the already successful second generation 4 channel data acquisition board. The new 8 channel DAQ board accommodates two SST chips, effectively doubling the number of channels, new improved firmware and an updated MBED microcontroller code. Having more channels per station improves the effective volume of the ARIANNA station.

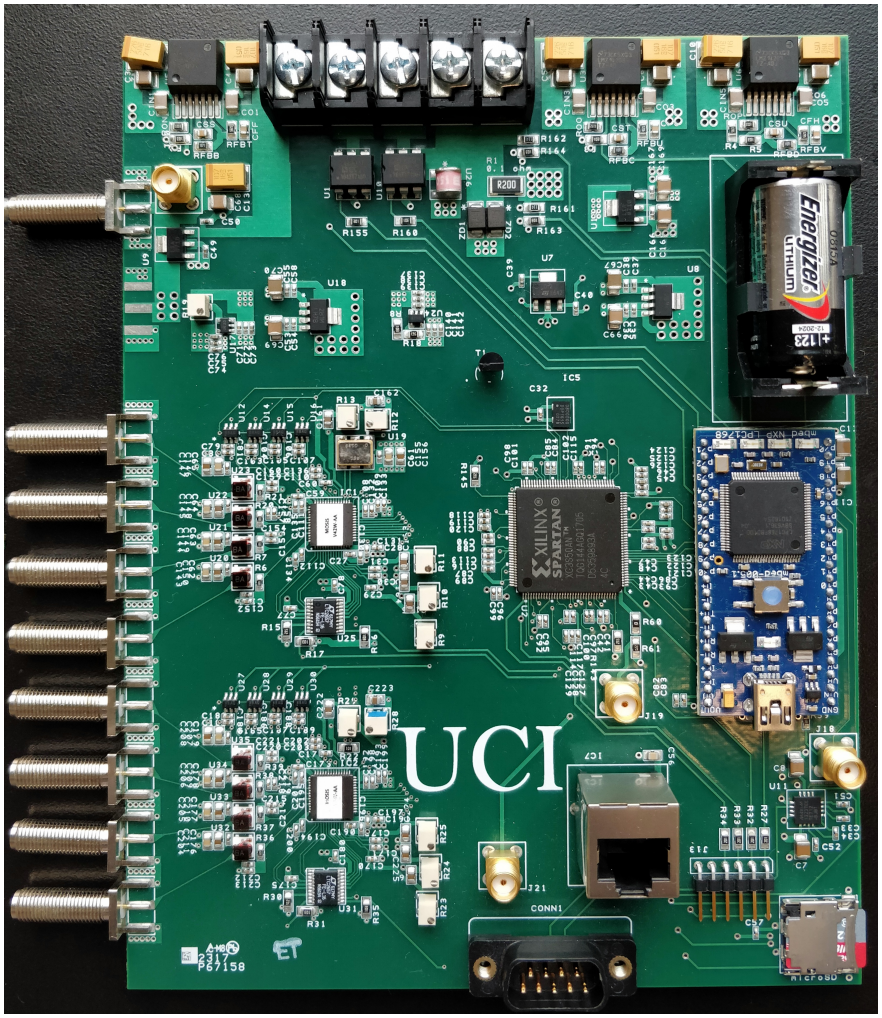


Figure 1.7: Third generation eight channel single board data acquisition system with two SST chips

Part I

Synchronous Sampling and Triggering (SST) Circuit Design and Results

Chapter 2

Synchronous Sampling and Triggering Integrated circuit

This chapter presents the work on the synchronous Sampling and Triggering Integrated Circuit (SST). As the name implies, the objective of the SST is to sample and readout very fast analog signals (in the range of 1.5 GHz) with pico-second timing precision. A hierarchal and block level description of SST circuit is provided with emphasis on clock generation, data acquisition, triggering and analog data readout is presented. The two operating modes of the SST acquisition mode and the readout mode is also presented. The functionality of the control signals are explained.

This chapter also discusses the analog and mixed signal circuit blocks used in the SST. Each circuit block is analyzed on a transistor level and examines the component's functionality, design, and challenges. The circuit blocks discusses are the LVDS receiver, clock synchronizer, two phase non overlapping clock circuit, clock distribution network, high speed sampling clock, sampling and readout circuit, triggering logic, readout clocking circuitry and stop position readout circuitry.

2.1 Technology Used

The SST is fabricated using the $0.25\mu m$ CMOS design kit provided by Taiwan Semiconductor Manufacturing company limited (TSMC). The details of the characteristics and performance of these technologies are confidential. Publicly available information about the process properties and fabrication options will be discussed.

2.1.1 The $0.25\mu m$ CMOS Process

The SST was fabricated using TSMC $0.25\mu m$ CMOS process. The CMOS process has 5 metal layers and 1 poly layer and the process is for 2.5V applications. A thick-oxide layer can be used for 3.3 V transistors. This technology offers Thick TopMetal (inductor) and MIM options. The MIM (CapTopMetal) provides a capacitance of $1fF/\mu m^2$. The process allows for resistors to be designed using either poly or NWELL layers. The option of silicide block is available for the poly resistors. The process also offers three threshold voltages: "Nominal", "Medium" and "Zero", Zero threshold voltage is also called depletion threshold voltage. For the SST, we have the default threshold voltage which is "Nominal". The nominal threshold voltages without any body effect for NMOS and PMOS are about 0.51V and -0.52V respectively. NMOS transistors generally yield better performance than PMOS transistors due to its 4.5 times higher electron mobility compared to hole mobility.

2.2 Overview, Theory and General Architecture

The Synchronous Sampling and Triggering (SST) chip is a fully-synchronous multi-G-samples/s analog transient waveform recorder and readout integrated circuit with fast, flexible and real time triggering capabilities. The SST chip contains 4 channels with 256 samples per channel

to capture the analog input signal. The SST is designed and fabricated in $0.25\mu m$ CMOS process. The chip has 12 bits of dynamic range and uses approximately 128mW of power while operating at 2 G-samples/s. With standard 50Ω input source, the SST achieves 1.5 GHz of 3 dB bandwidth. The synchronous and purely digital nature of the SST, a pico-second level timing uniformity is achieved over six orders of sampling frequency. Only three active control lines are required for normal operation of the SST, this makes the SST very easy to use and control. The SST can discriminate signals with $\sim$1mV RMS resolution. The real-time flexible trigger outputs can either be CMOS or low-voltage differential signals (positive ECL 0.8V) for low noise operation.

The SST circuit belongs to a family of high speed analog waveform acquisition and read-out circuits. The analog waveform acquisition and readout circuits evolved from Switched Capacitor Array (SCA) circuits first developed by Prof. Stuart Kleinfelder [36]. The SCA circuits are storage devices used to save analog signals until they can be readout at a later instance of time. The SCA circuits are essentially analog time delay elements which holds signals until they are either digitized or discarded. The voltage level of the analog signal is stored on the capacitor cells, the process of storing will be continued in a circular fashion, to provide the sampling event information. When an interesting event is collected, the data can be readout and digitized by Analog to Digital Converter (ADC).

The SCA circuits have evolved continuously over the past three decades, SCA circuits with parallel analog to digital conversion, asynchronous clocking with phase locked loop and delay lock loop based clock generation have been widely used in the field of particle physics. SST belongs to a new generation of SCA circuits with synchronous sampling with sample rate spanning over 6 orders of magnitude, high dynamic range and timing precision with Nyquist rate bandwidth.

The following discussion presents the hierarchal description of the SST circuit. Figure 2.1 shows the architecture of the Synchronous Sampling and Triggering circuit, all the individual

blocks and their connections are also shown.

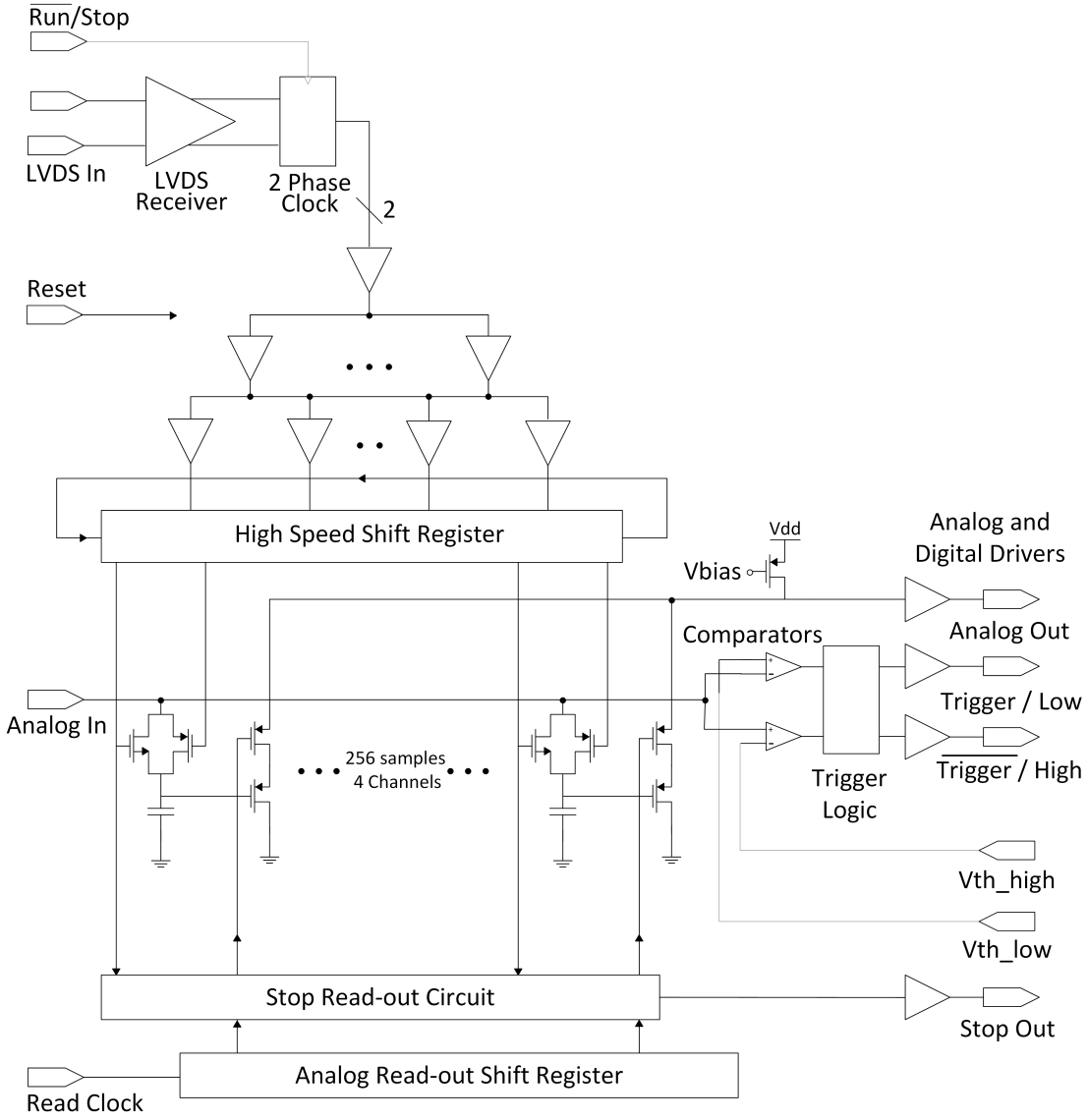


Figure 2.1: Synchronous Sampling and Triggering Circuit Block Diagram [1]

The SST relies on an external Low Voltage Differential Signaling (LVDS) oscillator to generate sampling clock signals. LVDS standard is widely used across the industry to generate low jitter signals with high timing accuracy. The LVDS receiver circuit provides the on chip clocking signals for the SST, the essential function of the SST is to convert the external LVDS clock to the complementary, rail-to-rail clock.

[1]The schematic originally published in [39]

The rail-to-rail full scale clock, 0V to 2.5V is then passed to a 2 phase non-overlapping clock generator circuit. The external $\overline{RUN}/STOP$ signal is passed through a synchronizer circuit and the synchronized $\overline{RUN}/STOP$ signal acts as a reset to the 2 phase non-overlapping clock generator circuit.

The 2 phase non-overlapping clock signal is distributed to the sampling clock generator signal via a reliable, low jitter clock distribution network. The sampling clock for the SST is generated by an array of dynamic shift registers consisting of 128 master-slave shift registers configured in a circular fashion. The sampling clock is nothing but a pointer moving in a circular fashion. The sampling for the SST is achieved by an array of 256 sample and hold cells. Each sample and hold cell will track the input analog waveform, samples the voltage and stores on the switch capacitor. 128 master-slave shift registers supply clock for the 256 sample and hold cells. The SST uses both master and slave section of the shift register to generate the 256 sample clocks, thus doubling the sample rate, e.g., a 1 GHz clock will result in a 2 GHz sample rate.

The sample and hold cells are connected together to an "Analog In" bus line. The "Analog In" bus line consist of multiple metal layers connected together to make a low resistance connection. Based on the sample clock, the sample and hold cell samples the voltage on the "Analog In" line and stores on the switch capacitor.

The "Analog In" line is also connected to a real time fast-flexible trigger circuitry via two comparator circuits, intended for high and low threshold crossings. The comparator circuit monitors the instance when the analog input signal crosses the voltage threshold values, during which time an output signal is generated. This output signal is processed through pulse-stretching latches with delay lines, which can hold the comparator outputs for a specific amount of time. During normal operation of the SST, this pulse-stretched trigger signal is sent to the off chip FPGA to intimate that a signal of interest has been captured. The FPGA will then stop the SST and starts the readout by asserting the read clock signal.

Another set of 256 static shift registers are used to generate the readout clock for the SST. This readout clock is relatively slow compared to the sampling clock and is applied to the analog readout and multiplexing circuitry. The analog readout multiplexing circuitry is an extension of the sample and hold circuitry and it acts a voltage buffer for the sampled input. During the SST readout phase, the stored sample voltages are serially read out with the help of the analog readout and multiplexing circuit.

During the readout phase of the SST, the sample clocks are also read out in parallel. The sample clocks are a steam of zeros with two one's. This steam of bits are referred to "STOP" bits in this dissertation. The STOP bits are very useful to discern the beginning and end of the sampled analog signal.

2.2.1 Operating Modes and Control Signals

The operation of the SST can be divided into two phases: Acquisition and Readout phase. This section explains the SST's two phases of operations and describes the purpose of active and passive control signals of the SST.

2.2.1.1 Acquisition Phase

During normal operation, the SST will be operated in common-stop mode endlessly sampling until it is stopped by a trigger, at which time the sample and hold array contains the signal of interest. In addition to all the bias signals, the SST requires 4 signals for normal acquisition: RESET, STOP, CLOCK and ANALOG INPUT SIGNAL. Figure 2.2 illustrates the input and control signals for the acquisition phase. The figure 2.2 also shows the internal sampling clocks generated by the high speed shift registers and shows the tracking of the analog input signal.

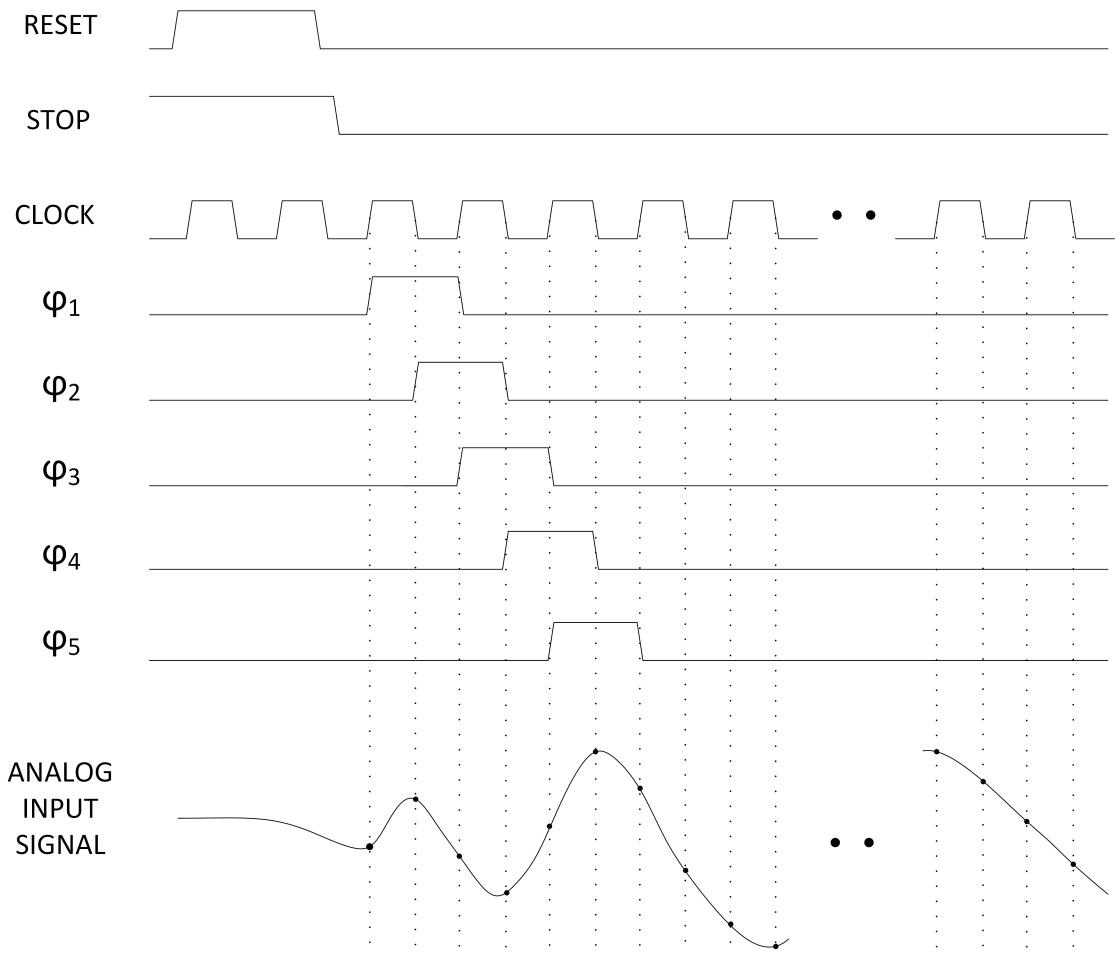


Figure 2.2: Synchronous Sampling and Triggering Acquisition Phase

The acquisition phase of the SST starts off with assertion of the RESET signals and de-assertion of STOP signal. The RESET signal resets or rather initializes the sampling clock generator, i.e., high speed shift registers. When the RESET signal is asserted, the "initialization shift registers" (first two shift registers in the array of dynamic shift registers) will reset and the sampling pointer is generated. Once the RESET signal is de-asserted after at-least one clock period, the sampling pointer will propagate through the shift registers, which in turn samples the input analog signal. For the high speed shift registers to function properly the RESET signal should be high for at least one clock period, during this period the STOP signal is required to be held high.

The STOP signal is also referred to as $\overline{RUN}/STOP$ in this text. The STOP signal is

an external control signal, which dictates the mode of operation for the SST. During the acquisition phase, the STOP signal is set to logic zero and during the readout phase, the STOP signal is set to logic one. The SST begins with continuously acquiring the analog input signal until it is stopped. For the transition from acquisition phase to the readout phase, the STOP signal should switch from logic zero to logic one. At this logic zero to logic one transition of the STOP signal, the internal clock is disabled causing the sampling clock to be stopped and hold its previous position. Figure 2.3 shows the relationship between the STOP signal, internal sampling clocks and the SST's modes of operation.

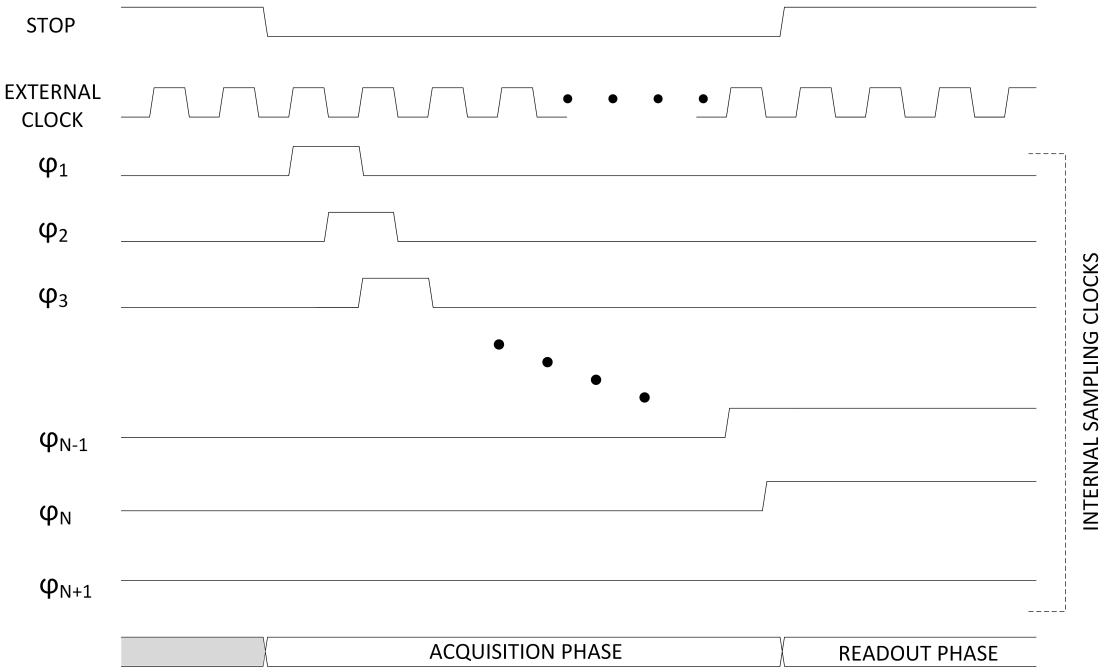


Figure 2.3: SST's Modes of Operation With Respect to STOP Signal

For the STOP to be issued, the SST should trigger on the analog input signal. The trigger block shown in figure 2.34 detects events of interest by comparing the analog input with predefined voltage threshold values. The trigger circuitry is active during the acquisition phase and disabled during the readout phase. Additionally, the trigger circuit has to be configured for the normal operation of the SST - five control signals are employed to control the trigger logic. The trigger configuration pins are passive, and are not required to be

modified during the normal acquisition phase. The five trigger configuration pins are: Enable (STOP), Delay control 1, Delay control 2, AND/OR Select and Differential/Single Ended Select. Other than these five configuration pins, two DC threshold input signals per channel are also required by the trigger logic's comparators. The two threshold voltages V_{th_high} and V_{th_low} are connected to the two comparators. The comparator to which V_{th_high} is connected, drives V_{DD} when the analog input goes above the threshold value. Similarly, the comparator to which V_{th_low} is connected, drives V_{DD} when the analog signal goes below the threshold value.

The trigger configuration pin "Differential/Single-Ended Select" (Diff/Single) is used to select trigger output structure. The SST's trigger outputs are set to Differential ended when the "Diff/Single" pin is high, otherwise they are single ended. During the single ended mode of operation, the configurations pins Delay control 2, AND/OR select are don't care. The trigger output of the SST will be the pulse stretched version of the comparator outputs. The amount of pulse stretching is defined by the Delay control 1 pin. The Delay Control 1 is also referred to as L1 delay in this dissertation, L1 as in *level 1* delay. Similarly Delay Control 2 pin is commonly referred to as L2 delay, as in *level 2* delay. In the differential mode of operation, the trigger outputs are complementary and additional AND/OR logic is applied to the comparator outputs. The logic value of the configuration pin AND/OR select dictates the type of logic operation performed on the comparator outputs. The final trigger is asserted when both V_{th_high} and V_{th_low} threshold voltages are crossed by the analog input signal within a specific period of time. This specific period of time is defined by the L1 delay control pin. The AND logic mode is effective to detect bipolar pulses. OR logic which is akin to the AND logic is selected when the AND/OR pin is set to logic low. The OR logic is effective in detecting unipolar pulses where the analog signal crosses either V_{th_high} or V_{th_low} threshold voltages. During the differential mode of operation, the SST's trigger outputs are the pulse stretched versions of the AND/OR logic blocks. The amount of pulse stretching is determined by the L2 delay control pin.

2.2.1.2 Readout Phase

The assertion of trigger out is an indication that an interesting analog signal has been captured. Once the SST's peripherals see the trigger out signal, the STOP is asserted. Assertion of STOP signal essentially halts the acquisition phase and begins the readout phase. The readout phase is recovery of the analog waveform captured during the acquisition phase. The timing diagram of the readout phase is shown in figure 2.4.

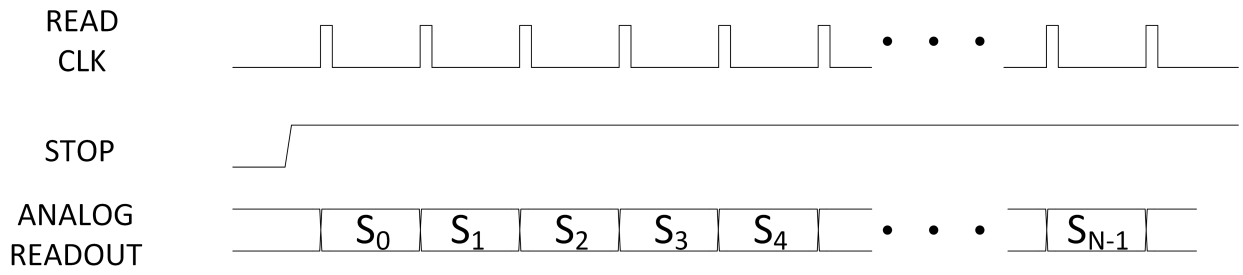


Figure 2.4: Synchronous Sampling and Triggering Readout Phase

During the acquisition phase, the sampled transient waveform is stored on the 80fF MIM capacitor. Since the analog waveform is stored on a MIM capacitor, the stored waveform should be readout prior to the corruption cased by the non-zero leakage currents. Lowest frequency, that the SST's sampled waveform can be readout without losing one least significant bit in the dynamic range is 243.9 Hz. During the normal operation, the SST is readout at 1 MHz. This 1 MHz of readout frequency is chosen so that it's compatible to the TI 12-bit 1MSPS ADC. The SST can support up to 5 MHz of readout frequency.

In addition to reading out the analog waveform captured during the acquisition phase, the SST chip also reads stop-out. Stop-out data is essentially the sampling clock pointer read out in a sequential manner. As the analog samples are being read out, stop-out pin will readout the corresponding sampling clock logic level in parallel. As shown in figure 2.3, the sampling clock logic level (ψ_{N-1} and ψ_N) will be high for the beginning/end of the analog transient signal and low for rest of the samples(ψ_1, ψ_2 etc.). The position of the beginning/end of

the analog transient signal is random relative to the start. Insight into the beginning/end position remains very important in order to delineate the transient signal.

2.3 Low Voltage Differential Signaling Circuit

The SST is capable at operating at sampling speeds ranging from 2 kHz to 2 GHz. An external clock ranging from 1 KHz to 1 GHz should be applied to the SST to achieve these sampling speeds. There are many crystals available in the market which generate the required clock signals. For Arianna we use an external LVDS oscillator with low jitter (e.g., Fox "XpressO Ultra" oscillators).

The external clock upon entering the SST chip interacts with the LVDS receiver circuit. The circuit transforms the low-voltage differential clock signal to differential CMOS signal.

The design details of the LVDS receiver circuit will not be discussed in this dissertation, only a brief overview of the receiver circuit will be discussed.

The LVDS receiver shown in figure 2.5 is designed by Edwin Cheim and the design details can be found in his dissertation [19]. The circuit can function for input clock frequencies up to 1.4 GHz for the common mode range varying from 0.9 V to 1.5 V. Ideally the input signals can be 350 mVpp for the best operating scenario.

The cross-coupled PMOS transistor pair provides negative resistance which is equivalent to the load resistance, a sufficient voltage gain is achieved by this process. The bias currents are required to be high (around 75 μA) to achieve high speeds of operation.

The input to the LVDS receiver is a differential 1 GHz clock signal with 350 mVpp (single ended) and with rise and fall times of $\approx$400ps. The LVDS receiver circuit converts the LVDS

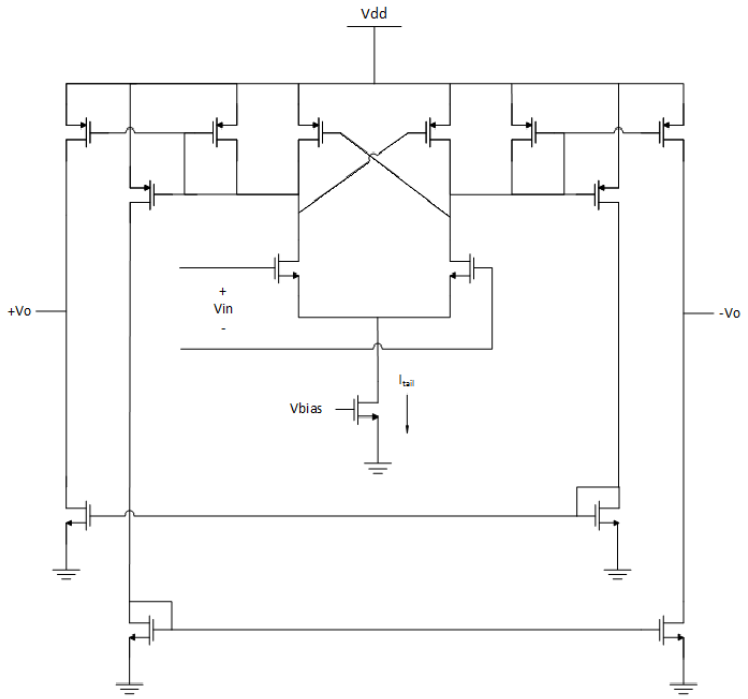


Figure 2.5: Low voltage differential signaling circuit schematic [2]

input to full 0 V to 2.5 V CMOS logic clock signal.

2.4 Clock Synchronizer

One of the primary advantages of the SST is the ability to start, stop and synchronize immediately with nano-second precision. This ability of the SST can be achieved by synchronizing the external STOP signal with the clock. The clock synchronizer circuit reduces the probability for failure by minimizing the effects of metastability.

Metastability is an inherent phenomenon of any clocked digital logic circuits. Any CMOS device, also dubbed as bistable device will have two stable states. A third state known as the metastability is also present. When a device enters a metastability state, it will stay there for an undetermined time and eventually transition to one of the stable states.

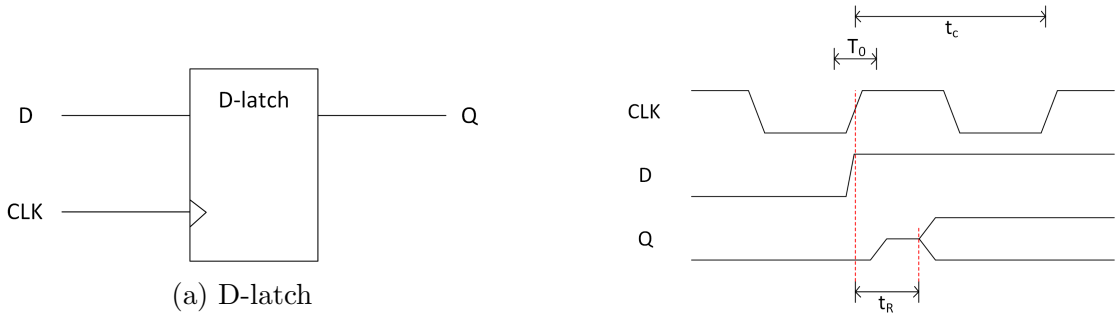
[2]The schematic originally published in [19]

Flip-flops and latches can enter metastability conditions when the triggering conditions such as input setup time and input hold times are violated. Although metastability cannot be completely eliminated, the effects and probability of failure by isolating the asynchronous inputs by using a synchronizer circuit can be minimized.

The synchronizer circuit in the SST conditions the external STOP signal into a known relationship with the input clock signal.

Before examining the design details of the synchronizer circuit a review of the mathematical analysis of metastable behavior would be beneficial.

In order to elucidate the metastable behavior, an insight into certain behaviors would be practical. First, how often does the metastability occur? And once the metastability occur, how long does it last?



(a) D-latch

(b) D-latch Waveform

Figure 2.6: Metastability

In the figure 2.6 consider the D-latch. The probability of failure is the product of the probability of entering the metastable state and the probability that the metastable state still persist till time t_R

$$P_{(\text{of failure})} = P_{(\text{entering metastability})} \times P_{(\text{still in metastable state after tR})} \tag{2.1}$$

$$P_f = P_E \times P_S \tag{2.2}$$

In order to calculate the probability, one needs to first discern the probability of entering the metastability. From figure 2.6 we define a short window T_0 around the clock rising edge. The latch will become metastable when the input changes during this window.

Since the input 'D' can arrive anytime during the clock period (t_C), the probability of entering is nothing but the probability of input 'D' arriving during T_0.

$$P_E = \frac{T_0}{t_C} \tag{2.3}$$

$$P_E = f_C \times T_0 \tag{2.4}$$

f_C is the clock frequency.

Next, calculation of the probability that the latch will remain in metastable state for t_R is required. Since the metastable condition occurs only during the liner operating region of the gates, the initial voltage difference in the gate will be exponentially amplified by the gain of the gates. If the latch is in metastable condition at time 0, then the probability of metastability after t_R is

$$P_S = e^{\frac{-t_R}{\tau}} \tag{2.5}$$

The time constant τ is the inverse of the gain of the gates and t_R is the resolution time. We have,

$$P_F = P_E \times P_S = f_C \times T_0 \times e^{\frac{-t_R}{\tau}} \tag{2.6}$$

If we assume that our input 'D' is changing at frequency f_d then the failure rate λ is the input frequency times the probability of failure for single input transition.

$$\lambda = f_d \times P_F = f_d \times f_c \times T_0 \times e^{\frac{-t_R}{\tau}} \tag{2.7}$$

The Mean time between failures (MTBF) is defined as the inverse of the failure rate.

$$MTBF = \frac{1}{\lambda} = \frac{e^{\frac{t_R}{\tau}}}{f_d \times f_c \times T_0} \tag{2.8}$$

2.4.1 Design and Analysis

The Synchronizer circuit designed for the SST is shown in the figure 2.7. In the bottom half of the figure, the external stop signal is being synchronized with respect to the clock signal. The output of the flip-flop is "syncstop" signal. This "syncstop" signal which is the synchronized stop is in-turn used to block/allow the clock signal for the SST.

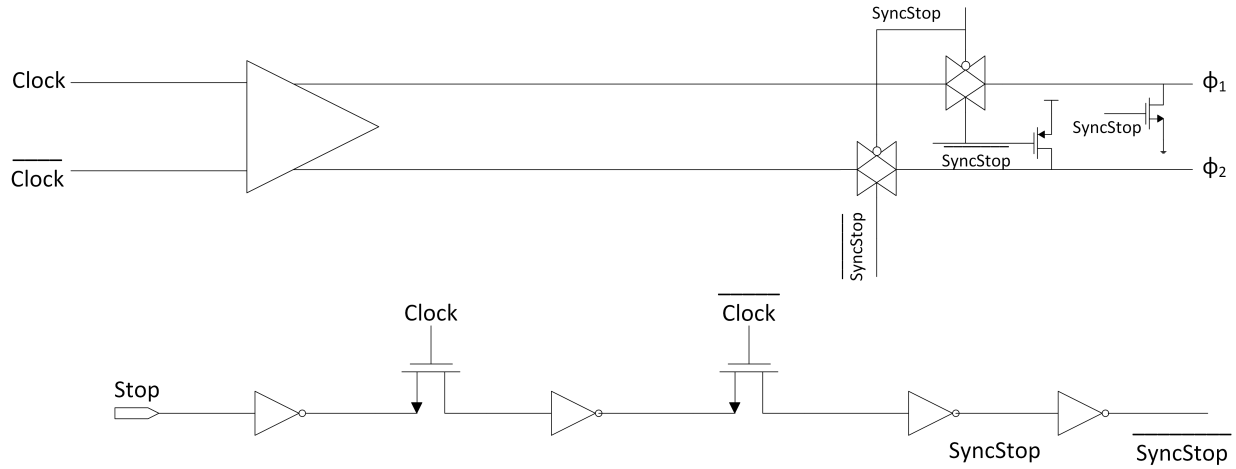


Figure 2.7: Synchronization Circuit

A conscious choice was made to design a single edge synchronization circuit. The reason for this choice will be discussed at the end of this section.

Here dynamic edge triggered flip-flop is utilized. This circuit has two bistable devices master

latch and slave latch. The master latch samples the STOP at the rising edge of the clock and the slave latch samples the output of the master at the falling edge of the *clock* (rising edge of $\overline{clock}$). There is a possibility that each of these latch can go into metastability. Here the resolution time of each latch is half the clock period. An analysis of the structure and the appearance of MTBF would be constructive.

Since there are two latches and the resolution of each latch is half the clock period, there are two time constants and two metastability windows. The two time constants are τ_M (time constant of the master latch) and τ_S (time constant of the slave latch). The two metastability windows are T_{0m} (metastability window for master latch) and T_{0s} (metastability window for slave latch). The propagation delay between the latches needs to be considered.

It's necessary to understand that the metastability of the master latch is irrelevant. However it matters whether the slave latch is metastable since it drives the output "syncstop". The metastability of the master latch can propagate to the slave latch during the first half of the clock period. If the master latch resolves the output during the rising edge of the $\overline{clock}$ then this transition can induce metastability in slave latch.

The overall MTSB of the flip-flop will be typically:

$$MTBF = \frac{1}{\lambda} = \frac{e^{\frac{t_R}{\tau}}}{f_d \times f_c \times T_0} \tag{2.9}$$

The parameters for τ and T_0 vary slightly for the latches. There is a possibility of another phenomenon called the clock back edge effect [34] discussed by Kinniment which can cause a significant increase in rate of failure during the second half of the clock period due to propagation delay between two latches. The duty cycle of the clock has an effect for metastabilty of the slave latch [53]. For example if the high low ratio is 4: 1 then the master latch has 4× more time to resolution.

The circuit is a rising edge clock synchronization circuit. A conscious choice was made to avoid dual edge synchronizer. SST uses an external oscillator to provide the clock to the circuit, due to this inherent feature, duty cycle of the input clock cannot be controlled. Let's consider a hypothetical situation, where the duty cycle of the external oscillator is $\neq 50\%$. For the circuits like SST with single edge synchronization, this duty cycle will appear as a fixed offset and can be calibrated out post data acquisition. However, in a dual-edge synchronization system, there is no way of knowing whether "odd" or "even" edge was chosen for synchronization, as this will be chosen randomly in an asynchronously triggered system. Therefore, calibration for the dual-edge synchronization system is nearly impossible. Under most circumstances, dual-edge synchronous systems require a perfect 50%-50% duty cycle or risk the non-uniformity in the sample interval appearing to be random noise that cannot be calibrated out. Calibrating out the duty cycle of the oscillator is possible by measuring it with the oscilloscope, but the scope's ability to detect $\sim 50ps$ differences at 1 GHz of speeds is limited. Therefore to avoid all additional complications, single edge triggered synchronization circuit was designed.

The layout of the synchronizer circuit used in SST is shown in the figure 2.8. The inputs are applied to *clock* and $\overline{clock}$ pins. The asynchronous stop is applied the flip-flop. The output clocks are synchronous to the stop signals. In order to reduce the effects of mismatch the layout of the synchronizer is symmetrical as this reduces the effects of mismatch.

2.5 Two-Phase Non-Overlapping Clock Generator Circuit

The SST's sampling clocks are generated by high speed fast shift registers containing a single '1' as a pointer to the sample and hold circuitry. These dynamic shift registers contain 128

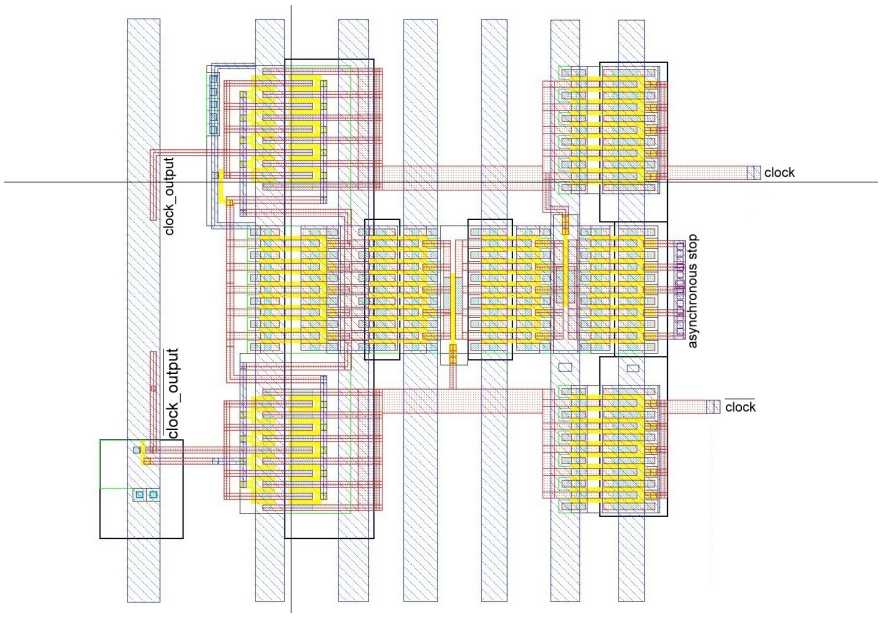


Figure 2.8: Layout of Synchronization Circuit - Symmetry Maintained

master-slave flip-flops which are configured in a circular fashion need a very reliable robust clocking. For sampling circuits such as SST, a very clean timing reference is of utmost importance.

A very precise timing information is needed to reconstruct an analog signal along with the amplitude information. The dynamic shift registers used in the SST need 2-phase non-overlapping clocks to generate sampling clocks. The non-overlapping clocks should be designed in such a way that problems such as insufficient duty-cycle and clock-skew must be avoided.

The SST's fast shift registers use N-MOS pass transistor logic, therefore only 2 phases of clock is more than sufficient to generate stable sampling clocks.

The two phase clocking system used in switch-capacitor circuits must have sufficient duty-cycle for each clock phase so as to give enough time for the capacitors to charge. Further, there should not be any overlapping to avoid charge sharing between adjacent capacitors.

2.5.1 Design and Analysis

A NAND-based non-overlapping clock generation circuit was designed for SST. Both NOR-based clock generation circuit and NAND-based clock generation circuit were analyzed and simulated. Figure 2.9 shows the conceptual diagram of NAND-based clock generation circuit and NOR-based clock generation circuit.

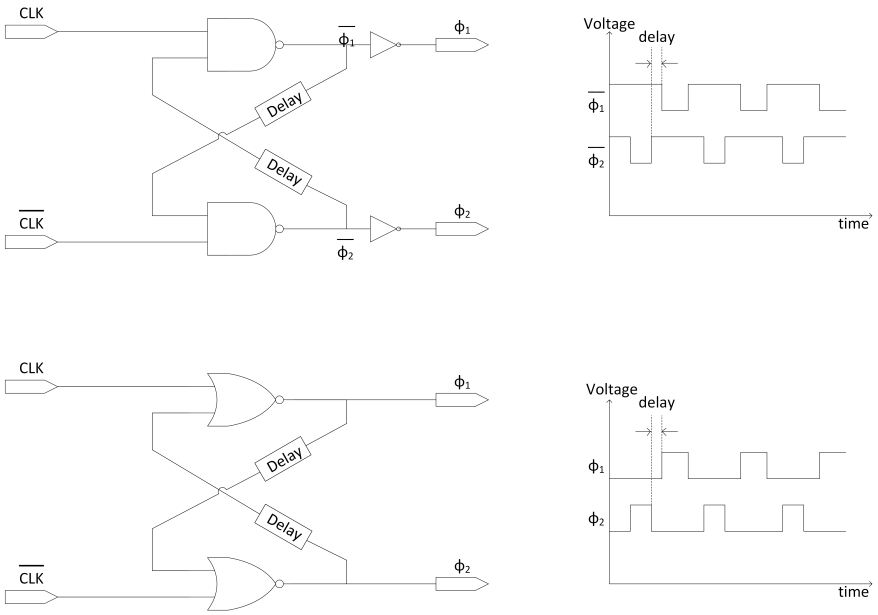
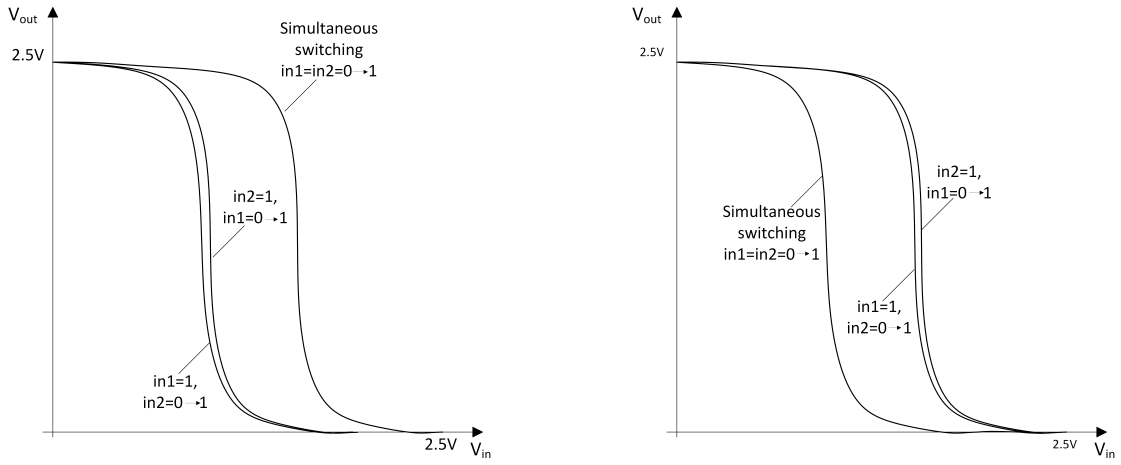


Figure 2.9: Conceptual Circuit

The DC characteristics of both NAND gate and NOR gate depend on the input combinations. Figure 2.10 illustrates the VTC curve for both NAND gate and NOR gate. The differences in the curves are due to the electrical structuring of the gates, i.e., additional node between NMOS in the case of NAND and PMOS in the case of NOR gate.

The case where the inputs of the NAND gates and NOT gates switch simultaneously is distinct. The NAND gate ($V_{M_{NAND}}$) and NOR gate ($V_{M_{NOR}}$) threshold voltages for this case are defined by the point where the voltage transfer curve intersects the unity gain line. The threshold voltages are useful parameters that characterize the entire VTC curve.



(a) 3 Cases of NAND Gate VTC Curve (b) 3 Cases of NOR Gate VTC Curve

Figure 2.10: VTC Curve: NAND and NOR Gate

For the NAND gate, the threshold voltage when both inputs switch simultaneously is given by [46]

$$V_{M_{NAND}} = \frac{V_{DD} - |V_{Thp}| + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}V_{Thn}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}} \tag{2.10}$$

Comparing the threshold voltage of an inverter given in equation 2.38 and the threshold voltage of an NAND gate given in equation 2.10, we can see the difference is the factor of half multiplying the square root term. For example, if we construct the inverter and an NAND gate with same $\left(\frac{W}{L}\right)$ ratios, the value of $V_{M_{NAND}}$ is going to be larger than $V_{M_{Inverter}}$. This is due to the series NMOS transistors and the combined increase in resistance from output to ground. The threshold voltages for two other cases where in1=1 and in2 switches and in2=1 and in1 switches can be easily calculated. The separation of the curves of these two cases shown in figure 2.10a is due to the stacking order of the NMOS transistors and body-bias effects between the two NMOS transistors.

For the NOR gate, the threshold voltage when both inputs switch simultaneously is given by [46]

$$V_{M_{NOR}} = \frac{V_{DD} - |V_{Thp}| + 2\sqrt{\frac{\beta_n}{\beta_p}}V_{Thn}}{1 + 2\sqrt{\frac{\beta_n}{\beta_p}}} \tag{2.11}$$

Similar to NAND gate analysis, comparing the inverter threshold voltage given in equation 2.38 and equation 2.11, the difference is the multiplying factor of 2 at the square root term.

Both NAND gates and NOR gates can be easily implemented, for similar device sizes and equal number of inputs, NAND gates have better transient response than NOR gates, thus enabling them to be the gate for choice for SST's clock generator design. The rationale behind this conclusion can be verified by comparing the delay times. In both NAND gates and NOR gates the series connected transistors are the limiting factor. In NAND gate, the discharge delay time is determined by a series combination of NMOS transistors. The discharge delay time is given by

$$\tau_n = (R_{n_{in1}} + R_{n_{in2}})C_L + R_{n_{in1}}C_{seriesnode} \tag{2.12}$$

where, $R_{n_{in1}}$ and $R_{n_{in2}}$ are equivalent NMOS resistances, $C_{seriesnode}$ represents the internal node capacitance between the two series NMOS transistors, and C_L is the output capacitance. In NOR gate, the charging delay time is the bottle neck and is determined by the series combination of PMOS transistors. The charging delay time is given by

$$\tau_p = (R_{p_{in1}} + R_{p_{in2}})C_L + R_{p_{in2}}C_{seriesnode} \tag{2.13}$$

where, $R_{p_{in1}}$ and $R_{p_{in2}}$ are equivalent PMOS resistances, $C_{seriesnode}$ represents the internal node capacitance between the two series PMOS transistors, and C_L is the output capacitance.

In general, the resistance transistors is given by

$$R = \frac{1}{k' \left(\frac{W}{L}\right) (V_{DD} - V_{Th})} \tag{2.14}$$

where $\frac{k'_n}{k'_p} > 1$. Similar sizes of NMOS and PMOS will yield $R_p > R_n$. Series NMOS chain

can always discharge faster than a series PMOS chain can charge.

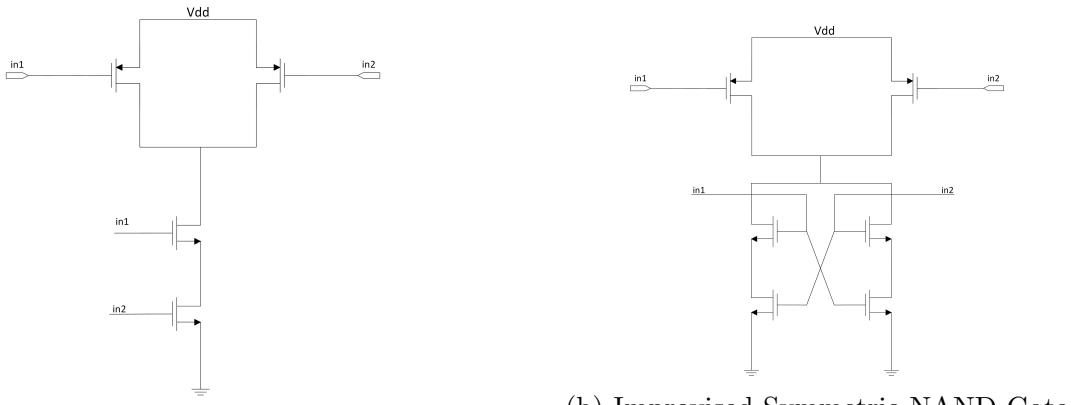
After comparing the performances of both designs, NAND-based design has better jitter characteristics compared to NOR-based design. The larger size of the NMOS transistor in NAND-based design explains this performance advantage. To achieve similar performances, the PMOS in the NOR-based design has to be at least four times larger in order to compensate for this disadvantage. The additional power and area consumption can be avoided by choosing the NAND-based design.

The decision to choose NAND-based design was also made partly based on the work done by A. Stark and H. Tenhunen [52]. The work analyses power-supply noise induced timing variations in NAND and NOR logical blocks. The work focuses on NAND and NOR blocks used in non-overlapping clock generation circuits used for switched capacitor sigma-delta analog-digital converters. A. Startk and H. Tenhunen [52] present the following conclusions, NAND-based non-overlapping circuit is less sensitive to power supply noise in terms of timing jitter. Power supply noise was induced and the timing jitter between NAND and NOR blocks were measured. The NAND blocks consistently showed better jitter performances compared to NOR block.

2.5.1.1 NAND-Based 2-phase Non-Overlapping Clock Generator Circuit

Figure 2.9 shows two types of design choices, a NAND-based clock generation circuit was used for the SST. An improvised version of the NAND gate was used to design the NAND-based clock generation circuit. Figure 2.11a shows a typical NAND gate structure and figure 2.11b shows an improvised version on the NAND gate used in the SSTs clock generation circuit.

In the figure 2.11b the improvised version of the NAND gate is shown. Here addition of two more NMOS transistors in parallel to the existing transistors and cross-coupling the gates,



(a) Standard NAND Gate

(b) Improvised Symmetric NAND Gate

Figure 2.11: NAND Gate Structure

can ensure that the outputs are matched with respect to the inputs. The output waveform is symmetric.

In the figure 2.11b we can determine that the pull-up circuitry is same in the typical and improvised circuit. The rise time of the standard and the improvised NAND gate will be same. Both the circuits have the same time constants. However, for the pull-down circuitry the fall time of the improvised circuit is approximately half the time constant of the standard circuit. This is due to the shortened time constant.

The improvised NAND gate is inherently faster compared to the standard circuit. Although, the rise time of both the circuits are same, the fall time of the improvised circuit is half compared to the fall time of the standard circuit.

Moreover, an important factor to consider is the selection of delay for the NAND-based non-overlapping clock generator circuit. For switch-capacitor circuits such as SST, the two phase clocking systems must have sufficient duty-cycle for each clock phase so as to give enough time for the capacitors to charge. The figure 2.12 shows the circuit used in the SST. To achieve the maximum duty-cycle possible the delay should be minimum. The 2-phase clock generation circuit used in the SST was designed without the delay lines.

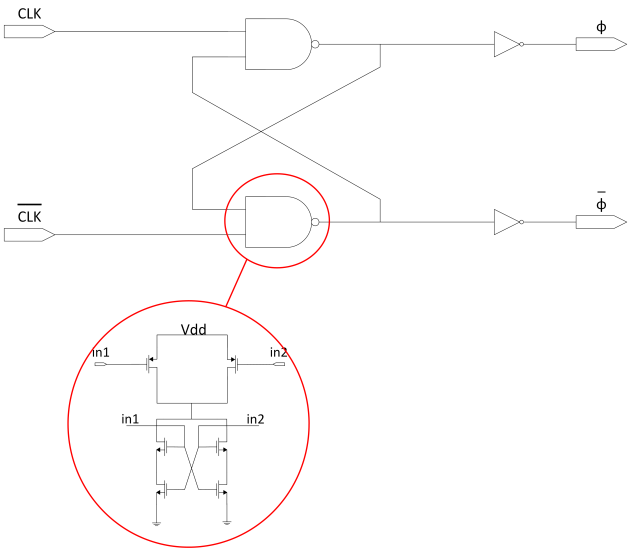


Figure 2.12: 2-Phase Non-Overlapping Clock Generator Circuit

The non-overlapping period of the clock phases is guaranteed to avoid the charge sharing between capacitors. The duty-cycle is designed to be as high as possible to ensure sufficient time is provided for the capacitors to charge. The layout of the 2-phase non-overlapping clock generation circuit is shown in the figure 2.13. The layout of the circuit is designed to be very symmetric so as to keep both phases of the clock signal symmetric. The output clocks of the synchronization circuit is applied to the *clock* and $\overline{clock}$. The non-overlapping clocks appear at phi-1 and phi-2.

2.6 Clock Distribution Network

A reliable clock is required by the SST to generate a high speed sampling clock. An off chip LVDS oscillator feeds a clock signal into an LVDS receiver which feeds into a 2-phase clock generator, the output of the 2-phase clock generator drives a clock distribution buffer tree network in a uniform and jitter free form to 128 flip-flops which in-turn generates the sampling clock.

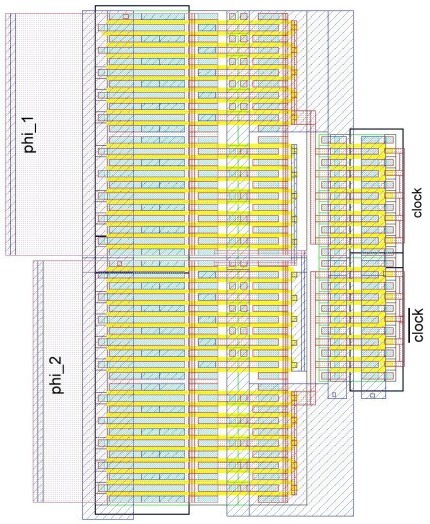


Figure 2.13: 2-Phase Non-Overlapping Clock Generator Circuit Layout

In synchronous systems, the clock signal is used to define the time reference for the movement of the "pointer" for the sampling circuitry. Since this function is vital to the operation of the chip, significant attention is given to the characteristics of this clock signal and the network used in its distribution.

These clock signals typically travel over longer distances and operate at higher speeds in comparison to any other signals within the system. These clock signals are more prone to technology scaling, for example the long interconnect lines will become more resistive as the line dimensions decreases. In addition to this, other variations such as manufacturing variations, temperature variation, and power supply noise will start affecting the high speed clock significantly. Most importantly these variations are very difficult to be modeled and in majority of cases no information about these variations are available during designing. For example, process variations in the ICs have become a major concern for the chip designers. If the process variations are not taken into account in the early design stages, final production yield will be low [16]. Similarly power variations are most common and significant, in particular for clock distribution networks. During data switching, the capacitors are charged by VDD and discharged by GND networks, during these charging and discharging cycles

current flows through power-supply lines. Since these lines have finite resistances, voltages drop and/or rise [49]. A small variation may generate unwanted skew which will affect the performance of the entire chip. A variation aware design methodology should be employed so that the circuits work reliably during the presence of variations. Variability aware optimization is one such technique which can be employed to design novel optimization methods which make circuits more tolerant to variation.

2.6.1 Clock Skew

Synchronous system consist of globally clocked registers and few combinational elements. For an arbitrary pair of registers one of the following two situations can be observed.

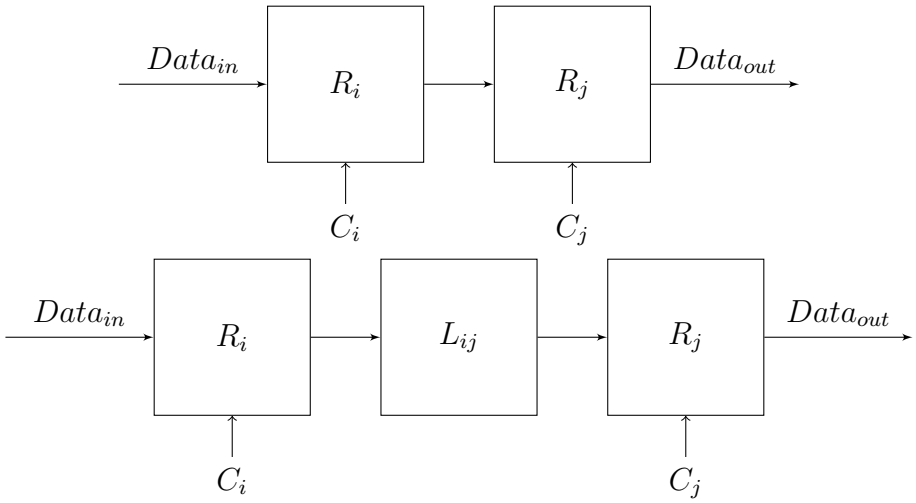


Figure 2.14: Data Path

As illustrated in the figure 2.14, the input of R_j is directly connected to output of R_i or the output of R_i is connected to input of R_j though a sequence of logic blocks. In the latter case the minimum allowable cock period $T_{cp}(min)$ between two registers in a sequential data path is given by

$$T_{cp}(min) \geq T_{c-q} + T_{logic} + T_{hold} + T_{set-up} + T_{skew} \tag{2.15}$$

This requirement ensures that the register latches the correct data to the output. To minimize the clock skew the time T_{skew} must be

$$T_{skew} \leq T_{cp}(min) - T_{pd}(max) \tag{2.16}$$

where the total path delay is the sum of the maximum time required for the data to leave the initial register once the clock signal C_i arrives, T_{C-Q}, the time necessary to propagate through the logic and interconnect $T_{logic} + T_{int}$

$$T_{pd}(max) = T_{logic} + T_{c-q} + T_{int} \tag{2.17}$$

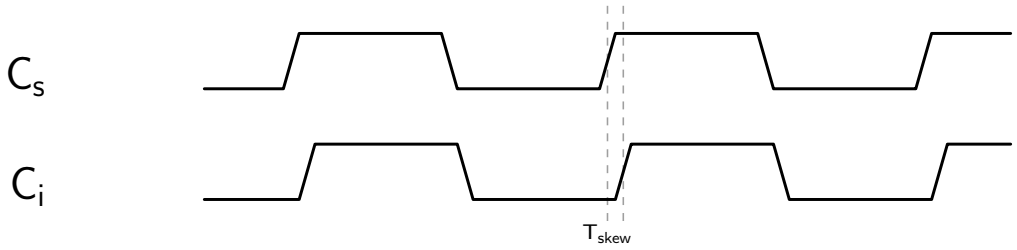
The difference in the clock signal arrival time between two sequentially adjacent registers is clock skew T_{skew}. Ideally for a complete synchronous circuit the clock skew should be zero. This is possible if the clock signals C_i and C_j arrive at their respective registers at exactly the same time.

For example T_{s-i} assumed to be the propagation delay from source to register i, and T_{s-j} is the propagation delay from source to register j. The clock skew between registers i and j can be given as:

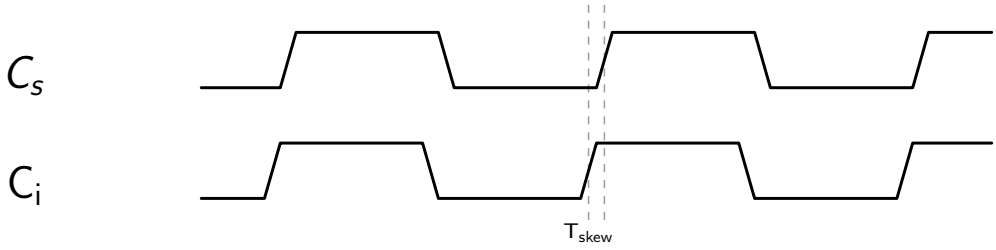
$$T_{skewij}(max) = T_{s-i} - T_{s-j} \tag{2.18}$$

The clock skew T_{skew} can be positive or negative depending on weather C_i leads or lags C_s respectively.

From equation 2.15, clock skew has as much on an impact on overall speed of the circuit as any other effect such as propagation delay. In typical circuits, there are far fewer clock lines than data lines, therefore for big improvements in timings, designing great clocks distribution lines are the key.



(a) Positive Skew



(b) Negative Skew

Figure 2.15: Clock Skew

2.6.2 Low-Impedance Drivers and Clock Distribution Lines

Designing low impedance drivers is one of the best method to achieve low skew. Low clock skew is achieved via the close congregation of all clock inputs and then by driving them from the same source. One method that has been tried and tested is to promote spider distribution network and transmission lines with low impedance as this distributes a clock from single source to N remote destinations. The reflections can be damped by termination resistors R at the end of each spider distribution network. This type of spider distribution network will experience a total load of $\frac{R}{N}$. A common method is to use discrete low impedance amplifier circuit to drive various spider legs within a network.

Employment of clock distribution tree, trades quality over power. This tree scheme distributes clocks through a tree network to the final destination. A balanced-buffered tree network with equal number of identical gates assists in the reduction of clock skew. The clock line in figure 2.16 has many fan-outs. As the clock signal passes through each inputs, the load increases and a small reflected pulse propagates backward along the line. This reflected pulse interfere with reception.

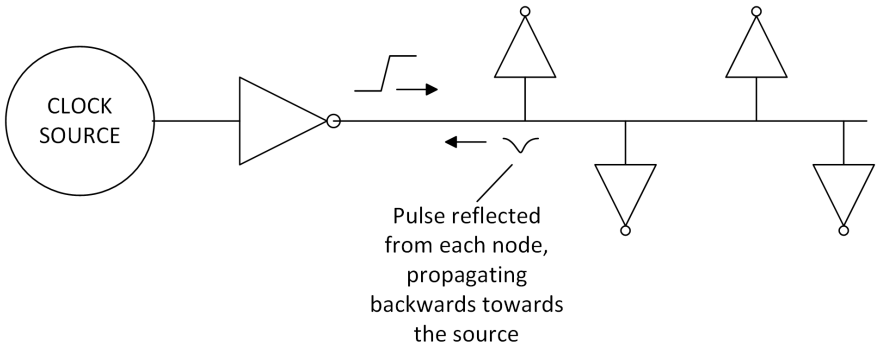


Figure 2.16: Clock Driver with Many Loads

The fraction of the propagated signal that reflects back towards the source is known as the far-end reflection function. Assuming a low loss line, the reflection coefficient ($R_{C\_REF}(\omega)$) at a capacitive load is given by [7]

$$R_{C\_REF}(\omega) = \frac{-j\omega C Z_O}{2 + j\omega C Z_O} \tag{2.19}$$

Where C is the parallel combination of capacitance of the transmission line and Z_O is the high frequency impedance of the transmission line ($\sqrt{\frac{L}{C}}$). For frequencies above $f_{max} = (CZ_O\pi)^{-1}$ reflection is almost total, for frequencies below f_{max} the reflection coefficient differentiates. It effectively returns a pulse equal to the derivative of the in input step, i.e., the height of the reflected pulse is proportional to $(-C(\frac{Z_O}{2}))$. Some of the chief practices to reduce reflected pulse amplitude is to reduce capacitance at each node and to lower the characteristic impedance of the clock distribution lines. For example, a 20Ω clock line is approximately 2.5× less sensitive to the node capacitance than a 50Ω clock line is a good way to put this in perspective.

2.6.3 Crosstalk on Clock Lines

The cross talk between two conductors depends on their mutual inductance and their mutual capacitance. Typically in digital designs, inductive crosstalk is as big as or larger problem

than capacitive crosstalk. In the inductive coupling mechanism, the induced voltages are proportional to the derivative of the driving signal, they are worse for higher frequencies. Figure 2.17 shows the cross section of two traces showing cross talk.

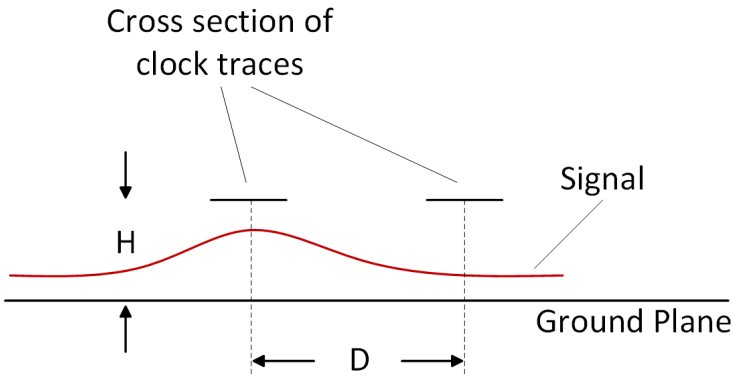


Figure 2.17: Cross Section of Two Traces Showing Crosstalk

The mutual inductive crosstalk drops off as the clock lines move away from each other. The crosstalk can be expressed as a ratio of measured noise voltage to the driving step size.

$$Crosstalk \approx \frac{K}{1 + \left(\frac{D}{H}\right)^2} \tag{2.20}$$

The constant K depends on the frequency and the interfering trace length, the value of K is always < 1 [18]. In general doubling the trace separation divides the crosstalk by 4. Since the clock signals are extremely vital and delicate, extra crosstalk protection should be implemented. The best means of providing crosstalk protection is to physically laying out the traces by leaving extra gaps or to have clock signals on separate layers encapsulated between ground planes. For the SST design, to enforce additional spacing for crosstalk protection, guard traces were inserted during layout design and these guard traces were removed last minute. The temporary implementation of guard traces forced other traces to be distanced from the high speed clock lines during routing so as to ensure crosstalk protection.

2.6.4 Design and Analysis

Clock distribution networks are more susceptible to clock skews. The different clock signal paths can have varying delays for different reasons. Wann and Franklin [55] present few cases of clock skew in clock distribution networks.

- The difference in the wire lengths from the clock source to the different registers.
- The difference in transistor sizing of distributed buffers along the clock network path.
- Difference in passive interconnects parameters such as line resistivity, dielectric constants and thickness, via/contact resistance, fringe capacitances and line/wire dimensions.
- Variations in active device parameters such as MOS threshold voltages and channel mobility which affects the delay of switching buffers.

It should also be noted that for a well-designed and balanced clock distribution network. The distributed clock buffers are the principal sources of clock skew. The structural topology of the clock distribution networks should be carefully developed to tightly control the variations of clock skew.

Numerous clock routing techniques have been proposed to reduce the variations of clock skew. Such clock distribution networks include buffered clock distribution network, H-tree distribution network, X-tree distribution network, and mesh type clock distribution network

The most common clock distribution strategy is to insert buffers at the source and along the clock path forming a tree structure. More often utilization of a mesh version [48, 42] of the clock tree structure is used. This mesh structure effectively places the branch resistance in parallel, minimizing the clock skew. Although clock meshes are effective in reducing

clock skew variations, they have larger area and power overheads compared to buffered clock distribution networks.

A hybrid network was used to design SSTs clock distribution circuitry. A combination of buffered tree structure and a mesh structure was adapted to design the clock distribution circuitry. Structures like this have been proposed before [47, 54] as an alternative to reduce clock skew variability. The works of [47] attempts to resolve this issue by inserting links to a buffered clock tree structure. In these works the links are placed closer to the sinks [47], the algorithm restrains the selection of nodes pairs to be sink nodes. As the number of levels increases in the clock distribution network, adding links only at the sinks may not be sufficient to reduce the variations of all levels. In our work, we insert links after each level between the internal nodes of the clock tree.

2.6.4.1 Qualitative Analysis

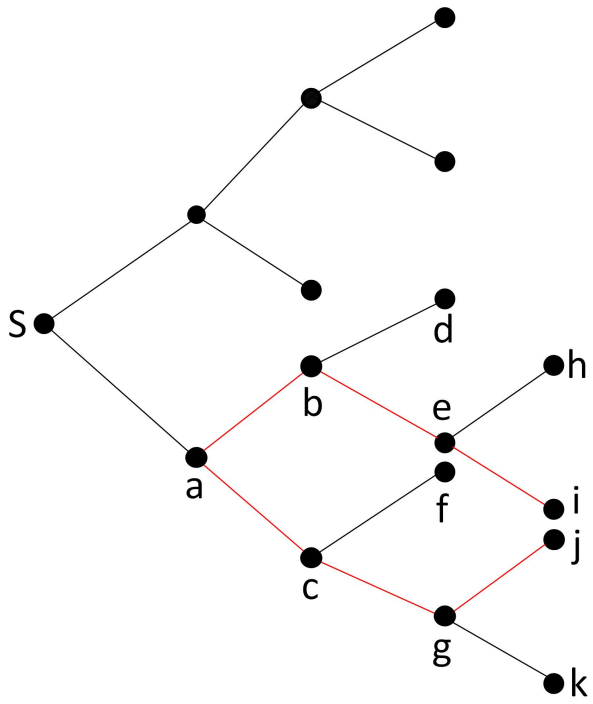


Figure 2.18: Link Insertion

A review if the link insertion proposed by Rajaram [47] will prove beneficial. Consider a tree $T_S = (V, E_T)$ where i and j are the vertices shown in Figure 2.18. The vertex a is the nearest common ancestor of nodes i and j. If a link l is inserted between the nodes i and j as shown in the figure 2.18 the skew between i and j after the link is given by

$$\hat{q_{i,j}} = \frac{R_l}{R_l + r_i - r_j}\left(q_{i,j} + \frac{C_l}{2}(R_{i,i} - R_{j,j})\right) \tag{2.21}$$

$$t_{pd} = \sum_i R_{iS} C_i \tag{2.22}$$

$$\hat{q}_{u,v} = \frac{R_l}{R_l + r_u - r_v}\left(q_{u,v} + \frac{C_l}{2}(R_{u,u} - R_{v,v})\right) \tag{2.23}$$

$$\hat{q}_{u,v} = \frac{R_l}{R_l + r_u - r_v} q_{u,v} \tag{2.24}$$

where $\hat{q_{i,j}}$ is the final skew after the link insertion between the nodes i and j; $q_{i,j}$ is the original skew before the link insertion; R_l the link resistance; C_l the link capacitance; $R_{i,i}$ and $R_{j,j}$ are the sums of the resistances along the paths from the source (node a) to the nodes i and j, respectively; r_i and r_j are equal to Elmore delays at i and j when the node capacitances of i and j are 1 and 1, respectively, and all the other node capacitances are set to zero.

$R_l + r_i - r_j$ is the total resistance along the loop $a \rightsquigarrow i \rightsquigarrow j \rightsquigarrow a$. According to the above equation the skew is smaller if the ratio $\frac{R_l}{R_l + r_i - r_j}$ is smaller. In our work, to satisfy this equation links are inserted at the beginning of the inverters of the clock tree.

In the Figure 2.18 the nearest common ancestor for nodes i and j is a node which has the

depth of 3. Let's call this depth as the level of the node pair and denote it as α. In order to get a relatively low variation results, α needs to be minimum. In our design α is chosen to be 1. Figure 2.19 shows the overall clock distribution network employed in SST.

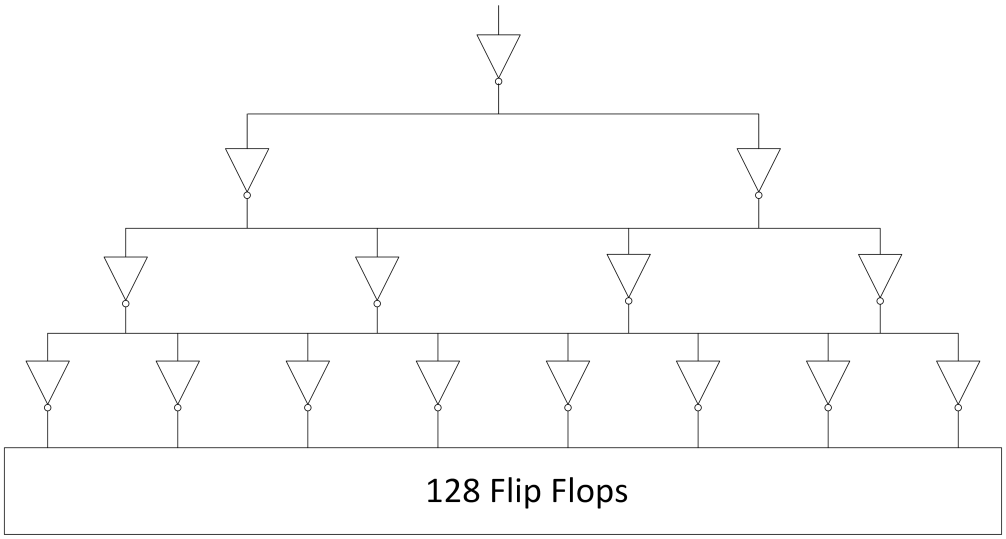


Figure 2.19: Clock Distribution Network

2.6.4.2 Buffer Design

The buffer is one of the most important component of the tree based clock distribution design. The buffer circuit is essentially a series of two inverters. The inverter is the nucleus of all digital designs.

The switch model is the simplest way to understand the operation of the inverter: the transistor is essentially a switch with an infinite OFF resistance and a finite ON resistance when gate voltage is less than the threshold voltage and when the gate voltage is greater than the threshold voltage respectively. This property of the transistor will lead to the following interpretation of the inverter. When input is high the NMOS is ON while the PMOS is OFF, a direct path exist between the output and ground, which results in a steady state value of 0V. Conversely when the input is low the PMOS is ON whilst the NMOS is OFF, a path

exist between Vdd and output.

The DC input-output characteristics are shown graphically using the Voltage-Transfer Curve (figure 2.20). An ideal inverter should have a very narrow transition zone. A high gain during the switching when both PMOS and NMOS are in saturation region results in this transition zone. In this zone, even a minute change in the input voltage will result in a substantial output variation. The VTC curve shown in figure 2.20 is simply a plot of V_{out} as a function of V_{in}. Qualitatively, the sharpness of the transition is a measure of the performance of the inverter. For digital designs, the plot is good way to realize the range of voltages for logic 0 and logic 1. It is important to understand that the limits of logic 0 and logic 1 are different for inputs and outputs. The VTC gives a set of critical voltages for defining the input and output ranges. These critical voltages for input and output voltages are V_{IH}, V_{IL} and V_{OH}, V_{OL} respectively and V_M which is the inverter threshold voltage. All the critical voltages are analyzed below.

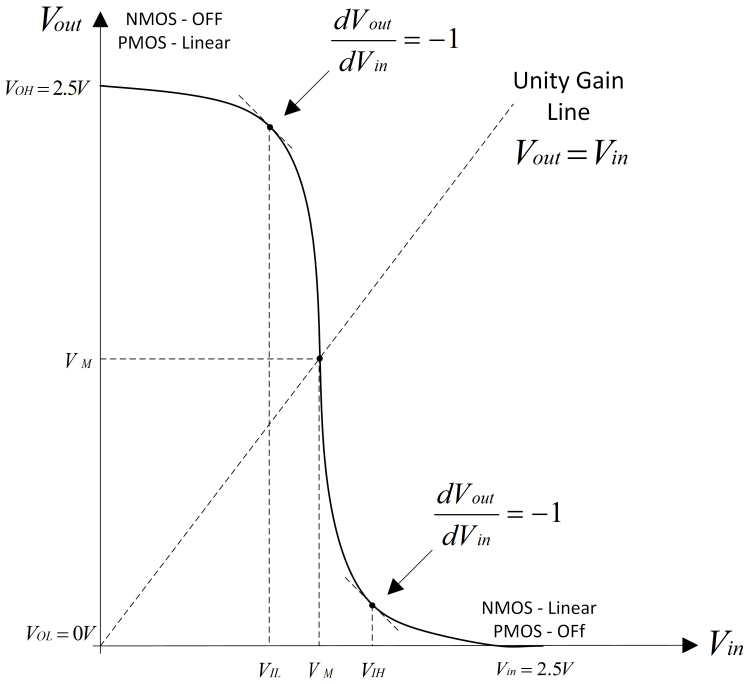


Figure 2.20: Voltage Transfer Curve of an Inverter

The critical voltages are established to characterize the DC response of the circuit. In the

digital CMOS circuit design, the designers can change only the aspect ratios of the devices: $(\frac{W}{L})_n$ and $(\frac{W}{L})_p$, other parameters such as V_{Th} and k' cannot be changes as they are the result of fabrication. The critical voltages are computed by setting the input voltages to the desired values and later equating the NMOS and PMOS drain currents.

Output-High Voltage (V_{OH})

Output-High voltage is the largest value of V_{out}, the V_{OH} can be calculated by applying an input voltage of $V_{in} < V_{Thn}$. V_{Thn} is the threshold voltage of the NMOS. The most simplified MOSFET equations give drain current ($I_{Dp} = 0$), and therefore the source-drain voltage is $V_{SDp} = 0$.

$$\begin{aligned} V_{out} &= V_{DD} - V_{SDp} \\ &= V_{DD} \\ &= V_{OH} \end{aligned} \tag{2.25}$$

Output-Low Voltage (V_{OL})

Output-Low voltage is the smallest value of V_{out}. The condition needed to calculate $V_{out} = V_{OL}$ is defined when the input value is set at $V_{in} = V_{DD} > (V_{DD} - |V_{Thp}|)$, i.e., PMOS is in the cutoff region. NMOS is biased active, drain current is 0 ($I_{Dn} = 0$), the drain-source voltage $V_{DSn} = 0V$. The output of the inverter is given by the following equation:

$$V_{out} = V_{DSn} = 0 = V_{OL} \tag{2.26}$$

Input-Low Voltage (V_{IL})

The Input-Low voltage V_{IL} represents the largest value of V_{in} that can be interpreted as logic 0. From the VTC curve in the figure 2.20 if the input voltage satisfies $V_{in} < V_{IL}$, the output voltage V_{out} is either V_{DD} or close to V_{DD}, indicating that the output is logic 1. V_{IL} can be defined as a point where the slope of the VTC curve has a value of -1, i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1 \tag{2.27}$$

At this mid point of the VTC curve, NMOS is saturated and PMOS is conducting. Equating I_{Dn} and I_{Dp} we get:

$$\frac{\beta_n}{2}(V_{in} - V_{Thn})^2 = \frac{\beta_p}{2}[2(V_{DD} - V_{in} - |V_{Thp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2] \tag{2.28}$$

where, $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right)$ and $\beta_p = \mu_p C_{ox}\left(\frac{W}{L}\right)$.

The derivative condition is applied by first writing the functional relationship

$$I_{Dn}V_{in} = I_{Dp}(V_{in}, V_{out}) \tag{2.29}$$

Taking differential on both sides and rearranging results in:

$$\frac{dV_{out}}{dV_{in}} = \frac{\frac{dI_{Dn}}{dV_{in}} - \frac{\partial I_{Dp}}{\partial V_{in}}}{\frac{\partial I_{Dp}}{\partial V_{out}}} = -1 \tag{2.30}$$

This shows that the derivative condition may be found using the equations for the current

flow. By substitution and calculation of the derivatives yields

$$V_{in}\left(1+\frac{\beta_n}{\beta_p}\right) = 2V_{out} - V_{DD} - |V_{Thp}| + \frac{\beta_n}{\beta_p}V_{Thn} \tag{2.31}$$

The value of $V_{in} = V_{IL}$ can be realized by solving equations 2.28 and 2.31.

Input-High Voltage (V_{IL})

The Input-High voltage V_{HL} represents the smallest value of V_{in} that can be interpreted as logic 1. From the VTC curve in the figure 2.20 if the input voltage satisfies $V_{in} \geq V_{IH}$, the output voltage V_{out} is either $0V$ or close to it's value. V_{IH} can be calculated by using current flow equations just like V_{IL}. Here, however, NMOS is conducting where as PMOS is saturated. Equating the currents gives:

$$\frac{\beta_n}{2}(V_{in} - V_{Thn})V_{out} - V_{out}^2 = \frac{\beta_p}{2}(V_{DD} - V_{in} - |V_{Thp}|)^2 \tag{2.32}$$

similar to V_{IL}, the functional relationship for this case is

$$I_{Dn}(V_{in}, V_{out}) = I_{Dp}V_{in} \tag{2.33}$$

Taking differential on both sides and rearranging to get slope requirement

$$\frac{dV_{out}}{dV_{in}} = \frac{\frac{dI_{Dp}}{dV_{in}} - \frac{\partial I_{Dn}}{\partial V_{in}}}{\frac{\partial I_{Dn}}{\partial V_{out}}} = -1 \tag{2.34}$$

Substituting the current equations and differentiating generates

$$V_{in}\left(1+\frac{\beta_p}{\beta_n}\right)=2V_{out}+V_{Thn}+\frac{\beta_p}{\beta_n}(V_{DD}-|V_{Thp}|) \tag{2.35}$$

Just like V_{IL} analysis, the value of $V_{in}=V_{IH}$ can be realized by solving equations 2.32 and 2.35.

Inverter Threshold (Midpoint) Voltage (V_M)

The voltage V_M in the figure 2.20 is the inverter threshold or rather midpoint voltage. V_M is defined as the point where the VTC curve intersects the unity gain line. Unity gain line is defined by $V_{out}=V_{in}$, where V_M is the midpoint between $0V$ & V_{DD} on the y-axis and V_{IL} & V_{IH} on the x-axis. V_M can be define as

$$V_{out}=V_{in}=V_M \tag{2.36}$$

Here both NMOS and PMOS are saturated and equating the currents we get

$$\frac{\beta_n}{2}(V_{in}-V_{Thn})^2=\frac{\beta_p}{2}(V_{DD}-V_M-|V_{Thp}|)^2 \tag{2.37}$$

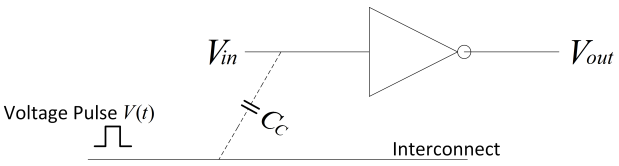
rearranging,

$$V_M=\frac{V_{DD}-|V_{Thp}|+\sqrt{\frac{\beta_n}{\beta_p}}V_{Thp}}{1+\sqrt{\frac{\beta_n}{\beta_p}}} \tag{2.38}$$

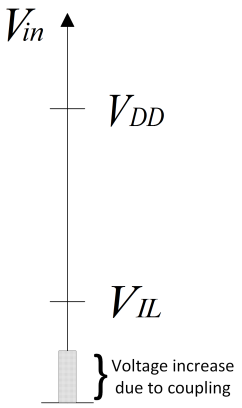
We get the desired V_M equation.

Noise Margin

The amount of noise a CMOS circuit can withstand without compromising the circuit operation is the noise margin. Parasitic coupling is one of the main source of noise in CMOS circuits. Figure 2.21a presents a graphical example where noise can be generated. The parasitic coupling C_C exists between the circuit (Inverter) and interconnect. Applying a voltage pulse $V(t)$ on one line will invariably affect change in voltage on the other line.



(a) Noise Margin Circuit Concept



(b) Variation in V_{in} Due to Noise

Figure 2.21: Noise Variation Due to Stray Coupling

In the presence of electrical coupling, the input voltage will jump by a small value as shown in figure 2.21b. As long as the voltage increase due to electrical coupling remains $< V_{IL}$, incorrect switching will not occur. Figure 2.22 shows a graphical interpretation to the noise margin. For logic 1, the noise margins are defined as follows

$$V_{NM_H} = V_{OH} - V_{IH} \tag{2.39}$$

Similarly, the voltage noise margin for logic 0 is defined as

$$V_{NM_L} = V_{IH} - V_{OH} \tag{2.40}$$

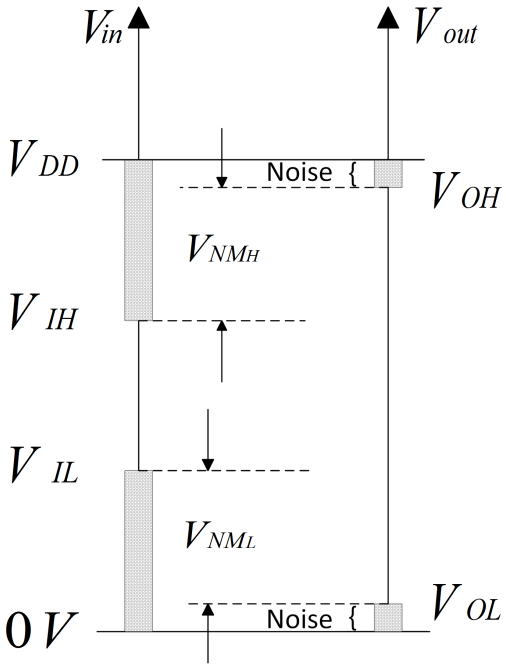


Figure 2.22: Graphical Representations of Noise Margin

For CMOS inverter, $V_{OH} = V_{DD}$ and $V_{OL} = 0V$. In general for the circuit to function without any errors, conditions $V_{NM_H} > 0$ and $V_{NM_L} > 0$ should be true. For the SST clock lines, the traces are spread apart so as to reduce cross coupling and increase noise margins.

Switching Intervals

This transient behavior is dominated by numerous capacitances such as drain diffusion capacitances of NMOS and PMOS, the inter-connect capacitance and the input capacitance of the load circuitry. For the sake of simplicity lets combine all these capacitances to C_L, we can an approximate idea of the inverter switching response can be gauged by looking at simple switch model in the Figure 2.23. For low to high transition the response time is the time taken to charge the capacitance C_L through R_P which is the propagation delay of the R_p C_L network which is $\tau = R_p \times C_L$, Thus, the switching can be fast either by decreasing the load capacitance or by keeping the ON resistance low. The latter can be achieved effortlessly by increasing the W/L ratio of the transistor. Similarly for high to low transitions the

switching speeds depend on the propagation delay of R_n C_L network.

(a) Low to High

(b) High to Low

Figure 2.23: Switching Model of Dynamic Behavior of Static CMOS inverter

The charging time constant is calculated using the subcircuit in figure 2.23a. The time for low to high transition represents the time interval needed for the output capacitor to charge via PMOS while NMOS is cutoff. The time constant of the charging current is given by τ_p

$$\begin{aligned} \tau_p &= C_L \times R_p \\ &= \frac{C_L}{\beta_p(V_{DD} - |V_{Thp}|)} \end{aligned} \tag{2.41}$$

The discharging time constant is calculated using the circuit presented in the figure 2.23b. The high to low time represents the time interval needed for the output capacitor to discharge through the NMOS transistor when the PMOS transistor is cutoff. The time constant for the discharge current is given by

$$\begin{aligned} \tau_n &= C_L \times R_n \\ &= \frac{C_L}{\beta_n(V_{DD} - |V_{Thn}|)} \end{aligned} \tag{2.42}$$

R_n and R_p are the drain source resistance, which are inversely proportional to the $\left(\frac{W}{L}\right)$ ratio. Increasing the aspect ratio will decrease the equivalent resistance.

The sum of the transient times in general represents the minimum time for the gate to churn through one complete switching cycle. The fall time (τ_f) is defined as the time need for the output voltage to fall from $0.9V_{DD}$ to $0.1V_{DD}$. The fall time can be estimated as

$$\tau_f \approx ln(0.9)\tau_n \approx 2.2\tau_n \tag{2.43}$$

Similarly, the low to high time τ_r can be estimated as

$$\tau_r \approx ln(0.9)\tau_p \approx 2.2\tau_p \tag{2.44}$$

From the above two expressions, the maximum switching frequency in this approximation is given by

$$f_{max} \approx \frac{0.45}{\tau_n + \tau_p} \tag{2.45}$$

2.6.4.3 Robustness and Stability of the Buffer

Buffer is one of the main source of skew in the clock distribution networks. The buffers of the clock distribution networks have to be very stable and robust for least amount of skew. The buffers are designed to tolerate device variations, operating temperatures and supply voltage variations.

Two methods were employed to ensure that the buffers were more robust and stable. Although the circuit was designed for nominal operating conditions, actual operating conditions might vary over a large range. The device parameters after the fabrication will probably deviate from the nominal values which we used to design the circuit. Fortunately for the inverter, the DC-characteristics will be more or less insensitive to these device variations.

The inverter will remain functional over a wide range of operating conditions.

We re-simulated the voltage transfer characteristics for corner cases. These corner cases are plotted in the Figure 2.24. Comparing the curves the variations mainly cause a shift in the switching thresholds, but the operation remains normal. This inherent behavior of the inverter ensures the functionality of the circuit over a wide range of variations. More effort is made to keep all the buffers in nominal range of operation.

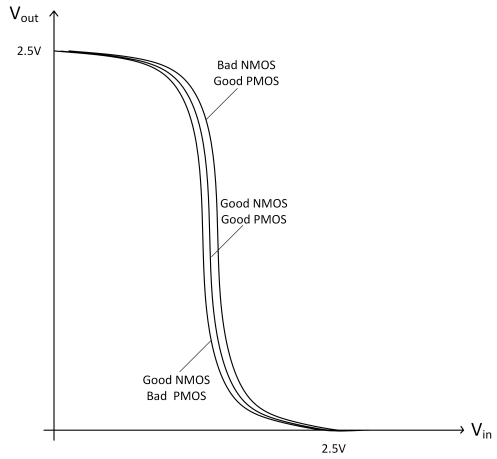


Figure 2.24: Device Variations on Inverter Voltage Transfer Characteristics

Secondly, the inverters used are essentially two inverters connected in parallel as shown in Figure 2.25. The parallel circuit has the same characteristics of an average characteristics of two inverters and dispersion of each element is compensated. Issues in relation to low stability or accuracy due to dispersion of elements are not present. This parallel structure improves the yield and cost performance of manufacturing.

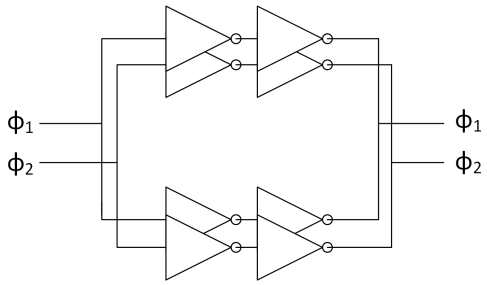


Figure 2.25: Buffer Strategy

2.6.5 Interconnect and Delay Considerations

The goal of the clock distribution network is to achieve low jitter and highly accurate clock signals. The clock skew between two elements in equations 2.15 and 2.16 is the difference between the two propagation delays from the source. The balance between the clock propagation paths must be designed meticulously. During the design, a small positive or negative skew may be desired to improve timing margins for one part of the circuit.

Interconnect and buffers are the main source of clock delays for the SST. These delays are constant and provide a predetermined amount of clock delay form clock source to the destination registers. Although, a great care is taken to keep the delays constant, the delays due to fabrication variations and active components cannot be eliminated. There are three main sources of fixed delays: interconnect, logic gates and lumped circuits. The clock distribution network comprise of interconnect and logic gate, delays due to these components are discussed in this text.

The exact switching moments is altered by the asymmetry in the wiring. The delay due to interconnect is fairly constant. Delay calculation methods such as Elmore delay functions can be used. For a lumped RC model, the interconnect delay is given by

$$\begin{aligned} \tau_i d &= \frac{RC}{2} \\ &= \frac{1}{2}\left(r\frac{l}{w}\right)(c_a l w + 2c_f(l+w)) \\ &\approx \frac{1}{2} r c_a l^2 \end{aligned} \tag{2.46}$$

where, w & l are width and length of the interconnect in μm, r is the sheet resistance in $\Omega/\square$, c_a is the unit area of capacitance in $fF/\mu m^2$ and c_f is the unit effective fringe capacitance in $fF/\mu m$. The delay is proportional to the square of the length of the interconnect.

The logic gates also contribute to the delay, the problem with using these non-linear elements

is that, while the fabrication labs specify the maximum propagation delay, the minimum gate delay is seldom discussed. The total variation in gate delay is large and often for high speed circuits the delay variation will hinder the clock skew. One other issue with logic gates is that the stability depends on the value of the parasitic gate capacitance of the load, secondly, the logic gates have uncertainties in switching thresholds. For example in figure 2.19 the level 2 inverters will switch when the input to the second gate crosses the switching thresholds, if the threshold is uncertain the switching times are uncertain.

2.7 High Speed Sampling Clock

The SST's high speed sampling clocks are generated by 128 dynamic fast shift registers containing a single "1" as a pointer. The figure 2.26 shows that the external clock is applied through LVDS receiver which is fed into 2-phase non-overlapping clock generator and later through a buffer clock tree and finally to the fast shift registers. The clocks are distributed in a uniformed fashion to all the 128 dynamic master-slave flip-flops which are configured in circular fashion. The sampling clocks are generated by both master and slave flip-flops, hence the sample rate is double with respect to the external clock.

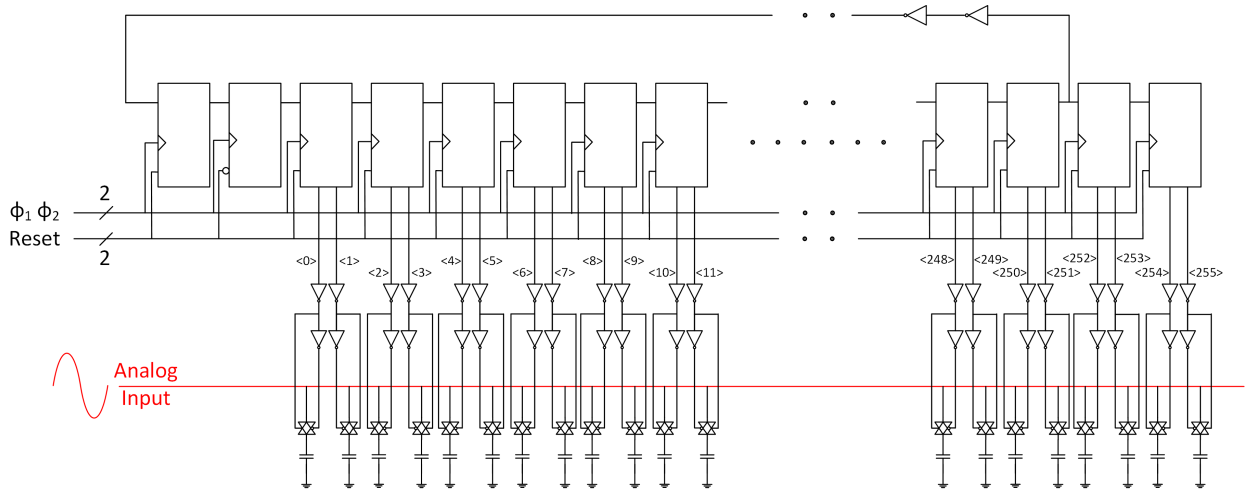


Figure 2.26: Fast Shift Register Block Diagram

2.7.1 Design and Analysis

The 256 sample clocks are generated in a circular array of 128 high speed dynamic master-slave flip-flops. Both master and slave sections are used to provide the sampling clocks, hence doubling the sample and hold frequency compared with the clock that drives the shift register itself. The block diagram and the corresponding connections to the sample and hold capture circuitry is shown in figure 2.26. The prevailing advantage of using both master and slave latches for the sampling clock is the ability to have an increased (twice) sampling clock frequency. Although, a minor disadvantage that needs to be accounted is the inherent "fixed pattern noise" in the sampling clock. The type of fixed pattern noise and the analysis will be discussed in part II.

2.7.1.1 Dynamic Logic

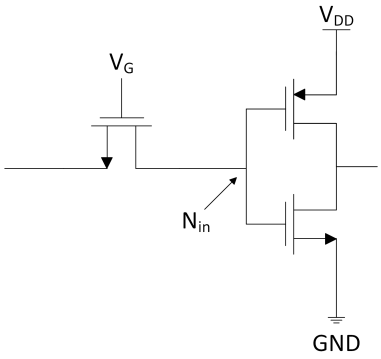
The static logic gates are widely used, the outputs of the static gates are valid as long as the inputs are defined. However, the results in the dynamic logic is valid for only short period of time. The dynamic logic uses capacitive nodes to store electrical charge. The transfer and retention of charge at these capacitive nodes are critical for the operation of the dynamic logic circuits.

Dynamic Logic Charge Leakage

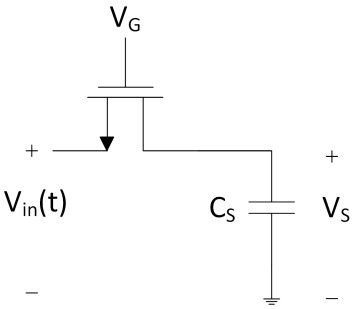
Transistors are usually modelled as voltage-controlled switches that are capable of turning ON and OFF when the input voltages crosses the threshold voltage. In reality, leakage persist and the leakage currents are minute. For dynamic logic these leakage currents are very critical.

Figure 2.27 shows a simple switching inverter circuit. When the NMOS is turned off, the

input node N_{in} is isolated from V_{DD} and GND. The storage capacitor C_S is solely responsible to hold the charge.



(a) Switching Circuit



(b) Storage Capacitor Model of the Switching Circuit

Figure 2.27: Charge Storage Node of a Dynamic Inverter Circuit

The total stored charge on the storage capacitor is given by

$$Q_s = C_s \times V_{max} \tag{2.47}$$

V_{max} is given by $V_{max} = V_{DD} - V_{Thn}$.

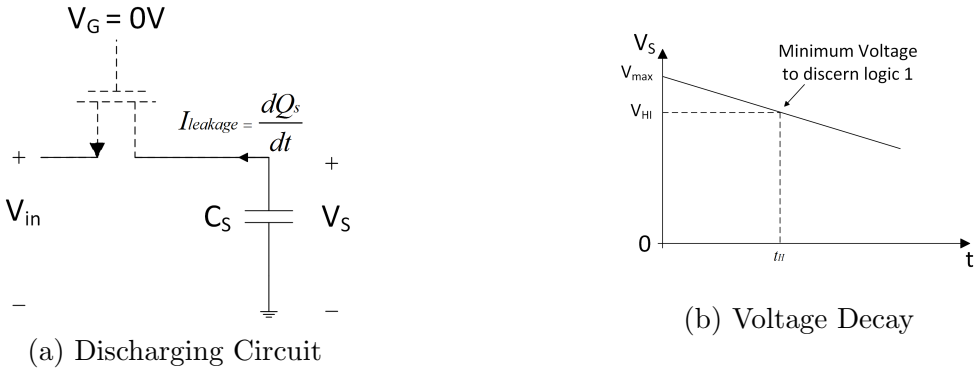
Any attempt to hold the gate-source voltage of the switch at $V_{Gsn} < V_{Thn}$, results in leakage. The leakage current $I_{leakage}$ slowly degrades the charge from capacitor C_S in figure 2.27b. The leakage current is given by

$$I_{leakage} = -\frac{dQ_S}{dt} = -C_S\frac{dV_s}{d_t} \tag{2.48}$$

Overtime, the leakage current will remove the charge, the V_S will eventually decrease from V_{max} and fall to a value where it can be interpreted to an incorrect logic. By using the initial condition, $V_S(0) = V_{max}$, the charge leakage across the capacitor is given by equation 2.49

and shown in figure 2.28a

$$V_S(0) \approx V_{max} - \frac{I_{leakasge}}{C_S}\tau \tag{2.49}$$



(a) Discharging Circuit

(b) Voltage Decay

Figure 2.28: Charge Leakage Node of a Dynamic Inverter Circuit

The linear decay is plotted in figure 2.28b. The hold time of the dynamic circuit is given by

$$t_H \approx \frac{C_S}{I_{leakasge}}(V_{max} - V_{HI}) \tag{2.50}$$

2.7.1.2 Dynamic Master-Slave Edge Triggered Flip-Flop

The fully dynamic negative edge triggered master-slave register used in the SST is shown in the figure 2.29. When $\phi_1 = 1$, the input data is sampled on node N_1, which has an equivalent parasitic capacitance of C_1 which consist of the gate capacitance of the first inverter and the source capacitance of switch S_1. During this period the slave stage is in hold mode i.e., node N_2 is high-impedance. On the rising edge of ϕ_2 the switch S_2 turns ON, and the value sampled on node N_1 right before the rising edge propagates to the output Q (node N_1 is stable during the high phase of ϕ_2 since the first switch is turned off). Node N_2 now stores the inverted version of node N_1.

This implementation of the edge-triggered flip-flop is very efficient as it requires only 6 transistors. This reduction in transistor count is very attractive for SSTs high speed performance

and very low power utilization.

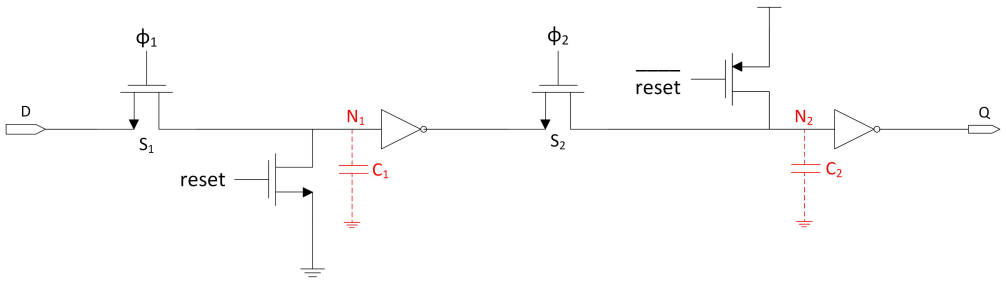


Figure 2.29: Fast Shift Register Cell

The set-up time of the flip-flop is just the delay of the NMOS switch S_1, it's basically the same time it takes node N_1 to sample the input "D".

The hold time of this register is approximately zero, since the NMOS switch is turned off on the falling edge of ϕ_1 and further changes in "D" are ignored.

The propagation delay t_{c-q} is equal to the two inverter delays with addition to the delay of the switch S_2.

The master-slave shift register shown in figure 2.29 is designed to move a data bit by one position to the right during each half clock cycle. The data bit is admitted to the master stage when $\phi_1 = 1$ and its transferred to slave stage when $\phi_2 = 1$. Every bit entered through the system, follows the previous bit which results in movement of the bit from left to right. This operation of the circuit will place some strain on the operating clock frequency f.

Let's assume the reset is zero, and analyze the data input movement from input to slave stage via master stage. During this time $\phi_1 = 1$, which means $V_{\phi_1} = V_{DD}$. This will turn on the switch S_1 allowing C_1 to charge to the appropriate value. S_1 is acting as a pass transistor, the worst-case situation will be logic HI and the input voltage is given by

$$V_1(t) = V_{max}\left[\frac{\frac{t}{2\tau_n}}{1+\frac{t}{2\tau_n}}\right] \tag{2.51}$$

where

$$V_{max} = V_{DD} - V_{Thn} \tag{2.52}$$

For NMOS transistors, the switching times (rise and fall times) are defined as the voltage switching between $0.1V_{DD}$ to $0.9V_{DD}$. In terms of NMOS charging time constants (τ_n) the rise and fall times are given by [46]

$$\tau_{rn} = 18\tau_n \tag{2.53}$$

$$\tau_{fn} = 2.94\tau_n \tag{2.54}$$

Therefore, combining the charge time constant of the NMOS (S_1) and the total delay associated with the NMOS (τ_n) of the inverter, the time needed for the capacitor (C_1) to react to the input is

$$t_{C1} = \tau_{rn} + \tau_n \tag{2.55}$$

During the next instance of the clock, when $\phi_1 = 0$, $V_{\phi_1} = 0V$, the switch S_1 is OFF. During this time, the charge leakage will occur and the voltage V_1 across capacitor C_1 will decay form the original V_{max} value. The minimum voltage value at the master inverter input that will still be interpreted as logic 1 value is V_{1HI}, from equation 2.50 the maximum hold time is estimated to be

$$t_H \approx \frac{C_1}{I_{leakasge}}(V_{max} - V_{1HI}) \tag{2.56}$$

From these two times, the maximum and minimum clock frequency can be estimated. The maximum clock frequency which sets the upper limit for the systems data rate is given by

$$f_{max} = \frac{1}{T_{min}} \approx \frac{1}{2t_{C1}} = \frac{1}{2(\tau_{rn} + \tau_n)} \tag{2.57}$$

The charge leakage problem will set the limit for the minimum frequency. Since the node

N_1 cannot hold logic 1 for longer time, the f_{min} is given as

$$f_{min} = \frac{1}{T_{max}} \approx \frac{1}{2t_H} \tag{2.58}$$

In general the clock frequency must be chosen in the range of

$$f_{min} < f < f_{max} \tag{2.59}$$

for proper operation of the dynamic register.

Another very important concern for this type of register is clock-overlapping. For example consider the clock waveform shown in figure 2.30. Here during the high-overlap period, there exists an input-output path through NMOS switch S_1 and NMOS switch S_2. This scenario creates a direct path from input "D" to output "Q". The "Q" changes at the rising edge of ϕ_1 if the overlap period is large and this is undesirable effect for the negative edge triggered flip-flop. This undesirable effect can be taken care by enforcing a hold time constraint for ϕ_1. That is the data must not change during the high overlap period. The low overlap period is not a concern for this design.

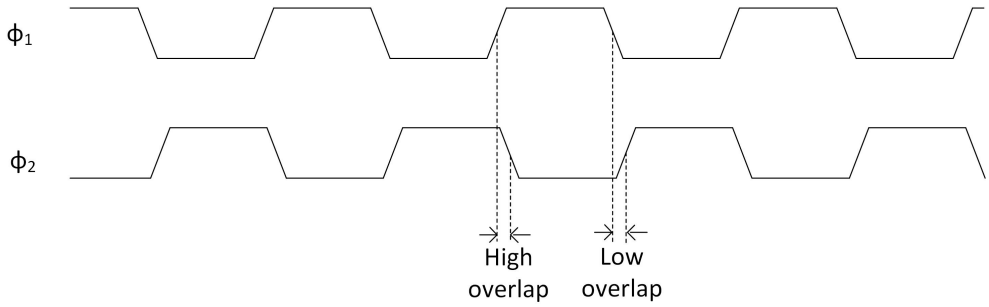


Figure 2.30: Overlap Clock Waveform

The SST however does not suffer from this overlap issue since we use non-overlapping clocks to drive the sift registers. Figure 2.31 shows the 2 phase non-overlapping clock signal used to drive the shift registers.

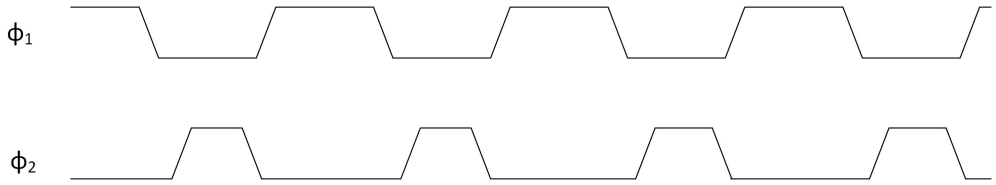


Figure 2.31: Non-Overlap Clock Waveform

The high speed dynamic shift registers are of utmost importance to generate ideal sampling clock. Asymmetry in the layout will cause the sampling clock to vary and affect the timing of the whole circuit. The layout of the high speed dynamic shift registers with the buffered feed back path is shown in the figure 2.32

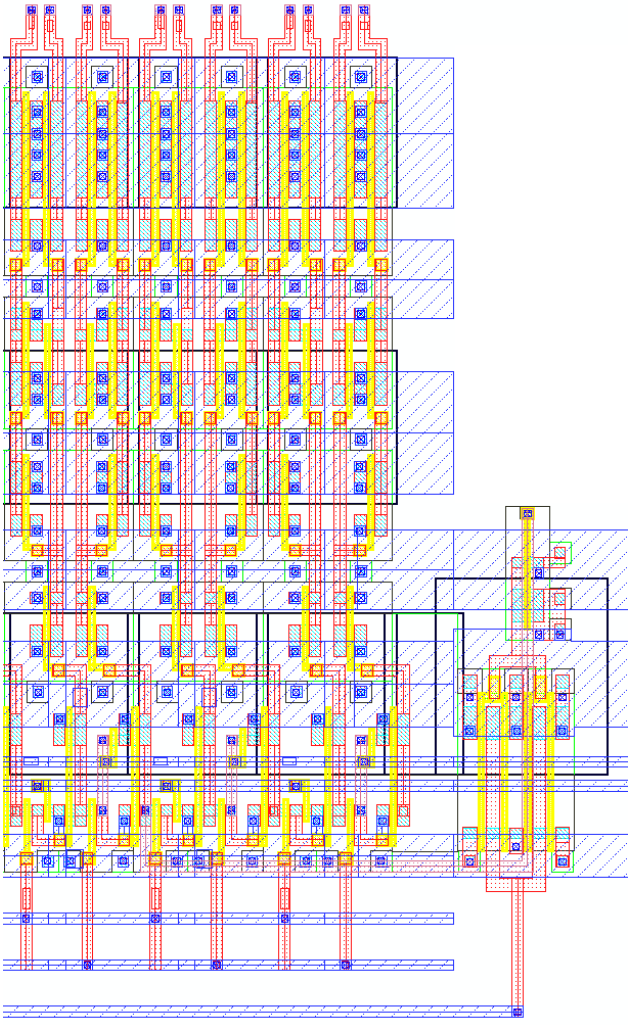


Figure 2.32: A Section of the Layout Block that shows the High-Speed shift register block and the Feed-Back Circuitry

The pitch of 3.6μm is maintained in order to snap the clock generation circuit to the sample and hold circuit. The bottle neck for the pitch is the capacitor layout.

2.8 Sampling

The sampling in the SST is performed by the complementary CMOS switches and 80 fF metal-insulator-metal capacitors.

The design details of the sample and hold circuity will not be discussed in this dissertation. For the sake of continuity, only a brief overview of the sample and hold circuit array will be discussed. Figure 2.33 shows the schematic of a single sample and hold circuit used in the SST. A detailed analysis of the sampling and hold circuit can be found in [19].

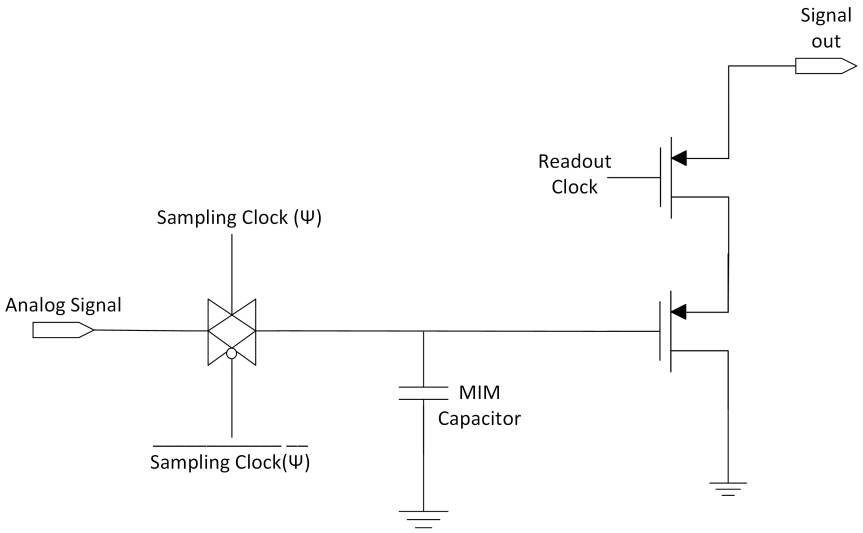


Figure 2.33: Sample and Hold Circuit

Each sample and hold circuit consist of a transmission gate followed by a MIM capacitor. Connected to the MIM capacitor is the circuitry for the voltage buffering and selection for analog readout. The fast shift registers discussed in section 2.7 supply the sampling clock to the sample and hold circuitry. When the sampling clock is asserted, the transmission gate

is ON and the voltage of the input analog signal is stored on the MIM capacitor.

Each channel of the SST has 256 sample and hold array. The sampling clocks of all four channels are connected and the fast shift registers will move the clock (pointer) in a circular fashion so that one sample is ON and all other samples are OFF at any given time.

The decision to use complementary transmission gate instead of NMOS pass transistor was made so that the input voltage range will be higher for the sample and hold circuit. The CMOS pass gate can maintain a suitably low ON resistance for a wider range of input voltages. The additional capacitance from PMOS has minimal effect on the individual circuit. However since the sample and hold array has 256 circuits connected to the single node the contribution of 256 PMOS will be substantial and will affect the bandwidth of the circuit. The sample and hold circuit was carefully designed to achieve 1.4GHz of bandwidth.

The performances parameters such as speed, noise and voltage variation due to charge injection and leakage of the sample and hold circuit will mostly depend on the size of the MIM capacitor [26]. The capacitor should be sufficiently small such that fast input analog signals can be traced. However reducing the size of the capacitor will increase the effects of charge injection and current leakage as well as worsen the RMS noise power. The MIM capacitor of 80 fF yields and acceptable speed and noise tradeoffs.

The readout circuitry is used to buffer the voltage on the capacitor. The signal out wire of each of the 256 sample and hold cells are connected to a PMOS current source load. During the SST readout only one of the 256 readout clock will be asserted, the rest of the signals will be de-asserted. When the readout clock is asserted, the voltage stored on the capacitor will be readout. Conversely, when the readout clock is de-asserted the PMOS is cutoff and acts as high impedance and thus it will not affect the output node.

2.9 Triggering Circuitry

A very sensitive real-time dual threshold triggering circuit was designed for the SST to detect very small and fast impulse signals. For ARIANNA the frequency of interest in 100 MHz to 1 GHz, the trigger circuitry is capable of detecting these radio-frequency signals due to Askaryan effect. The circuitry compares a transient voltage signal with a threshold voltage in real-time. The circuit will send an interrupt (Trigger) when the thresholds are crossed. By adjusting the control signals to the triggering circuitry, the SST will trigger when the incoming transient signal crosses either one or both thresholds.

Each channel of the SST has an independent trigger circuitry. The trigger circuitry will be active during the acquisition mode, the trigger circuit will send out an interrupt when the input stimulus crosses the threshold. This interrupt will indicate the external off chip microcontroller that a signal of interest has been acquired and the SST can be readout.

Figure 2.34 shows the trigger circuitry of one channel.

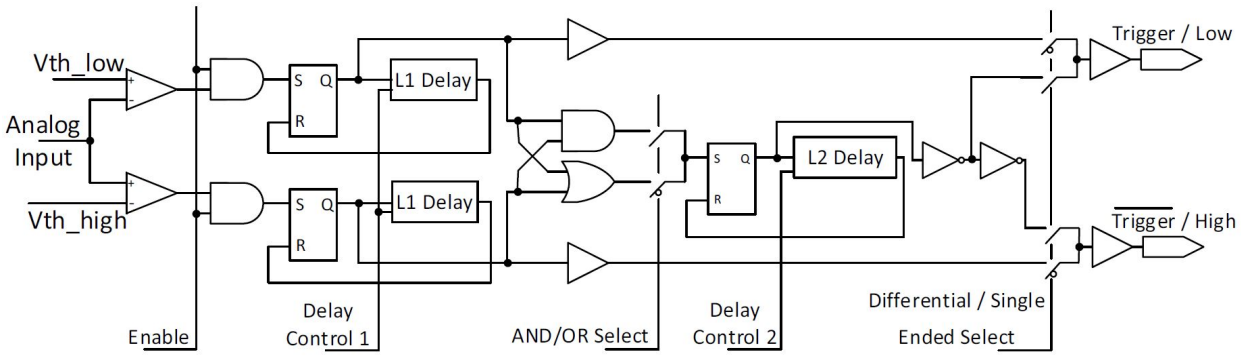


Figure 2.34: Trigger Circuit

The two comparators pass through a set of SR latches and delay lines which stretch the output pulses of the comparator. The delays can be controlled by the external analog control. These stretched pulses will be used for the coincidence logic. These coincidence

logics are simple AND/OR operation. The selection can be done externally. For example if the L1 delay is set to 5ns then the all the bipolar signals 100MHz and above will be captured by the coincidence logic. The signals below 100MHz frequency will be not be captured and these signals will be suppressed.

2.9.1 Triggering Modes

The triggering logic is capable of operating in two modes. The single ended mode and the differential mode. During the single ended operation, the comparator outputs are directly read out via the pulse stretching latches. The comparator outputs are subjected to additional coincidence logic during the differential mode of operation. The following subsetions explain these modes in detail.

2.9.1.1 Single ended

The triggering circuitry is divided into trigger logic and coincidence logic, in the figure 2.34 the comparators, enable circutry and L1 delay control logic is considered as trigger logic, the rest of the circuitry is coincidence logic. During the single ended mode the coincidence logic becomes irreverent. The output of the SST is basically the stretched versions of the HIGH and LOW comparators. Figure 2.35 shows a scenario for single ended operation.

Here the width of the trigger pulses can be manually adjusted by adjusting the L1 width/delay. By default, the SSTs L1 width is set to 5 ns.

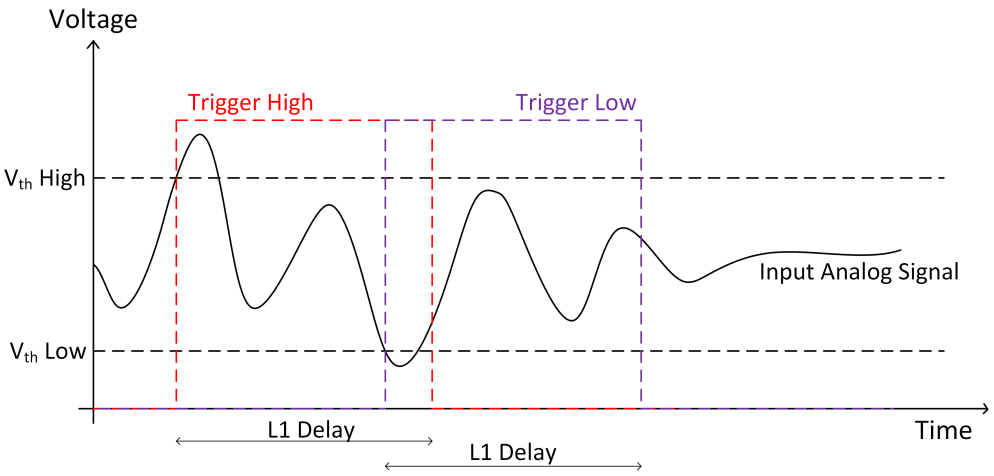


Figure 2.35: Single Ended Operation

2.9.1.2 Differential Mode

The outputs of the comparators are subjected to AND/OR coincidence logic during differential mode of operation. An additional "AND/OR Select" control signal is required to choose between AND/OR logic. ARIANNA experiment mainly uses differential mode of operation.

AND Operation

In this mode of operation, the SST will trigger only if both the comparators trigger within the specified delay.

An exploration of the scenario where the mode of operation is set to differential, the type of operation is AND, L1 delay is set to 4ns and L2 delay is set to 8 ns can be insightful. In the figure 2.36 below the input to the coincidence high logic will trigger as soon as the input crosses the high threshold. Since the L1 delay is set to 4 ns the input pulse to the coincidence high logic will be 4ns wide. The input to the coincidence low logic will trigger as soon as the input crosses the low threshold. The trigger output is the AND operation of these two coincidence inputs. The SST will trigger when both the coincidence inputs trigger.

The final trigger of the SST will be 8ns wide (L2 delay).

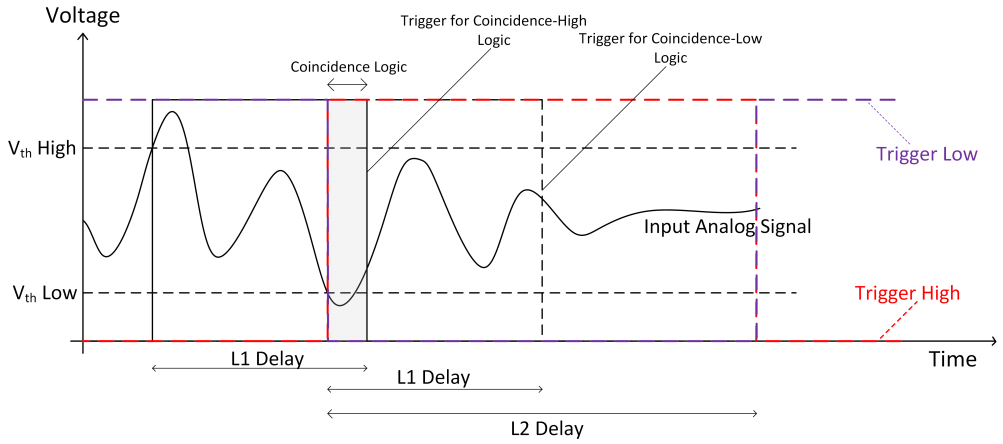


Figure 2.36: Differential Mode - AND operation. Assume L1 Delay is 4 ns and L2 Delay is 8 ns

Let's take another scenario where the mode of operation is set to differential, the type of operation is AND, L1 delay is set to 4ns and L2 delay is set to 8 ns but with different input stimulus. In the figure 2.37 below the input to the coincidence high logic will trigger as soon as the input crosses the high threshold. Since the L1 delay is set to 4 ns the input pulse to the coincidence high logic will be 4ns wide. However in this scenario the coincidence low trigger will assert approximately 6ns after the coincidence high trigger is asserted. There is no overlap between the coincidence low and high trigger. In this case the SST will not trigger and this signal will be suppressed by the SST.

OR Operation

In this mode of operation, the SST will trigger if either of the comparators trigger. OR operation is essentially a single ended mode of triggering discussed in section 2.9.1.1 with differential outputs.

Another instance that can be delved into is one where the mode of operation is set to

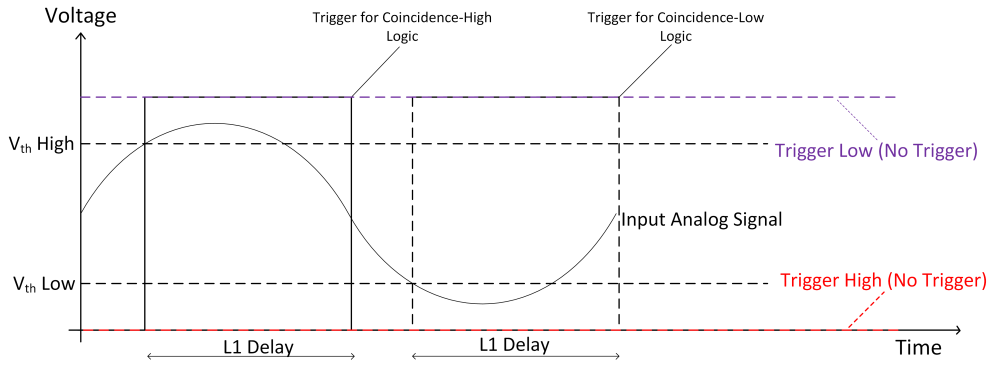


Figure 2.37: Differential Mode - AND operation. Assume L1 Delay is 4 ns and L2 Delay is 8 ns

differential, the type of operation is OR, L1 delay is set to 4ns and L2 delay is set to 8 ns. In the figure 2.38 below, the input to the coincidence high logic will trigger as soon as the input crosses the high threshold and the SST will trigger as soon as either of the coincidence logic triggers. The SST trigger will be 8ns wide (L2 delay).

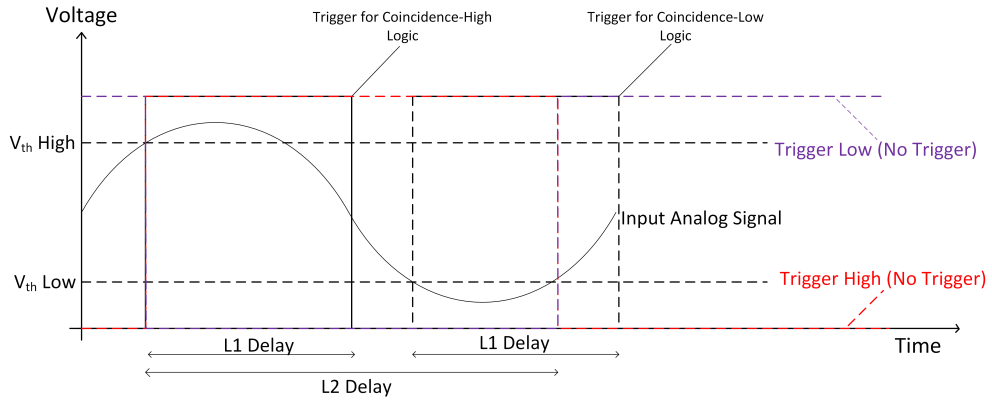


Figure 2.38: Differential Mode - OR operation. Assume L1 Delay is 4 ns and L2 Delay is 8 ns

2.9.2 Design and Analysis

The trigger circuitry can be broken into three sections: the comparator, trigger logic and coincidence logic.

2.9.2.1 Comparator

The design details of comparator will not be discussed in this dissertation. For the sake of continuity, only a brief overview of the comparators will be discussed. The comparators shown in the figure 2.39 for the SST were designed by Edwin Cheim [19]. The SST has 8 comparators, 2 per each channel. Each comparator has a P-channel input stage to allow for low common mode voltages, followed by four n-channel stages plus differential to single ended converter. Resistor loads with low parasitic capacitances allow for higher speed. The gain of each differential stage is ∼3.3, the bandwidth is around 1.2GHz. The simulated trigger sensitivity is 1 mV RMS at 500 ps Full Width Half Maximum.

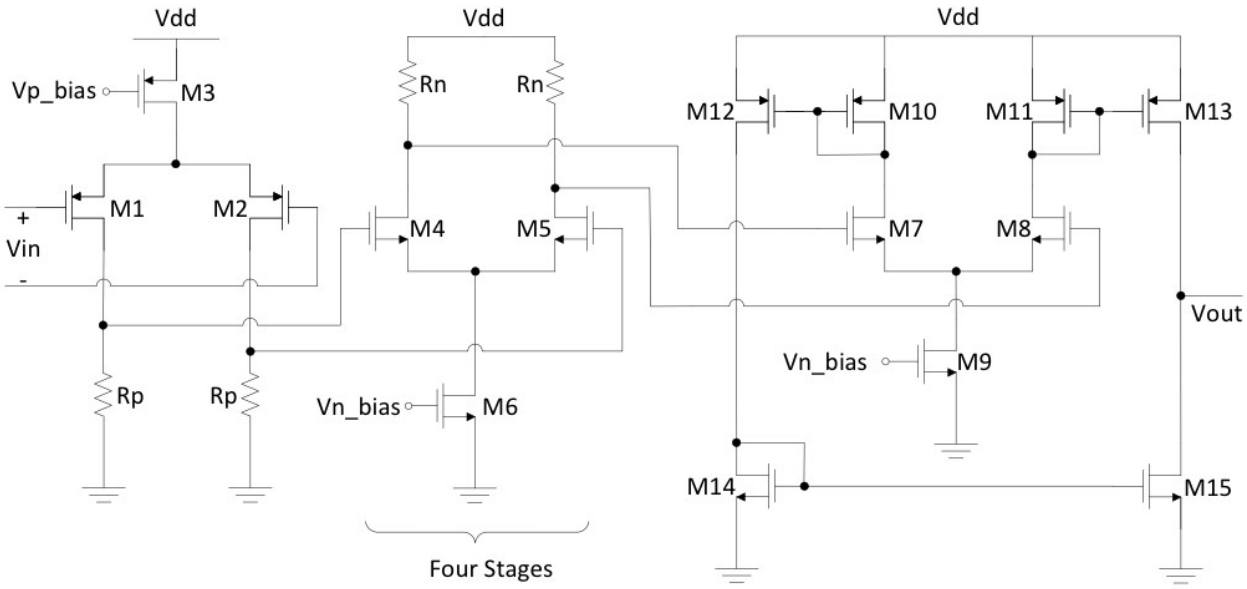


Figure 2.39: Comparator Schematic [3]

2.9.2.2 Trigger and Coincidence Logic

Since the comparators are sensitive, and to reduce the trigger rates due to thermal noise, a combination of two comparators with high and low thresholds (for bipolar signals) are

[3]figure originally published in [40]

used. The trigger logic works in tandem with two comparators. The trigger logic consist of enable circuitry, pulse-stretching latches, analogically-controlled digital delay lines, AND/OR coincidence logic and selection circuitry.

The enable circuitry turns on the trigger logic during acquisition mode and turns off the trigger logic during readout mode. The circuitry is a very simple digital 2 input AND gate. The enable is connected to one input and the comparator output is connected to the second input of the AND gate. The enable is HI during acquisition and LO during readout phase.

The pulse-stretching latches consist of Set-Reset latches and analogically-controlled digital delay lines. This circuit will basically hold the comparator outputs high for an amount of time which is typically set based on the frequency of interest. The figure 2.40 shows the circuitry and waveform of the pulse stretching latches. The coincidence logic is shown in figure 2.34.

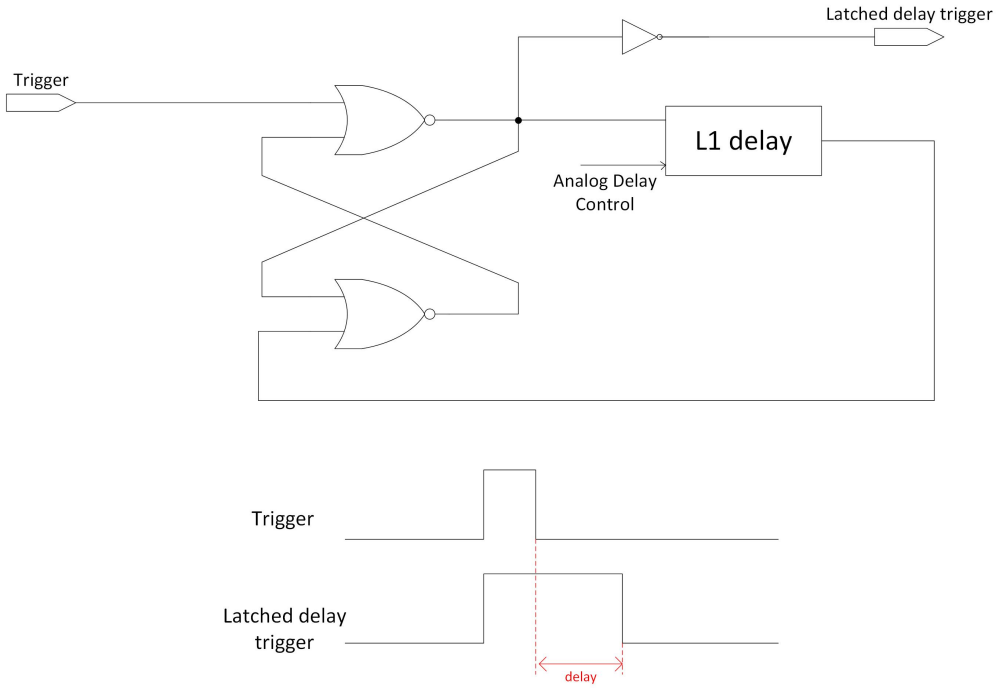


Figure 2.40: Trigger Logic

Delay Lines

The Delay lines consist of a chain of identical adjustable delay elements, connected front to back (Figure 2.41) and controlled by the same control voltage V_{ctrl}. Since each delay element of the line is controlled by the same voltage reference, all the delays of the line are identical. When a signal V_{in} is set at the input of a delay line made of n cells, it will propagate through the line, being successively shifted n times. At the end, the output signal V_{out} is a copy of V_{in} after $n\times$ delay

$$V_{out}(t) = V_{in}(t - n \times delay) \tag{2.60}$$

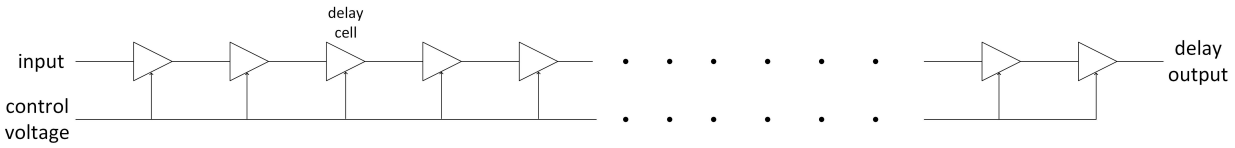


Figure 2.41: Delay Line

Current Starved Inverters

A variable delay elements such as current starved inverter chain are used for fine, precise and accurate pulse delay control for high speed digital integrated circuits. Voltage control delay lines elements are also known as analog voltage controlled delay line elements, these delay elements are efficient in applications where small and accurate amount of delay is necessary to achieve. To achieve this delay, SST employs current starved delay elements. I_D vs V_{GS} curve in figure 2.42: The saturation current is a quadratic function with respect to gate-source voltage above the threshold voltage (V_T). In this region, the transistor can be used as a voltage controlled current limiter circuit. For the NMOS in saturation region, I_D is given as

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \tag{2.61}$$

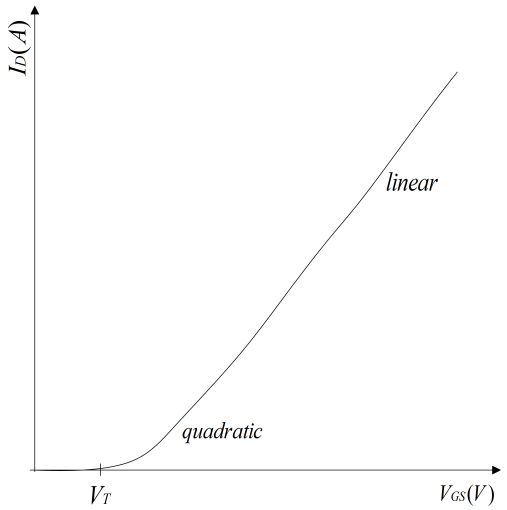


Figure 2.42: NMOS Transistor: $I_D - V_{GS}$ Characteristics

SST's trigger delay chain is more like a pulse stretching circuit. Only the falling edge is delayed. The schematic for the current starved inverter circuit is given in the figure 2.43 The delay cell shown in figure 2.43 can control the delay of the falling edge with the change

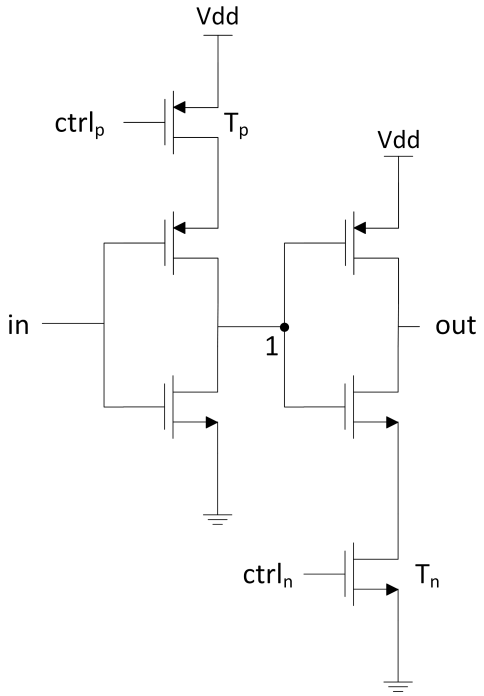


Figure 2.43: Schematic of Current Starved Delay Element

in voltage controls $Ctrl_p$ and $Ctrl_n$. In the first inverter (fig: 2.43), the voltage controlled

PMOS transistor (T_p) becomes a controllable resistor R_P. The formula for the controllable resistor of the switch versus the control voltage $Ctrl_p$ is given by

$$R_p = \frac{1}{\beta_p(V_{DD} - Ctrl_p - V_{Thp})} \tag{2.62}$$

The voltage controlled PMOS (T_p) becomes a highly non-linear function of $Ctrl_p$ as it varies proportional to $\frac{1}{Ctrl_p}$. The charging time is controlled by the RC filter comprising of T_p and the gate capacitance of the second inverter (Capacitance at node $1(C_1)$). The delay introduced by the voltage controlled PMOS is given by

$$delay = \frac{2C_1}{\beta_p(V_{DD} - Ctrl_p - V_{Thp})} \tag{2.63}$$

Similar calculations can be made for T_n and $Ctrl_n$. As expected the delay introduced by the current-starved inverter is highly non-linear and the simulation results of the falling edge delay versus the control voltages are presented below.

The trigger circuitry has two independent delay lines (L1 delay logic and L2 delay logic). Each of these delay logics are controlled by separate analog delay controls. The first delay line is used in the trigger logic and the second delay block is used in the coincidence logic.

The figure 2.44 is shows the delay (y-axis) with respect to the control voltage (x-axis) of the first delay element. This delay line is mainly used to stretch the comparator pulse. The figure 2.45 is shows the delay (y-axis) with respect to the control voltage (x-axis) of the second delay element. This delay line is mainly used to stretch the coincidence logic pulses. The SST's two delay lines are made of 30 delay cells (L1 delay block) and 60 delay cells (L2 delay block). Biasing circuitry and a part of delay cells are shown in figure 2.46.

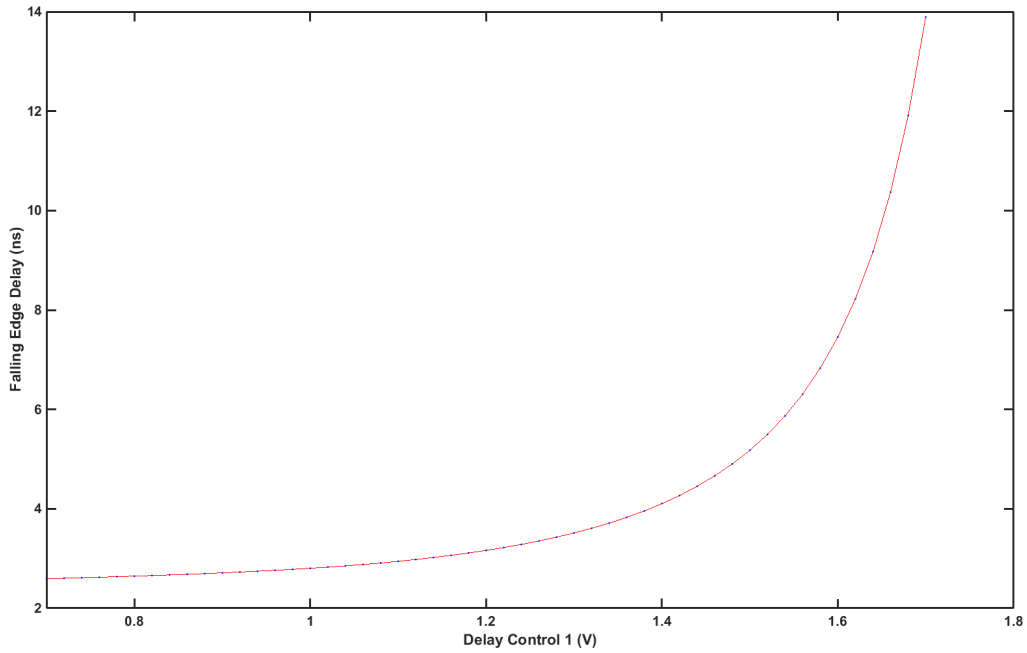


Figure 2.44: Simulation of Falling Edge Level 1 Delay

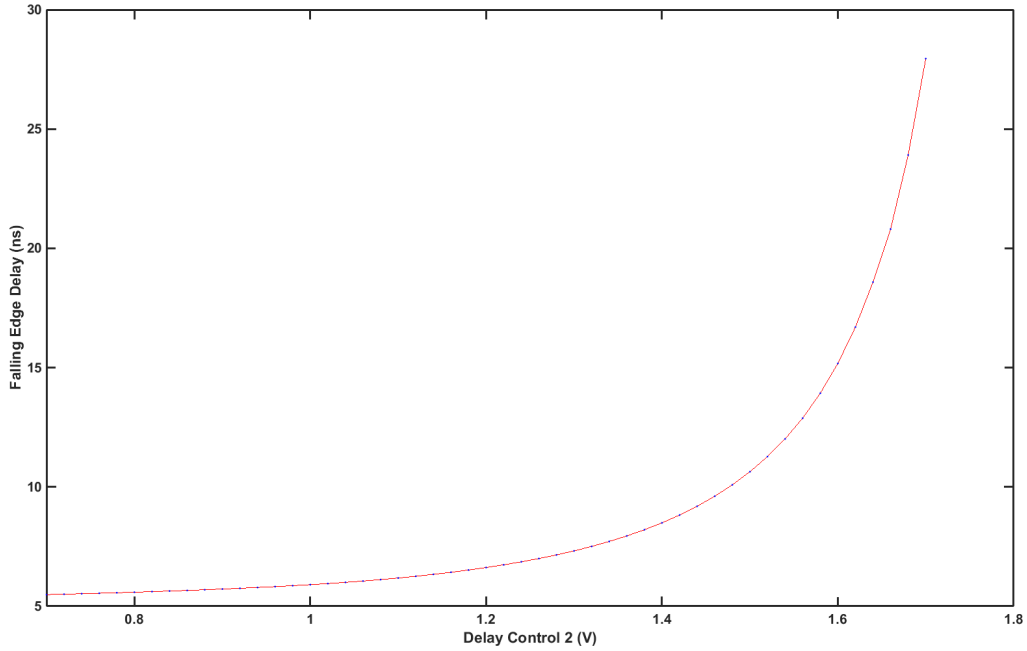


Figure 2.45: Simulation of Falling Edge Level 2 Delay

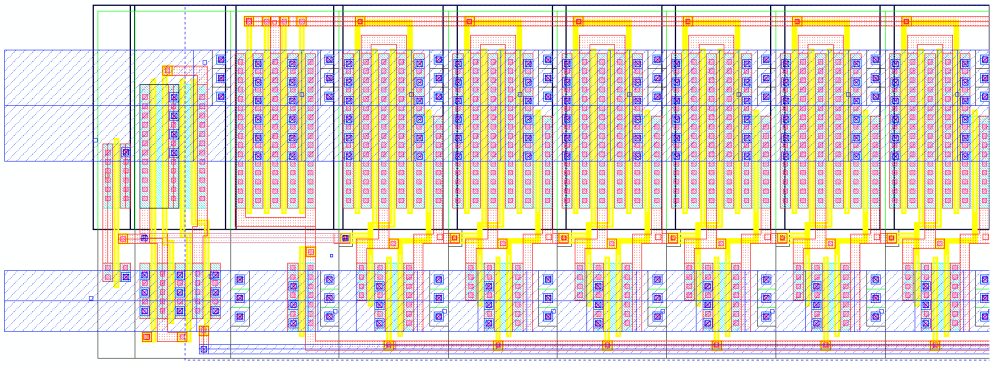


Figure 2.46: A Section of the Delay Line Layout

2.10 Readout Clock Generation

A simple active pixel sensor-type readout scheme was employed for the SST. From the discussion in section 2.2, the SST has two modes of operation, acquisition and readout. The readout mode is engaged by the external controller (FPGA in our case). The assertion of read clock by the FPGA will engage the readout mode. The readout is sequential and is in the order of 800 kHz and 10 MHz.

As discussed in section 2.8 the sampled data is readout by a source follower circuit. The source follower circuit is followed by a PMOS switch which is controlled by a slow readout shift register.

The figure 2.47 shows the block diagram of the readout clock generation circuit. The slow readout clock generation circuit is a combination of two phase clock generation circuit and 256 master-slave shift registers.

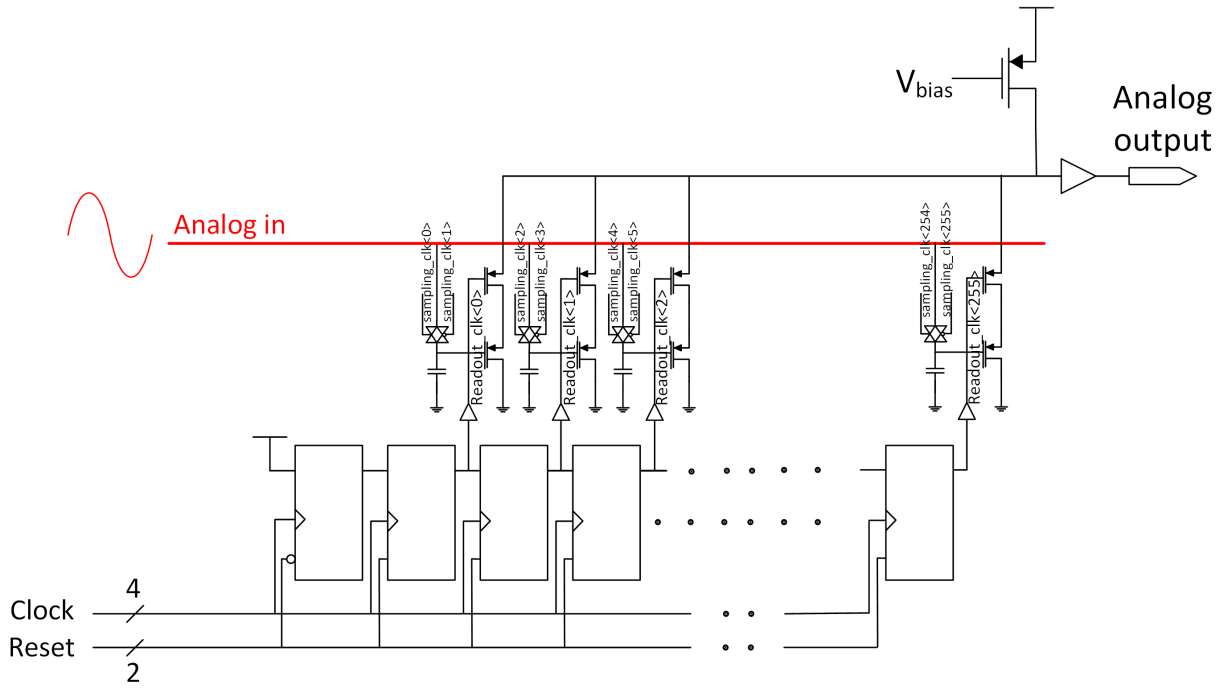


Figure 2.47: Readout Clock Generator Block diagram

2.10.1 Design and Analysis

The SST's readout clocks are generated by 256 static shift registers connected is series. The clocks to the 256 shift registers are generated by a 2 phase clock generation circuit. In practice, a 1 MHz clock is applied to the two phase cock generation circuit which in-turn clocks the shift registers to generate readout clocks.

2.10.1.1 Two Phase Clock Generation Circuit

The two phase clock generation circuit is shown in figure 2.48. The input clock is generally from the FPGA in the range of 800 kHz to 10 MHz. The speed of the clock is not a priority, hence additional care was taken to design a robust circuit. The two phase clock generation circuit produces two non-overlapping phases and their complements ($\phi_1, \phi_2, \overline{\phi_1} and \overline{\phi_2}$). The non-overlapping clock is essential to ensure that the two latches are not transparent at the

same time.

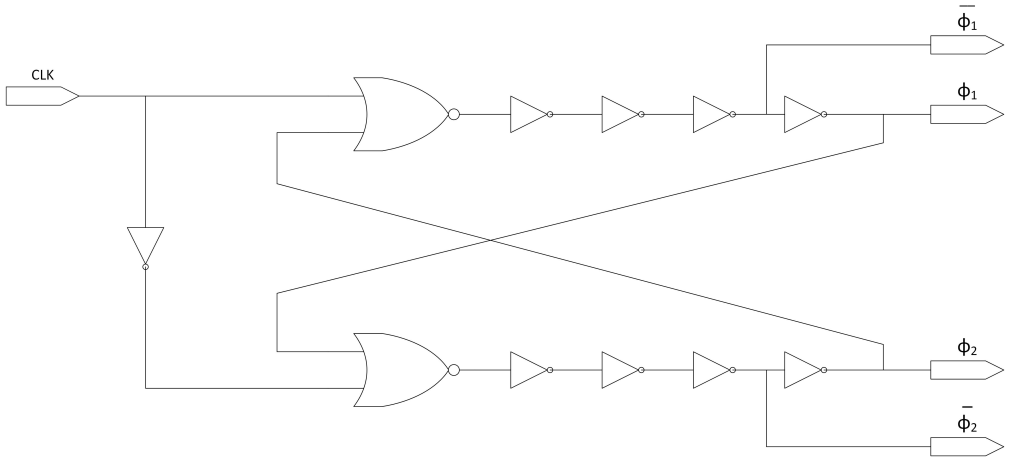


Figure 2.48: Two Phase Clock Generator Block Diagram

2.10.1.2 Shift Registers

The shift registers are used to convert the non-overlapping clock to a readout pointer which propagates through the chain and readout the capacitors data sequentially.

Figure 2.49 shows a single shift register used in the readout clock generation circuit. The NAND gate in the master and NOR gate in the slave is used to reset all the 256 shift registers. A complementary reset shift register, connected to VDD is placed at the beginning of the chain to insert a pointer. Figure 2.50 shows the complementary-reset shift register. When the *Reset* is high and $\overline{Reset}$ is low the pointer is inserted and successive clocks will shift the pointer along the row.

Figure 2.51 shows the output waveforms of the shift registers. The pointer (0 in this case) is shifted along the row. The capacitor values are readout out from a single sample at any given time during the readout phase.

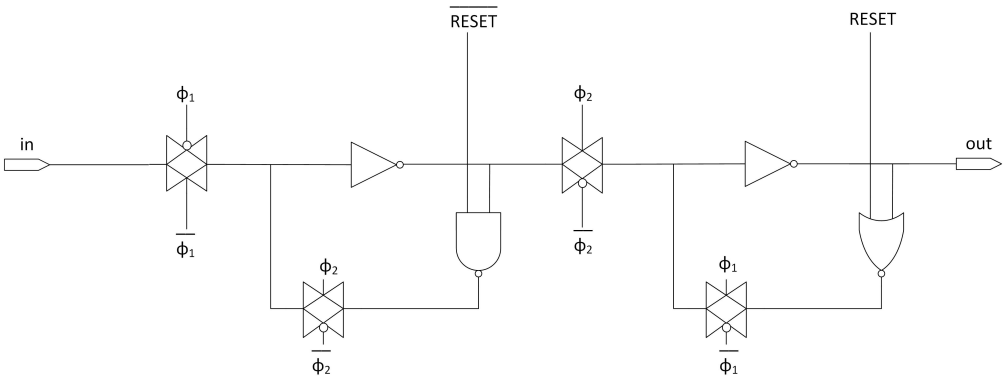


Figure 2.49: Readout Shift Register

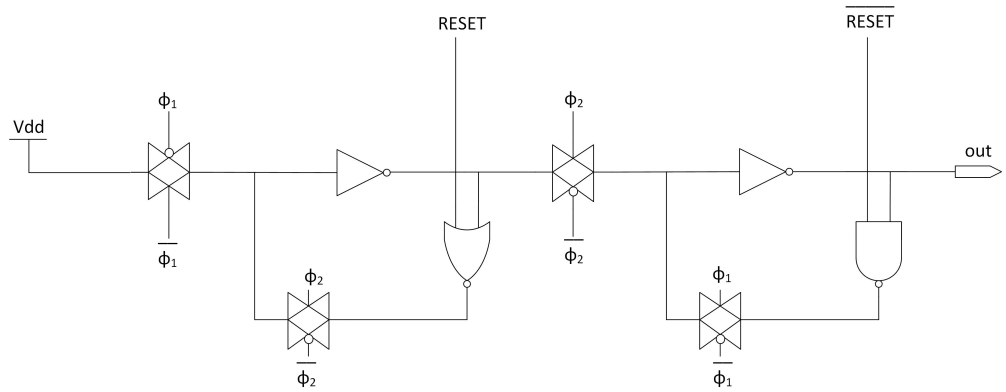


Figure 2.50: Complementary Reset Readout Shift Register

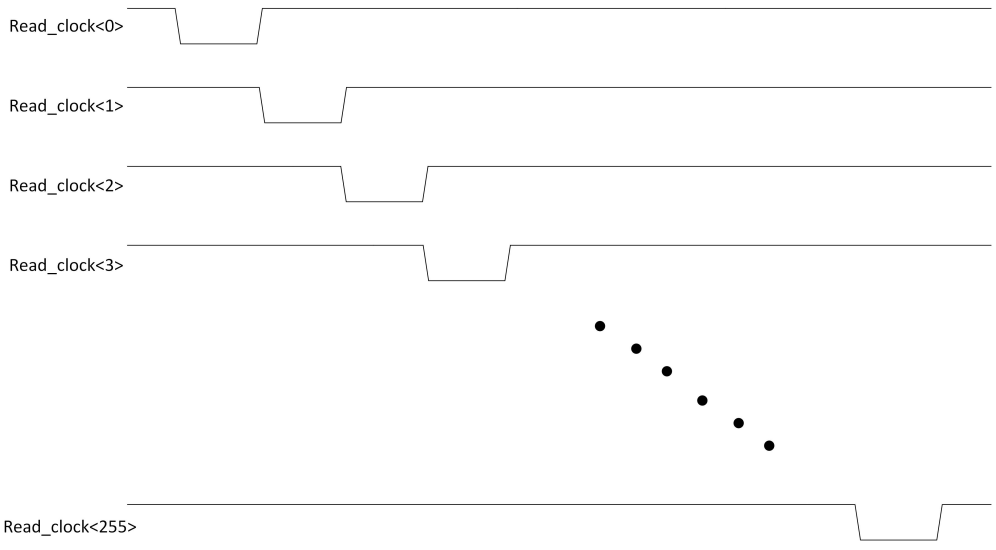


Figure 2.51: Conceptual Waveform Output of the Readout Shift Register

2.11 Stop Position Readout Circuit

The SST is operated in common-stop mode. Common-stop mode is employed when the arrival of the analog transient signal is unknown. The SST is started and runs continuously, circularly sampling the analog data whilst discarding the oldest data. When a signal of interest arrives, a trigger is asserted and the SST is stopped after a predefined delay. The position of the sample clock pointer at the moment it is stopped is read out in parallel with the analog samples. The position of the sample clock is essentially the STOP position.

2.11.1 Design and Analysis

A simple inverter-switch circuit is used to readout the stop positon of the SST. During the readout phase of the SST, the stop position circuitry will output the sampling clocks for the sample and hold circuit serially. Figure 2.52 shows a block diagram of the stop position readout circuitry.

STOP is essentially the sample pointer, the term STOP is used because that is the position at which the chip was stopped. In most applications, the SST would be operated in a common-stop mode, endlessly sampling until it is stopped by a trigger, at which time the preceding samples contain the signal of interest.

The position of the stop may hence be random relative to the start, yet knowing its position remains important in order to delineate the beginning and end of the record.

Another primary advantage of knowing the STOP data is to detect synchronization failures. As discussed in section 1.2.2, out first generation data acquisition system (ATWD chip) suffered from synchronization failures, the engineers defined these failures as “slippage issues”. When the external STOP signal is not synchronized with the SST's clock domain,

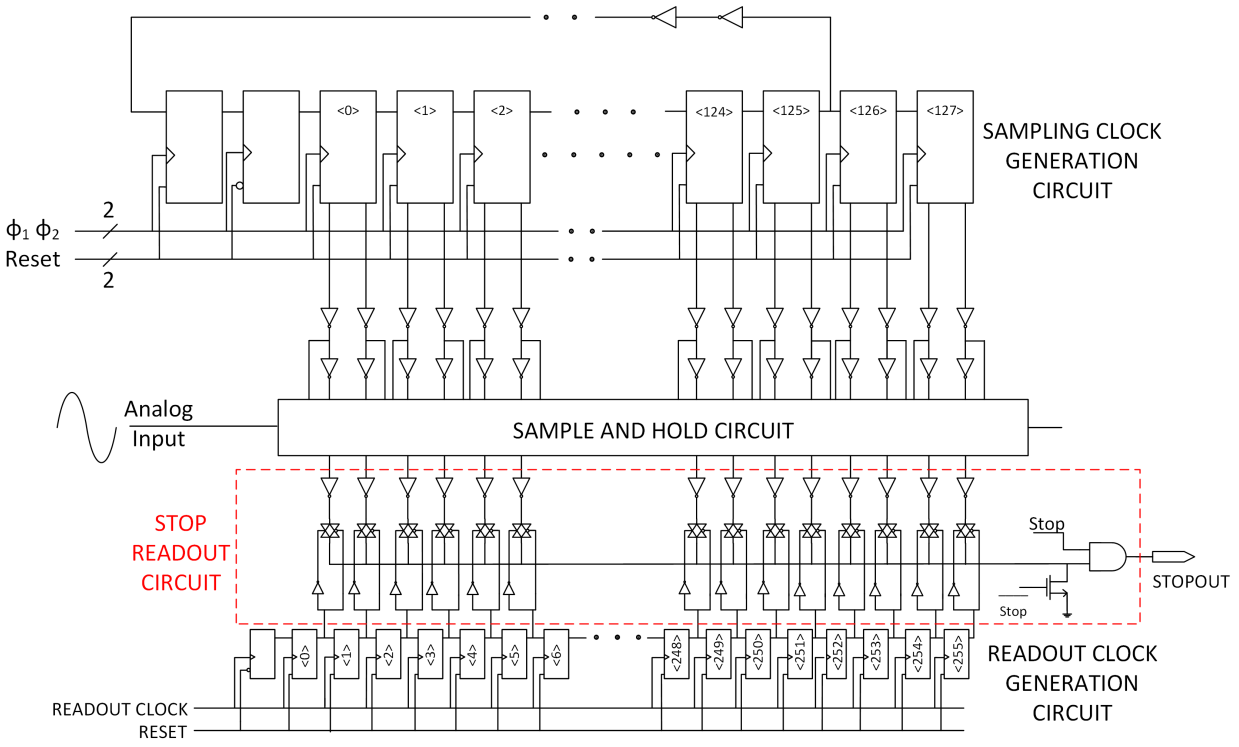


Figure 2.52: Stop Readout Block Diagram

the external STOP goes into metastability and the sampling clocks become unpredictable. Unfortunately for the ATWD chip, there was now way of knowing the status of the sampling clocks. To overcome this issue, the SST chip is equipped with sampling clock-position readout circuit or stop-position readout circuit. The synchronization failures can be detected by looking at the width of the STOP-data (pointer) pulses. STOP-data pulses $\neq$2 bits wide proves synchronization failures, the corresponding analog sample is discarded. Detailed discussion on synchronization failures are presented in section 3.3.7

Chapter 3

Test results - $0.25\mu m$ SST Chip

The performance specifications and functional test results of the SST are specified in this chapter. The following sections in this chapter describe the manufacturing and packaging details of the SST chip. This chapter also describes the functionality test board and the data acquisition board manufactured for the ARIANNA experiment. Testing methodologies and measurement results are described. Specific measurements include: sampling rates, bandwidth, voltage fixed pattern noise, system stability, timing fixed pattern noise, voltage gain and trigger sensitivity.

3.1 Manufacturing and Packaging

The SST was manufactured through MOSIS Integrated Fabrication Service, operated by the University of Southern California's information sciences institute [3]. The design was made using the TSMC (Taiwan Semiconductor Manufacturing Company Limited) $0.25\mu m$ Mixed-mod MS G ICs. A total of 240 chips were manufactured and 40 of those chips were packaged inside a 56 pin 8mm x 8mm Open Cavity Plastic - Quad Flat No-leads Package

(OCP-QFN).

The chip was functional right out of the box and all the basic tests were conducted successfully. A test board and a Data Acquisition Board (for the ARIANNA) were designed and the results from both the boards are presented in the following sections.

Figure 3.1 shows the picture of a manufactured SST die. The size of the die is $2500\mu m$ by $2500\mu m$.

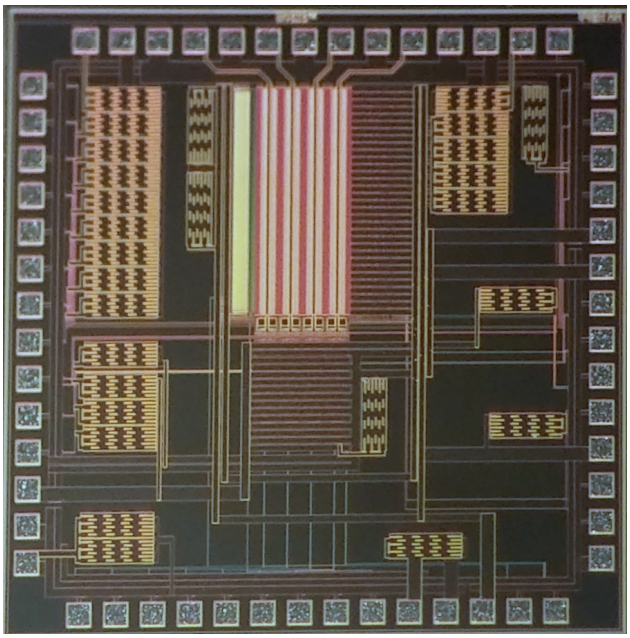


Figure 3.1: Picture of the Manufactured SST die. The size of the Die is $2500\mu m$ by $2500\mu m$

3.2 Testing Platform

To verify the functionality of the SST, a small test board was designed and manufactured. After we verified the functionality of the SST, a "Data Acquisition Board" was developed for the ARIANNA experiment. Both the boards are presented in the subsections below.

3.2.1 Functionality Test Board

A 4 layer printed circuit test board was designed and fabricated to facilitate the initial testing of the SST. The test board was fabricated through ExpressPCB. The test board is $6.5cm$ wide and $9.5cm$ long and the layout of the test board is shown in the appendix. The top and bottom layer is used for signal routing, the second layer is the ground layer and the third layer is used as the power layer. The test board is shown in Figure 3.2.

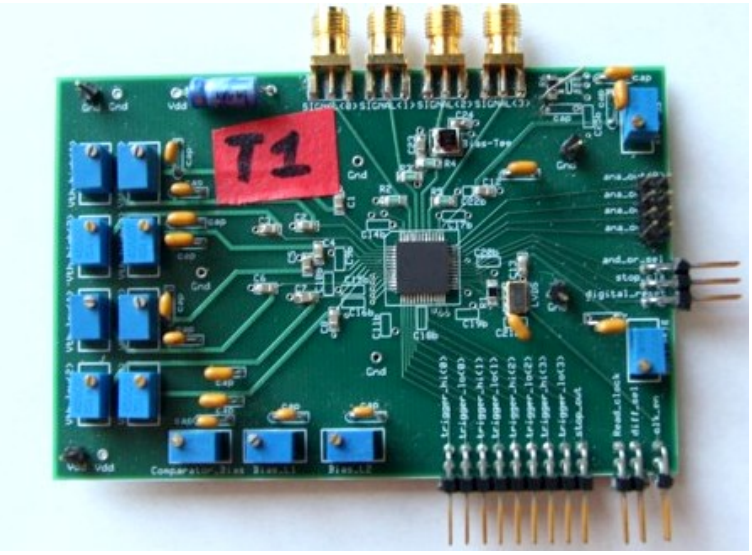


Figure 3.2: Picture of the SST Test Board: Constant Sampling Frequency

A great care was taken to minimize the loss and parasitics. The traces that carry high speed signals are kept very short (e.g., trace from the high speed oscillator to the SST), surface mount capacitors are placed very close to the package to reject high-frequency noise on the supply lines, comparator threshold lines and bias lines. Electrolytic capacitors are also added to reject low frequency noise. Through-hole potentiometers are used to tune the current references and also adjust the low and high thresholds of the comparators.

The PCB tracks carrying the analog signals all need to be matched for 50Ω impedance, therefore these tracks need to be designed as transmission lines. A micro-strip line approach was decided upon and the calculations for the PCB tacks are given below. The following

constants were acquired from the manufacturer: The dielectric spacing between the top layer and the inner ground layer is $0.3048mm$ (h) with the dielectric constant of $4.6 \pm 0.2(\varepsilon_r)$. The ExpressPCB software does not allow arbitrary trace widths, the software only allows $0.25mm$, $0.30mm$, $0.38mm$, $0.51mm$, $0.64mm$ and $0.76mm$ trace widths. The calculations shown below are for $w = 0.51mm$.

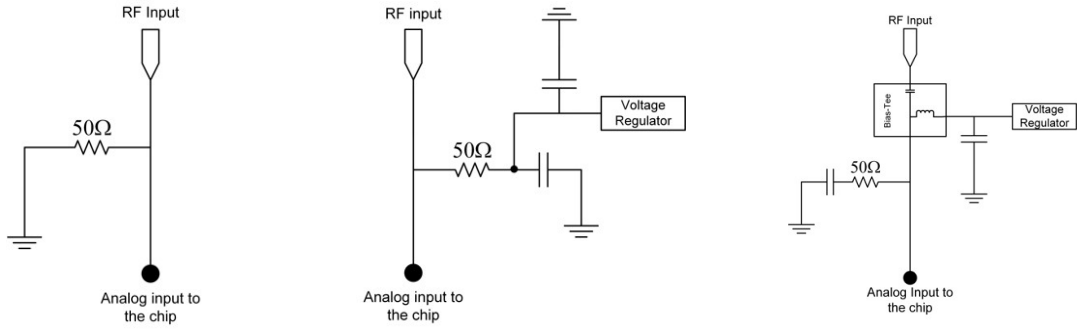
For $\left(\frac{w}{h} > 1\right)$ the effective dielectric constant ε_{eff} was calculated using the formula 3.1

$$\begin{aligned} \varepsilon_{eff} &= \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}}\right]\right] \\ &= 3.43 \end{aligned} \tag{3.1}$$

The characteristic impedance was calculated using the equation 3.2 and it was found to be 53.07 Ω

$$Z_0 = \left[\left[\frac{120\pi}{\sqrt{\varepsilon_{eff}}}\right] \times \left[\frac{1}{\frac{w}{h} + 1.393 + 0.677ln\left(\frac{w}{h} + 1.444\right)}\right]\right] \tag{3.2}$$

The SST has four channels, three different types of input terminations were tested on a single test board: a 50 Ω DC termination, a 50 Ω AC termination and a Bias-tee AC termination was designed on channel 0, 3 and 2 respectively, channel 1 has 50 Ω DC termination. Figure 3.3 shows the schematics for different types of terminations.



(a) 50 Ohms DC Termination (b) 50 Ohms AC Termination (c) Bias-Tee AC Termination

Figure 3.3: Termination

For the normal operation of the SST, five control signals: three active and two passive have to be applied to the SST chip. The three active control signals are read clock, sampling clock reset signal and SST stop signal. The two passive control signals are differential or single ended trigger select signal and AND/OR trigger select signal. A Tektronix DG2020A Data Generator is used to assert and de-assert the control signals. All the comparator thresholds are tuned using potentiometers.

The high speed clock to the SST is given by a 1 GHz oscillator (FXO LC526R -1000). The Fox Electronic XpressO series offers excellent low jitter, stable oscillators. This oscillator was chosen due to the excellent performance, low noise and low cost. The oscillator outputs low-voltage differential signal. Multiple surface mount capacitors are placed close to the power pad of the oscillator to mitigate the high frequency supply noise.

The sampling speed of the SST is decided by this oscillator and it is generally twice the frequency of the oscillator. Driving the clock with the help of an oscillator has it's disadvantages i.e., the sampling speed is constant and therefore the signal capture time. For example, when a 1 GHz clock is applied to the SST, the circuit acquires and reads out 128 ns of the analog input signal, similarly, when a 512 MHz clock is applied, the SST can acquire and readout 256 ns of the analog input signal. To test the SST for different sampling speeds a second test board was populated so that a function generator can be used to drive the clock to the SST. Figure 3.4 shows the picture of this board.

3.2.2 Data Acquisition Board

The functionality of the SST was first tested using the test board designed and presented in the section 3.2.1. A new data acquisition board for the ARIANNA experiment was designed by Anirban Samanta [50]. The design details of the data acquisition board will not be discussed here, a very basic overview of the board is presented.

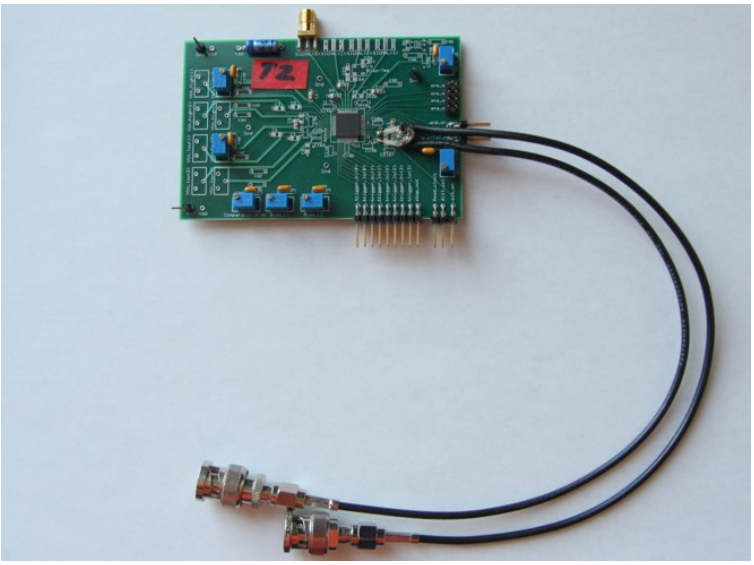


Figure 3.4: Picture of the SST Test Board Variable Sampling Frequency

Figure 3.5 shows the data acquisition board designed for the ARIANNA experiment. The data acquisition board has reduced power usage, remote system measurement capabilities with accurate current and voltage measurements. The board also includes a digital temperature sensor.

Log periodic dipole antennas are used to capture the RF signals in ice. The RF signals are then amplified and passed onto the data acquisition system. Each antenna forms an independent channel which feeds the analog information to the DAQ system. The RF signal is passed through the amplifiers and bias-tee is used in order to bring the incoming signals within the SST's operational limits. The SST continuously acquires the incoming analog signals until a signal of interest is detected. The analog signal is then digitized using ADCs on the system board and passed on to an onboard FPGA, where the incoming digital data is temporarily stored. An ARM Cortex-M3 based MBED microcontroller platform oversees the configuration, communications and housekeeping functions. The MBED controls when the data from the FPGA is collected and stored on the onboard SD card and transmitted over AFAR and Iridium networks back to servers at UC Irvine. The MBED can also control when the system is functional by controlling clock generators and voltage supplies. An SD

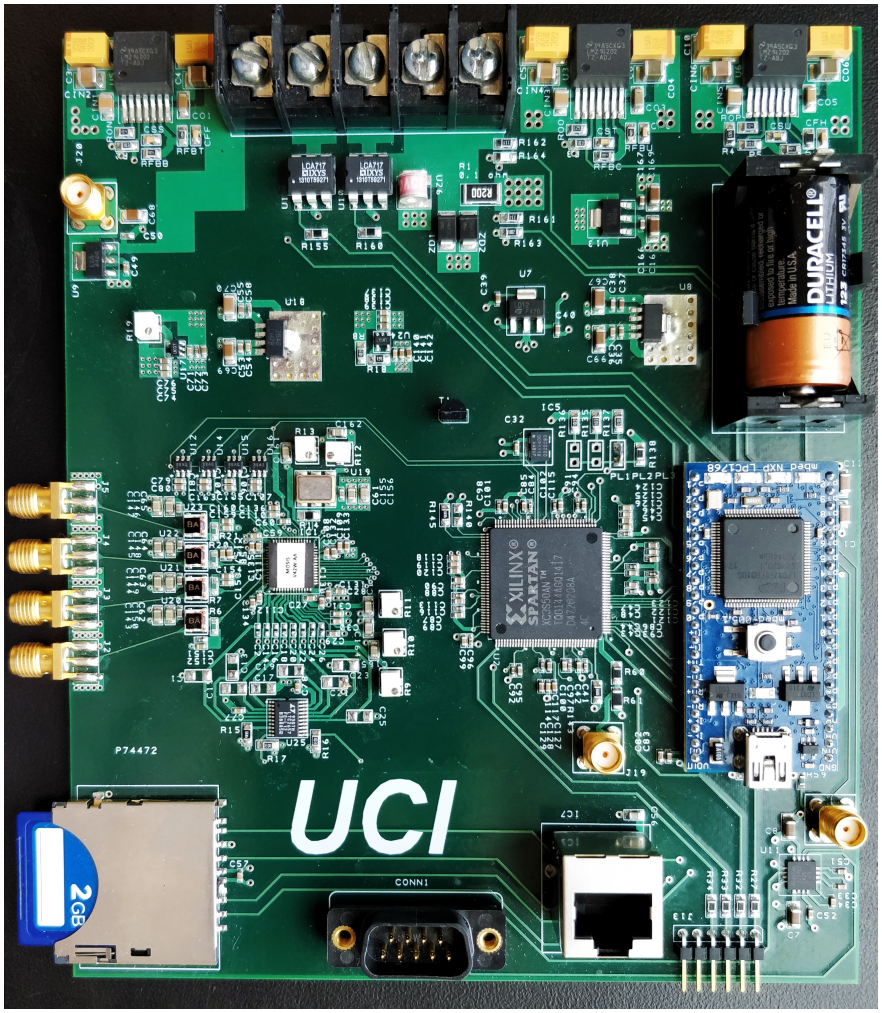


Figure 3.5: Picture of the Data Acquisition Board for the ARIANNA Experiment

card is present to store all the saved waveforms. The system board has Iridium and Wi-Fi communication capabilities.

3.3 Chip Performances

3.3.1 Sampling and Readout

Initial functionality verification of the SST was performed on test boards shown in figures 3.2 and 3.4. The SST has the ability to capture and read out at a wide range of sampling

frequencies. This is demonstrated in the figures 3.6 and 3.7. Figure 3.6 shows a 100MHz sine wave being captured at 2 Giga Samples/s and read out at 1MHz. The sampling clock was generated by an external LVDS oscillator (FXO LC526R -1000).

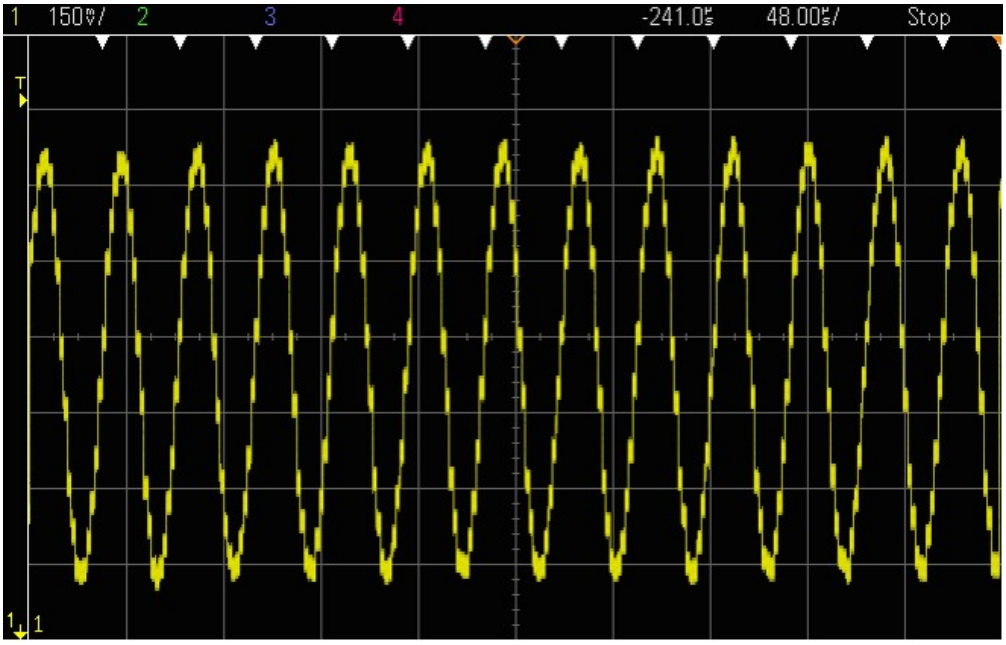


Figure 3.6: SST Analog Readout of a 100 MHz Sine Wave Sampled at 2 GHz

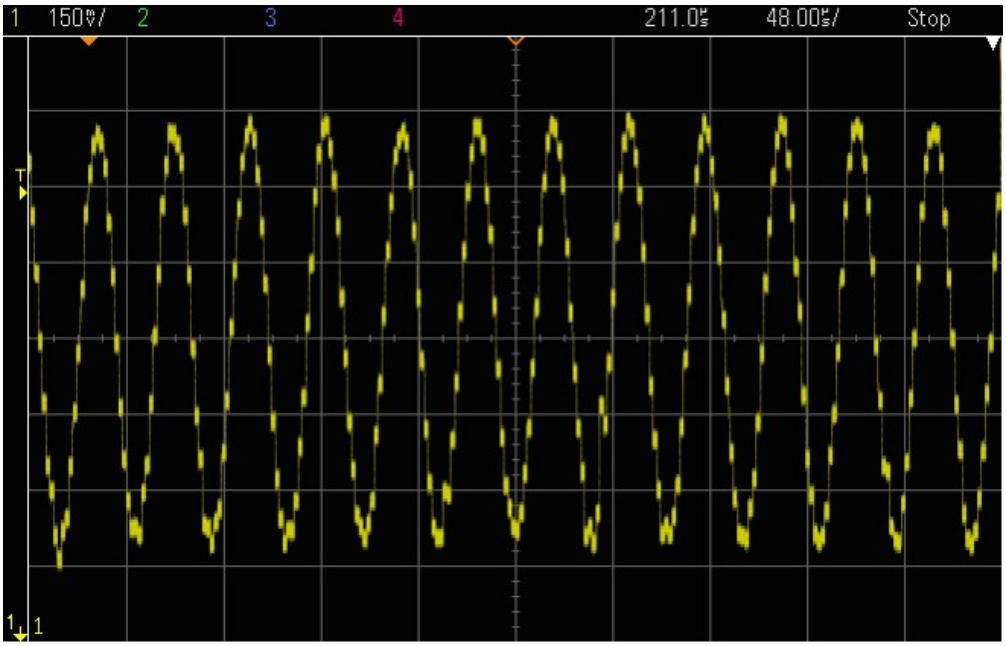


Figure 3.7: SST Analog Readout of a 100 Hz Sine Wave Sampled at 2 kHz

Figure 3.7 shows a 100 Hz sine wave being sampled at an extremely low sampling rate of 2 k samples/s. This was achieved using the test board in figure 3.4, thus demonstrating that the SST achieves an extremely wide range of sampling rates from as low as 2k samples/s to as high as 2G samples/s. Sampling at very low speeds will intensify the leakage of the chip. Leakage can be seen in the figure 3.7 on few outer samples, this is due to very long acquisition time of about 0.128s. In both the figures 3.6 and 3.7 the analog readout is the RAW data without pedestal subtraction. The waveform include noise at 88.9MHz picked up by the oscilloscope probes from KUCI 88.9 FM (UC Irvine's college radio station).

3.3.2 Bandwidth

The bandwidth of the circuit was measured by applying large signal waveforms with varying frequency from an Agilent N5181A MXG analog signal generator and reading out the recorded waveform and measuring the peak to peak of the output signal. The signals were applied to the SST circuit though a Bias-tee circuit centered about 0.9V and AC-terminated at 50 Ohms. The SST recorded the signals at 2 G samples/s. The negative 3dB bandwidth frequency of the SST is measured to be 1.52 GHz. The recorded sine waves was normalized to unity gain at the lowest frequency (100MHz). The gain versus frequency of the SST normalized to 0 dB can be seen in the figure 3.8.

3.3.3 Voltage Fixed Pattern Noise (VFPN) Characterization

The SST chip is prone to "Voltage Fixed Pattern Noise" where each sample has a random offset voltage. The VFPN can be caused by several factors such as process variations and varying offsets in the threshold voltages of the source followers and gain components.

Every transistor used as a switch generates a deviation from the ideal switched capacitor

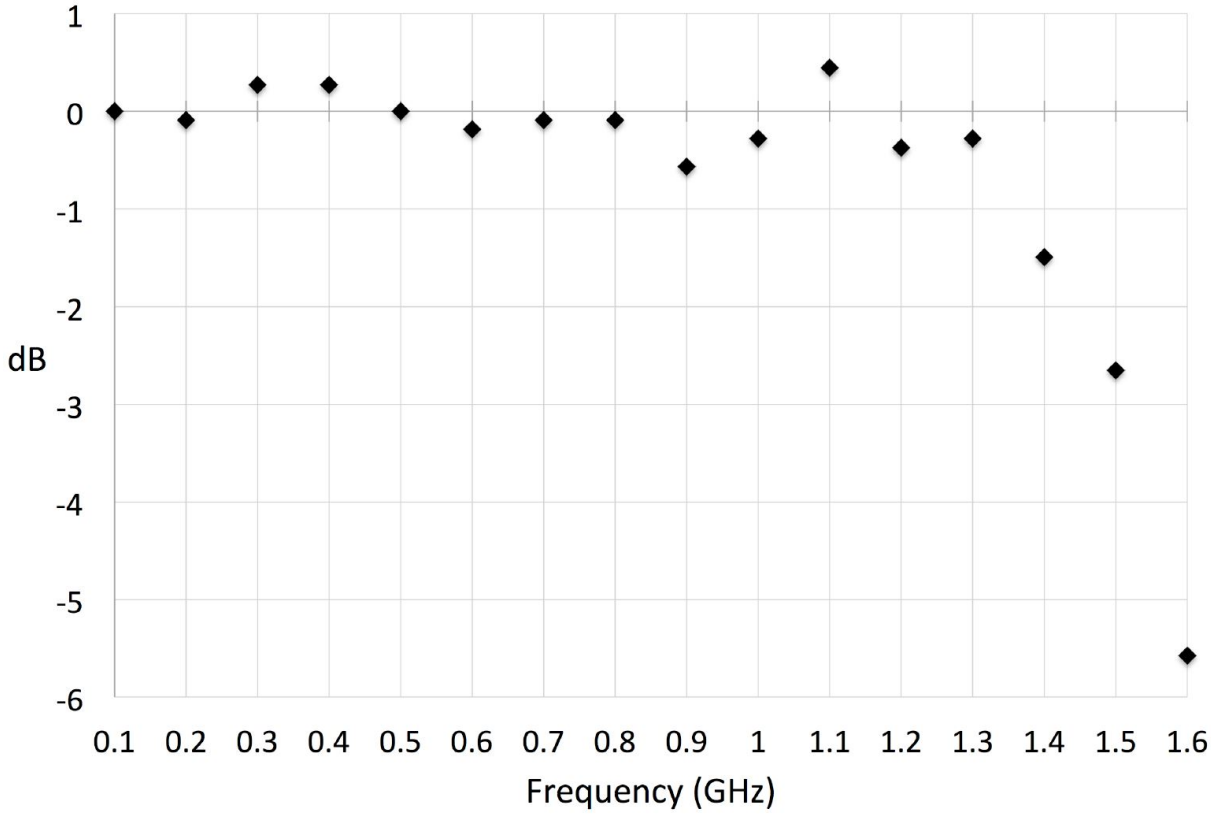


Figure 3.8: Magnitude vs Frequency of the SST

network operation due to its charge injection and finite channel resistance. The absolute charge injected by the switches produces a small deviation in the ideal transistor behavior. The fixed pattern noise is also increased by the readout circuit, i.e., source follower circuit. The error in the analog sampled waveform has two main contributions: sample and hold stage and the source follower stage.

The input analog signal is coupled with the fixed pattern noise which is unique to each sample and contribute to the overall noise of the system. To analyze the VFPN of the SST, a 0.9V DC was applied to the input. The output noise vectors were digitized and averaged. The characteristic VFPN with ∼0.9V DC offset is presented in the figure 3.9.

The distribution of the VFPN is presented in figure 3.10, the standard deviation of the fixed pattern noise for one single channel is $\sim 5.64mV$. The contribution of this VFPN to the

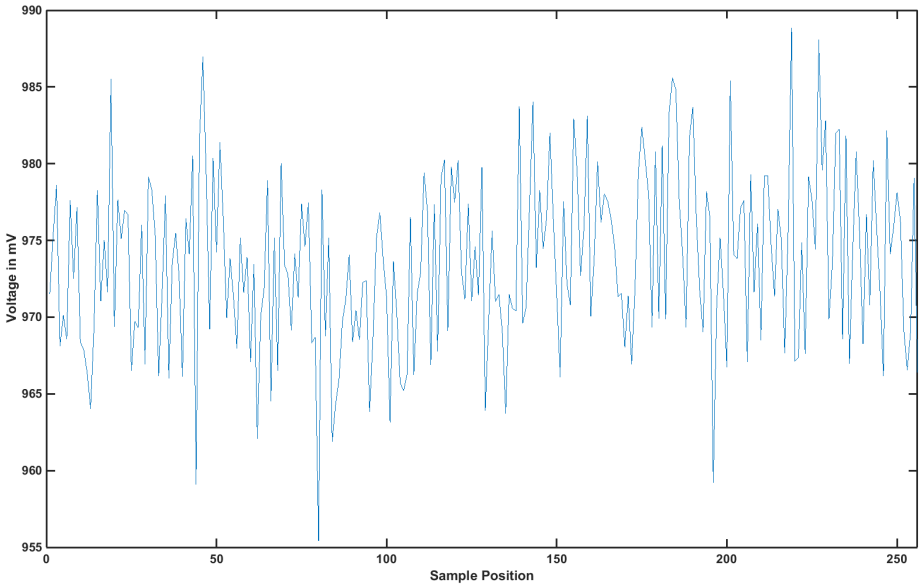


Figure 3.9: Average Voltage Fixed Pattern Noise Measured on a Single Channel 10K Events

analog readout signal degrades the signal to noise ratio and reduces the effective number of bits.

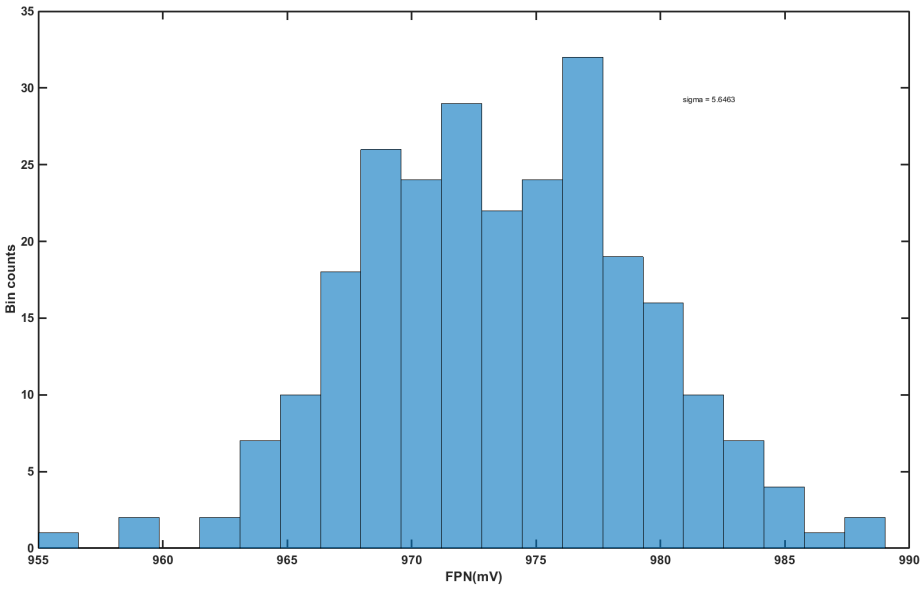


Figure 3.10: Histogram of Average Voltage Fixed Pattern Noise Measured on a Single Channel 10K Events

This VFPN can easily be calibrated out by simple fixed-pattern pedestal correction and cell-to-cell subtraction. The VFPN is fixed for each channel, therefore the noise can be easily calibrated-out post readout and digitization. The characteristic VFPN shown in figure 3.9 is the average of 10K base line voltage measurements. The characteristic VFPN vector represents the cell dependent voltage deviations present in all the analog readout samples. Pedestal subtraction of this vector with the analog readout vector results in the removal of the DC offset and VFPN.

3.3.4 Nosie Measurements

The output noise of one channel of the SST chip is measured by taking the standard deviation of the pedestal corrected DC base line voltages. A single DC base line voltage is recorded and the average VFPN vector, i.e., the VFPN of the same channel shown in figure 3.9 is subtracted. The resulting signal is the output voltage noise shown in figure 3.11. SST displayed excellent FPN performance.

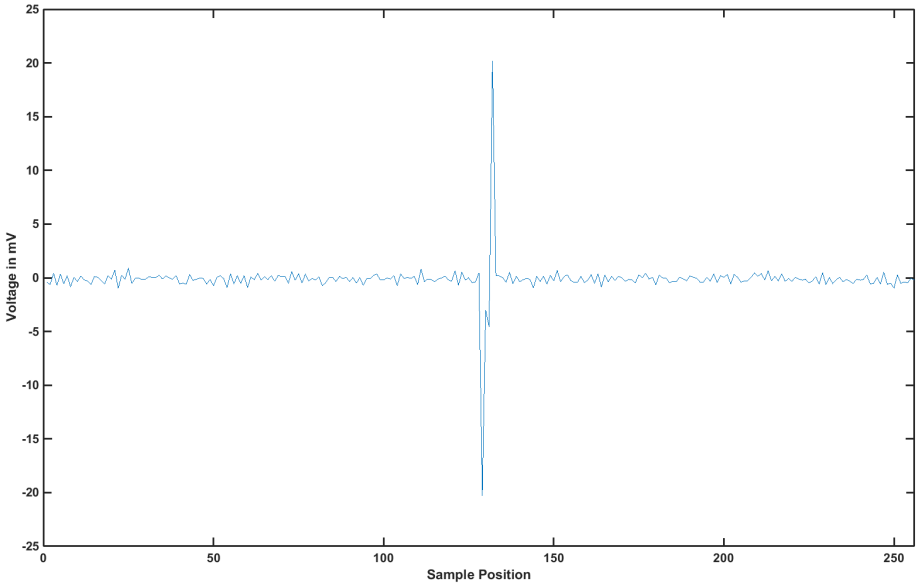


Figure 3.11: Pedestal Subtracted Fixed Pattern Noise

Peak to peak noise of about 1mV and the RMS noise of about 0.39mV can be seen in the pedestal subtracted fixed pattern noise plot shown in figure 3.11. The output voltage range of the SST is about 1.9V, this leads the signal to RMS noise of about 4871:1, which is approximately 12 bits of dynamic range. A stable FPN allows for a simple FPN subtraction, and indicates a well-designed system, making it very easy to analyze the data. The spike at around sample 128 represents the STOP bit and can be ignored. The distribution of the noise is shown if figure 3.12

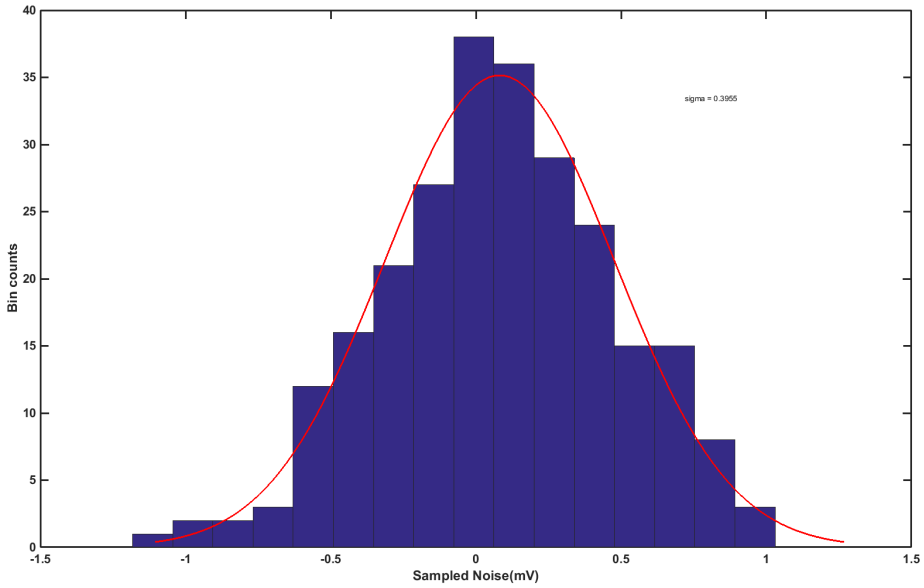


Figure 3.12: Distribution of Pedestal Subtracted Fixed Pattern Noise

A total-system level output noise is $381\mu V$ was measured after external digitization to 12 bits and pedestal subtraction, but with no other filtering and processing. 10 thousand DC baseline voltages were recorded across all four input channels, the distribution of cell-to-cell pedestal subtracted noise is plotted in figure 3.13.

The ADC digitization and post processing adjust the output voltages using correction vectors that have averaged ADC digitized data. Excluding the external 12-bit ADC's quantization noise, the standard deviation of the input-referred noise is 0.4857 mV (RMS).

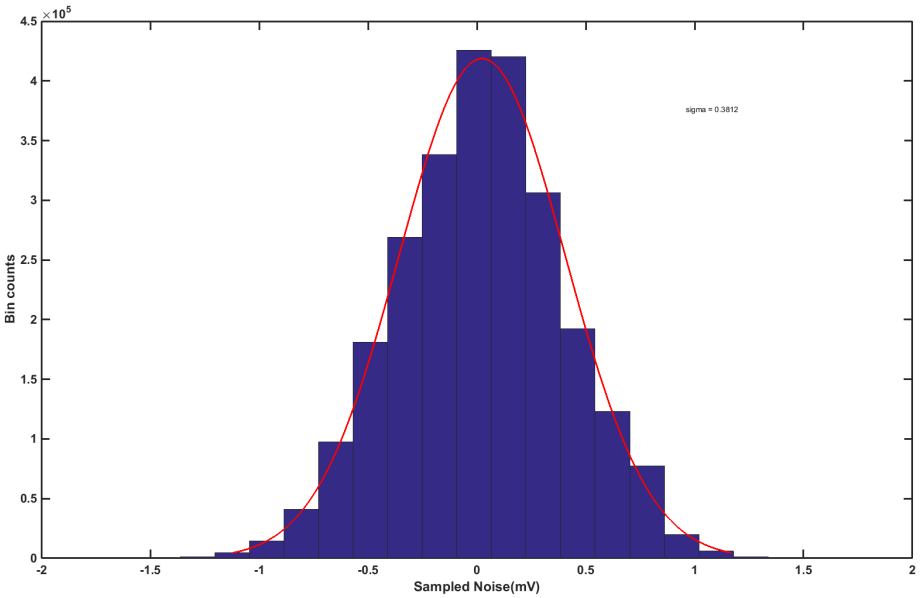


Figure 3.13: Distribution Total SST Noise

3.3.5 Sampling and Digitization

A 100 MHz sinusoidal signal was applied to the data acquisition board from an Agilent N51818A MXG analog signal generator. A plot of the recovered signal is shown in the figure 3.14. The SST sampled the input waveform at 2 GSamples/s and data is readout at 980kHz. The signal was reconstructed in MATLAB. Without pedestal subtraction, FPN is visible in the waveform.

The pedestal subtracted sinewave is plotted in the figure 3.15. A very uniformly-spaced sampling points noted from wave to wave that are indicative of low noise an excellent timing uniformity.

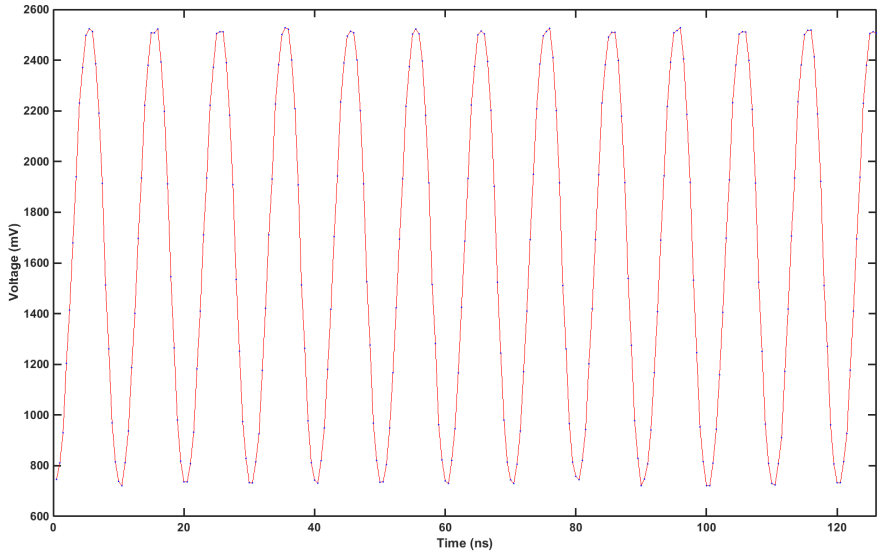


Figure 3.14: Recovered and Digitized 100MHz Sine Wave

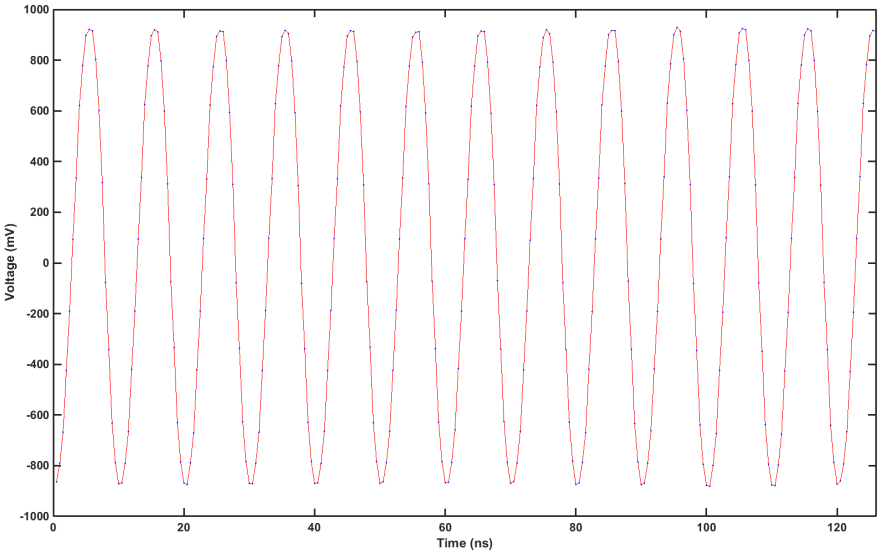


Figure 3.15: Pedestal Subtracted 100MHz Sine Wave

3.3.6 Trigger Sensitivity

The triggering circuity for the SST was designed to be sensitive to small, fast impulsive signals. A high-performance real-time triggering circuit was tested for all combinations for

operating modes discussed in section 2.9.1. The comparator circuit will discern the signal of interest and by comparing the input analog signal and the threshold voltages set by external digital to analog converters (DAC). Each SST channel is equipped with two comparator circuits to check for high or low threshold crossings. For continuous monitoring of threshold crossings, an open loop comparator is used to implement the SST's asynchronous comparator logic.

A $\sim$ 8 mV high, 500 ps full-with half-maximum signal from an Avtech model AVP-AV-1S-P-UCIA pulse generator is applied to the SST. Scope photo showing a trigger stimulus of about 8 mV height and the resulting trigger pulse.

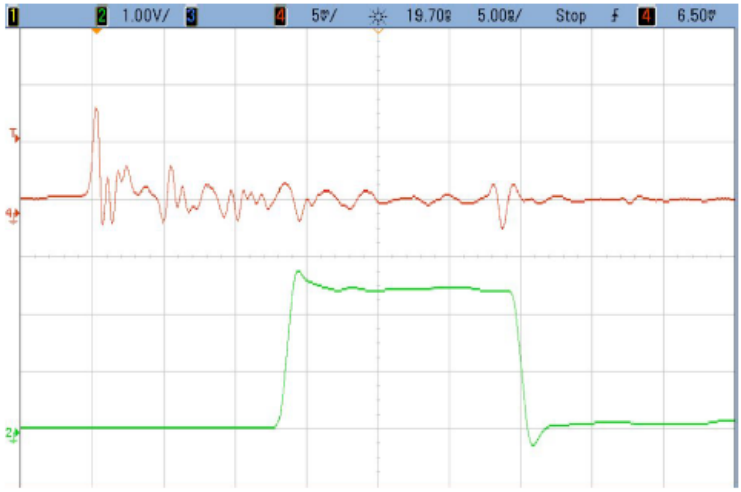


Figure 3.16: Oscilloscope Screenshot Showing the Trigger Sensitivity of the SST Chip

A bias-tee was used to set 0.9V DC offset at the input of the SST. The SST's trigger width was set to differential-ended mode and OR logic, an L1 delay of $\sim$ 2.6 ns and L2 delay of $\sim$ 15 ns was set using external potentiometers. The SST successfully detected the input pulse with a height of $\sim$ 8 mV and 500 ps FWHM. The SST detected events with 100% accuracy for inputs with at least 500 ps FWHM and a minimum height of $\sim$ 8 mV. The delay between the input stimulus and the trigger output is dominated by cable and probe delays. Subtracting the cable delay, the resulting delay (the comparator, pulse stretcher and

output port) of about 2.5 ns.

3.3.7 System Stability (Synchronization Errors)

A well-defined switching of events such as the assertion of the asynchronous STOP into to the SST's clock domain must be imposed for the SST to operate correctly. If this is not the case, the flip-flops might enter metastablility, resulting in the functional failure of the system. The synchronous approach in which the clocks are simultaneously updated based on the asynchronous STOP clock signal is the best way to ensure that the SST operates correctly.

A synchronization circuit presented in figure 2.7 is used in the SST chip. A dynamic pass transistor flip-flop is used to synchronize the external asynchronous STOP to the SST's clock domain. The dynamic pass transistor flip-flop is a non-restoring flip-flip, there is no amplification and the time constant of the latch which is approximately the inverse of the gain is infinity. The SST chip suffers from synchronization failures.

We can detect if the SST entered metastability or failed to synchronize by looking at the sample clock pointers. During the normal operation, two sample clock pointers will move in a circular fashion sampling and storing the analog waveform. If the SST enters metastability, these sample clock pointers can either grow or shrink. The best way to detect synchronization failures is to look at the number of sample pointers which are logic '1'. Events whose sample clock pointers are 2-bit wide did not suffer synchronization failure, however, if the sample clock pointers are anything other than 2-bit wide we conclude that the particular event is erroneous and discard that specific event. The terms "sample clock pointer" and "STOP data" mean the same and are used interchangeably in this dissertation.

The synchronization failure rates of the SST are plotted in the figure 3.17.

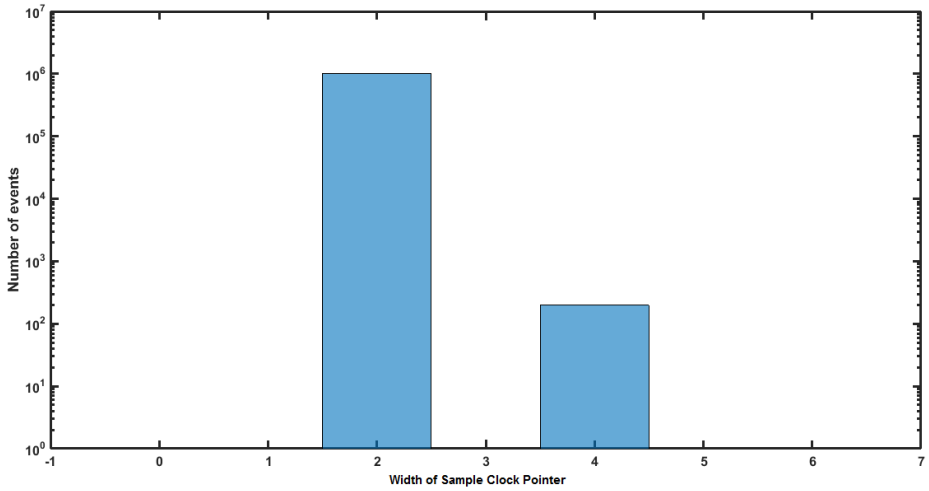


Figure 3.17: Histogram of Sampling Pointer Widths - 1M Events

Readers must note that the y-axis in figure 3.17 is on a semi-log scale. Using the data acquisition board, 1 million events were captured and digitized. The STOP data was read out for all 1 million events. Approximately 200 of the total 1 million events suffered from synchronization failures. For the ARIANNA experiment, we discard the analog samples which has synchronization failures. This data set has 0.02% failure rate.

Setup and/or hold time failures can occur during clocking, however, this has not been found in SST despite 30×10^{15} clocks.

3.3.8 STOP Distribution

Another important study to determine the stability of the system was a study of the stop bits. The stop bits as explained in section 2.11 indicates where the data ends for a particular sample. The position of the stop bit is random relative to the start, however, knowing its position remains important in order to delineate the beginning and end of the sampled record. The presence of stop bits is extremely important for the integrity of the collected data. The position of the STOP is read out in parallel with the analog samples during the

readout phase.

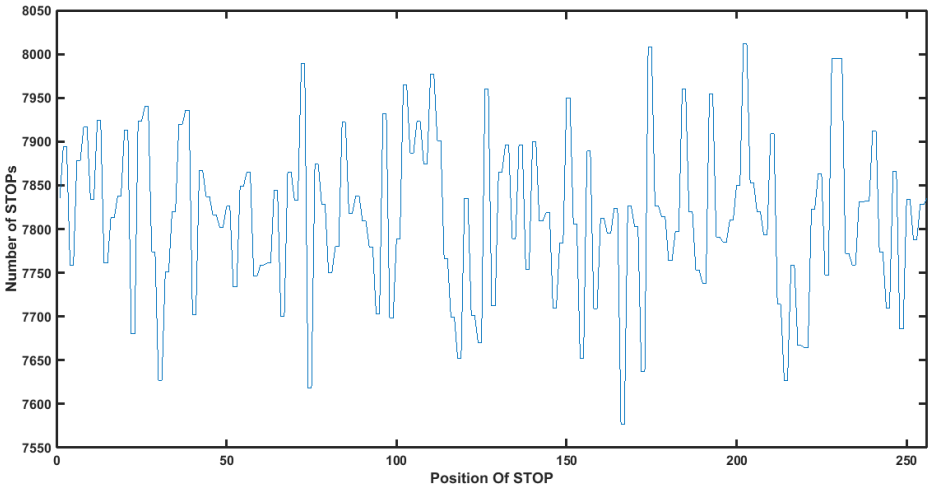


Figure 3.18: Distribution of STOP Positions for 1M Events

Here we are interested in counting the number of occurrences for the STOP bit in a certain region of space i.e., 128 high-speed shift registers. The arrival of STOP signal is independent and random, the distribution of the STOP bits obeys Poisson distribution. Poisson random variable arises in situation where the events occur completely in random time or space [44]. Here the probability mass function for the Poisson random variable is given by

$$P(X = x) = \frac{\lambda^x e^{-\lambda}}{x!} \tag{3.3}$$

The Poisson parameter λ is given by

$$\lambda = \frac{10^6}{128} = 7812.5 \tag{3.4}$$

here, we are counting the occurrences of STOP bit within 128 shift registers for 10^6 events.

Next, we will find the theoretical variance and standard deviation and compare it with

measured data. Expectation of a discrete random variable X is given by

$$E(X) = \sum_{x=0}^{\infty} xP(x) \tag{3.5}$$

$$E(X) = \sum_{x=0}^{\infty} x\frac{\lambda^x e^{-\lambda}}{x!} \tag{3.6}$$

$$E(X) = \mu = \lambda \tag{3.7}$$

The expected value $E[X]$, by itself, provides us with very limited information about X. For example, if we know that $E[X] = 0$, then it could either be, that X is zero all the time or it could be that X is taking extremely large positive and negative values. Here we are not only interested in mean of the STOP position distribution, but also the extent of the STOP position's variation from its mean. The variance of the random variable X is defined as the mean-squared variation

$$Var(X) = E[(X - \mu)^2] \tag{3.8}$$

$$Var(X) = E[X^2] - [E(X)]^2 \tag{3.9}$$

where

$$E[X^2] = \lambda^2 + \lambda \tag{3.10}$$

therefore,

$$Var(X) = \sigma^2 = \lambda \tag{3.11}$$

Sample theoretical standard deviation is given by

$$\sigma = \sqrt{\lambda} = \sqrt{7812.5} = 88.388 \tag{3.12}$$

Figure 3.19 plots the histogram of the distribution of STOP positions for 1 million events.

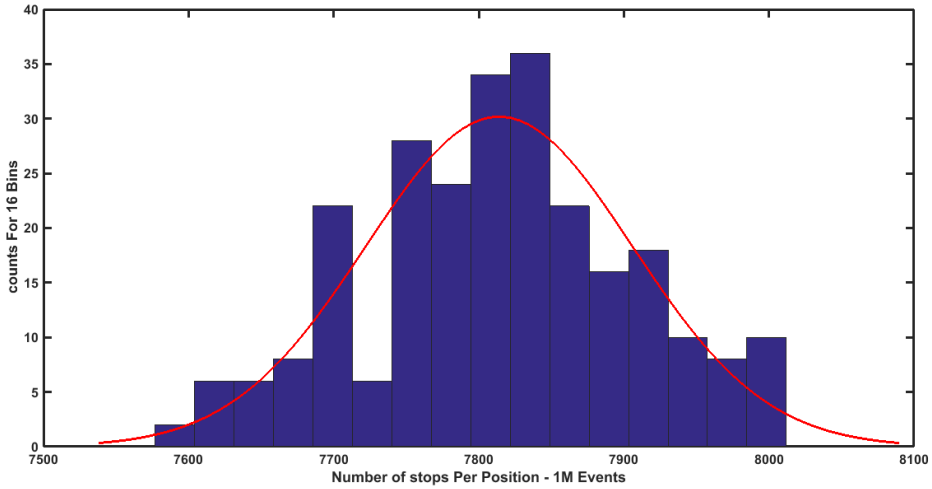


Figure 3.19: Histogram of STOP Position Distribution

From the plot, variance is found to be 8462.068 and the standard deviation σ is 91.9895 events. This values matches closely with the theoretical calculations.

3.3.9 Timing Fixed Pattern Noise

A zero crossing method discussed in the section 5.1 is used to measure the cell-to-cell sample interval non-uniformity of the SST. Figure 3.20 plots the cell-to-cell sampling interval deviation from the nominal 500 ps. The RMS of the fixed pattern sampling timing non-uniformity is measured to be 30.39 ps. The timing FPN has two distinct features, the alternating, i.e., "ODD/EVEN" pattern across all the samples and the large spike at sample position 251-252.

The "ODD/EVEN" pattern reveals a binomial distribution in the SST's timing FPN. The binomial distribution is plotted in the figure 3.20. The "ODD/EVEN" timing effects are caused due to asymmetry in the sampling clock tracks and/or duty cycle variations in the external oscillator. Deviation in the duty cycle from 50% will cause variations between adjacent sampling clocks since SST uses both phases of external clock to generate the sampling

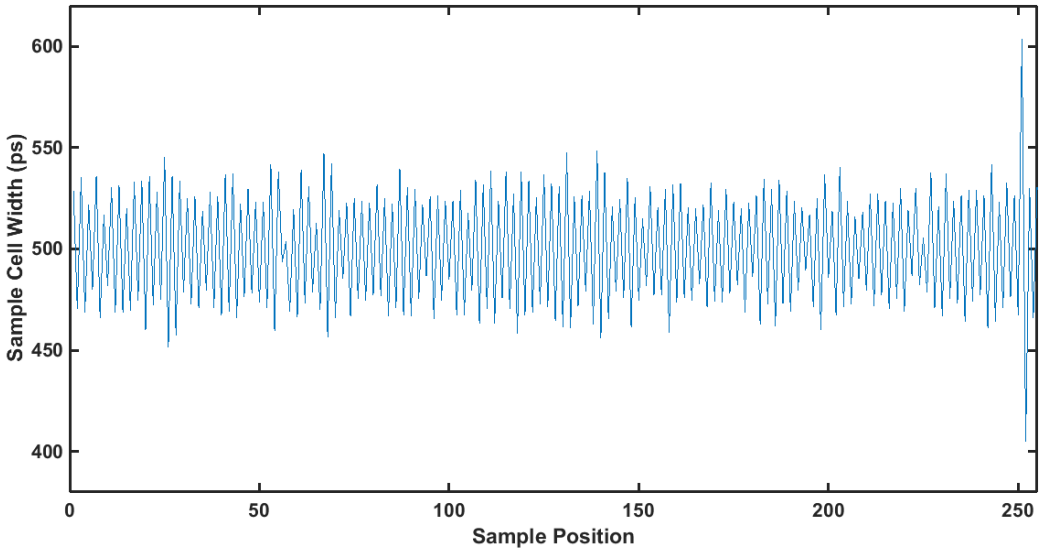


Figure 3.20: Fixed Pattern Cell-to-Cell Sample Interval Non-Uniformity

clock. The mismatches in the clock distribution circuitry will also cause the "ODD/EVEN" fixed pattern to prevail, for e.g., uneven rise and fall times will translate into unequal HI and LO times resulting in the duty cycle to deviate from 50%. However, most notable contributor to the "ODD/EVEN" fixed pattern timing error is the sampling clock generation shift registers.

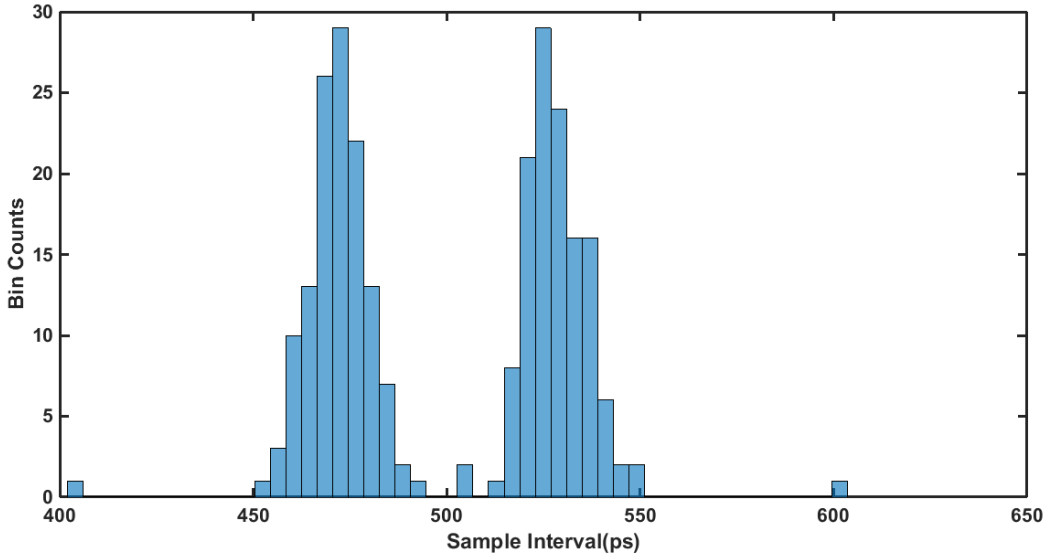


Figure 3.21: Histogram of Cell-to-Cell Sample Interval Non-Uniformity

The second distinct feature, i.e., the large spike at the sample position 251-252 is due to uneven loading of feedback registers. 128 high speed shift registers are connected in circular fashion to generate the sampling clocks for the SST. The feedback registers have additional buffering to drive the clock all the way to the front of the registers, the buffering circuit introduces additional capacitive loading causing large sampling time fluctuations. More detailed explanation and the suggested design modification is presented in section 4.3.1.

3.3.10 Timing Resolution Measurements

Work related to timing resolution measurements was done by my peer Edwin Chiem in the ARIANNA engineering team. Detailed explanation about the timing tests are presented in his dissertation [19]. The results of the timing tests is briefly discussed in this section.

There are two components of timing resolution, the SST's ability to measure time differences among different channels and how accurately the recorded event can be reconstructed. The first measurement - "Intra Channel Timing Test" measures the period variations among the recorded sine waves. This measurement depends on the input frequency and amplitude. The best results for intra channel timing measurements are got when large input amplitudes (1.6V) are supplied. The standard deviation of the intra channel timing tests for uncalibrated measurements and the timing results with zero-crossing and simulated annealing calibrations methods are shown in the table 3.1. The results of four different input frequencies are presented.

Table 3.1: Intra Channel Timing Test (Period Error) for various Node Frequencies

Frequency	No Timing Corrections	Zero Crossing	Simulated Annealing
100 MHz	9.640 ps RMS	5.768 ps RMS	5.826 ps RMS
125 MHz	9.238 ps RMS	3.955 ps RMS	4.028 ps RMS
200 MHz	8.997 ps RMS	3.034 ps RMS	3.061 ps RMS
333.333 MHz	8.690 ps RMS	2.210 ps RMS	2.300 ps RMS

The results of the intra channel timing test tell us that the SST can accurately capture timing features on a single channel within 2.21 ps (RMS) error rate. This timing resolution is obtained under favorable conditions of frequency and amplitude.

The second component of the timing resolution is the accurate measurement of time delay between multiple channels. This timing resolution is more important for the ARIANNA experiment, since it helps us to accurately measure the arrival times of the neutrino signal. The inter channel timing tests are measured using 1.2V P-P bipolar pulses with 10 ns period. The inter channel timing tests were performed for different delays and the results are presented in table 3.2. Similar to intra channel test, the results of uncalibrated measurements, timing results with zero crossing method of timing calibrations and timing results with simulated annealing timing calibrations are presented here.

Table 3.2: Inter Channel Timing Test (Delay Uncertainty) for various Delays

Dealy	No Timing Corrections	Zero Crossing	Simulated Annealing
0 ns	1.15 ps RMS	1.15 ps RMS	1.15 ps RMS
3.79 ns	2.68 ps RMS	2.35 ps RMS	2.26 ps RMS
12.33 ns	3.62 ps RMS	2.32 ps RMS	2.29 ps RMS
24.42 ns	3.59 ps RMS	2.33 ps RMS	2.29 ps RMS
60.74 ns	4.29 ps RMS	2.36 ps RMS	2.36 ps RMS

The SST achieves its best resolution of 1.15 ps (RMS) at 0 ns delay. With timing corrections, the inter channel resolution remains practically flat at around $\sim$2.32 ps (RMS) across all non-zero delays up to 60 ns delay. This indicates that there is no significant drifting in the sample interval errors across the sampling array, and that the interval errors maintain centered about a zero mean.

3.4 Summary of Chip Performance

Table 3.3: Chip Performance

Parameter	value
Technology	0.25 m CMOS, 2.5V
Samples per channel	256
Number of channels	4
Chip size	2.5 by 2.5 mm
Package size	8 mm by 8 mm
Input clock (typical)	1 GHz LVDS
Sample rate(typical)	2 GHz
Minimum sample rate	$\sim$2 kHz
Analog bandwidth	$\sim$1.5 GHz, -3dB
Max power per chip with trigger	160 mW at 2 GHz
Analog input range	0.05-1.95 V
Input-referred temporal noise	$\sim$0.42 mV RMS
Analog dynamic range	12 bits, RMS
Fixed pattern noise	$\sim$6.5 mV RMS
Trigger	Bipolar, AND/OR, windowed
Trigger sensitivity	$\sim$1 mV RMS
Trigger bandwidth	$>$600 MHz
Trigger outputs	Differential, dual single-ended
Trigger output voltage	0.8V, 1.2V or 2.5V CMOS
Intra-Channel Period timing test: Uncorrected	9.3 ps σ
Intra-Channel Period timing test: FPN corrected	2.1 ps σ
Inter-Channel Split-Pulse timing test: Uncorrected	1.15 - 4.3 ps σ
Inter-Channel Split-Pulse timing test: FPN corrected	1.12 - 2.37 ps σ

Part II

Prototype Synchronous Sampling and Triggering Circuit (SST0.18μ)

Chapter 4

Synchronous Sampling and Triggering Prototype Circuit

This chapter presents the work on the synchronous Sampling and Triggering Prototype Circuit (SST0.18μ). The prototype chip was designed and developed for experimental purposes in 0.18μm IBM technology. Apart from the obvious change in technology, few design changes were made to the 0.18μm chip. The prototype chip has increased depth of sampling cells, better synchronization circuitry and reduced fixed pattern timing noise. This chapter presents all the design changes and the performance improvements.

4.1 Technology Used

The SST0.18μ chip is fabricated using the 0.18μm RF CMOS design kit provided by IBM Foundry and Manufacturing Services. The details of the characteristics and performance of these technologies are confidential. Publicly available information about the process properties and fabrications options are briefly discussed in the next sub section.

4.1.1 The 0.18μm RF COMS Process

The SST0.18μ chip was fabricated using the IBM 0.18μm RF CMOS process. This process is also called as CMOS7RF. The CMOS7RF process offers highest integration density up to 118kGates/mm^2 at up to 7 levels of metal, supply voltages from 1.8V to 5V and ESD protection cells with up to 8 kV HBM level.

The NFETs are formed in the p-type substrate within a p-well. CMOS7RF supports six NFETs. The standard NFET operates at 1.8V, an optional 1.8V high-Vt is also supplied. Three optional high voltage NFETs are provided for 2.5V, 3.3V and 5.0V operation. The standard NFET has an effective gate oxide thickness of 3.5 nm and a minimum channel length of 0.18μm. Similar to NFETs CMOS7RF also supports six PFETs, nominal PFET for 1.8V, an optional 1.8V high Vt, 2.5V, 3.3V and 5.0V operation. The MIM capacitors have two options, standard or HD. The capacitor metal top plate (AM) is separated from the MT metal level bottom plate by a thin nitride. The nitride can either by standard (standard MIM) or high density (MIM-HD). The capacitance density is 2.05 fF/μm^2 for MIM and 2.70 fF/μm^2 for MIM-HD. The CMOS7RF process provides three standard resistors. The standard resistors are n+ and p+ single-crystal (sometimes called "diffused" resistors) formed from unsilicided junctions from the standard FET process, and a p-type unsilicided polysilicon resistor over shallow trench isolation.

4.2 Overview of SST0.18μ Chip

During 2015/16 academic year, ARIANNA engineering team delved into re-designing the SST in 0.18μm technology. The main motivation was to explore the capabilities of IBM 0.18μm technology and to experiment with scaling down the design of the synchronous sampling and triggering circuit. The power supply voltage for the IBM 0.18μm technology is

1.8V and it allows for shorter transistor gate length and feature size compared to the $0.25\mu m$ technology. Comparing to $0.25\mu m$ technology, $0.18\mu m$ technology has higher transconductance parameter K'and the nominal threshold voltage of 0.35V compared to 0.43V for $0.25\mu m$ process. The core functionality and the circuit operations of the SST0.18μ is basically same compared to the $0.25\mu m$ SST. With the migration to newer technology and reduction of parasitic capacitance, the performance in speed and timing was greatly improved for the SST0.18μ. The sampling array depth of the 4 channel SST0.18μ was increased to 512 samples per channel, all the while maintaining 1.2 GHz of -3 dB bandwidth.

Figure 4.1 shows the architecture of the SST0.18μ circuit. The basic architecture is very much similar to the $0.25\mu m$ SST chip, few design changes were made to the blocks greyed out in the figure 4.1. An array of 512 track and hold cells are responsible for storing samples of the input signal. The sampled signals are stored as voltages across the cell's 62.8fF MIMs sampling capacitor. The SST0.18μ performs continuous sampling by circularly rotating through the array and overwriting previous samples once the end of the array is reached. Nominally the SST0.18μ operates with the sampling rate of 3.0 Gsamples/second. At 3.0 Gsamples/s sampling speed, the entirety of the 512 sampled voltages results in a 170.67 ns record length. To achieve the continuous and precise sampling over long periods of time, the sampling clocks is generated by two sets of tightly interleaved high speed sample clock shift registers.

The clocking for the high speed shift registers is provided by an off chip LVDS oscillator. An on chip LVDS receiver block receives this low voltage differential clock signal from an off chip oscillator and converts it to a rail to rail (0V-1.8V) CMOS logic levels. It is designed for a nominal common mode voltage of 1.25V but supports a common mode input range 1.0V to 1.6V. The LVDS receiver functions for an input with 350mV peak to peak or greater. A four phase non overlapping clock generator circuit synchronizes the external LVDS clock and converts the single phase external clock to a non-overlapping four phase clock. The four

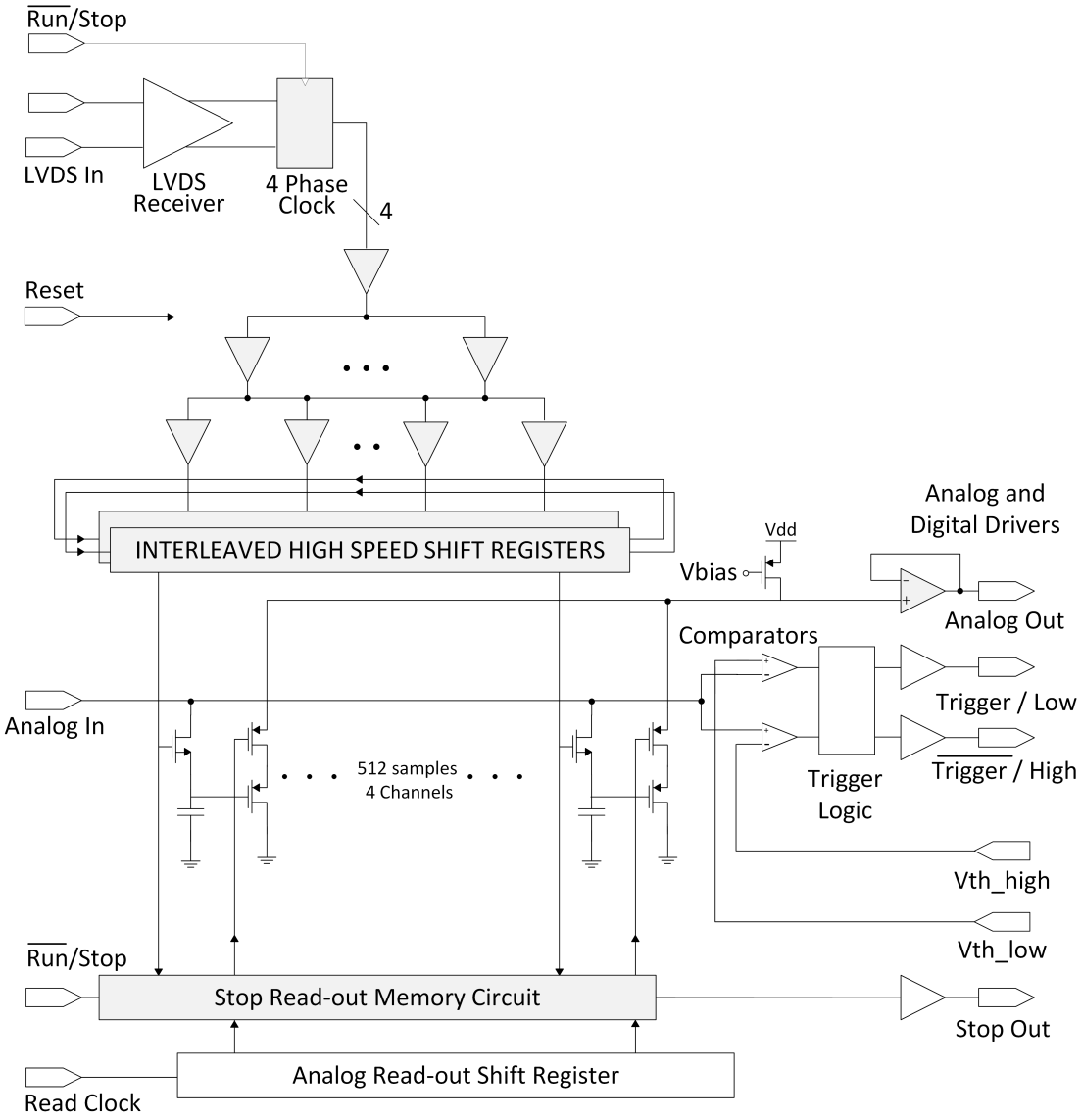


Figure 4.1: 0.18μm Synchronous Sampling and Triggering Prototype Circuit Block Diagram

phases of the clock is distributed to the tightly interleaved high speed shift registers via a symmetric clock distribution network.

Each channel of the SST0.18μ has a set of comparators to determine if the input signal exceeds a high threshold or falls below a low threshold. The high and low thresholds are set with analog voltages applied to input pins on the chip. An event trigger signifies a signal of interest has occurred and the event trigger can be set to check for various comparators output logic combinations.

A simple Active Pixel Sensor-type readout scheme was employed, using P-channel switched source-followers to match the sampled input range. The analog readout circuit consist of an external clock driver circuit which drives 512 static shift registers which in turn distribute the clock to source followers.

Similar to the $0.25\mu m$ SST, direct readout of sampling pointer's position is available. The sampling clocks for the SST0.18μ is generated by two sets of tightly interleaved 512 high speed dynamic shift registers. A D-latch based stop readout circuitry was implemented to store and readout the sampling clock pointer positions during the readout phase of the SST0.18μ.

4.3 Analog and Mixed Signal Circuit Blocks

This section presents some of the analog and mixed signal circuit blocks used in the SST0.18μ. This section focuses on the design changes that were performed for the SST0.18μ chip. The rationale behind these design changes are also discussed in subsequent sections.

4.3.1 Sampling Clock Generation

The general description of the Sampling clock generation circuit is presented in section 2.7. With respect to functionality, the sampling clock generation circuit of the SST and the SST0.18μ are same. The high speed sampling clock generation circuit is also called the High speed dynamic shift registers, both terms are used interchangeably in this text. Dynamic shift registers are arranged in circular fashion, where a single pointer "1" is cycled through to sample the waveform. The $0.25\mu m$ SST chip consist of 256 samples per channel and for these 256 samples, 128 dynamic master-slave shift registers were connected in circular fashion to generate the sampling clock. The sampling clocks are generated by both master and slave

flip-flops. Figure 4.2 shows a segment of the sampling clock generator circuit (Master-Slave Shift Register) where the sampling clocks ψ_{N-1} and ψ_N are generated. Ideally the sampling

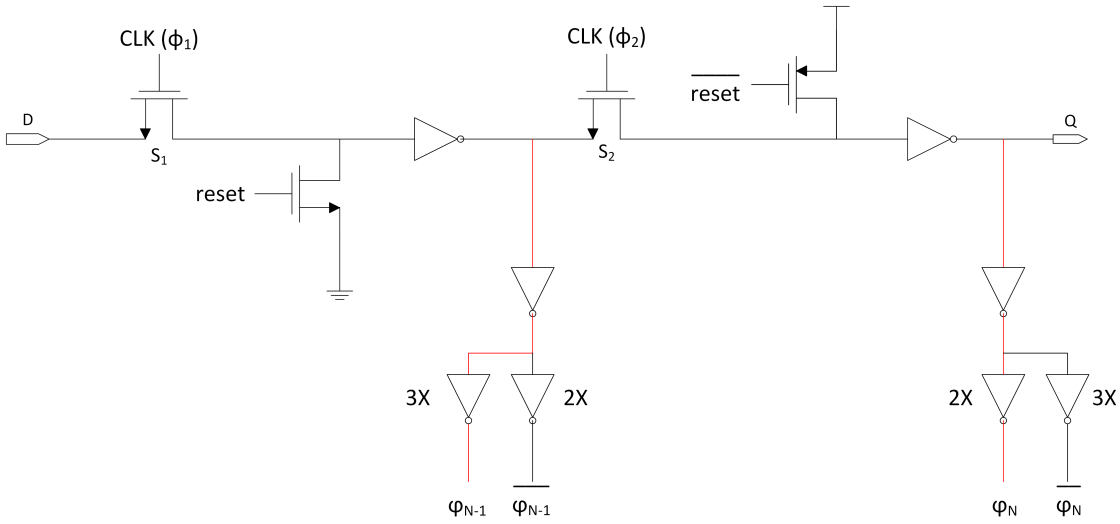


Figure 4.2: Sampling Clock Generation Circuit of the $0.25\mu m$ SST Chip, Showing Asymmetric Sampling Clock Paths

interval for all clocks, ψ_1 to ψ_N is given by

$$T_{Sample} = \frac{1}{2 \times f_{osc}} \tag{4.1}$$

where f_{osc} is the high speed oscillator frequency. For the ARIANNA experiment, $f_{osc} = 1GHz$, therefore $T_{Sample} = 500ps$. In reality, a fixed pattern timing jitter appears on top of the sampling interval. The fixed pattern timing jitter over the sampling interval can be attributed to duty cycle variations of the external oscillator, device mismatches due to process variations and the mismatches in the sampling clocks. Although, all the former variations contribute to the fixed pattern timing jitter, the latter contributes the most. The mismatches in the sampling clocks paths can be seen in the figure 4.2 (clock paths shown in red). ψ_{N-1} and ψ_N are the sampling clock signals to the two adjacent sample and hold circuit. The buffer delay for ψ_{N-1} is $4\times$ whereas the buffer delay for the next clock ψ_N is $3\times$. In addition to this, uneven rise and fall times in the switches will translate into variations between adjacent sampling clock. NMOS switches used in the high speed shift

register can potentially pile on to the "ODD/EVEN" sample interval variations. 128 of these high speed shift registers are connected in circular fashion, every alternating sampling clock has this "ODD/EVEN" sampling clock timing differences. Despite equalization of these inverters, the manifestation of this ODD/EVEN sampling clock differences can be seen in the simulation plot shown in figure 4.3.

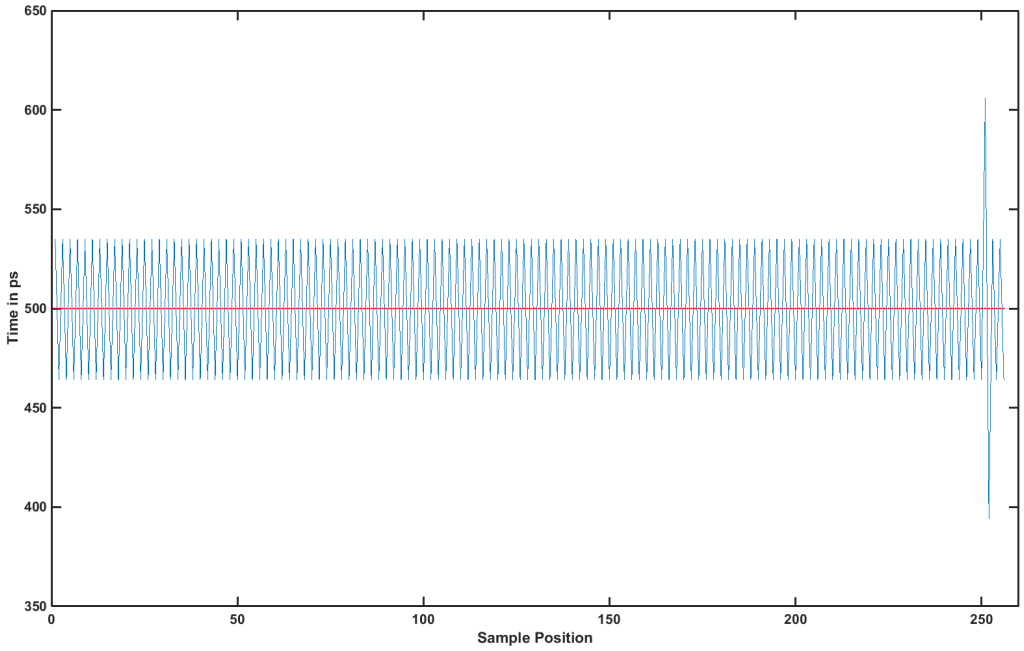


Figure 4.3: Simulation of Fixed Pattern Timing Non-Uniformity due to High Speed Shift Registers of the $0.25\mu m$ SST Chip

The fixed pattern timing non-uniformity has two features, "ODD/EVEN" effects explained above is the first feature, the second feature is the spike in the sampling positions 251 and 252. This large spike is attributed to the feedback node of the circular high speed shift register chain. The shift register that feedbacks the sampling clock pointer has additional capacitive loading. This additional loading introduces additional time delays to the feedback nodes and can be seen in the figure 4.3. The red line at $500ps$ is the nominal sampling time interval for $f_{osc} = 1GHz$.

4.3.1.1 Design Changes for SST0.18μ Sampling Clock Generation Circuit

The major advantage of moving to newer technology is the reduction in the parasitic capacitances, this improves the performances of the SST0.18μ in terms of speed and timing. The SST0.18μ chip consist of 4 channels and 512 samples per channel. A new sampling clock generation circuit was developed to eliminate the deterministic sampling time non-uniformity which is evident in the 0.25μm SST chip shown in figure 4.3. The architecture of the new sampling clock generation circuit is very different from the 0.25μm SST chip. The two distinct features seen in the fixed pattern timing non-uniformity are the alternating "ODD/EVEN" pattern among the sampling intervals and the large timing fluctuation in the timing interval due to the feedback node. The first notable feature (ODD/EVEN) is eliminated by using two sets of tightly interleaved high speed sampling clock shift registers instead of using both stages of the master-slave shift register. This design feature can be seen in the figure 4.4, the two adjacent clock paths highlighted in red have matched buffering and hence equal delay. The second notable feature (large fluctuation at the feedback node) is eliminated by balancing the loads on every shift register regardless of whether it is used as a feedback node or not. This design feature can also be seen in figure 4.4, the dummy inverters after the master stage of the dynamic shift registers is used for load balancing. Further layout optimizations can be made to reduce the random stochastic timing jitter.

Figure 4.4 shows one interleaved block of the high speed sampling clock generation circuit. Other than the architectural difference, the SST0.18μ's sampling clock generator uses transmission gates as switches as opposed to NMOS switches for 0.25μm SST. Using transmission gates help us to keep the rise and fall times constant, and therefore reduces the possibility of "ODD/EVEN" non-uniformity.

The switches shown in figure 4.4 are transmission gates. The transmission gates are designed to act as voltage-controlled switches. The transmission gate is nothing but a NMOS and

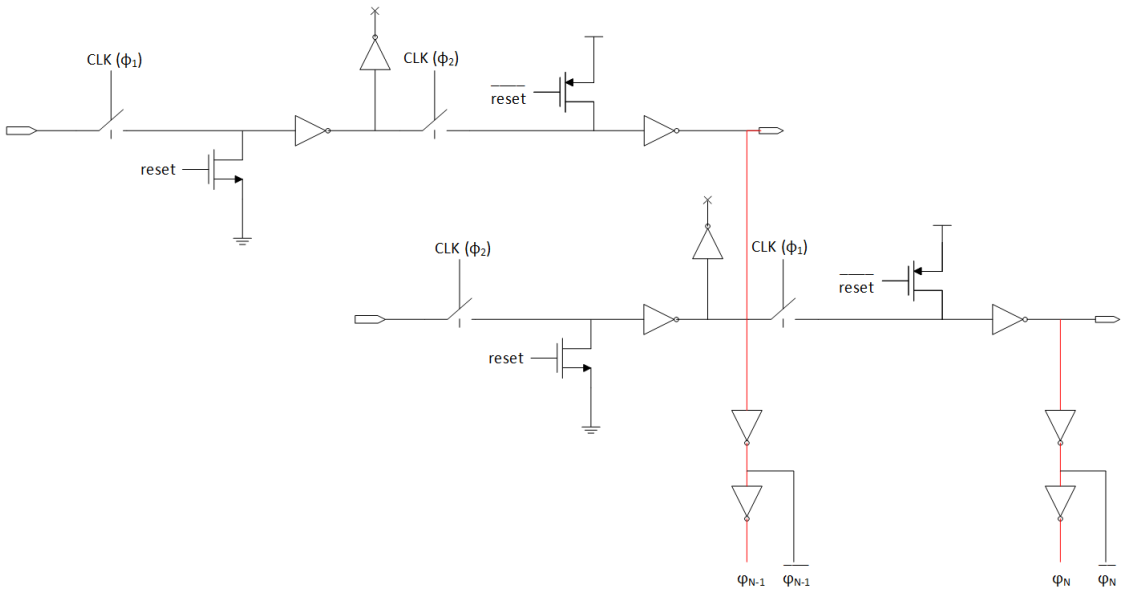


Figure 4.4: Sampling Clock generation circuit of the $0.18\mu m$ SST chip, Showing Interleaved Shift Registers and Load Balancing

PMOS connected in parallel. The philosophy to use the transmission gate is very easy to understand. It is well understood that NMOS cannot pass a strong '1' and PMOS cannot pass a strong '0' voltages, but by connecting the NMOS and PMOS in parallel full voltage range from 0 to V_{DD} can be achieved. A brief analysis, of transmitting logic '1' and logic '0' through a capacitive load C_L is performed below. The input voltage to the transmission gate is assumed to be V_{in} and the output voltage (V_{out}) is measured across the capacitive load C_L. Assume that both the transistors are conducting, the gate voltage of NMOS is V_{DD} and the gate voltage of PMOS is $0V$. The transistor currents at the output node is given by the equation 4.2 for output voltage $V_{out}(t)$

$$I_{out} = C_L \frac{dV_{out}}{dt} = I_{Dn} + I_{Dp} \tag{4.2}$$

Here, I_{Dn} and I_{Dp} is a function of V_{in}, V_{out} and the load capacitance C_L.

Electrical Characteristics of Transmission Gate for Logic '1' Transmission

Biasing both the transistors for conduction and applying $V_{in} = V_{DD}$ forces the capacitor C_L to charge. If the initial condition at the output node is assumed to be $V_{out} = 0V$ and if $V_{in} = V_{DD}$ is applied at the input, the current conducting paths are defined as shown in figure 4.5. The PMOS is initially conducting to pass the high voltage V_{DD}, at this point the

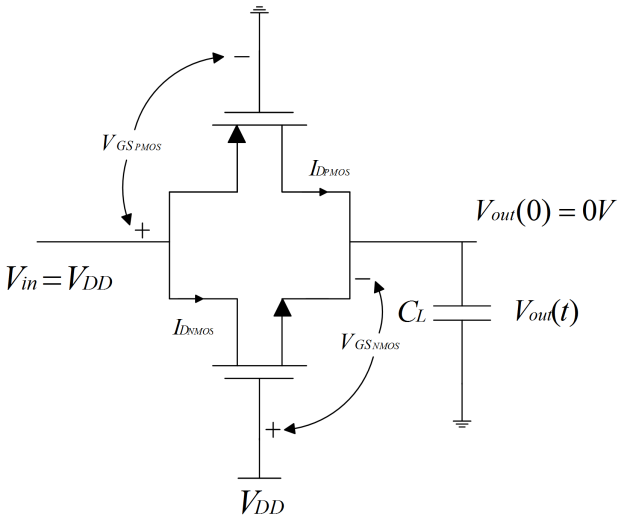


Figure 4.5: Transmission Gate Device Voltages for Logic '1' Transfer

gate source and source drain voltages are given by

$$V_{GSp} = V_{DD} \tag{4.3}$$

$$V_{SDp} = V_{DD} - V_{out}(t) \tag{4.4}$$

since PMOS is conducting and in saturation region the drain current at the initial condition is

$$I_{Dp} = \frac{\beta_p}{2}(V_{DD} - |V_{Thp}|)^2 \tag{4.5}$$

when $t > 0$, V_{out} increases, and V_{SDp} decreases. When V_{out} approaches $|V_{Thp}|$ the PMOS will change from saturation region to linear region at $V_{out} = |V_{Thp}|$,

$$I_{Dp} = \frac{\beta_p}{2}(2(V_{DD} - |V_{Thp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2) \tag{4.6}$$

The NMOS transistor operates differently than a PMOS transistor, at $V_{in} = V_{DD}$ the NMOS cannot pass the high voltage. The terminal voltages of the NMOS are

$$V_{GSn} = V_{DD} - V_{out}(t) \tag{4.7}$$

$$\begin{aligned} V_{DSn} &= V_{in} - V_{out}(t) \\ &= V_{DD} - V_{out}(t) \end{aligned} \tag{4.8}$$

for arbitrary times t

$$V_{GSn} = V_{DSn} \tag{4.9}$$

Saturation voltage for NMOS is $V_{DSn} - V_{Thn}$ and $V_{Thn} > 0$, V_{DSn} >Saturation Voltage will be satisfied as long as the NMOS is biased to conduct. NMOS remains in saturation with

$$I_{Dn} = \frac{\beta_n}{2}(V_{DD} - V_{out} - V_{Thn})^2 \tag{4.10}$$

when $V_{out} \geq (V_{DD} - V_{Thn})$, the V_{GSn} falls below the threshold voltage and the NMOS is cutoff. The output Capacitor C_L is charged entirely by the PMOS.

Electrical Characteristics of Transmission Gate for Logic '0' Transmission

For the opposite scenario, when the transmission gate is trying to pass logic '0', $V_{in} = 0V$ and biasing both the transistors for conduction. This scenario is shown in figure 4.6.

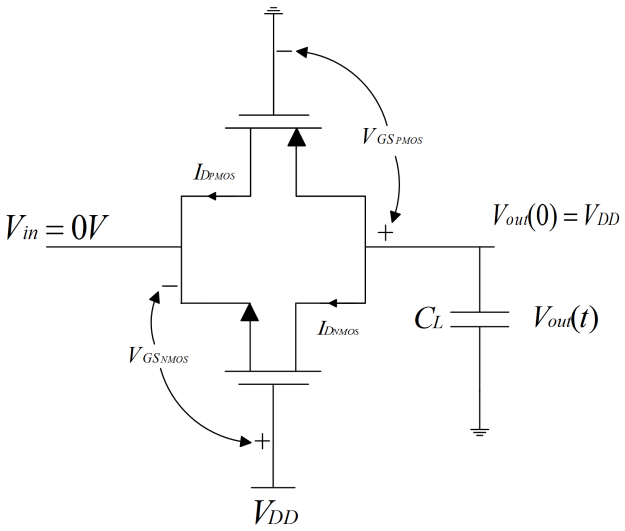


Figure 4.6: Transmission Gate Device Voltages for Logic '0' Transfer

The terminal NMOS voltages are given by

$$V_{GSn} = V_{DD} \tag{4.11}$$

$$V_{DSn} = V_{out}(t) \tag{4.12}$$

NMOS initially conducts in saturation region

$$I_{Dn} = \frac{\beta_n}{2}(V_{out} - V_{Thn})^2 \tag{4.13}$$

Since the load capacitor is discharging, NMOS goes to linear region when V_{out} falls to a value of $V_{DD} - V_{Thn}$, during the linear region I_{Dn} is given by

$$I_{Dn} = \frac{\beta_n}{2}(2(V_{DD} - V_{Thn})V_{out} - V_{out}^2) \tag{4.14}$$

At $V_{in} = 0V$ the PMOS cannot pass the low voltage. The terminal voltages of the PMOS

are

$$V_{GSp} = V_{out}(t) \tag{4.15}$$

$$V_{SDp} = V_{out}(t) \tag{4.16}$$

Initially, the PMOS is in saturation region with

$$I_{Dp} = \frac{\beta_n}{2}(V_{out} - |V_{Thp}|)^2 \tag{4.17}$$

since NMOS allows for complete discharge of the load capacitor C_L, PMOS will be cutoff when $V_{out} < |V_{Thp}|$. In principle, we can use the above equations at each voltage ranges to solve for transistor currents

$$I_{Dn} + I_{Dp} = C_L \frac{dV_{out}}{dt} \tag{4.18}$$

For the transfer of logic '1' through the transmission gate is equivalent to charging the load capacitor C_L through the Transmission gate equivalent resistance, let's call this resistance as R_{tg}. So the output voltage for charging the load capacitor C_L through the equivalent resistor R_{tg} is given as

$$V_{out}(t) = V_{DD}[1 - e^{-t/\tau_{tg}}] \tag{4.19}$$

where τ_{tg} is given as

$$\tau_{tg} = R_{tg}C_L \tag{4.20}$$

Similarly, logic '0' transfer through the transmission gate corresponds to discharging of the

capacitor, the output voltage is given by

$$V_{out}(t) = V_{DD}e^{-t/\tau_{tg}} \tag{4.21}$$

both high and low transmissions are characterized by same time constant.

The transmission gate equivalent resistance R_{tg} is a non-linear function of voltages. The value of R_{tg} can be obtained by analyzing the current flow through the transistors. A voltage dependent non-linear resistance for NMOS and PMOS can be defined as follows

$$r_n = \frac{V_{DSn}}{I_{DSn}} \tag{4.22}$$

$$r_p = \frac{V_{DSp}}{I_{DSp}} \tag{4.23}$$

Let's consider logic '1' transfer scenario, here the NMOS is always conducting and always in saturation. The non-linear resistance r_n is given by

$$r_n = \frac{2(V_{DD} - V_{out})}{\beta_n(V_{DD} - V_{out} - V_{Thn})^2} \tag{4.24}$$

equation 4.24 is valid until $V_{out} \leq (V_{DD} - V_{Thn})$, as the capacitor C_L is charging and $V_{out} \geq (V_{DD} - V_{Thn})$, the NMOS is cutoff, $I_{Dn} = 0$ and $r_n \rightsquigarrow \infty$.

For the same logic '1' transfer scenario, the PMOS is initially saturated and later goes to linear region. For $V_{out} \leq |V_{Thp}|$ the PMOS is in saturation, the non-linear resistance is given by

$$r_p = \frac{2(V_{DD} - V_{out})}{\beta_p(V_{DD} - |V_{Thp}|)^2} \tag{4.25}$$

as V_{out} increases, r_p decreases linearly. When V_{out} rises above $|V_{Thp}|$, the PMOS goes into

linear region and the non-linear resistance is given by

$$r_p = \frac{2}{\beta_p(2(V_{DD} - |V_{Thp}|) - V_{DD} + V_{out})} \tag{4.26}$$

r_p decreases as the output voltage increases.

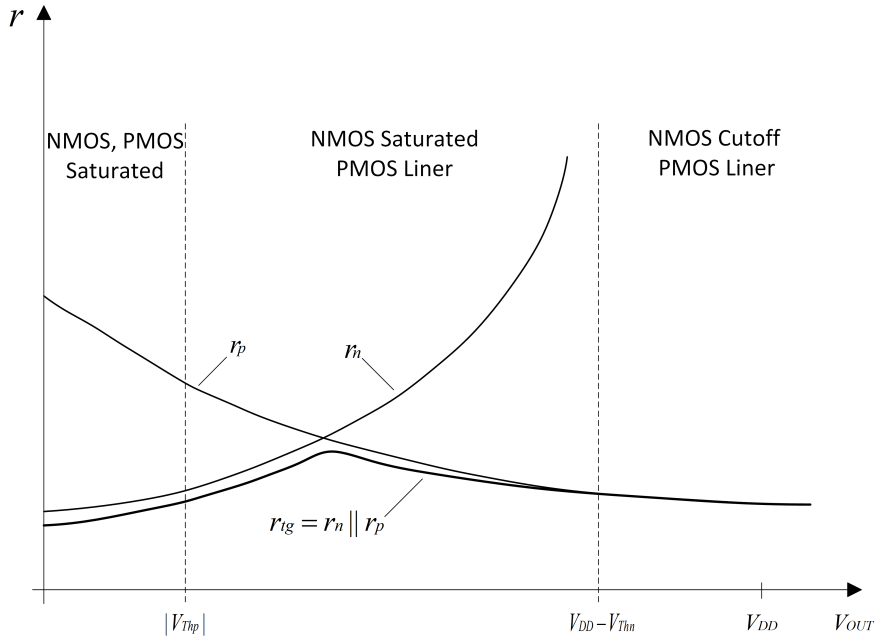


Figure 4.7: Graphical Illustration of Transmission Gate Resistance for Logic '1' Transfer

Figure 4.7 graphically illustrates the behavior of r_p and r_n and the value of r_{tg} for logic '1' transfer, where $r_{tg} = r_n||r_p$. For the initial condition, where $V_{out} = 0V$, transmission gate resistance can be approximated to

$$R_{tg} \approx r_{tg} = r_n||r_p \tag{4.27}$$

as the output voltage increases, NMOS will enter cutoff region and r_n is infinite. At this

point when the NMOS enters the cutoff region the transmission gate resistance is given by

$$\begin{aligned} R_{tg} &= r_p \\ &= \frac{2}{\beta_p(2(V_{DD} - |V_{Thp}|) + V_{Thn})} \end{aligned} \tag{4.28}$$

The time constant for the transmission gate is given by

$$\tau_{tg} = R_{tg} \times C_{out} \tag{4.29}$$

where C_{out} is the sum of external load capacitance (C_L) and all internal transistor capacitances.

A great care was taken while designing the layout of the high speed sampling clock generation circuit. Randomly distributed fixed pattern timing noise can be reduced with layout optimizations and also by avoiding minimum-sized transistors. Figure 4.8 shows a section of the high speed dynamic shift register layout. The four phases of clock lines are at the bottom and the sampling clocks are driven by the metal lines at the top. Two sets of 512 shift registers, 1024 in total and 2 dummy shift registers for load normalization are added at both the ends. To achieve precise sampling clock timings, symmetry is maintained and the high speed shift registers are made to be extremely reproducible.

The simulation results of the sampling clock timing non-uniformity showed major improvements, all the "ODD/EVEN" effects and the non-uniformity due to loading of the feedback register was eliminated, however, randomly distributed timing uniformity cannot be eliminated. The post silicon results of the timing non-uniformity is discussed in section 6.3.6

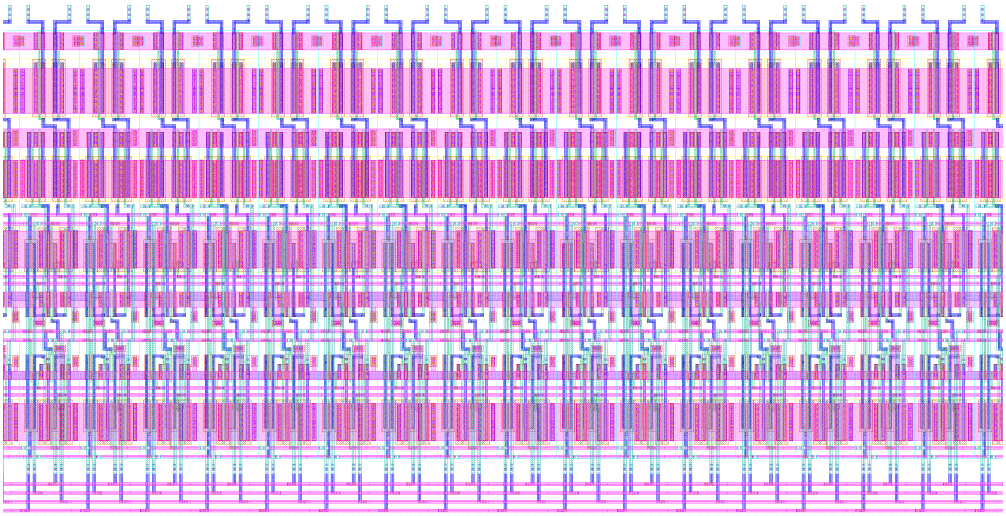


Figure 4.8: A Section of the High Speed Dynamic Shift Register Layout

4.3.2 Synchronization Circuit

In digital design, when two clocks are not synchronous, signals that are used to communicate between these two asynchronous clock domains require synchronization. For the $0.25\mu m$ SST chip, system reset (STOP) signal is asynchronous to the external LVDS input clock. The STOP synchronization circuit presented in the figure 4.9 uses a dynamic master slave flip-flop to synchronize the STOP signal to the input clock. The description of the $0.25\mu m$ SST's synchronization circuit is presented in section 2.4.

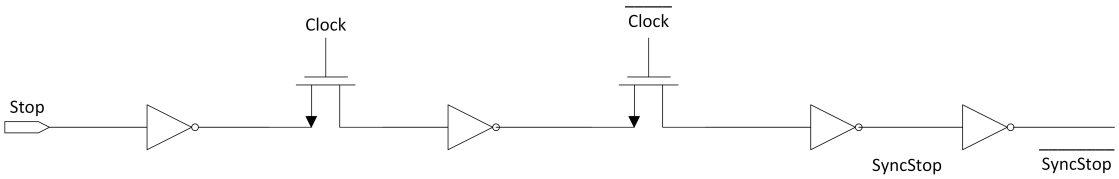


Figure 4.9: Schematic of the Synchronization Flip-Flop for the $0.25\mu m$ SST Chip

The mean time between failures for the dynamic shift register is given by

$$MTBF = \frac{1}{\lambda} = \frac{e^{\frac{t_R}{\tau}}}{f_d \times f_c \times T_0} \tag{4.30}$$

here, λ is the failure rate, t_R is the resolution time, i.e., the time after the clock edge that the output data is needed, τ is the time constant of the latch, f_d is the data arrival rate, f_c is the clock sampling rate and T_0 is the metastibility window for the latch.

The dynamic pass transistor flip-flop is a non-restoring flip-flop, there are no cross coupled gates, there is no amplification, τ is roughly the inverse of the gain of the gates, since we are not using cross coupled inverters, there is no amplification, effectively making the value of τ infinite and there is no metastability resistance. Unfortunately, dynamic pass transistor flip-flop is not a good choice for synchronization circuits. In general, the best choices for synchronization flip-flops are the flops with, high power, faster clock to Q time and very simple logic avoiding reset logic and multiplexes. These circuits tend to have high gain and thus smaller τ.

The $0.25\mu m$ SST suffers with synchronization failures. The failure rates for the $0.25\mu m$ SST are presented in section 3.3.7. These failures are so rare they do not affect for the ARIANNA experiment. We simply detect the synchronization failure by looking at the STOP data and discard the corresponding event. The detection of synchronization failures is fairly simple, the SST has the ability to readout the sampling clock pulses, these pulses are also called "STOP" data. Nominally, for 256 samples, two sampling clock pulses should be logic '1' and the rest should be logic '0'. During synchronization failures, the width of the sampling clock pulses increase, which essentially mean that more than two sample and hold switches are closed and the data is erroneous. The $0.25\mu m$ SST chip suffers from 0.02% synchronization failure rate.

4.3.2.1 Design Changes for SST0.18μ Synchronization Circuit

A new synchronization circuit was developed using restoring flip-flops to eliminate synchronization failures for the SST0.18μ chip. The edge-triggered flip-flop is implemented internally

with two latches as shown in figure 4.10.

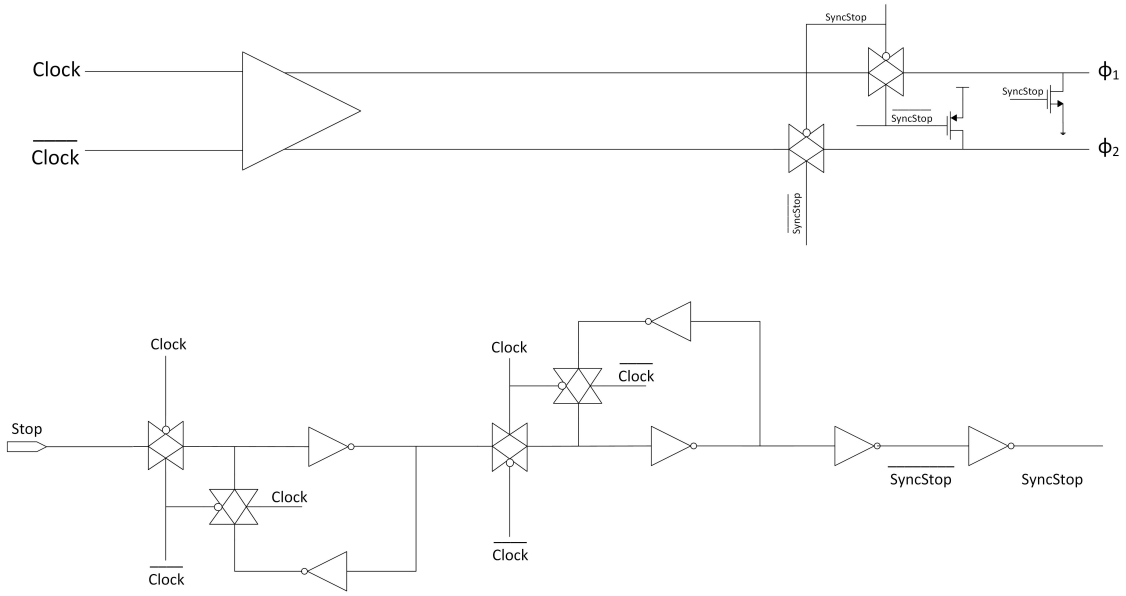


Figure 4.10: Schematic of the Synchronization Circuit for the 0.18μm SST Chip

The master latch samples "stop" on the rising edge of the clock, the slave latch samples the output of the master latch on the falling edge of the clock. The resolution time for each of these latches are one half clock cycle. Here in this scenario, it is unimportant if the master latch goes to metastable, but whether the slave latch goes to metastable. Metastability of the master can propagate to the slave during the first half of the clock cycle, if the master resolves its value close to the falling edge of the clock violating its setup and hold times, the metastability can be transitioned to the save latch.

The mean time between failures of this synchronization circuit is given in the equation 4.31. By using restoring flip-flops, we decreased the time constant (τ) of the latch. The synchronizer time constant is approximately the inverse of the small-signal amplifier gain around the cross-coupled gates of the latch. Simulations were performed to make sure the time constant is as small as possible. Smaller time constant was achieved by avoiding the use of minimum-sized transistors for the latches. The latches are faster and more power hungry. From the equation 4.31 τ affects the exponent, therefore improving the time constant is very

beneficial. Post silicon testing of the SST0.18μ chip revealed 0% synchronization failure rate. The results are presented in section 6.3.4

4.3.3 Stop Position "Memory" Readout Circuit

Section 2.11 describes the stop position readout circuit for the 0.25μm SST chip. The block diagram of the stop position readout circuit can be seen in figure 2.52 and the individual cell of the stop position readout circuit is essentially an inverter and a switch. The stop position circuit will transfer the sample clock logic level to the output. As we recall from section 2.7, the sampling clocks are generated by high speed dynamic shift registers and the charge hold time for the dynamic shift registers are given by

$$t_H \approx \frac{C_{node}}{I_{leakasge}}(V_{max} - V_{1HI}) \tag{4.31}$$

where, C_{node} is the node capacitance of the dynamic shift registers, for all intense and purposes we can consider C_{node} as the input capacitances of the inverter. $I_{leakasge}$ is the leakage current defined in equation 2.48, V_{max} is the maximum voltage given by $V_{max} = V_{DD} - V_{Thn}$ and V_{1HI} is the minimum voltage value at the inverter input that will still be interpreted as logic '1'.

Although, the dynamic register hold time is not a problem for the ARIANNA experiment, we decided to update the design by adding a static D flip-flip to hold the sample clock for indefinite amount of time. ARIANNA experiment reads out the sample clocks (STOP data) at 1MHz, this read clock frequency is chosen for its compatibility to the 12 bit-1MSPS ADC used for the experiment. Readout clock speed of 1 MHz will not degrade the sample clock stored on the dynamic shift register. However, if we choose to read out at a much slower rate, the sampling clock can degrade and we will not be able to recover the STOP data.

For the SST0.18μ to be compatible to readout at much slower speeds, a new stop position "memory" readout cell was designed. Figure 4.11 shows one cell of the stop position readout circuit. 512 of these cells are connected in parallel to readout 512 STOP data.

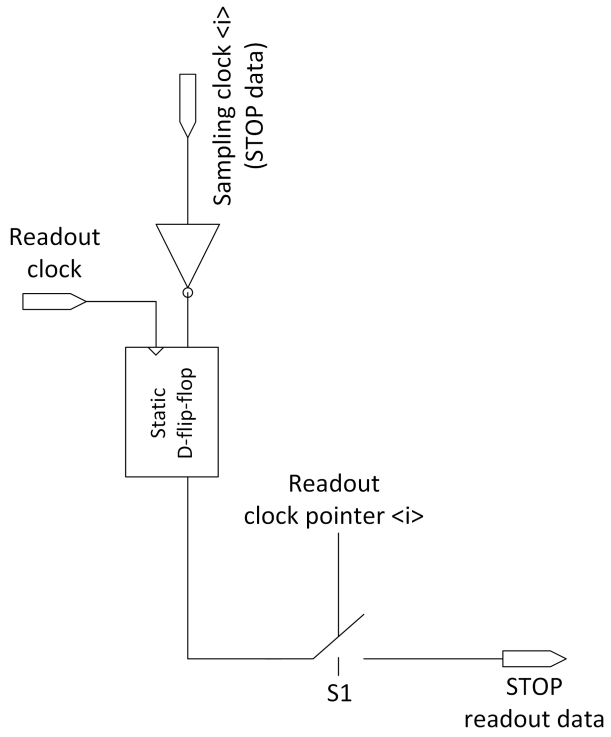


Figure 4.11: Stop Position "Memory" Readout Cell

In the figure 4.11, the input to the cell is the sampling clock pointer, also called as the STOP data is latched to the static D flip-flop, the readout clock pointer will manage the switch. When the switch is closed, the stop data is sequentially read out of the chip for processing.

4.3.4 Unity Gain Feedback Analog Output Driver

An analog amplifier in unity gain feedback configuration is used to implement the analog buffer that drives the off chip load capacitance. The SST0.18μ reads the sample voltages through a source follower stage followed by a unit gain feedback buffer. The 0.25μm SST chip, uses only source follower stage to drive the analog output pin. The voltage gain of

the $0.25\mu m$ SST chip was measured to be 0.7 V/V, were as the voltage gain of SST0.18μ is measured to be 0.714 V/V. The increase in the gain is attributed to the unity gain feedback analog output driver.

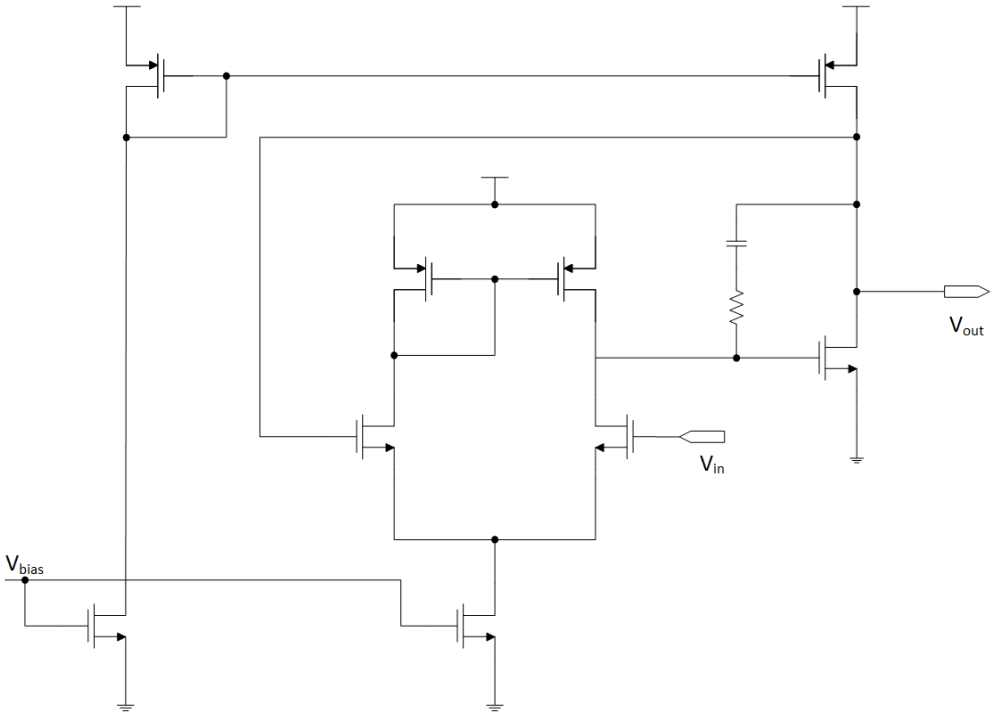


Figure 4.12: Schematic of the Unity Gain Analog Output Driver

The amplifier circuit was designed by Edwin Chiem and detailed description of the unity gain feedback output driver is presented in his dissertation [19]. A brief overview of the circuit is presented here. The amplifier in the feedback configuration consist of two stage opamp circuit shown in figure 4.12. The first stage is a differential pair with current mirror load to achieve voltage gain. The second stage is a common source stage that provide sufficiently wide output voltage swing and additional voltage gain. As the analog buffer is used in feedback, the circuit compensation is implemented to ensure stability. The load capacitance of the circuit is fairly large ($\sim$12.5 pF) making the output node the dominant pole. With the output pole closet to the origin, the Miller compensation technique is not as useful. However, the compensation capacitor and resistor are used to place as LHP zero to aid in compensation. With a load capacitance of 12.5 pF, the open loop amplifier has as phase

margin of greater than 60 degrees.

The layout of the analog output driver is shown in figure 4.13. Large current sources and the input transistors utilize interdigitated transistor pairs to reduce the effects of mismatch. Drains diffusion are shared when possible to minimize the capacitance and guard rings are placed for isolation.

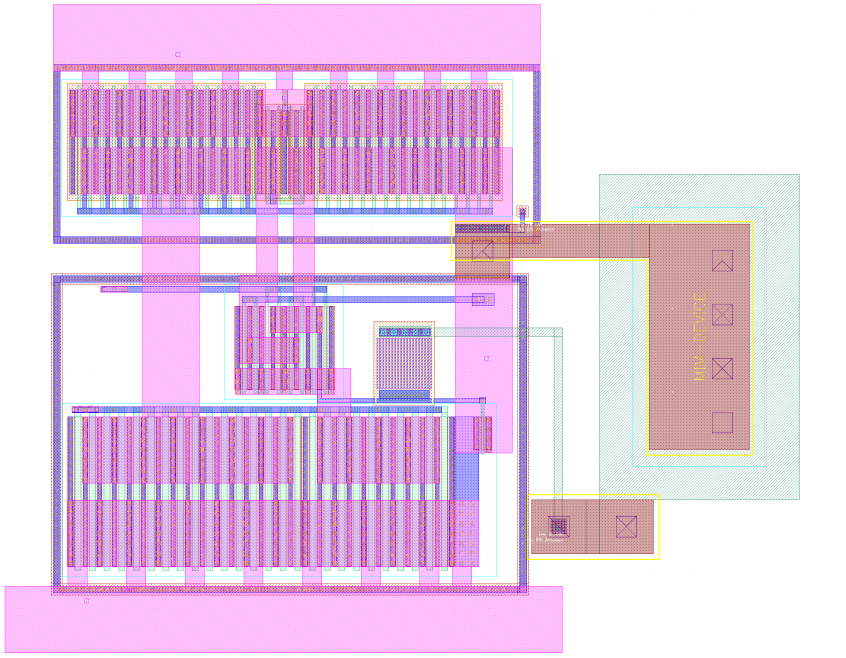


Figure 4.13: Unity Gain Analog Output Driver Layout

Chapter 5

Sample Interval Variation Characterization

Sampling and hold circuits which operate at high frequencies, such as Synchronous Sampling and Triggering Chip, are limited by an uncertainty caused by the instability of the sampling clock and its clock distribution circuitry. However, the sample clock jitter is not the only source for sample interval variation. Other various noise sources and devices mismatches also cause timing errors on the sampling clock. These variations causes the circuit to vary from the idea sampling time (T_S). SST circuit, uses an interleaved sampling clock generation circuitry. Although, this sampling clock generation scheme is an effective way to achieve high sampling rates, it is susceptible to the sampling timing errors. These timing errors will degrade the performance of the SST. Figure 5.1 illustrates the sampling interval variations for the SST.

The sampling interval uncertainty (clock jitter or clock phase noise) creates an amplitude variation, this variation is relative to the input signal frequency and the sampling clock speed. As the input frequency increases for the same sampling speed, the fixed amount of

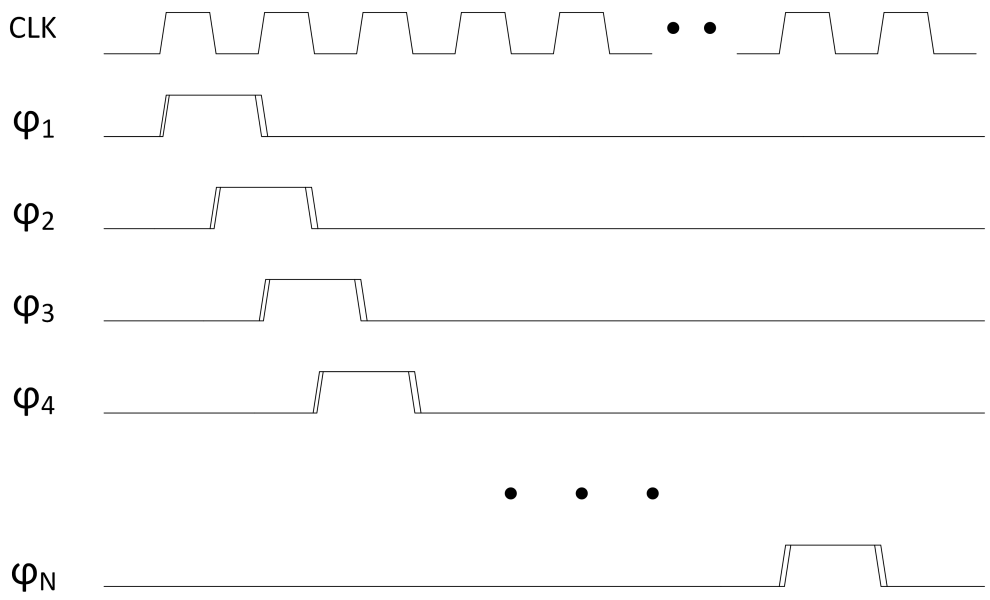


Figure 5.1: Illustration of Sampling Clock Timing Uncertainty

clock jitter generates larger amount of amplitude variation, this is illustrated in the figure 5.2, input signal with frequency f_1 f_2 the amplitude variation is larger. Figure 5.2 shows the impact of amplitude variation with clock jitter.

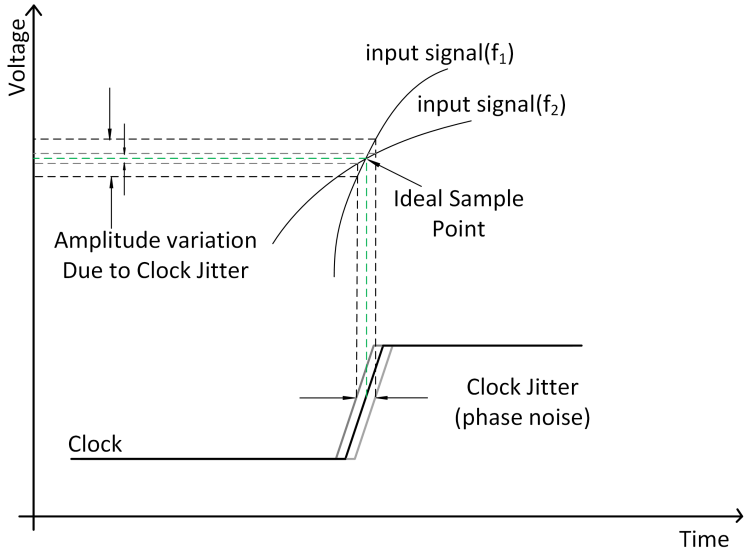


Figure 5.2: Amplitude Variation Based on Clock Jitter

The average error power (referred to 1Ω) of the sample interval error can be estimated for

the sinusoidal input with equation 5.1.

$$E_P \simeq \frac{A^2\omega^2\sigma_t^2}{2} \tag{5.1}$$

Where A is the amplitude, ω is the input frequency and σ_t is the RMS value of the sample interval error [33]. The sample interval error (clock jitter) will degrade the SNR (SNR_{Jitter}). There are several other factors that limit the SNR, such as quantization noise and thermal noise. We will mostly discuss the SNR degradation by the sample interval error.

The SNR_{Jitter} is limited by the input frequency ω and the total amount of clock jitter σ_t. The SNR_{Jitter} can be calculated by the equation below

$$SNR_{Jitter}[dBc] = -20 \times log(2\pi \times \omega \times \sigma_t) \tag{5.2}$$

As expected, the fixed amount of clock jitter, the SNR degrades as the sampling frequency decreases. Another major factor that affects the SNR is the thermal noise. The thermal noise does not change with input frequency or sampling frequency. In the equation 5.2 ω is the input frequency and σ_t is the sampling clock jitter.

The sampling clock jitter consist of timing uncertainty of the clock as well as the aperture jitter of the SST. The two components combine to give the equation below.

$$\sigma_t = \sqrt{(\sigma_{Jitter,clock-input})^2 + (\sigma_{Aperture-SST})^2} \tag{5.3}$$

The $\sigma_{Aperture-SST}$ is the aperture uncertainty of the system. It is the sample-to-sample variation in the encoding process. The aperture uncertainty has three distinct effects on the system performance. First, it can increase the system noise, second, it can contribute to the uncertainty in the actual phase of the sampled signal itself giving rise to increases in error

vector magnitude. Third, the aperture uncertainty can increase intersymbol interference. The $\sigma_{Jitter,clock-input}$ is the jitter from the clocking chain for e.g., oscillator, two phase clock generator, clocking buffer and the high speed sample clock generator.

In general, the timing uncertainties can be attributed to two separate categories: bounded and unbounded jitter. Unbounded jitter is nothing but the random jitter and the bounded jitter, which is deterministic jitter. For the Synchronous Sampling and Triggering circuit, the random jitter is produced by various devices noise sources such as flicker noise and thermal noise. The distribution of random jitter is described by a Gaussian random variable with zero mean. The random jitter is unpredictable and the sampling interval variations caused by random jitter change from moment to moment.

The bounded jitter or the deterministic jitter can be further classified into correlated jitter and uncorrelated jitter. The correlated jitter is usually caused by duty cycle distortions and intersymbol interference, however the uncorrelated jitter is caused by periodic jitter and other factors. The bounded jitter in the sampling clock is defined as the jitter that is well defined and periodic. This bounded jitter which appears on top of the sampling interval is referred to as fixed pattern noise (FPN). For the SST chip, mismatches in the sampling clock paths and loading variations on the transistors are the major contributors for the fixed pattern noise. Other than these mismatches in the sampling clock paths, the duty cycle variations of the external oscillator, device mismatches caused due to process variations also contribute to deterministic jitter.

The unbound or random jitter can be suppressed by averaging sufficiently large set of sample intervals. After averaging large set of sample intervals, only the deterministic jitter components will be present. Once the deterministic jitter components are known, the well-defined nature of the jitter can be calibrated out. The calibration method for the SST's fixed pattern noise was developed by Edwin Chiem [19].

The SST has a very unique deterministic sampling time error. The sampling clocks are generated by a fast shift registers containing a single "1" as a pointer. The fast shift registers are dynamic and both master and slave sections of shift registers are used to generate the sampling clock. Due to this inherent interleaving, the path lengths of the clock signal is different for adjacent samples. For 2 Gsamples/s sampling frequency, all the odd samples are deviated by +30ps from the mean sampling time and the even samples are deviated by -30ps from the mean sampling time. This results in an alternating pattern in the sampling interval.

Two methods of FPN characterization was developed for the SST: the zero crossing method and simulated annealing method. A very brief description of zero crossing method and simulated annealing method is presented in this dissertation. Detailed information about the FPN characterization can be found in [19].

5.1 Fixed Pattern Noise Characterization Zero Crossing Method

Zero crossing detection is the most common method for measuring the period of the signal. Zero crossing is the method of choice for measuring phase and frequency. The reference is very easy to establish and the rate of signal amplitude change is usually maximum at the zero crossings. Whether measuring period, frequency or phase, the source of errors are the same. Post processing of signal conditioning is important to achieve high timing accuracy. The digital processing of the output signal present significant advantages. An approach which relies on statistical probability that the next zero crossing will be close to the next half period. In this method of zero crossing the sample interval associated with each sample cell is calculated based on the probability it would receive a randomly assigned zero crossings.

The probability that a zero crossing occurs between a pair of samples is directly proportional to the sample interval. This method of counting zero crossings and determining the sample interval relies on the statistical law of large numbers.

The zero crossing FPN characterization [19] works with large number of input waveforms ($\sim$ 2 million waveforms were sampled on SST for zero crossing FPN characterization). A statistically large number of waveforms are recorded and a zero crossing probability mass function is calculated using the equation 5.4

$$Pd[i] = \frac{Z_c[i]}{\sum_{k=1}^{N} Z_c[k]} \tag{5.4}$$

The sampling intervals are calculated from the probabilities with the following equation [19]:

$$T_{sample}[i] = T_{nominal} \times Pd[i] = T_{nominal} \frac{Z_c[i]}{\sum_{k=1}^{N} Z_c[k]} \tag{5.5}$$

Here, $T_{nominal}$ is the ideal sample interval, for SST running at 2 Gsamples/s the nominal sampling interval ($T_{nominal}$) is 500 ps.

The zero crossing FPN characterization suffers from statistical error. Larger the number of sample waveforms, lower is the statistical error. The equation 5.6 shows the error on the sampling interval in seconds.

$$StatisticalError = \frac{T_{sample}}{N} \sqrt{\frac{1}{M \times T_{sample} \times \omega}} \tag{5.6}$$

Where, N is the number of sample cells in the SST (256), SST0.18μ (512), M is the number of waveforms in the zero crossing data set and ω is the input frequency of the sinusoids.

5.2 Fixed Pattern Noise Characterization Simulated Annealing Method

Simulated annealing method of fixed pattern noise characterization is a stochastic computational method of finding extremums to large optimization problems. This heuristic method was first proposed by Kirkpatrick [35]. The optimization algorithm is based on a physical annealing analogy. Unlike " hill climber" algorithm which is very effective at finding local optimums, simulated annealing algorithms are really good at finding global optimums. The simulated annealing algorithm occasionally accepts worse solutions, and therefore jumps out of any local optimums and find global optimums.

The acceptance function for the simulated annealing is fairly simple, first we check if the neighbor solution (timing correction vector with additional RMS noise parameter) is better than the current solution (current timing correction vector), if it is, we accept the new solution unconditionally. If however the neighbor solution is not better, a couple of factors should be considered. Firstly, how much worse is the neighbor solution is and secondly, how high the current "temperature" of our system is. The "temperature" in this scenario is the amount of added noise and the probability of accepting a worse solution. The "temperature" decreases for each iteration and it approaches to zero as the number of runs approach infinity. At high "temperatures" the system is more likely to accept solutions that are worse.

The simulated annealing algorithm for the SST to characterize fixed pattern timing noise is briefly described below:

- First, we need to set the initial "temperature" and set a random initial timing correction.
- Then we begin looping until the condition for the cost function is met. This is usually when the system reaches a sufficiently low "temperature" or a good enough cost

function is achieved.

- From here we select a new timing correction vector by making small change i.e., adding RMS noise to the current timing correction vector.
- We then decide whether to move to the new timing correction vector.
- Finally, we decrease the "temperature" and continue looping.

The simulated annealing method was successfully used to characterize the fixed pattern timing noise for the SST. The results of the fixed pattern timing noise characterization is presented in section 3.3.10.

Chapter 6

Test Results SST0.18μ Chip

This chapter presents the functional test results of the SST0.18μ chip. Manufacturing and packaging details, data acquisition board designed for the SST0.18μ chip and the performance specifications are described in this chapter.

6.1 Manufacturing and Packaging

The SST0.18μ Chip designed using IBM 7HV 0.18μm technology [1]. A total of 40 chips were manufactured and packaged inside a 56 pin 8mm x 8mm Open Cavity Plastic - Quad Flat No-leads Package (OCP-QFN). The cavity size of the package is $6000\mu m \times 6000\mu m$

A System board was designed for the SST0.18μ Chip and the results are presented in the following sections.

Figure 6.1 shows the picture of a manufactured SST0.18μ die. The size of the die is $1583\mu m \times 3105\mu m$.

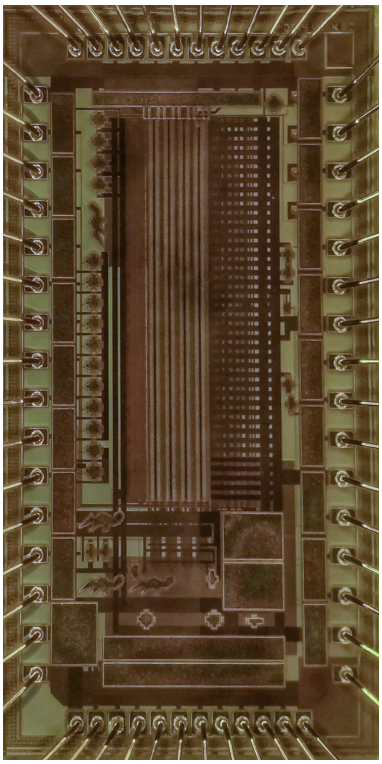


Figure 6.1: Picture of the Manufactured SST0.18μ Die. The Size of the Die is 1583μm by 3105μm - Notice the Filler AM Metal Made in the Shape of "Anteaters" (UC Irvine's Mascot)

6.2 System Board

To verify the functionality of the SST0.18μ, a system board with data digitization capabilities was designed and manufactured. A 4 layer printed circuit system board was designed and fabricated through Advanced Circuits (4PCB). The board was populated in house. The test board is shown in Figure 6.2.

The board requires 5V and 3.3V to operate. Several fast Ultra Low Dropout Linear Regulators are used to generate required 1.8V, 2.5V, 2.7V and 1.2V supplies. Great care has been taken to load match the analog input lines in order to reduce signal loss. The PCB tracks carrying analog signals are matched to 50Ω and as such the tracks are designed as transmission lines. Additional care was taken to keep the transmission lines as short as possible and design considerations were made to avoid corners, with any corners kept to obtuse angels.

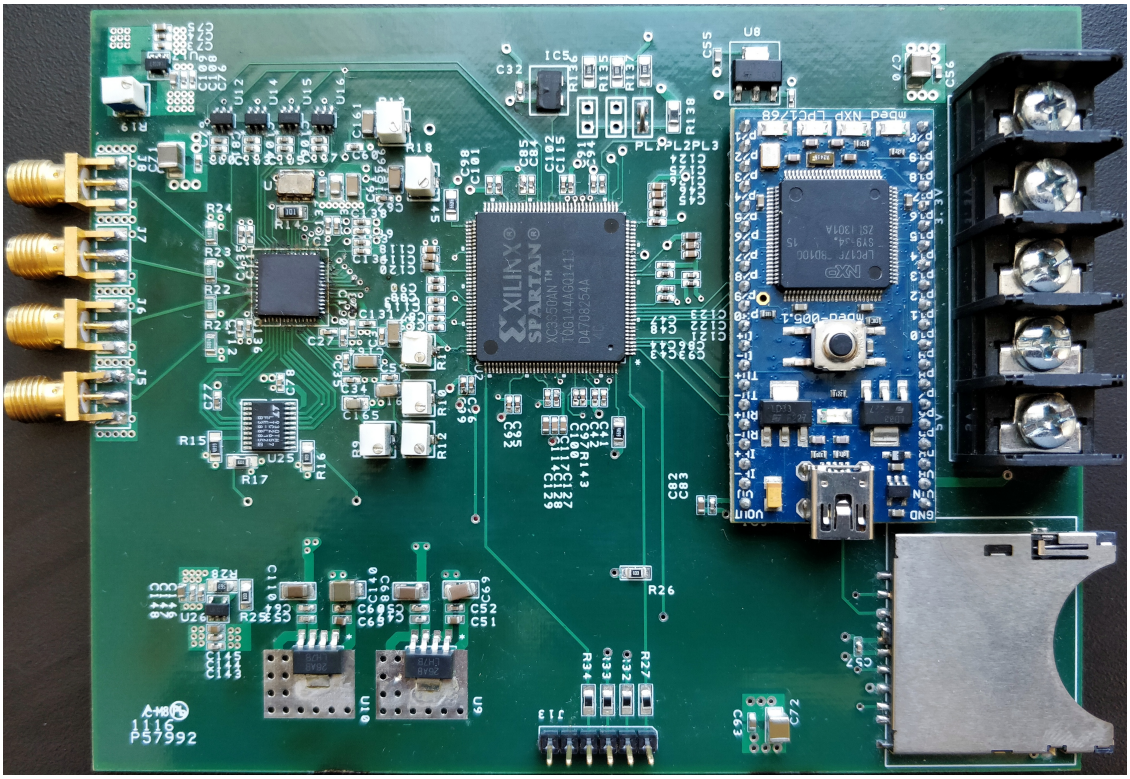


Figure 6.2: Picture of the SST0.18μ System Board

Surface mount capacitors are placed very close to the package to reject high-frequency noise on the supply and passive control lines.

The control signals for the SST0.18μ are driven by the XILINX Spartan 3AN FPGA. The high speed clock for the SST0.18μ is supplied by 1.5 GHz FXO XpressO series low jitter oscillators (currently manufactured by Integrated Device Technology, Inc). The comparator thresholds are supplied by 12 bit Linear Technologies LTC2657 digital to analog converter. The MBED microcontroller programs the DAC to supply appropriate threshold voltages to the SST0.18μ. The sampled data is readout via Texas Instruments ADS7886 ADC, the digitized data is temporarily stored in FPGA until the MBED accesses it and saves it on the SD card.

6.3 Functionality Testing

This section presents the SST0.18μ's functionality results and performance parameters. Most of the testing methodologies are similar to that of 0.25μm SST chip and they are presented in in chapter 3. The following subsection discusses sampling and digitization, VFPN, analog bandwidth, stability of the system, noise measurements and timing resolution.

6.3.1 System Verification

A functionality of the SST0.18μ was tested by recording and reading out a pure 100 MHz sine wave. The SST0.18μ sampled the input at 2.5 Gsamples/s and the analog data was read out at 980 KHz. The recovered analog signal is digitized using a 12 bit ADC. The signal was reconstructed in MATLAB, the pedestal subtracted sinewave is plotted in figure 6.3.

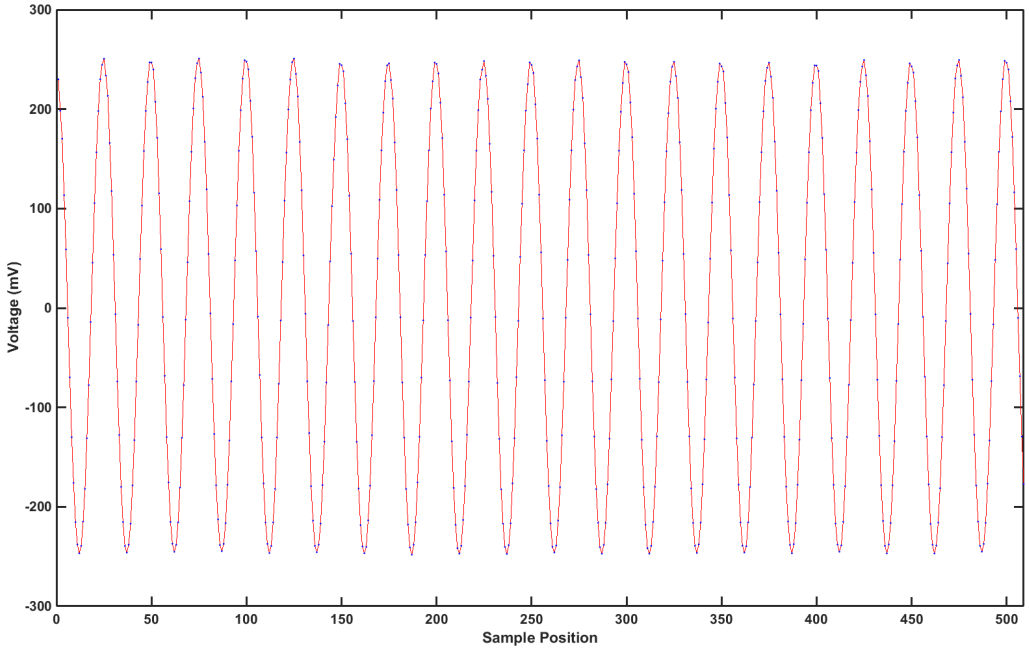


Figure 6.3: SST0.18μ Readout of a Recorded 100 MHz Sinewave

6.3.2 Voltage Fixed Pattern Noise

The SST0.18μ chip is prone to Voltage Fixed Pattern Noise. The theory of VFPN is described in section 3.3.3. The VFPN vector is measured by recording and digitizing DC bias voltages repeatedly and averaging each sample cell's offset voltage. The voltage fixed pattern measurement with DC offsets is plotted in figure 6.4.

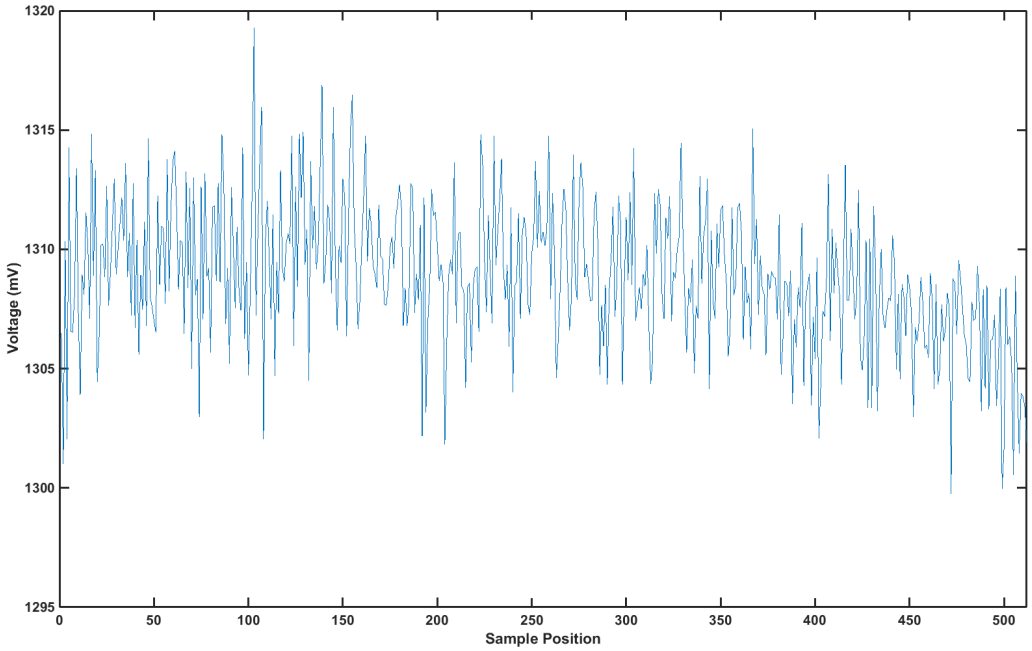


Figure 6.4: VFPN Measurements with DC Offsets

Here, the large scale non-uniformity in the VFPN is attributed to the process variations. This is consistent with all the channels in the chip. The distribution of the VFPN is plotted in the figure 6.5. The standard deviation of the VFPN across the channel is measured to be 2.992 mV (RMS). Fortunately, VFPN can be easily calibrated out of the recovered analog signal.

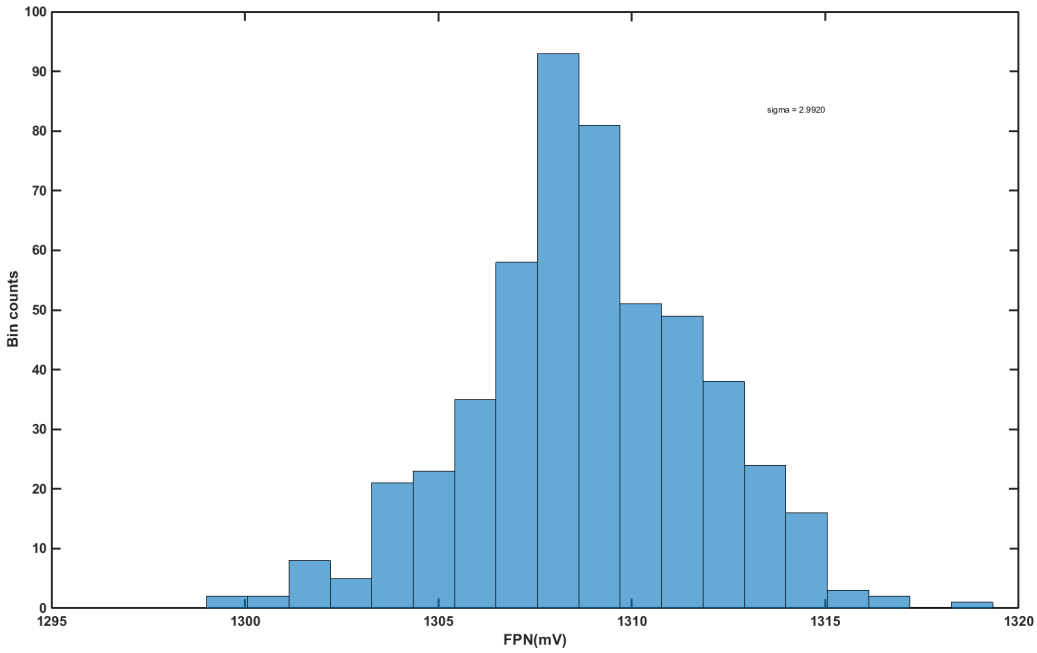


Figure 6.5: VFPN Distribution

6.3.3 Bandwidth

The bandwidth of the SST0.18μ was measured by applying large signal waveforms with varying frequency from an Agilent N5181A MXG analog signal generator and reading out the recorded waveform and measuring the peak to peak of the output signal. The SST0.18μ recorded the signals at 2.5 G samples/s. The negative 3dB bandwidth frequency of the SST is measured to be slightly above 1.2 GHz. The recorded sine waves was normalized to unity gain at the lowest frequency sine wave in the data (100MHz). The gain versus frequency of the SST0.18μ was normalized to 0 dB, and can be seen in the figure 6.6. The input sine waves were large signal waveforms that span the SST0.18μ's linear input voltage range. The input sinewaves were centered on 0.6V which was set by an external bias-tee.

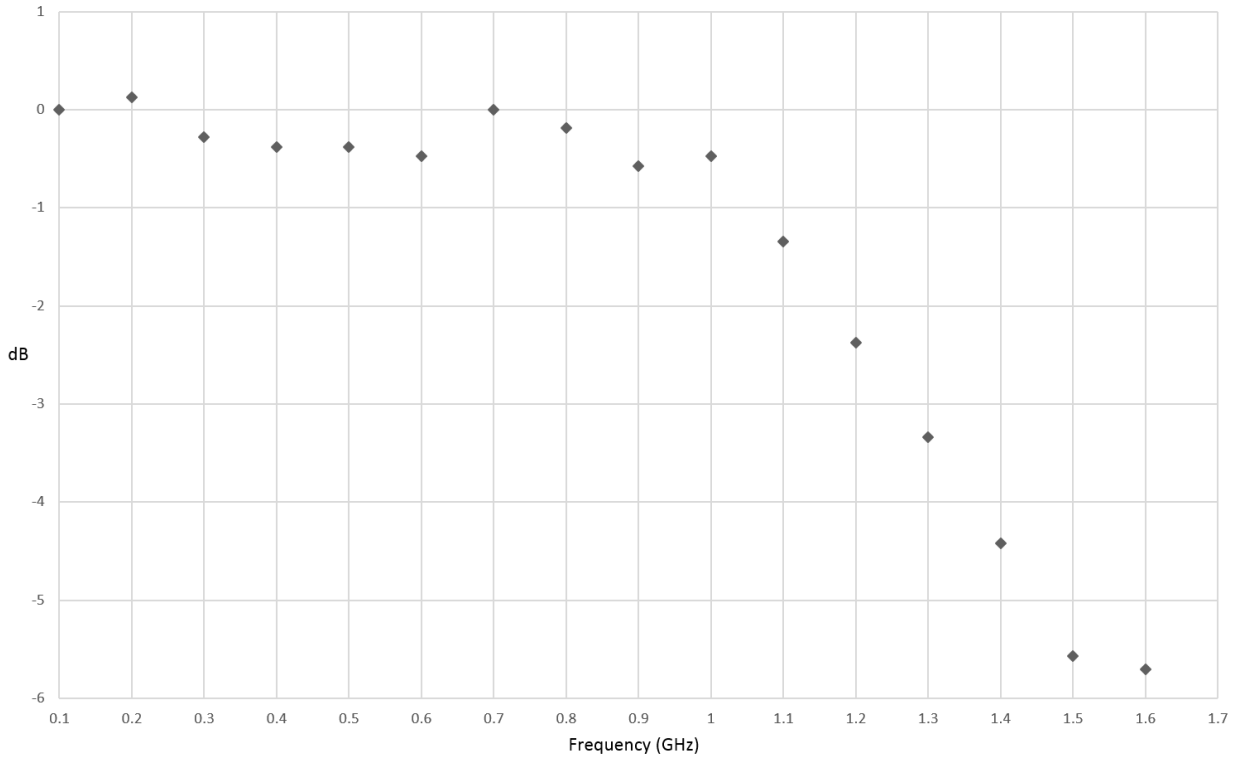


Figure 6.6: Magnitude vs Frequency of the SST0.18μ

6.3.4 System Stability

$0.25\mu m$ SST suffers from synchronization failures. The failure rates for the SST is presented in the section 3.3.7. The synchronization circuitry for the SST0.18μ was updated to restoring flip-flops to eliminate synchronization failures (sec: 4.3.2). The synchronizer time constant (τ) is approximately inverse of the small signal amplifier gain around the cross-coupled gates of the latch, here τ is small, thus increasing the mean time between failures (MTBF).

Synchronization failures can be detected by looking at the width of the sampling clock pointers (STOP data). If the SST0.18μ enters metastibility the sampling clock pointer will no longer be 2-wide but it will either grow or shrink. Figure 6.7 shows the histogram of sampling pointer widths for SST0.18μ.

1×10^6 events were acquired and readout and we did not see any synchronization failures.

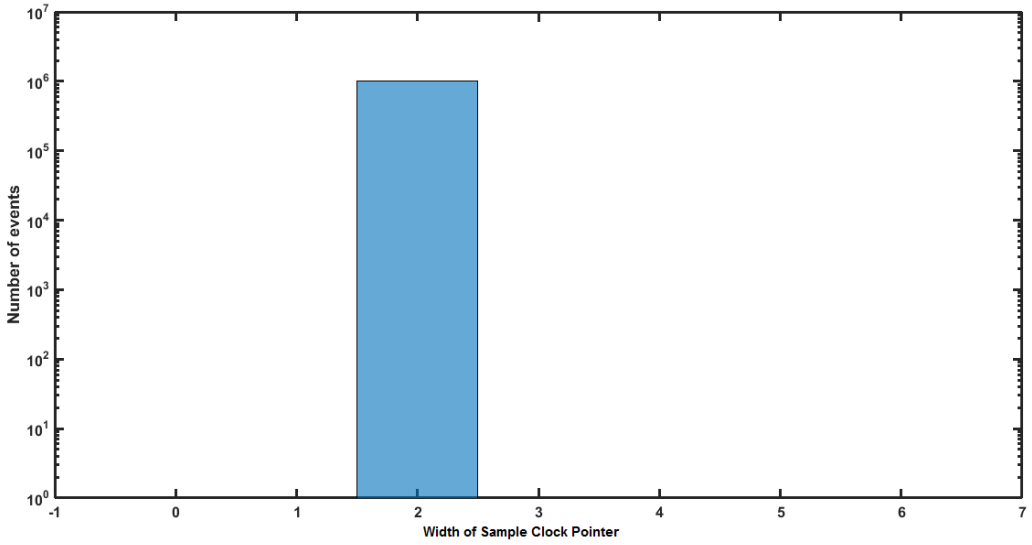


Figure 6.7: Histogram of Sampling Pointer Width for SST0.18μ

Let's extrapolate this result for the lifetime of the ARIANNA experiment. Each ARIANNA station on an average trigger at 1 mHHz, for the complete experiment total of 1000 stations will be installed on ice, so for 1000 stations the trigger rate is 1 Hz. At the rate of 1Hz we get $\sim 31.5 \times 10^6$ events per year. If we assume the lifetime of the experiment is 3 years, we have a grand total of $\sim 94.5 \times 10^6$ events. Conservatively, let's say we have 50% more synchronization failures, i.e., 1 failure for 2×10^6 events, we will have 47 Synchronization failures for the lifetime of the experiment. This failure rate is completely acceptable.

6.3.5 Sampled Noise Measurements

The sampled noise measurements of the SST0.18μ chip is measured by taking the standard deviation of the pedestal corrected DC baseline voltages of several thousand events for all channels. The total system level output noise is measured to be 0.862 mV. The distribution of cell-to-cell pedestal subtracted noise is plotted in the figure 6.8

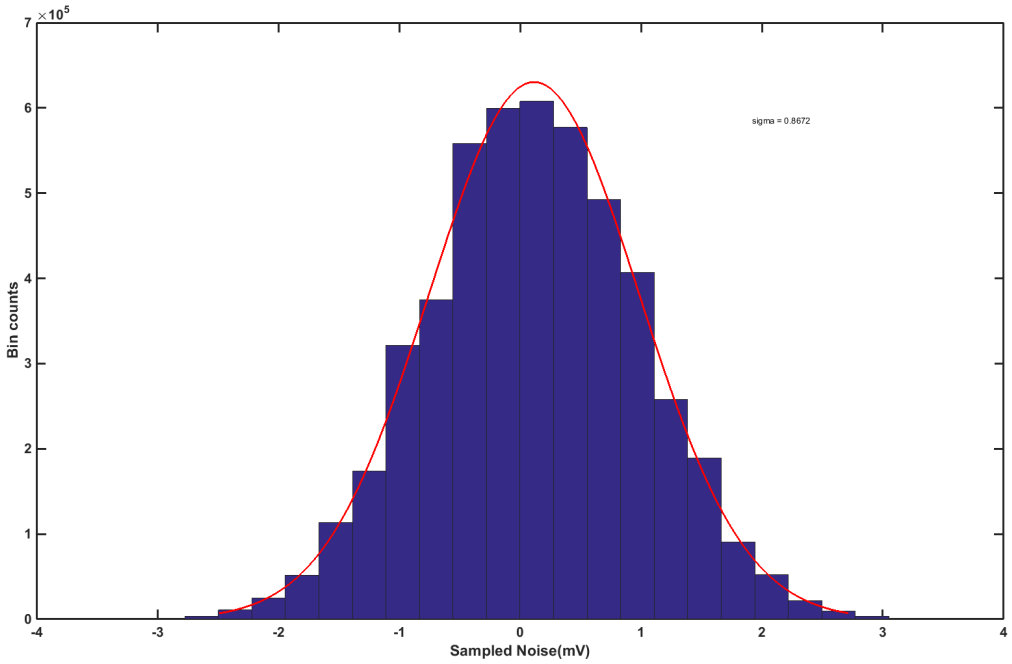


Figure 6.8: Noise Distribution

6.3.6 Fixed Pattern Sample Interval Error

The mean cell-to-cell sample intervals were measured using two methods, zero crossing method and simulated annealing method. The two methods of measuring sample interval non-uniformity is discussed in sections 5.1 and 5.2. Both the methods are independently verified and the timing measurements produces with these two methods reasonably line up. $0.25\mu m$ SST chip suffers from 30.39 ps (RMS) fixed pattern sampling time non-uniformity. The results and plots of the fixed pattern timing noise for the $0.25\mu m$ SST chip is discussed in section 3.3.9.

Designing the new SST0.18μ chip offered us the opportunity to examine and redesign the sampling clock generation circuit to eliminate fixed pattern sampling interval non-uniformity. Section 4.3.1.1 describes the design improvements made to the sampling clock generation circuit for the new SST0.18μ chip. Very briefly, the "ODD/EVEN pattern is eliminated by

using two sets of tightly interleaved high speed sampling clock shift registers and the timing fluctuation with respect to the feedback node is eliminated by adding dummy buffers and balancing the loads at every shift register regardless of whether it is used as a feedback node or not. In addition to that transmission gates are used so that the rise and fall times are constant and the delays do not translate into timing non-uniformity.

The fixed pattern timing non-uniformity for the SST0.18μ sampling at 3 GHz was measured using zero crossing method. The figure 6.9 shows the cell-to-cell sampling interval deviation from the nominal 333.33 ps. The RMS of the fixed pattern timing non-uniformity is measured to be 8.27 ps.

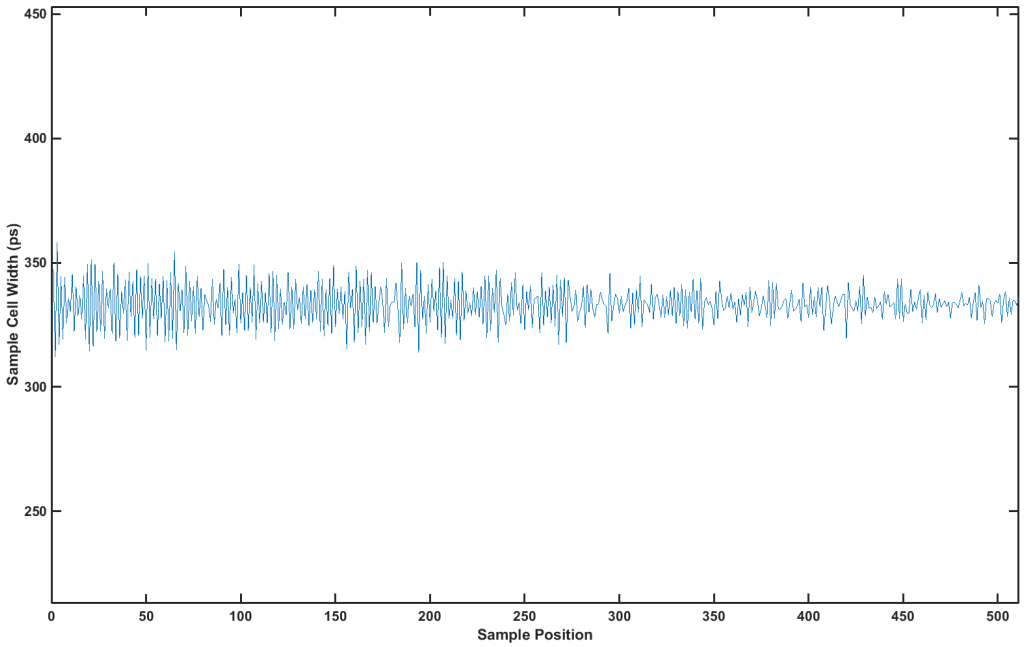


Figure 6.9: Fixed Pattern Sample Interval Non-Uniformity Versus Cell Position

The alternating "ODD/EVEN component in the fixed pattern sampling interval non-uniformity and the large fluctuation at the feedback node is greatly diminished compared to the 0.25μm SST chip. This can be seen in the plot 6.9. However, random non-uniformity, which is caused by the various device noise sources such as flicker noise and thermal noise cannot be elim-

inated and the SST0.18μ is subjected to these variations. The large scale non-uniformity can be seen in the fixed pattern sampling interval variation, and this is attributed to process variations of the chip. The distribution of the random non-uniformity is described by a Gaussian random variable with a mean of 333.33 ps. The histogram of the SST0.18μ fixed pattern sampling interval non-uniformity is plotted in figure 6.10

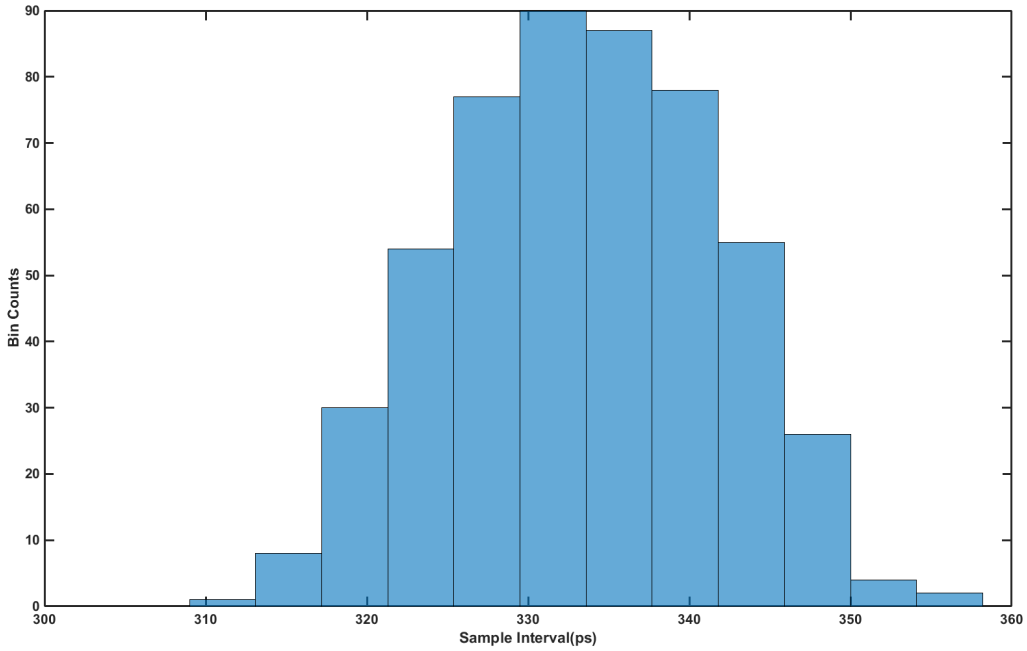
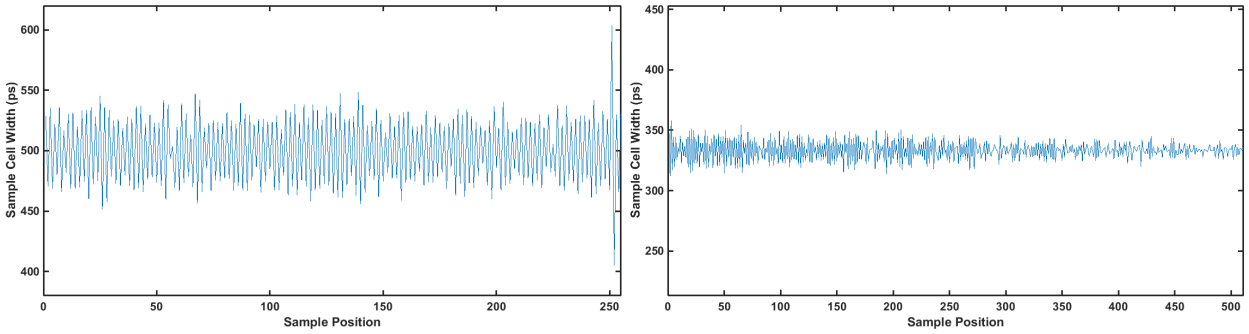


Figure 6.10: Histogram of Fixed Pattern Sample Interval Non-Uniformity for SST0.18μ

6.3.6.1 Comparison of Sample Interval Non-Uniformity between SST0.18μ and 0.25μmSST chip

Normalizing the sample interval error against the nominal sample interval allows for comparison of sample interval non-uniformity between SST0.18μ and 0.25μmSST chips despite different sampling rates. The two sampling interval non-uniformity plots are shown in figure 6.11



(a) FPNT Variation - 0.25μmSST chip (b) FPNT Variation - SST0.18μ chip

Figure 6.11: Comparison of Sampling Interval Variation between SST0.18μ and 0.25μmSST chips

σ for the 0.25μm SST chip is 30.39 ps and σ for the SST0.18μ chip is 8.28 ps. The comparison plots with equal scaling can be seen in figure 6.11. The normalized sample interval error of the SST0.18μ is 2.48% of the nominal interval; whereas the normalized sample interval error of the 0.25μm SST is 6.078%. A clear improvement to the fixed pattern sample interval non-uniformity can be seen. This is mainly due to the re-design of the sampling clock generator to eliminate "ODD/EVEN" fixed pattern variations.

6.3.7 Intra Channel Timing Test

The Intra channel timing measurements were performed by Edwin Chiem, the detailed testing methodologies are presented in his dissertation [19]. The following results were obtained, thanks to the work done by Edwin Chiem after finishing his PhD.

The intra channel timing test, measures the cell-to-cell period variations among recorded sinewaves. The measurement depends on the input frequency and amplitude. The intra channel timing measurements for uncalibrated measurements are shown in the table 6.1.

The intra channel timing rest reveals that the SST0.18μ accurately capture timing features on a single channel with an error of 4.833 ps (RMS) without any calibrations. This resolution

Table 6.1: Intra Channel Timing Test (Period Error) for Various Node Frequencies - SST0.18μ

Frequency	No Timing Corrections
100 MHz	16.31 ps RMS
312.5 MHz	4.833 ps RMS
500 MHz	15.16 ps RMS
833.1 MHz	21.26 ps RMS

was achieved under favorable conditions. Input amplitude was set high to maximize SNR and the input frequency was relative high 312.5 MHz. The SST0.18μ was sampling at 2.5 GSample/s. No timing corrections were performed on the data. The best uncorrected intra channel timing measurements from 0.25μm SST chip was measured to be 8.69 ps for 333.333 MHz sine wave sampling at 2 Gsample/s. We clearly see improvements in the SST0.18μ chip. Figure 6.12 shows the plot of the uncorrected intra channel timing test. The plot also show

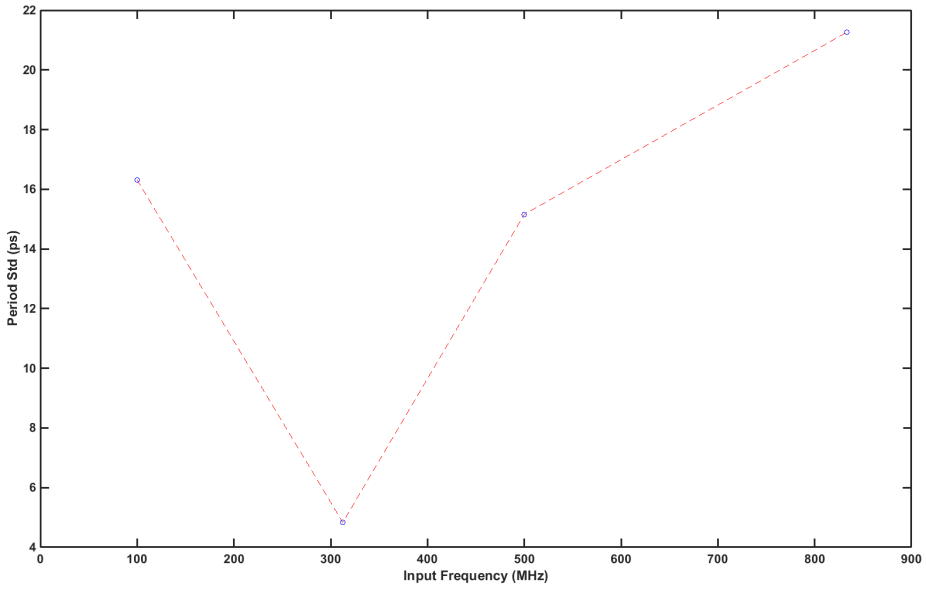


Figure 6.12: Scatter Plot of Intra Channel Timing Test Results for Various Node Frequencies for SST0.18μ

that the intra channel timing test depend on input node frequency. To accurately measure the periods, the input sinusoidal frequencies should be a node frequency of the sampling

frequency. The mathematical calculation for selection of node frequencies is presented in Edwins dissertation [19]

6.4 SST0.18μ Chip Performances

Table 6.2: SST0.18μ Chip Performance

Parameter	value
Technology	0.18 m CMOS, 1.8V
Samples per channel	512
Number of channels	4
Chip size	1.5 by 3 mm
Package size	8 mm by 8 mm
Input clock (typical)	1.5 GHz LVDS
Sample rate typical)	3 GHz
Analog bandwidth	$\sim$1.2 GHz, -3dB
Input-referred temporal noise	$\sim$0.862 mV RMS
Fixed pattern noise	$\sim$2.992 mV RMS

Part III

8-Channel Data Acquisition System

Chapter 7

2017 - 8 channel Data Acquisition System.

As of 2016/17 Austral summer ten SST stations have been successfully installed and collecting data in Antarctica. In order to improve the effective volume of an ARIANNA station, a new 8 channel SST system board was developed for 2017/18 Antarctic campaign. The design of the 8 channel system board was inspired from our already successful 4 channel SST system board designed by Anirban Samanta. The new board is designed to accommodate two SST chips, effectively doubling the number of channels, and giving us the option to configure the stations in a more efficient way. Significant changes were made to the firmware and MBED program. The board design and firmware will be discussed in sections7.1 and 7.2 respectively.

At present, the ARIANNA stations are configured in three different ways; seven hexagonal radio array (HRA) stations are equipped with 4 down-ward facing log-periodic dipole antennas (LPDA) for neutrino detection, two stations have upward facing LPDAs to look for cosmic air showers and one horizontal cosmic ray (HCR) station with LPDAs pointed hori-

zontally towards Mt Discovery for horizontal extensive air showers (EAS). Having more than 4 channels for the neutrino stations allows us to add a set of vertically oriented LPDAs to our stations. This would mean that we would cover all three polarizations, which increases our effective volume, and it will be easier to reconstruct the neutrino direction. The 8 channel stations can also be configured with four down-ward facing LPDAs and four up-ward facing LPDAs, this makes it easier to distinguish between an upward and downward going signal and to tag air shower events so that they do not get mistaken for neutrinos. Simulation results of ten antennas per detector and the response to neutrino signals are presented in [14]. Another motivation for moving to a board with 8 channels is that, we can impose more restrictive coincidence triggers, which lowers the thermal trigger rate and therefore we can lower our trigger thresholds and in turn improve the effective volume of each station.

There has been three major iterations of the system hardware throughout the lifetime of the ARIANNA experiment. The first generation systems were deployed in 2011/12 Austral summer, these stations had 4 channels and the data acquisition was done by ATWD chip. The second generation systems were deployed during 2014/15 Austral summer. These second generation systems had 4 channels per station and housed SST chip for data acquisition. The third generation DAQ systems were designed and built for the 2017/18 season. Here we will describe the third generation system and note that the main motivations behind the majority of changes between the two hardware configurations were reduction of power consumption, eliminating RF noise leaks and improving the effective volume per station.

7.1 Architecture of 2017 Data Acquisition System.

The 2017 data acquisition system uses eight log periodic dipole antennas (LPDA) as receivers, listening to RF pulses. Each of these antennas forms a channel for the SST chip. The SST chip will continuously look for threshold crossings to detect neutrino event. When an input

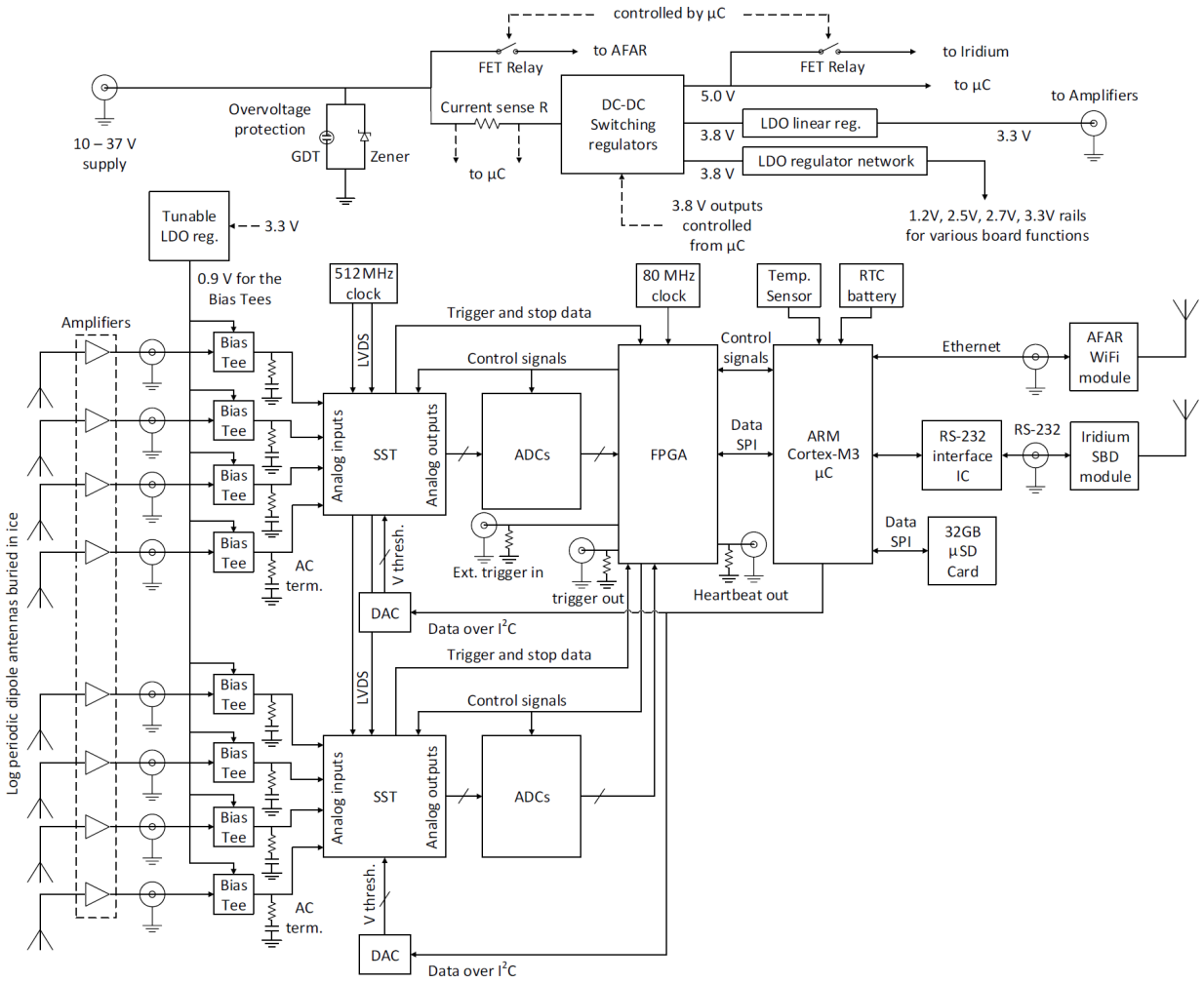


Figure 7.1: Block Diagram of the 8-Ch DAQ System

RF pulse crosses the threshold, the SST chip will trigger an event, which is sent to the on-board Xilinx Spartan 3AN FPGA. After receiving the trigger signal, the FPGA will cease the acquisition phase and begins the readout phase on the SST chip. The sampled analog signal is readout and digitized by the onboard 12 bit TI ADS7886 ADC. The digitized data is forwarded to the FPGA and stored in its block ram. The entire system is overseen by the MBED micro-controller which are based on ARM Cortex-M processors. The MBED later forwards the data form FPGA to the /*mu*SD card. The data acquisition system samples at 1 Gsamples/s using a 512MHz clock. The FPGA controls the SST chip independently, allowing the MBED to perform other critical functions. The system features a secure digital

standard capacity (SDSC) card storage for digitized data and various other readings. The system also features two modes of communications, wireless AFAR Ethernet Bridge and Iridium Short-Burst-Data (SBD) satellite communications module. Figure 7.1 shows the architecture of the data acquisition system.

7.1.1 Data Acquisition Board.

The data acquisition board was developed using PCB artist software by Advanced Circuits. The PCB artist software was chosen for two main reasons, first, most of the component footprints were readily available and could be imported from our second generation board, second, Advanced Circuits is the third largest printed circuit board manufacturer in North America and they offer full-service printed circuit board manufacturing, full CAM review, IPC-A600 Class 2 review and very convenient assembly service.

The following sub-sections briefly discusses the power distribution circuitry, SST peripheral circuitry, FPGA peripheral circuitry, communication and housekeeping circuitry of the data acquisition board. The following sub-sections also discusses the updates made for the new 2017 data acquisition board.

7.1.1.1 Power distribution circuitry

The Power distribution circuitry was mainly unchanged from the second generation DAQ board. Figure 7.2 shows a detailed map of the power distribution circuitry for the DAQ board.

To safeguard the system from power supply overvoltage, the 12V power supply is distributed to DAQ board via an overvoltage protection circuitry. The board is protected from overvoltage conditions with a combination of Gas discharge tubes (GDT) and Zener diodes. Gas

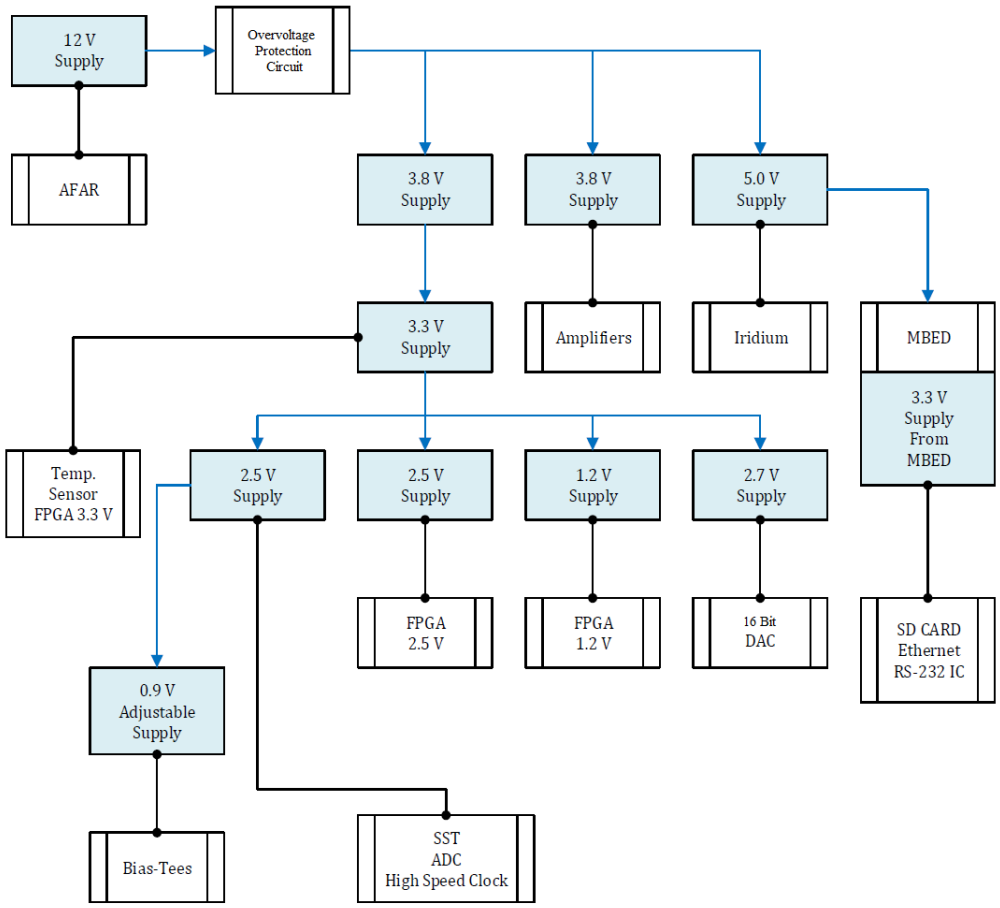


Figure 7.2: DAQ Power Distribution Map [1]

discharge tubes are usually formed with a ceramic body filled with gas mixture containing neon and argon. DAQ board is protected by 60V, 2 pole, surface mount Bourns Inc. GDT. When the voltage across the electrodes exceeds 60V, and arc occurs within the tube, providing a low current path. Gas discharge tubes have the bidirectional crowbar I-V curve similar to a bidirectional thyristor. The GDTs are best used as primary protection device in conjunction with other faster turn on and lower voltage secondary protection elements like Zener diodes. The 2017 DAQ board is equipped with two Littelfuse Inc. SMBJ40A Zener diodes rated to 40V. The Zener diodes are used as transient voltage suppressors optimized for carrying high currents, tailored for 40V breakdown voltage. The Zener diodes provide protection with a combination of forward bias and reverse bias breakdown conduction. After

[1]The schematic originally published in [50]

the overvoltage protection circuitry, three Texas Instruments LMZ14202 DC-DC converters are used to convert 12V to 3.8V, 3.8V and 5V power supplies to be used for SST, FPGA and MBED and their peripheral circuitries.

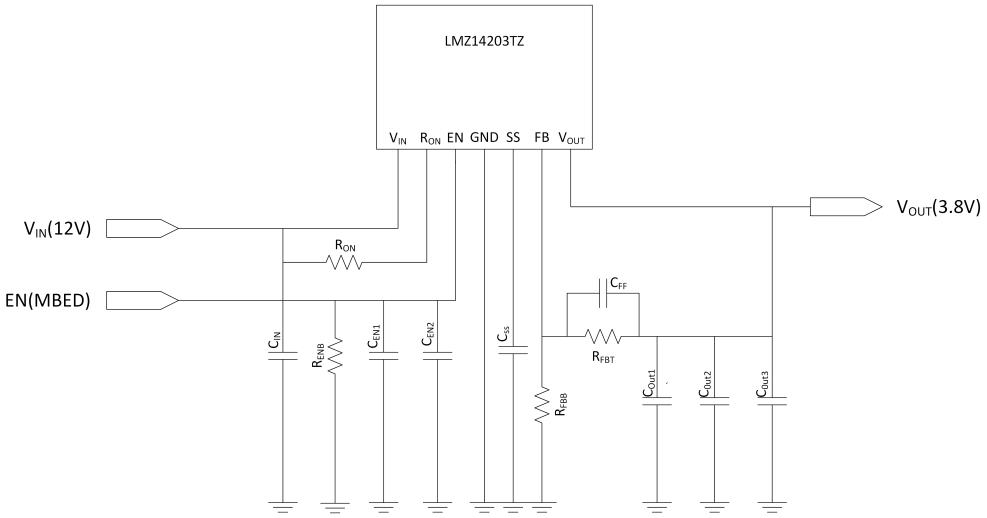


Figure 7.3: Power Switching Circuitry

Figure 7.3 shows the schematic of the power switching circuit. The regulated output voltage is determined by the resistor divider circuit connected between the output and ground. The midpoint of the divider is connected to pin 6 (FB). The regulated output voltage is determined by the equation 7.1.

$$V_O = 0.8V \times \left(1 + \frac{R_{FTB}}{R_{FBB}}\right) \tag{7.1}$$

This system was designed by Anirban Samanta [50] for our second generation DAQ system, however some changes were made in the current design in terms of layout and signal routing.

Furthermore, linear regulators are used to generate the required 2.5V, 1.2V and 2.7V for FPGA, SST, and 16 bit DAC chips. A band gap regulator is used to generate bias voltage of 0.9 V for the bias-tees.

7.1.1.2 SST and peripheral circuitry

Based on the results of our functionality test board explained in section 3.2.1 similar design choices were employed for the second and third generation DAQ boards. Great care was taken to minimize the loss and parasitic, the surface mount capacitors were placed very close to the chip to reject high-frequency noise and the analog signal lines were matched to $50W$. Equations presented in section 3.2.1 were used to calculate the trace widths of the analog signal lines. Bias-Tee with AC termination show in figure 3.3c were used to offset the incoming analog signal. The control signals such as read clock, differential single ended select, reset, AND OR select signal and stop signal are asserted and de-asserted by the FPGA. The bias voltages for the comparators, source follower circuit, low voltage differential signaling circuit and control voltage for trigger delay lines are adjusted by surface mount potentiometers. All the n-mos bias are referenced to GND and p-mos biases are referenced to VDD.

The threshold voltages for the SSTs are provided by two 16 bit I^2C based Linear Technologies LTC2657 Digital to Analog Convertor (DAC). The DAC has a full-scale output of 2.5V with the integrated reference and operates from a single 2.7V supply. The DAC is controlled by MBED using a 2-wire I^2C compatible interface. The linearity and monotonicity for the DAC is defined from code 128 to code 65535. The DAC features power-on reset circuit which is controlled by $PORSEL$ (pin 14) and $REFLO$ (pin 1). The DAC resets to Zero-Scale at power up if the $PORSEL$ and $REFLO$ are tied to GND.

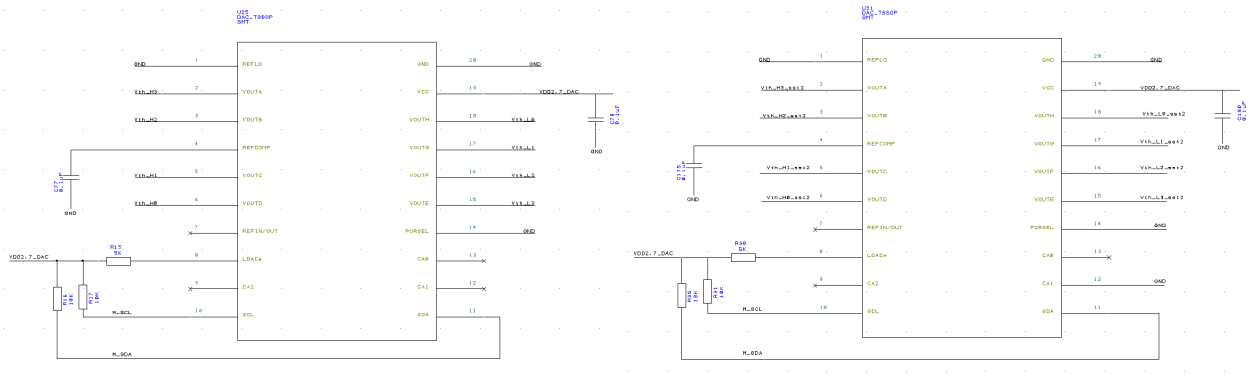
Unlike our second generation DAQ board, we have two DAC chips on the DAQ board. I^2C slave addresses should be assigned to each of the two DAC chips so that right threshold values can be set on all 16 channels. The state of the chip address pins $CA0$ (Pin 13), $CA1$ (Pin 12) and $CA2$ (Pin 7) decides the I^2C slave address for the DAC. Each of these three pins can be set to any one of three states, V_{DD}, GND and $FLOAT$. The slave address

assignments for the two DAC chips are shown in the table 7.1

Table 7.1: Digital to Analog Converter Slave Address Assignments

CA2	CA1	CA0	ADDRESS
FLOAT	FLOAT	FLOAT	1000001
FLOAT	GND	FLOAT	0110010

The DAC communicates with the MBED using the standard I^2C interface. The two busses SDA (pin 11) and SCL (pin 10) are used for communication between the DAC and MBED. The two busses SDA and SCL, must be high when the bus is not in use, external pull-up resistors are required on both SDA and SCL. The values of the pull-up resistors depend on the power supply and are obtained from I^2C specifications [2]. The connections and configurations for DAC chip 1 and DAC chip 2 are shown in figure 7.4



(a) DAC Chip 1

(b) DAC Chip 2

Figure 7.4: Schematic and Configuration of DAC Chips

7.1.1.3 FPGA Peripheral Circuitry

The DAQ board uses XILINX Spartan 3AN XC3S50AN FPGA. The 3AN family FPGAs includes SPI-based serial In-System Flash (ISF) memory. The memory consists of a main non-volatile reprogrammable flash memory array and one SRAM page buffer. The ISF memory in the FPGA is primarily designed to automatically configure the FPGA with

ARIANNA firmware when power is applied or the DAQ board is reset. This is one of the important features used by the ARIANNA experiment. An Abracon ASFLMB 80MHz oscillator is used to assert the clock signal to the FPGA. Exceptional care is taken in placing a large amount of decoupling capacitors around the periphery of the FPGA so as to provide a clean and stable power supply. The Spartan 3AN family FPGAs support a wide variety of I/O standard interfaces. The current system uses the LVCMOS single ended I/O standard. All the MBED interface signals use LVCMOS33 I/O standard which has a nominal voltage of 3.3V and the SST interface signals use LVCMOS25 I/O standard which has a nominal voltage of 2.5V. Few pins control the configuration process of the FPGA, the mode select pins M[2:0] (Pin 39, Pin 37 and Pin 38) define the configuration mode that the FPGA uses to load its configuration data. The DONE pin (Pin 73) indicates the successful completion of loading the configuration data. The program pin, PROG_B (Pin 144) initiates the configuration process, this pin forces a master reset on the FPGA. CCLK (Pin 72), INIT_B (Pin 67) and PUDC_B (Pin 143) are few other configuration pins, not used in the current configuration mode. Spartan 3AN family FPGAs can be configured in 7 different ways. The logic levels applied to the mode select pins define the configuration mode of the FPGA. Table 7.2 shows the FPGA configuration modes for Spartan 3AN family.

Table 7.2: Mode Pin Settings and Associated FPGA Configuration Modes

M[2]	M[1]	M[0]	Configuration Mode
0	0	0	Master Serial Mode
0	0	1	Master SPI Mode
0	1	0	BPI Up
0	1	1	Internal Master SPI
0	0	0	Reserved
0	0	1	JTAG Mode
0	1	0	Slave Parallel Mode
0	1	1	Slave Serial Mode

For the current design the mode pins are set to Internal Master SPI mode.

7.1.1.4 MBED Peripheral Circuitry

High performance NXP LPC1768 based MBED microcontroller, with a 32-bit ARM cortex-M3 core running at 96MHz is used to control the whole system. The microcontroller includes 512 KB FLASH, 32KB RAM, built-in Ethernet, USB Host and device, CAN, SPI, I^2C, ADC, DAC, PWM and other I/O interfaces. The MBED microcontroller oversees all the configuration, communication and house-keeping functions of the DAQ board. The MBED also oversees the data transfer from the FPGA to the 32GB μSD card for long term data storage, in addition to that, the MBED controls the relay switches to control the power supply for the amplifiers, AFAR wireless Ethernet bridge and Iridium satellite communication modules.

7.2 Firmware Design

The firmware for the 2017 data acquisition system went through a complete overhaul, major optimizations were made to the clock generation and synchronization logic, SST control logic, majority logic block and data storage architecture. To maintain consistency and backward computability, the firmware was designed in Xilinx ISE environment.

Figure 7.5 shows the schematic of the firmware designed for the 2017 DAQ board. The firmware consist of three main blocks, Clock generation and synchronization block, SST control and majority logic block and data storage logic.

7.2.1 Clock Generation and Synchronization Logic

An external 80 MHz oscillator is used to generate all the internal clocks of the FPGA. A low jitter 80 MHz Abracon ASFLMB oscillator is used for this purpose.

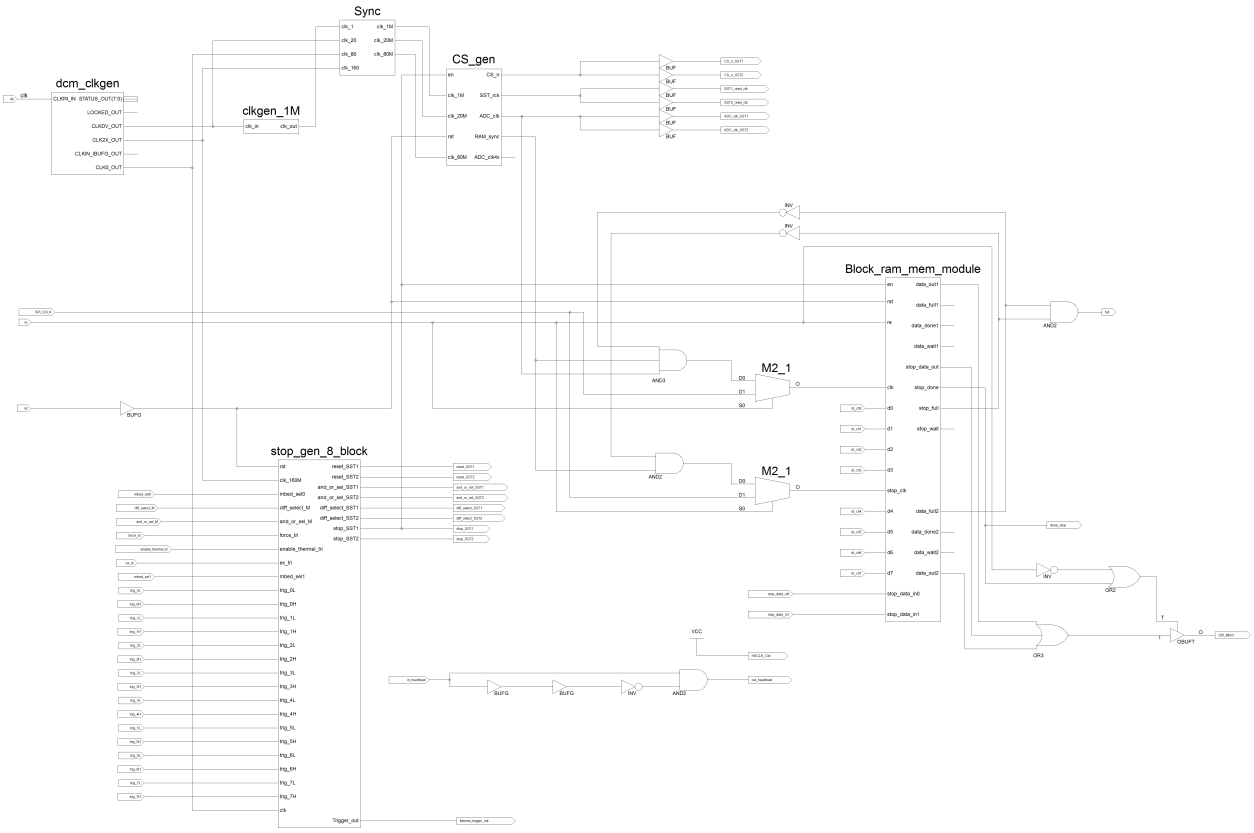


Figure 7.5: Firmware System Overview

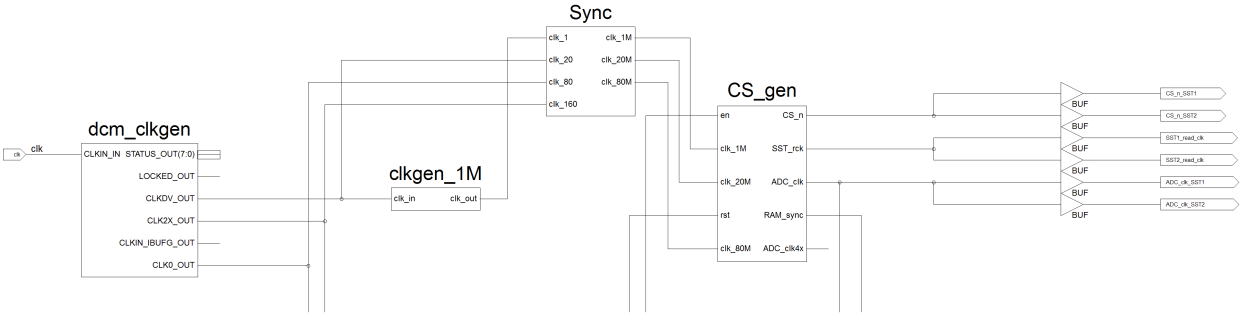


Figure 7.6: Clock Generation and Synchronization Logic

The clock generation and synchronization logic can be seen in the figure 7.6. The clock generation circuit generates readout clock for the SST, ADC clocks and data write clock.

The DAQ firmware takes the advantage of Xilinx Digital Clock Manager (DCM) primitive to synthesize new clocks from the incoming clock signals. The DCM primitive integrates advance clocking capabilities into the FPGA clock distribution network, few of which are;

conditioning the clock to ensure 50% duty cycle, elimination of skew to improve the overall system performance and re-buffer the clock signal often to deskew and to convert the incoming clock signal to a different IO standard. Although, DCM offers multiple functionalities, the DAQ firmware takes advantage of clock divider and clock multiplier circuit. The 80 MHz external clock is sent to the DCM primitive, which generates three different clocks with 50% duty cycle; a 20 MHz clock, 160 MHz clock and an 80 MHz clock. The 20 MHz clock is further divided 32 times to generate 625 KHz clock. All the clocks are synchronized to 160 MHz clock using two flip-flop and three flip-flop strategies to avoid metastability. Figure 7.7 shows the synchronization logic used in the DAQ firmware.

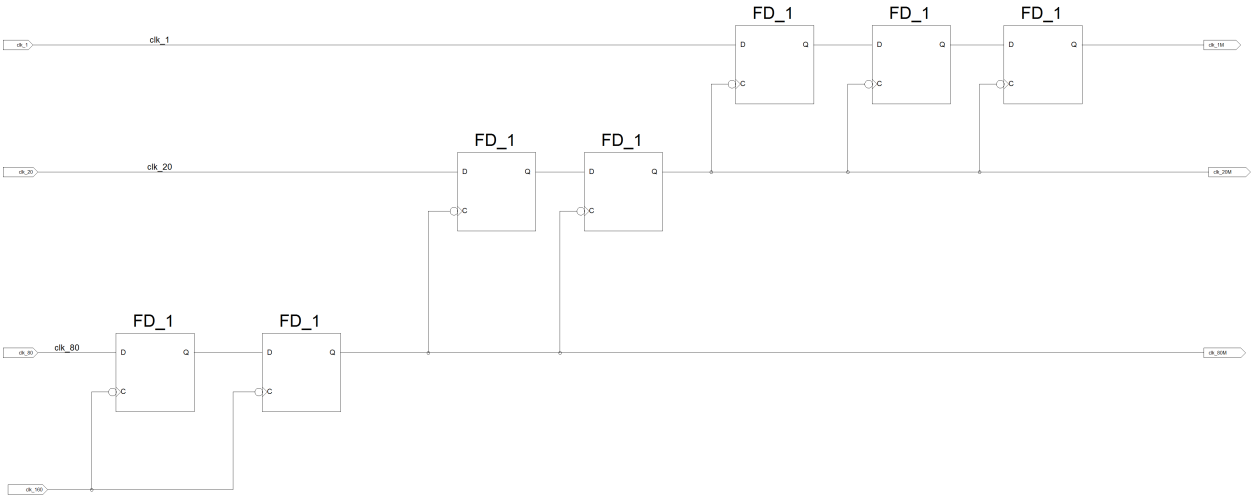


Figure 7.7: Synchronization block

Quoting, Dally and Poulton [21]:

> A synchronizer is a device that samples an asynchronous signal and outputs a version of the signal that has transitions synchronized to a local or sample clock.

The DAQ firmware employs the simplest and most common synchronization circuit - "Two Flip-Flop Synchronizer". The first flip-flop in the synchronization circuit samples the asynchronous clock to the new clock domain and waits for one clock cycle to allow the metastability to decay, the second flip-flop then samples the output of the first flip-flop at the same

new clock domain, thus making sure that the new clock signal is stable and synchronized to the new clock domain. The synchronization circuit in the firmware shown in figure 7.7 synchronized all the clocks to 160 MHz clock. It is necessary to synchronize all the clocks in the firmware as they are used for ADC clocking and write clock for sample data. A very basic two and three flip-flop synchronization techniques are used to synchronize the clocks.

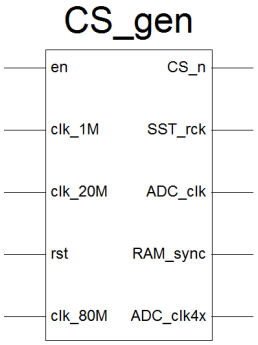


Figure 7.8: SST and ADC Clock Generation Block

The last block in the clock generation and synchronization logic is the CS_gen block shown in the figure 7.8. The CS_gen block generates ADC chip select signals and ADC clocks for data transfer. The chip select signal (CS) and ACD read clock (SCLK) are the two clocks required by the ADC to transfer the digital data back to the FPGA. The CS_n clock is a 625 KHz clock and ADC_clk is a 20 MHz clock. The CS_gen block also generates a 625 KHz SST read out clock. The RAM_sync clock and the ADC_clk is used by the data management bock in the firmware to store the data arriving from the ADC.

7.2.2 SST Control Logic Block

All the control signals required by the SST is generated by the SST control logic block. The SST control logic block is also equipped with second level triggering (i.e., merging multiple channels triggering) for majority logic selection. The signals for the SST control and logic block is shown if the figure 7.9.

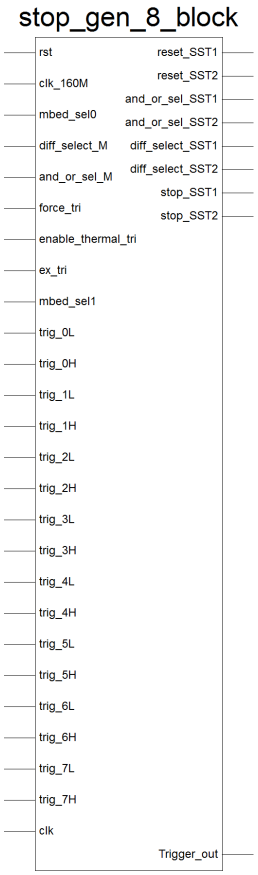


Figure 7.9: SST Control Logic Block

The SST control logic block consist of Trigger encoder & majority logic circuitry and stop generation circuitry.

7.2.2.1 Trigger Encoder & Majority Logic Circuitry

Trigger encoder and & majority logic circuity generates all the control signals required for the SST except STOP signal. Figure 7.10 shows the trigger encoder & majority logic circuitry. Based on AND_OR_SEL signal and DIFF_SELECT signal, asserted by the MBED, the trigger encoder block conditions all the 16 triggers to be used for the majority logic block. For example, if DIFF_SELECT signal is high, the all the trigger HIs are considered as dontcare and all the trigger LOs are passed on to the majority logic. However if the DIFF_SELECT signal is low, the trigger encoder block encodes the triggers of each

channel based on AND_OR_SEL signal. For example if DIFF_SELECT signal is low, and AND_OR_SEL signal is high, the LO and HI triggers of each channels are ANDed together to generate the output of the trigger encoder block, similarly, the HI and LO triggers of each channels are ORed together to generate the output if both DIFF_SELECT signals and AND_OR_SEL signals are low.

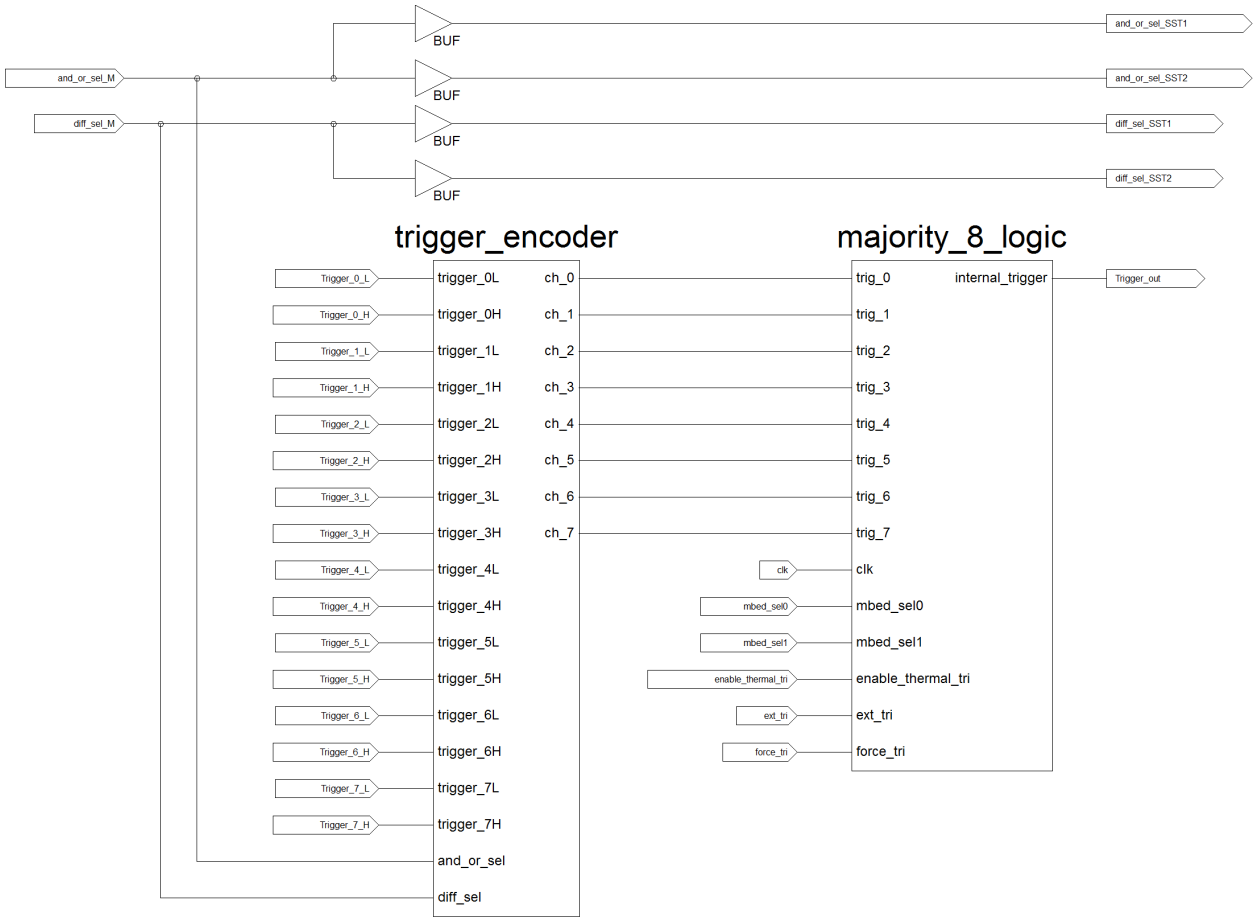


Figure 7.10: Trigger Encoder & Majority Logic Circuitry

The majority logic block produces a STOP signal which terminates the acquisition phase of the SST and initiates the readout phase. The majority logic block looks at the majority conditions asserted by the MBED and the STOP signal is generated when these conditions are met. At any given time, the MBED can request the firmware to check 4 of 8 majority conditions. The firmware is equipped to check 1 of 8, 2 of 8 and all the way up to 8

of 8 majority logic (i.e., coincidence triggers). For the 2017 deployment, the firmware is programmed to check for 1 of 8, 2 of 8, 3 of 8 and 4 of 8 coincidence triggers. The signals mbed_sel1 and mbed_sel0 defines the number of coincidences. For example if mbed_sel1 and mbed_sel0 are "01" then the majority logic block will assert the STOP signal when any two of eight channels trigger within a coincidence time of 187 ns, similarly if mbed_sel1 and mbed_sel0 are "11" then the majority logic block will assert the STOP signal when any four of eight channels trigger within a period of 187 ns.

Designing majority logic using AND-OR gates for 8 channels is impractical, at least 2^8 gates are required to realize the logic. A more efficient alternative design was employed to implement the majority logic. A combination of ones counter, logic gates and de-multiplexer is used to design majority logic block. Ones counting, in this case trigger counting can be easily described by behavioral design, however most of the logics are very slow and inefficient. A more efficient architecture of ones counter was designed and realized. Figure 7.11 shows the architecture of the ones counter used in the firmware. A full adder (FA) (fulladder1) adds three input bits to produce a 2-bit sum, the pair of 2-bit sums are combined in a 2-bit adder (fulladder2), and the carry input of the 2-bit full adder is included to add another bit. Finally, separate 4 bit incrementer is used to add the last trigger bit. A very fast 8-bit ones counter shown in figure 7.11 is designed to count the triggers.

The output of the ones/trigger counter is a 4 bit unsigned integer, a combinational logic is used to compare the output of the trigger counter and de-multiplexed mbed select signals to generate appropriate trigger output. Three other signals, ext_tri, force_tri and enable_thermal_tri are used to control the output trigger. The signal ext_tri is just an SMA connection to the data acquisition board, this signal is used during debugging and forcing the SST to stop acquisition phase. The force_tri signal asserted by the MBED and is used when data has to be taken continuously, the force_tri signal is mostly used to take data for voltage fixed pattern noise calibration and timing fixed pattern calibration. The final trigger

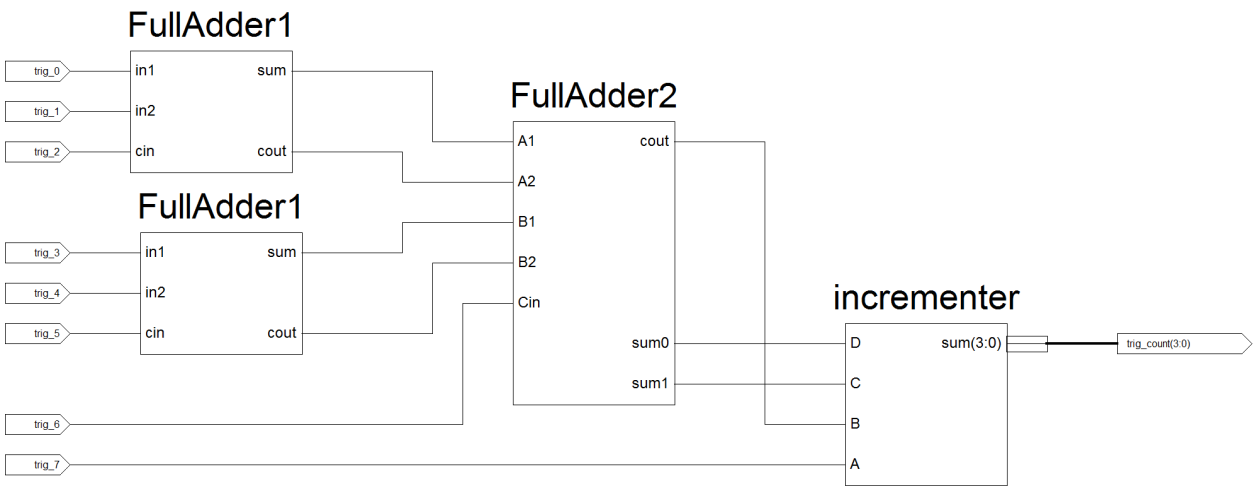


Figure 7.11: Majority Logic Trigger Counter Circuit

control signal enable_thermal_tri, as the name suggests, is used to enable or disable the thermal triggers. The trigger_out signal of the trigger encoder & majority logic circuitry is used to generate the STOP signal which is required for the SST to stop the acquisition phase and start the readout phase. It is very important not to assert the STOP signal immediately, the tail end of the analog data is lost if the STOP signal is asserted immediately. Figure 7.12 shows an example of a neutrino template, for example if the DIFF_SEL and AND_OR_SEL signals are LO, for the analog signal shown in the figure 7.12 the trigger is asserted when the analog signal crosses the high threshold which is at around 22 ns. Say, for example if the STOP signal is asserted immediately, the acquisition of the analog waveform will cease and we will lose the tail end of the signal. So to makes sure that the whole analog signal is sampled, assertion of STOP signal is delayed by few ns.

This specific delay can be adjusted in the firmware, and it depends on the sampling speed of the SST. For the 2017 ARIANNA deployment, all the SST chips are sampling at 1 giga-samples per second. For sampling speeds of 1 giga-samples per second, the channel length is 256 ns. The default delay for the 2017 deployment is set to 187 ns. As shown in figure 7.13, two 16 bit shift registers (SRL16) are used to adjust the delay. The delay can be customize by changing the number of flip-flops in the 16 bit shift register. The delay can be customized

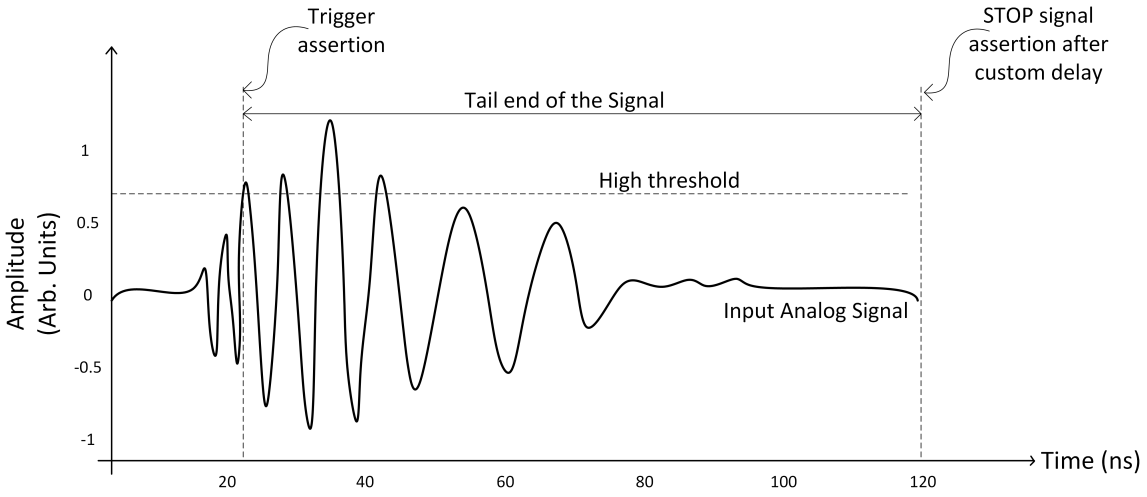


Figure 7.12: STOP Signal Delay Requirement

from 12.5 ns to 200 ns in increments of 6.25 ns (160 MHZ). The final stoplatch_SCH circuit synchronizes the reset and trigger to the 80 MHz clock to generate a STOP signal to be sent to the SST. The STOP signal acts as an enable to the CS_gen block and memory storage block.

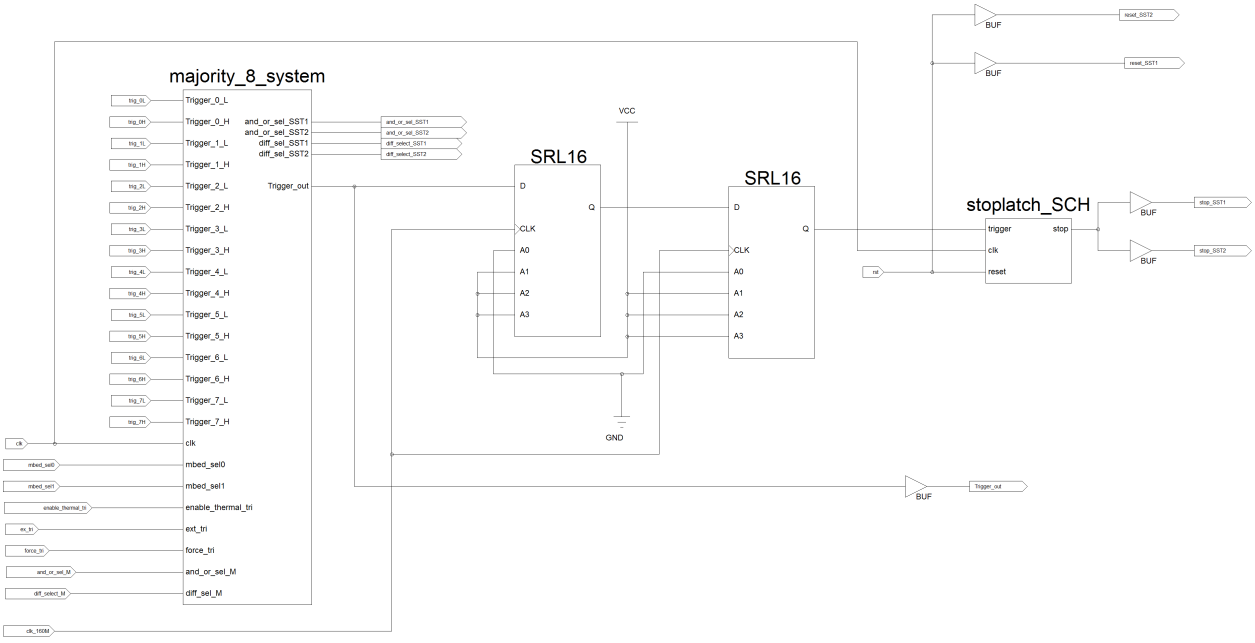


Figure 7.13: Generation of STOP Signal

7.2.3 Memory Storage Block

Memory storage block in the firmware is designed to store the sampled data from all 8 channels and the stop data of two SST chips. The firmware will wait for trigger signal either thermal, external or forced, once the trigger signal arrives to the FPGA, the firmware generates a STOP signal after waiting for 187 ns. This STOP signal is used as an enable for SST readout clocks, ADC clocks and memory storage block. The memory storage block essentially collects all the data from the ADC and stores it. The memory storage block then sends a memory FULL signal to MBED, informing it that the data is available to readout. The memory block then waits for the MBED to collect the data. When the MBED is ready to collect the data, it asserts read enable "re" signal and activates the SPI clock. A 10 MHZ SPI clock is applied to the FPGA to readout the stored data.

Figure 7.14 shows the logic of the memory storage including all the clocks and control signals. The memory block uses three control signals (enable (en), reset (rst) & read enable (re)), two clocks (sample data clock (clk) & stop data clock (stop_clk)) and ten serial data lines (data of channel 0 through data of channel 7, stop data of SST chip1 and stop data of SST chip2).

The control signal en is an active low signal, the memory storage block is turned on when the en is low and the memory storage block is turned off when the en is high. Signal en is nothing but the STOP signal generated by the SST control logic block. The re signal is active high, when re is low, the memory storage block is storing the ADC sampling data and SST stop data. However, when re is high, the memory storage block stops writing and starts reading out the stored data to the MBED.

The memory storage block requires three different clocks. Two clocks for writing operation and one common SPI clock for reading. Consider writing operation the two clocks are necessary since the channel data is clocked at a higher rate than the stop data from the

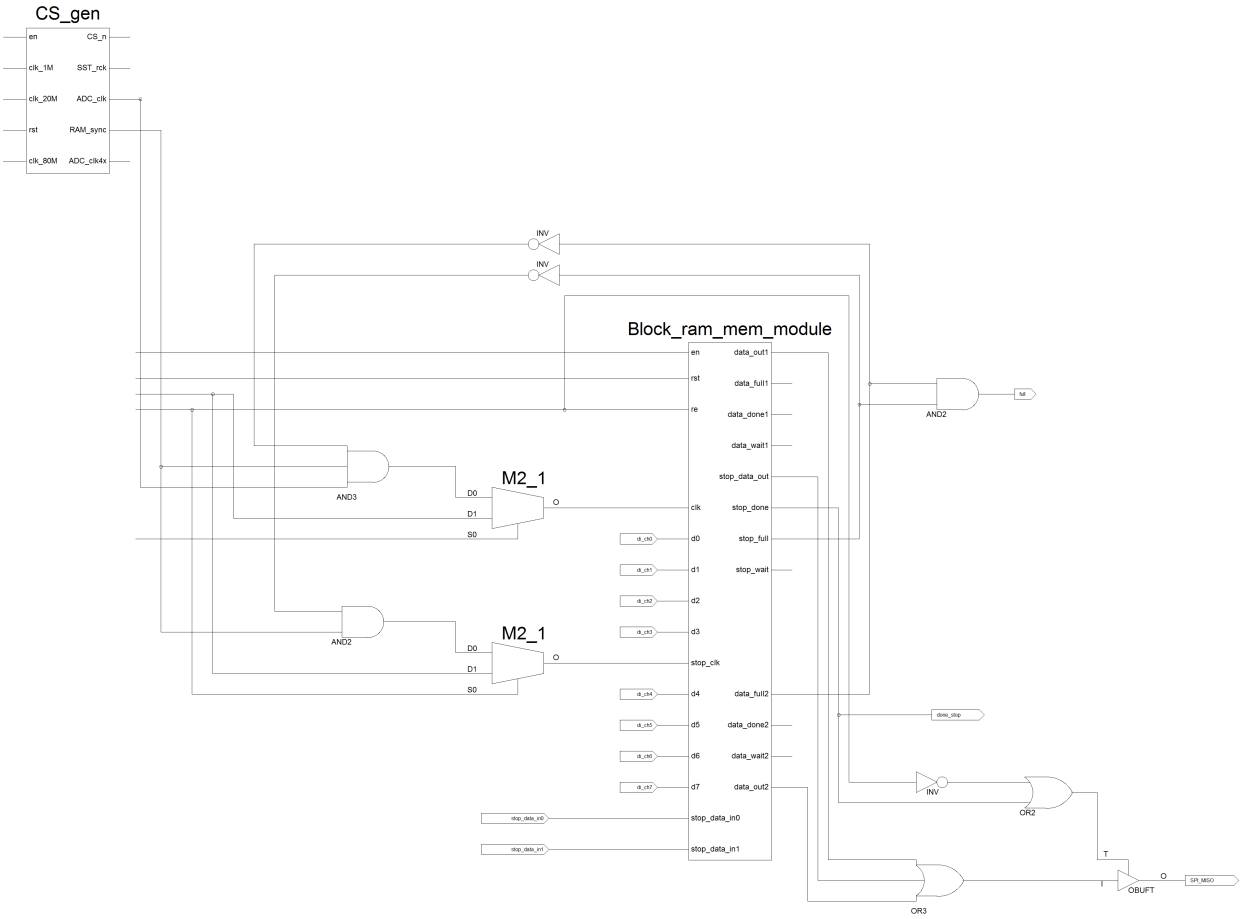


Figure 7.14: Memory Storage Block

SST. The sample data clock (clk) runs at 20 MHz and stop data clock (stop_clk) switches at 625 KHz. A common 10 MHz SPI clock is used to readout the data, based on "re" control signal, the two muxs M2_1 will select the SPI clock to be sent to the memory storage block.

The data lines di_ch0 through di_ch7 are the 8 channels' data input from the ADCs. The signals stop_data_in0 and stop_data_in1 are the inputs from the two SST chips' STOP readout data.

Spartan 3AN FPGA is equipped with 18Kbits (16 K data and 2K parity) Block Ram. The memory can be organized in few different ways. Table 7.3 shows the different ways of memory organization for the Spartan 3AN FPGA.

Table 7.3: Spartan 3AN Memory Organization

Spartan 3AN FPGA	Organizations
Memory organizations	16K × 1
	8K × 2
	4K × 4
	2K × 8
	1K × 16
	512 × 32

Figure 7.15 shows the logic of the memory storage block. The memory storage block consist of address controller which generates the right addresses for the bock ram, and other MBED-FPGA handshaking signals. The handshaking signal data_full will go high when all the data has been written to the RAM during the writing phase. Similarly, data_done will assert when the readout of all the bits are complete. Data bits d0 through d3 belong to the first SST chip, all the ADC data is concatenated together to be sent to the block ram block.

There are 16 bits of data per sample and there are 256 samples per channel and totally there are 8 channels. So in total there are 32768 data bits. The best way to organize this large data is to have two 4K × 4 block rams each capable of holding 16384 bits. The concatenated data is written into to block ram in 4 bit chunks. Similarly the stop block ram is used to store the stop data from the SST chips. The stop block ram is organized in 8K × 2 chunks. Each SST chip has 256 stop data and in total we have 512 bits of SST stop data. To summarize, we totally have 33280 bits of data per event.

The writing process for the bock ram is concurrent. The sampling data from all the channels arrive in parallel and the data is written simultaneously. However, the read process is different when compared to the write process. The reading is done through SPI protocol. When the MBED is ready to read the data, read enable (re) signal is set and SPI clock is applied. The first address controller starts counting the addresses from the beginning and repeating four times while incrementing the 2-bit count value every time. Once all 4

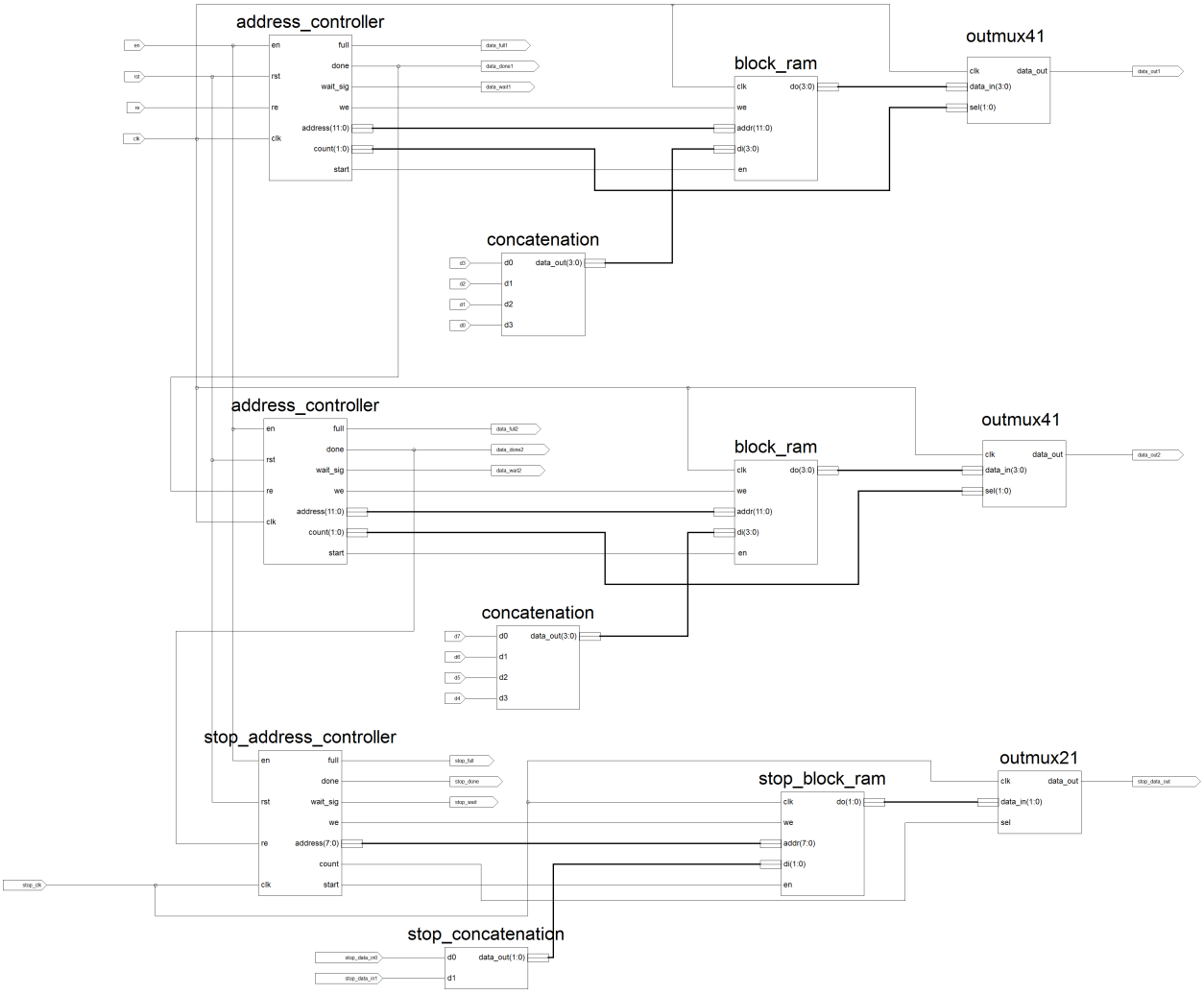


Figure 7.15: Memory Logic

channels of data are sent out the done flag is asserted, this done flag in-turn is becomes the read enable signal for the next chip, and the process continuous for the stop data.

7.2.4 Heartbeat Signal

Like the previous generation DAQ board, this system also features a fast pulse generator called as the "heartbeat" signal. This pulse generator was designed by Linag Zou [57] and employs a simple edge detector mechanism. The heartbeat signal is included in this thesis for completion. The logic is shown in the figure 7.16.

Figure 7.16: Heartbeat Pulse Generator

The input for the heartbeat pulse generator is a regular square wave pulse from the MBED, which is fed into two signal lines, one of which is delayed. The resulted signals are then ANDed together to generate a heartbeat signal.

7.3 High Voltage DC-DC Converter Module for the South Pole ARIANNA Station

At present, there are two high energy radio neutrino experiments in Antarctica - ARIANNA and ARA (Askaryan Radio Array). In January of 2017, at the weiznamm workshop, the collaborators of ARIANNA and ARA discussed potential to transfer the ARIANNA hardware to the South Pole (ARA Site). The theoretical physics community has targeted a flux of $10^{-9}\frac{GeV}{cm^2 ssr}$ at 10^{18} ev as the critical number where the lack of observation has theoretical significance. Getting to $10^{-9}\frac{GeV}{cm^2 ssr}$ will be a challenge. For ARIANNA it will most likely require 5 years of operation in Moores Bay and for ARA it is even more challenging since it likely requires approximately 370 stations. The collaborators decided that there is a non-trivial expectation that the things can improve for the better by transferring ARIANNA technology to the South Pole.

Installing ARIANNA stations in South Pole means that we can use the power grid available and not use the solar power. With the use of the power grid, the cost of the ARIANNA station will reduce drastically, we no longer need towers, solar panels, battery unit and battery management unit (BMU), also since ARIANNA uses less power ($<$ 5kW for 1000 stations) the power cables used can be smaller and less expensive.

A fan out of 400V DC power is available at the South Pole. Since the ARIANNA station requires input voltage in the range of 12V to 40V, a DC-DC power converter circuit was designed to convert 400V to 28V. An isolated VICOR DC-DC converter with V_{OUT} of 28V and V_{IN} range of 200V to 400V is used to design the power converter circuit. The VICOR DCM is rated to $-55\,°C$. A "DCM300P280x500A40" was used to design the circuit. The DCM circuit operates from an unregulated wide range input to generate an isolated 28V Vdc output. Filter circuits were designed on the input and output side to reduce the noise. The input and output pins of the VICOR DCM is shown in figure 7.17.

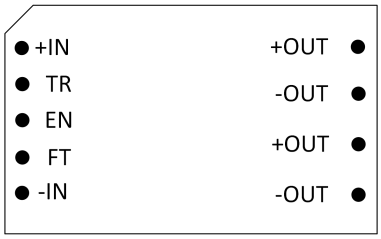


Figure 7.17: VICOR DCM Pin Outs

The VICOR DCM has 7 pins. +IN and IN are the positive input power terminal and negative input terminal. Pin TR enables and disables trim functionality, the pin adjusts the output voltage when trim is active. Pin EN enables and disables the power supply and pin FT is an output pin for fault monitoring. +OUT and OUT pins are the positive and negative power terminals respectively. For the ARIANNA DC-DC power converter, pins TR, EN and FT are not connected.

For demanding applications like the ARIANNA experiment, VICOR converters require external input/output filtering. The DC-DC converter circuit has single stage high-voltage filter on the input side and two stages of filtering on the output side of the VICOR DCM module. A filter network is generally required for the DC-DC converters to have low electromagnetic interference (EMI) and high input noise rejection. The high voltage power supply usually have switches, a basic EMI suppression specific to the power supply is practiced so that the interference with other parts of the system is minimized. For ARIANNA South

Pole station, filtering is designed for both input and output ends and the complete system is shielded to enclose all the noise sources so that sufficient EMI attenuation is achieved.

7.3.1 Input Filter Design

Input filter design of the DC-DC power converter circuit has a structure shown in figure 7.18. The input filter serve to both eliminate noise from the supply and to prevent noise being fed back to the supply.

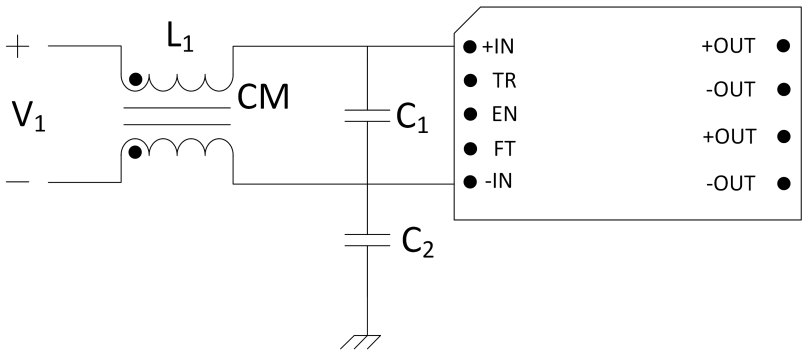


Figure 7.18: Input Filtering Circuit for the DC-DC Power Converter Circuit

Conducted noise on the input power line can appear as either common-mode or differential mode noise currents. Common-mode noise, which are mostly high frequency content is measured between the converters input conductors and ground. Differential-mode noise is mostly low frequency content and it appears at the converters input conductors. It comprises of fundamental switching frequencies and its harmonics.

The VICOR DCMs have an internal differential mode LC filters which in conjunction with external input capacitor, C_1 in figure 7.18 reduces differential-mode conducted noise.

The most effective way to reduce the common-mode noise is to bypass both input leads to the VICOR DCM to the chassis using capacitors, C_2 in figure 7.18. Additionally, a common-mode choke (L_1) is also used to further reduce the common-mode noise. In general common-

mode choke is the inductor of choice for EMI filters, since it offers better attenuation.

A common mode choke is a power magnetics component which is widely used to filter electromagnetic interference (EMI) currents without falling apart under high currents and without causing signal degradations. The common mode chokes are applied to hot and return pairs of conductors and are ideal for EMI filtering for power lines. It is essentially an inductor that is used to block high-frequency noise in a circuit while allowing lower frequencies. The common mode choke normally consist of insulated wire that is wound around a magnetic core. The common mode chokes are very useful for the prevention of electromagnetic interference (EMI) and radio frequency interference (RFI) from power supply lines. For the ARIANNA DC-DC power converter circuit, a 1 mH Bourns 8108-RC common mode choke was used for filtering circuit. The Bourns chokes offers excellent EMI suppression capability over wide frequency spectrum, high current capacity, dielectric strength of 1500 Vrms and is capable of operating at $-55\,^{\circ}\mathrm{C}$.

There are a variety of different types of capacitors available in the market, ARIANNAs main concern is that the capacitance should not degrade at very low temperatures ($-60\,^{\circ}\mathrm{C}$). Film capacitors, tantalum capacitors and low temperature ceramic capacitors with class II (X7S) dielectric materials have been chosen to build the DC-DC power converter circuit. These capacitor materials are known to be very stable at low temperatures.

Film capacitors basically consist of two metal foil electrodes that are separated by an insulating plastic film. The film capacitors offers high insulation resistance, excellent current carrying and pulse handling capability and good capacitance stability at very low temperatures. Vishay offers a 10 μf 600V high density film capacitor, which are used in the input filtering circuit.

7.3.2 Output Filter Design

The output filtering is actually taken care in the VICOR DCM. According to the datasheet only an external capacitor ($C_{OUT\_EXT\_TRANS}$) is adequate for output filtering. For applications like ARIANNA, noise is of major concern. Two stages of external LC filter circuits are added on the output side. Figure 7.19 shows the filtering circuit on the output side. The LC filter design shown in the figure 7.19 is a comparatively simple solution to reducing ripple on the outputs of the converter modules. Together with the VICOR DCMs internal output filter, external $C_{OUT\_EXT\_TRANS}$ and external LC filter a low-noise solution is achieved.

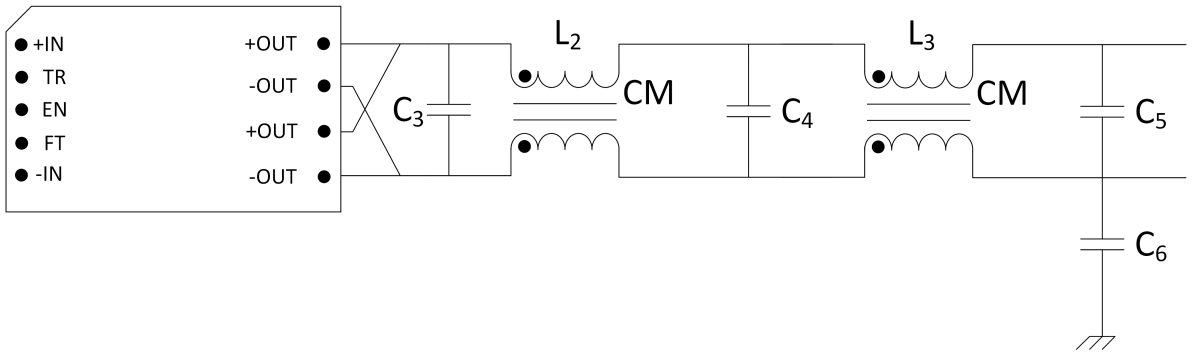


Figure 7.19: Output Filtering Circuit for the DC-DC Power Converter Circuit

Tantalum capacitors have low equivalent series resistance (ESR) and they are very stable over broad temperature range. The VICOR DCM requires a minimum external output capacitor ($C_{OUT\_EXT\_TRANS}$) in the range of 200 μF and 2000 μF with ESR of 10 mΩ. This external capacitor is required for DCM control loop compensation purposes. A 1000 μf tantalum capacitor is used at the output of the VICOR DCM, capacitor C_3 in figure 7.19

Ceramic capacitors with class II (X7S) dielectric materials are used in the output filtering circuit. The Class-II ceramic capacitors exhibit a small change in capacitance over a wide range of temperature. The expected change is $\pm 15\%$ from $-55\,^{\circ}$C to $125\,^{\circ}$C.

7.3.3 Radiated Electromagnetic Interference (EMI) Noise Rejection

Radiated EMI noise is a non-trivial issue for the ARIANNA experiment. VICOR DCM uses ZVS/ZCS switching technology and has a narrow spectrum of switching noise. The radiated EMI usually happens at higher frequencies (30 MHz) and can be easily picked up by the LPDAs of the ARIANNA station jeopardizing the experiment. The ARIANNA experiment is significantly impacted by the EMI radiated noise in the 50 MHz to 500 MHz region. Figure 7.20 shows the completed DC-DC converter board with input and output filtering.

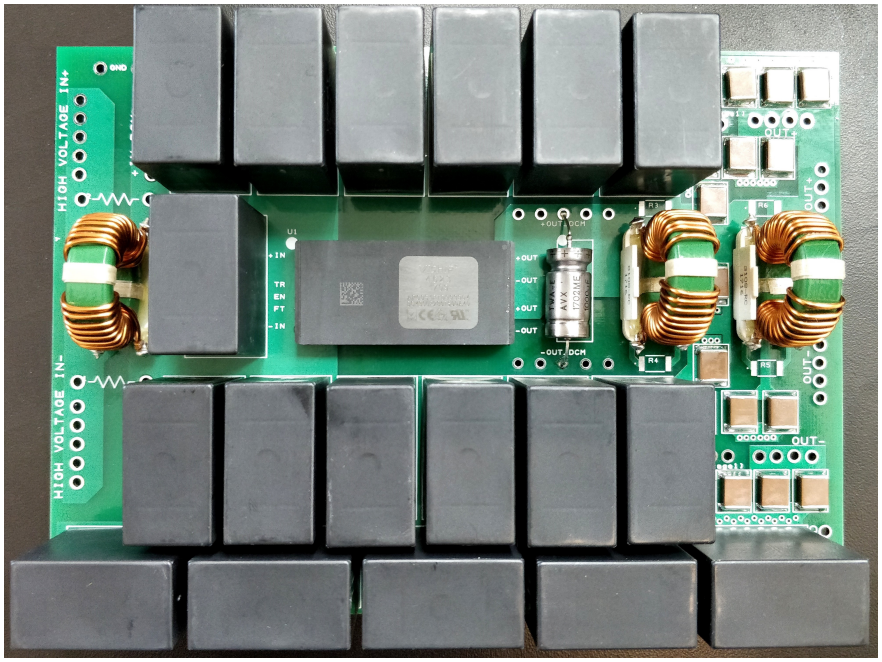


Figure 7.20: DC-DC Power Converter Board

The whole system is placed inside a RFI/EMI shielded enclosure to limit the radiated EMI noise. The radiated EMI noise is further reduced by adding ferrite beads to the power cables and adding EMI feedthrough filters to the panel mount power connectors.

Choosing ferrite beads with a right mix is very important. The ferrite mix has to be selected based on the frequency range of the application. In general there are two basic groups of

ferrite mixes, those with permeability range from 20 to 850 μ are of the Nickel Zinc (NiZn) and those with permeability more than 850μ which are usually Manganese Zinc (MnZn). For most RFI/EMI common monde suppression, NiZn ferrite cores are usually used. The NiZn ferrite cores (mix 43, 52, 61) have low permeability, and moderate temperature stability. The NiZn ferrites have a higher resistivity and are used in frequencies from 2 MHz to several hundred megahertz. The DC-DC power converter circuit uses KEMET (ESD-R-10D) NiZn Ferrite toroids.

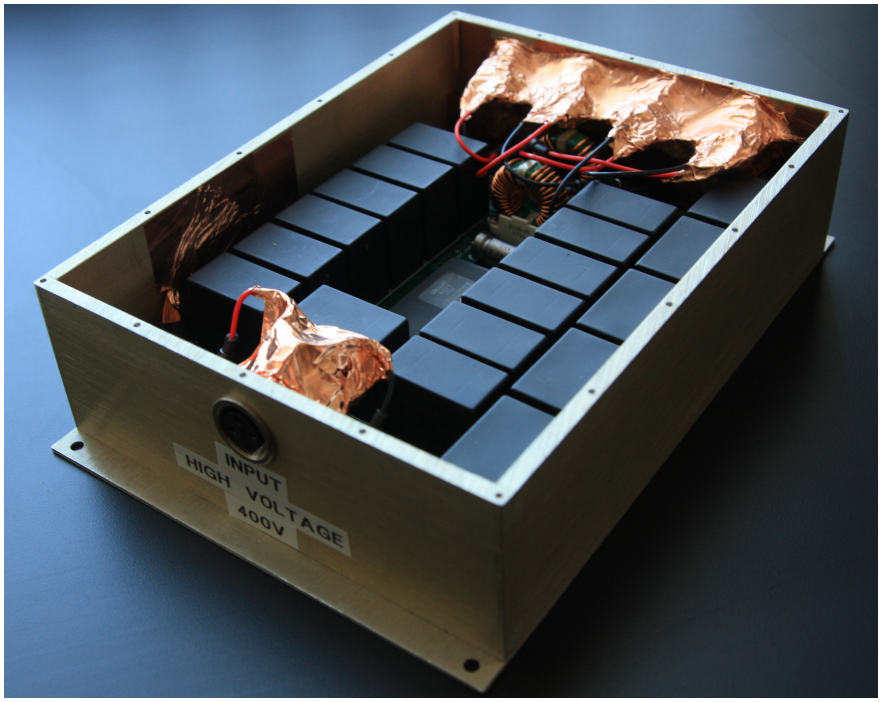


Figure 7.21: DC-DC Power Converter Box

A 500V 0.01μF feedthrough capacitor is used on the input side of the RFI/EMI enclosure. On the output side of the enclosure, a 50V 0.3μF capacitor filter is mounted on the connector. These feedthrough capacitors further reduce the EMI noise. A copper tape is used to shield the whole feedthrough capacitor setup. Figure 7.21 shows the total setup with shielding.

Chapter 8

8 channel Data Acquisition System Test Results

The 2017 8 channel DAQ board is built and populated. An extension of our previous 4 channel DAQ board, the new system has few new features. The test results of these new features are described in the following sections.

First, the board must be set up for normal operation. There are number of hardware configurations which must be performed before testing the board, these hardware configurations include, tuning the bias voltages, programming the FPGA and MBED μcontroller. The correct bias voltages can be set up by tuning the potentiometes on the board. The tuning of these bias voltages are critical for the correct operation of the SST chip, and the default bias voltages that must be set up is shown in table 8.1.

Most of the SST test results presented in chapter 3 is the same for the 2017 DAQ board. The sampling and readout performance is presented in section 3.3.1, the bandwidth measurement is presented in section 3.3.2. The trigger sensitivity and system stability is presented in sections 3.3.6 and 3.3.7. The 8 channel 2017 DAQ boards samples at 1 Gsamples/s and are

Table 8.1: Default Configuration of Bias Voltages for the SST Chip

Bias circuit	Potentiomenter	Default bias voltage
Bias-Tee Bias Voltage	R19	0.9V
LVDS Bias Voltage	R13, R29	0.71V
Source Follower Bias Voltage	R12, R28	1.72V
Comparator Bias Voltage	R9, R23	1.47V
Trigger circuit - L1 Timing bias	R11, R25	1.57V
Trigger circuit - L2 Timing bias	R10, R24	0V

used for detection of cosmic air showers. Since the sampling speed is half of the previous generation SST, the STOP delay must be increased for this generation SST DAQ board.

8.1 STOP Delay Testing

The testing and verification of the delay applied to the STOP signal is important. The figure 8.1 shows the delay between the trigger out signal and STOP signal generated after 187 ns of delay. This delay is measured with forced triggers applied by the MBED

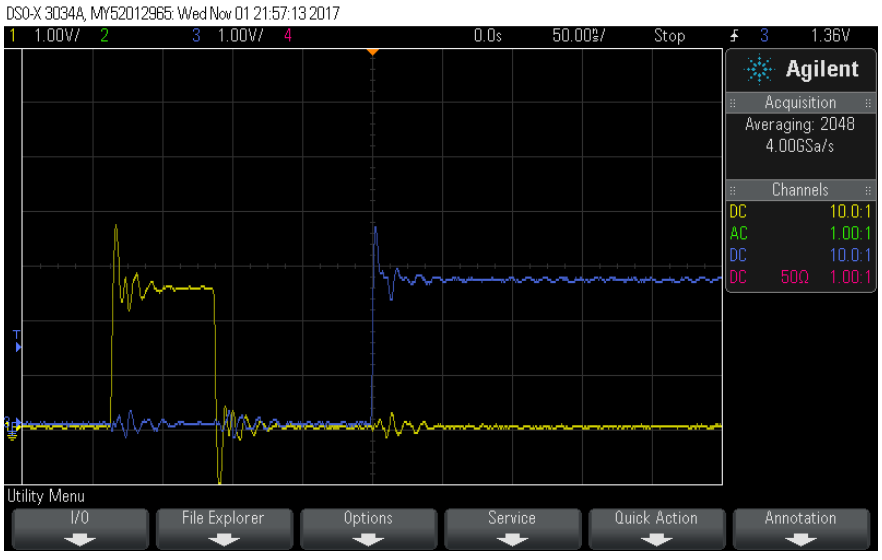


Figure 8.1: STOP Delay Testing

Channel 1 (yellow) of the scope is the external trigger applied to the FPGA, for all intense

and purposes this trigger can be considered as trigger from the SST chip, the firmware delays this signal by 187 ns and the channel 3 (blue) of the scope shows the delayed STOP signal.

8.2 Relative Stop Positions Between Two SST Chips

The 2017 DAQ board, consist of two SST chips running on one single oscillator. The oscillator is placed closed to the first SST chip and there is additional 2.021 inches of track length for clock to reach second SST chip. The track lengths of the control signals from the FPAG to the two SSTs are not equal. These inequalities in the track path lengths will contribute to signal skew. These skewed STOP signals will caused the two SST chips to reset at different times and the relative position of the STOP bits will vary between the two SST chips.

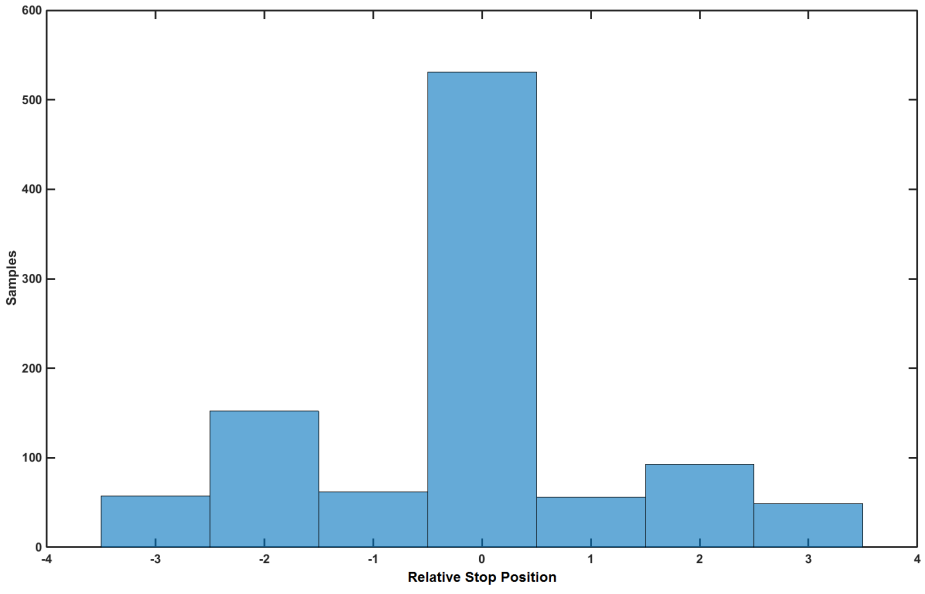


Figure 8.2: Histogram of Relative Stop Positions

The 2017 DAQ board set up for forced triggering and the STOP data for 1000 samples are collected. The STOP positions for both the chips are compared and the relative STOP positions between two chips are plotted on the waveform. The figure 8.2 shows the histogram

of the relative STOP position between the two chips for 1000 samples.

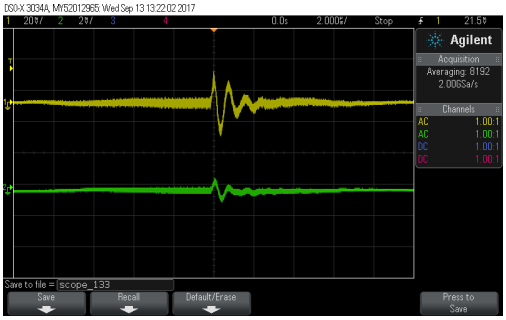
The histogram plot shown in figure 8.2 shows the relative positions of STOP data. The histogram essentially proves that the two chips do not start and stop at the same time, the maximum deviation is ±3 samples. For sampling speed of 1 GSamples/s, the max deviation between two chips is ∼3 ns. This relative STOP positon deviation is potentially caused by two factors, first, the unequal signal tracks from the oscillator to both SST chips. For e.g., SST chip 1 will receive the clock at $t = x$ and the SST chip 2 will receive the oscillator clock at $t = x + \Delta x$, Δx is the time taken by the clock to traverse the distance of 2.021 inches. Secondly, two independent tracks are used to control the SST chips. The track lengths of two control lines from the FPGA and the internal FPGA routing will add additional skew to the control signals. This skew will also contribute to deviation of the relative STOP position. Form the plot, we can see that $\sim 50\%$ of the time the two chips are synchronous with each other.

Although, this deviation appears to be bad, but in reality this will not affect the physicists of the ARIANNA experiment. During post processing, the relative deviation of the STOP positons can be readout and the analog data can be shifter by this deviation.

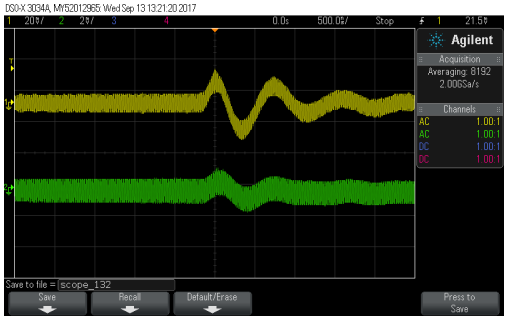
8.3 DC-DC Power Converter EMI Input/Output Noise

The ARIANNA experiment is very sensitive to external noise within 50 MHz and 1 GHz. Any radiated noise in this spectrum will essentially flood the system with unwanted noise and kill the experiment. The radiated electromagnetic interference noise is a non-trivial issue for the ARIANNA experiment and extra care should be taken to shield all the noise sources. The high voltage DC-DC converter is notorious to produce high voltage switching noise. Section 7.3.3 discusses all the efforts taken to shield the high voltage DC-DC converter. A

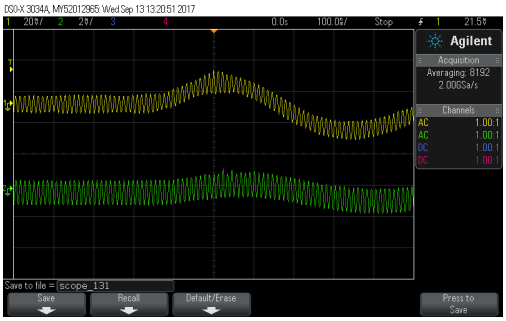
combination of ferrite beads, feed-through capacitors and RF/EMI shielded enclosure was used to suppress EMI noise from the DC-DC converter (VICOR DCM) chip.



(a) EMI Noise $20\mu s$



(b) EMI Noise $5\mu s$



(c) EMI Noise $1\mu s$

Figure 8.3: EMI Noise

Figure 8.3 shows the scope measurement of noise at the power inputs and outputs of the shielded DC-DC power converter. In the scope photos, channel 2 (yellow) is the noise at the output connector of the DC-DC power converter box and channel 1 (green) is the noise at the input connector of the DC-DC power converter box.

On the input connector, 2 mV of noise was measured and on the output connector ~40 mV of noise was measured. It is important to understand that, this noise is not the radiated noise but rather the noise on the power lines. RF shielded cables are used to transmit the power from the DC-DC power converter box to the ARIANNA station, therefore, radiated noise will be much less than the noise on the power lines.

Two frequency components of noise can be seen in the figure 8.3. The low frequency compo-

nent (1.3 MHz) and high frequency component (88.9 MHz). The low frequency component is of no concern to us, the high pass filters will attenuate this frequency component. The high frequency component is attributed to KUCI (UC Irvines) college radio station. This high frequency noise can be ignored.

8.4 DC-DC Power Converter Temperature Test at $-60\,^{\circ}\mathrm{C}$

Cold temperature test was performed on the DC-DC converter box. A data acquisition board was connected to the DC-DC power converter box and the whole system was placed in the fridge for 13 hours. The data acquisition board successfully measured the output voltage of the DC-DC power converter box every 123 seconds. The plot of voltage vs time can be seen in figure 8.4.

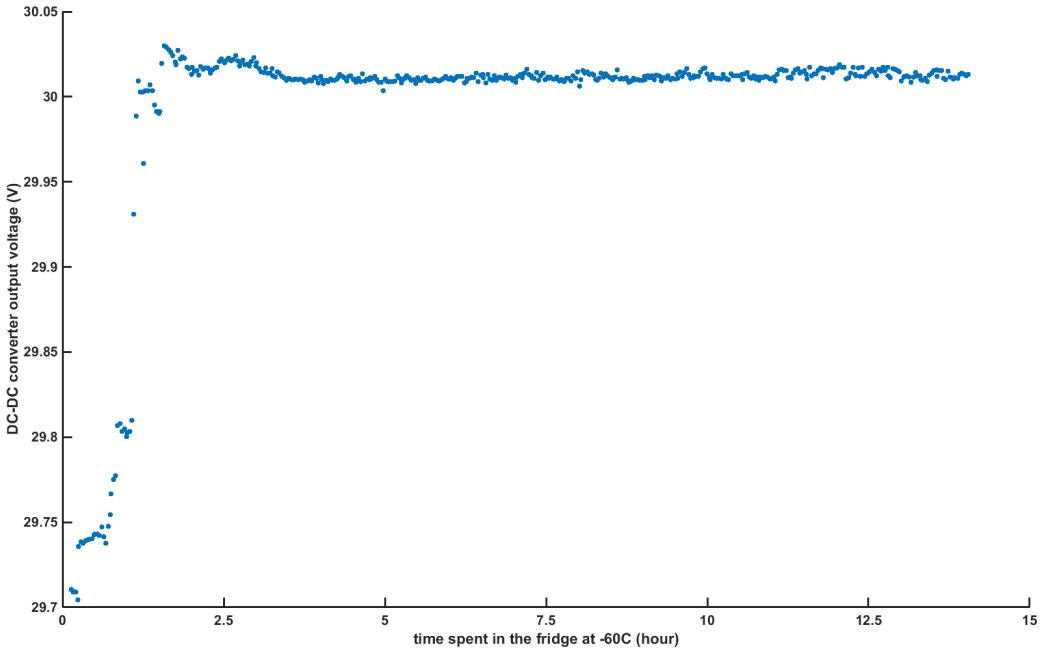


Figure 8.4: DC-DC Power Converter Cold Temperature Test $-60\,^{\circ}\mathrm{C}$

Chapter 9

Conclusion

In this dissertation, we have presented the conception of a synchronous analog waveform recording and triggering circuit for the ARIANNA Ultra-High-Energy Neutrino Detector. A fully synchronous 2 GHz analog transient waveform recording and triggering circuit (SST) containing 4 channels of 256 cells per channel with fast, flexible, real-time and on-chip trigger circuitry with ps-level timing accuracy was described.

The SST was designed and fabricated in TSMC $0.25/mum$ technology and measures $2.5mm \times 2.5mm$. The SST contains a circular array of 256 sample and hold circuits for continuous sample and storage. The SST attains 2 GHz of sampling speed with 1.5 GHz of -3 dB analog bandwidth. The SST has a 1.9V input range on a 2.5V supply. The chip exceeds 12 bits of dynamic range and uses $\sim$160 mW of power while operating at 2 Gsamples/s and full trigger rate. The SSTs internal sample clocks are generated synchronously via high-speed dynamic shift registers driven by an external LVDS oscillator running at half the sample rate (e.g., a 1 GHz oscillator yields 2 G-samples/s). The SST has ps-level timing uniformity that is independent of sample frequencies spanning over 6 orders of magnitude ($2kHz < f_{sampling} < 2GHz$). Each channel of SST includes a dual-threshold triggering circuitry with

windowed coincidence logic. SST can discriminate signals with ∼1 mV RMS resolution with at least 600 MHz bandwidth. The input referred noise for the SST is measured to by 0.42 mV (RMS). The SST demonstrated a 30.39 ps (RMS) fixed pattern sampling time non-uniformity. With timing calibrations, the SST achieves inter channel timing resolutions between 1.12 ps (RMS) and 2.37 ps (RMS).

A new 8 channel data acquisition (DAQ) board was designed and fabricated for the ARIANNA experiment. The DAQ board features two SST chips with onboard temperature measurements, accurate voltage and power monitoring with optimized firmware and software all the while maintaining compatibility with the previous generation system.

Several neutrino stations equipped with SST chips were deployed in the Antarctica's Ross Ice Shelf. The neutrino stations are actively monitoring for short radio Cherenkov pulses since 2014-15 austral summer. One eight channel station is set to be deployed at the South Pole in the 2017-18 austral summer.

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Appendix A

Test board layout

A.1 Test board - SST - 0.25 TSMC layout

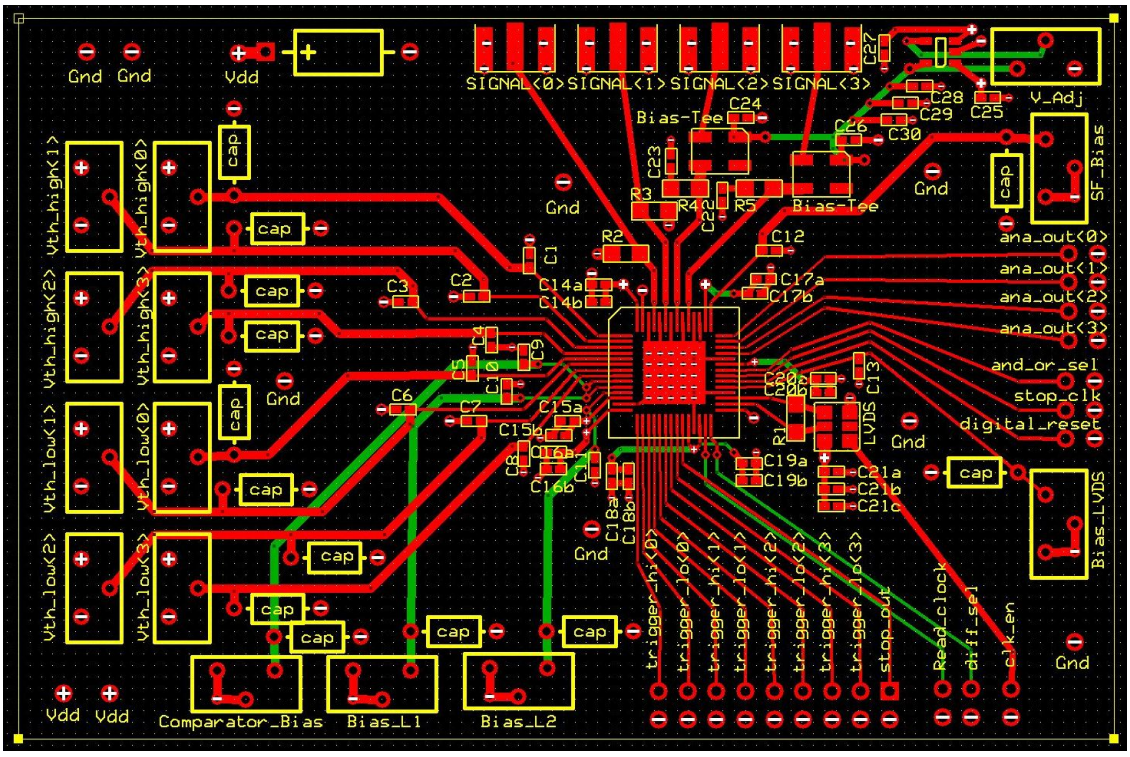

Figure A.1: Test board - top layer

A.2 Test board - SST - 0.18 IBM layout

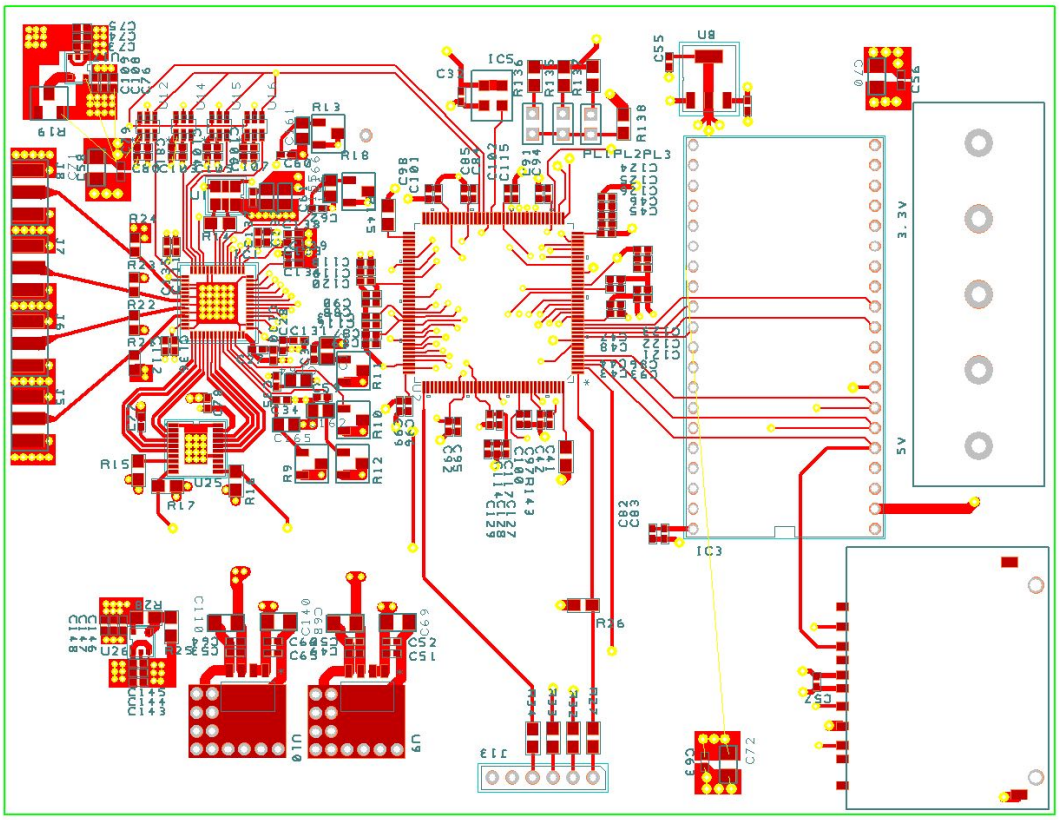

Figure A.2: Test board - top layer

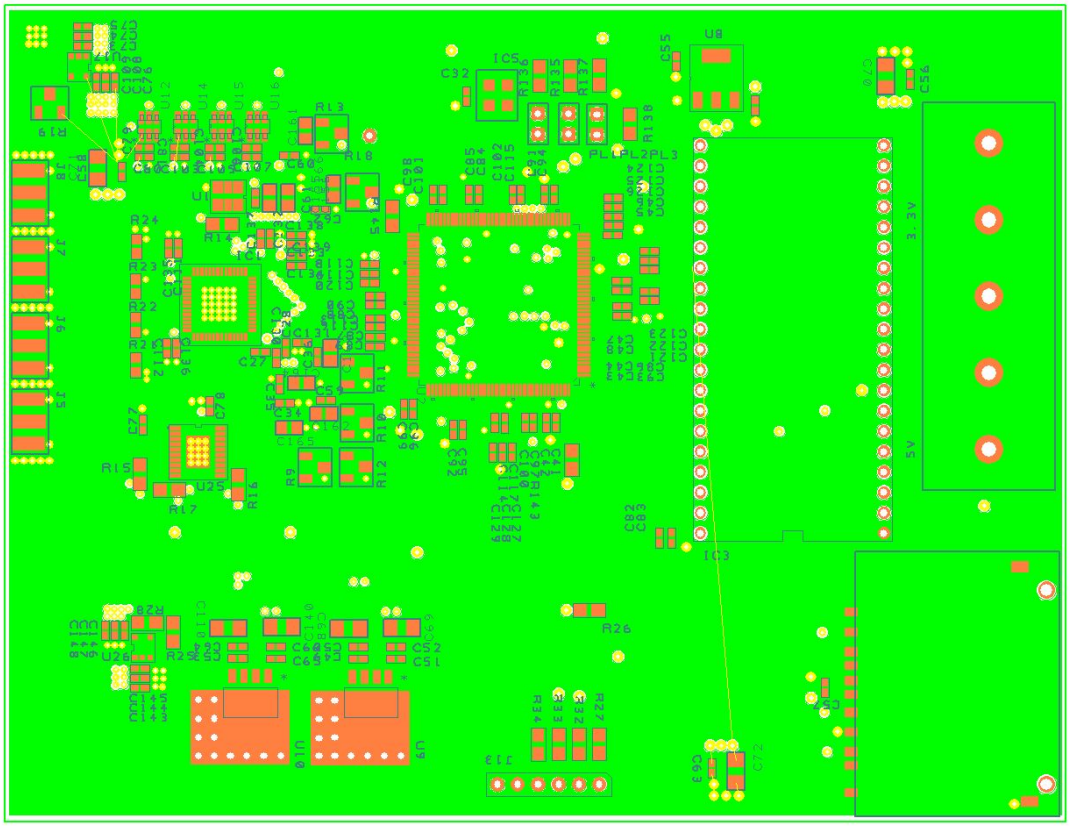

Figure A.3: Test board - ground layer

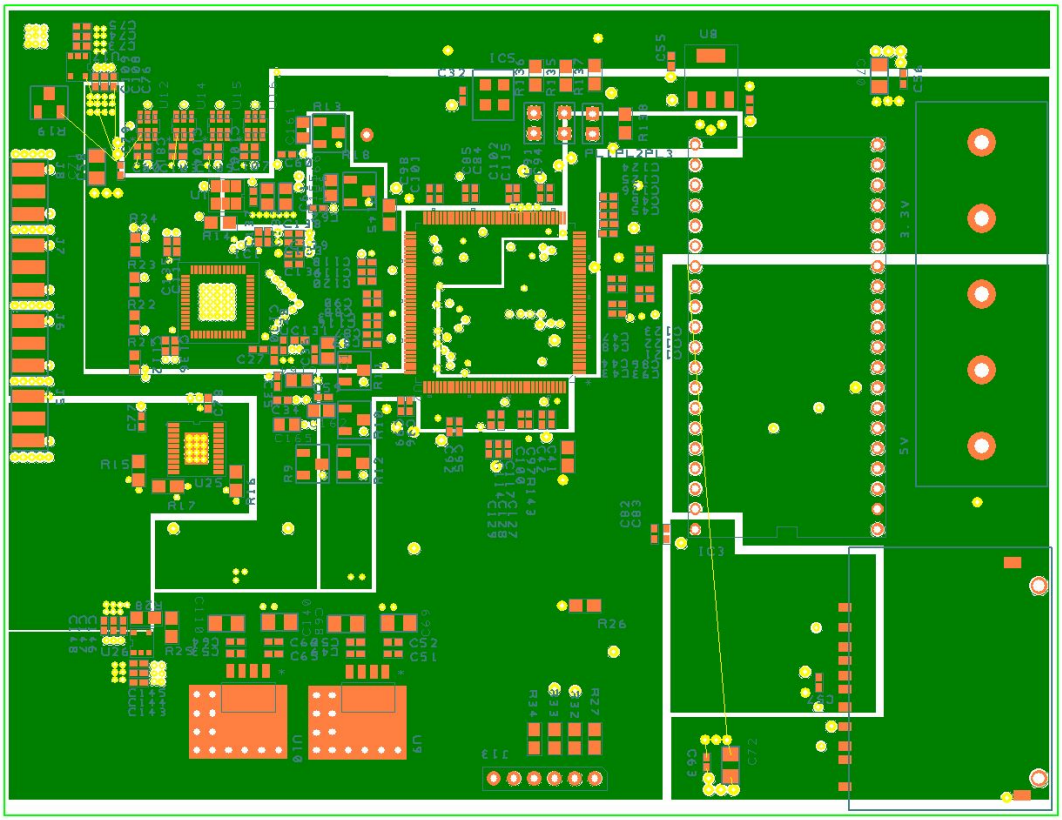

Figure A.4: Test board - power layer

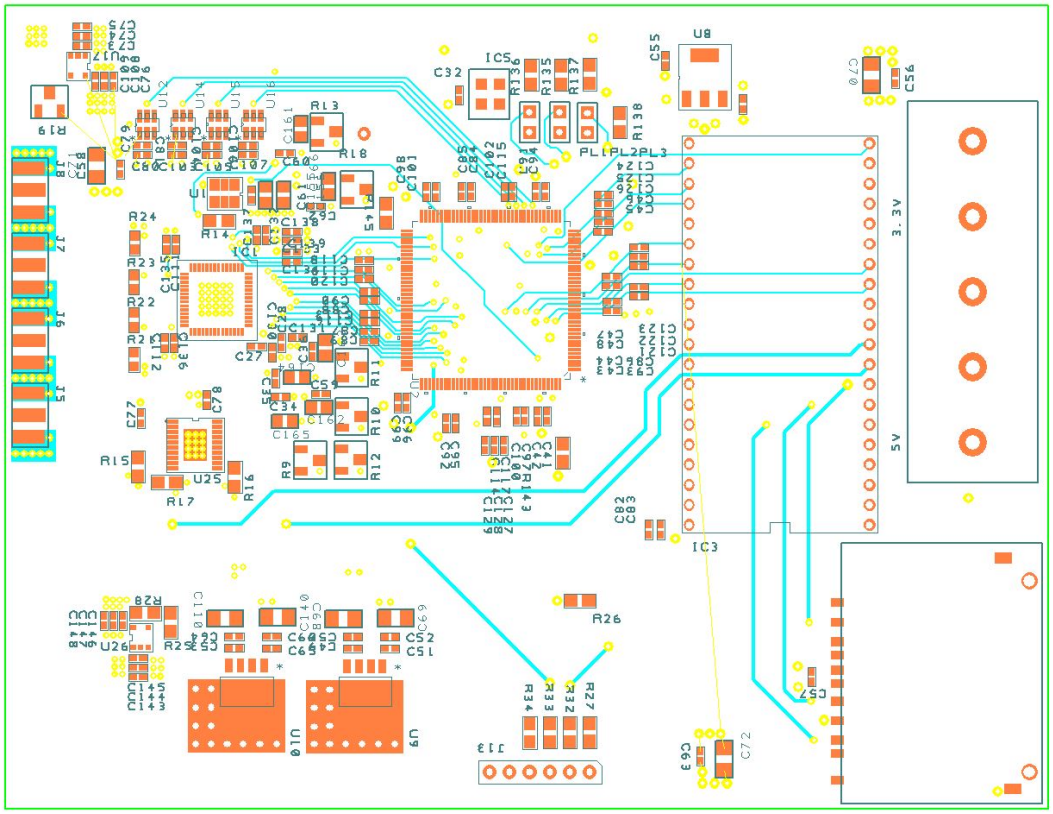

Figure A.5: Test board - bottom layer

A.3 2017 8-ch ARIANNA Board

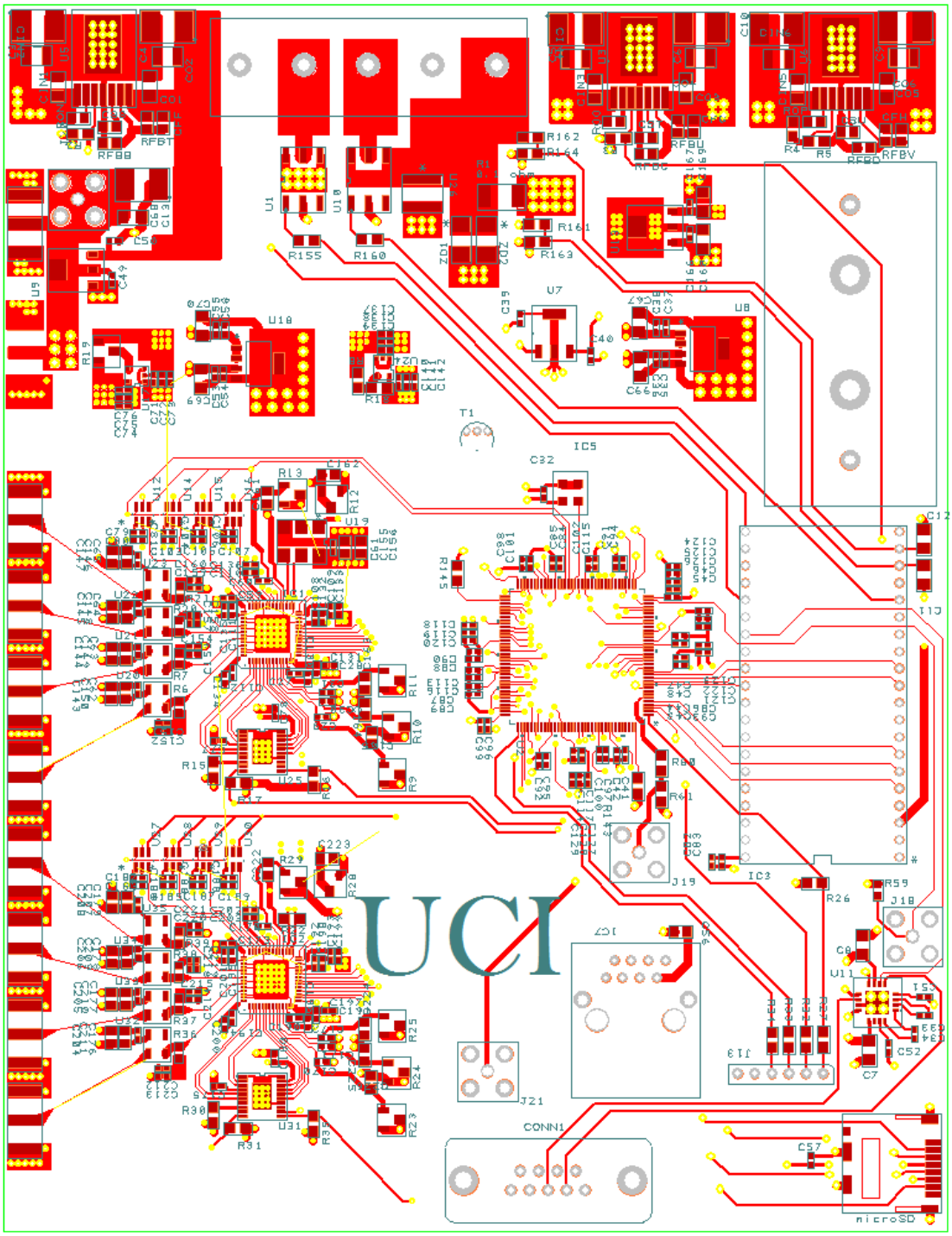

Figure A.6: 2017 8-ch ARIANNA Board - Top layer

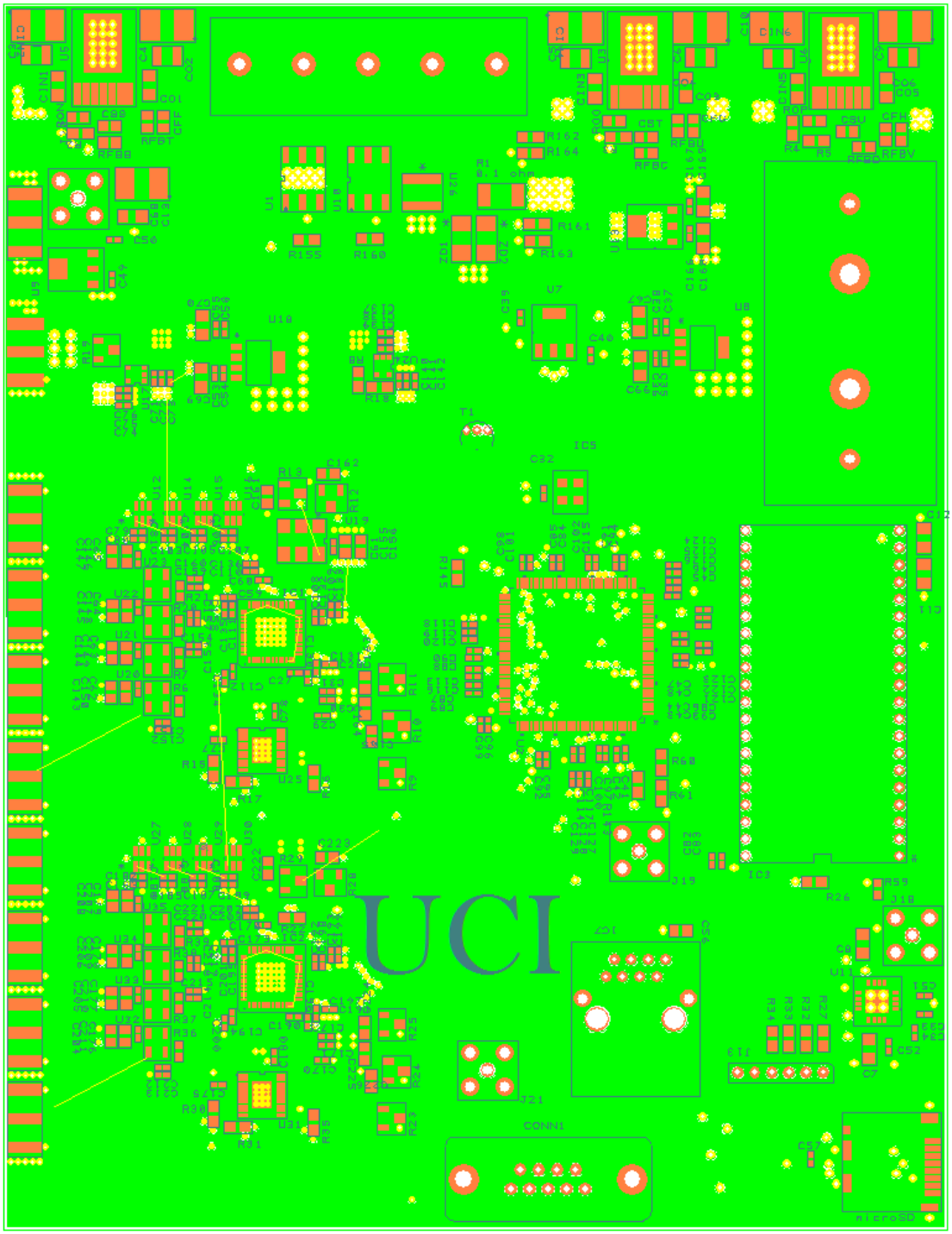

Figure A.7: 2017 8-ch ARIANNA Board - Ground layer

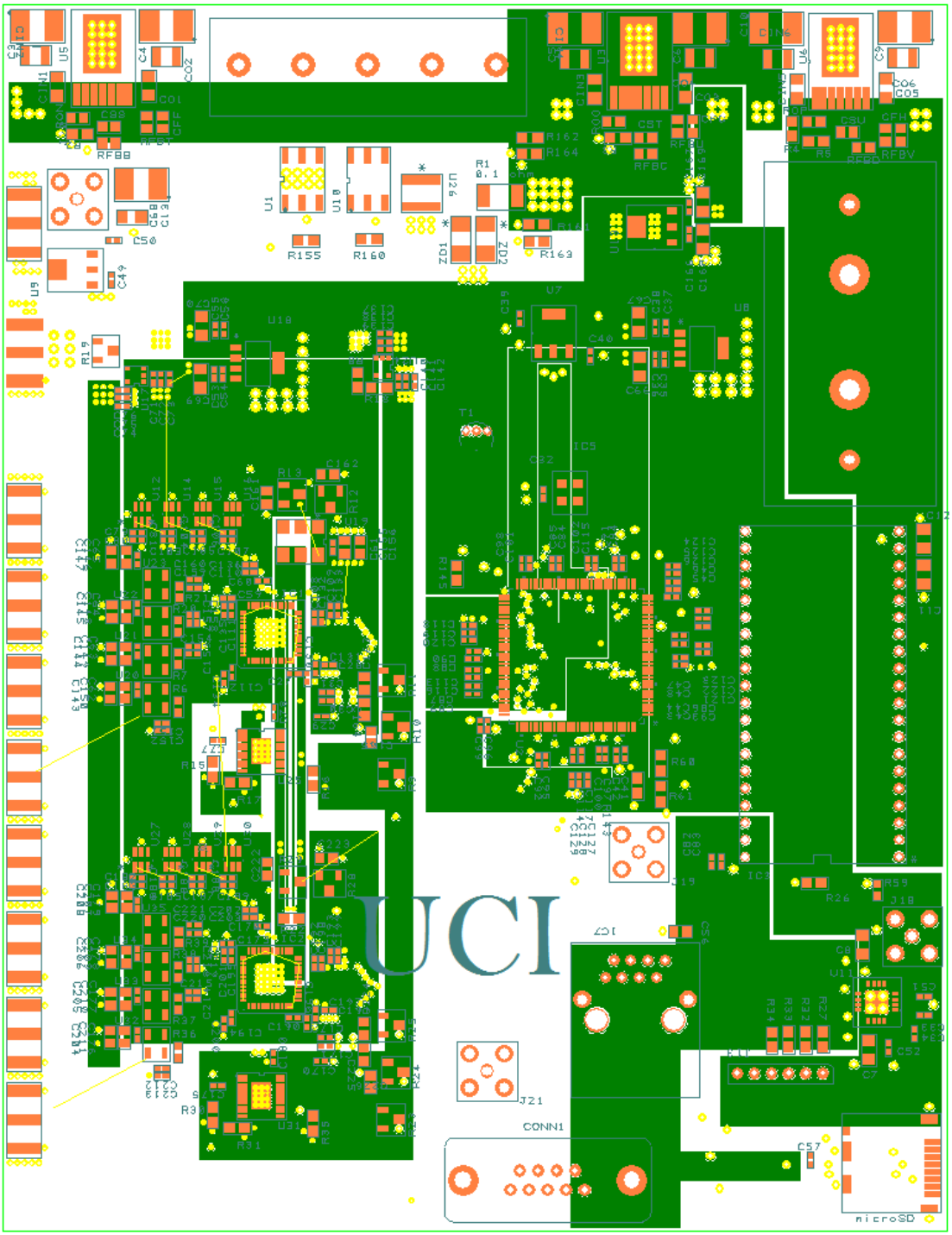

Figure A.8: 2017 8-ch ARIANNA Board - Power layer

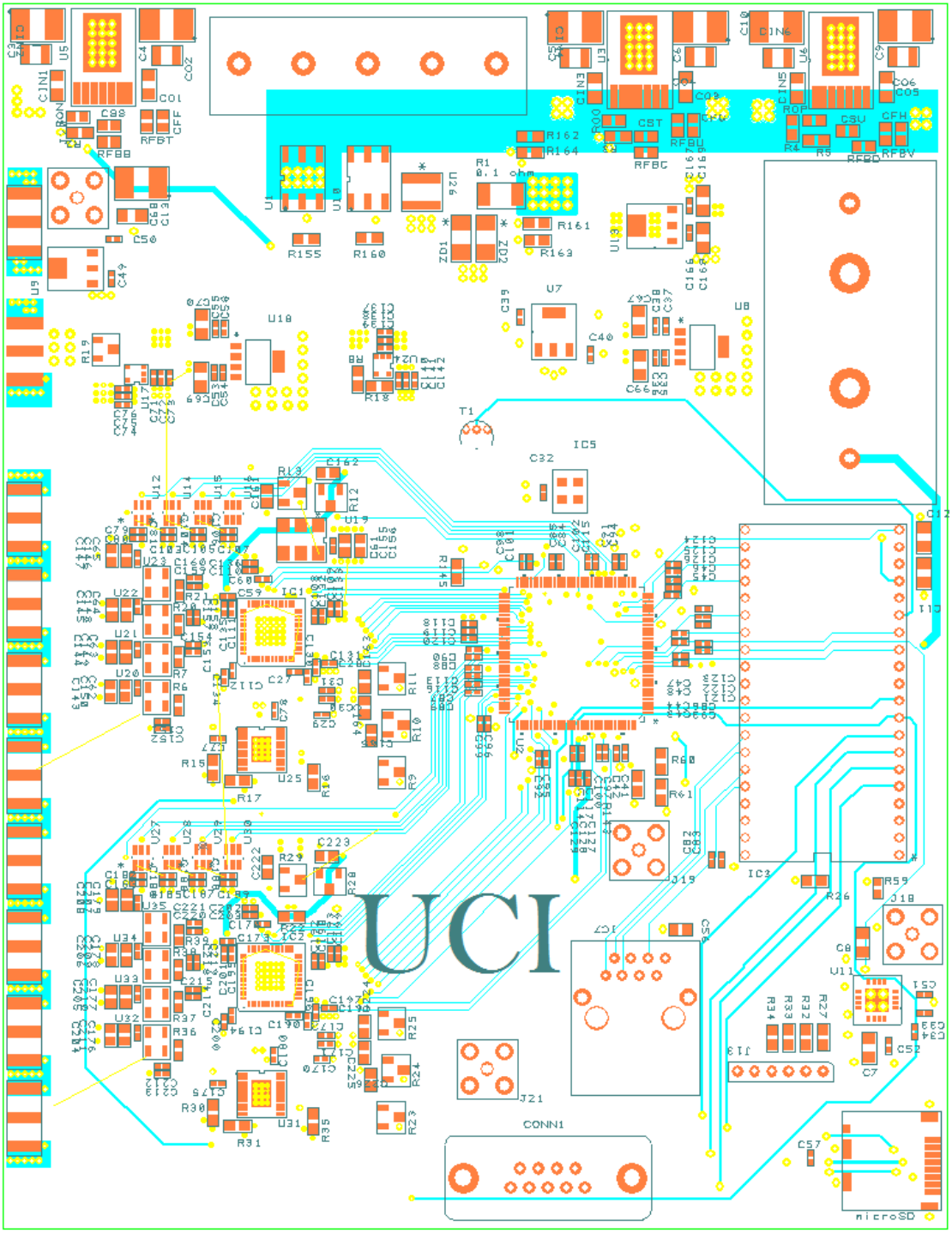

Figure A.9: 2017 8-ch ARIANNA Board - Bottom layer

A.4 2017-South Pole High Voltage DC-DC converter Board

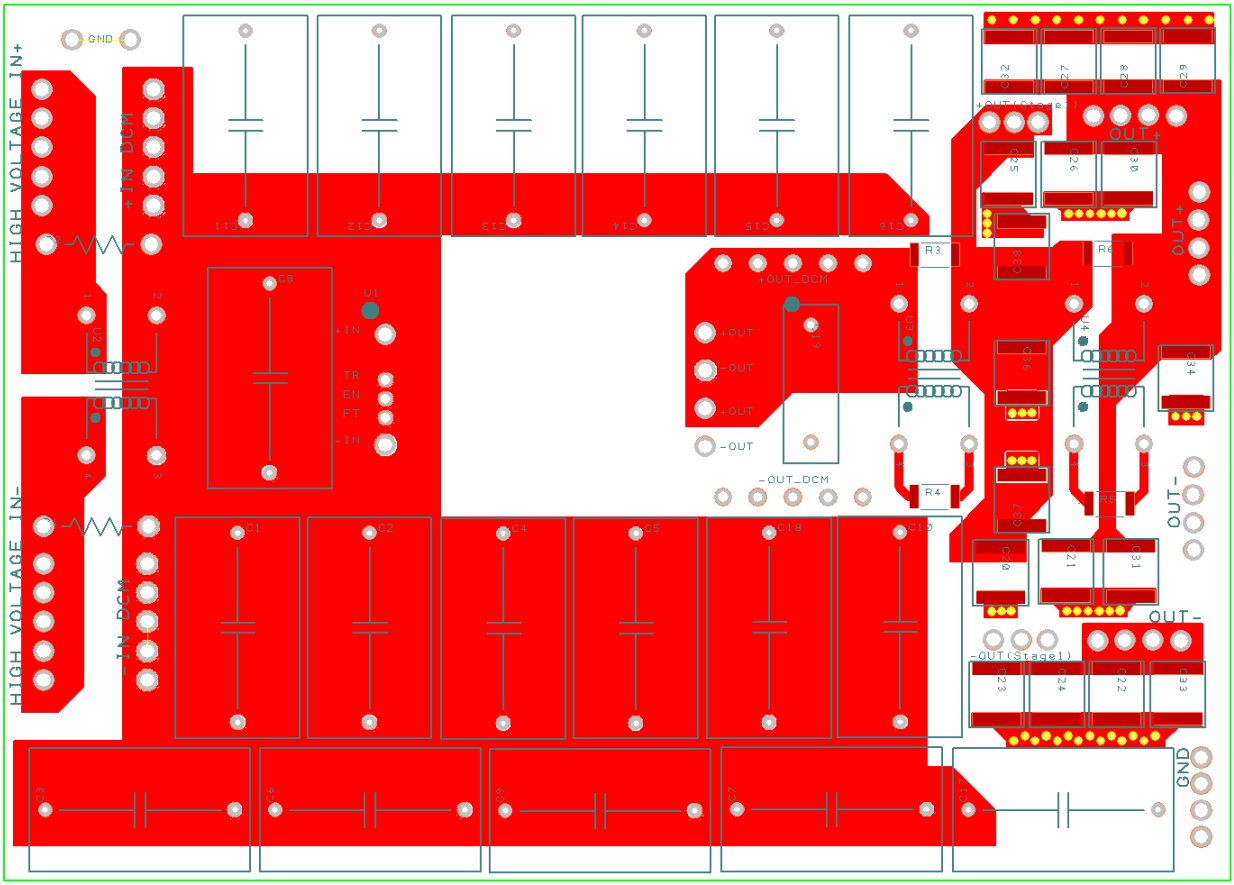

Figure A.10: 2017-South Pole High Voltage DC-DC converter - Top layer

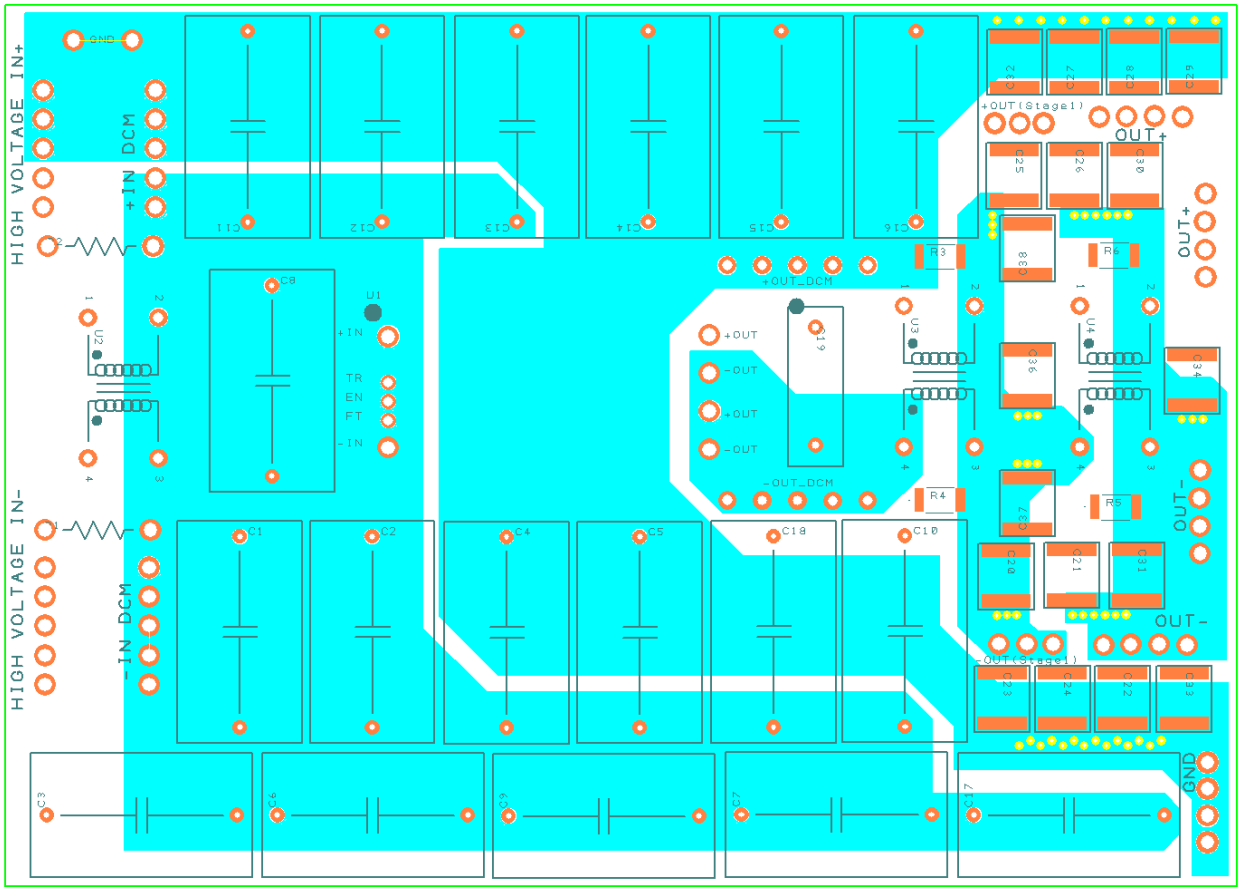

Figure A.11: 2017-South Pole High Voltage DC-DC converter - Bottom layer

Appendix B

Firmware Source Code

B.1 Trigger Encoder

This block of the code, encodes all 16 trigger outputs of the two SST chips into 8 trigger signals. Encoding is done based on the MBED control signals - "and-or-sel" and "diff-sel".

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity trigger_encoder is
    Port ( trigger_0L : in  STD_LOGIC;
           trigger_0H : in  STD_LOGIC;
           trigger_1L : in  STD_LOGIC;
           trigger_1H : in  STD_LOGIC;
           trigger_2L : in  STD_LOGIC;
           trigger_2H : in  STD_LOGIC;
           trigger_3L : in  STD_LOGIC;
           trigger_3H : in  STD_LOGIC;
```

```
            trigger_4L : in  STD_LOGIC;
            trigger_4H : in  STD_LOGIC;
            trigger_5L : in  STD_LOGIC;
            trigger_5H : in  STD_LOGIC;
            trigger_6L : in  STD_LOGIC;
            trigger_6H : in  STD_LOGIC;
            trigger_7L : in  STD_LOGIC;
            trigger_7H : in  STD_LOGIC;
            and_or_sel : in  STD_LOGIC;
            diff_sel   : in  STD_LOGIC;
            ch_0 : out STD_LOGIC;
        ch_1 : out STD_LOGIC;
        ch_2 : out STD_LOGIC;
        ch_3 : out STD_LOGIC;
        ch_4 : out STD_LOGIC;
        ch_5 : out STD_LOGIC;
        ch_6 : out STD_LOGIC;
        ch_7 : out STD_LOGIC);
end trigger_encoder;
architecture Behavioral of trigger_encoder is
begin
ch_0 <= trigger_0L when diff_sel = '1' else
      (trigger_0L and trigger_0H) when and_or_sel = '1' else
      (trigger_0L or trigger_0H) when and_or_sel = '0' else
      '0';
ch_1 <= trigger_1L when diff_sel = '1' else
      (trigger_1L and trigger_1H) when and_or_sel = '1' else
```

```
      (trigger_1L or trigger_1H) when and_or_sel = '0' else
      '0';
ch_2 <= trigger_2L when diff_sel = '1' else
      (trigger_2L and trigger_2H) when and_or_sel = '1' else
      (trigger_2L or trigger_2H) when and_or_sel = '0' else
      '0';
ch_3 <= trigger_3L when diff_sel = '1' else
      (trigger_3L and trigger_3H) when and_or_sel = '1' else
      (trigger_3L or trigger_3H) when and_or_sel = '0' else
      '0';
ch_4 <= trigger_4L when diff_sel = '1' else
      (trigger_4L and trigger_4H) when and_or_sel = '1' else
      (trigger_4L or trigger_4H) when and_or_sel = '0' else
      '0';
ch_5 <= trigger_5L when diff_sel = '1' else
      (trigger_5L and trigger_5H) when and_or_sel = '1' else
      (trigger_5L or trigger_5H) when and_or_sel = '0' else
      '0';
ch_6 <= trigger_6L when diff_sel = '1' else
      (trigger_6L and trigger_6H) when and_or_sel = '1' else
      (trigger_6L or trigger_6H) when and_or_sel = '0' else
      '0';
ch_7 <= trigger_7L when diff_sel = '1' else
      (trigger_7L and trigger_7H) when and_or_sel = '1' else
      (trigger_7L or trigger_7H) when and_or_sel = '0' else
      '0';
end Behavioral;
```

B.2 Majority 8 Logic

This block of code, continually counts the number of triggers from the SST chips, if the number of triggers exceed the majority logic count, an interrupt signal is asserted to stop the acquisition phase of the SST.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity majority_8_logic is
 Port ( trig_0 : INSTD_LOGIC;
trig_1 : INSTD_LOGIC;
trig_2 : INSTD_LOGIC;
trig_3 : INSTD_LOGIC;
trig_4 : INSTD_LOGIC;
trig_5 : INSTD_LOGIC;
trig_6 : INSTD_LOGIC;
trig_7 : INSTD_LOGIC;
clk : INSTD_LOGIC;
mbed_sel0 : INSTD_LOGIC;
mbed_sel1 : INSTD_LOGIC;
enable_thermal_tri : INSTD_LOGIC;
ext_tri : INSTD_LOGIC;
force_tri : INSTD_LOGIC;
internal_trigger : OUT STD_LOGIC);
end majority_8_logic;
architecture Behavioral of majority_8_logic is
 COMPONENT trigger_counter
 PORT( trig_0 :INSTD_LOGIC;
```

```
  trig_1 :INSTD_LOGIC;
  trig_2 :INSTD_LOGIC;
  trig_3 :INSTD_LOGIC;
  trig_4 :INSTD_LOGIC;
  trig_5 :INSTD_LOGIC;
  trig_6 :INSTD_LOGIC;
  trig_7 :INSTD_LOGIC;
  trig_count: OUTSTD_LOGIC_VECTOR(3 downto 0));
 END COMPONENT;
COMPONENT demux
PORT( clk : IN STD_LOGIC;
  sel0 : IN STD_LOGIC;
  sel1 : IN STD_LOGIC;
  cout0 : OUTSTD_LOGIC;
  cout1 : OUTSTD_LOGIC;
  cout2 : OUTSTD_LOGIC;
  cout3 : OUTSTD_LOGIC);
end COMPONENT;
SIGNAL trig_count_sig : STD_LOGIC_VECTOR(3 DOWNTO 0);
SIGNAL demux_0, demux_1, demux_2, demux_3 : STD_LOGIC;
SIGNAL majority1, majority2, majority4, majority3 : STD_LOGIC;
begin
 UU1: trigger_counter PORT MAP(
  trig_0 => trig_0,
  trig_1 => trig_1,
  trig_2 => trig_2,
  trig_3 => trig_3,
```

```
  trig_4 => trig_4,
  trig_5 => trig_5,
  trig_6 => trig_6,
  trig_7 => trig_7,
  trig_count => trig_count_sig
  );
UU2: demuxPORT MAP(
  clk=> clk,
  sel0 => mbed_sel0,
  sel1 => mbed_sel1,
  cout0 => demux_0,
  cout1 => demux_1,
  cout2 => demux_2,
  cout3 => demux_3
  );
--To change majority logic, uncomment the corresponding majority
--logic equation and define the signal and update the signal in
--the internal_trigger equation. Also assign the correct demux_x
--value to the corresponding majority logic.
 majority1 <= (((not(trig_count_sig(3)) and not(trig_count_sig(2)) and
  not(trig_count_sig(1)) and (trig_count_sig(0))) or --0001
  (not(trig_count_sig(3)) and not(trig_count_sig(2)) and
  (trig_count_sig(1)) and not(trig_count_sig(0))) or --0010
  (not(trig_count_sig(3)) and not(trig_count_sig(2)) and
  (trig_count_sig(1)) and (trig_count_sig(0))) or --0011
  (not(trig_count_sig(3)) and (trig_count_sig(2)) and
  not(trig_count_sig(1)) and not(trig_count_sig(0))) or --0100
```

```
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 not(trig_count_sig(1)) and (trig_count_sig(0))) or --0101
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 (trig_count_sig(1)) and not(trig_count_sig(0))) or --0110
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 (trig_count_sig(1)) and (trig_count_sig(0))) or --0111
 ((trig_count_sig(3)) and not(trig_count_sig(2)) and
 not(trig_count_sig(1)) and not(trig_count_sig(0))))
 and demux_0 and enable_thermal_tri); --1000

majority2 <= (((not(trig_count_sig(3)) and not(trig_count_sig(2)) and
 (trig_count_sig(1)) and not(trig_count_sig(0))) or --0010
 (not(trig_count_sig(3)) and not(trig_count_sig(2)) and
 (trig_count_sig(1)) and (trig_count_sig(0))) or --0011
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 not(trig_count_sig(1)) and not(trig_count_sig(0))) or --0100
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 not(trig_count_sig(1)) and (trig_count_sig(0))) or --0101
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 (trig_count_sig(1)) and not(trig_count_sig(0))) or --0110
 (not(trig_count_sig(3)) and (trig_count_sig(2)) and
 (trig_count_sig(1)) and (trig_count_sig(0))) or --0111
 ((trig_count_sig(3)) and not(trig_count_sig(2)) and
 not(trig_count_sig(1)) and not(trig_count_sig(0)))) and
 demux_1 and enable_thermal_tri); --1000

majority3 <= (((not(trig_count_sig(3)) and not(trig_count_sig(2)) and
```

```
(trig_count_sig(1)) and (trig_count_sig(0))) or --0011
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
not(trig_count_sig(1)) and not(trig_count_sig(0))) or --0100
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
not(trig_count_sig(1)) and (trig_count_sig(0))) or --0101
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
(trig_count_sig(1)) and not(trig_count_sig(0))) or --0110
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
(trig_count_sig(1)) and (trig_count_sig(0))) or --0111
((trig_count_sig(3)) and not(trig_count_sig(2)) and
not(trig_count_sig(1)) and not(trig_count_sig(0)))) and
demux_2 and enable_thermal_tri);--1000

majority4 <= (((not(trig_count_sig(3)) and (trig_count_sig(2)) and
not(trig_count_sig(1)) and not(trig_count_sig(0))) or --0100
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
not(trig_count_sig(1)) and (trig_count_sig(0))) or --0101
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
(trig_count_sig(1)) and not(trig_count_sig(0))) or --0110
(not(trig_count_sig(3)) and (trig_count_sig(2)) and
(trig_count_sig(1)) and (trig_count_sig(0))) or --0111
((trig_count_sig(3)) and not(trig_count_sig(2)) and
not(trig_count_sig(1)) and not(trig_count_sig(0)))) and
demux_3 and enable_thermal_tri); --1000

internal_trigger <= majority1 or majority2 or majority4 or
                    majority3 or ext_tri or force_tri;
```

```
end Behavioral;
```

B.3 Address Controller

The Address controller block, generated the addressing for the block ram of the FPGA. The ADC data is acquired and stored on the Block ram. 12 bits of address are generated for data storage and readout.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_unsigned.all;
entity address_controller is
Port (
        en : in STD_LOGIC;
        rst : in  STD_LOGIC;
        re : in  STD_LOGIC;
        start : inout  STD_LOGIC;
        clk : in STD_LOGIC;
        address : out  STD_LOGIC_VECTOR (11 downto 0);
        full : out  STD_LOGIC;
        done : out  STD_LOGIC;
        wait_sig : out  STD_LOGIC;
        count: out STD_LOGIC_VECTOR(1 downto 0);
        we : out STD_LOGIC);
end address_controller;
architecture Behavioral of address_controller is
```

```
  signal addr : std_logic_vector (11 downto 0) := "000000000000";
   signal r_addr : std_logic_vector (12 downto 0) := "0000000000000";
  signal full_f : std_logic := '0';
  signal done_f : std_logic := '0';
  signal wait_f : std_logic := '0';
  signal count_f  : std_logic_vector(1 downto 0) := "00";
   signal r_count  : std_logic_vector(1 downto 0) := "00";
begin
process(clk, rst) begin
    if rst = '1' then
      addr <= "000000000000";
        r_addr <= "0000000000000";
      full_f <= '0';
      done_f <= '0';
      wait_f <= '0';
      --count_f <="00";
      r_count <= "00";
    else
      if falling_edge(clk) then
        if en = '1' then
          if start = '1' then
            case re is
              when '0' => if addr < "111111111111" then -- 4k
                          addr <= addr + 1;
                        else
                          addr <= "000000000000";
                          full_f <= '1';
```

```
                wait_f <= '1';
              end if;
        when '1' => if r_count < "11" then
              if r_addr < "1000000000000" then -- 4k
                --if r_addr < "0111111111111" then
                r_addr <= r_addr + 1;
              else
                r_addr <= "0000000000000";
                r_count <= r_count +1;
              end if;
            else
              if r_addr < "0111111111111" then
                r_addr <= r_addr + 1;
              else
                r_addr <= "0000000000000";
                r_count <="00";
                done_f <= '1';
                wait_f <= '1';
              end if;
            end if;
        when others => null;
      end case;
    else
      addr <= "000000000000";
      r_addr <= "0000000000000";
      if re = '0' and full_f = '1' then
        wait_f <= '1';
```

```
            elsif re = '1' and done_f = '1' then
              wait_f <= '1';
            else
              wait_f <= '0';
            end if;
          end if;
        else
          wait_f <= '1';
        end if;
      end if;
    end if;
  end process;
    full <= full_f;
    done <= done_f;
    wait_sig <= wait_f;
    start <= not wait_f;
    we <= not re;
    count <= r_count;
    address <= addr when re = '0' else r_addr(11 downto 0);
end Behavioral;
```

B.4 Stop Address Controller

This block is similar to the address controller block, except it is used for STOP data instead of ADC data. 8 bits of address are generated for data storage and readout.

```
library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_unsigned.all;
entity stop_address_controller is
Port (
        en : in STD_LOGIC;
        rst : in  STD_LOGIC;
           re : in  STD_LOGIC;
           start : inout  STD_LOGIC;
        clk : in STD_LOGIC;
        --clk4x:in STD_LOGIC;

           address : out  STD_LOGIC_VECTOR (7 downto 0);
           full : out  STD_LOGIC;
           done : out  STD_LOGIC;
           wait_sig : out  STD_LOGIC;
        count: out STD_LOGIC;
        we : out STD_LOGIC);
end stop_address_controller;
architecture Behavioral of stop_address_controller is
  signal addr : std_logic_vector (7 downto 0) := "00000000";
   signal r_addr : std_logic_vector (8 downto 0) := "000000000";
  signal full_f : std_logic := '0';
  signal done_f : std_logic := '0';
  signal wait_f : std_logic := '0';
  signal count_f  : std_logic := '0';
   signal r_count  : std_logic := '0';
begin
```

```
process(clk, rst) begin
    if rst = '1' then
      addr <= "00000000";
        r_addr <= "000000000";
      full_f <= '0';
      done_f <= '0';
      wait_f <= '0';
      --count_f <="00";
      r_count <= '0';
    else
      if falling_edge(clk) then
        if en = '1' then
          if start = '1' then
            case re is
              when '0' => if addr < "11111111" then -- 4k
                            addr <= addr + 1;
                          else
                            addr <= "00000000";
                            full_f <= '1';
                            wait_f <= '1';
                          end if;
              when '1' => if r_count < '1' then
                            if r_addr < "011111111" then -- 4k
                              r_addr <= r_addr + 1;
                            else
                              r_addr <= "000000000";
                              r_count <= not(r_count);
```

```
            end if;
          else
            if r_addr < "011111111" then -- 4k
              r_addr <= r_addr + 1;
            else
              r_addr <= "000000000";
              r_count <='0';
              done_f <= '1';
              wait_f <= '1';
            end if;
          end if;
        when others => null;
      end case;
    else
      addr <= "00000000";
      r_addr <= "000000000";
      if re = '0' and full_f = '1' then
        wait_f <= '1';
      elsif re = '1' and done_f = '1' then
        wait_f <= '1';
      else
        wait_f <= '0';
      end if;
    end if;
  else
    wait_f <= '1';
  end if;
```

```
      end if;
    end if;
  end process;
    full <= full_f;
    done <= done_f;
    wait_sig <= wait_f;
    start <= not wait_f;
    we <= not re;
    count <= r_count;
    address <= addr when re = '0' else r_addr(7 downto 0);
end Behavioral;
```

B.5 Block Ram

The Block Ram code with read and write capabilities. The block ram is an array of 4095 rows with 4 columns per row. Each block can store one chip's worth of information.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;
use IEEE.NUMERIC_STD.ALL;
library UNISIM;
use UNISIM.VComponents.all;

entity block_ram is
Port (
        clk : in  STD_LOGIC;
```

```
        we : in std_logic;
        en : in std_logic;
        di : in std_logic_vector(3 downto 0);
        do : out  STD_LOGIC_vector(3 downto 0);
        addr : in  STD_LOGIC_VECTOR (11 downto 0));
end block_ram;

architecture Behavioral of block_ram is
type ram_type is array (0 to 4095) of std_logic_vector(3 downto 0);
signal RAM: ram_type;
attribute ram_style: string;
attribute ram_style of RAM : signal is "block";
begin
  --process (clk, en, we)
  process(clk)
  begin
    if rising_edge(clk) then
      if en = '1' then
        do <= RAM(conv_integer(addr));
        if we = '1' then
          RAM(conv_integer(addr)) <= di;
        end if;
      else
        do <= "0000";
      end if;
    end if;
  end process;
```

```
end Behavioral;
```

B.6 Stop Block Ram

The Block Ram code with read and write capabilities. The block ram is an array of 256 rows with 2 columns per row.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;
use IEEE.NUMERIC_STD.ALL;
library UNISIM;
use UNISIM.VComponents.all;
entity stop_block_ram is
Port (
        clk : in  STD_LOGIC;
        we : in std_logic;
        en : in std_logic;
           --di : in  STD_LOGIC_vector(3 downto 0);
        di : in std_logic_vector(1 downto 0);
        do : out  STD_LOGIC_vector(1 downto 0);
           addr : in  STD_LOGIC_VECTOR (7 downto 0));
        --count :in std_logic_vector (1 downto 0));
end stop_block_ram;
architecture Behavioral of stop_block_ram is
type ram_type is array (0 to 255) of std_logic_vector(1 downto 0);
signal RAM: ram_type;
```

```
attribute ram_style: string;
attribute ram_style of RAM : signal is "block";
begin
  --process (clk, en, we)
  process(clk)
  begin
    if rising_edge(clk) then
      if en = '1' then
        do <= RAM(conv_integer(addr));
        if we = '1' then
          RAM(conv_integer(addr)) <= di;
          --RAM(conv_integer(addr)) <= (d3&d2&d1&d0);
        end if;
      else
        do <= "00";
      end if;
    end if;
  end process;
end Behavioral;
```