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Design, Fabrication and Characterization of Highly Linear N-Polar GaN MIS-HEMT for mm-Wave Receiver Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

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ABSTRACT

Design, Fabrication and Characterization of Highly Linear N-Polar GaN MIS-HEMT for mm-Wave Receiver Applications

by

Pawana Shrestha

Gallium Nitride is widely employed for microwave and mm-wave applications. Though GaN HEMTs have primarily been used for power amplification, they are also well suited for receiver applications. In the receiver front-end, the linearity of an RF transistor is an important requisite. In a crowded wireless spectrum with large in-band interferers, non-linearities can mask or distort a weak desired signal. At mm-wave frequencies and high data rates, circuit-level linearization techniques increase system complexity. Therefore, this study focuses on linearization at the device-level.

Traditionally, GaN is grown and fabricated in the Ga-polar orientation. In the N-polar orientation, the inverse polarization fields enable the implementation of device structures that provide excellent mm-wave performance. The devices presented in this work are based on N-polar GaN MIS-HEMT technology and are designed to achieve high gain and high linearity performance, simultaneously. This dissertation reports the device architecture with a detailed description of the fabrication process, the challenges involved in device fabrication and the solutions explored to overcome them.

Device results including linearity characterization at 30 GHz are discussed. The linearity performance is described through OIP3 and OIP3/Pdc. An OIP3 of 32 dBm, OIP3/Pdc of 15 dB and 12.7 dB transducer gain at 30 GHz were obtained at a bias specific for high linearity. A strategy to achieve high linearity over a wide input bias range is to use derivative superposition at the device-level with a dual-threshold voltage device design. In this approach, the device transconductance (g_m) is engineered to achieve a flat g_m profile over a wide range of gate-bias. The results of the first demonstration of a dual-threshold voltage N-polar GaN transistor show 10.8 dB OIP3/Pdc, 34 dBm OIP3 and 11 dB transducer gain at 30 GHz.

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Chapter 1. Introduction

Most wireless systems today—particularly those used in cellular networks—operate in the low gigahertz (GHz) frequencies. The increasing demand for high data transmission rates is driving the utilization of frequencies in the millimeter wave regime (30 to 300 GHz); this frequency range is currently being investigated for applications such as 5G-LTE, satellite communication, radars for collision detection in automobiles, and other radars for civilian and military use.

Every wireless communication system—ubiquitous in today's age—depends on the ability of a transmitter and a receiver to process signals reliably. In the receiver front-end, the signal is received by the antenna, selected by a low-loss bandpass filter, then amplified by a Low-noise amplifier (LNA). The LNA is the most critical element in the receiver; its function is to amplify the desired signal without distorting it and without introducing additional noise. At the heart of the LNA lies the RF transistor. Key requisites of the RF receiving transistor are high gain, high linearity, and low noise figure. This dissertation focuses on gain and linearity.

The adopted device technology is a high electron mobility transistor (HEMT) based on III-Nitride semiconductor materials, including gallium nitride (GaN), aluminum nitride (AlN) and related aluminum gallium nitride alloys (AlGaN) grown with N-polar orientation. In this dissertation, I present innovative device designs to achieve simultaneously high gain and high linearity at device-level, crucial for high performance receiver application at mm-wave. This chapter explains the requisites of mm-wave receiving transistors, the linearity metrics, and state-of-the-art technologies. It concludes with the synopsis of the entire dissertation.

1.1 Requisites of the mm-Wave Receiving Transistor

This section discusses the important requisites of the mm-wave receiving transistor.

1.1.1 High Linearity

In a crowded wireless spectrum shared by many devices, the linearity of mm-wave transistors is important to avoid devices interfering with each other. Linearity is important for both transmitter and receiver. On the transmitter end, non-linearities can distort the modulated signal and generate power that falls out of the intended channel into adjacent channels. The undesired power in adjacent channels causes adjacent channel interference. On the receiver end, non-linearities can generate spurious signals that are difficult to filter out as they are very close to the fundamental tones (as described in detail in Chapter 2), and can distort or mask a weak desired signal in the presence of large in-band interfering signals [1, 2].

In receivers, there are two possible approaches to improve linearity: at the circuit-level and at the device-level. Circuit-level linearization techniques include feedback, feed-forward, post-distortion [3]. Circuit-level techniques can increase system complexity, cost, and interconnect parasitics, which make these techniques challenging to implement in mm-wave applications.

Device-level linearization techniques are more attractive for mm-wave LNAs as they can eliminate interconnect parasitics and avoid system complexity and cost associated with circuit linearization techniques. Therefore, realizing a highly linear mm-wave transistor is the key to obtain high linearity performance of mm-wave LNAs. Linearization strategies at the device-level will be discussed in Chapter 2.

1.1.2 High Gain

The main purpose of the mm-wave receiving transistor is to amplify the received signal. Therefore, gain is another important requisite. High gain allows to amplify very weak received signals, and feed them to the subsequent blocks in the receiver system, with enough strength to be reliably processed. Additionally, high gain can be useful not only for amplification, but also for linearity. In fact, source and load impedances can be tuned to trade gain for linearity.

1.1.3 Low Noise Figure

Noise is another important factor to be considered when designing a mm-wave receiving transistor. The presence of noise sets a lower limit on the minimum signal level that can be reliably detected by a receiver. It is important that the receiving transistor does not introduce additional noise which would otherwise mask the very weak signal that needs to be amplified. The noise generated by the transistor can be quantified by the noise figure (NF), a measure of the degradation of the signal-to-noise ratio between its input and output.

This dissertation primarily focuses on gain and linearity of mm-wave receiving transistors. Noise figure will be the subject of future research work.

1.2 Linearity Metrics

The linearity of a device can be characterized by a *two-tone* test. In this test, a *two-tone* input at closely spaced frequencies is applied to a device. If the device is non-linear, the output spectrum consists of mixing products in addition to the fundamental tones. These mixing products arise as a linear combination of the fundamental tones, and are called *intermodulation* (IM) products. Since the third-order IM products are close to the fundamental tones, they cannot be easily filtered out and are therefore of serious concern. Linearity is

characterized by measuring the output power in the third-order IM product and comparing it with the output power in the fundamental tone. The following terminologies (depicted in Figure 1.1) are introduced to aid the discussion in sections to follow:

1. IM3 is the power in the third-order IM product (should be small).
2. C/IM3 is the ratio of the power in the fundamental tone (carrier power) to IM3 (decreases with increasing carrier power).
3. Output-referred 3rd order intercept point (OIP3) is the extrapolated output power at which the carrier power equals IM3 (should be large).
4. OIP3 normalized over dissipated DC power (OIP3/P_{DC}), a useful figure of merit to compare the linearity among different devices and bias conditions where power dissipation is important (should be high).

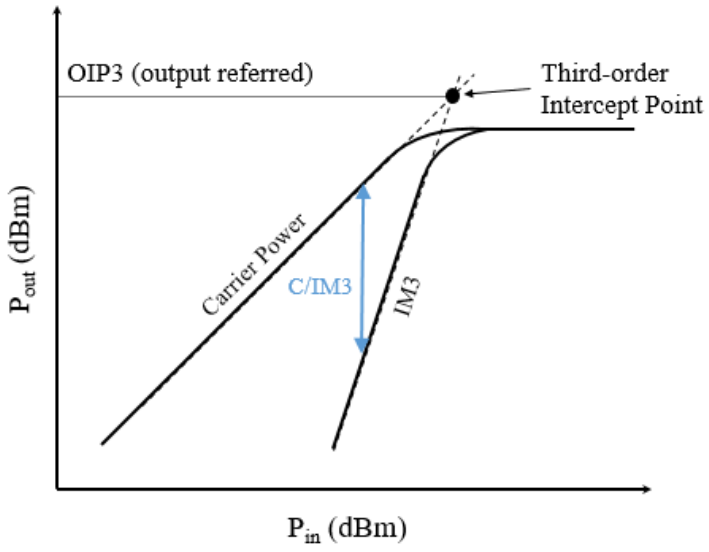

Figure 1.1 Output power resulting from a *two-tone* excitation versus input power in log-log scale. Figure shows output power in the fundamental tone (carrier power), output power in the third-order IM product (IM3) and output-referred 3rd order intercept point (OIP3).

OIP3 and OIP3/P_{DC} values are calculated assuming or extracted in the region where the output power in the fundamental tone and IM3 follow the theoretical lines with slopes 1:1 and 3:1 respectively. This is not always the case for every input power level. Therefore, C/IM3 is sometimes reported in literature to demonstrate the linearity performance of the device over the entire operating range.

1.3 State-of-the-Art GaN Receiving Technologies

So far, GaN HEMTs have primarily been employed for mm-wave power amplification. The physical properties of GaN – a large critical electric field (3.3 MV/cm) and high electron saturation velocity ($2.5 \cdot 10^7$ cm/s), combined with high electron density ($n_s > 10^{13}$ cm^{-2}) and high mobility at the AlGaN/GaN interface – have enabled GaN HEMTs to be excellent candidates for RF power amplification. Due to their power handling capability, low noise figure and the potential for high linearity performance, GaN HEMTs are well suited not only for power amplification, but also for robust receiver applications. In fact, some mm-wave LNAs based on GaN HEMTs have already been reported in the literature [4], [5], [6], [7].

A key advantage of GaN HEMTs over incumbent LNA technologies (e.g., silicon germanium heterojunction bipolar transistors, gallium arsenide HEMTs, indium phosphide HEMTs, etc.) is their intrinsic robustness. In fact, the receiving transistor also needs to be able to handle high input powers as it may be subjected to jammers or interfering signals from nearby transmitters. Including overload protection circuitry for the LNA increases system complexity and introduces additional noise. Therefore, it is desirable for the mm-wave receiving transistor to survive large input powers. Due to the wide band-gap of GaN, it can support high breakdown fields (~8 times that of GaAs). The main advantage of GaN over

existing technologies is its robustness; GaN HEMT technology is capable of realizing LNAs that survive high input power levels [8, 9], eliminating the need for overload protection circuitry, which lowers the overall noise figure.

Traditionally, GaN HEMTs are grown and fabricated in the Ga-polar orientation. So far, solutions for high device-level linearity have been explored for Ga-polar GaN HEMTs. They include: *(i)* HEMTs patterned with variable-width fins [10], *(ii)* HEMTs with threshold voltage modulated along the gate-width demonstrating OIP3 of 43 dBm at 8 GHz [11], *(iii)* HEMTs with graded AlGaN/GaN channel and SiN_x passivation reporting OIP3/P_{DC} of 13.3 dB at 10 GHz [12], *(iv)* HEMTs incorporating planar and variable-width fins demonstrating OIP3/P_{DC} of 8.24 dB at 30 GHz [13], *(v)* HEMTs with graded AlGaN/GaN channel reporting C/IM3 of 30 dBc at 30 GHz [14].

In the N-polar orientation, the inverse polarization fields enable the implementation of device structures that provide excellent mm-wave performance. The benefits of the N-polar orientation are discussed in Chapter 2. The linearity data of N-polar GaN MIS-HEMTs has been reported by Arias et al. [15], and Guidry et al. [16], with OIP3/P_{DC} of ~12 dB at 10 GHz and up to 11.4 dB at 30 GHz respectively. The device structures reported in [15, 16] were designed for mm-wave power amplification, demonstrating breakthrough power density of 8 W/mm at 94 GHz [17]. This work explores N-polar GaN MIS-HEMT technology for low-power receiver applications.

1.4 Synopsis of the Dissertation

Chapter 2 provides insight into the device concept and structural design for high linearity and high gain performance at mm-wave frequencies. The non-linear phenomena in transistors

is analyzed using a power-series technique, showing the relationship between device transconductance, its derivatives and device non-linearity. Bias conditions for high linearity performance are identified. Single- and dual- threshold device designs based on N-polar GaN MIS-HEMT technology are discussed. Chapter 3 describes the fabrication process development for the devices presented in this dissertation. It provides a detailed description of process flow, highlighting the challenges involved and the solutions explored. Chapter 4 presents the device results, analysis and comparison between single- and dual- threshold devices. The DC and pulsed I-V, RF small-signal and mm-wave linearity characteristics are examined. Chapter 5 presents a summary and concluding remarks. It also provides directions for future work.

Chapter 2. Device Design for Linearity and Gain

This chapter discusses device designs to achieve high linearity and high gain performance for receiver applications at mm-wave frequencies. It begins with an analysis of non-linear phenomena in transistors using a power-series technique, leading to the relationship between device transconductance (g_m), its derivatives and device non-linearity (Section 2.1). Based on the g_m profile of GaN HEMTs, two conditions for high linearity are identified in Section 2.2. Device designs for both biasing conditions are explored in this chapter. Both designs are based on N-polar GaN deep-recess HEMT technology (Section 2.3). The device concept and structural design to achieve high linearity and high gain are detailed in Section 2.4 and Section 2.5.

2.1 Non-Linear Phenomena and Device Transconductance

If a *two-tone* input at closely spaced frequencies – ω_1 and ω_2 – is applied to a linear device, the response is an amplification of the two tones at the same frequencies. The output spectrum of a non-linear device, however, consists of other mixing products. The following sub-sections explain this non-linear behavior and establish the relationship between device non-linearity and transconductance. The analysis presented here uses a power-series technique [1, 2] with the assumption that the device contains only memoryless transfer non-linearities.

2.1.1 Intermodulation Distortion

Let us consider a *two-tone* input voltage at closely spaced frequencies – ω_1 and ω_2, applied to a transistor:

$$v_{gs} = V_{pk}[\cos(\omega_1 t) + \cos(\omega_2 t)] \tag{2.1}$$

where, v_{gs} is the gate-source voltage and V_{pk} is the amplitude of excitation. Assuming the transfer non-linearities are memoryless i.e. the output at time 't' depends only on the input at the same instant, the small-signal output current can be modeled as a Taylor series expansion:

$$\boldsymbol{i_d = \sum_{k=1}^{\infty} g_{mk} v_{gs}^k = g_{m1} v_{gs} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + \cdots} \tag{2.2}$$

where,

$$\boldsymbol{g_{mk} = \frac{1}{k!} \frac{\partial^k i_d}{\partial v_{gs}^k}} \tag{2.3}$$

The first three terms of the above series are sufficient to define a weakly non-linear behavior. Here, g_{m1} is the device transconductance (g_m), the first derivative of the i_d (v_{gs}) relationship. The g_m and its derivatives are defined as:

$$\boldsymbol{g_{m1} = \frac{\partial I_D}{\partial V_{GS}},\ g_{m2} = \frac{1}{2} \frac{\partial^2 I_D}{\partial V_{GS}^2},\ g_{m3} = \frac{1}{6} \frac{\partial^3 I_D}{\partial V_{GS}^3}} \tag{2.4}$$

From (2.1) and (2.2), the output current can be expanded as:

$$\begin{aligned} i_d = {} & g_{m1} V_{pk} [\cos(\omega_1 t) + \cos(\omega_2 t)] \\ & + \tfrac{1}{2} g_{m2} V_{pk}^2 [1 + \cos(2\omega_1 t)] + \tfrac{1}{2} g_{m2} V_{pk}^2 [1 + \cos(2\omega_2 t)] \\ & + g_{m2} V_{pk}^2 [\cos(\omega_1 t + \omega_2 t) + \cos(\omega_1 t - \omega_2 t)] \\ & + \tfrac{1}{4} g_{m3} V_{pk}^3 [3\cos(\omega_1 t) + \cos(3\omega_1 t) + 3\cos(\omega_2 t) + \cos(3\omega_2 t)] \\ & + \tfrac{3}{2} g_{m3} V_{pk}^3 \left[\cos(\omega_1 t) + \tfrac{1}{2}\cos(2\omega_2 t - \omega_1 t) + \tfrac{1}{2}\cos(2\omega_2 t + \omega_1 t)\right] \\ & + \boldsymbol{\tfrac{3}{2} g_{m3} V_{pk}^3 \left[\cos(\omega_2 t) + \tfrac{1}{2}\cos(2\omega_1 t - \omega_2 t) + \tfrac{1}{2}\cos(2\omega_1 t + \omega_2 t)\right] + \cdots} \end{aligned} \tag{2.5}$$

The output signal consists of terms other than those at the fundamental frequencies. These mixing products, which arise as a linear combination of the two input frequencies are called *intermodulation* (IM) products.

The output spectrum of second- and third- order IM products is shown in Figure 2.1. The second-order IM products are far from ω_1 or ω_2 and can therefore be easily filtered out. The third-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, which are close to the fundamental tones, cannot be easily filtered out. They are the strongest of all odd-order IM products, closest to the fundamental tones and are therefore of great concern. For an arbitrary input signal with several frequencies, the in-band third-order IM products can distort the modulated signal. The IM products that lie outside the intended band or channel of a transmitter generate power that falls into adjacent channels, potentially causing interference with nearby receivers. Large interfering signals can generate IM products within the passband of a receiver, which can distort or mask a weak desired signal making it difficult to detect [1, 2].

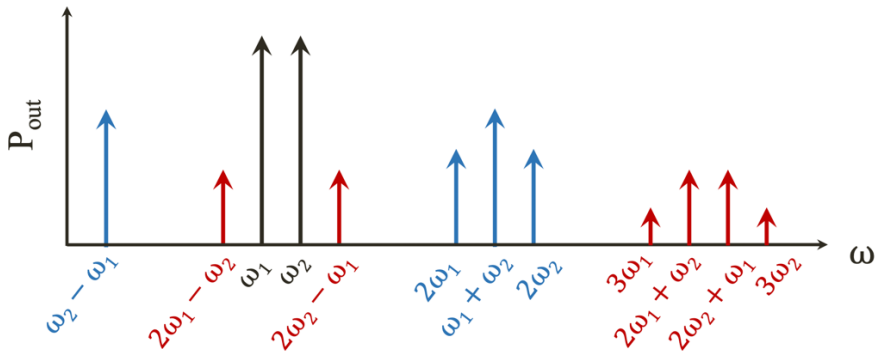

Figure 2.1 Output spectrum of a non-linear device resulting from a *two-tone* input at closely spaced frequencies ω_1 and ω_2. Second- and third- order intermodulation (IM) products are shown with blue and red lines respectively.

2.1.2 Third-Order Intercept Point

From (2.5), we observe that the coefficient of first-order output term is directly proportional to V_{pk}. Whereas, the coefficient of third-order term is proportional to V_{pk}^3. The output power in the third-order IM product is small but rises sharply as the input power increases. If the output power is plotted against the input power in log-log scale (Figure 2.2), the first-order response is a line with slope 1, and the third-order response is a line with slope 3. Both first- and third- order responses exhibit compression at high input powers. When we extrapolate the idealized responses, the two lines with different slopes intersect at a point. This hypothetical point—where the third-order power is equal to the first-order power—is called the *third-order intercept point* (IP3). IP3 can be referred to either the input (IIP3) or the output (OIP3). High IIP3 or OIP3 is indicative of a more linear device: higher values represent smaller power in the third-order IM product in relation to that in the fundamental tone.

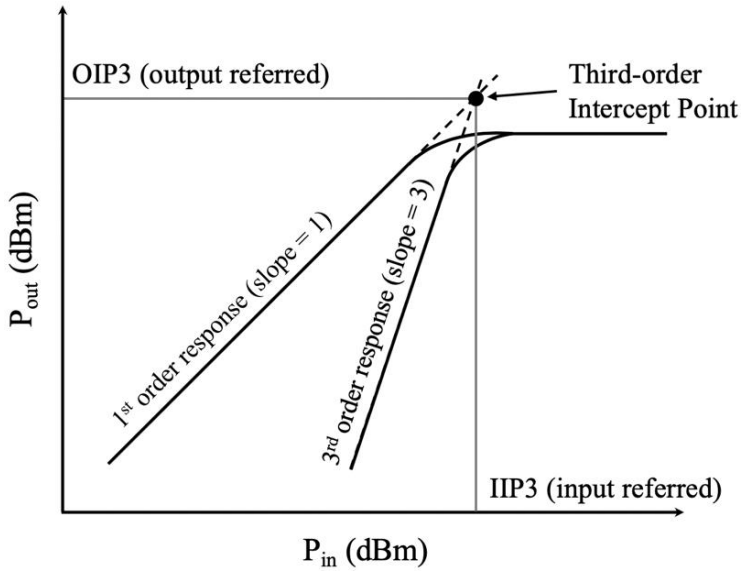

Figure 2.2 Output power resulting from a *two-tone* excitation versus input power in log-log scale. The third-order intercept point is the intersection between the extrapolated linear responses of the first- and third- order.

Let us calculate the output power in the fundamental tone (P_{01}) and in the third-order IM product (P_{03}) when delivered to a load (R_L).

$$\boldsymbol{P_{01} = \frac{1}{2} \cdot \left(g_{m1} V_{pk}\right)^2 R_L} \tag{2.6}$$

$$\boldsymbol{P_{03} = \frac{1}{2} \cdot \left(\frac{3}{4} g_{m3} V_{pk}^3\right)^2 R_L} \tag{2.7}$$

At the third-order intercept point,

$$\boldsymbol{P_{01} = P_{03}} \tag{2.8}$$

Substituting (2.6) & (2.7) into (2.8) and solving for V_{pk}:

$$\boldsymbol{V_{pk} = \sqrt{\frac{4}{3} \frac{g_{m1}}{g_{m3}}}} \tag{2.9}$$

Output-referred third-order intercept point (OIP3) is given by substituting (2.9) into either (2.6) or (2.7):

$$OIP3\ [W] = P_{01} = P_{03}$$

$$= \frac{1}{2} \cdot \left(\sqrt{\frac{4}{3} \frac{g_{m1}^3}{g_{m3}}}\right)^2 \boldsymbol{R_L} = \frac{2}{3} \frac{g_{m1}^3}{g_{m3}} \boldsymbol{R_L} \tag{2.10}$$

$$\boldsymbol{OIP3[dBm] = 10\, log_{10}\left(\frac{2}{3} \frac{g_{m1}^3}{g_{m3}} R_L\right) + 30} \tag{2.11}$$

Equation (2.11) shows that high linearity is achieved when the device transconductance (g_m) is high and the corresponding g_{m3}, the third derivative of I_D (V_{GS}) relationship is low. Based on this relationship, the following section describes the bias conditions for achieving high linearity.

2.2 Bias Conditions for High Linearity

Transconductance (g_m) and its derivatives dominate the linearity characteristics of a transistor. The sharp decrease in g_m beyond the g_m peak as the gate voltage is increased is common in GaN HEMTs (Figure 2.3). This effect manifests as "gain compression" and drop in current-gain cutoff frequency (f_T) at high drain currents. While factors such as source access region resistance may contribute to g_m roll-off [18, 19, 20], it has theoretically been shown that optical-phonon scattering is the dominant g_m roll-off mechanism in GaN HEMTs [21]; the latter is an inherent limitation of GaN. The peaked profile of electron velocity extracted from N-polar GaN deep-recess HEMT [22] corroborates the theoretical model in [21].

From the g_m profile of GaN HEMTs and the relationship between g_m, g_{m3} and OIP3 in equation (2.11), there are two bias conditions for high OIP3: *(i)* at the g_{m3} zero-crossing point, where the device is turning on and the OIP3/P_{DC} is expected to peak over a limited range of gate-bias, and *(ii)* at the g_m peak, where several approaches—including but not limited to polarization engineering [23, 24, 12, 14]—are implemented aiming for a flat g_m profile, with high OIP3/P_{DC} over a wide range of input-bias. In this dissertation, device designs for both bias conditions are explored.

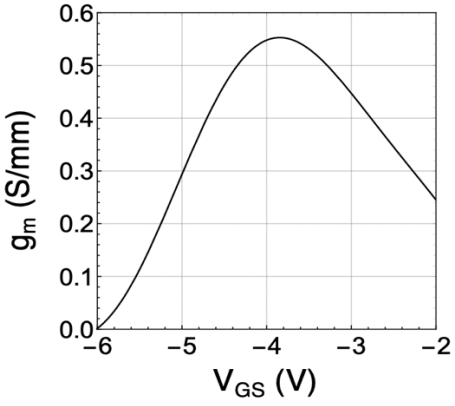

Figure 2.3 Transconductance (g_m) profile of a GaN HEMT showing g_m roll-off at high gate bias (drain current).

2.3 Technology Platform: N-polar GaN Deep-Recess HEMT

The device designs presented in this dissertation are based on N-polar GaN deep-recess HEMT technology developed at UCSB, demonstrating breakthrough power density of 8W/mm at 94 GHz [17]. A standard device structure is shown in Figure 2.4 (a). The epitaxial structure is grown on a miscut SiC substrate by means of metal-organic chemical vapor deposition (MOCVD) [25]. The active layers—backbarrier, GaN channel, AlGaN cap and GaN cap—are grown on a semi-insulating Fe-doped GaN buffer. The Fe-doping compensates the effects of residual oxygen – a shallow donor in GaN [26]. The backbarrier consists of 10-nm Si-doped GaN, 20-nm Si-doped graded $Al_xGa_{1-x}N$ (x from 5% to 38%), 10-nm unintentionally doped (UID) $Al_{0.38}Ga_{0.62}N$ spacer, and 0.7-nm AlN.

The energy band diagram of the N-polar epitaxial structure—simulated using BandEng [27]—is shown in Figure 2.4 (b). The curvature of the Si-doped graded AlGaN in the backbarrier keeps the Fermi-level (E_F) away from the valence band edge (E_V); this is to avoid the modulation of hole traps [28, 29]. The UID AlGaN spacer separates the Si-doped region from the channel to prevent scattering from ionized donors. A binary AlN interlayer is inserted between the GaN channel and the AlGaN backbarrier to reduce alloy-disorder-scattering and enhance the confinement of 2-DEG in the GaN channel (large ΔE_C at the AlN/GaN interface) [30, 31].

The backbarrier is also the charge inducing layer. Therefore, N-polar GaN HEMT architecture allows for the vertical scaling of GaN channel, while maintaining high 2-DEG sheet charge density (n_s). Furthermore, the centroid of 2-DEG is displaced toward the gate electrode, reducing the effective gate-channel distance and enhancing the gate-source capacitance (higher transconductance) [31]. This becomes more significant as the

gate-channel distance is reduced, to maintain a good aspect-ratio in mm-wave devices with scaled gate-length (L_g).

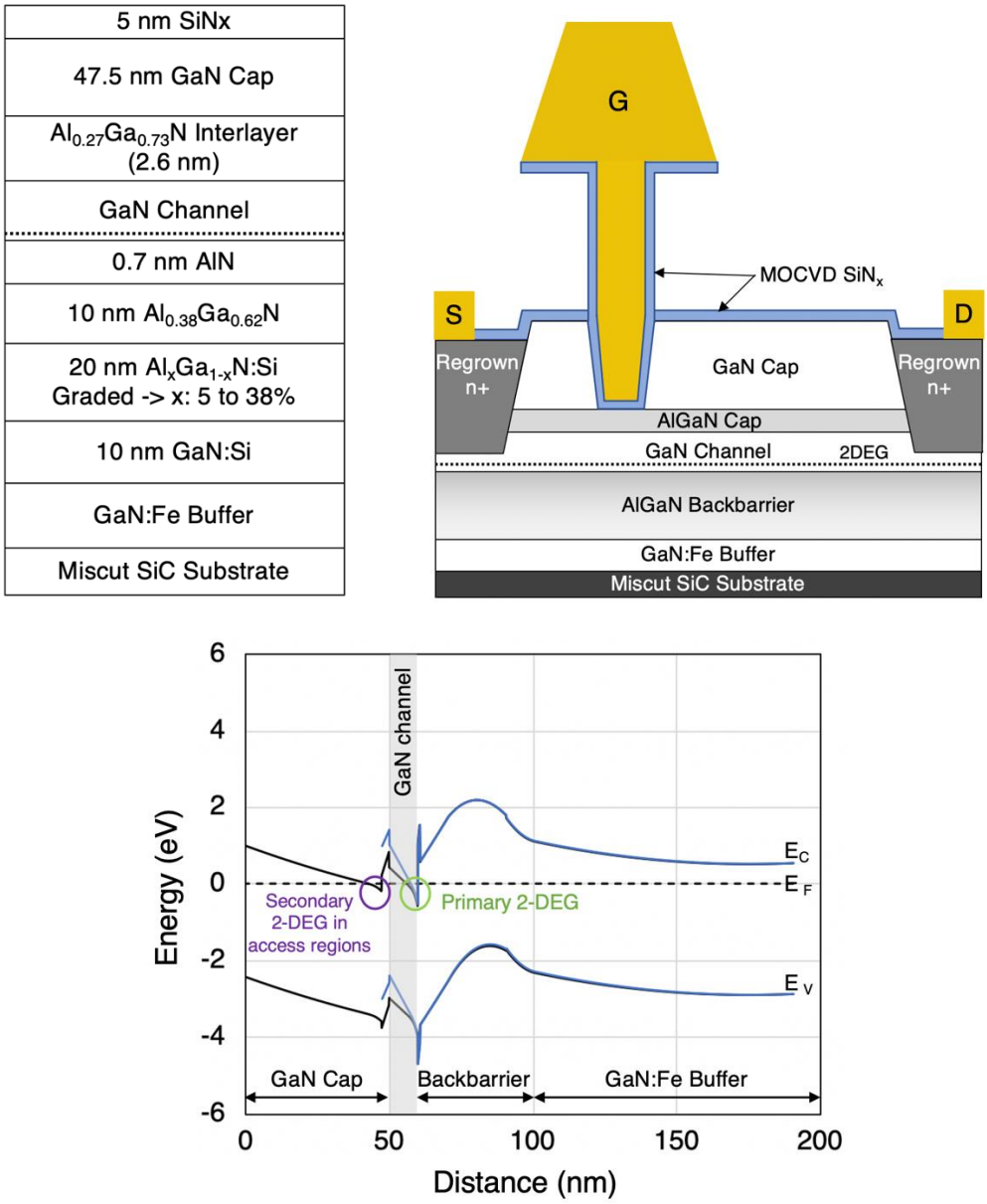

Figure 2.4 (a) MOCVD epitaxy and schematics of a N-polar GaN deep-recess high electron mobility transistor. **(b)** Energy band-diagram showing the curvature of the graded AlGaN backbarrier and improved access-region conductivity in N-polar GaN deep-recess HEMTs.

The gate trench is realized using a selective dry etch to remove the GaN cap and stop on the AlGaN cap (2.6-nm $Al_{0.27}Ga_{0.73}N$) [32]. Details of this selective etch process will be discussed in Chapter 3. The low Al composition of AlGaN cap is chosen to prevent the depletion of 2-DEG n_s. A high quality SiN_x gate dielectric is deposited by MOCVD in the gate trench. The combination of AlGaN cap and SiN_x gate dielectric serve to reduce gate leakage and improve breakdown voltage [33]. The Cr/Au T-gate metal stack is deposited in the gate trench using a self-aligned process developed by Romanczyk, where the hard mask used during the recess etch to define the gate trench also defines the foot of the T-gate [34]. This allows gate metal to fully cover the gate trench eliminating dispersion from partial metal coverage [33, 34].

The low-resistance source and drain ohmic contacts are realized by n+ GaN contacts regrown by MBE. Since the buried AlGaN backbarrier is the charge inducing layer, the 2-DEG is preserved under the ohmic contacts, yielding very low contact resistance in the order of 0.05 Ω-mm. The details of the regrowth process will be discussed in Chapter 3.

The GaN cap serves two functions [35, 17]. First, it provides DC to RF dispersion control. It is grown *in-situ* and therefore the interface between the GaN cap and AlGaN cap is pristine and high quality. Crystalline GaN cap moves surface states away from the GaN channel, reducing dispersion. Second, it enhances source and drain access region conductivity by reducing the vertical electric fields and increasing charge density in the channel (Figure 2.4). This is an outcome of the built-in polarization of N-polar GaN structure. A secondary channel forms at the interface between the AlGaN cap and the GaN cap; while this may shield the primary channel from the effects of surface traps in the access regions, a high sheet charge density in the secondary channel can potentially reduce the breakdown voltage of the device.

As mentioned in Section 2.2, there are two bias conditions for high linearity: *(i)* at the g_{m3} zero-crossing point, where the device is turning on and the OIP3/P_{DC} peaks over a narrow range of input-bias, and *(ii)* at the g_m peak, where a flat profile is desired, with high OIP3/P_{DC} over a wide range of input-bias. In the following sections, I report device designs for both bias conditions. The device fabrication, results and comparison between the two device designs will be discussed throughout the dissertation.

2.4 Device Design #1: Single-threshold Device

The term "single-threshold" refers to the fact that the threshold voltage of the device is the same along the entire gate-width (as in a conventional HEMT). The single-threshold device is designed to operate at the g_{m3} zero-crossing point, where the device is turning on and the OIP3/P_{DC} is expected to peak over a limited range of input-bias. At this bias condition, the current density (and therefore power dissipation) is low. The goal is to simultaneously achieve high linearity and high gain performance at small-signal levels, with lowest possible power dissipation for receiver applications.

While the device is biased at the g_{m3} zero-crossing point for high linearity, the device structure is designed for high gain. In two-tone RF measurements (discussed in Chapter 4), it has been observed that there is a trade-off between gain and linearity; devices with high gain can better accommodate this trade-off. In the design space of the single-threshold device based on N-polar GaN deep-recess HEMT technology, there are two important parameters to achieve high gain: *(i)* thin GaN cap, and *(ii)* scaled gate-length (L_g).

2.4.1 Thin GaN Cap

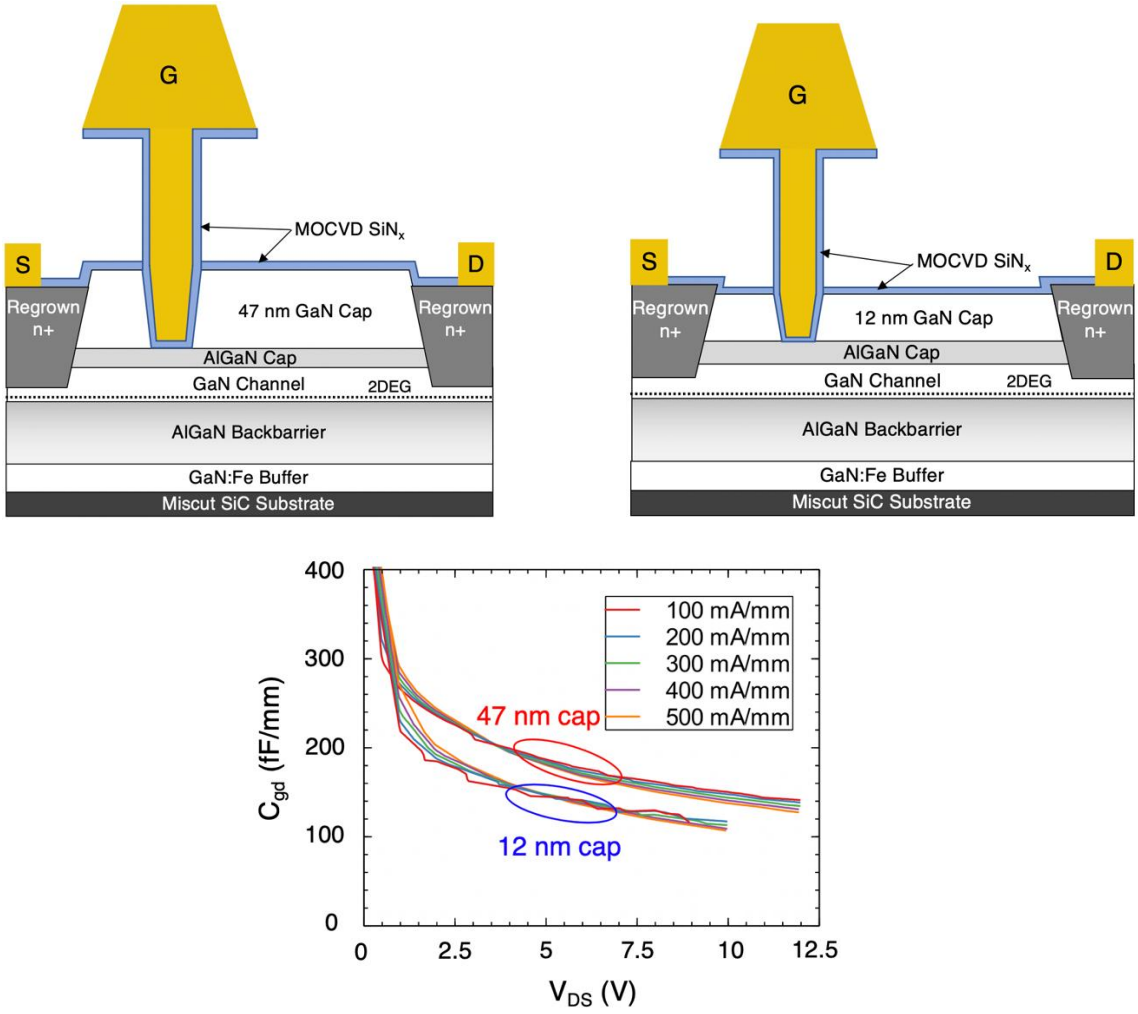

Figure 2.5 Reduced GaN cap thickness showing lower gate-drain capacitance (C_{gd}). Data, courtesy of Dr. Brian Romanczyk; Small-signal parameter extraction, courtesy of Dr. Matthew Guidry.

The N-polar GaN deep-recess HEMT structure developed for power amplification has a 47 nm thick GaN cap [35, 17]. The thick GaN cap provides dispersion control at high drain bias, to achieve high efficiency and high output-power density for transmitter applications at mm-wave frequencies. The single-threshold device, however, is designed to operate at low drain bias voltages. For receiver application, the drain bias voltage is smaller than that used for power amplifiers in order to reduce power consumption and noise figure. Therefore, the

single-threshold device has a thin GaN cap (12-to-20 nm). It is designed to improve gain by reducing parasitic fringing capacitance and associated parasitic delays, while still availing of the benefit of improved access region conductivity due to built-in polarization of N-polar GaN structure. Figure 2.5 shows the gate-drain capacitance (C_{gd}) extracted using the small-signal model described in [36] for two N-polar GaN HEMT structures: one capped with 47-nm GaN and the other with 12-nm GaN[1]. The C_{gd} is plotted against drain bias for current densities ranging from 0.1 to 0.5 A/mm. We observe that C_{gd} of the HEMT capped with 12-nm GaN is 40 fF/mm lower than the sample with 47-nm GaN.

2.4.2 Scaled Gate-Length (L_g)

Scaling the gate-length of a transistor reduces the time taken by charge carriers to transit through the gated region. This improves device transconductance, which contributes to high gain. As L_g is scaled, it is important to maintain a good aspect-ratio—ratio of L_g to the distance between gate and 2-DEG—in order to avoid short-channel effects. At the present time, Schottky contact to the N-polar AlGaN/GaN surface has yet to be realized. Therefore, the SiN_x gate dielectric and the underlying AlGaN cap are essential to reduce gate leakage and improve breakdown voltage [33]. To maintain a good aspect-ratio in scaled L_g devices, the GaN channel can be vertically scaled.

In a N-polar GaN HEMT architecture, the GaN channel can be scaled while maintaining high 2-DEG sheet charge density (n_s); the Si-doping in the backbarrier can be increased to compensate for the decrease in n_s with reduced channel thickness[2]. However, as the GaN

[1] Data, courtesy of Dr. Brian Romanczyk; Small-signal parameter extraction, courtesy of Dr. Matthew Guidry.

[2] While adjusting Si-doping, it is worthwhile to note that over-doping can lead to a formation of parallel channel in the backbarrier [51].

channel is aggressively scaled while maintaining the same n_s, the vertical electric fields are stronger and the electron wavefunction penetrates further into the backbarrier, reducing electron mobility (μ_e). The reduction in μ_e has been attributed to scattering mechanisms such as: interface-roughness scattering [37]; alloy-disorder scattering [38]; scattering from charged-interface-states and surface-state-dipoles [39]. The mobility drops rapidly as the channel thickness is reduced from 9 to 8 nm [40]. Therefore, in the single-threshold device design, the GaN channel is designed to be 10-nm thick, to allow for gate-length scaling without degrading electron mobility.

2.4.3 Single-threshold Device Parameters

The physical definition of single-threshold device parameters are shown in Figure 2.6. Gate-length (L_g) is the physical base of the gate trench and includes the thickness of SiN_x gate-dielectric. In the single-threshold device design, L_g ranges from 45 to 60 nm. Gate-source spacing (L_{gs}) is the distance between the edge of n+ regrowth and the source-side edge of gate trench. Small L_{gs} is desired to reduce source resistance. L_{gs} is designed to accommodate T-gate alignment tolerance to prevent the shorting of gate and source. $L_{r,slope}$—the base of the sloped side-wall of the gate-trench—is taken into account in the design of L_{gs}. The uneven topology at the n+ regrowth edge on the source-side can transfer to the hard mask used to define the gate trench; this leads to uneven thickness of hard mask close to the n+ regrowth edge, thereby complicating the process of defining the hard mask and subsequently defining the gate trench [34]. With all these considerations, L_{gs} is nominally designed to be 85 nm. Gate-drain spacing (L_{gd}) is designed to achieve breakdown voltage of ~40V. Based on past study of N-polar GaN deep-recess HEMTs [17], L_{gd} is designed to be ~300 nm. Ohmic-regrowth spacing is the distance between the edge of ohmic contact and the edge of n+ regrowth on the source side

($L_{or,s}$) and the drain side ($L_{or,d}$). $L_{or,s}$ and $L_{or,d}$ are limited by the alignment tolerance of the ohmic layer, which is patterned by photolithography. They are defined to be 400 nm. The base of the top gate (T_G) is 400-to-500 nm and the T-gate stem is designed to be 225 nm (with tolerance of ±15 nm). The device has a two-finger T-feed layout [41] with co-planar waveguide probe pads. The total gate-width (W_G) of the two fingers is designed to be 2 x 25 µm.

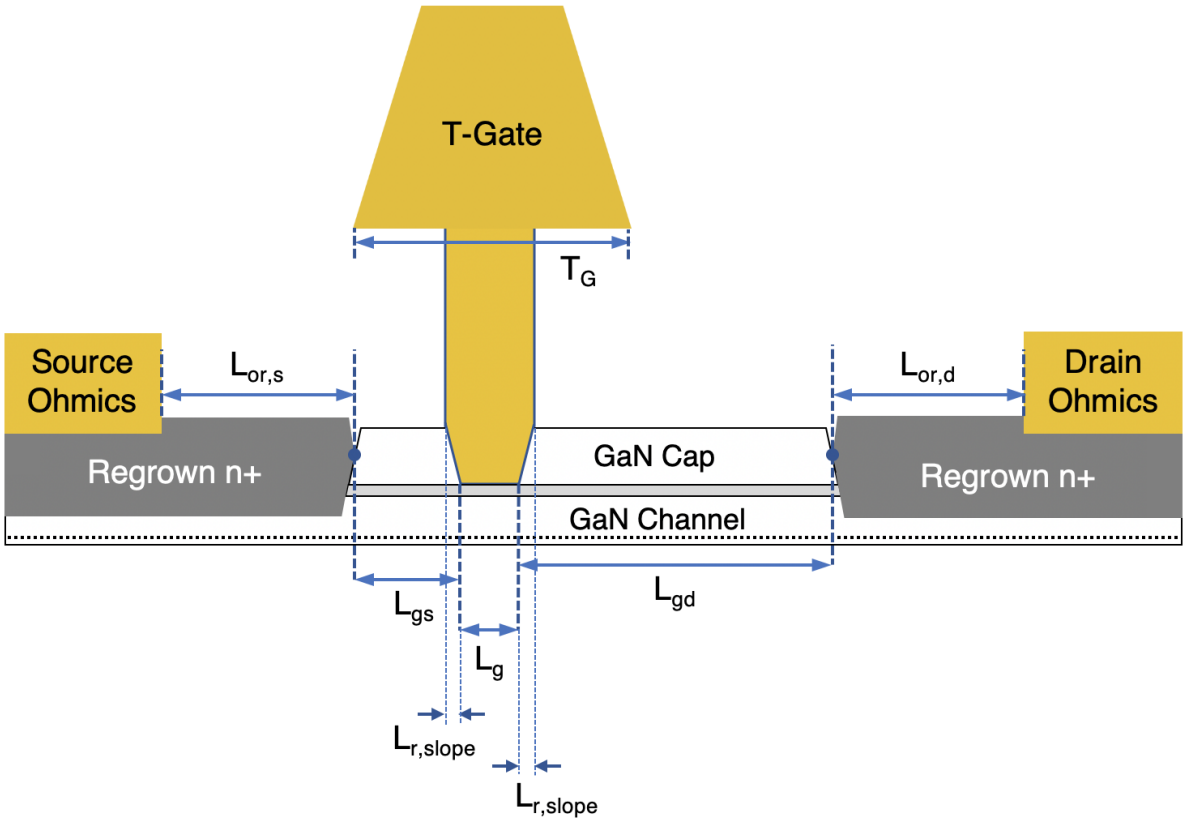

Figure 2.6 Definition of single-threshold device lateral parameters.

2.5 Device Design #2: Dual-threshold Device

The device design presented in this section implements a circuit-level linearization technique, namely – Derivative superposition (DS), at the device-level to cancel g_m derivatives and tailor the g_m profile for high linearity over a wide range of input-bias. Device-level implementation of DS has been reported in literature; it has been achieved by patterning fins with variable widths [10], incorporating a combination of planar and multi-width fins [13], and recessing the gate to different depths along the gate-width [11]. The concept of DS, implementation of DS at the device-level and the dual-threshold device structure are discussed in the following sub-sections.

2.5.1 Derivative Superposition

Derivative superposition (DS) is traditionally a circuit technique [42, 43], whereby linearization is achieved by the parallel combination of two (or more) transistors—having the same threshold voltage (V_T) but driven at different gate-bias (V_G)—such that the positive g_m derivative of one device cancels out the negative g_m derivative of another. There are two parameters – gate-drive ($V_G - V_T$) and gate-width (W_G), which can be adjusted for g_m derivative cancellation. In the circuit technique, V_T is the same whereas, V_G and W_G are different for the two transistors. The difference in gate-drive aligns the positive g_m derivative of one device with the negative g_m derivative of another. The gate-widths are selected so that the two g_m derivatives are equal and opposite. Figure 2.7 shows the g_{m3} profiles of two devices and the composite g_{m3} of their parallel combination. We can observe that there is an extended range of input-bias where the composite g_{m3} is essentially zero and the OIP3/P_{DC} is expected to be high.

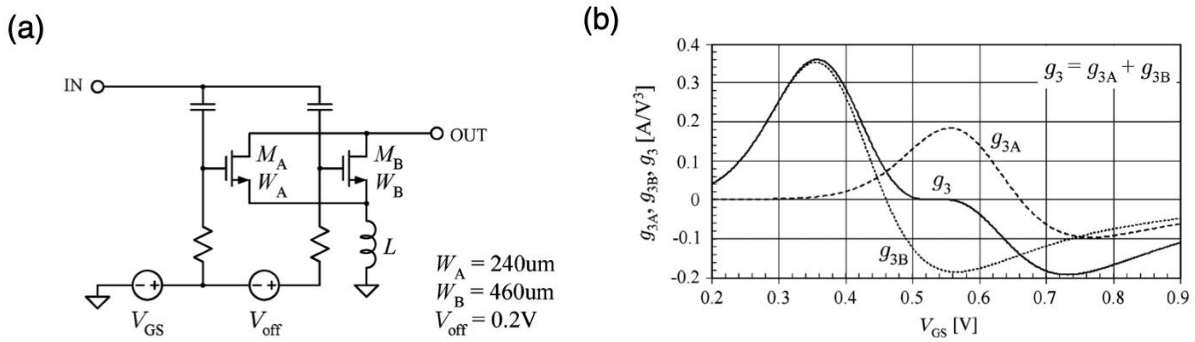

Figure 2.7 Derivative superposition: (a) Schematics of two transistors T_A, T_B in parallel combination. (b) The g_{m3} profiles of M_A, M_B and their parallel combination exhibiting g_{m3} cancellation over an extended range of bias. Figure © [2005] IEEE **[43]**.

DS is one of the many circuit techniques implemented for linearization. Implementing these techniques increases system complexity and cost. Moreover, at mm-wave frequencies, biasing the two devices separately and combining them is challenging: the associated interconnect parasitics degrade the overall circuit performance. Therefore, the approach here is to achieve g_m derivative cancellation with a single device – a dual-threshold device.

2.5.2 Derivative Superposition at the Device-level

A "dual-threshold" device consists of segments of two different threshold voltages – V_{T1} and V_{T2} along its gate-width. It implements DS at the device-level. To reiterate, there are two parameters – gate-drive ($V_G - V_T$) and gate-width (W_G), to be adjusted for g_m derivative cancellation. In the device technique, the applied gate-bias (V_G) remains the same whereas, V_T and W_G are varied for the two different segments within the device. Figure 2.8 shows the top view and cross-sectional schematics of the dual-threshold device. The two threshold voltages – V_{T1} and V_{T2} are defined by recessing the gate to different depths, forming a castellated structure along the gate-finger. As shown in Figure 2.8, V_{T1} and V_{T2} are defined epitaxially with AlGaN etch-stop layers. V_{T2} is designed to be a more negative threshold

voltage than V_{T1} as the gate is placed further away from the channel. In the castellated gate-finger, the spacing between identical segments would ideally be in the order of the transfer length. This would allow instantaneous current combination in the source and drain ohmic regions with no parasitic inductance.

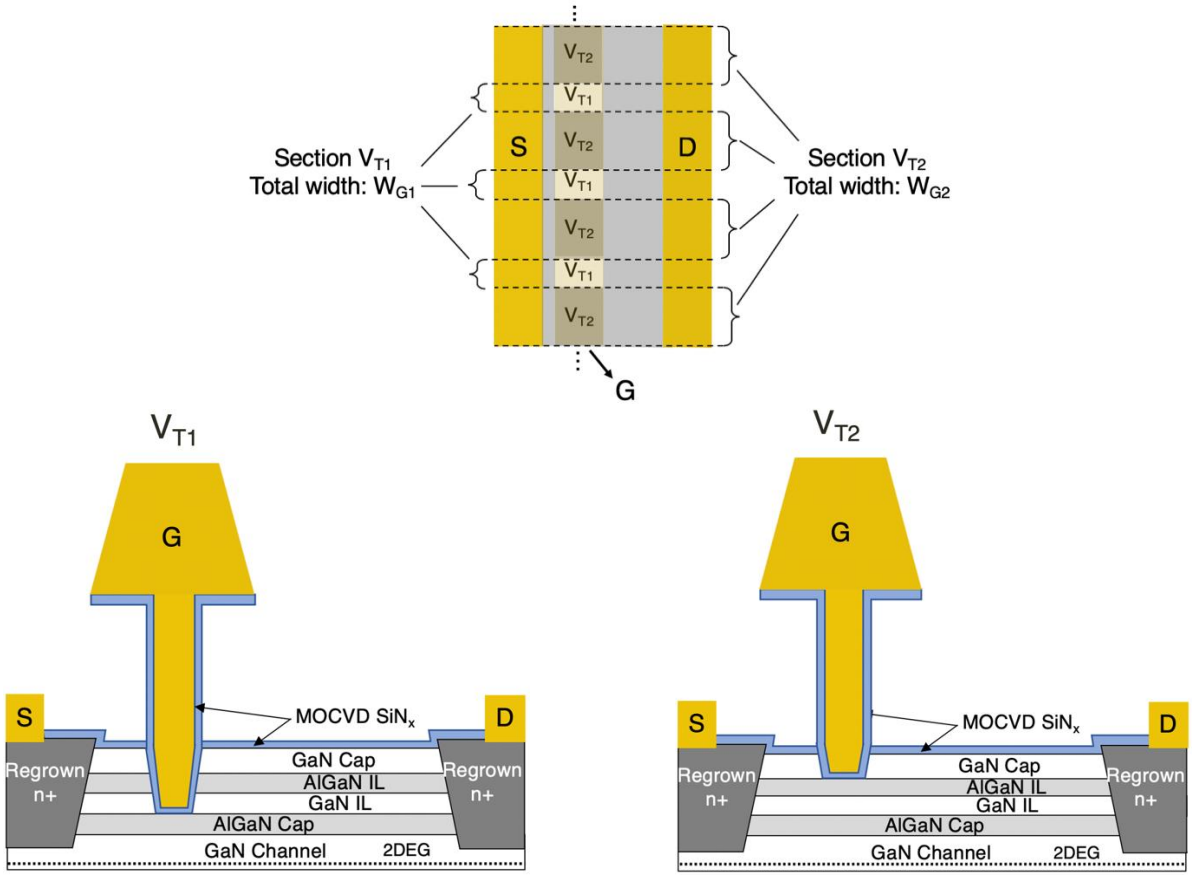

Figure 2.8 Schematics of dual-threshold device: top-view showing sections – V_{T1} and V_{T2} along the gate-width (top); cross-section V_{T1} (bottom left); cross-section V_{T2} (bottom right). Threshold voltages – V_{T1} and V_{T2} are defined epitaxially with AlGaN etch-stop layers.

2.5.3 Dual-threshold Device Parameters

The lateral device parameters of the dual-threshold device—L_g, L_{gs}, L_{gd}, $L_{or,s}$, $L_{or,d}$, $L_{r,slope}$, T_G and W_G—are the same as the single-threshold device (Figure 2.6). These are defined for section V_{T2}. The dual-threshold device also has a two-finger T-feed layout [41] with co-planar waveguide probe pads. There are additional parameters for the dual-threshold device. $V_{T,\,diff}$ is

defined as the difference between threshold voltages $-V_{T1}$ and V_{T2}. It is defined epitaxially with the thickness of AlGaN and GaN interlayers. The ratio of the total width of section V_{T1} to section V_{T2} (W_{G1}:W_{G2} also expressed as $\%W_G$) is designed for the two g_m derivatives to be equal and opposite, to allow g_m derivative cancellation. W_{G1} and W_{G2} are defined by photolithography. This determines the device parameter n_{seg} – defined as the number of V_{T1} segments. The spacing between V_{T2} segments—or equivalently the width of each V_{T1} segment—is ~2µm, designed to ensure that the dual-threshold devices yield. The challenges involved in device fabrication will be discussed in Chapter 3.

2.5.4 Comparing g_{m3} and g_{m2} Cancellation

At the device-level, both g_{m2} and g_{m3} cancellations are explored. The analysis presented here is carried out on existing N-polar GaN deep-recess HEMT data[3]. The data is empirically fit with Angelov model (to smooth it and give accurate derivatives beyond the first), and establishes a baseline for section V_{T1} of the dual-threshold device. $V_{T,\,diff}$ is chosen such that the positive g_m derivative of section V_{T1} aligns with the negative g_m derivative of section V_{T2}. The transfer characteristics of section V_{T2} is predicted by: *(i)* shifting the transfer curve of section V_{T1} by $-V_{T,\,diff}$, and *(ii)* scaling its g_m profile by the corresponding change in gate-source capacitance (C_{gs}), with the assumption that the shape of g_m remains unchanged. The gate-width of the sections are scaled so that the two g_m derivatives are equal and opposite.

[3]Data, courtesy of Dr. Brian Romanczyk [17]; Angelov model analysis for g_{m2} and g_{m3} cancellation, courtesy of Dr. Matthew Guidry.

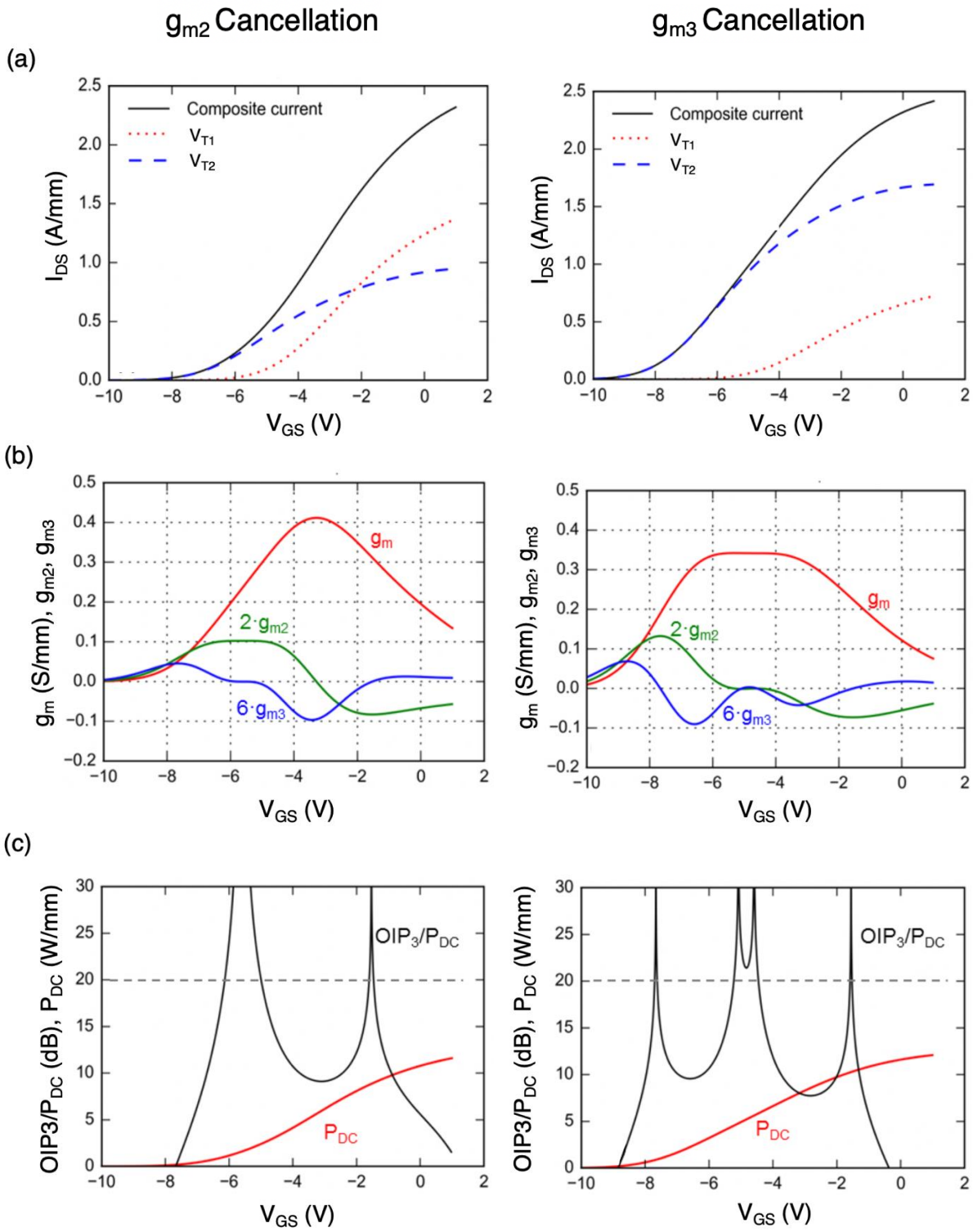

Figure 2.9 Comparison between g_{m2} and g_{m3} cancellation based on Angelov model. (a)Transfer I-V characteristics showing contribution from sections V_{T1} & V_{T2}, and their combination. (b) Composite g_m and its derivatives (g_{m2}, g_{m3}). (c) Composite OIP3/P_{DC} versus input-bias. Data, courtesy of Dr. Brian Romanczyk **[17]**. Angelov model analysis for g_{m2} and g_{m3} cancellation, courtesy of Dr. Matthew Guidry.

Figure 2.9 illustrates g_{m3} and g_{m2} cancellation. The transfer curves of section V_{T1}, section V_{T2}, and the dual-threshold device, are shown. The g_m and its derivatives, and the OIP3 calculated using equation (2.11) derived in Section 2.1.2, are also shown. In the case of g_{m3} cancellation (shown in Figure 2.9), the calculated OIP3/P_{DC} is over 20 dB over an input-bias range of 1.1 V. In this region, g_{m3} is essentially zero, but g_{m2} has a broad peak and therefore, the second-order non-linearities are expected to be high; if there is a feedback path, the second-order non-linearities can mix with the fundamental tones to generate third-order products. The corresponding g_m is low, resulting in low gain. In the case of g_{m2} cancellation (shown in Figure 2.9), the calculated OIP3/P_{DC} is over 20 dB over an input-bias range of 0.8 V. The broad, flat g_m peak is indicative of an inherently linear device. The g_{m3} is greatly reduced in the input-bias range where g_{m2} is essentially zero. The corresponding g_m is also high. Therefore, the dual-threshold device is designed for g_{m2} cancellation. Based on this analysis, g_{m2} cancellation requires $V_{T,\,diff}$ of 3V and 33% of the total device-width comprised of section V_{T1}.

2.5.5 Dual-threshold Device Structure

Although the concept of dual-threshold device can be applied to both power and receiver applications, we are targeting device design for receiver applications. Figure 2.10 shows the dual-threshold device designed for g_{m2} cancellation, with schematics of section V_{T1} and V_{T2} and their corresponding energy band diagrams. The epitaxial structure is grown on a miscut SiC substrate [25]. The active layers are grown on Fe-doped GaN buffer. The backbarrier, GaN channel and AlGaN cap layers are the same as the single-threshold device. The 2-DEG forms in the GaN channel, at its bottom interface with the AlGaN backbarrier. The GaN channel is designed to be 10-nm thick, to allow for gate-length scaling without degrading

electron mobility [40]. In section V_{T1} shown in Figure 2.10 (b), the combination of the AlGaN cap (2.6-nm $Al_{0.27}Ga_{0.73}N$) with 5-to-7 nm SiN_x gate dielectric reduces gate leakage and improves breakdown voltage [33]. The low Al composition of the AlGaN cap prevents the depletion of 2-DEG in the channel.

In section V_{T2} shown in Figure 2.10 (c), there are additional layers under the gate: *(i)* 2.6-nm $Al_{0.34}Ga_{0.66}N$ interlayer (IL) and *(ii)* 10-nm GaN IL. The combination of AlGaN IL and GaN IL define $V_{T,\,diff}$ at the epi-level. For g_{m2} cancellation, the layers are designed to obtain $V_{T,\,diff}$ of 3V. The high Al composition in the AlGaN IL prevents the formation of a parallel channel between GaN IL and AlGaN cap as shown by the band diagram in Figure 2.10 (c). The formation of a parallel channel under the gate in section V_{T2} influences its g_m characteristics, which may adversely affect g_m derivative cancellation.

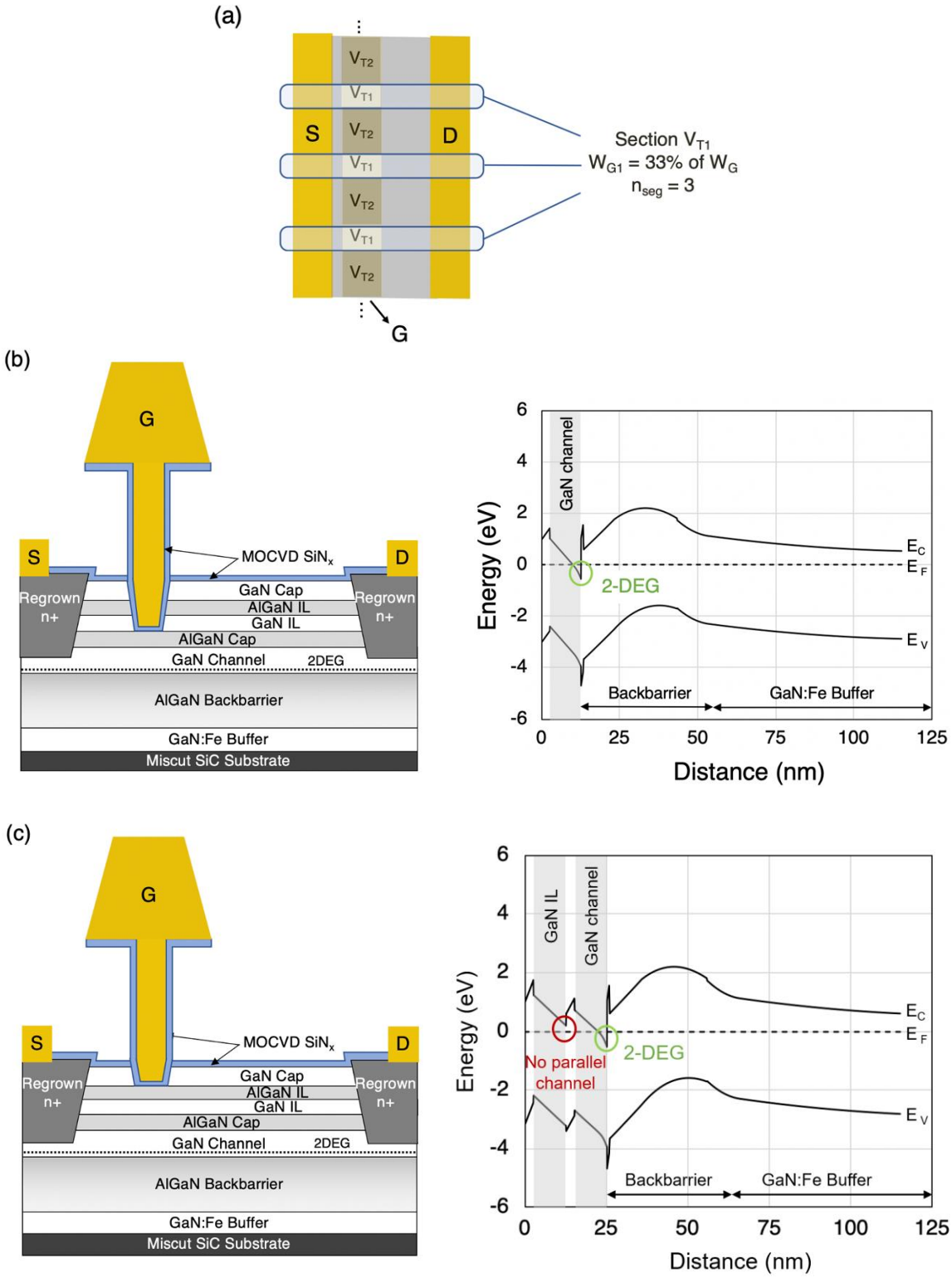

Figure 2.10 Dual-threshold device designed for g_{m2} cancellation. **(a)** Top view showing sections V_{T1} and V_{T2}. **(b)** Cross-section V_{T1} and **(c)** V_{T2} with corresponding energy band diagram.

Chapter 3. Device Fabrication

This chapter describes the fabrication process development for single- and dual- threshold devices. It begins with a detailed description of process flow (Section 3.1), highlighting the challenges involved. The fabrication steps are based on the self-aligned process developed by Romanczyk [34]—which derives from past work by Wienecke [33], Denninghoff [44] & Kolluri [45]—with modifications to realize two different threshold voltages – V_{T1} and V_{T2} – in the dual-threshold device. As mentioned in Chapter 1, the two threshold voltages are defined at the epi-level with AlGaN etch-stop layers—to ensure etch-depth accuracy and process reproducibility. Therefore, the process has been developed for two successive selective etch of GaN over AlGaN. The dual selective etch process is described in detail in Section 3.2. A castellated gate-trench—with well-defined V_{T1} and V_{T2} sections—is achieved by using a second mask during the gate recess etch; section V_{T2} is masked off and the openings in the second mask define section V_{T1}. The challenges involved in the masking process and the solutions explored are discussed in Section 3.3.

3.1 Process Flow Description

Both single- and dual- threshold devices are fabricated on the same wafer. The epitaxial structure (shown in Figure 3.1) is grown on a miscut SiC substrate by means of metal-organic chemical vapor deposition (MOCVD) [25]. As mentioned in Chapter 1, the epitaxial stack consists of semi-insulating Fe-doped GaN buffer, AlGaN backbarrier, GaN channel, AlGaN cap, GaN interlayer (IL), AlGaN IL and GaN cap. Since N-polar GaN surface is etched and roughened by tetramethyl ammonium hydroxide (TMAH) based developers, the epitaxial structure is protected with an *in-situ* grown SiN_x layer (5 nm).

The first module is the regrowth of n+ GaN for source and drain ohmics (Figure 3.1). An oxide mask protects the source-to-drain region during the regrowth. 10-nm Al_2O_3 is deposited by atomic layer deposition (ALD), followed by the deposition of 350-nm SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). SiO_2 is the regrowth mask and Al_2O_3 is the etch-stop layer for regrowth mask patterning. A thin film of Cr (15 nm) is deposited using electron-beam evaporation. The source-to-drain spacing (L_{sd}) is defined with electron-beam lithography using UVN 30 – a negative deep UV photoresist[4]. After exposure and development of the resist, Cr is patterned with inductively coupled plasma (ICP) dry etch based on Cl_2/O_2 chemistry, following which the regrowth dimensions are examined by scanning electron microscope (SEM). If the E-beam lithography process needs re-work, Cr can be removed and re-deposited with the regrowth mask intact. The regrowth mask (SiO_2) is patterned with high-power ICP dry etch based on $CF_4/CHF_3/O_2$ chemistry. The SiO_2 etch stops in the Al_2O_3 layer. Since F- ion based plasma can etch the SiN_x protection layer and the N-polar GaN surface underneath, Al_2O_3 is used as an etch-stop layer during the patterning of SiO_2. Cr is removed with ICP dry etch, followed by the wet-etch of Al_2O_3 in AZ 300 MIF developer.

The *in-situ* grown MOCVD SiN_x is removed with CF_4/O_2-based low-power ICP dry etch. The GaN cap is selectively removed with BCl_3/SF_6-based ICP dry etch developed by [32], which stops on the AlGaN IL. Then, the AlGaN IL is removed, followed by the selective etch of GaN IL, which stops on the AlGaN cap. The two successive (dual) selective etch process will be discussed in detail in Section 3.2. It is important to implement the dual selective etch

[4] Cr is oxidized prior to the deposition of UVN 30 for better adhesion.

process successfully, or else we run the risk of etching through the 10-nm thin GaN channel. This process step is more critical during the gate recess etch.

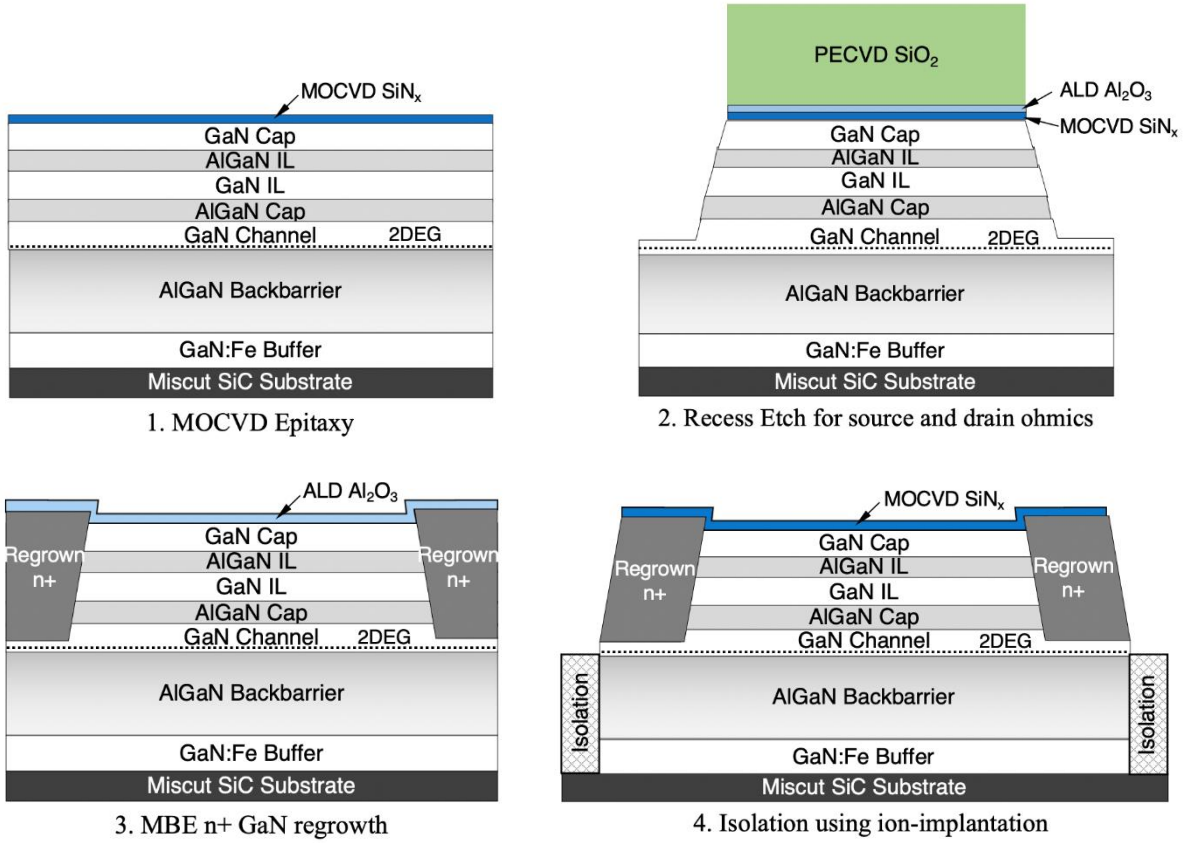

Figure 3.1 Process flow showing the selective area MBE n+ GaN regrowth (for source and drain ohmics) and the isolation of devices.

Following the dual selective etch, the AlGaN cap is removed with BCl_3/Cl_2-based low-power reactive ion etch (RIE). This non-selective etch is timed to remove 5 nm of AlGaN/GaN, and therefore etches part of the GaN channel. 20-nm UID GaN and 30-nm highly doped GaN is grown off the GaN channel by plasma-assisted molecular beam epitaxy (PA-MBE). The polycrystalline GaN does not grow off the vertical sidewalls of the SiO_2 mask; this is ensured by the MBE regrowth conditions and the verticality of the SiO_2 mask. Therefore, the mask can be cleanly removed. The mask is removed in 1:1 HF:HNO_3 solution

in ultrasonic bath. A 20-nm SiO_2 protection layer is then deposited by ALD, which will be removed later in the process.

The next module is the isolation of devices using ion-implantation. The isolation regions are defined by photolithography. Using photoresist (PR) to mask the active region, ALD SiO_2 is dry-etched, and n+ GaN is removed using BCl_3/SF_6 selective dry etch, prior to ion-implantation. After ion-implantation, PR is stripped off, followed by the removal of ALD SiO_2 protection layer. 7-nm SiN_x protection layer is deposited by MOCVD; this protection layer remains in the device access regions after the fabrication process is complete.

Following the deposition of MOCVD SiN_x protection layer, an oxide hard mask is deposited for gate recess. The hard mask consists of 10-nm ALD Al_2O_3 and 225-nm PECVD SiO_2. In the self-aligned process [34], this hard mask remains in-place during the deposition of T-gate, and therefore defines the T-gate foot. The thickness of the hard mask determines the thickness of the T-gate stem (taking into consideration that SiO_2 etches vertically during the BCl_3/SF_6 selective dry etch of GaN). The gate recess dimensions are defined with E-beam lithography using a positive E-beam resist CSAR-62. After exposure and development, SiO_2 is patterned with ICP dry etch. The SiO_2 etch stops in the Al_2O_3 layer, following which Al_2O_3 is wet-etched in developer.

The *ex-situ* MOCVD SiN_x is patterned with CF_4/O_2-based ICP dry etch. To realize the gate-trench, the dual selective etch process is employed. The first selective etch removes the GaN cap and stops on the AlGaN IL. A second mask is deposited over the oxide hard mask (Figure 3.2). The second mask fills in the trench in the oxide hard mask and the GaN cap. The selection of material for second mask and the challenges involved in its patterning and removal will be discussed in Section 3.3. The second mask is patterned using

photolithography to define sections V_{T1} and V_{T2} in the dual-threshold device. Section V_{T2} is masked—whereas the openings in second mask define section V_{T1}. In the single-threshold device, the second mask is removed along the entirety of its gate-width. In the unmasked regions, the AlGaN IL is removed, followed by the selective etch of GaN IL, stopping on the AlGaN cap (Section 3.2). The second mask is subsequently stripped off, following which a high quality MOCVD SiN_x gate dielectric is deposited at 1020ºC.

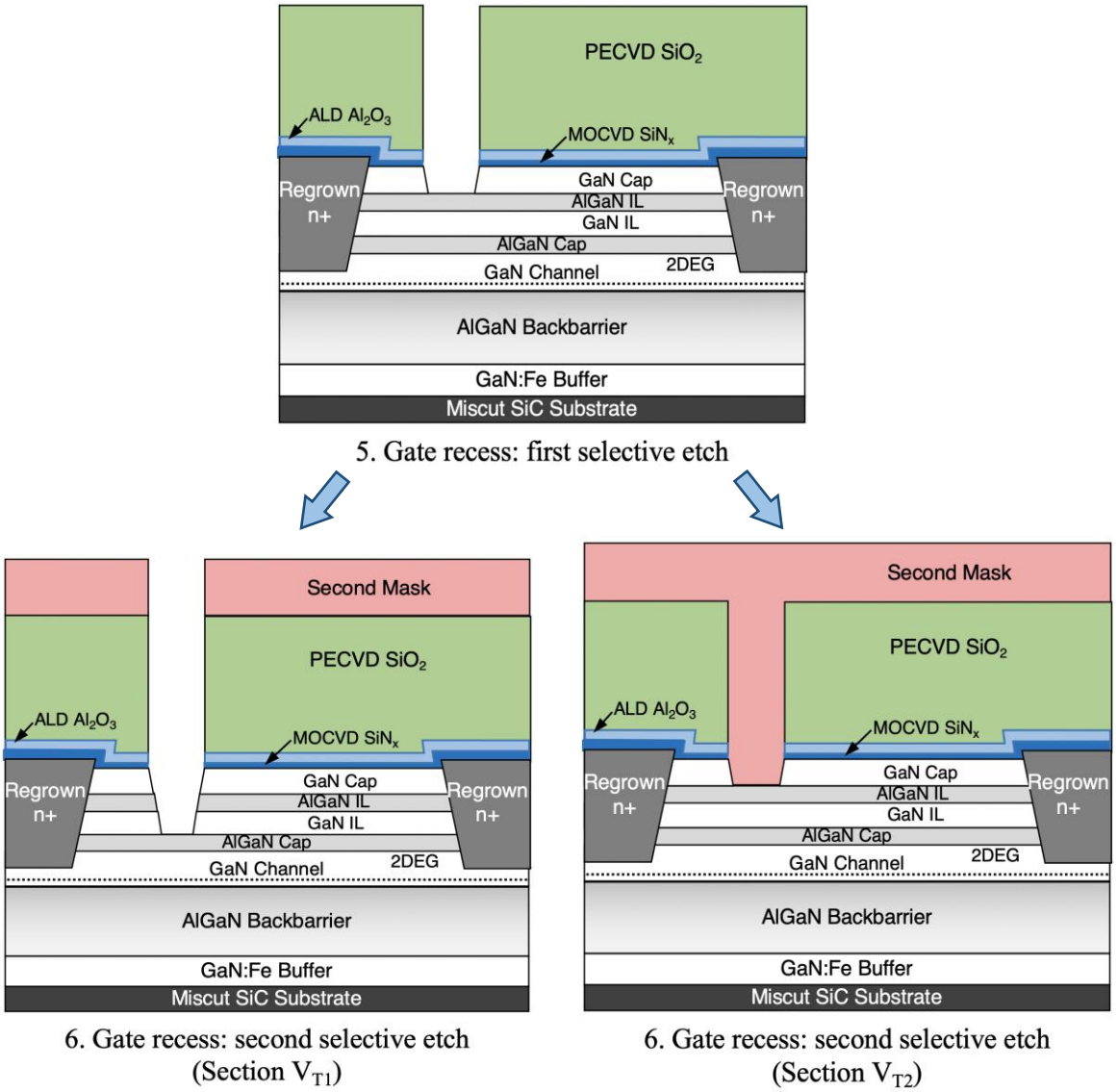

Figure 3.2 Illustration of the gate recess etch—first selective etch, patterning of second mask and second selective etch.

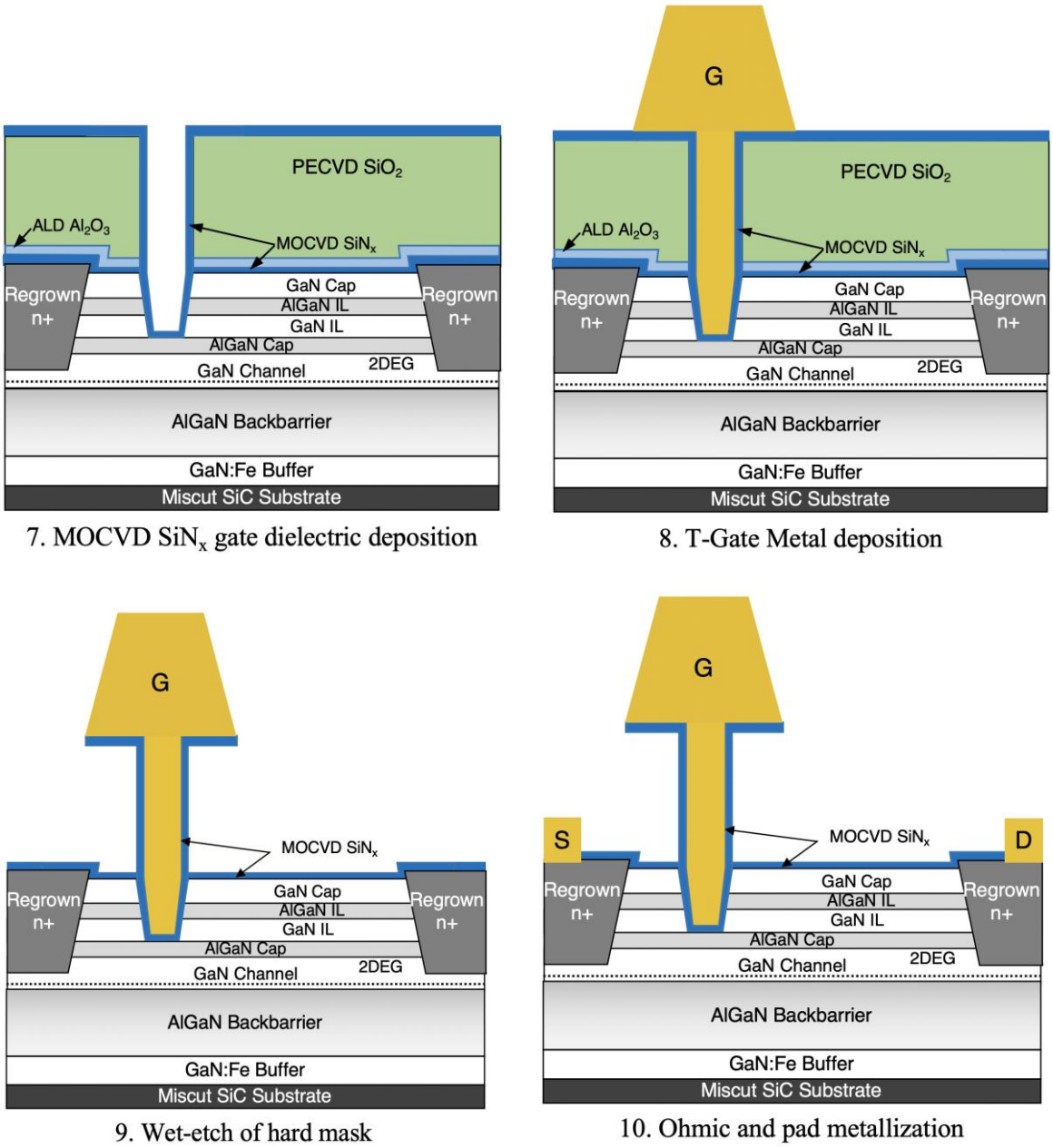

Figure 3.3 Illustration of the final steps of device fabrication—deposition of MOCVD SiN_x gate dielectric; T-gate metallization; wet-etch of hard mask; and ohmics and pad metallization. Only section V_{T1} is shown; same process steps simultaneously apply to section V_{T2}.

The T-gate top dimension is defined with E-beam lithography using UV6 – a positive deep UV photoresist. After exposure and development, the T-gate metal stack comprising of 45-nm Cr and 500-nm Au is deposited using E-beam evaporation. Cr sets the work-function, provides adhesion for the low-resistance Au layer, and is resistant to the diluted buffered hydrofluoric acid (BHF) treatment to etch away the hard mask later. After T-gate metallization, recessed but un-gated regions in test structures (for example, recessed TLM structures) are masked with photoresist to protect the surface during subsequent SiN_x dry etch. SiN_x in the field is removed with CF_4/O_2-based ICP dry etch, followed by the wet-etch of hard mask in 4:1 deionized (DI) H_2O:BHF. The T-gate structures are then examined with SEM.

The device fabrication process completes with the metallization of ohmic contacts and probe pads. Prior to ohmic metal deposition, the SiN_x protection layer is removed with CF_4/O_2-based ICP dry etch, followed by BCl_3/Cl_2 low-power RIE etch and wet etch in 1:1 DI H_2O:HCl [44]. Ti/Au (20 nm/100 nm) is then deposited by E-beam evaporation for ohmic metal contacts. Finally, Ti/Au/Ni (30 nm/650 nm/ 30 nm) is deposited using E-beam evaporation for probe-pads.

3.2 Challenge 1: Dual Selective Etch Process

In the dual-threshold device design, the gate is recessed to two different depths to realize the two threshold voltages – V_{T1} and V_{T2}. As mentioned in Chapter 1, the threshold voltages are defined at the epi-level with AlGaN etch-stop layers – to ensure etch-depth accuracy and process reproducibility. Hence, the process has been developed for two successive selective etch of GaN over AlGaN: *(i)* the selective etch of GaN cap stopping on AlGaN IL and *(ii)* the removal of AlGaN IL, followed by the selective etch of GaN IL stopping on AlGaN cap. As mentioned in Section 3.1, the dual selective etch also appears in the first fabrication module:

the regrowth of n+ GaN for source and drain ohmics. However, this process step is more critical during the gate recess etch.

The first selective etch—using BCl_3/SF_6-based ICP dry etch to remove GaN cap and stop on AlGaN IL [32]—is a standard processing step in the fabrication of N-polar GaN deep-recess HEMTs [34, 33, 45]. However, the removal of AlGaN IL and the successive selective dry etch of GaN IL pose some challenges: it has been previously observed that using non-selective RIE dry etch to remove AlGaN/GaN layers prior to the selective etch of GaN over AlGaN can result in the loss of selectivity; the digital etch of AlGaN IL with UV ozone and HF treatment is incompatible with the oxide hard mask used during the gate recess as well as the source and drain ohmic recess etch. With these considerations, two approaches are explored to remove the AlGaN IL: *(i)* optimization of BCl_3 pre-treatment time, and *(ii)* digital etch of AlGaN in organic acid.

3.2.1 Optimization of BCl_3 Pre-Treatment Time

The selective dry etch begins with BCl_3 pre-treatment to break through the surface oxides [32]. The BCl_3 pre-treatment is normally carried out for 90 s. The efficacy of a prolonged BCl_3 pre-treatment in removing a thin AlGaN IL (2.6-nm $Al_{0.34}Ga_{0.66}N$) was investigated in this study. Samples with N-polar GaN epitaxial structure grown on miscut SiC substrates were used for this experiment. The epitaxial stack consisted of semi-insulating Fe-doped GaN buffer, AlGaN backbarrier, 10-nm GaN channel, 2.6-nm $Al_{0.27}Ga_{0.73}N$ cap, 10-nm GaN IL, 2.6-nm $Al_{0.34}Ga_{0.66}N$ IL, GaN cap and 5-nm SiN_x. The SiN_x protection layer was dry etched, following which the first selective etch was carried out using an oxide hard mask and standard selective dry etch parameters. During the second selective etch, the BCl_3 pre-treatment time was varied for three samples: 2 min for sample A, 3 min for sample B, and 5 min for sample C.

All other etch parameters, including the subsequent BCl_3/SF_6 treatment time, were constant for the three samples. The hard mask was removed in 1:1 $HF:HNO_3$ solution. The etched surface was examined using SEM and etch-depth was measured using atomic force microscope (AFM).

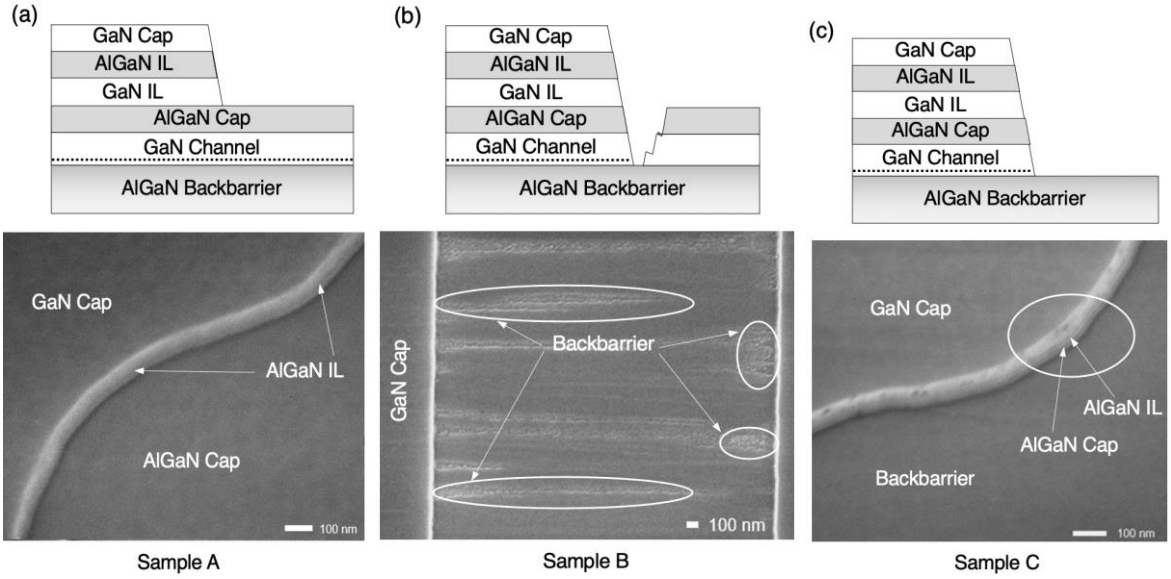

Figure 3.4 The experimental results of optimizing the BCl_3 pre-treatment time to remove AlGaN IL during the second selective etch. The BCl_3 pre-treatment time was varied for three samples: 2 min for sample A, 3 min for sample B, and 5 min for sample C. The SEM image of: **(a)** sample A shows a smooth AlGaN cap surface; **(b)** sample B shows partial etch through the GaN channel; and **(c)** sample C shows a smooth backbarrier surface.

The SEM image of sample A (Figure 3.4 (a)) shows that the AlGaN IL was etched, followed by the selective etch of GaN IL stopping on the AlGaN cap. The AFM profile verified that the second selective etch stopped on the AlGaN cap. Figure 3.4 (b) shows that the sample B etched through the GaN channel in some regions, particularly along the miscut steps, with the etch penetrating deeper near the edge of the masked region. The SEM image of sample C (Figure 3.4 (c)) shows that it etched through the GaN channel stopping at the

AlGaN backbarrier with a smooth surface. The experiment shows that 2 min of BCl_3 pre-treatment is sufficient to etch the AlGaN IL during the second selective etch. However, a longer BCl_3 pre-treatment etches through the GaN channel.

3.2.2 Digital Etch of AlGaN in Organic Acid

In another set of experiments conducted to test the compatibility of N-polar (Al)GaN with a wide range of chemical solvents, B. Romanczyk discovered that N-polar (Al)GaN etches in citric acid resulting in a smooth surface. A premix solution of citric acid monohydrate combined with 1:1 DI water by weight is used for this wet etch. In the digital etch technique, one etch cycle consists of 1 min O_2 plasma treatment, followed by 2 min immersion in citric acid solution. The etch rate is 1 nm/cycle for UID N-polar (Al)GaN, with no surface degradation. The digital etch allows for the accurate control of etch depth to remove thin (Al)GaN layers. Therefore, it is used as the preferred method to remove the AlGaN IL prior to the second selective etch for devices presented in this dissertation.

3.3 Challenge 2: Masking for Second Selective Etch

To realize the gate-trench, the dual selective etch process is employed. An oxide hard mask is used for the first selective etch. Following this, a second mask is deposited over the oxide hard mask, filling the trench in the hard mask and the GaN cap (Figure 3.2). The second mask is patterned using photolithography to define sections V_{T1} and V_{T2}. Section V_{T2} is masked—whereas section V_{T1} is unmasked—during the second selective etch. The single-threshold device is unmasked along the entirety of its gate-width during the second selective etch.

There are important considerations to be taken into account while selecting the material for second mask. First, the etched trench in the GaN cap with the AlGaN IL at its bottom surface is exposed after the first selective etch. The exposed surface should not degrade during the deposition, patterning and removal of second mask. Commonly used metal ion free (MIF) alkaline photoresist developers (based on TMAH) cannot be used in this process; they roughen N-polar (Al)GaN surface. Therefore, alternatives to using photoresist mask are explored in this study. Second, in the self-aligned process, the oxide hard mask used during the gate recess etch defines the foot of T-gate; it must remain in place during the second selective etch and the subsequent removal of second mask, to achieve a constant L_g along the gate-width. This puts a constraint on what material can be used for second mask: for example, SiO_2 or SiN_x dielectric layer—which can be deposited, patterned and removed without degrading the N-polar (Al)GaN surface—is incompatible with the self-aligned process.

3.3.1 Germanium/ALD SiO_2 Mask

Germanium (Ge) is one of the materials explored for second mask. Ge can be wet-etched in hydrogen peroxide (H_2O_2), which does not etch or roughen N-polar GaN. To test the Ge/SiO_2 second mask, 200-nm Ge was deposited with E-beam evaporation after the first selective etch. Following which 25-nm ALD SiO_2 was deposited to pattern Ge. The thickness of SiO_2 was chosen so that it is almost completely etched in the subsequent BCl_3/SF_6 selective dry etch. SiO_2 was patterned with a photoresist mask in 25:1 DI H_2O:BHF solution. The photoresist mask was stripped off. Using SiO_2 mask, Ge was wet-etched in H_2O_2 with a significant over-etch (150%); this was to ensure that the unmasked Ge etched through the trench in the oxide hard mask and GaN cap. With Ge/SiO_2 second mask, AlGaN IL was removed and second selective etch was carried out. 24-nm ALD SiO_2 etched during the

selective dry etch. Ge was removed in H_2O_2; few nanometers of remaining SiO_2 was expected to lift off during Ge removal.

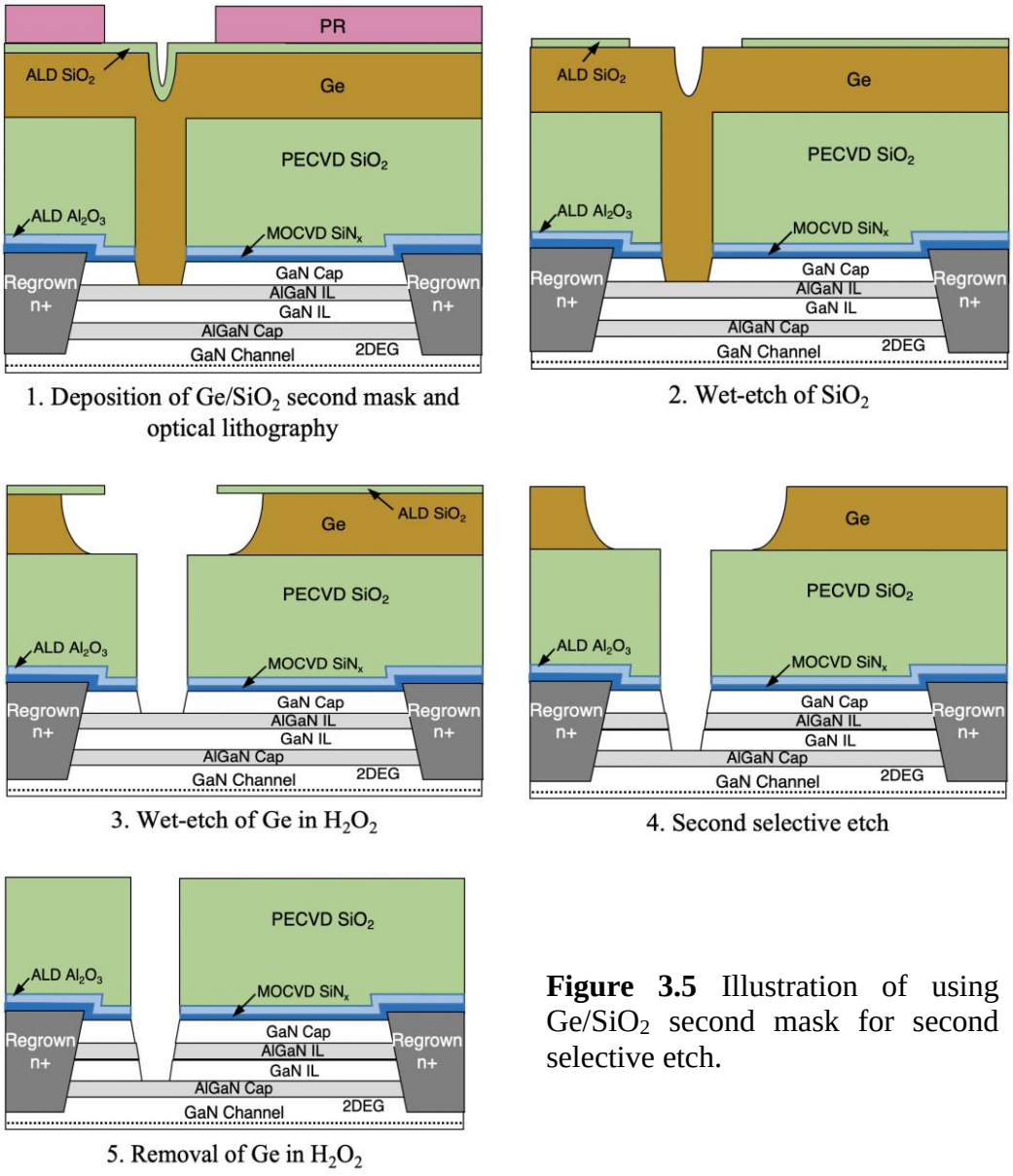

Figure 3.5 Illustration of using Ge/SiO_2 second mask for second selective etch.

The SEM image taken after Ge/SiO_2 second mask patterning (Figure 3.5 (a)) – prior to the second selective etch – shows that the Ge mask was severely undercut, with the openings in the second mask merged together, and the over-hanging ALD SiO_2 possibly collapsed. After the second selective etch and the removal of Ge/SiO_2 second mask, the SEM image (Figure 3.5 (b)) shows that the oxide hard mask had retreated laterally exposing the GaN cap surface. Only single-threshold devices yielded in this fabrication run.

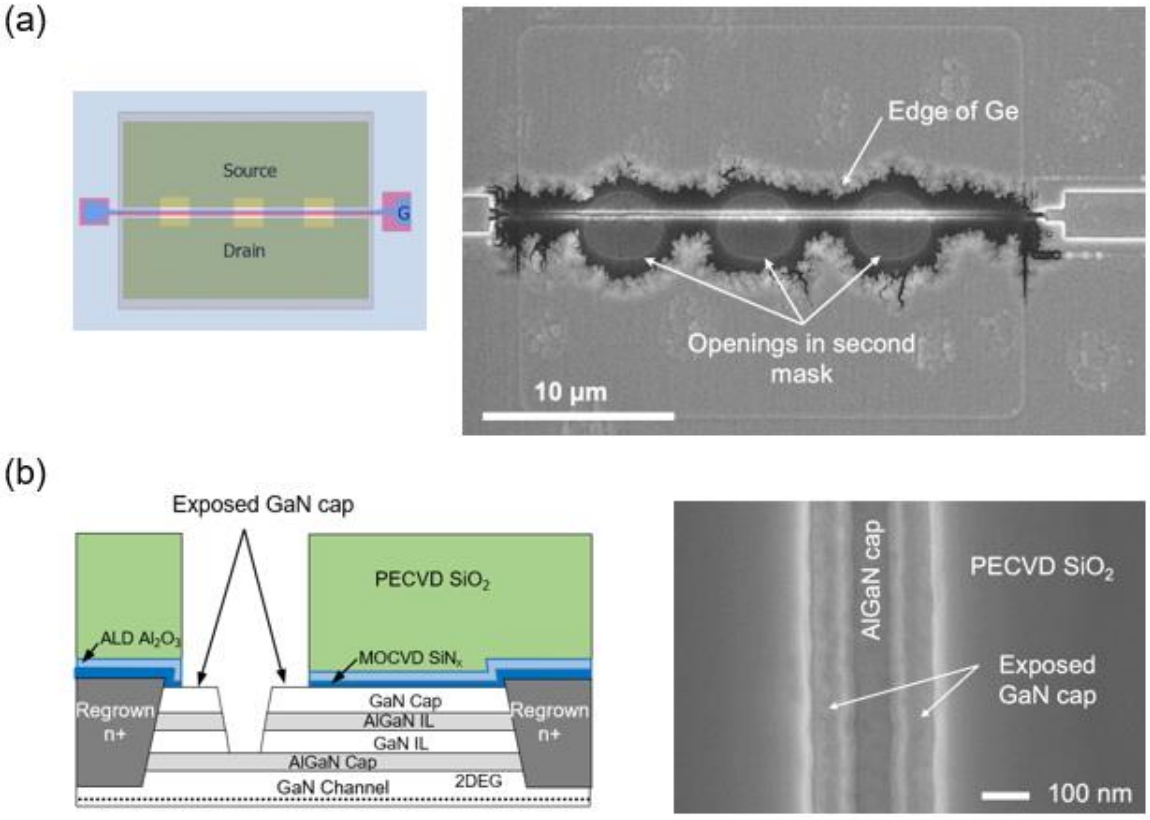

Figure 3.6 (a) Schematics of the designed top view of the device showing openings in the second mask and the SEM image taken after the patterning of Ge/SiO_2 mask. The Ge was severely undercut and the openings in the second mask merged together. **(b)** Schematics and the SEM image showing the oxide hard mask retreated laterally after the second selective etch.

3.3.2 PMMA/Chromium Mask

In the next fabrication run, poly(methyl methacrylate) (PMMA) – a polymer based E-beam resist – was employed for second mask. PMMA utilizes an inert solvent developer – a mixture of methyl isobutyl ketone (MIBK) and isopropanol (IPA), which is compatible with N-polar GaN. After the first selective etch, PMMA 950K-A8 was spin-coated at 4krpm, resulting in 900 nm thick resist. 30-nm Cr was thermally evaporated to serve as a hard mask during subsequent deep ultraviolet (DUV) flood exposure and development of PMMA. Thermal evaporation is used instead of E-beam evaporation, which risks PMMA exposure to electron radiation. Cr also serves as a hard mask during second selective etch as PMMA is known to have poor resistance to plasma etch.

The second mask was patterned by photolithography. Using a photoresist mask, Cr was wet-etched in chromium etchant. This was followed by a 20-min DUV flood exposure. The photoresist was then stripped in AZ 300 MIF developer. After stripping photoresist, PMMA was developed in 1:1 MIBK:IPA mixture for 60 s, followed by rinse in 1:3 MIBK:IPA for 20 s and DI water for 1 min to prevent scumming. The sample was examined under microscope after PMMA development. Although cracks were observed in Cr film, the PMMA/Cr mask held up effectively during the subsequent second selective etch. Using PMMA/Cr mask, AlGaN IL was removed using the aforementioned digital etch technique (Section 3.2.2) and the second selective etch was carried out. Finally, PMMA was stripped in photoresist stripper – AZ NMP at 80ºC, with Cr lifting off during the stripping of PMMA.

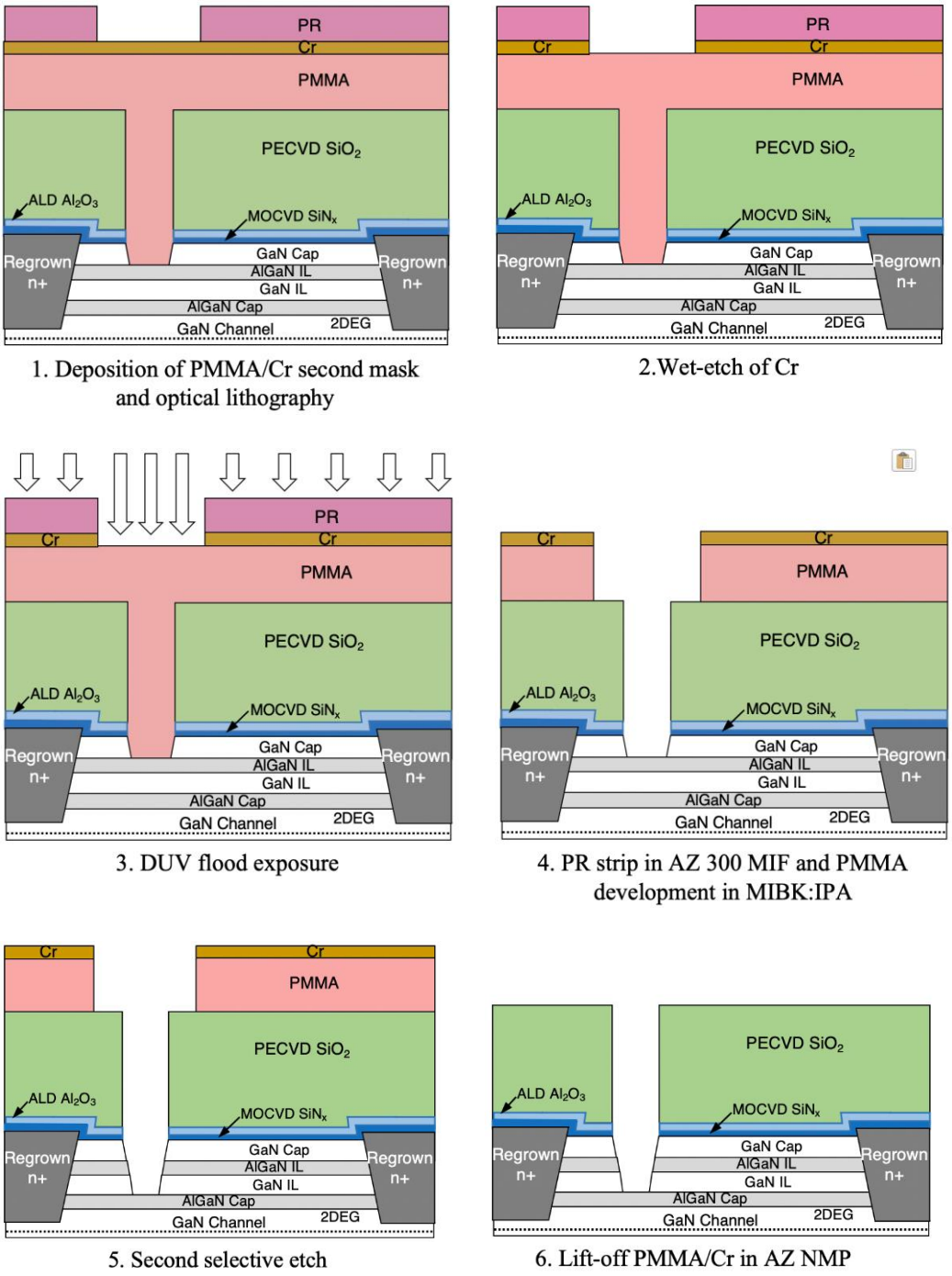

Figure 3.7 Illustration of using PMMA/Cr second mask for second selective etch.

The SEM image (Figure 3.8) taken after the second selective etch and PMMA removal shows the partitioning of sections – V_{T1} and V_{T2} in a CV test structure. The large area structure is shown here for visual clarity; well-defined sections – V_{T1} and V_{T2} are also achieved at gate--length dimensions. Both single- and dual- threshold devices yielded successfully in this run.

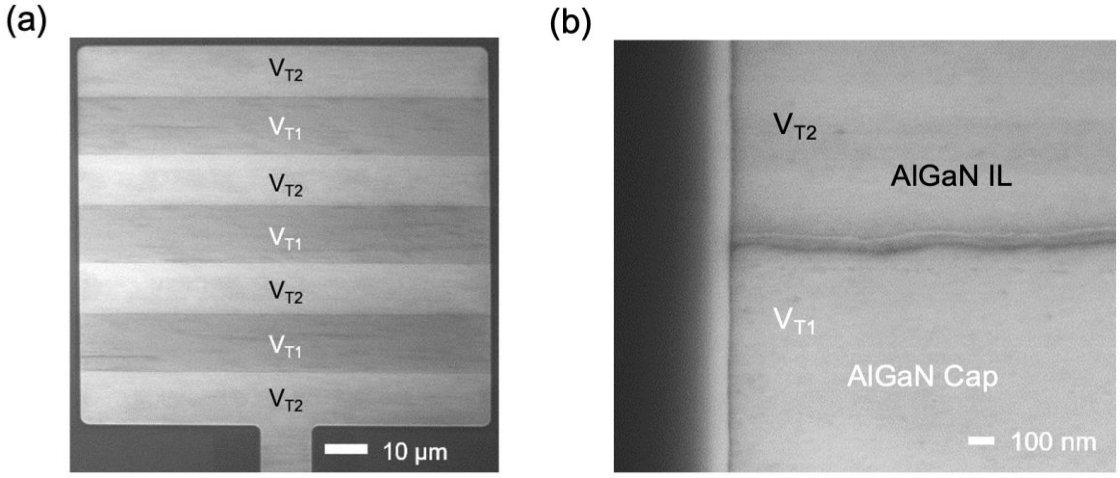

Figure 3.8 (a) SEM image of a CV test structure showing well-defined partitioning of sections V_{T1} and V_{T2} after second selective etch. **(b)** SEM image of the same structure taken at higher resolution. Figure © [2020] IEEE **[46]**.

Chapter 4. Device Results and Analysis

This chapter presents the device results and comparison between single- and dual- threshold devices. The DC and pulsed I-V, RF small-signal and mm-wave linearity characteristics are examined. Unless stated otherwise, all measurements are taken on devices with 60-nm L_g, 85-nm L_{gs}, 315-nm L_{gd}, 2 x 25 µm W_G and coplanar waveguide probe pads.

4.1 Single-Threshold Device Results

This section presents the single-threshold device results. The device structure is shown in Figure 4.1. In the access regions, the device is capped with 10-nm GaN IL and 2.6-nm AlGaN IL (without GaN cap). A 20-nm thin PECVD SiN_x passivation was applied after the deposition of probe pads. The choice of thin passivation has been made to control RF dispersion while minimizing additional parasitic capacitances.

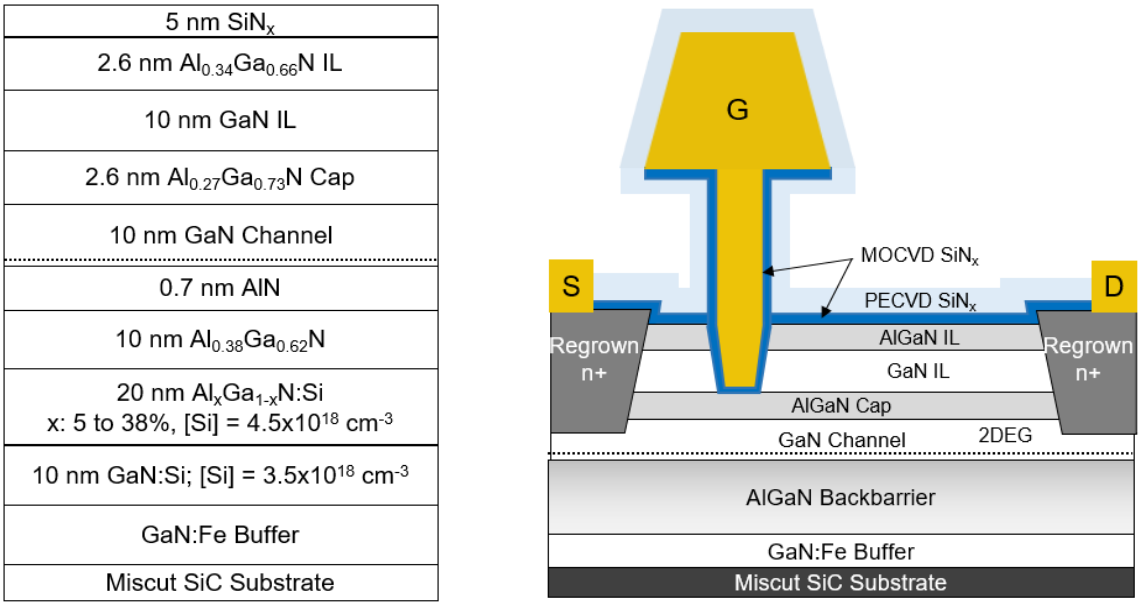

Figure 4.1 MOCVD epitaxy and the single-threshold device structure.

4.1.1 DC I-V Characterization

The DC characteristics of a single-threshold device is shown in Figure 4.2. The device demonstrates a maximum extrinsic transconductance (g_m) of 460 mS/mm peaking at V_{GS} of -4.1V. From the output characteristics in Figure 4.2 (b), we observe a maximum saturation current density of 1.63 A/mm at V_{DS} of 5V. The R_{on} is 0.47 Ω-mm. The gate leakage current density is measured to be 3.3×10^{-5} A/mm at V_{GS} of -6V and V_{DS} of 5V. The C-V characteristics of a capacitor with gate recessed to the AlGaN cap is shown in Figure 4.3. The 2-DEG sheet charge density (n_s) — calculated by integrating capacitance over V_{GS} — is 1.25×10^{13} cm^{-2} at V_{GS} of 0V.

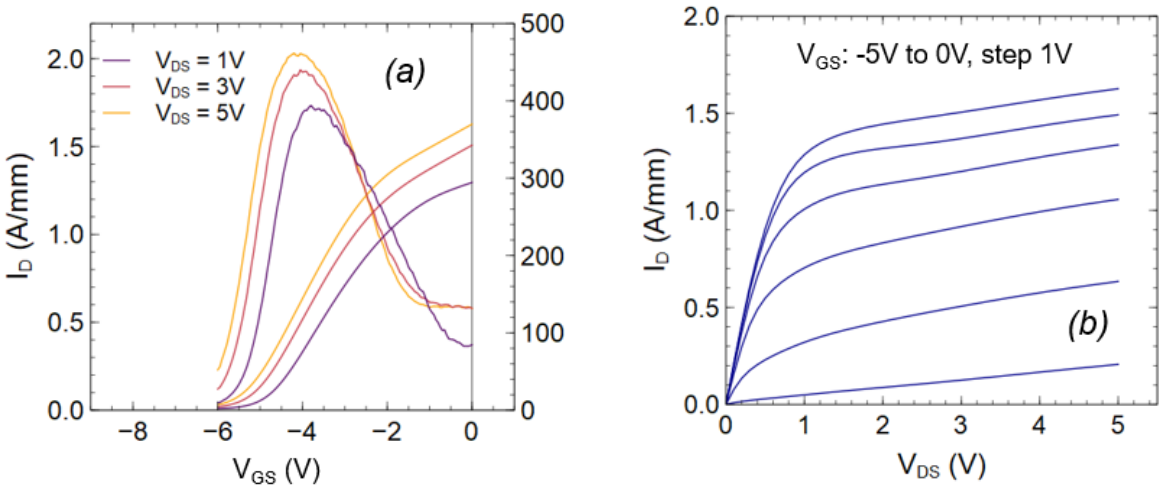

Figure 4.2 DC-IV characteristics of a single-threshold device. **(a)** Transfer characteristics showing the input I_D and g_m profiles. The peak g_m is 460 mS/mm at V_{GS} of -4.1V. **(b)** Output characteristics of the device. We observe a maximum I_D of 1.63 A/mm at V_{DS} of 5V and V_{GS} of 0V.

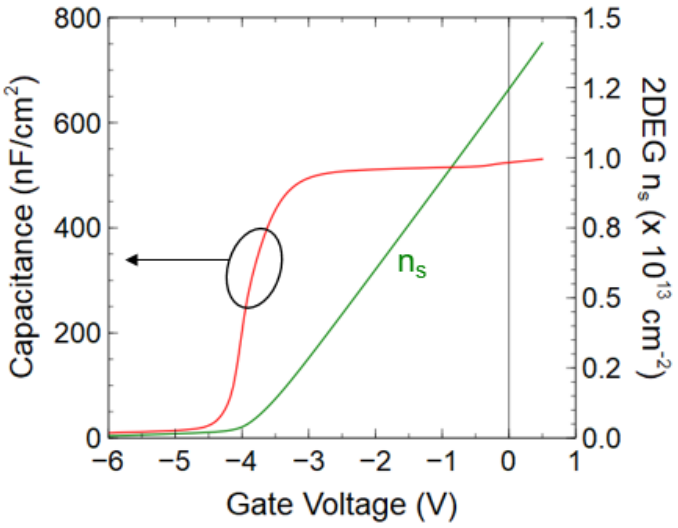

Figure 4.3 100 kHz C-V characteristics of a capacitor—with gate recessed to the AlGaN cap. The square capacitor has a length of 100 µm. The 2-DEG sheet charge density (n_s) is calculated to be 1.25 x 10^{13} cm^{-2} at V_{GS} of 0V.

4.1.2 Pulsed I-V Characterization

The pulsed I-V characteristics is measured with AMCAD AM3200 PIV system. The gate pulse-width is 800 ns, and the drain pulse-width is 600 ns inset within the gate pulse. The measurement window of 200 ns is chosen such that the switching current transients—arising from the pulsed waveforms—fall outside the measurement window. Figure 4.4 (a) shows the transfer characteristics measured at a quiescent drain voltage ($V_{DS,Q}$) of 0V, and quiescent gate voltage ($V_{GS,Q}$) varied from 0V to -8V. The pulsed drain voltage ($V_{DS,P}$) is kept at 5V and the pulsed gate voltage ($V_{GS,P}$) is swept from -6V to 0V. We observe that the threshold voltage (V_T) shifts negative from the cold bias condition ($V_{GS,Q}$; $V_{DS,Q}$) of (0V; 0V) with decreasing $V_{GS,Q}$. The shift in V_T is most pronounced (600 mV) between $V_{GS,Q}$ of 0V and -1V. Beyond $V_{GS,Q}$ < -5V, additional shift in V_T is negligible. This behavior indicates that there are traps in the region underneath the gate. In a standard N-polar GaN MIS-HEMT, traps under the gate associated with the SiN_x gate dielectric surface have been reported by [34]. The

reported solution is using O_2 plasma descum and buffered HF dip prior to the deposition of gate metal. This procedure has been adopted in this work as well. However, compared to a standard N-polar GaN MIS-HEMT, the gate-trench of the single threshold device in this work has witnessed more fabrication steps (the deposition, etch and removal of second mask); this could have introduced additional traps not seen in [34]. This negative shift in threshold has been taken into account when analyzing the g_m derivatives and choosing the quiescent bias condition for two-tone load-pull measurements.

Figure 4.4 (b) shows the output characteristics with $V_{GS,Q}$ = -6V, and drain stressed from 0V to 9V. The pulsed gate voltage ($V_{GS,P}$) is 0V. For low quiescent drain bias, we observe an increase in pulsed drain current compared to the DC measurement. This phenomena termed as "*anti-dispersion*" has been previously observed in N-polar GaN MIS-HEMTs [34]. For higher drain bias, a small amount of knee walk-out is observed. The overall deviation from the DC output characteristics at the knee is <10%.

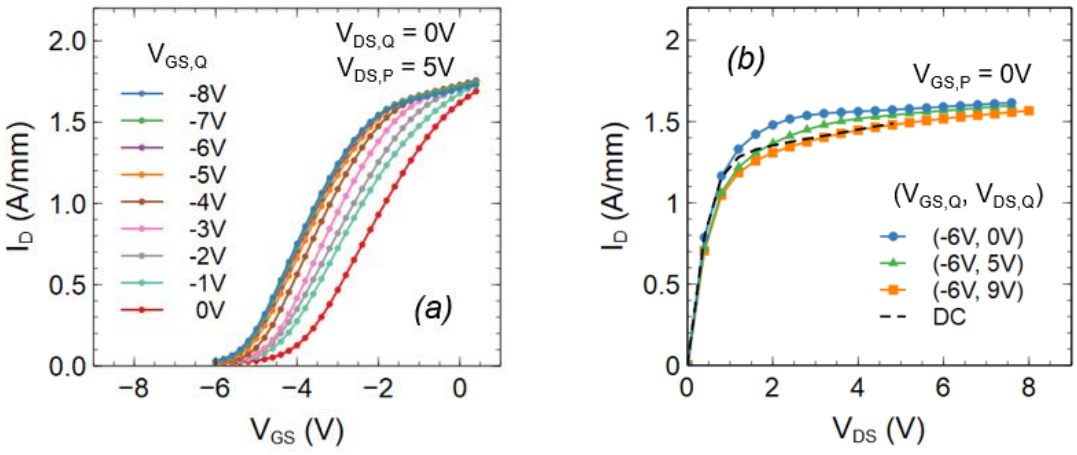

Figure 4.4 Pulsed I-V characteristics. **(a)** Transfer characteristics measured at a quiescent drain voltage ($V_{DS,Q}$) of 0V, and quiescent gate voltage ($V_{GS,Q}$) varied from 0V to -8V. The threshold voltage (V_T) shifts negative from the cold bias condition ($V_{GS,Q}$; $V_{DS,Q}$) of (0V; 0V) with decreasing $V_{GS,Q}$. **(b)** Output characteristics with $V_{GS,Q}$ = -6V, and drain stressed from 0V to 9V.

4.1.3 G_m and its Derivatives

The g_m derivatives are analyzed with pulsed measurements taken at a quiescent gate and drain bias ($V_{GS,Q}$; $V_{DS,Q}$) of (-6V; 7V) to observe the relevant I-V characteristics for RF measurements. In the transfer curve (Figure 4.5 (a)), the pulsed gate voltage ($V_{GS,P}$) has been swept from -6V to 0V, while pulsed drain voltage ($V_{DS,P}$) is kept at 7V. We observe a threshold voltage of -5.24V and a peak g_m of 530 mS/mm at $V_{GS,P}$ of -4.3V. Figure 4.5 (b) shows g_m and its derivatives (g_{m2}, g_{m3}). Note that g_{m3} crosses zero at $V_{GS,P}$ = -5.18V, where the device is turning on. As explained in Chapter 1, this g_{m3} zero-crossing point is where we expect a high linear response and a peak in the OIP3 and OIP3/P_{DC} linearity metric.

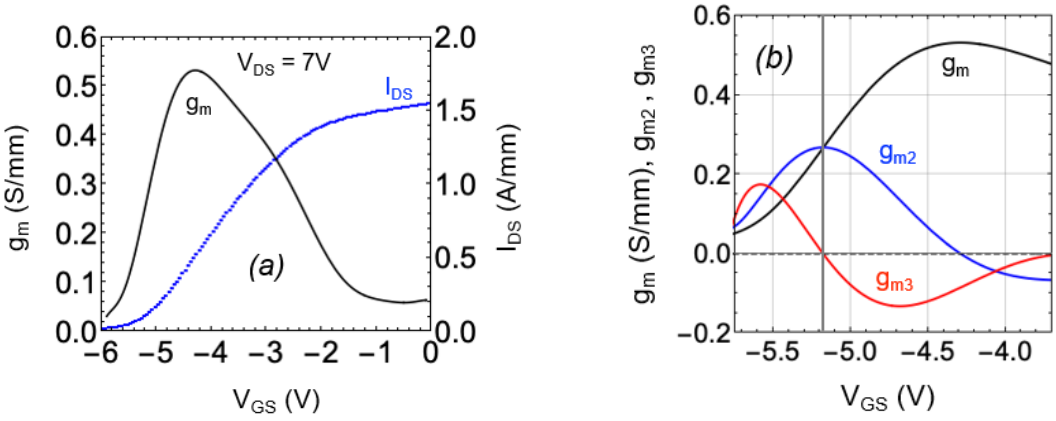

Figure 4.5 (a) Transfer characteristics measured at a quiescent gate and drain bias ($V_{GS,Q}$; $V_{DS,Q}$) of (-6V; 7V). **(b)** Transconductance (g_m) and second and third I_D (V_{GS}) derivatives (g_{m2}, g_{m3}). The g_{m3} crosses zero at device turn-on (V_{GS} = -5.18V). This is where we expect a high linear response and a peak in the OIP3 and OIP3/P_{DC} linearity metric. Figure © [2020] IEEE **[47]**.

4.1.4 Small-Signal Performance

The S-parameters were measured from 0.25 to 67 GHz with GSG probes calibrated by 2-port line-reflect-reflect-match (LRRM) method using an impedance standard substrate.

On-wafer open and short structures were measured for de-embedding probe pads. The de-embedded f_T and f_{max} contour plots—extrapolated using a -20 dB/decade slope from short--circuit current gain $|h_{21}|^2$ and Mason's unilateral gain (U) respectively—are shown in the I-V plane in Figure 4.6. The current gain, unilateral gain and maximum stable/available gain (MSG/MAG) for peak f_T and f_{max} conditions are plotted in Figure 4.7. The device demonstrates a peak f_T of 138 GHz at a quiescent gate and drain bias ($V_{GS,Q}$; $V_{DS,Q}$) of (-4V; 5V), and a peak f_{max} of 287 GHz at ($V_{GS,Q}$; $V_{DS,Q}$) of (-4.25V; 9V). Figure 4.8 shows the maximum stable gain (MSG) at 30 GHz plotted against gate-bias. At 30 GHz, the MSG is 13.8 dB at the bias condition for peak f_T and 15 dB for peak f_{max} condition.

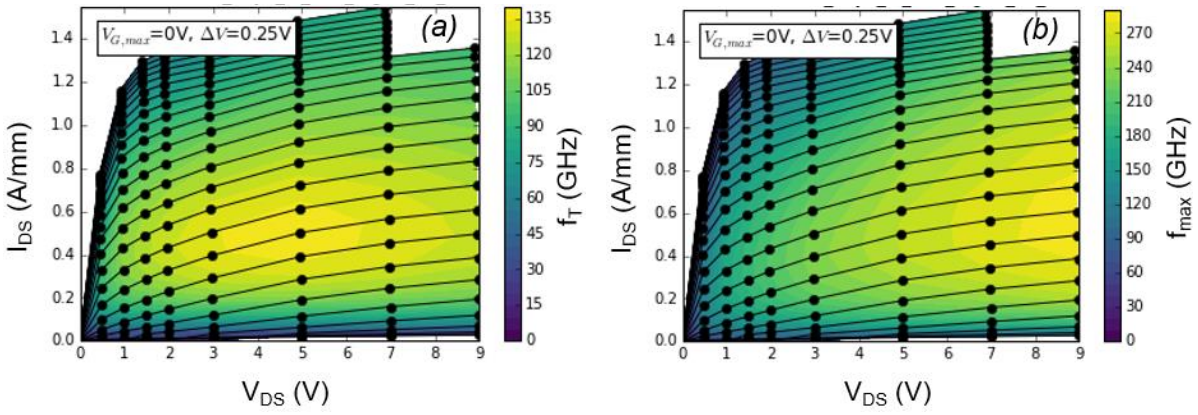

Figure 4.6 De-embedded f_T and f_{max} contour plots shown in the I-V plane for the single-threshold device with 60-nm L_g, 85-nm L_{gs}, 315-nm L_{gd}.

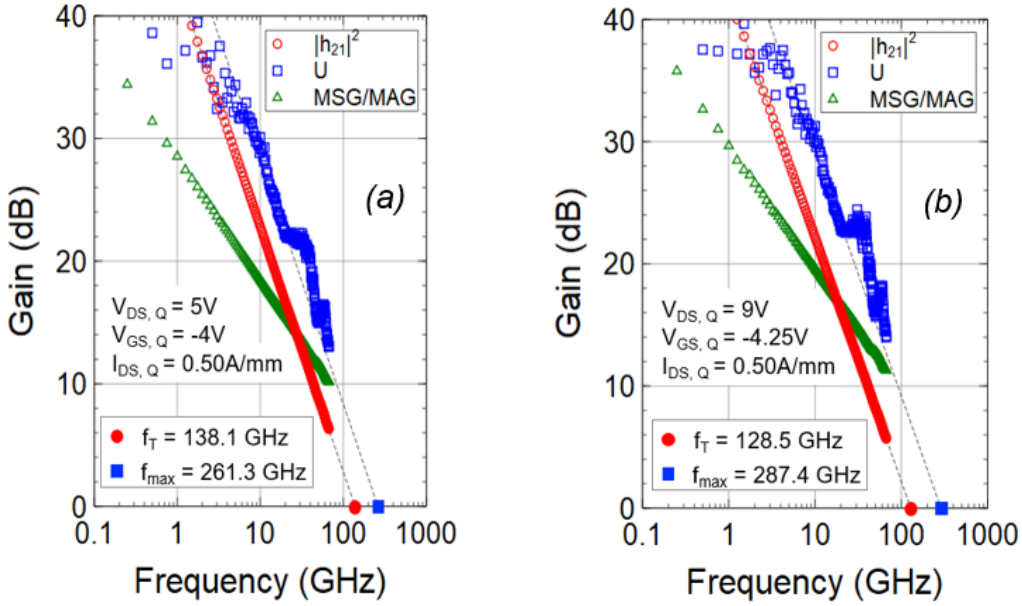

Figure 4.7 The current gain, unilateral gain and maximum stable/available gain (MSG/MAG) for **(a)** peak f_T Figure © [2020] IEEE **[47]** and **(b)** peak f_{max} conditions. The device demonstrates a peak f_T of 138 GHz at ($V_{GS,Q}$; $V_{DS,Q}$) of (-4V; 5V), and a peak f_{max} of 287 GHz at ($V_{GS,Q}$; $V_{DS,Q}$) of (-4.25V; 9V).

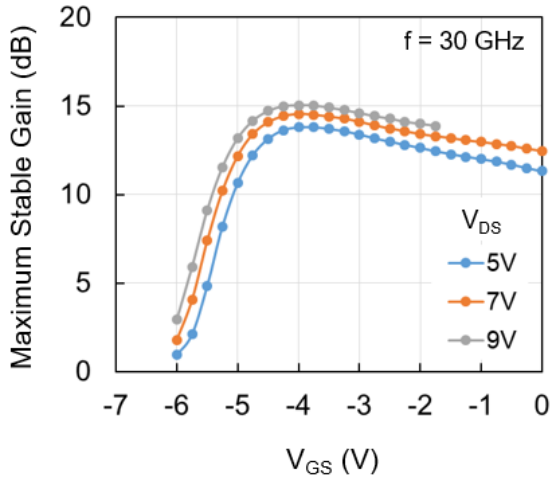

Figure 4.8 The maximum stable gain (MSG) at 30 GHz plotted against gate-bias. The MSG is 13.8 dB at the bias condition for peak f_T and 15 dB for peak f_{max} condition.

4.1.5 Two-Tone Load-Pull Characterization at 30 GHz

The two-tone measurement was performed with a vector receiver load-pull system at Maury Microwave. A vector network analyzer (Keysight PNA-X) supplied the two tones centered at 30 GHz with a tone-spacing of 1MHz[5]. Though linearity characterization with a tone-spacing of 10 MHz has been widely reported in literature [14, 13] we have chosen to conduct our measurements at a smaller tone-spacing. In passive load-pull, the tuning element is at an electrically large distance away from the device. Therefore, different impedances are presented to the device at the two input tones—an effect that increases with tone-spacing. In order to reduce this effect which can influence the measured OIP3, we have chosen a tone-spacing of 1 MHz instead of 10 MHz. The two tones were amplified separately and then combined externally to reduce distortion introduced by the instrumentation. Both source and load tuners were used in this measurement. The system linearity was validated with a low-loss thru line, prior to linearity characterization of devices.

In order to determine the bias condition for the two-tone power sweep, we initially performed input-bias sweeps. The source impedance (Γ_S) was tuned for maximum transducer gain (G_T), whereas the load impedance (Γ_L) was tuned for a trade-off between maximum OIP3 and maximum G_T. Figure 4.9 shows the input-bias sweeps, taken at total available input power ($P_{in,available}$) of -9 dBm. The red curve is the initial coarse sweep and the blue curve is taken with finer V_{GS} steps to capture the OIP3/P_{DC} peak. The load impedance (Γ_L) was further tuned between the coarse and fine sweeps. The OIP3/P_{DC} is sensitive to load impedance. Therefore, the data-points in fine sweep (blue curve) do not overlap with the data points in coarse sweep

[5] The two-tone load-pull measurements at 30 GHz were performed by Dr. Matthew Guidry.

(red curve) at V_{GS} of -5V. Nevertheless, in bias sweeps, we are looking for the location and not the magnitude of the OIP3/P_{DC} peak. We observe a sharp, narrow peak of OIP3/P_{DC} versus gate bias (V_{GS}) at V_{GS} = -5.1V; which is consistent with the g_{m3} zero-crossing point in Figure 4.5 (b). The fact that OIP3/P_{DC} peaks over a limited range of gate-bias means that linearity is sensitive to bias. Generally, all transistors exhibit a g_{m3} zero-crossing point and a corresponding OIP3/P_{DC} peak at the device turn-on point.

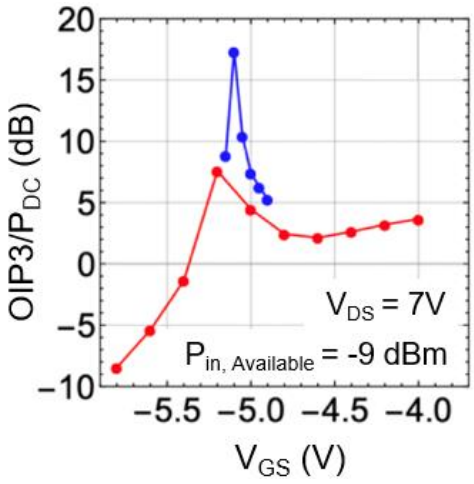

Figure 4.9 Two-tone load-pull input-bias sweep at 30 GHz with a tone-spacing of 1MHz. The red curve is the initial coarse sweep and the blue curve is taken with finer V_{GS} steps to capture the OIP3/P_{DC} peak. OIP3/P_{DC} peaks at V_{GS} = -5.1V, consistent with g_{m3} zero-crossing. At this OIP3/P_{DC} peak, linearity is characterized by means of a two-tone input-power sweep. Figure © [2020] IEEE **[47]**.

At this OIP3/P_{DC} peak, linearity is characterized by means of a two-tone input-power sweep shown in Figure 4.10. The device is biased at $V_{GS,Q}$ of -5.125V, $I_{D,Q}$ of 135 mA/mm (deep class AB), $V_{DS,Q}$ of 7V and Γ_S; Γ_L of $0.66\angle 52°$; $0.65\angle 53°$. The results in Figure 4.10 (a) show the total output power in the fundamental tones (P_{out}), the Upper (Hi) and Lower (Lo) intermodulation products ($P_{I3,hi}$, $P_{I3,lo}$), and the corresponding OIP3. $P_{I3,hi}$ and $P_{I3,lo}$ closely follow the line with slope 3:1 for low input powers, showing the dominant response of the

third-order intermodulation distortion products (IM3). We observe the generation of low IM3, with C/IM3 better than 50 dBc for input powers less than -5 dBm (Figure 4.10 (b)). The device simultaneously exhibits a maximum OIP3 of 32 dBm and a gain (G_T) of 12.7 dB at $P_{in,available}$ of -12.1 dBm (Figure 4.10 (a)). We observe a maximum OIP3/P_{DC} of 15 dB (Figure 4.10 (b)), which is an excellent linearity performance at 30 GHz [47] © [2020] IEEE.

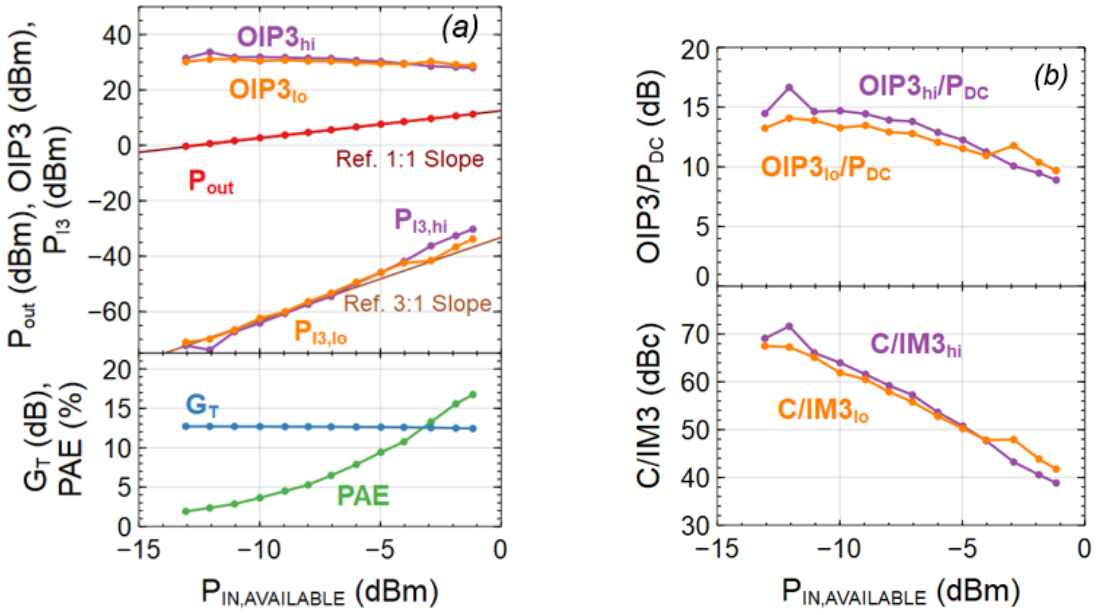

Figure 4.10 Two-tone load-pull input-power sweep at 30 GHz with tone spacing of 1MHz. **(a)** Total output power in the fundamental tones (P_{out}), Upper (Hi) and Lower (Lo) intermodulation products ($P_{I3,hi}$, $P_{I3,lo}$), and corresponding OIP3 are shown. The device simultaneously exhibits a maximum OIP3 of 32 dBm and G_T of 12.7 dB. **(b)** Linearity is reported in two different metrics. Carrier power to IM3 ratio (C/IM3) is better than 50 dBc for input powers less than -5 dBm. We note a maximum OIP3/P_{DC} of 15 dB. Figure © [2020] IEEE **[47]**.

4.2 Dual-Threshold Device Results

This section presents the dual-threshold (dual-V_T) device results. The device comprises of segments of two different threshold voltages – V_{T1} and V_{T2}, and 33% of the entire gate-width

is designed to be section V_{T1}. To better understand the dual-V_T device characteristics, we evaluate the results of two other devices: *(i)* all-V_{T1} device having threshold voltage V_{T1} along the entirety of its gate-width—essentially the single-threshold device discussed in Section 4.1; and *(ii)* all-V_{T2} device having threshold voltage V_{T2} along the entirety of its gate-width.

4.2.1 DC I-V Characterization

Figure 4.11 (a) shows the DC transfer characteristics of the dual-V_T device for various V_{DS} values. We observe that as V_{GS} increases, the g_m rises, plateaus and then peaks, before finally rolling-off. At a V_{DS} of 5V, the device demonstrates a g_m plateau of 250 mS/mm in the V_{GS} range -6.9V to -5.8V, and a peak of 345 mS/mm at V_{GS} of -4.4V. The gate leakage current density is measured to be 6.9 x 10^{-5} A/mm at V_{GS} of -8V and V_{DS} of 5V, which is on the same order of magnitude as the single-threshold device (Section 4.1.1). From the output characteristics in Figure 4.11 (b), we observe a maximum current density of 1.93 A/mm at V_{DS} of 5V. The R_{on} is 0.46 Ω-mm.

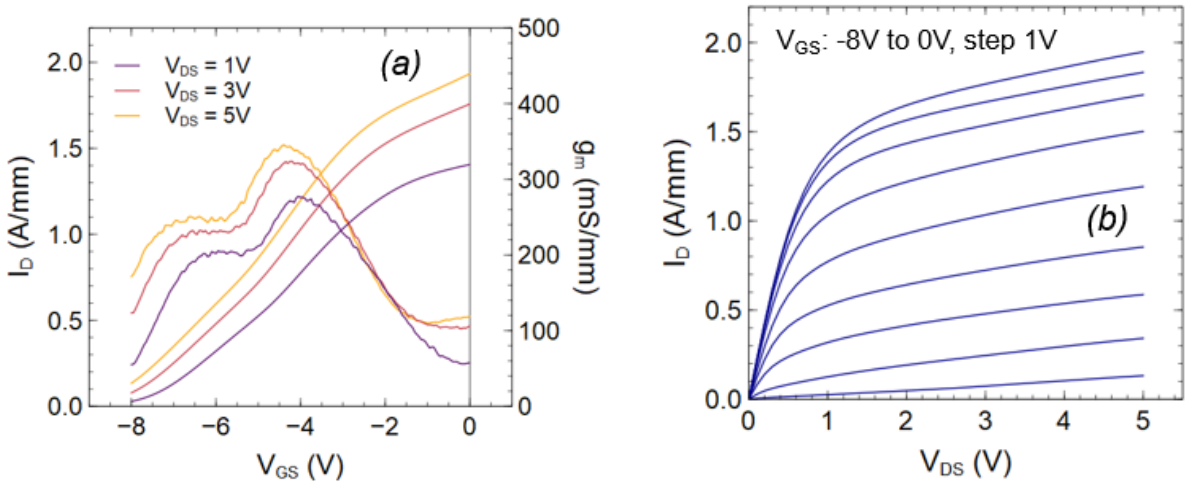

Figure 4.11 DC-IV characteristics of a dual-threshold device. **(a)** Transfer characteristics showing the input I_D and g_m profiles. At a V_{DS} of 5V, the device demonstrates a g_m plateau of 250 mS/mm in the V_{GS} range -6.9V to -5.8V, and a g_m peak of 345 mS/mm at V_{GS} of -4.4V. **(b)** Output characteristics of the device. We observe a maximum I_D of 1.93 A/mm at V_{DS} of 5V and V_{GS} of 0V.

To understand the behavior of the dual-V_T device, the DC transfer characteristics of all-V_{T1} (green curve), all-V_{T2} (blue curve), and dual-V_T (magenta curve) devices—measured at V_{DS} of 5V—are plotted in Figure 4.12. V_{T2} is a more negative threshold voltage than V_{T1} as the gate is placed further away from the channel. The threshold voltage difference between V_{T1} and V_{T2} ($V_{T,diff}$) is 3.45V. The I_D-V_{GS} curve of the dual-V_T device lies in-between those of all-V_{T1} and all-V_{T2} devices (Figure 4.12 (a)); this is expected as the dual-V_T device is a parallel combination of sections V_{T1} and V_{T2}. Evaluating the data of all-V_{T1} and all-V_{T2} devices, we observe that 38% of the total gate-width of the dual-V_T device is composed of section V_{T1}; this is larger than the designed value of 33%. As mentioned in Chapter 3, the realization of the gate-trench utilizes a second mask (PMMA/Cr). The openings in the second mask define section V_{T1}. The O_2 plasma and citric acid treatment during the removal of AlGaN IL may oxidize and possibly etch PMMA, widening the openings in the mask—and therefore section V_{T1}.

The g_m characteristics of the three devices—measured at V_{DS} of 5V—are shown in Figure 4.12 (b). As the gate-bias increases, the g_m profile of the all-V_{T1} device (green curve) rises sharply, peaks to 460 mS/mm at V_{GS} of -4.1V and then rolls-off. The all-V_{T2} device has a lower and broader g_m peak of 330 mS/mm at V_{GS} of -6.9V. Beyond the g_m peak, the g_m profile broadens out, rolling-off slowly at first and steeply later. While it is expected for the all-V_{T2} device to have a lower g_m peak and a broader g_m profile, we have verified with C-V measurements (Figure 4.13) that there is no parallel channel—between GaN IL and AlGaN cap—underneath the gate. From the g_m-V_{GS} plot of the dual-V_T device (magenta curve), we observe that as V_{GS} increases, the g_m rises, plateaus and then peaks, before finally rolling-off. At a V_{DS} of 5V, the device demonstrates a g_m plateau of 250 mS/mm in the V_{GS} range -6.9V

to -5.8V. The g_m plateau occurs in the region where the falling g_m of section V_{T2} is compensated by the rising g_m of section V_{T1}.

The C-V characteristics of all-V_{T1}, all-V_{T2} and dual-V_T structures are shown in Figure 4.13. As the gate is pinched-off—with increasing negative gate bias—in the dual-V_T structure, the 2-DEG charge in section V_{T1} fully depletes first, followed by the full depletion of charge in section V_{T2}; this phenomena gives rise to the double humped C-V profile.

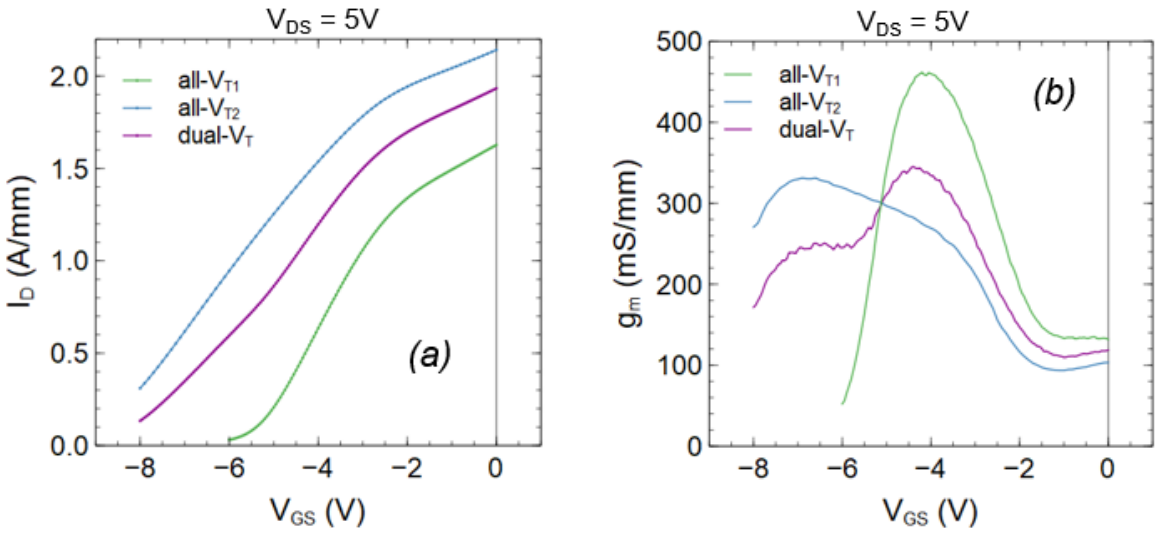

Figure 4.12 DC-IV characteristics three devices: of all-V_{T1} (green curve), all-V_{T2} (blue curve) and dual-VT (magenta curve). **(a)** The transfer ID characteristics showing that dual-V_T is a parallel combination of section V_{T1} and V_{T2}. **(b)** The respective gm profiles. At a V_{DS} of 5V, the dual-V_T device demonstrates a g_m plateau of 250 mS/mm, which occurs in the region where the falling g_m of section V_{T2} is compensated by the rising g_m of section V_{T1}.

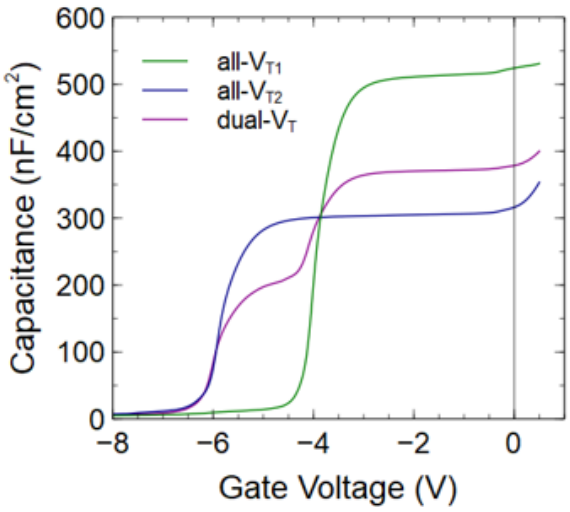

Figure 4.13 100 kHz C-V characteristics of three capacitors with gated regions resembling all-V_{T1}, all-V_{T2} and dual-V_T devices: Each square capacitor has a length of 100 µm. The dual-V_T capacitor shows a double humped CV profile.

4.2.2 Pulsed I-V Characterization

The pulsed I-V characteristics is measured with a gate pulse-width of 800 ns and drain pulse-width of 600 ns. Figure 4.14 (a) shows the pulsed transfer characteristics of all-V_{T1} and all-V_{T2} devices—measured at a quiescent drain voltage ($V_{DS,Q}$) of 0V, and quiescent gate voltage ($V_{GS,Q}$) varied from 0V to -8V. The pulsed drain current ($V_{DS,P}$) is 5V. We observe that the negative shift in threshold voltage (ΔV_T)—from the cold bias condition ($V_{GS,Q}$; $V_{DS,Q}$) of (0V; 0V) with decreasing $V_{GS,Q}$—is smaller in all-V_{T2} compared to all-V_{T1}. It has been discussed in Section 4.1.2 that ΔV_T possibly arises due to additional traps underneath the gate—at the AlGaN / SiN_x gate dielectric interface. In all-V_{T2} device, these traps are farther away from the 2-DEG, as the gate is placed farther away from the channel. Therefore, the influence of the traps is less, resulting in a smaller ΔV_T. The pulsed transfer characteristics of dual-V_T device with the same bias conditions is shown in Figure 4.14 (b). The shift in threshold voltage with decreasing $V_{GS,Q}$ resembles the all-V_{T2} device (67% of the dual-V_T

device is composed of section V_{T2}). However, the deviation from the cold bias condition is larger at high drain current densities—where section V_{T1} is fully turned-on.

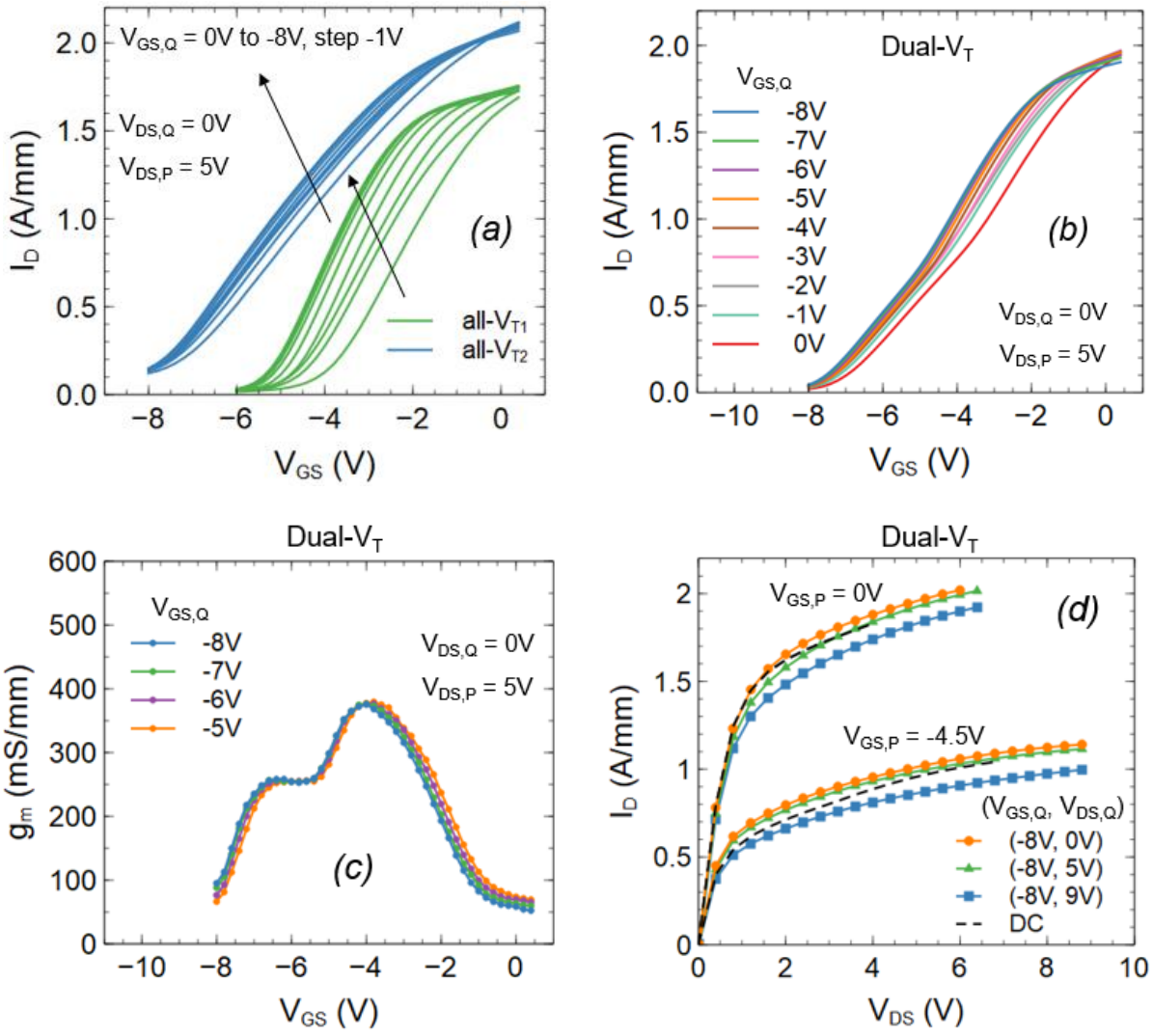

Figure 4.14 Pulsed I-V characteristics. Transfer characteristics of (a) all-V_{T1} and all-V_{T2} devices, and (b) dual-V_T device showing the shift in threshold voltage (ΔV_T) from the cold bias condition ($V_{GS,Q}$; $V_{DS,Q}$) of (0V; 0V) with decreasing $V_{GS,Q}$. ΔV_T is most pronounced for all-V_{T1}. (c) g_m profile of the dual-V_T device with $V_{GS,Q}$ swept from -5V to -8V. The g_m plateau does not shift in this quiescent gate-bias range. (c) Output characteristics of the dual-V_T with $V_{GS,Q}$ = -8V, and drain stressed from 0V to 9V.

Figure 4.14 (c) shows the g_m profile of the dual-V_T device with $V_{GS,Q}$ swept from -5V to -8V. In this quiescent gate-bias range, there is negligible shift in the region where the g_m plateaus. Figure 4.14 (d) shows the output characteristics of the dual-V_T device with $V_{GS,Q}$ = -8V and drain stressed from 0V to 9V. The pulsed gate voltage ($V_{GS,P}$) is 0V. For low quiescent drain bias, we observe *anti-dispersion*. For higher drain bias, knee walk-out and decrease in drain current are observed. The deviation from the DC output characteristics is ~10%.

4.2.3 Small-Signal Performance

The S-parameters were measured from 0.25 to 67 GHz with GSG probes calibrated by 2-port line-reflect-reflect-match (LRRM) method at the probe tips—using an impedance standard substrate. On-wafer open and short structures were measured for de-embedding probe pads. The de-embedded f_T and f_{max} contour plots of the dual-V_T device—extrapolated using a -20 dB/decade slope from short-circuit current gain $|h_{21}|^2$ and Mason's unilateral gain (U) respectively—is shown in the I-V plane in Figure 4.15. The presence of a peak and a plateau are evident in the contour plots. Figure 4.16 shows the device f_T and f_{max} values as a function of gate bias at $V_{DS,Q}$ of 5V; all-V_{T1} and all-V_{T2} device results are also shown for comparison. We observe that the f_T and f_{max} of all three devices follow the trend of their respective g_m profiles. The current gain, unilateral gain, and maximum stable/available gain (MSG/MAG) for peak f_T and f_{max} conditions are plotted in Figure 4.17. The device demonstrates a peak f_T of 108.2 GHz at a quiescent gate and drain bias ($V_{GS,Q}$; $V_{DS,Q}$) of (-4.5V; 7V), and a peak f_{max} of 221.3 GHz at ($V_{GS,Q}$; $V_{DS,Q}$) of (-4.5V; 9V).

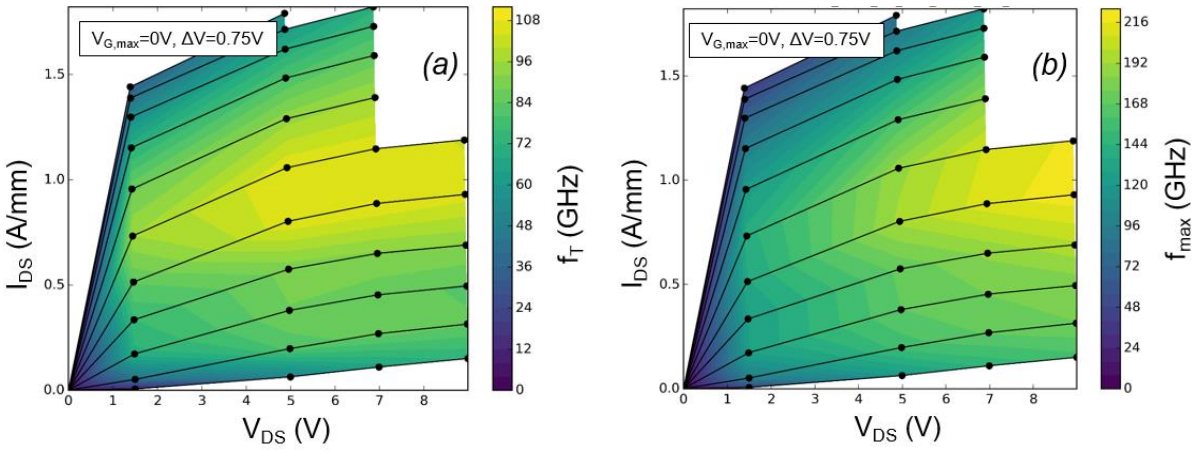

Figure 4.15 De-embedded **(a)** f_T and **(b)** f_{max} contour plots shown in the I-V plane for the dual-threshold device with 60-nm L_g, 85-nm L_{gs}, 315-nm L_{gd}. The presence of a peak and a plateau are evident in the contour plots.

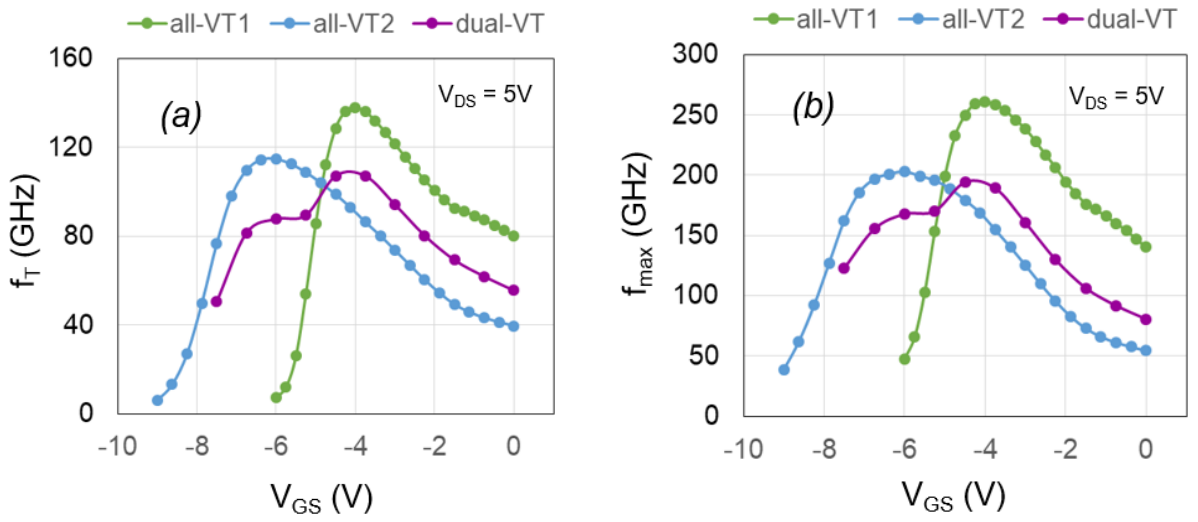

Figure 4.16 The **(a)** f_T and **(b)** f_{max} values of the dual-threshold device as a function of gate bias at $V_{DS,Q}$ of 5V; all-V_{T1} and all-V_{T2} device results are also shown for comparison. The f_T and f_{max} of all three devices follow the trend of their respective g_m profiles.

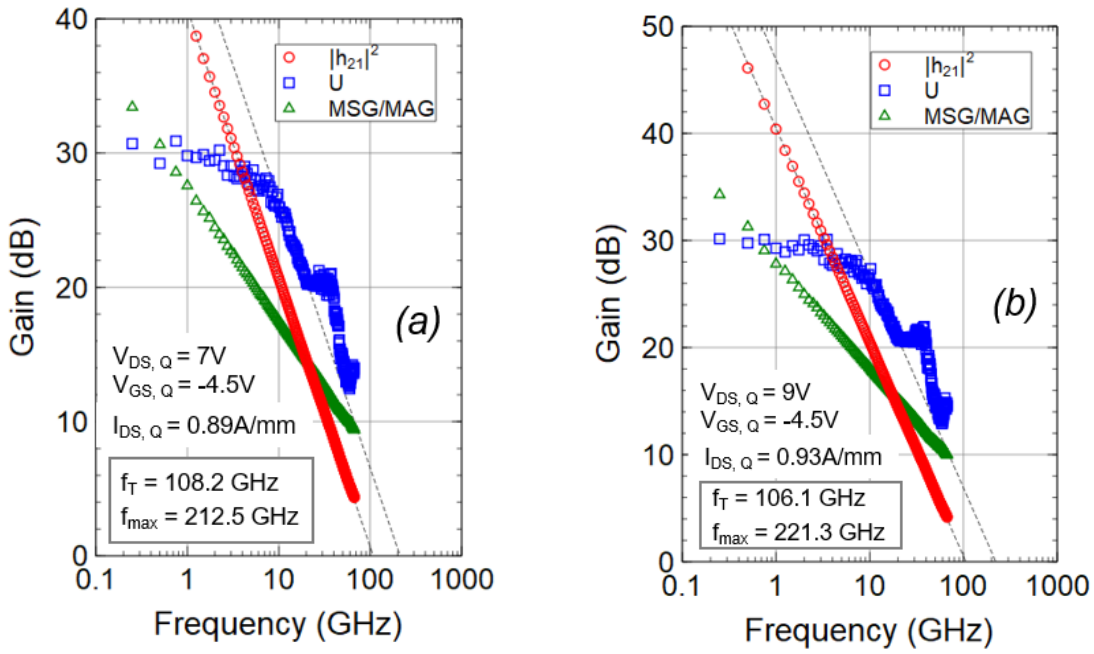

Figure 4.17 The current gain, unilateral gain and maximum stable/available gain (MSG/MAG) for peak f_T and f_{max} conditions. The device demonstrates a peak f_T of 108.2 GHz at a quiescent gate and drain bias ($V_{GS,Q}$; $V_{DS,Q}$) of (-4.5V; 7V), and a peak f_{max} of 221.3 GHz at ($V_{GS,Q}$; $V_{DS,Q}$) of (-4.5V; 9V).

4.2.4 Two-Tone Load-Pull Characterization at 30 GHz

The two-tone load-pull measurement was performed at 30 GHz with a tone-spacing of 1MHz[6]. In order to compare all-V_{T1}, all-V_{T2} and dual-V_T devices, input-bias sweeps were performed at constant source and load impedance (Γ_S; Γ_L) of $0.65\angle 52°$; $0.65\angle 52°$ and total available input power ($P_{in,available}$) of -9 dBm. We are looking at the overall trend of OIP3/P_{DC} and comparing that with the g_m profiles in Figure 4.18. All-V_{T1} (green curve) and all-V_{T2} device (blue curve) demonstrate a sharp peak in OIP3/P_{DC} at the device turn-on point. In the dual-V_T device (magenta curve), we observe three distinct OIP3/P_{DC} peaks: *(i)* the lower peak

[6] The two-tone load-pull measurements at 30 GHz were performed by Dr. Matthew Guidry.

occurs where section V_{T2} is turning on, *(ii)* the middle peak occurs in the g_m plateau—the region where the falling g_m of section V_{T2} is compensated by the rising g_m of section V_{T1}, resulting in a flat g_m region, *(iii)* the upper peak occurs where section V_{T1} is turning on. The overall trend of OIP3/P_{DC} is consistent with the g_m profile. The transducer gain (G_T) also follows the g_m profile.

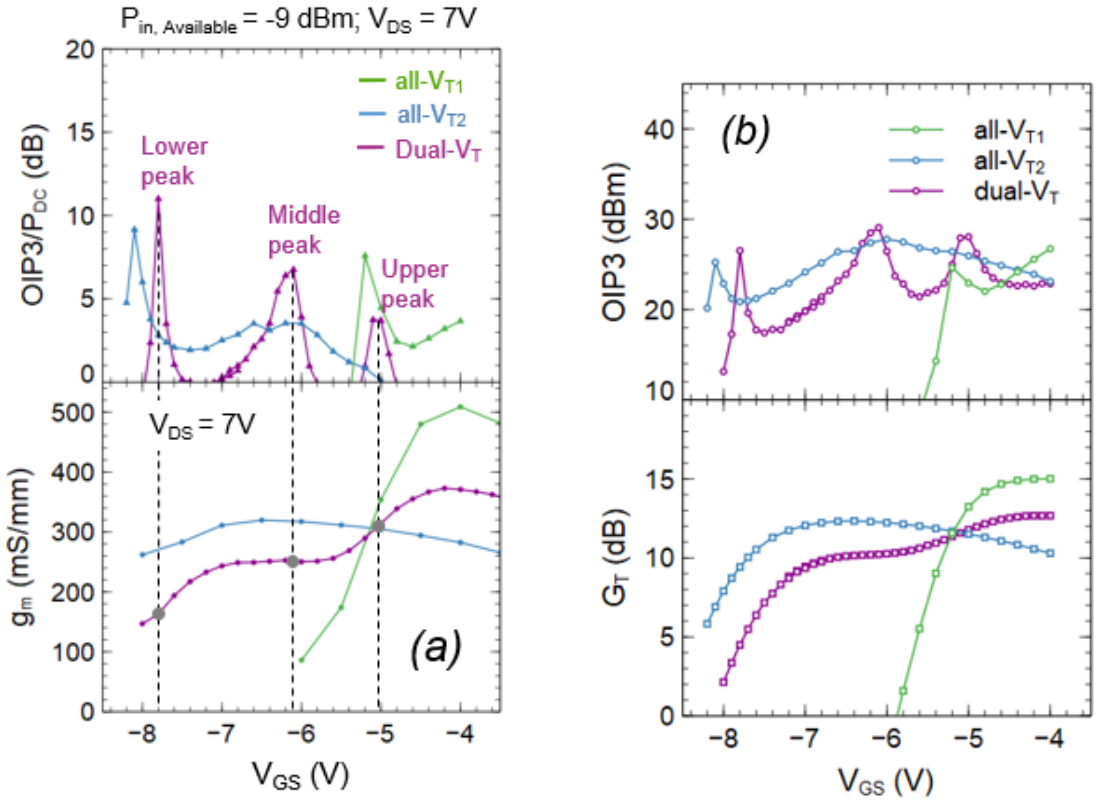

Figure 4.18 Two-tone load-pull input-bias sweep at 30 GHz with a tone-spacing of 1MHz. **(a)** OIP3/P_{DC} of three devices are shown: all-V_{T1} (green curve), all-V_{T2} (blue curve) and dual-V_T (magenta curve). Their respective g_m profiles are also shown for comparison. The dual-V_T device exhibits three distinct OIP3/PDC peaks, consistent with its g_m profile. Figure © [2020] IEEE **[46]**. **(b)** The corresponding OIP3 and transducer gain (G_T) of the three devices.

At the middle OIP3/P_{DC} peak, linearity of the dual-V_T device is characterized by means of a two-tone input-power sweep shown in Figure 4.19. Prior to the input-power sweep, the

source and load impedance (Γ_S; Γ_L) were tuned for maximizing transducer gain. The device is biased at $V_{GS,Q}$ of -6.312V, $I_{D,Q}$ of 463 mA/mm, $V_{DS,Q}$ of 9V and Γ_S; Γ_L of 0.66∠50°; 0.65∠45°. The results in Figure 4.19 (a) show the total output power in the fundamental tones (P_{out}), the Upper (Hi) and Lower (Lo) intermodulation products ($P_{I3,hi}$, $P_{I3,lo}$), and the corresponding OIP3. We observe the generation of low IM3, with C/IM3 better than 56 dBc for input powers less than -5 dBm (Figure 4.19 (b)). The device simultaneously exhibits a maximum OIP3 of 34 dBm and a gain (G_T) of 11 dB at $P_{in,available}$ of -10.57 dBm. We observe a maximum OIP3/P_{DC} of 10.8 dB (Figure 4.19 (a)).

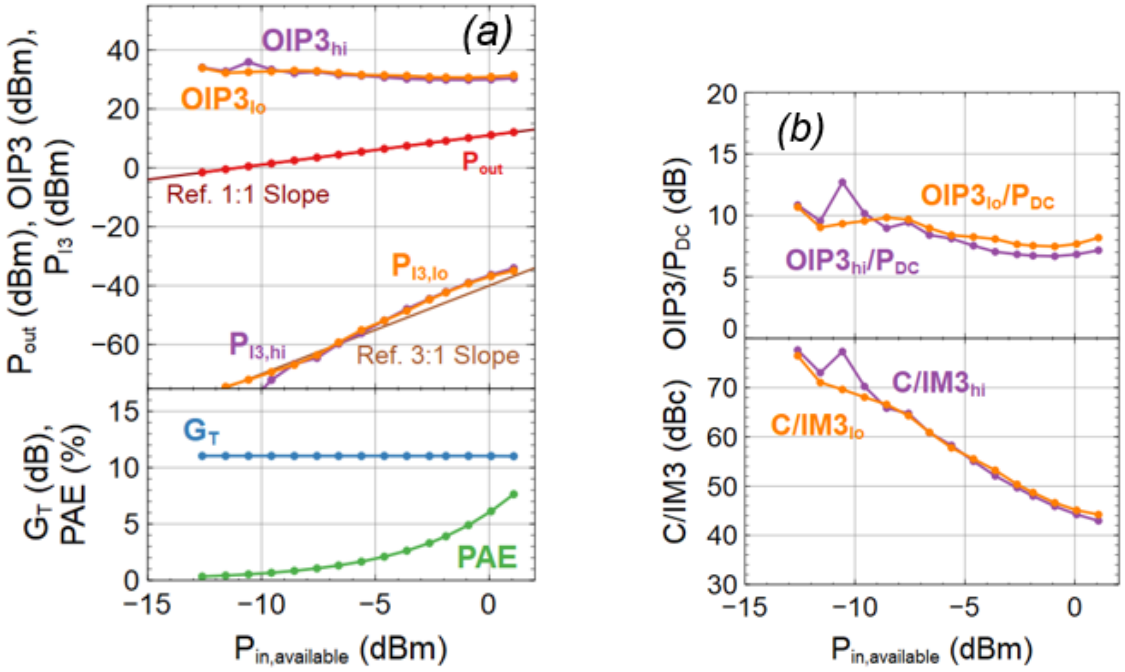

Figure 4.19 Two-tone load-pull input-power sweep at 30 GHz with tone spacing of 1MHz. (a) Total output power in the fundamental tones (P_{out}), Upper (Hi) and Lower (Lo) intermodulation products ($P_{I3,hi}$, $P_{I3,lo}$), and corresponding OIP3 are shown. The device simultaneously exhibits a maximum OIP3 of 34 dBm and G_T of 11 dB. (b) Linearity is reported in two different metrics. Carrier power to IM3 ratio (C/IM3) is better than 56 dBc for input powers less than -5 dBm. We note a maximum OIP3/P_{DC} of 10.8 dB.

Chapter 5. Conclusion and Future Work

5.1 Conclusion

In this dissertation work, N-polar GaN MIS-HEMT technology has been explored for receiver applications at mm-wave frequencies. This study focuses on device-level linearity performance of the receiving transistor, while simultaneously achieving high gain. Transconductance and its derivatives dominate the intermodulation distortion and the linear response of the device. Therefore, based on the g_m profile, two bias conditions for high linearity are identified: *(i)* at the g_{m3} zero-crossing point, where the device is turning on and the OIP3/P_{DC} is expected to peak over a narrow range of input-bias, and *(ii)* at the g_m peak, where a flat profile is desired, with high OIP3/P_{DC} over a wide range of input-bias. Device designs for both biasing conditions have been reported in this work.

The single-threshold device is designed to operate at the g_{m3} zero-crossing point, where the device is turning on. While the bias condition is selected for high linearity, the device structure is designed for high gain; the single-threshold device implements a thin GaN cap and scaled gate-length to achieve high gain. The device simultaneously exhibited excellent linearity and high gain performance of 15 dB OIP3/P_{DC}, 32 dBm OIP3 and 12.7 dB G_T at 30 GHz, demonstrating its potential as a suitable device technology for small-signal receiver applications. The linearity of this high performance HEMT is sensitive to bias. With a two-tone load-pull input-bias sweep, we demonstrated that the OIP3/P_{DC} peaks over a narrow range of gate-bias showing that linearity is sensitive to bias. Generally, all transistors exhibit a g_{m3} zero-crossing point and a corresponding OIP3/P_{DC} peak at the device turn-on point.

The dual-threshold device implements a linearization technique called Derivative superposition (DS) at the device-level to cancel g_m derivatives and tailor the g_m profile for high linearity over a wide range of input-bias. The device consists of segments of two different threshold voltages – V_{T1} and V_{T2} – defined by recessing the gate to different depths, forming a castellated structure along the gate-finger. The dual-threshold device has been fabricated using the self-aligned process with modifications to realize the two threshold voltages. A castellated gate-trench—with well-defined V_{T1} and V_{T2} sections—is achieved by using a PMMA/Cr second mask during the gate recess etch. We have demonstrated that the dual-threshold device technology based on N-polar GaN MIS-HEMT is realizable and can achieve high gain at mm-wave frequencies. Results show 10.8 dB OIP3/P_{DC}, 34 dBm OIP3 and 11 dB G_T at 30 GHz. An optimized dual-threshold device is promising for achieving high linearity performance over a wide range of input-bias.

5.2 Future Work

5.2.1 Optimizing Dual-Threshold Device

The dual-threshold device can be optimized for high linearity over a broader input-bias range. This can be achieved by reducing $V_{T,diff}$ —the threshold voltage difference between V_{T1} and V_{T2}. As discussed in Chapter 4, the two-tone load-pull input-bias sweep of the dual-threshold device shows three distinct OIP3/P_{DC} peaks: the lower peak occurs where section V_{T2} is turning on; the middle peak occurs in the region where the falling g_m of section V_{T2} is compensated by the rising g_m of section V_{T1}, resulting in a flat g_m profile; the upper peak

occurs where section V_{T1} is turning on. Reducing $V_{T,diff}$ by designing threshold voltage V_{T2} to be less negative will bring the middle peak closer to the upper peak; this can be achieved at the epi-level by reducing the GaN IL thickness. By reducing $V_{T,diff}$ and adjusting the width of section V_{T1} and V_{T2}, a good overlap between the middle and upper peaks can be achieved. This will result in high OIP3/P_{DC} over a broader range of input-bias. To explore this approach, the dual-threshold device can be optimized with a thickness series of the GaN IL. Furthermore, reducing the GaN IL thickness will also reduce the effective gate-to-channel distance in section V_{T2} of the dual-threshold device, which will improve the gain of section V_{T2} and the overall gain of the dual-threshold device.

5.2.2 Reducing Output Conductance

We have addressed transconductance non-linearity—the dominant source of distortion in transistors. As g_m non-linearity is minimized or eliminated, other sources of distortion increasingly dominate the linearity performance of the device. Therefore, they must be investigated to further linearize the device. Among other sources of distortion output conductance (G_{ds}) plays a role as it affects output current when the device is operated in the saturation regime at a given gate and drain bias. As the gate-length is further scaled to achieve higher gain, gate aspect-ratio could be affected and associated short-channel effects could increase G_{ds} introducing additional source of distortion. The overall influence of lateral and vertical scaling of device dimensions and the effect of G_{ds} on the intermodulation distortion with varying load impedance shall therefore be investigated.

5.2.3 Noise Characterization

So far, little work has been done on noise figure for N-polar GaN HEMTs. The only noise performance of N-polar GaN MIS-HEMTs has been reported by Guidry *et al.* with NF_{min} as low as 1.1 dB at 30 GHz [48]. Further investigation into the sources of noise and noise characterization would be significant in evaluating the performance of N-polar GaN MIS-HEMTs for receiver applications.

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