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UNIVERSITY OF CALIFORNIA
RIVERSIDE

Study of Nanocrystal Structures and Their Memory Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Mario Jesus Olmedo

June 2012

Dissertation Committee:
Dr. Jianlin Liu, Chairperson
Dr. Roger Lake
Dr. Cengiz Ozkan

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The Dissertation of Mario Jesus Olmedo is approved:

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University of California, Riverside

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This thesis is dedicated to my Mom and Dad.

ABSTRACT OF THE DISSERTATION

Study of Nanocrystal Structures and Their Memory Applications

by

Mario Jesus Olmedo

Doctor of Philosophy, Graduate Program in Electrical Engineering

University of California, Riverside, June 2012

Dr. Jianlin Liu, Chairperson

In the field of floating gate memory, also known as flash memory, silicon (Si) nanocrystals (NC) are one of the leading alternatives to traditional poly-Si floating gate memory because of their improved scalability, speed and simpler fabrication. In our research, Si NCs are grown on top of oxide covered carbon nanotubes (CNTs) by gas source molecular beam epitaxy for the purpose of making floating gate memory with the CNT as the field effect transistor (FET) channel. At certain conditions the NCs align on the apexes of the CNTs. These alignment properties are studied with relation to different growth conditions and sample parameters. Also FET and memory device characteristics are studied for devices based on this structure as well as the frequency response of devices that exhibit ambipolar properties. Another memory technology that has been attractive to replace flash due to its low power consumption and its stacking properties is resistive memory. Here ZnO NCs are used as the resistive switching material. The memory characteristics are studied with a conductive atomic force microscope contacting

a single NC. Both of these technologies will be shown to have favorable properties compared to the current floating gate technology.

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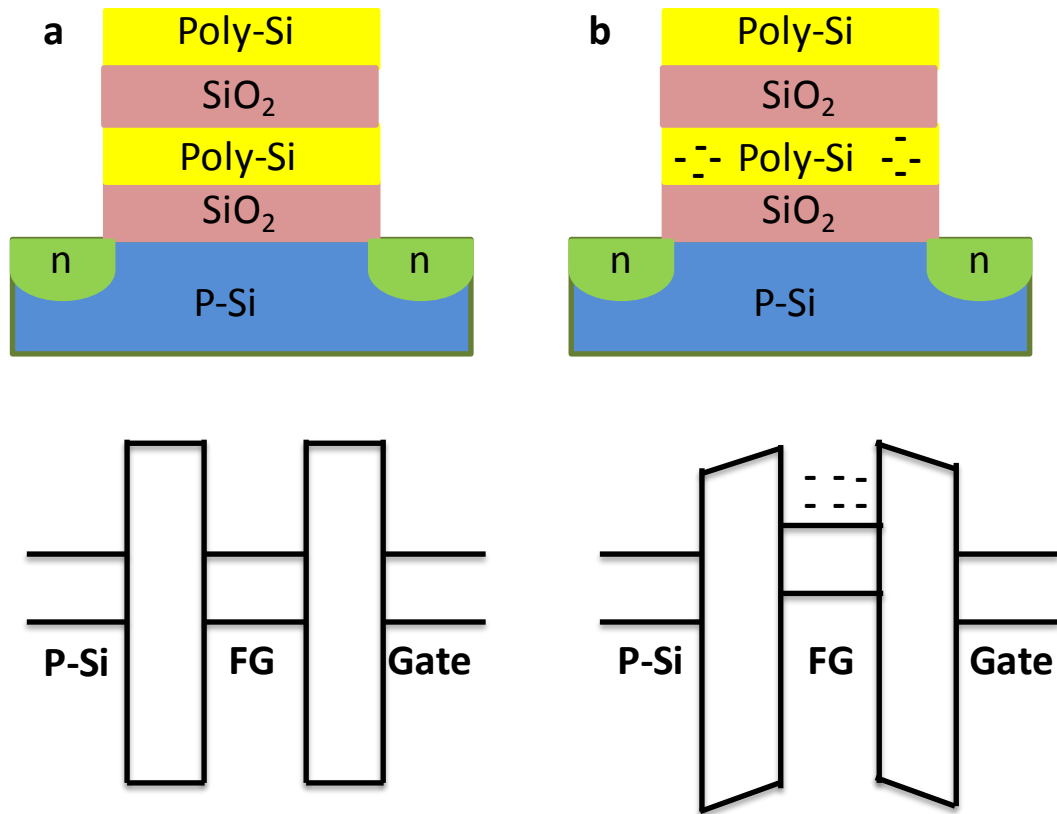
Chapter 1: Introduction

1.1 Introduction to flash

In the field of electronic storage based on complementary metal oxide semiconductor technology there are two main types of memories. First is volatile memory such as random access memory (RAM) that retains a bit of information for a short amount of time and requires intermittent refreshing to retain that same bit for longer periods. There are several types of volatile memories in use such as static-RAM that has really fast write and erase speeds and it is used as cache in central processing units. Due to the use of six transistors per SRAM cell however this memory is only used in applications where speed and not cost is the main concern. For larger storage, yet volatile performance capabilities, there is dynamic-RAM. This memory is used as temporary storage in computers. It consists of a transistor and a capacitor combination and can be made cheaper than SRAM. Since both memory technologies are volatile, once the power is turned off, all the stored information is lost. For longer, non-volatile electronic storage other technologies are used such as flash memory.

Flash memory, also known as floating gate memory is composed of a single metal oxide semiconductor field effect transistor (MOSFET) that has an extra insulated gate between the control gate and channel. This floating gate has the ability to store charge and change the characteristics of the transistor. Specifically, the stored charge changes the threshold voltage. This means that when device is programmed, when an excess of electrons are present in the floating gate, then the threshold voltage increases in the positive direction. The reason for this is that the field from the floating gate competes

with the electric field of the control gate. To achieve programming and erasing procedures into the floating gate, the electrons are tunneled through the oxide separating the channel and the floating gate. The schematic and respective energy band diagram of the floating gate structures are shown in figure 1-1(a) for the initial state and figure 1-1(b)



for the program state.

Figure 1-1. Schematic cross section of a floating gate transistor and energy band diagram for the (a) initial state and (b) programmed state.

To read the two states in the memory cell, a reading voltage is supplied and the resulting current is measured at the drain. For the programmed state with an n-type transistor the reading current should be near 0 or I_{OFF} . While after erase there should be a detectable current (I_{ON}) as shown in figure 1-2.

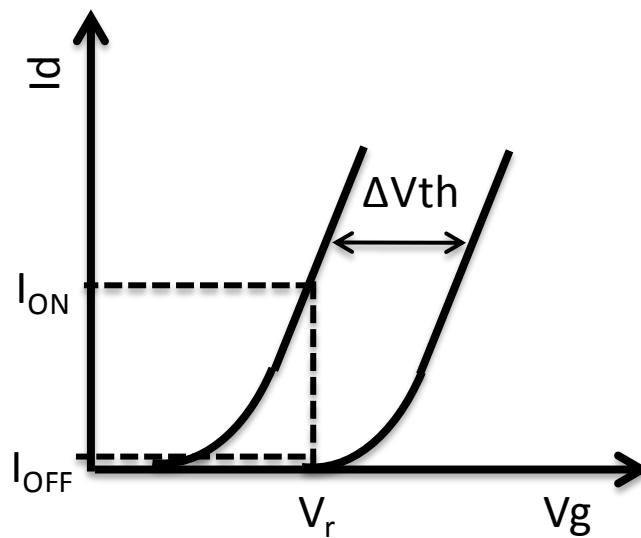


Figure 1-2. I-V curves of a floating gate device when there is no charge stored (I_{ON}) and when there is negative charge stored (I_{OFF}).

It is not a simple task to transfer charge from the channel to the floating gate. There are several methods of tunneling that are used in programming and erasing for different floating gate technologies. The first one is hot electron injection which is generally used in programming and consists of putting a lateral field between the source and drain that heats up the electrons in the channel while also adding a field from the

control gate that will attract the electrons into the floating gate.¹ The second method is called Fowler-Nordheim (FN) tunneling. This method consists of putting a high electric field to the control gate while leaving the source and drain either floating or grounded. The high field would lower the oxide barrier width and make it into a triangular shape. This will increase the probability of electron tunneling through the oxide.² Since both mechanisms involve electrons passing through the oxide layer, there is no surprise that this layer is the most important and most likely to fail part of the device. A typical oxide failure is the development of leakage sites within the oxide that set a path for electrons that are stored in the floating gate to be released into the channel. A simple solution for this is the use of nanocrystals (NC) as the floating gate instead of a continuous floating gate. The main advantage of NCs is the discretization of charge. So that when a leakage site appears on the tunnel oxide only a small part of the charge is lost and the whole device is not rendered useless. This is depicted in figure 1-3(a) for a continuous floating gate and figure 1-3(b) for a NC floating gate.

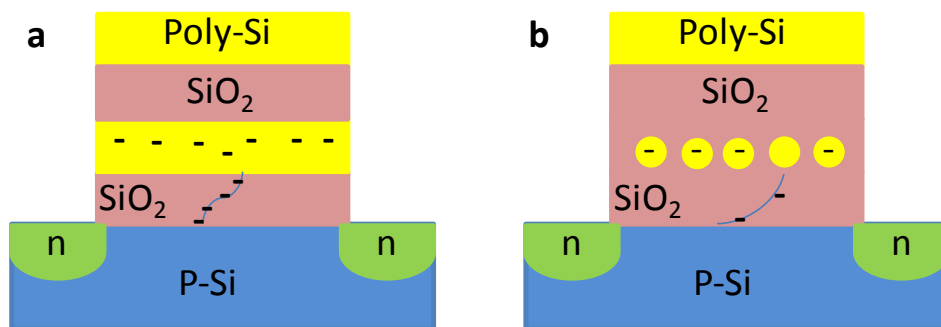


Figure 1-3. Schematic representation of a leakage site in (a) a continuous floating gate and (b) NC floating gate transistor memory.

1.2 Introduction to NC floating gate memory

To scale flash memory to ever smaller dimensions the thickness of the oxide needs to also be decreased. As the oxide decreases in thickness the durability is compromised. NC floating gate memory has the advantage of having discrete charge distribution that increases the stability and endurance of flash memory. This leads to thinner oxide thicknesses that would not be reliable under a continuous floating gate. In addition, the NCs would be able to affect the channel with as little as one electron per NC. This would also lead to lower power consumption and higher speeds.³⁻⁷ Other ways of implementing NCs have been with MOS capacitor structures,⁸⁻¹⁰ as well as with other semiconductors, such as Ge,⁹⁻¹² instead of Si, and metals.¹³⁻²⁸ Also, different methods can be used to grow the NCs such as ion implantation, CVD, MBE and sputtering.^{8-9,28-30} Since damage to the tunneling oxide is detrimental to memory characteristics, methods such as ion implantation and sputtering that can damage the oxide layer are avoided in favor of CVD and MBE. A major focus for the improvement of NC memory has been density. The higher the density of the NCs, the more charge can be stored and the faster the memory can be switch from one state to another. CVD techniques have been able to reach high densities of 10^{11} - 10^{12} NCs/cm² with Si NCs³¹⁻³³ and silicide NCs³⁴⁻³⁸. The growth mechanism for CVD grown NCs on oxide starts with introducing a reactive gas, such as silane (SiH₄), with a heated substrate. On the surface of the substrate the silane breaks into Si adatoms and diffuses until it finds a seed site or trap. Once settled other atoms attach to the seed and the NC forms. Controlling the seed mechanism or the trap sites is a way to increase or decrease density. In the case of CNT alignment, the surface

energy difference between the flat areas and the mesas act as a trap, inducing preferential NC growth.

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Chapter 2: Methodology

2.1 Nanocrystal growth

2.1.1 Si nanocrystal growth

For the growth of silicon NCs on oxide covered CNTs I designed and built a gas source molecular beam epitaxy system (GSMBE). This system consists of two different vacuum chambers separated by a gate valve. The growth chamber is pumped by a turbo molecular pump capable of pumping 170ls^{-1} of nitrogen and it is also backed by scroll pump capable of pumping $10\text{m}^3\text{h}^{-1}$. The transfer chamber is only pumped by a scroll pump. The typical vacuum achieved before growth was about 2×10^{-8} torr. The vacuum is measured first by thermocouple gauges that read pressures starting from atmosphere to 1×10^{-3} torr. Then a Bayard-Alpert ionization gauge is used from $\sim 10^{-4}$ to maximum vacuum. The loading procedures for a typical growth begin by introducing the sample to the inside of the transfer chamber in atmosphere and placing it in a holder that attaches to the transfer rod. After the sample is in place, the chamber door is sealed and the chamber is evacuated. Once the set vacuum is reached the gate valve is opened and the sample is transferred to the growth chamber. Inside the growth chamber the sample detaches from the transfer rod while at the same time attaching to the manipulator for growth. The manipulator uses a resistive heater behind the sample to provide heat and raise the sample temperature for growth. In between the heater and the sample lies a C-type thermocouple wire that measures temperature. This wire is calibrated by an outside pyrometer.

For Si/Ge growth the sources used are disilane (Si_2H_6) and digermane (Ge_2H_6). At high temperatures both gases break into their respective components. The gas lines are

evacuated before every growth to prevent contamination. A mass flow controller controls the gas flow between the low pressure line and the high vacuum chamber. The gas source is introduced to the growth chamber in a direct path to the sample so that even source coverage is reached. Additional features of the GSMBE include a solid source effusion cell; which consists of a tubular resistive heater with a boron nitride crucible in the middle of it that contains the solid source, as shown in figure 2-1. The use of this source is to heat the material inside the crucible to the point of sublimation. The source vapor will then be directed towards the sample because the cell is pointed in a direct path towards it. Also, there is a gas source cracker, which consists of two resistive tubular heaters protected by a boron nitride tube. This addition is used to crack the bonds of a gas passing inside by exposing to large amounts of heat. The gas used in combination with the cracker is acetylene (C_2H_2) for the growth of graphene. This growth, however, will not be discussed.

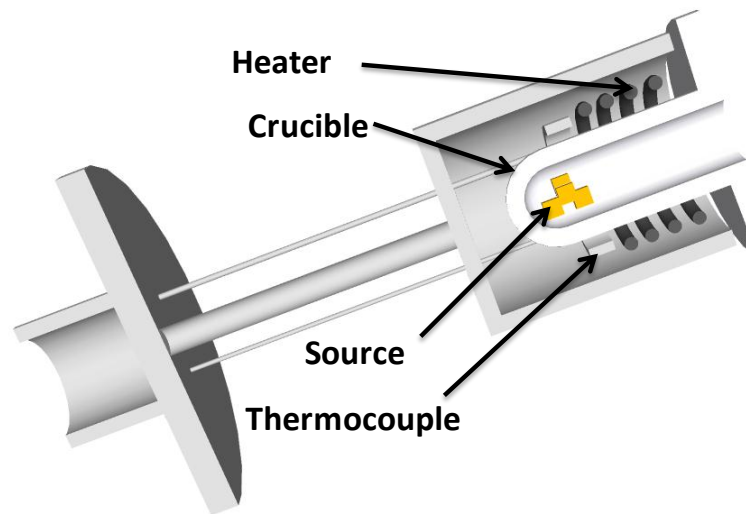


Figure 2-1. Effusion cell schematic

Initial growths were performed on SiO₂ surfaces. Growth temperatures were between 500°C and 700°C. It was evident that Ge NCs grew faster than Si NCs on the surface. As seen in figure 2-2. The slower and more controlled Si growth would then be chosen as the material for the use in the alignment experiments.

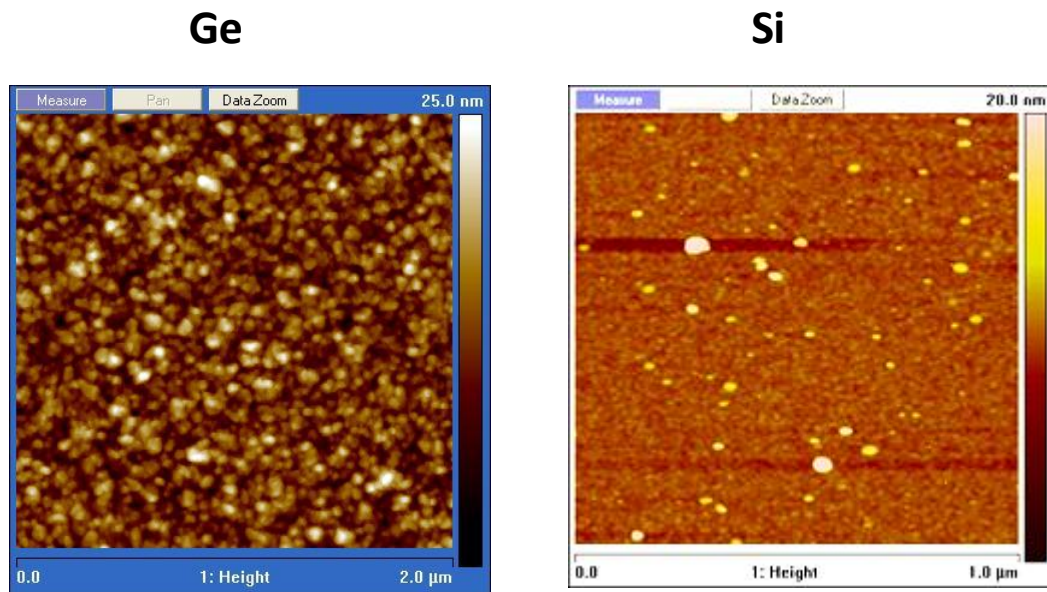


Figure 2-2. Examples of Ge and Si growths; Images were taken by AFM.

2.1.2 ZnO nanocrystal growth

ZnO NCs were grown on a plasma assisted MBE system. The process of growing ZnO NC starts with a clean Si wafer. The reaction consists of a beam of elemental Zn that oxidizes in contact with O⁻ that has been previously cracked in the plasma chamber. It will be discussed in more detail in chapter 6.

2.2 Nanocrystal characterization

2.2.1 AFM characterization

Atomic force microscopy was developed in the 1980's by Gerd Binnig and Calvin Quate and Christoph Gerber. This tool has the ability to detect surface topography at the nanoscale. It uses a mechanical probe sustained by a cantilever. The probe is in contact with the sample and interacts with it through van der Waals force. The back of the cantilever is coated with a reflective material so that a laser directed to it can be reflected. On the other side of this reflection, a photodetector is used to track the movements of the laser as shown in figure 2-3. The movement of the laser spot on the photodetector is directly proportional to the movement of the cantilever as it moves across the surface of the sample. This movement is achieved by the deformation of piezoelectric actuators that precisely control the tip movements to less than a nanometer in distance.

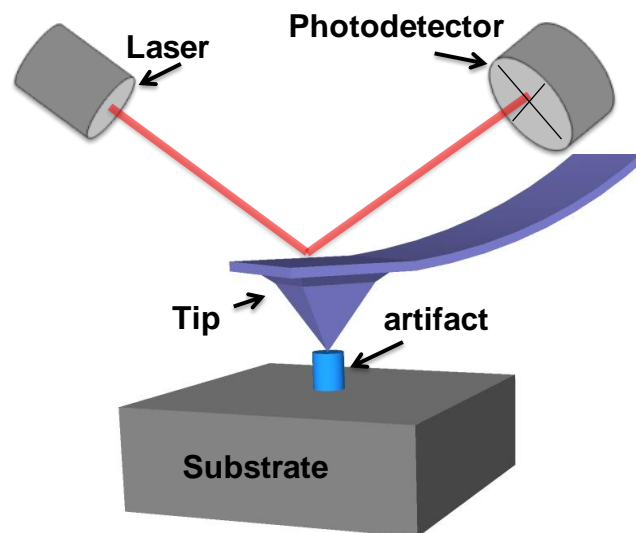


Figure 2-3. AFM mechanism schematic in contact mode.

The AFM has three main operation modes: contact mode, non-contact mode and tapping mode. Contact mode is the easiest mode of operation to understand, it was also the first to be developed. Contact mode is also widely used for measurements that require physical contact such as conductive AFM, lateral force AFM and piezoelectric force AFM. Contact mode measures the surface by scanning the tip back and forth on its x-axis then moving its y axis and so forth. The image is created as the laser deflection is detected from tip movement caused by surface corrugations. This however causes the tip to apply different forces to the surface as it moves through it because of the different bend angles of the cantilever with different distances between the tip and surface. A solution is to track the force the tip imposes on the surface by using a constant force mode. For which the tip's height is constantly adjusted to maintain a constant deflection. It is this adjustment that is displayed as height data and composes the images. A feedback circuit is needed to properly make adjustments as the tips moves across the surface. The ability to track the surface in this manner is limited by the feedback circuit speed. If the tip scan mode does not use height adjustment, it will only measure the deflection. This is useful for small area, high-speed scans that can reach atomic resolution. This technique is known as variable-deflection mode. However, because the tip is in direct contact with the surface, the stiffness of the cantilever needs to be less than the effective spring constant holding atoms together, which is on the order of 1 - 10 nN/nm. Most contact mode cantilevers have a spring constant of $< 1\text{N/m}$.

Non-contact mode as its name entails is not in contact with the surface. It belongs to a family of AC modes, which refers to the use of an oscillating cantilever. A stiff

cantilever is oscillated in the attractive force regime (fig. 2-4), meaning that the tip is quite close to the sample, but not touching it, just enough to be affected by Van der Waals forces. The forces between the tip and sample are quite low, on the order of pN (10^{-12} N). The detection scheme is based on measuring changes to the resonant frequency or amplitude of the cantilever.

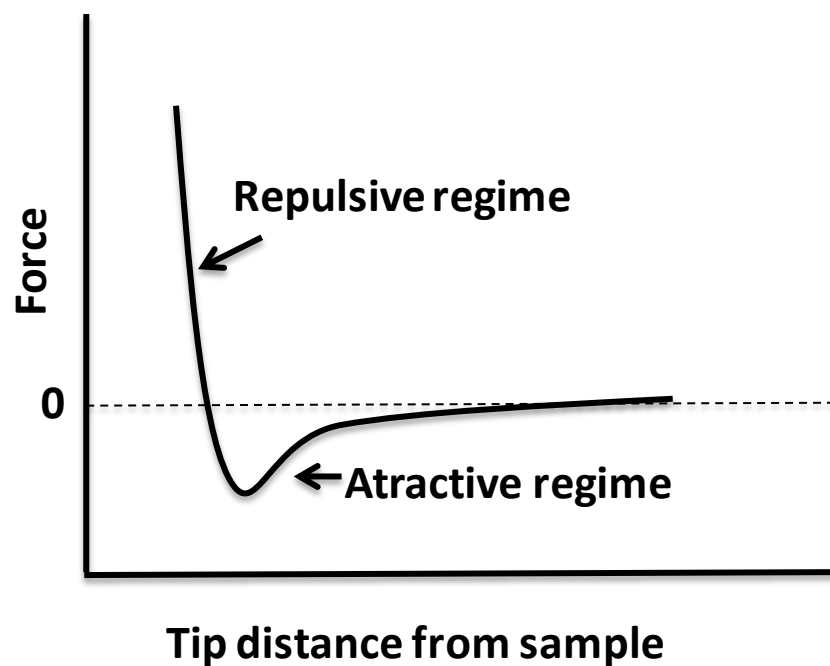


Figure 2-4. Force curve as a measure of distance. As the tip gets closer to the sample, the tip will have an attractive force towards the sample. Until the sample and tip touch each other then the tip and the sample would have a repulsive force upon them.

In tapping mode a stiff cantilever is oscillated closer to the sample than in noncontact mode. Part of the oscillation's amplitude extends into the repulsive regime, so effectively the tip intermittently taps the surface. Very stiff cantilevers are typically used,

as tips can get attached in the water contamination layer. The advantage that tapping mode has is that the lateral resolution on soft samples is improved. Lateral forces such as drag, common in contact mode, are virtually eliminated. For poorly adsorbed specimens on a substrate the tapping mode advantage is clearly seen because in contact mode the tip might move that sample. All of the CNT NC sample topographies are measured in tapping mode; while the ZnO NC samples are measured in contact mode.

2.2.2 SEM characterization

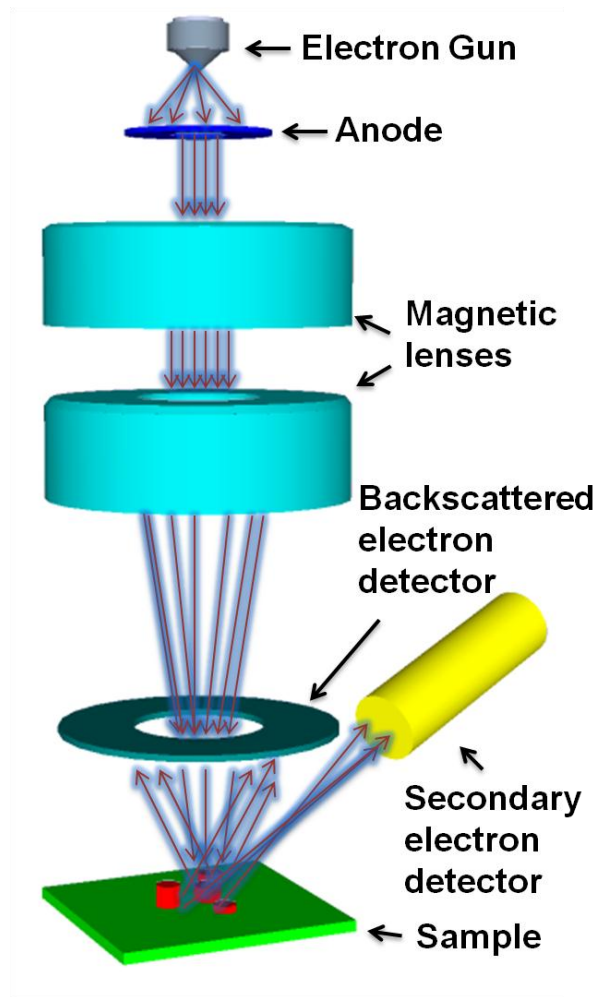


Figure 2-5. Schematic drawing of the SEM electron optics

The scanning electron microscope (SEM) is a microscope that uses electrons instead of light to form an image. A beam of electrons is produced at the top of the microscope by an electron gun composed commonly by a Ta filament and an anode. The electron beam follows a straight vertical path through the microscope, which has to be held within a vacuum. The beam travels through electromagnetic fields and lenses, as seen in figure 2-5, which focus the beam, like its light counterparts, down toward the sample. Once the beam hits the sample, secondary electrons, X-rays and photons are ejected from the sample. These particles are then detected and processed into an image. The scanning electron microscope has many advantages over traditional microscopes. The SEM has a large depth of field, which allows for specimens with large height contrast to be in focus at one time. The SEM also has much higher resolution, so closely spaced specimens below the 200nm limit of light microscopes can still be detected at much higher levels. Because the SEM uses electromagnets rather than lenses, the researcher has much more control in the degree of magnification. All of these advantages, as well as the actual strikingly clear images, make the scanning electron microscope one of the most useful instruments in research today.

2.2.3 TEM characterization

The transmission electron microscope (TEM) uses a higher energy electron beam than an SEM (>100 kV) transmitted through a very thin sample to image and analyze the structure of materials with atomic scale resolution. The electron beam is focused with electromagnetic lenses and the image is observed on a fluorescent screen, or recorded with a digital camera. The electrons are accelerated to several hundred kV, giving them

wavelengths much smaller than that of light: 200kV electrons have a wavelength of 0.025Å. However, whereas the resolution of the optical microscope is limited by the wavelength of light, that of the electron microscope is limited by aberrations inherent in electromagnetic lenses, to about 1-2 Å.

Because it is almost impossible to look through a single layer of atoms, it is unlikely that TEM images would yield images of individual atoms. Rather for high resolution TEM images that show the crystal lattice of a material it is actually the interference pattern between the transmitted and diffracted beams. This imaging mode allows us to observe planar and line defects, grain boundaries, interfaces, etc. with atomic scale resolution. The TEM has also the capability of having brightfield/darkfield imaging and diffraction pattern modes, which operate at intermediate magnification. They also provide invaluable information about the morphology, crystal phases, and defects in a material.

2.2.4 AES characterization

In an Auger electron spectroscope (AES) which is part and electron microscope which consists of electrons of energy 3-20keV that are incident upon a conducting sample. These electrons cause bound electrons from atoms contained in the material to be ejected resulting in a photoelectron and an atom with a core hole. The atom then relaxes by capturing an electron with a lower binding energy that drops into the core hole. The energy thus released by the electron captured is converted into an X-ray or causes a second electron to be emitted. This electron is called an Auger electron after Pierre Auger who discovered this relaxation process. After the emission of the Auger electron, the

atom is left in a doubly ionised state. The energy of the Auger electron is characteristic of the element that emitted it, and can thus be used to identify the element. The short inelastic mean free path of Auger electrons in solids ensures the surface sensitivity of AES.

AES is a popular technique for determining the composition of the top few layers of a surface. It cannot detect hydrogen or helium, but is sensitive to all other elements, being most sensitive to the low atomic number elements. AES must be carried out in ultra high vacuum (UHV) conditions. A popular method of looking at buried layers with AES is to use the technique in combination with ion milling. This is also common to do when a sample is brought into the UHV environment from air, because it will be coated with carbon compounds and oxygen. These materials have to be removed (usually by sputtering) before a clean surface can be achieved and studied. Sputtering involves directing a beam of plasma ions (usually Ar, Cs or O ions) at between 500eV and 5keV at the sample. This process cleans the surface, but can also be used to erode away the sample to reveal structure beneath the surface. This is obviously a destructive technique.

2.3 Nanocrystal device fabrication

2.3.1 ALD deposition

Atomic layer deposition (ALD) is a self-limiting, sequential surface chemistry technique that deposits conformal thin-films of materials onto substrates of varying compositions. ALD is similar in chemistry to chemical vapor deposition (CVD), except that the ALD reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction. Due to the characteristics of self-limiting

and surface reactions, ALD film growth makes atomic scale deposition control possible. By keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as $\sim 0.1 \text{ \AA}$ (10 pm) per cycle. Separation of the precursors is accomplished by pulsing a purge gas (Ar/N₂) after each precursor pulse to remove excess precursor from the process. Figure 2-6 shows a typical deposition cycle of Al₂O₃ using both water and AlCl₄ as the precursors.

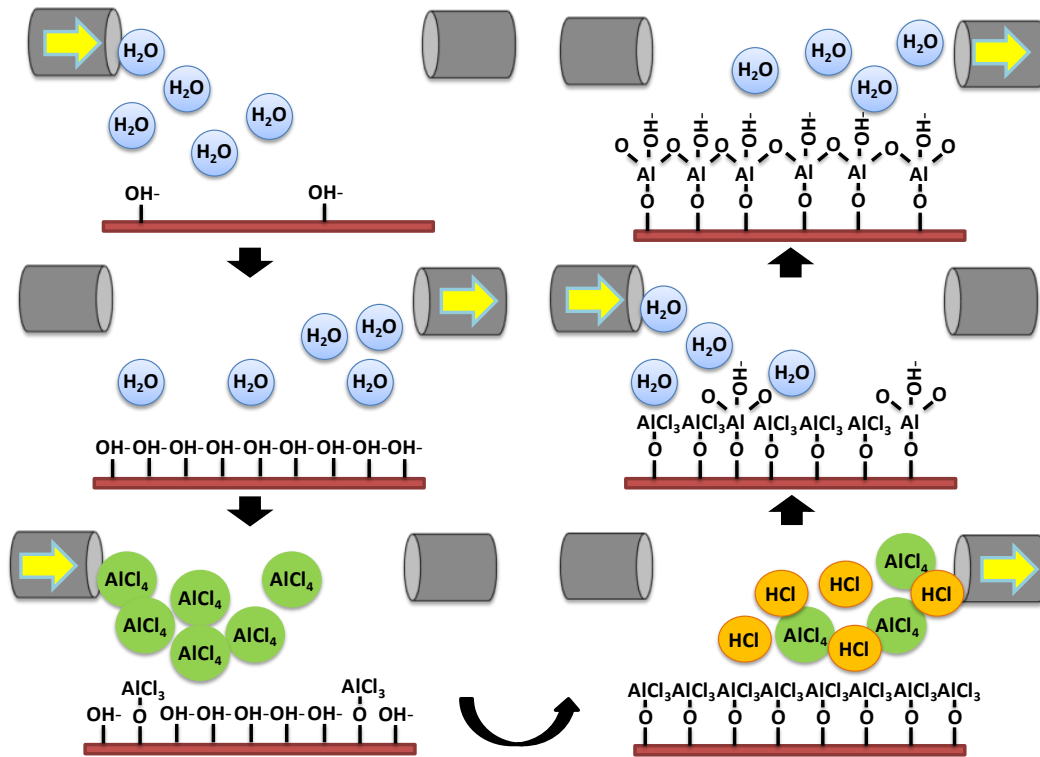


Figure 2-6. ALD deposition process. First water is pulsed from the source to the growth chamber, then a set time is waited until the substrate surface is fully covered. After that time has passed, the remaining water is pumped out and the AlCl₄ sourced is pulsed in. The second precursor reacts with the water to create HCl. After the next water pulse the first layer of Al₂O₃ is formed.

2.3.2 Photolithography

Photolithography is the process of transferring geometric shapes on a mask to the surface of a silicon wafer. The steps involved in the photolithographic process are wafer cleaning; barrier layer formation; photoresist application; soft baking; mask alignment; exposure and development; and hard-baking. In the first step, the wafers are chemically cleaned to remove particulate matter on the surface as well as any traces of organic, ionic, and metallic impurities. After cleaning, silicon dioxide, which serves as a barrier layer, is deposited on the surface of the wafer. After the formation of the SiO₂ layer, photoresist is applied to the surface of the wafer. High-speed centrifugal whirling of silicon wafers is the standard method for applying photoresist coatings in IC manufacturing. This technique, known as "spin coating," produces a thin uniform layer of photoresist on the wafer surface. There are two types of photoresist: positive and negative. For positive resists, the resist is exposed with UV light wherever the underlying material is to be removed. In these resists, exposure to the UV light changes the chemical structure of the resist so that it becomes more soluble in the developer. The exposed resist is then washed away by the developer solution, leaving windows of the bare underlying material. The mask, therefore, contains an exact copy of the pattern which is to remain on the wafer.

Negative resists behave in just the opposite manner. Exposure to the UV light causes the negative resist to become polymerized, and more difficult to dissolve. Therefore, the negative resist remains on the surface wherever it is exposed, and the developer solution removes only the unexposed portions. Masks used for negative photoresists, therefore, contain the inverse (or photographic "negative") of the pattern to

be transferred. Figure 2-7 below shows the pattern differences generated from the use of positive and negative resist.

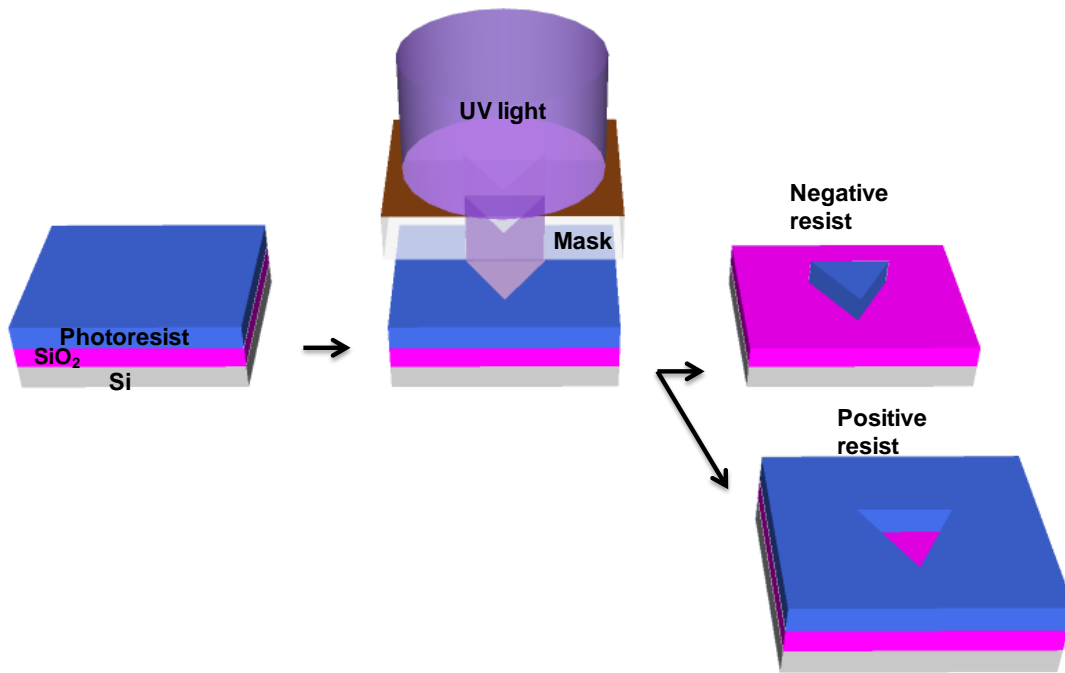


Figure 2-7. Schematic of the photolithography process.

2.3.3 E-beam evaporation

In evaporation the substrate is placed inside a vacuum chamber, in which a block of the material to be deposited is also located. The source material is then heated to the point where it starts to boil and evaporate. The vacuum is required to allow the molecules to evaporate freely in the chamber, and they subsequently condense on all surfaces. This principle is the same for all evaporation technologies, only the method used to the heat (evaporate) the source material differs. There are two popular evaporation technologies,

which are e-beam evaporation and resistive evaporation each referring to the heating method. In e-beam evaporation, an electron beam is aimed at the source material causing local heating and evaporation. The material to be evaporated is in the form of single ingots if they are to be melted or in pieces if they are to be sublimated. The electron beams can be generated by thermionic emission, field electron emission or the anodic arc method. The generated electron beam is accelerated to a high kinetic energy and focused towards the ingot. When the accelerating voltage is between 20 kV – 25 kV and the beam current is a few amperes, 85% of the kinetic energy of the electrons is converted into thermal energy as the beam bombards the surface of the ingot. The surface temperature of the ingot increases resulting in the formation of a liquid melt. Although some of incident electron energy is lost in the excitation of X-rays and secondary emission, the liquid ingot material evaporates under vacuum.

Chapter 3: Periodic Alignment of Si Quantum Dots on Hafnium Oxide Coated Single Wall Carbon Nanotubes

3.1 Introduction

Si QDs are utilized for a wide range of applications including traditional electronics such as memory^{1,2}, optoelectronics^{3,4}, and biotechnology⁵. Single QD devices have been fabricated to outperform current devices such as field effect transistors⁶ for ultra large scale integration. Several options are already available via top-down approaches such as electron beam lithography and nanostamping⁷ that can fabricate single QD devices. Another popular method is the growth of QDs via self assembly instead of fabrication. One of the major hurdles in this approach is the alignment of the QDs themselves. Here we demonstrate a solution to Si QD alignment using a hafnium oxide covered SWCNT template.

The template comprises of HfO₂ ridges formed by atomic layer deposition growth of a HfO₂ thin film on SWCNTs on a SiO₂ surface. The major advantage for the use of SWCNTs is in their 1-D shape and nanometer scale diameter, which will enable applications to go beyond the CMOS ultimate limit. The technique of selective area epitaxy^{8,9} has reported the alignment of QDs on Si ridges. This technique starts with a top down patterned template, followed by a bottom up growth of QDs. This process requires a smooth surface so that during the QD growth the adatoms can migrate to the lowest energy spots. Traditionally, single crystal surfaces have been used for the alignment of QDs via selective epitaxial growth or QD superlattice growth. The atomic layer

deposition technique can produce HfO_2 thin dielectric films with smooth conformal polycrystalline surfaces, which can be used for QD self assembly¹⁰. QDs grown on HfO_2 surfaces may have potential applications in nonvolatile nanocrystal memories.

3.2 Experiment

First, SWCNTs were grown on SiO_2/Si substrates using a chemical vapor deposition technique [11-12]. The nanotube samples were then subjected to an UV cleaning for 5 minutes to make the substrate surface hydrophilic. This time was adjusted to ensure good precursor adhesion as well as keeping the CNTs intact. Following the surface treatment procedure, the samples were introduced to a Cambridge Nanotech Savannah 100 atomic layer deposition chamber. The system ran at a partial pressure of 3×10^{-1} torr, and a deposition time of 5 seconds was used for both precursor and source. Substrate temperature for the HfO_2 deposition was kept constant at 250°C . The Si QD deposition was done in a custom built gas source molecular beam epitaxy (GSMBE) system. The disilane (Si_2H_6) source points directly at the substrate. The base pressure was in the order of 10^{-8} torr, while growth pressure was in the range of 10^{-5} torr. The samples were heated via a Ta heating coil that coupled with the sample holder. Temperature readings were taken by a thermocouple situated between the sample and the heating coil. The source gas flow was controlled using a mass flow controller (MFC) UFC 1660. AFM characterization was carried out using a Veeco multimode AFM.

3.3 Results

3.3.1 Structure description

Figure 3-1(a) shows a schematic of aligned Si QDs on HfO₂ covered CNTs formed by selective epitaxial growth. The QDs are drawn only on the 1-D HfO₂ ridge created by the underlying CNTs. Other QDs could be formed on the surrounding flat surface depending on the magnitude of the length of Si adatom migration on HfO₂ and the proximity of adjacent CNTs. Figure 3-1(b) shows a cross sectional SEM image of a QD alignment sample. The HfO₂ thickness is 6 nm and the ridge height was measured to be 1nm to 1.2 nm by AFM characterization. QDs are clearly observed to align along the 1-D HfO₂ ridge, while QDs are also seen on the flat surface close to the CNT ridge. The QDs on top of the CNT are larger in size demonstrating that more Si adatoms preferentially migrated to the 1-D ridge. We hypothesized that if the density of CNTs is increased, selective growth of Si dots only on the ridges will be evident. The HfO₂ layer is highly conformal on the SiO₂ surface as the shape of the CNT is seen in the SEM image. The CNT surface however is not chemically active¹³ so fewer layers are deposited over the ridge than the rest of the film. This characteristic can be advantageous in a circuit setting by utilizing different thicknesses of the oxide film in between CNT channels¹⁴ as the LOCOS equivalent of isolating oxide.

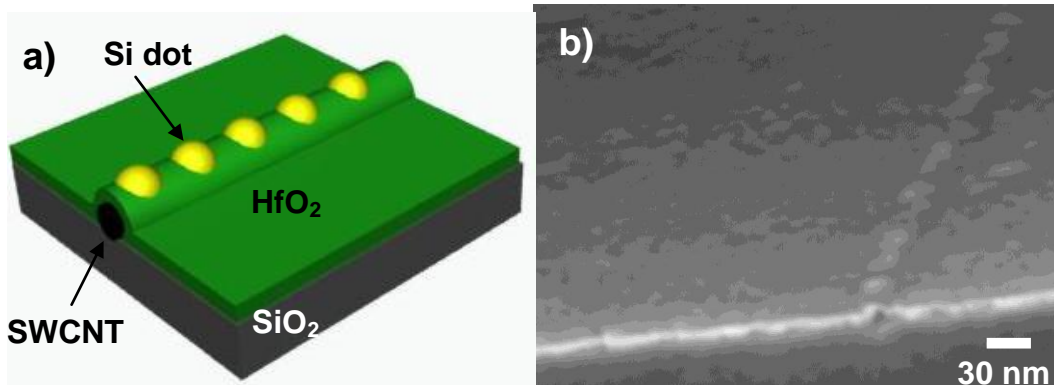


Figure 3-1. Quantum dots on a hafnium oxide covered carbon nanotube. (a) Schematic of a cross sectional view of the structure. (b) SEM image cross-sectional shows aligned QDs on a HfO_2 covered CNT.

3.3.2 Reference sample

To ensure that the observed quantum dots on the surface are Si dots rather than HfO_2 grains due to annealing, an experiment comparing the annealed samples before and after disilane flow was introduced. Figure 3-2(a)-(b) shows the AFM images of these samples. Both samples began with the 6 nm HfO_2 covered CNT. The in-situ annealing including ramping from room temperature to 650°C within 2 hours and maintaining at this temperature for 8 minutes was used for both samples. The control sample which was not subjected to disilane growth shows relatively smooth surface, while the sample with disilane flow of 1.6 sccm for 8 minutes shows rough surface with quantum dot alignment.

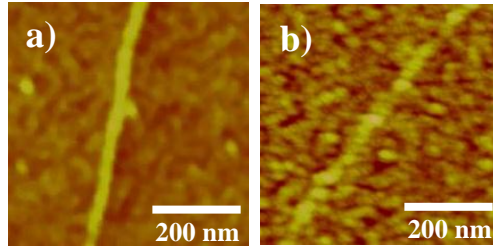


Figure 3-2. AFM images of HfO₂ covered CNT after in-situ annealing, (a) before and (b) after the introduction of disilane.

3.3.3 Flow rate dependence

The growth processes of the selective area epitaxy can be observed clearly through the changes in QD linear density. The QD linear density was obtained via AFM measurement along the CNT ridge. Figures 3-3(a)-(d) show the morphology of the samples grown at different flow rates; a higher rate of disilane flow results in smaller and denser QDs. This is due to the fact that with a higher flow rate there is more source material depositing over the substrate at any given time. More source impingement increases the opportunities for a Si atom to find a high strain point and settle to form a seed, which in turn will form a QD. This behavior has also been observed in QDs grown on HfO₂ patterned surfaces.¹⁰ In contrast, if less Si is deposited then the chances for strain driven alignment are fewer and more QDs start to form over the rest of the substrate as can be seen in Fig. 3-3(a). The size of each image is 200 nm by 200 nm. Due to tip deterioration some of the QDs appear larger in base than the others. Base size is dependent strictly on the size of the ridge created by the CNT since the formation of a

valley at the edges of the CNT is expected to have a greater surface energy. This pattern of size limitation can be seen throughout the different flow rates in the QD growth.

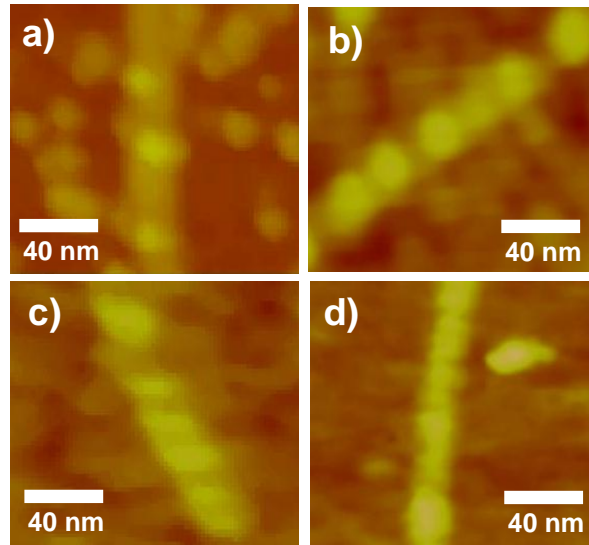


Figure 3-3. AFM image of four samples that were grown at different Si_2H_6 flow rate: a) 1.1sccm, b) 1.6sccm, c) 1.8sccm, d) 2.1sccm.

3.3.4 Growth time dependence

Figure 3-4(a)-(d) show the morphology of the samples grown at different growth time. Coincidentally the effects of time on the linear density resulted similar to the trend observed with varying flow rate the flow rate. The linear density increases with increasing time at the initial stage. For longer growth time, the QD density starts to decrease. The trend of the increase of linear density continues until the QDs exceed a certain size close to the width of the CNT ridge. The edge of the ridge is the threshold for

the QD growth along the CNT. As the QD size reaches that threshold, the strain created by the CNT is compensated and growth past the edges of the 1-D ridges is accelerated.

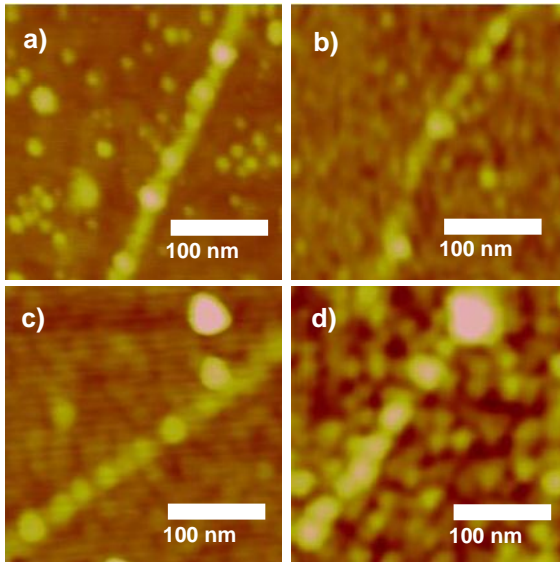


Figure 3-4. AFM images of four samples that have different growth times: a) 3 min, b) 5 min, c) 7 min, d) 8 min.

3.3.5 Growth temperature dependence

Figure 3-5(a)-(d) shows the growth temperature effect on the morphology of the dots on CNT. Interestingly different temperatures have a negligible effect on QD density in the window of alignment. Since growth temperature is known to affect adatom diffusion length^{15,16}, it is reasonable for Si adatoms that are farther from CNT ridges in the initial stages of growth to migrate over to the alignment sites at higher growth temperature. In the examined temperature range, sufficient number of Si adatoms can

migrate to preferential nucleation sites on 1-D HfO₂ ridges on CNTs. Until the strain distribution along the 1-D ridge becomes periodic, this is responsible for periodic aligned QDs. Such “cooperative” regimented growth mode was also observed when Ge dots were grown on 1-D Si ridges⁸. This correlates with our low temperature results (not shown here) that show no alignment due to a low diffusion length. Another reason for a constant density with respect to temperature is that surface desorption of Si adatoms also increases with respect to temperature¹⁰. All of the linear densities are calculated and summarized in figure 3-6.

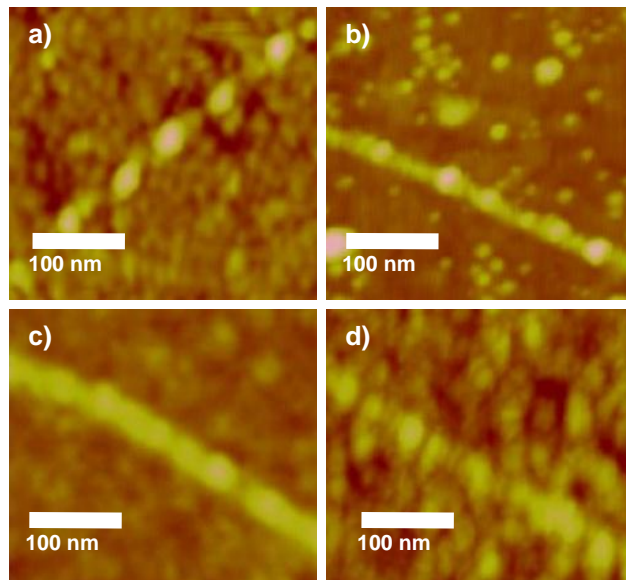


Figure 3-5. AFM images of four samples that have different growth temperatures:

a) 640°C, b) 650°C, c) 670°C, d) 680°C

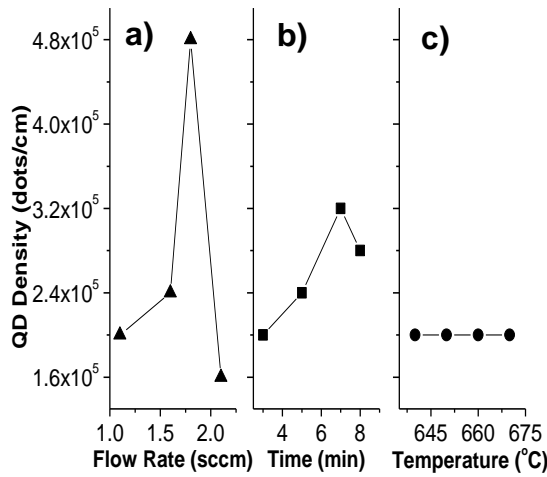


Figure 3-6. Linear density of QDs on CNTs as a function of a) flow rate, b) growth time, and c) growth temperature.

3.3.6 Oxide thickness dependence

To study different strain conditions created by the underlying CNT, we varied the oxide thickness. The effects created by the increase in oxide thickness can be seen in Fig. 3-7(a)-(d). The thicker the oxide is, the sharper QDs are around the CNT ridge. This is due to the relaxation of the strain that forms along the top of the ridge structure. This in turn will decrease the selectivity of Si adatoms, forming more QDs on flat areas of the substrate. Although atomic layer deposition is conformal to most surfaces, CNTs are known to be non-reactive to the H_2O precursor¹³. Therefore many more HfO_2 layers are needed to be deposited to fully cover the CNT and have a smooth surface for good Si migration. The window of selectivity starts close to the 6 nm mark and decreases after 1

to 2 nm depending on the size of the ridge, which is dependent on the diameter of the CNT.

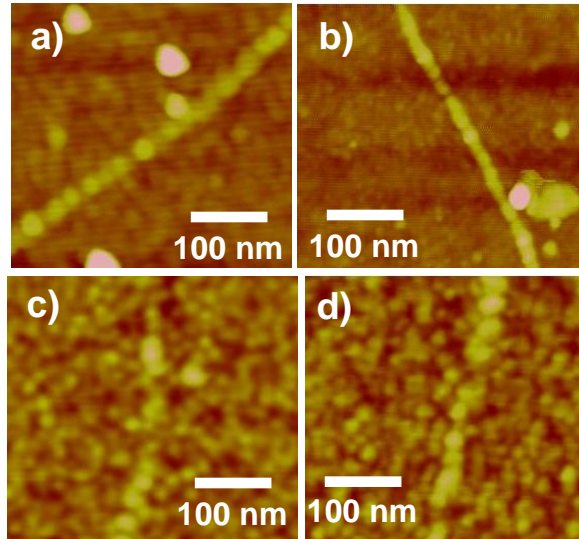


Figure 3-7. AFM images of four samples that have different hafnium oxide thickness: a) 6 nm, b) 7 nm, c) 7.6 nm, d) 8 nm.

3.4 Conclusion

In summary, we have successfully aligned Si QDs on strained HfO_2 covered CNTs. We studied the effects of growth temperature, disilane flow rate, and oxide thickness on the density of the QDs on the 1-D HfO_2 ridges created by the underlying CNTs. We found that the size of the ridge created by the CNT dictates the maximum size of the QDs but the effect is diminished with the increase of the oxide thickness. In addition, the changes in disilane flow rate and growth time showed that the density of the QDs on the ridges can be controlled as well as the QD deposition outside of the ridges.

These results show that the alignment of QDs by a bottom up approach to a size beyond CMOS ultimate limit is possible and controllable.

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Chapter 4: Carbon Nanotube Memory by the Self-Assembly of Silicon Nanocrystals as Charge Storage Nodes

4.1 Introduction

Advances in carbon nanotube field effect transistor (CNT-FET) memory have been achieved in the past decade. Most prominently the charge trapping memory with the CNT exposed to air has shown long memory window stability,¹ robust endurance,² sensitivity to various gases,^{3,4} and even resistive behavior.⁵ Other approaches such as oxide-nitride-oxide (ONO),⁶ nanocrystal(NC),⁷⁻¹¹ floating gate,^{12,13} ferroelectric,^{14,15} and oxide¹⁶ have also been implemented in CNT-based memories. These devices have shown interesting properties such as high speed programming/erasing¹⁶ and single electron detection.^{7,8} Although the use of Au NCs on oxide-covered CNT for memory was reported,⁷ the devices were fabricated based on randomly distributed CNTs. In addition, it remained unclear whether evaporation of Au thin film by electron beam evaporation could give rise to good self-alignment of Au dots on oxide covered CNTs and whether the NCs in the vicinity of the CNTs would add to the memory effect. In this chapter, a memory structure by using self-aligned Si NCs as the charge trapping nodes on parallel-aligned CNTs is demonstrated. The use of parallel-aligned CNTs would enable scalable fabrication, minimize the tube-to-tube junctions, and improve the device performance. Electrostatic force microscopy (EFM) measurements show that the charges on the NCs can be programmed and erased from the CNTs through Al₂O₃ tunneling layer. Furthermore, the device shows both direct tunneling (DT) and Fowler-Nordheim (FN)

tunneling characteristics at corresponding gate voltages, as well as good retention performance.

A major advantage that CNT-based devices have over traditional MOSFET is its superior scalability.¹⁷ The channel width of a CNT is less than 2 nm, and with the addition of discrete NCs the channel length for memory can also be decreased. A characteristic of CNT-based NC memory is that the NCs keep the charge discrete, which can withstand non-uniformities in the thickness of the tunneling oxide caused by CNT roughness. Areas where the CNT bends out of plane causing the tunneling oxide layer to be thinner, would lead to easier charge leakage. If the memory would have been made using traditional poly-Si as floating gate, it would be prone to very short retention because even a single leakage path caused by the CNT roughness would drain all charges on the continuous poly-Si gate. Moreover, NC memory in one-dimensional channels will have what is known as the “bottleneck” effect,¹⁸ for which as few as a single charged NC can keep the device in an ON or OFF state. This means that the ultimate scalability of this memory is limited only to the size of a single NC which in this case is approximately 5 nm.

4.2 Experiment

4.2.1 CNT transfer

The parallel-aligned CNTs were grown on a quartz substrate by the method described in Ref. 19. Then a 100nm Au layer was deposited by e-beam evaporation with a 0.01 nm/s rate for the first 5nm then a 0.1nm/s rate for the rest. A heavily boron doped

Si-p⁺ wafer that had been covered with 300 nm thermally grown SiO₂ was heated to 150°C on a hotplate. The thermal release tape (Nitto Denko Revalpha 3198M tape) was subsequently used to remove the Au/CNT film from the quartz and transfer to the SiO₂ surface. Oxygen plasma at 40 W for 10min was then used to get rid of the tape residue, and finally the Au layer was etched with an Au etchant (Transene Gold etchant TFA). The process is depicted in figure 4-1.

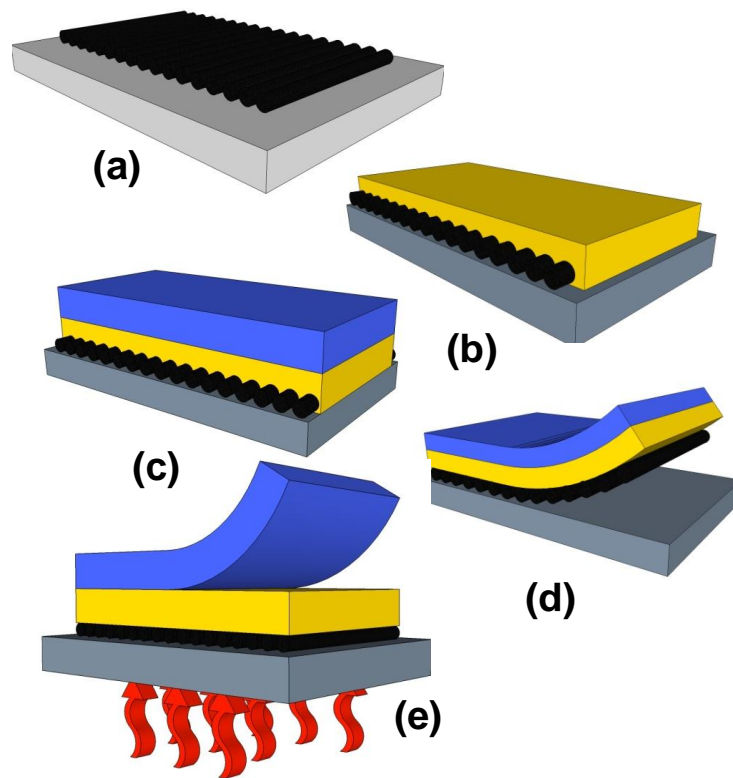


Figure 4-1. CNT transfer characteristics. (a) CNTs grown on quartz; (b) CNTs covered with 100nm Au; (c) thermal tape adhesion and to the quartz substrate and (d) transfer to the SiO₂ substrate; (e) thermal release of the Au/CNT film on the SiO₂ substrate.

4.2.2 CNT-based Si NC memory device structure growth

The CNT on SiO₂ samples were then prepared for ALD growth by introducing them to UV ozone treatment for 10 min to make the sample surface hydrophilic. The ALD sources used were aluminum tetrachloride (AlCl₄) and water (H₂O). The growth was carried out at 300°C under low pressure (2×10^{-2} torr) with a 15 sec interval between each source. A nominal 11nm Al₂O₃ was grown on the sample to act as tunneling layer. The samples were then introduced into a home-built GSMBE system, which was subsequently pumped to high vacuum (1×10^{-7} torr). The sample was heated to 650°C and disilane was introduced at 4 sccm for 5 min. For fabrication of the FET memory devices, a passivation layer of 20nm Al₂O₃ was grown using the same ALD conditions as used for the tunneling layer.

4.3 Results

4.3.1 Growth characteristics

The NC samples started with the growth of parallel-aligned CNTs on a quartz substrate by the method described in¹⁹ and then transferred to a highly boron-doped p⁺-Si[100] substrate with 300 nm thermally grown SiO₂ by thermal tape. The CNT/SiO₂ structure was then introduced to an atomic layer deposition (ALD) chamber for the deposition of 11 nm Al₂O₃ with 0.09 nm/cycle rate at 300°C. The average roughness for the ALD-grown Al₂O₃ surface was measured to be 0.3 nm by atomic force microscopy (AFM), which was slightly larger than the 0.2 nm average roughness of the SiO₂ only samples. This small increase in the film roughness was not found to affect NC growth.

The Al₂O₃ covered CNTs were then introduced to a gas source molecular beam epitaxy (GSMBE) chamber for Si NC growth. Figure 4-2a shows a schematic of the structure and Fig. 4-2b shows an AFM image of a typical sample, which was used for device fabrication. The density of Si NCs is approximately $2 \times 10^9 \text{ cm}^{-2}$. For conventional NC memory applications where two-dimensional cell is implemented, this areal density is too low, however it is acceptable for one-dimensional memory cell as most of the NCs are on the apexes of the CNTs. Similar preferential growth was noticed on the growth of Si NCs on randomly aligned CNTs covered with HfO₂.²⁰

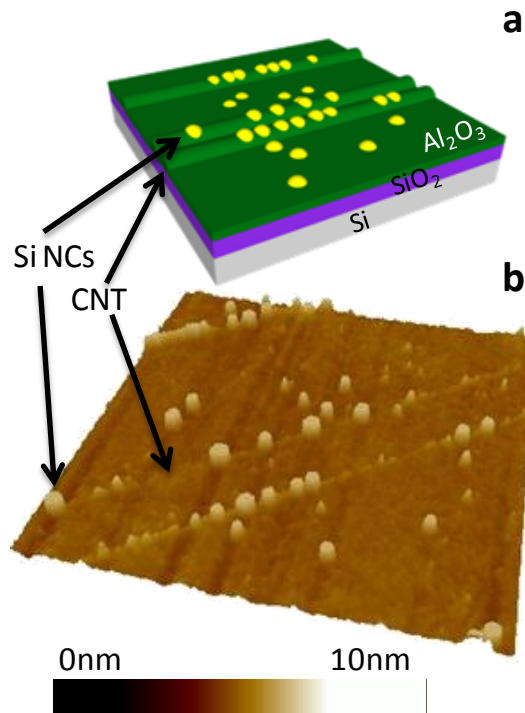


Figure 4-2. (a) Schematic representation, and (b) AFM image of parallel-aligned CNTs after ALD Al₂O₃ deposition and Si NC growth. The image size is 2 μm with average Si NC height of 5nm.

There it was studied how different growth conditions such as growth time, oxide thickness and source gas flow rate influenced the NC density. There are two reasons that may contribute to the preferential growth of the Si dots on the apex of the oxide covered CNTs. The first is related to strain in the Al_2O_3 layer as a result of the CNT underneath it. This strain can be manifested as a change in surface energy, with less energy at the surface of the oxide ridge on CNT; or with an increase in point defects at the areas with strain. The second one is effect from the trapping areas that are formed due to the slower ALD oxide growth on the top of the CNTs. The first reason is inspired by both theoretical and experimental work on single crystal quantum dot structures on patterned dissimilar substrate, showing that places with less surface energy will be preferential areas of nucleation of dots.^{21,22} The second reason is proposed because the growth of Al_2O_3 by ALD uses H_2O as oxygen precursor. This means the precursor cannot attach to the inert CNT so the layer has to overgrow the CNT from the sides. It has been claimed that at least 8 nm is needed to overgrow the CNTs to completely cover them.²³ which is thinner than the 11 nm used here. It can be safely assumed yet that coverage will not be uniform on a CNT that has uneven contact with the substrate and more point defects will be present at the places along the CNT where it is farther from the substrate.

4.3.2 Characterization of Si NC alignment

Si NC preferential growth on Al_2O_3 covered parallel-aligned CNTs was observed. This result is very similar to previous results of Si alignment on HfO_2 covered randomly aligned CNTs.²⁰ Fig. 4-3(a) shows an AFM image of one sample, which was grown at a growth temperature of 650°C and a Si_2H_6 flow rate of 2sccm for 5 minutes. Fig. 4-3(b)

shows an AFM image of the second sample, which was grown at a Si_2H_6 flow rate of 4sccm while other growth conditions were kept the same as the first sample. Fig. 4-3(c) shows an AFM image of the third sample, which was grown at the same growth condition as the second sample except that the growth time was doubled to be 10 min. As the flow rate of the Si source is reduced, the density and size of the Si NCs decreases. The increase of growth time increases both density and size of the Si NCs.

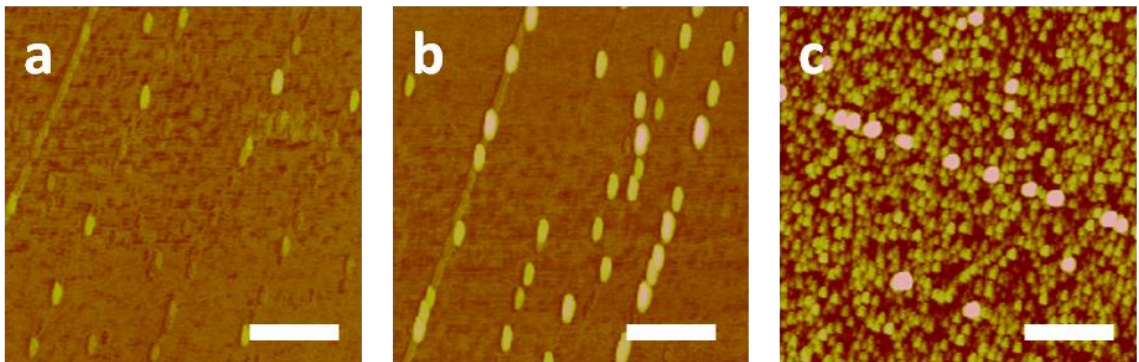


Figure 4-3. AFM images of Si NCs on Al_2O_3 covered parallel-aligned CNTs under the growth conditions of (a) 2 sccm Si_2H_6 flow rate, 650°C growth temperature, 5 min growth time, (b) 4 sccm Si_2H_6 flow rate, 650°C growth temperature, 5 min growth time, and (c) 4 sccm Si_2H_6 flow rate, 650°C growth temperature, 10 min growth time. The scale bar represents 500nm. Preferential alignment of Si NCs is evident in all samples and the density and size of NCs change as the growth condition changes.

4.3.3 EFM results

To detect charging and discharging properties of the NCs compared to the surrounding areas, EFM was used to map the charge distribution across the surface. The EFM measurement consists of a metalized Si tip first measuring the sample topography in tapping mode. Then the tip is raised at a constant height with respect to topography and does a second pass over the same area. The electrostatic force originated from the surface will interact with the tip by changing its resonant frequency. An attractive force lowers the frequency and appears dark in the image, while a repulsive force appears bright. A reading voltage (V_{EFM}) of -3 V was applied at the tip (Fig. 4-4a) during lift to be able to repel any capacitance effect from the CNTs²⁴ and distinguish different types of charges present at the surface. Fig. 4-4b shows the initial state EFM image of a CNT with NCs on top and adjacent to it and the inset shows its corresponding topography. Although aligned NCs are clearly observed in the topographic image, the EFM image shows relatively even contrast due to the lack of charges on the surface. To program and erase the NC/CNT structure, the tip was put in contact with the surface by using the ramp command, which lowers the tip to the point at which the frequency of tip is nullified. This ramp command was tuned to a level of 5 to 10 mV before the tip reached full contact with the surface in order to minimize charge leakage from the dots to the tip and vice versa. These experiments were also carried out in a nitrogen atmosphere to avoid anodic oxidation. While the tip was in ramping mode, a voltage (V_{P}) of 12 V was applied for programming and a -12 V was applied for erasing (V_{E}). In both cases, the total ramping time was 5 seconds. The ramp time defines the amount of time that the tip was in the

ramp routine continuously. Since a 1 Hz ramp rate was used it meant that the tip would only ramp 5 times in the ramping time of 5 seconds. This would account for a total contact time of about 500 ms for which the tip was at the lowest position. The results indicate the change in charge type from a dark CNT and light QDs after programming to bright CNT and dark QDs after erasing. The reason of this change in charge state was the large electric field that is being applied by the tip. At $V_P = 12$ V (Fig. 4-4c-d) the electrons would be attracted from the CNT through the oxide layer and into the NCs. This also happens with other NCs in the nearby area because of the tip size and the electric field distribution on the surface.²⁵ An opposite effect occurs when $V_E = -12$ V (Fig. 4-4e-f) was introduced on the tip, here electrons were repelled and tunnel back from the NCs to the CNT. Since the Al_2O_3 layer outside the vicinity of the CNTs shows little change, *i.e.*, there is no evidence of charge injection outside of the NCs, it can be concluded that Al_2O_3 does not play a major role in the storage of charges. This transfer of charge from a channel, in this case the CNT, to the floating gate, here the Si NCs, is similar to the charge transfer process in a traditional MOSFET based memory.

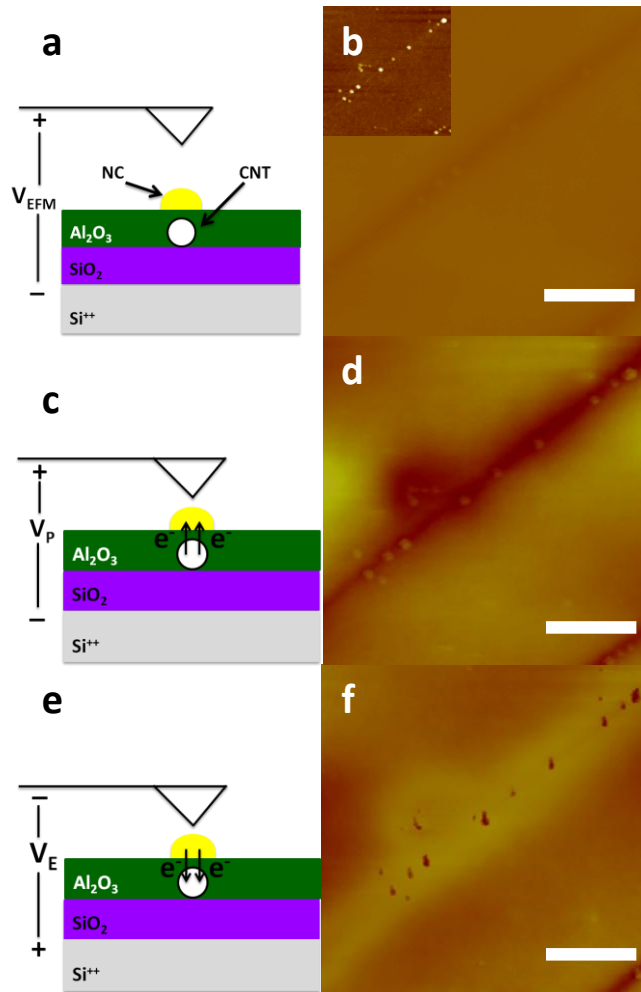


Figure 4-4. EFM characterization of CNT-based Si NC memory. (a) Schematic representation of $V_{\text{EFM}} = -3\text{V}$ applied as reading voltage. (b) EFM image of the initial state of a CNT with Si NCs and the inset shows the corresponding topography. (c) Schematic representation of programming at $V_{\text{P}} = 12\text{V}$ and shows (d) the resulting EFM image. (e) Schematic representation of erasing at $V_{\text{E}} = -12\text{V}$ and shows (f) the resulting EFM image. The scale bar represents 500nm.

4.3.4 Device characteristics

To further study the memory effects of the NC/CNTs structure, back-gated field effect transistor (FET) devices were fabricated. The fabrication began with the passivation of the NCs with 20 nm Al_2O_3 , followed by etching down to the CNTs by photolithography and wet etching. Source and drain contacts consisting of a 5 nm Ti adhesion layer followed by 50 nm Pd layer were then deposited by electron-beam evaporation.

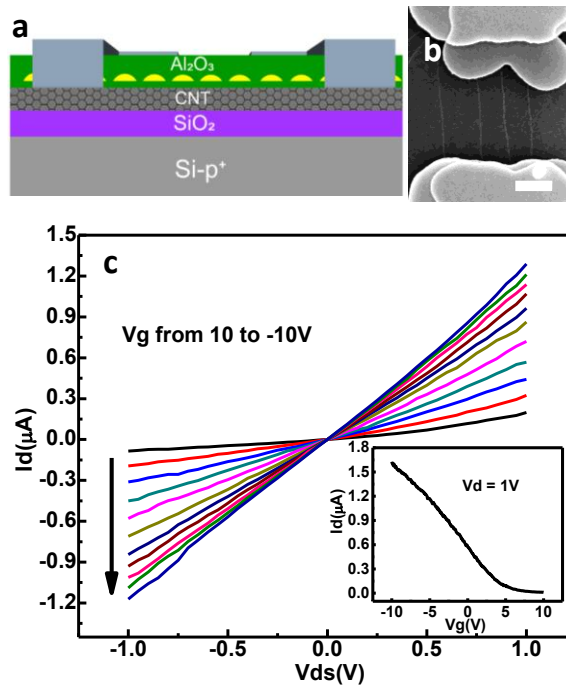


Figure 4-5. (a) Schematic of the fabricated back gate FET device with a passivation layer of 20 nm on top of the Si NCs. (b) SEM image of the CNT-based Si NC memory device after passivation; the scale bar indicates 1 μm. (c) Linear $I_d - V_d$ characteristics under $V_g = 10$ to -10V with -2V step, indicating that the contacts are Ohmic. The $I_d - V_g$ (inset) characteristic suggests that the device is a p-type semiconducting CNT FET.

A second photolithographic step was performed to align the measurement pads to the source/drain contacts and an additional 100 nm layer of Pd was deposited on the resulting pattern. The channel width and length of this device is 5 μm and 3 μm , respectively. Fig. 4-5a shows the schematic of the device and Fig. 4-5b shows a scanning electron microscopy (SEM) image of the fabricated device, which accommodated 4 parallel CNTs as its channel. The linear characteristics of the I_d - V_d curves in Fig. 4-5c indicate that the Ti/Pd contacts used are Ohmic with a current of 862 nA at $V_{ds} = 1$ V and a grounded gate. The inset I_d - V_g curve shows that the CNTs are p-type semiconducting and the current on and off ratio I_{ON}/I_{OFF} is less than 1×10^3 , which is similar to other FETs made with these CNTs.²⁶ Semiconducting characteristics in the CNTs are important because the large on and off ratio will facilitate the characterization of the memory, including an accurate evaluation of the threshold voltage (V_{th}) shift and monitoring of the I_{ON} and I_{OFF} currents as a function of time.

4.3.5 Tunneling characteristics

The change in V_{th} (ΔV_{th}) is tracked to measure the change in memory window. The method of linear extrapolation of I_d - V_g is used to obtain V_{th} , *i.e.*, $V_{th} = V_{gi} - V_d/2$ with V_{gi} being the gate voltage at which $I_{ds} = 0$ A.²⁷ Due to the effect of the fringing electric fields originated from the two-dimensional back gate and one dimensional CNT channel, as well as capacitive coupling between the NCs and the back gate,²⁸ a positive voltage is used for programming while a negative voltage is used for erasing. In programming, V_{th} shows an increase due to the presence of electrons in the NCs. While for erasing V_{th} decreases due to the lack of electrons or the presence of holes in the NCs.

Fig. 4-6 shows the change in V_{th} with an increase of absolute value of V_g . The pulse width used was 1 s with the programming voltage applied first, followed by the erasing voltage. As the pulse amplitude increases, V_{th} increases. At 20 V there is an evident change in slope. This was attributed to two different types of tunneling mechanisms, *i.e.*, direct tunneling (DT) for $V_g < 20$ V and Fowler-Nordheim (FN) tunneling for $V_g > 20$ V. At low V_g amplitudes, charges go through the insulator by DT, leading to the slow increase of ΔV_{th} . As V_g increases, the potential difference between the NCs and CNT channel increases to make the effective tunneling barrier width thinner, allowing more charges to tunnel in FN tunneling mode, as a result, ΔV_{th} increases dramatically. It was calculated that FN tunneling happens when the electric field between the CNT and the NCs is 6.4 MV/cm, which is similar to the reported results that FN tunneling starts on other NCs structures with an electric field of 7 MV/cm.²⁹

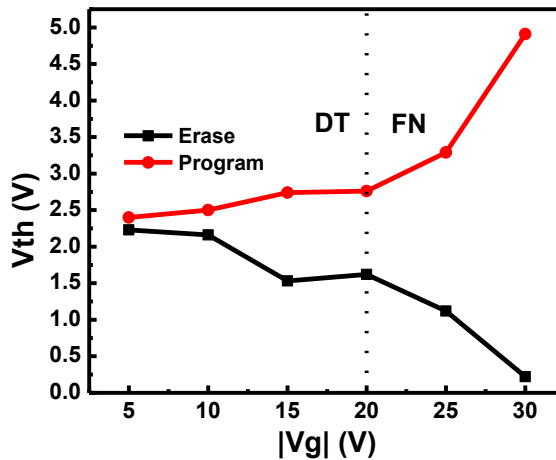


Figure 4-6. V_{th} change as a function of absolute value of V_g . A positive voltage is used for programming while a negative voltage is used for erasing. During the programming and erasing, the pulse width is 1 second while the source/drain are common.

4.3.6 Transient characteristics

Transient characteristics were measured by two ways. For programming and erasing times longer than 1ms, the change in V_{th} was tracked. For times shorter than 1ms, the change in I_d was tracked. Fig. 4-7(a) shows the change in V_{th} at pulse widths longer than 1ms under a writing and erasing gate voltage of +20, and -20V, respectively. The maximum memory window is shown at 1s. Fig. 4-7(b) shows the measured I_d under different pulse widths applied at the gate with a 20V amplitude. A +20V pulse would result in a higher current because the charge stored in the NCs increases the available carrier density in the CNTs and increases the threshold voltage. While a -20V pulse would result in lower current because electrons in the NCs are erased. The shortest pulse width that showed memory effect was 250ns with $I_{ON}/I_{OFF} = 2$.

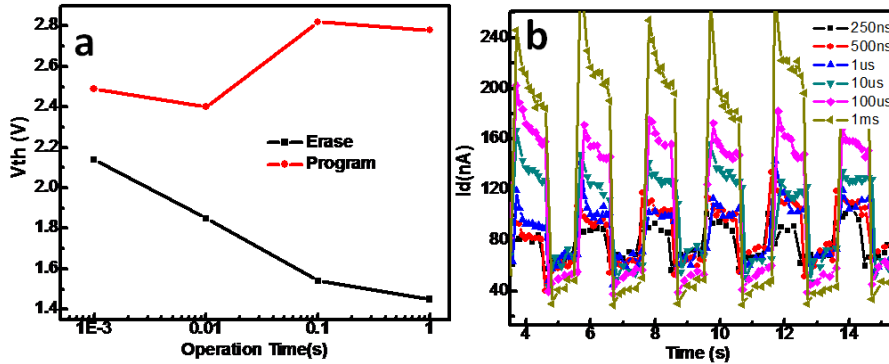


Figure 4-7. V_{th} change as a function of absolute value of V_g . A positive voltage is used for programming while a negative voltage is used for erasing. During the programming and erasing, the pulse width is 1 second while the source/drain are common.

4.3.7 Retention characteristics

Retention characteristics were measured by monitoring I_d for 2×10^4 s as shown in Fig. 4-8a after the device had been programmed and erased, respectively. Fig. 4-8b shows the I_d - V_g curves for the fresh device, programmed device after +30 V for 1 second, and erased device after -30 V for 1 second, respectively, indicating evident memory effect. In addition, the reading gate voltage can be tuned to show the largest window for the ON and OFF state currents. In this case the reading voltage is -2.5 V. The tradeoff is that the device will experience shorter electron retention due to the presence of the constant negative potential on the NCs. This can be avoided if a reading voltage of 0 V is used although in this case the memory window is smaller than that of -2.5 V reading. In Fig. 4-8a the top curve is the retention performance in programmed state while the bottom curve is retention performance in erased state. The retention curve for the programmed state has 2 slopes. The first slope ($\Delta I_d/t$) where t is from the initial to 7×10^3 s has a rapid loss of $\Delta I_d/t \approx -46$ pA/s, which is due to the fast leakage of the stored electrons at the higher energy levels in the NC quantum well or shallow defect levels such as interface trap levels between the CNTs and the surrounding oxide. The smaller slope of $\Delta I_d/t \approx -1.4$ pA/s for the waiting time longer than 7×10^3 s is due to the slower leakage of the stored charges occupying deeper energy levels in the NC quantum well. Hole retention differs from electron retention due to a smaller slope of $\Delta I_d/t \approx 1$ pA/s. This phenomenon is attributed to the higher electron barrier from the CNT to the NCs. Fig. 4-8c shows the band alignment of the device structure. The band gap (E_g) of Al_2O_3 is 8.8 eV.³⁰ This defines an electron barrier of 2.8 eV for electrons at the NC side, which is

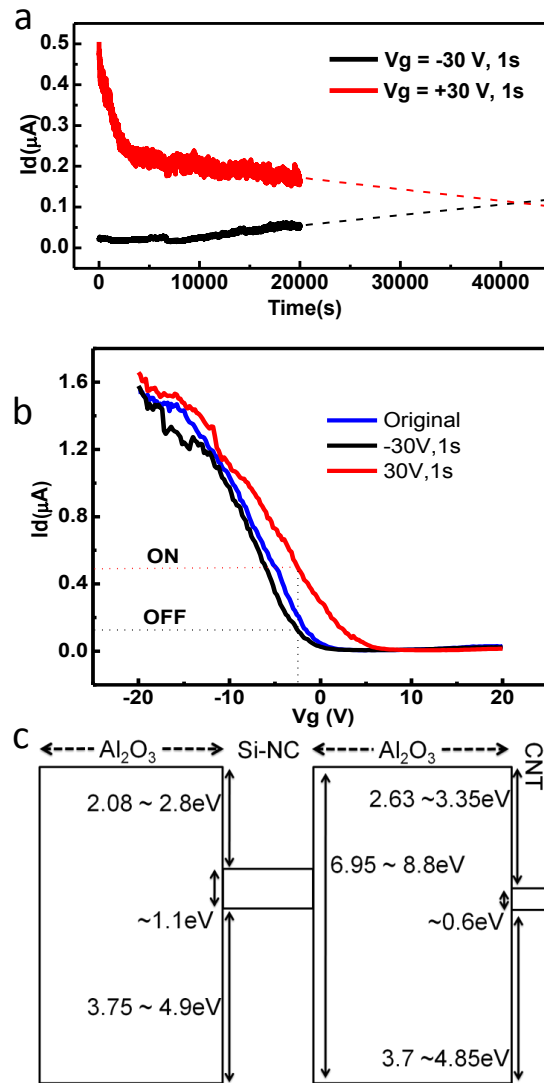


Figure 4-8. (a) Retention characteristics of the CNT-based Si NC FET memory device. Programming and erasing voltages are $V_g = -30\text{ V}$ and $V_g = 30\text{ V}$, respectively. The linear fitting is used to extrapolate the time when all charges are lost to be approximately $4 \times 10^4\text{ s}$. (b) I_d - V_g curves for fresh, programmed, and erased states, showing memory effect. The reading voltage of $V_g = -2.5\text{ V}$ was applied constantly throughout the retention measurement. (c) Band alignment of the CNT-based Si NC memory with

different values for the Al_2O_3 E_g , electron barrier height and hole barrier height depending on the crystalline state of the Al_2O_3 .

indeed smaller than the electron barrier of 3.35 eV at the CNT side. It should be noted that for amorphous Al_2O_3 which is closer to the film grown by ALD, E_g was observed to be 6.95 eV.³¹ This modification shall result in an electron barrier of 2.08 eV at the Si NC side and of 2.63 eV at the CNT side. These values though smaller would still yield the same relationship between the hole and electron retention results. By extrapolating the curve, the retention of this device can be approximately 1×10^4 s when $I_{\text{ON}}/I_{\text{OFF}}$ ratio reaches 10 and 4×10^4 s at the point of complete loss of charge. In contrast, the longest reported retention time for a CNT-based memory by using the time lasted until the $I_{\text{ON}}/I_{\text{OFF}}$ ratio reaches 10 is 1.5×10^4 s.¹⁶ Further extrapolation leads to a retention time of around 3×10^4 s assuming all charges are lost, which suggests the present device has a slightly better retention. Nevertheless, the retention is still short compared with state-of-the-art Si-MOSFET based floating gate memory where the requirement is $\sim 3 \times 10^8$ s. This suggests that there is plenty of room to optimize the CNT-based memory device, such as improving the quality of tunneling oxide.

4.3.8 Reference device

A reference sample without NCs was fabricated together with the CNT-based Si NC memory sample. Fig. 4-9 shows the retention characteristics of the reference device. An initial memory effect with a very small memory window was noticed, however after less than 10s, the entire charge is lost. This small storage is believed to be from shallow trapping levels in the Al_2O_3 .

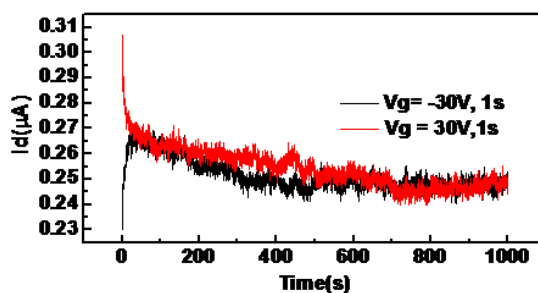


Figure 4-9. Retention characteristics of CNT memory without NCs.

4.5 Conclusion

A memory using Si NC floating gate on Al_2O_3 covered aligned semiconducting CNTs has been demonstrated. EFM measurement results show that the charges are transferred between the CNTs and the NCs in the process of programming and erasing, and are kept discretely in the NCs during the retention. NCs charging characteristics exhibit a change from DT at lower V_g to FN tunneling at higher V_g . Finally charge retention was measured by operating the device continuously and measuring the change in I_d , for which a moderate retention time was achieved. We believe that with further optimization, this technology can enhance the scalability of NC memory. Therefore it may be a potential candidate to replace traditional floating gate memory in the future.

4.6 References

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Chapter 5: Multi-mode Ambipolar Carbon Nanotube Floating Gate Memory

5.1 Introduction

Carbon nanotube (CNT) and graphene electronics have been rapidly evolving and changing the way traditional electronic components are used. Specifically the ambipolar characteristics observed in some small band-gap CNT field effect transistors (FETs) and graphene FETs have been shown to work as amplifiers with frequency doubling¹⁻⁴ and phase shifting capabilities.⁴ These advancements are of great importance because of the possible applications of carbon electronics in the field of radio frequency (RF) electronics. One of the properties that CNTs and graphene electronics have for the application in RF circuits is their high mobility of $230,000 \text{ cm}^2\text{A}^{-1}\text{s}^{-1}$ for suspended graphene in vacuum⁵ and $100,000 \text{ cm}^2\text{A}^{-1}\text{s}^{-1}$ for CNTs.⁶ This value however, is hard to achieve because as graphene and CNTs touch the substrate surface, scattering from the substrate dramatically reduces the mobility. So a problem exists on how to make high mobility graphene/CNT devices without having to suspend them. An answer might be found in floating gate memory. It has been found that graphene covered in nanoparticles (NPs) insulated by a ligand molecule can increase the mobility of the graphene channel by trapping excess charges.⁷ This structure is very similar to a standard floating gate memory. So it is possible that the use of floating gates in carbon electronics could solve the mobility hurdle. Another problem found in the use of ambipolar transistors is the constant addition of various DC voltages to access the different properties of a device. For frequency doubling, for example, the dirac point is expected to be at the lowest point of the signal's amplitude. Unfortunately, this point is dependent on the charge value of

the top- layer/graphene/substrate interfaces and difficult to be controlled. By adding a floating gate, the dirac point can be tuned by programming or erasing charges from it. This will reduce the use of constant DC voltages thus reducing constant stress on the device as well as overall power used in the circuit. In addition arrays of these devices could be then be used as field programmable gate arrays for RF applications. In this chapter we fabricate a floating gate CNT memory with Pt NCs as the floating gate. The ambipolar characteristics of the device as well as the memory characteristics are shown. The use of the device as a frequency doubler is demonstrated by tuning the dirac point with the charge in the floating gate. Also stress on the device is tested by running binary modes in the device to see whether the charge storage is stable under a DC gate bias. These results show that the use of this structure is a viable alternative to standard FET geometries for carbon electronics.

5.2 Experiment

5.2.1 CNT Pt NC memory device structure growth

The aligned CNTs were grown on a pre-patterned quartz substrate and then transferred to a SiO₂ surface by a thermal release tape method. For more details see.⁸⁻⁹ After transfer the samples were prepared for ALD growth by using UV ozone exposure for 10 min to make the sample surface hydrophilic. The ALD sources used were aluminum tetrachloride (AlCl₄) and water (H₂O). ALD growth was done at 300°C under low pressure (2×10^{-2} torr) with a 15 sec interval between each source. First an 11nm

Al_2O_3 was grown on the CNTs to act as tunneling layer. Then a layer of 0.2 nm of Pt was deposited by e-beam evaporation. This would be the floating gate layer. Afterward the samples were introduced into a rapid thermal annealing chamber and annealed at 800°C for 30s to form the NCs. After NC formation a passivation layer of 20nm Al_2O_3 was grown using the same ALD conditions as used for the tunneling layer.

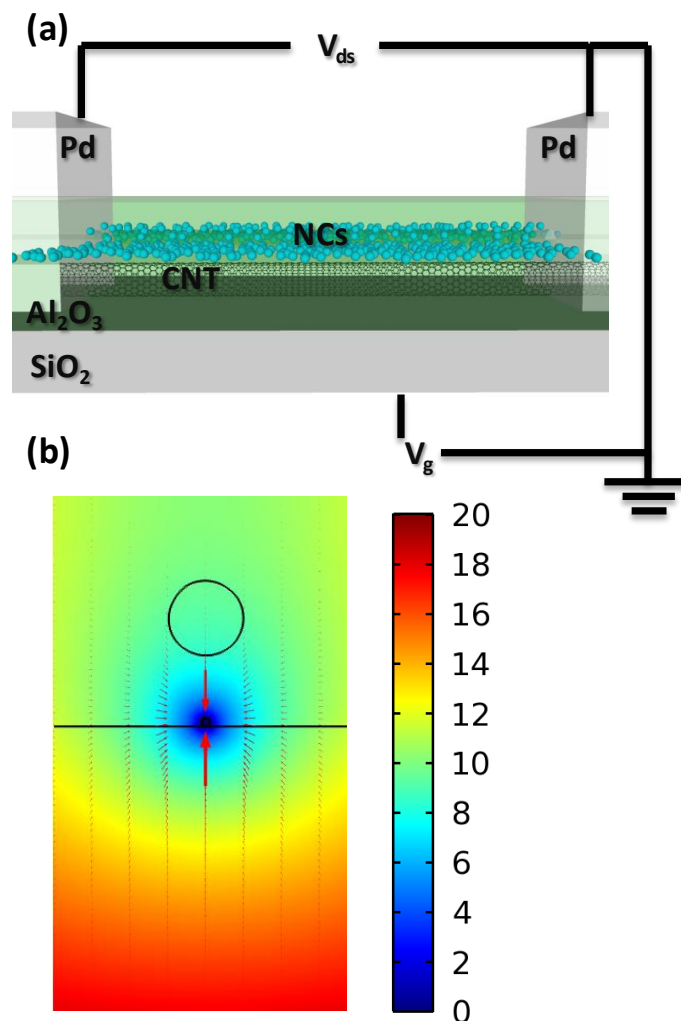


Figure 5-1. (a) CNT FET with NC floating gate structure. (b) Electrostatic simulation of 20V V_g on the CNT/NC structure.

5.3 Results

5.3.1 Device structure

After all the layers were deposited, fabrication started by patterning/etching the source and drain contacts by photolithography then wet etching. A 10nm/50nm Ti/Pd contact layer was then deposited. The pads were subsequently aligned to the contact layer and a 100nm Pd layer finalized the fabrication. Figure 5-1(a) shows the device structure. A back gate was used both for FET operation as well as programming and erasing routines. As shown in Figure 1(b) a simple electrostatic simulation of the CNT at ground and the backgate at 20V shows the fringing field lines of the device under programming. The effect is similar to a top gate device because the field between the CNT and the NC is the same direction as a top-gate geometry.

5.3.2 FET characteristics

The I_d - V_g characteristics of the FET device, shown in fig. 5-2(a) at different V_g sweep ranges, show clear ambipolar characteristics with a ratio $I_{ON}/I_{OFF} \approx 2$. Indicating that the CNTs have a small band gap.¹ The larger sweep range increases the size of the memory window. As the sweep starts from negative to positive V_g , I_d decreases behaving like a p-type transistor until the initial dirac point is reached. This point has a relation to the initial V_g as well as the initial charge already in the oxide/nanocrystal structure. After V_g passes the dirac point I_d increases in value behaving like an n-type transistor. As the sweep returns from the positive V_g the dirac point shifts to the right due to programming of electrons from the CNT to the NCs as V_g has a positive value. The inset shows the SEM image of the NCs on top of an oxide covered CNT. Figure 5-2(b) is

a plot of the V_g values taken at 100nA from the p-type curve showing the increase in the hysteresis window with larger V_g sweep values. Similar characteristics were observed on graphene FET devices with metal NC floating gates,¹⁰ which add to the possible application of these results on both technologies.

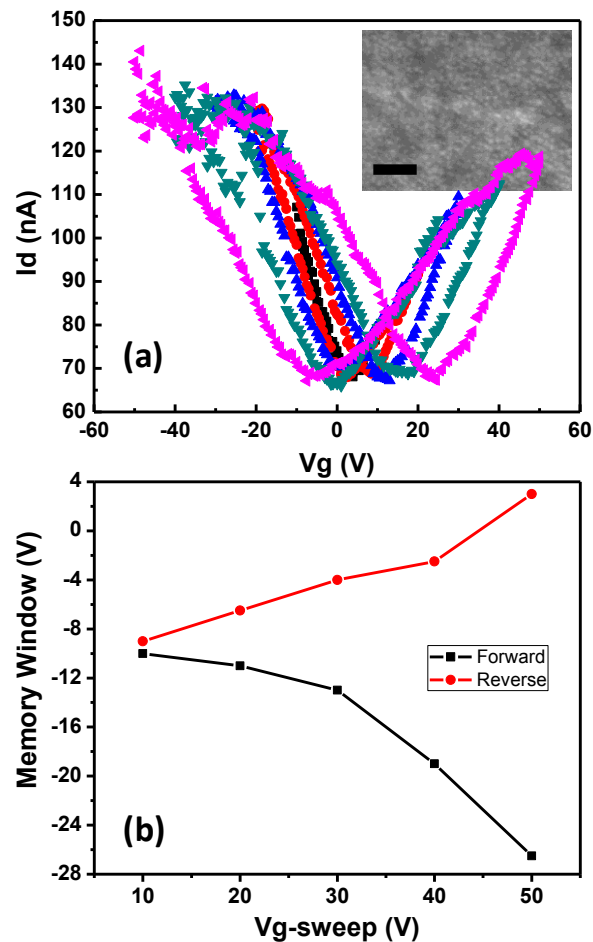


Figure 5-2. (a) I_d - V_g sweep characterization with increasing V_g sweep values. The inset shows the SEM picture of Pt NCs on top of oxide covered CNTs. (b) Memory window voltage characterization taken at $I_d=100$ nA with increasing V_g sweep values.

5.3.3 Signal response

Figure 5-3 shows the current response of the FET device to a sinusoidal signal input of 2Hz frequency and 20V_{pp} to the gate. The initial response shows that the current signal is in phase with the input. This indicates that the dirac point is already shift past 10V due to positive charges in the structure. After a 50V pulse for 1s, the device shows rectifying properties. This is due to the shape of the current response of an ambipolar FET device. This property can also be interpreted as frequency doubling³ and it can be very useful in RF applications. The erasing process consists of -50V pulse for 1s which brings the device back to n-type.

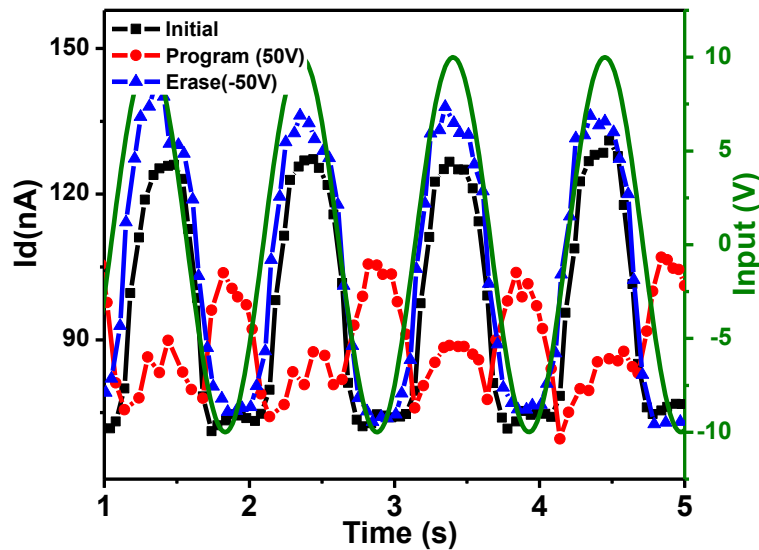


Figure 5-3. Id change over time with a sinusoidal input at the gate.

5.3.4 Binary signal response

To test the performance of the charge layer and add real world applications to the device a DC bias was added to the signal. This presented the opportunity to test both stability of the charge stored in the NCs under a DC bias as well a binary frequency shift keying of the ambipolar FET. Figure 5-4(a) shows the device after erasing with a -50V pulse for 1s. The signal input for this measurement is the same sinusoidal signal as fig. 5-3 with the addition of a binary DC bias that moves the sinusoidal signal by $\pm 10V$.

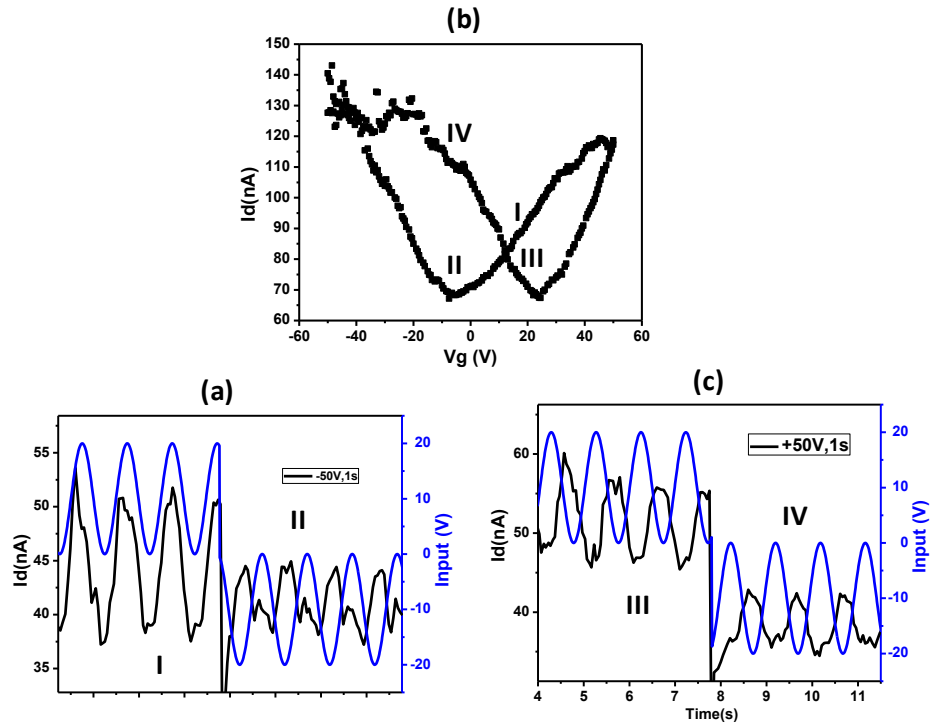


Figure 5-4. (a) I_d response over time to a binary sinusoidal signal after the NCs had been erased. (b) I_d - V_g sweep showing the points of measurement for the programmed and erased states. (c) I_d response over time to a binary sinusoidal signal after the NCs had been programmed.

At +10V the wave signal goes from +20V to 0V the resulting current response is in phase with signal indicating that the device is being swept in the n-type region. For the -10V DC bias the resulting signal is rectified, indicating the device is in the dirac point region. Fig. 5-4(b) indicates the points in the I_d - V_g curve at which the device is being biased. The results from figure 5-4(c) show the binary device performance after programming. As expected the device curve moves to the right and the dirac point in this case is out of the range of the positive bias. So both curves show the p-type characteristic of the device.

5.4 Conclusion

In summary we have shown that NC floating gate memory based on ambipolar CNT FETs can be used in RF applications. The advantages of having a floating gate were observed when the dirac point was shifted near 0V so that multiple modes of the ambipolar characteristics were able to be accessed. The memory characteristics show that with larger V_g the memory window increases giving to all three modes of ambipolar operation. Lastly, it was shown that the charge from the floating gate was stable enough to perform under binary conditions.

5.5 References

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Chapter 6: Resistive Switching in Single Epitaxial ZnO Nano-Island

6.1 Introduction

Resistive random access memory (RRAM) has been attracting attention for high-density, high-speed, and low-power non-volatile memory technology owing to its simple structure, high-density integration, low-power consumption, fast operation and strong potential for fabricating multilevel-per-cell memories.¹⁻⁵ RRAM based on various oxides including NiO,⁶⁻¹¹ TiO₂,¹²⁻¹⁶ CuO,¹⁷ CoO,^{18, 19} ZnO,²⁰⁻²² and others^{2, 23-25} have been widely investigated. Among numerous theoretical models proposed for explaining the resistive switching behavior, the formation/rupture of filaments consisting of oxygen vacancies or metallic ions in the insulating matrix was believed to be responsible for the resistance switching of both macroscopic and microscopic oxide RRAM devices.^{2, 6, 7, 9, 10, 13-19, 23, 24} However, the microscopic details of the ion migration during electroforming, SET and RESET processes still need to be clarified, especially for the conducting filaments consisting of oxygen vacancies. Furthermore, whether this model is applicable for resistive switching in nano-scale devices with sizes on the order of several to several tenth nanometers remains unclear.

While it is important to study the switching mechanism for understanding the scalability of RRAM, it is crucial to reliably fabricate and characterize RRAM cells with a size beyond the limitation of state-of-the-art lithography length scale. Toward scaling down the size of the memory devices, the bottom-up self-assembly of nanowires emerges as a popular method.^{11, 12, 26} For example, Nagashima *et al*²⁶ demonstrated multi-state resistive switching memory effect in a single cobalt oxide nanowire. However, the

memory window for nanowire device is usually less than 10^3 . In addition, the switching voltages are also very high. These results are partly due to the fact that the distance between the two electrodes is usually larger than 100nm. In order to achieve large memory window and low switching voltage, it is necessary to keep the distance between the two electrodes (top and bottom contacts in metal/insulator/metal structure case) to be less than 50nm. In this chapter, ZnO single-crystal nano-islands with base diameters of 20~60nm and heights of about 40nm, which have suitable structure for improving memory performance and understanding the mechanism at the nano-scale, were self-assembled on silicon substrates. Conductive atomic force microscopy (C-AFM) was used to study these nano-islands, virtually forming nanoscale devices with a small distance between top electrode (C-AFM tip) and bottom electrode (substrate), which is the height of the nano-islands. Bipolar resistive memory effect with memory windows on the order of 10^7 for single ZnO nano-island is demonstrated. The mechanism of the switching behavior and the ion migration during switching processes in the nanoscale resistive memories are discussed in detail.

6.2 Experiment

Self-assembled ZnO single-crystal nano-islands were grown on pre-cleaned p^+ -Si (100) substrates at 350°C in a radio frequency plasma-assisted MBE system. Electrical characterization utilizes Agilent 4155C semiconductor parameter analyzer to apply sweeping voltages and obtain *I-V* characteristics. For the C-AFM measurements, a Veeco Dimension Icon AFM with C-AFM capabilities is used. Both measurement systems are

connected to the tip through a manual 3-way switch so that they can be easily switched without interference with each other during measurements. The tip is Co/Cr coated. The radius of curvature of the C-AFM tip apex is 20-50nm. The typical diameter of contact area between the tip and a ZnO nano-island during *I-V* characterization is less than 20nm, while during C-AFM map it is about 5.2nm, estimated using DMT model.²⁷⁻²⁹ *I-V* characterization for state switching was done when the tip, acting as top contact of the nano-scale resistive memory cell, was fixed in the center of ZnO nano-island with the Si substrate grounded. The C-AFM images were measured immediately after state-switching to obtain current distributions for four states (initial, electroformed, ON and OFF) of the ZnO nano-island resistive memory. SEM, EDX, HSR-AES, and AES elemental map were utilized to study the layer coated on the C-AFM tips during the *I-V* characterizations. The cross-sectional TEM specimens were prepared using FEI Quanta 3D FEG dual-beam focus ion beam instrument at UCI (Calit2 microscopy center). The original sample surface was protected by a carbon layer and an electron beam-induced Pt layer. Bright-field and dark-field TEM images as well as selected area electron diffraction patterns were obtained using FEI CM-20 TEM operated at 200 kV with a LaB6 filament. The high-resolution TEM images were taken in a FEI Titan TEM operated at 300 kV with an image Cs-corrector.

6.2.1 ZnO growth conditions

Self-assembled ZnO single-crystal nano-islands were deposited on p⁺-Si (100) substrates in a plasma-assisted molecular-beam epitaxy (MBE) system. Si substrates were cleaned using conventional RCA cleaning process³⁰ as follows. The first step (called SC-

1, where SC stands for Standard Clean) was performed with a 1:1:5 solution of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and water (H_2O) at $80\text{ }^\circ\text{C}$ for 10 minutes, which resulted in the formation of a thin silicon dioxide layer (about 1nm) on the Si surface, along with a certain degree of metallic contamination that would be removed in subsequent steps. After SC-1, the wafers were rinsed in deionized (DI) water for 5 minutes. The second step was carried out with a short immersion (1 minute) in a 1:50 solution of HF and H_2O at room temperature in order to remove the thin oxide layer and some fraction of ionic contaminants. The third and last step for RCA cleaning process (called SC-2) was performed with a 1:1:6 solution of HCl, H_2O_2 , and H_2O at $80\text{ }^\circ\text{C}$ for 10 minutes, which effectively removed the remaining traces of metallic (ionic) contaminants. After the SC-2 process, the Si wafers were again rinsed in DI water for 5 minutes, dried by a nitrogen gun, and finally transferred into the MBE system. After the substrate was annealed at $900\text{ }^\circ\text{C}$ for 10 minutes to remove the oxide layer created by SC-2 cleaning step, the substrate temperature was decreased to $350\text{ }^\circ\text{C}$ and ZnO single-crystal nano-islands were grown. During the epitaxy, high-purity Zn (6N) source was evaporated from a regular Knudsen effusion cell and oxygen (5N) plasma generated by a radiofrequency plasma generator was used as the oxygen source.

6.2.2 *I-V* characterization and C-AFM measurement system setup

Fig.6-1 shows a home-designed measurement system setup including a semiconductor parameter analyzer and a C-AFM equipment. With this system, measurements can be easily switched between *I-V* characterization and C-AFM mapping without losing position of the measured nano-island on the sample.

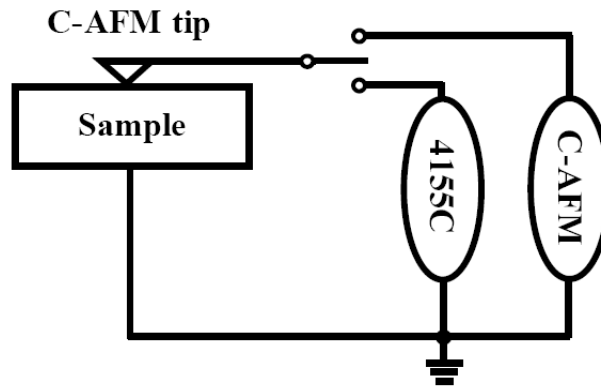


Fig.6-1. Schematic of measurement system setup including an Agilent 4155C semiconductor parameter analyzer and a C-AFM equipment.

6.3 Results

6.3.1 Growth characteristics

Self-assembled ZnO single-crystal nano-islands were grown on Si (100) substrates by plasma-assisted molecular beam epitaxy (MBE). These nano-islands were then characterized using scanning electron microscopy (SEM) and transmission electron microscopy (TEM) techniques. Figs.6-2 (a)-(d) show (a) top-view, (b) cross-sectional SEM images, (c) diameter and (d) height distributions of the ZnO nano-islands. The diameters of these ZnO nano-islands are between 10 and 60nm while the heights are between 20 and 70nm. The density of the nano-islands is about $100/\mu\text{m}^2$. Fig.6-2 (e) is a bright-field TEM micrograph of the nano-islands. The selected area electron diffraction (SAED) pattern (Fig.6-2 (f)) from the area displayed in Fig.6-2 (e) includes diffraction spots from both the Si substrate and ZnO nano-islands. The spots from Si form a network

and six of the spots close to the transmission beam (center of the pattern) are marked with lines. Additional spots result from ZnO nano-islands, which is confirmed by dark-field imaging of the spot marked in a circle in Fig.6-2 (f). The result is shown in the inset of Fig.6-2 (e). The fact that the nano-island is lit up in the inset means the existence of the correlation between the circled spot and the crystal. The scattered diffraction spots suggest that the ZnO nano-islands are in single crystalline form. Moreover, the interplanar spacings can be determined from the distances between these additional spots and the transmission beam. As marked in Fig.6-2 (f), the measured interplanar spacings are consistent with those of ZnO. The orientation relationship between the additional spots and Si-related spots shows that the ZnO crystals are randomly oriented. High-resolution TEM (HRTEM) image shown in Fig.6-2 (g) for one ZnO nano-island provides further evidence that the nano-islands are ZnO single crystals. The inset of Fig.6-2 (g) is a fast Fourier transform (FFT) of the image. The interplanar spacings measured from the image and FFT are consistent with those of ZnO in the zone axis of $[\bar{1}2\bar{1}0]$. AFM was also carried out to confirm the morphology of the ZnO nano-islands (section 6.5.2).

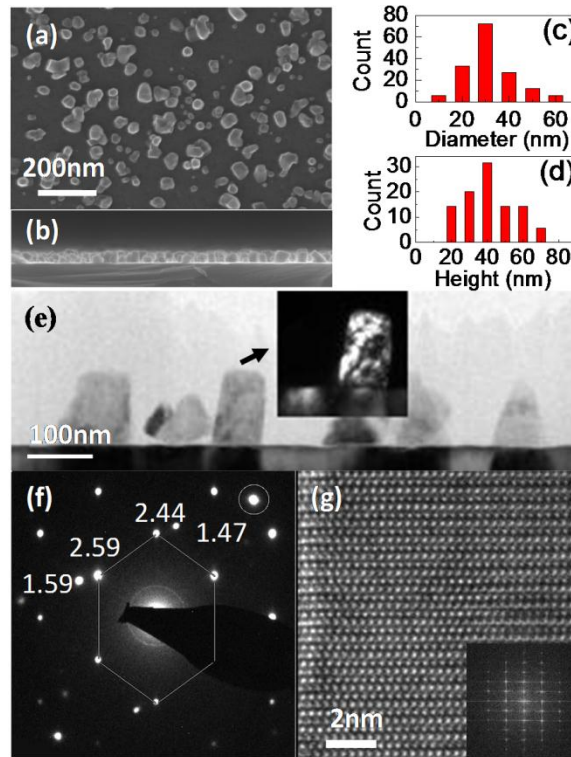


Figure 6-2. (a) Top-view, (b) cross-sectional SEM images, (c) diameter, and (d) height distributions of ZnO nano-islands. (e) Bright-field TEM micrograph of the nano-islands. (f) SAED pattern from the area displayed in (e) including diffraction spots from both the Si substrate and ZnO nano-islands. (g) A HRTEM image from one ZnO nano-island. Inset in (e): A dark-field image recorded with the spot marked in a circle in (f). Inset in (g): A fast Fourier transform (FFT) of the image (g).

6.3.2 Morphology of ZnO single-crystal nano-islands

Fig.6-3 (a) shows an AFM image of ZnO single-crystal nano-islands, which was measured in tapping mode. Only discrete nano-islands were utilized for *I-V*

characterizations and C-AFM measurements. The true width of the nano-island can be calculated according to ³¹

$$D = 2\left(\frac{W^2 + 4h^2}{8h} - R_T\right) \quad (\text{S1})$$

where D is the true width of the nano-island, W is the image width at half maximum height of the nano-island, h is the vertical distance from Si substrate to the top of the nano-island, and R_T is the radius of curvature of the C-AFM tip apex. Typical R_T values of these tips are 20-50nm as specified by the manufacturer. ³² The typical true width of the nano-islands is from 10nm to 60nm using $R_T = 45\text{nm}$, which is the same as the results obtained by top-view and cross-sectional SEM images shown in Fig.6-2 (a)-(d).

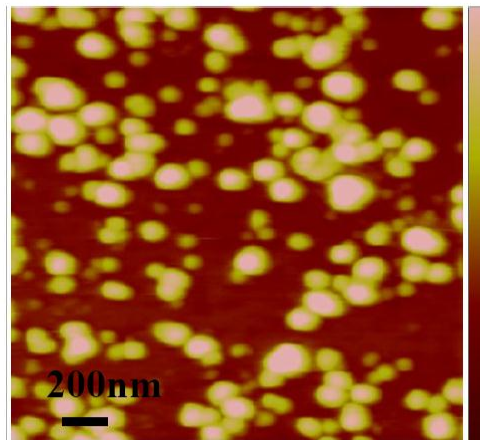


Fig.6-3 AFM image of ZnO single-crystal nano-islands observed in tapping mode.

6.3.3 *I-V* characteristics for ZnO single-crystal nano-islands

For *I-V* measurements, different current compliance (CC) was used for bipolar switching. The results show that only if there is an abrupt current increase in electroforming process for current compliance from 10 μ A to 500 μ A, bipolar switching phenomena will show up for the same or higher current compliance in the subsequent voltage sweeping process. Fig.6-4 (a) shows an example result measured from one nano-island. For this nano-island, current compliance of 10 μ A was used in the electroforming process (CC1). Current compliances of 50 and 500 μ A were used for subsequent voltage sweeping (CC2). Large memory windows can be found for both values of current compliance, which make ZnO nano-scale resistive memory capable for multilevel storage applications.³³ Both set and reset voltages are found to be higher with larger current compliance as a result of the formation of stronger filaments at larger current compliance.³⁴ In this study, most measurements related to C-AFM and *I-V* characterization were conducted in air.

Fig.6-4 (b) shows the room-temperature PL spectrum of ZnO nano-island sample. The spectrum has two emission peaks, centering at 3.3eV and 2.5eV, which are corresponding to the band gap energy of ZnO film and green emission caused by the intrinsic defects of oxygen vacancy.³⁵ Furthermore, the peak at 2.5eV can be divided into two peaks at 2.55 eV (~485 nm) and 2.3 eV (~539 nm), as shown in the figure. Both peaks are commonly ascribed to oxygen vacancies^{36,37}.

Fig.6-4 (c) and (d) show a typical high spatial resolution (HSR)-AES Zn map for a randomly chosen area and SEM image accordingly. The thermal pseudo-color images

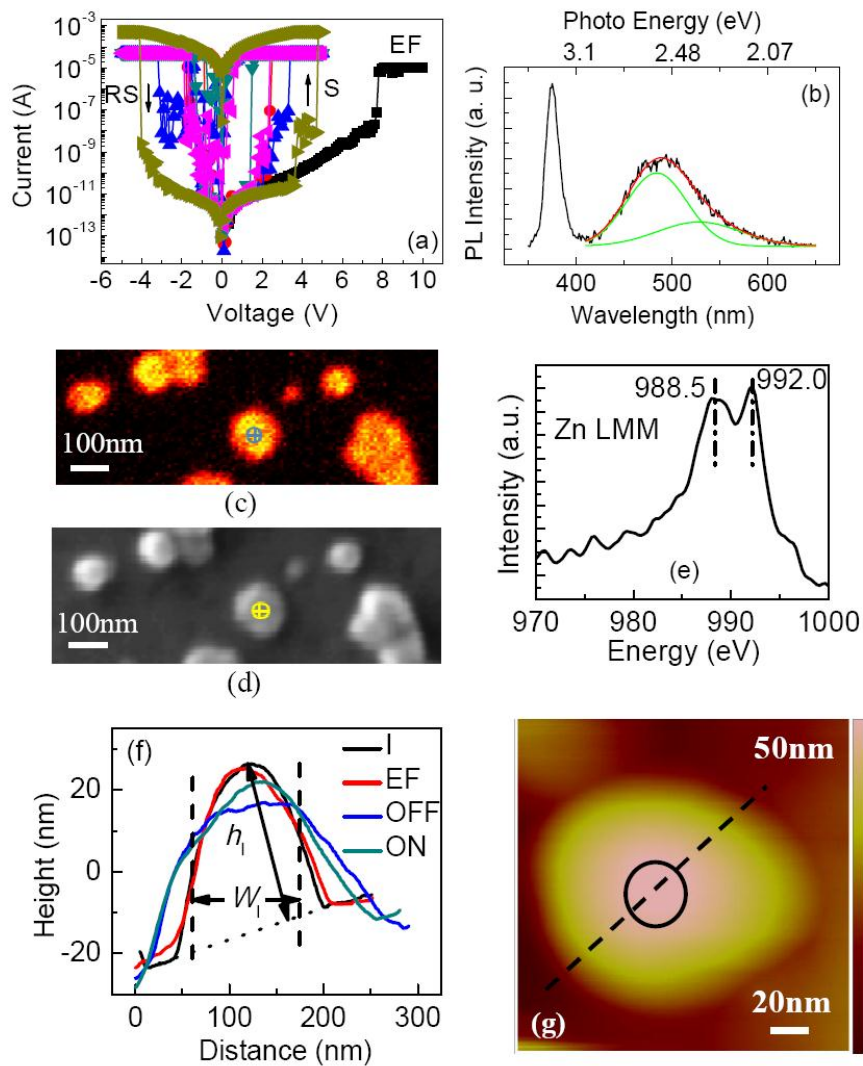


Fig.6-4 (a) Bipolar resistive switching behavior with $CC1=10\mu A$, $CC2=50\mu A$, and $500\mu A$. (b) PL measured at room temperature for ZnO nano-islands deposited on Si substrate. (c) AES Zn elemental map and (d) SEM image accordingly. (e) AES spectra of Zn LMM for the spot in (c) and (d). (f) Height cross-section profiles corresponding to the black dash line in (g) AFM image for four different states.

show relative amounts of Zn with three types of region: (1) the yellow dots are indicative of the highest concentration of Zn, (2) the orange dots are corresponding to the moderate concentration of Zn, and (3) the black dots region is the area where the concentration of Zn is the lowest. Fig.6-4 (e) shows the HSR-AES spectra of Zn LMM for the spot in (c) and (d). Two peaks at 988.5 and 990.2eV can be observed, which are corresponding to the transition energy for Zn in the oxide and elemental form, respectively.

An interesting phenomenon occurred after electrical measurement was a noticeable change in nano-island height and diameter. Fig.6-4 (f) shows the height profiles for four states, corresponding to the position of the dash black line for initial state in Fig.6-4 (g). As seen from Fig.6-4 (f), the height of the nano-island decreased and the diameter increased after electrical measurements. Additionally, after the nano-island was switched from OFF to ON, the height of the nano-island also increased. Note that AFM and C-AFM images for OFF-state were measured before those for ON-state.

6.3.4 Electrical characteristics

Typical current-voltage (I - V) results for the ZnO nano-scale resistive memories are shown in Fig.6-5 (a). An electroforming process is necessary, which occurred at a voltage of approximately +8V under a current compliance of 10 μ A during the first applied external voltage sweeping from 0 to 10V as shown in red circle line denoted as process (1). The presence of a forming process is one of the unique features of the filament model.²⁶ After the forming process, the bipolar resistive switching I - V curve, conducted by an application of voltage cycles ((2): +5V \rightarrow 0V; (3): 0V \rightarrow -5V; (4): -

5V→0V; (5): 0V→+5V), demonstrates high degree of repeatability at both the same (Fig.6-5 (a)) and different current compliance (Fig.6-4 (a)). The behavior of bipolar switching at different current compliance provides the potential application of ZnO nano-island resistive memory in multilevel-per-cell memory.²⁶ The ZnO nano-island resistive memory kept in low resistive state (LRS or ON-state) during voltage sweeping of process (2) and (3). During process (4), a pronounced change of resistance from LRS to high resistive state (HRS or OFF-state) was observed at -0.8V, which is defined as the “RESET” process, and corresponding voltage as RESET voltage (V_{RESET}). Subsequently, an opposite “SET” process with SET voltage (V_{SET}) can be observed as the voltage swept reversely from 0 to 5V (process (5)), evidenced by a two-step switching from HRS to LRS. The first switching occurred between 1.8 and 2.0V. The second one took place at 2.3-2.5V after the resistance of the nano-scale resistive memory stayed at an intermediate state from 2.0 to 2.3V. This kind of two-step “SET” process was even more obvious at higher current compliance as shown in Fig.6-4 (a), which implies another way of multilevel data storage as long as an effective control over threshold voltage could be realized.³⁸ A similar two-step “SET” process was also observed by Kim *et al* in TiO₂ systems,³⁹ in which filamentary switching *via* partial rupture and recovery of the ruptured portion of filaments were used to explain the two-step “SET” process.

The memory window defined by the two resistance states,

$$(R_{\text{OFF}} - R_{\text{ON}}) / R_{\text{ON}} \sim R_{\text{OFF}} / R_{\text{ON}} \quad (1)$$

is more than 10^6 over a large range of reading voltage (-0.4V~-0.1V and +0.1V~+1.7V) from Fig.6-5 (a). The large memory window would allow a periphery circuit to very

easily distinguish the information stored in ON- and OFF-state. It is also beneficial for fabricating multilevel memory through using different current compliance.

Fig.6-5 (b) shows that ON-state I - V curve can be well fitted with linear fitting, in which the reverse of slope, about $10^4 \Omega$, is the resistance of the ON-state resistive memory. This linear I - V relationship clearly exhibits an Ohmic conduction behavior, which is caused by the formation of conductive metallic filaments in ZnO nano-island during the SET process. Similar result was reported by Yang *et al* in RRAM device based on ZnO:Mn thin film.³⁸ In the mean time, I - V curve is similar to that of a practical diode for OFF-state (HRS), as shown in Fig.6-5 (c). The Si substrate here serves as the p-type material in the heterojunction diode system, which is composed of C-AFM tip, n-type ZnO nano-island, and p⁺-Si substrate. ZnO serves as the n-type material in which oxygen vacancy should be the intrinsic donor of the electron carrier because ZnO nano-islands were deposited in a zinc-rich condition. Under negative bias, the system is a forward biased diode. The conduction mechanism is dominated by three kinds of current as shown in Fig.6-5 (c): (1) recombination-generation current; (2) the diffusion current; and (3) the diffusion current at high-level injection. The I - V curve can be described by

$$I = I_s(\exp(qV/nkT) - 1) \quad (2)$$

where I , I_s , V , kT , q , and n are the junction current, saturation current, applied voltage, thermal energy, magnitude of electronic charge, and the fitting factor for different dominated current mechanism, respectively.⁴⁰ When positive bias is applied, the system is a reverse biased diode. Reverse leakage current is due to generation-recombination and

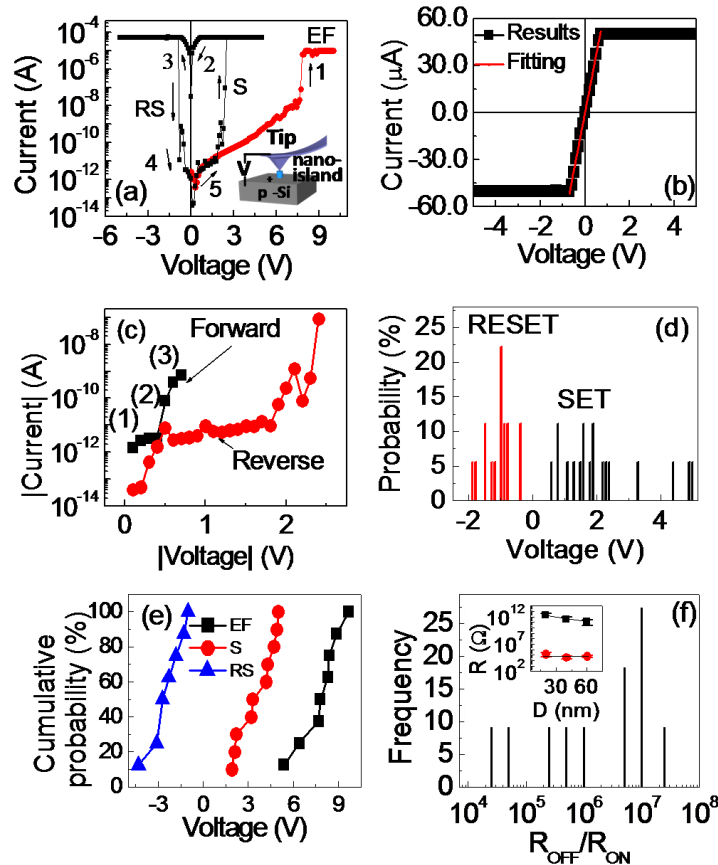


Figure 6-5. (a) Typical I - V characteristics of a ZnO nano-island resistive memory. Inset: schematic illustration of the experiment setup for switching a ZnO nano-island with C-AFM tip. (b) The linear fitting for the I - V curve of the LRS. (c) I - V curve in semilogarithmic scale for the HRS. (d) Typical V_{SET} (black) and V_{RESET} (red) distributions of different cycles for one nano-scale resistive memory. (e) Distributions of electroforming (EF), SET (S), and RESET (RS) voltages for different ZnO nano-island resistive memories. (f) Histogram of $R_{\text{OFF}}/R_{\text{ON}}$ for different nano-scale resistive memories. Inset: The relationship between resistance and diameter of the ZnO nano-islands for both ON- and OFF-states.

surface effects. The junction breakdown is corresponding to the “SET” process, which forms the filamentary conducting paths.²⁵

Fig.6-5 (d) shows distributions of SET and RESET voltages (V_{RESET} and V_{SET}) for different sweeping cycles performed on single ZnO nano-island resistive memory, in which if a two-step SET or RESET process happened, the voltage for the first one was utilized for statistics. V_{RESET} and V_{SET} distribute in the ranges of -0.4 to -1.9V and 0.6 to 5.0V, respectively. V_{SET} distribution shows much more scattering than that of V_{RESET} , which is another piece of evidence that conducting filaments play a crucial role in bipolar resistive switching characteristics in ZnO nano-scale resistive memories. According to the conducting filament model,^{38, 41} during filament formation and rupture process, the formation of a filament (SET) should be more random than the destruction of an existing filament (RESET), because the formation process is determined by the competition among different filamentary paths. Therefore larger variations in V_{SET} than in V_{RESET} should be expected, which is also validated in other oxide systems.^{42, 43}

The I - V measurements depicted previously were conducted on dozens of similar nano-islands. A new C-AFM tip was used for every single nano-scale resistive memory measurement to avoid effects caused by the change of the tip happening during I - V characterization. During these measurements, similar I - V characteristics as shown in Fig.6-5 (a) were obtained. Fig.6-5 (e) and (f) show distributions of electroforming, SET, RESET voltages, and memory window $R_{\text{OFF}}/R_{\text{ON}}$ for these measured ZnO nano-island resistive memories, respectively. Data for V_{SET} , V_{RESET} , and $R_{\text{OFF}}/R_{\text{ON}}$ are those of first voltage sweeping loop after electroforming. The electroforming voltage (V_{EF}) distributes

between 5.4 and 9.7V, while V_{SET} and V_{RESET} are in the range of +1.9 ~ +5V and -1 ~ -4.3V, respectively, according to cumulative probability results shown in Fig.6-5 (e). These voltage ranges are reasonable because the crystal orientation, oxygen vacancy density, diameter and thickness of the measured ZnO single-crystal nano-islands are slightly different from one to another. From the results of $R_{\text{OFF}}/R_{\text{ON}}$ frequency for different measured nano-scale resistive memories as shown in Fig.6-5 (f), the memory windows are no less than 10^6 for over 70% ZnO nano-scale resistive memories. Resistance ratios between OFF- and ON-state are several orders larger than reported ones based on undoped ZnO materials with sizes of μm^2 .⁴⁴ The nano-island size effect on RRAM switching behavior was also studied. All nano-islands between 20nm and 60nm have similar switching behavior while the R-ratio increases with the decrease of the nano-island size from 60nm to 20nm, as shown in the inset of Fig.6-5 (f). There is no obvious relationship between the ON-state resistance and size of nano-islands. However, OFF-state resistance decreases slightly with the increase of the nano-island size, similar to the reported results of RRAM at micro scale.⁴⁵

6.3.4 Retention and endurance

A DC sweep was used to measure the endurance of the nano-island devices. It should be noted that a sudden increase of voltage will change the distance between tip and island greatly, therefore it is not reliable to obtain endurance results by set and reset pulses. Typical results are shown in Fig.6-6 (a). After 48 cycles of sweep, the device would not turn to the ON state anymore and the measurement was terminated. The

retention measurement was performed in air first. It is found that OFF state is a stable state while ON state is sustained for only about 100 seconds.

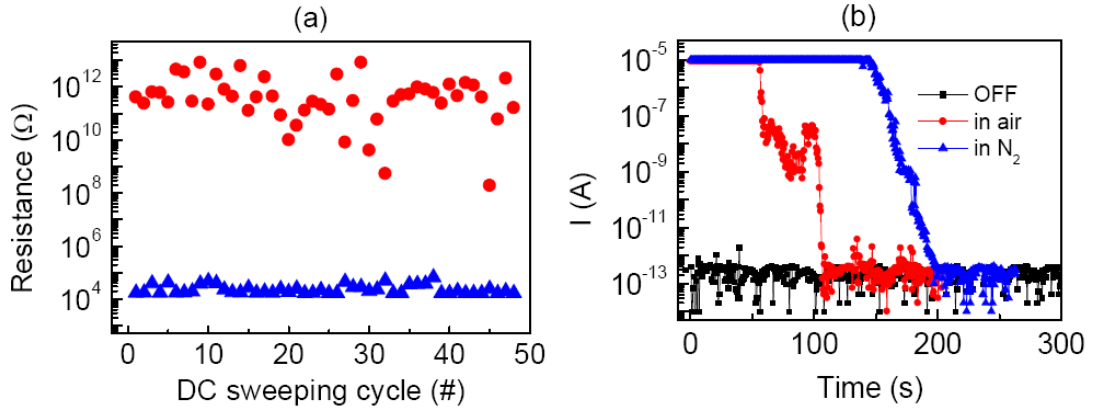


Fig.6-6 (a) Endurance and (b) retention results of ZnO nano-island.

Both phenomena were caused by the oxidation of filaments in air. This was confirmed by the longer retention results measured in N_2 , as shown in Fig. 6-6 (b), where the filaments retain longer because there is oxygen-deficiency near the nano-island. In other words, the results of retention and endurance results should be worsened by the situation that the nano-islands were not passivated from the environment. The role of passivation in resistive switching can also be found in the results investigated by Oka et al.⁴⁶ This result indicates that the retention and lifetime may not be a problem if the nano-islands could be properly passivated, which needs further investigations.

6.3.5 CAFM measurements

To clarify the operation mechanism of the nanoscale resistive memories, current distribution of single nano-island at the four different states was mapped using C-AFM.

Fig.6-7 shows a typical topographic image of a ZnO nano-island resistive memory (Fig.6-7 (a)) and its C-AFM images, showing local current distributions for different states of initial (Fig.6-7 (b)), electroformed (Fig.6-7 (c)), OFF (Fig.6-7 (d)), and ON (Fig.6-7 (e) and (f)), which were measured immediately after switching. During electroforming, SET, and RESET processes, which were completed by sweeping applied voltage (process (1) to (5)), the conducting tip was fixed in the center of the ZnO nano-island (the circle positions of the images in Fig.6-7). In addition, all C-AFM images were obtained with a bias of -2.0V applied to the tip, which did not change the initial state of the measured nano-islands as evidenced by the substantial number of measurements. In the initial state, current is almost evenly distributed in the whole area of the nano-island, at a level of about 20pA as shown in Fig.6-7 (b). This current is attributed to oxygen vacancies, which act as donors in ZnO materials.⁴⁷ The existence of oxygen vacancies was proven by a deep level peak of around 2.5eV in the photoluminescence (PL) spectrum⁴⁸ and metallic Zn peak at 992.0eV in high spatial resolution Auger electron spectroscopy (HSR-AES)⁴⁹ shown in Fig.6-4. After electroforming (Fig.6-7 (c)), the current, with the highest value of 40pA, is mainly distributed around the edge area of the nano-island, while the center area is highly resistive. In order to ensure that the bias of -2V during the C-AFM measurement will not RESET the nano-island from ON-state to OFF-state, the current compliance was increased from 50 μ A to 500 μ A, which elevates the RESET voltage to as high as -4V, as shown in Fig.6-4 (a). From Fig.6-7 (d), it is obvious that the whole nano-island was switched to OFF-state after the RESET process. After the SET process, the nano-island was switched back to ON-state as shown in Fig.6-7 (e). These results show that the size

of the actual working memory cell depends on the size of the nano-island in the ZnO nano-island resistive memory case.

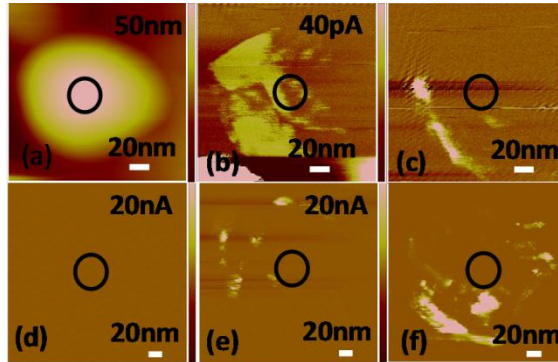


Figure 6-7. (a) AFM height image recorded in air on a ZnO nano-island on Si substrate for initial state. (b) ~ (f) Local current distributions of a nano-scale resistive memory for four different states: (b) initial, (c) electroformed, (d) OFF, and (e)-(f) two ON-states.

The ZnO nano-island was switched between ON and OFF states for several times. The C-AFM images were also recorded each time and Fig.6-7 (f) shows another ON-state image. Comparing these images such as Fig. 6-7 (e) and (f), it was noticed that every time when the nano-island was switched to ON state, the position of the higher current spots changed, which proves that during the SET process, there is competition among different filament paths, as evidenced by the distribution trait of V_{SET} and V_{RESET} in Fig.6-5 (d). It can also be obtained from C-AFM images of ON-states that the size of high

current spots can be smaller than 5nm, which show the potential of scaling down the device to 5nm.

An interesting phenomenon occurred after electrical measurements was a noticeable change in nano-island height and base diameter as a result of the obvious change of the AFM image size of the nano-islands as shown in Fig.6-4 (f), implying that some material had been transferred to the tip during *I-V* characterization. Fig.6-8 (a) shows AES Zn map of a C-AFM tip after electrical characterization. The inset is the corresponding top-view SEM image of the tip. Three points with diameters of 10nm marked in Fig. 6-8 (a) were chosen for HSR-AES high energy resolution spectrum measurements to determine the chemical state of Zn in the coated layer. The results are shown in Fig.6-8 (b) as P1, P2, and P3, respectively.

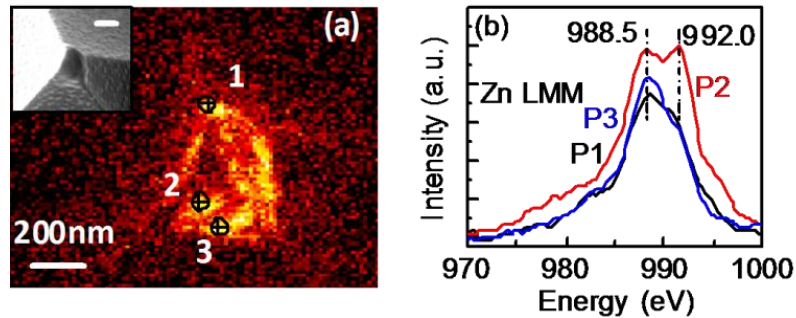


Figure 6-8. (a) AES Zn map of a C-AFM tip after electrical measurement, inset: top-view SEM image of this tip. (b) HSR-AES high energy resolution spectra of Zn LMM from the three spots with diameters of 10nm marked in (a) for this C-AFM tip.

A broad peak at 988.5eV is dominant for point 1 and point 3, which can be ascribed to ZnO.⁵⁰ While for point 2, another peak at 992.0eV can also be observed, which is

corresponding to the transition energy for Zn in the elemental form.⁴⁹ Additional SEM and energy-dispersive x-ray spectroscopy (EDX) measurements were carried out on these C-AFM tips and over-used tips. These results indicate that Zn exists as both oxide and metal in the coated layer on the C-AFM tips after electrical measurements, which indicates that the conducting filaments consist of oxygen vacancies.

6.3.6 Analysis of C-AFM tips

PHI 700 scanning Auger nanoprobe system with a spatial resolution of smaller than 10nm was utilized to analyze the C-AFM tips after electrical characterizations. AES elemental map were also employed to check the homogeneity of the coating layer on the over-used tips, i.e., the tips were used to measure *I-V* loops for several nano-islands. Fig.6-9 (a) shows a top-view SEM image of an over-used tip. Corresponding AES Zn map was obtained from the coated material on the tip before sputter etching (Fig.6-9 (b)), and after sputter etching of 3nm (Fig.6-9 (c)), 10nm (Fig.6-9 (d)), and 15nm coated materials (Fig.6-9 (e)). From these AES Zn maps, it is evident that as the sputter etching thickness increases, the Zn signal increases, and after removing the surface contamination by sputter etching of 15nm coated material, Zn is almost uniformly distributed in the coating layer of the over-used tip. In order to determine the chemical state of Zn, XAES were measured for the over-used tip both before and after sputter etching of 15nm coated material, as shown in Fig.6-9 (f). XAES results of standard Zn-metal and Zn-oxide are also shown for reference. It is easy to conclude that the coating layer on the over-used C-AFM tip consists of zinc oxide.

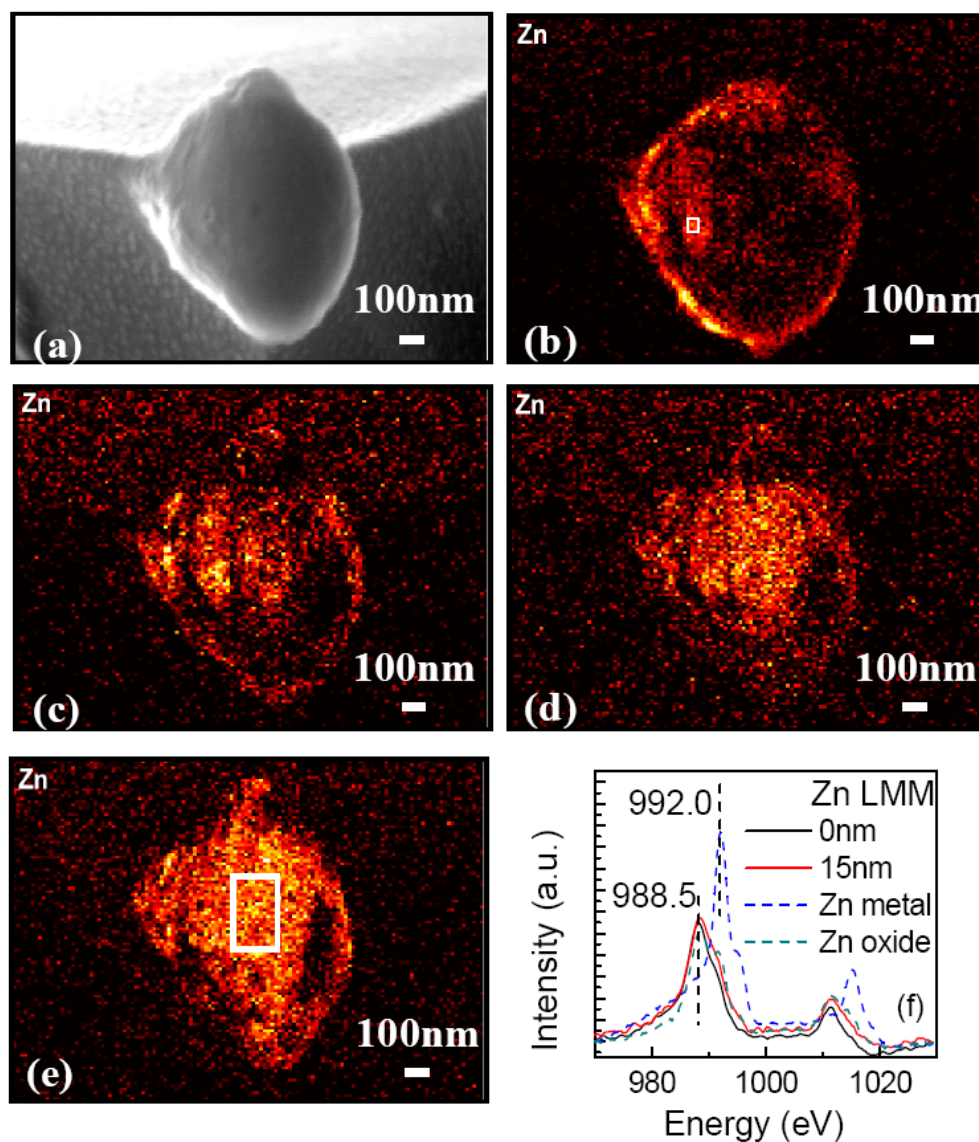


Fig.6-9 (a) Top-view SEM image of an over-used tip. AES Zn map of the over-used C-AFM tip: (b) before sputter etching, and after sputter etching of (c) 3nm, (d) 10nm, and (e) 15nm coated material. (f) XAES spectra of Zn LMM for the square areas in (b) and (e), XAES spectra for standard Zn-metal and Zn-oxide are also shown for reference.

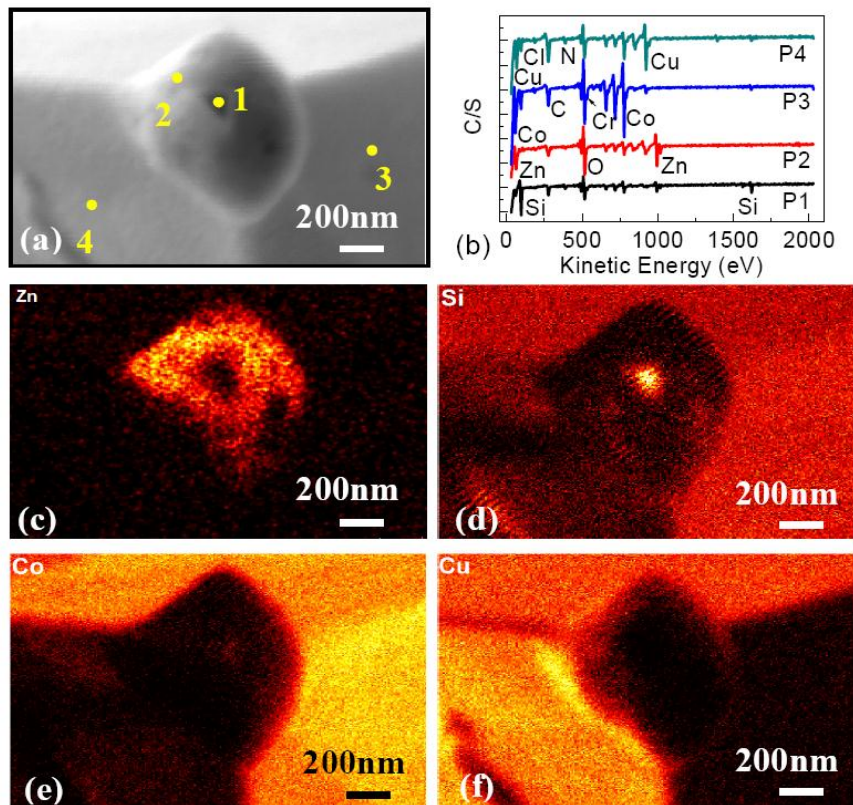


Fig.6-10 (a) Top-view SEM image of an over-used tip after sputter etching of 40nm coated material. (b) AES spectra obtained in location P1, P2, P3, and P4 with diameters of 10nm, corresponding to the SEM image in (a). (c) Zn, (d) Si, (e) Co, (f) Cu AES map of the over-used tip after sputter etching of 40nm coated material.

Fig.6-10 (a) shows a SEM image, Fig.6-10 (b) shows AES spectra for selected areas, and Fig.6-10 (c)-(f) show AES maps of Zn, Si, Co, and Cu of the over-used tip after sputter etching of 40nm coated material, respectively. Table 6-1 shows the atomic concentration for the selected area, in which Cu is not included because it is from the sample holder of the PHI 700 scanning Auger nanoprobe produced by backscatter

excitation. From these results, it is evident that the ZnO layer of about 40nm was uniformly coated around the top of the C-AFM tip by *I-V* characterization, which further supports the mechanism of the resistive switching behavior (Fig.6-8).

Area No.	C1	N1	O1	Al4	Si4	Cl1	Co2	Zn1	Cr2
P1	19.27	3.94	19.00	-	37.18	-	10.96	8.01	1.64
P2	17.59	2.31	36.6	-	7.64	0.25	11.31	24.31	-
P3	20.62	1.44	27.72	-	8.53	0.27	39.93	-	1.49
P4	40.33	4.71	20.17	6.02	14.12	0.38	14.28	-	-

Table 6-1. Atomic concentration for the selected areas.

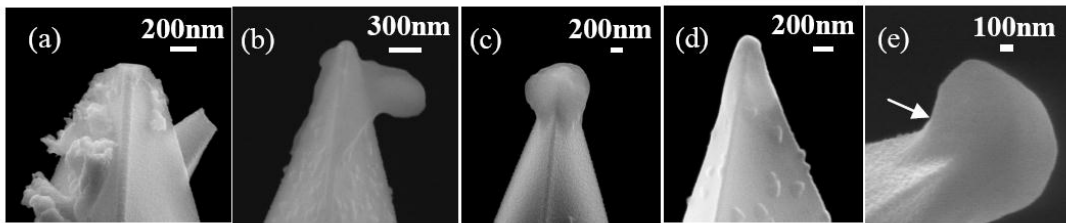


Fig.6-11 SEM images of three types of used C-AFM tips. C-AFM tip contaminated with particulates during AFM and C-AFM mapping (a) before (b) after *I-V* characterization, (c) over-used, and (d) used C-AFM tip. (e) Side-view SEM image of the over-used tip.

In order to ensure that the ZnO layers on used and over-used tips analyzed previously were coated during *I-V* characterization instead of results of AFM and C-AFM mapping, SEM images were obtained for 10 used tips. There are two types of tips as shown in Fig.6-11. One is the type of tips onto which some materials were transferred

during AFM and C-AFM mapping as shown in Fig.6-11 (a) and (b). The other is the type of tips around which a layer of ZnO was evenly coated during *I-V* characterization (Fig.6-11 (c) and (d)). A thin layer was coated on the used C-AFM tip extending 500nm from apex (Fig.6-11 (c)), which might consist of Zn, ZnO or both according to EDX results as shown in Fig.6-12. For the tip that was utilized for many times of *I-V* characterization, a thicker coated layer as well as the flow trend of the layer (arrow area) could be observed by side-view SEM image as shown in Fig.6-11 (e). From these images, it can be observed that the layer of materials coated by *I-V* characterization is definitely different from those transferred by AFM and C-AFM mapping. The coated layer was uniformly distributed around the top of the tip while the transferred materials are randomly distributed on the tip.

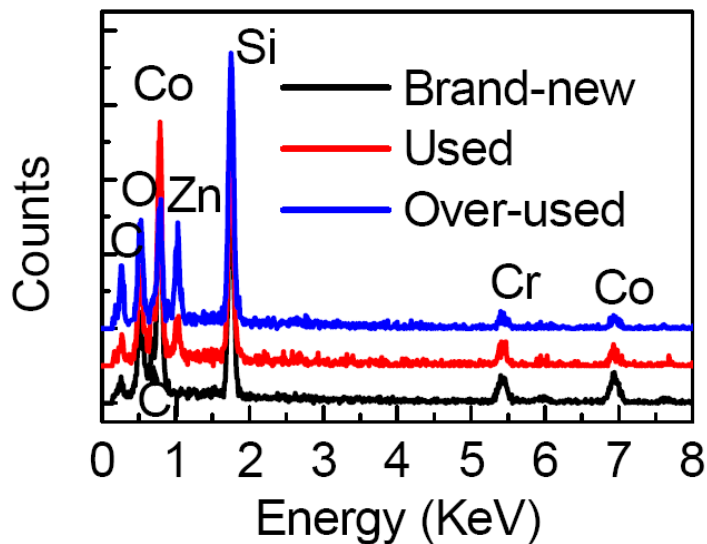
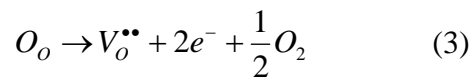


Fig.6-12 EDX analysis of the new (black), used (red), and over-used (blue) tips.

6.3.7 Mechanism

Finally we discuss redox-controlled oxygen vacancy filament formation and rupture process, which are responsible for the bipolar resistive switching behavior in C-AFM tip/ZnO nano-island/p⁺-Si resistive memory system (Fig.6-13). For initial state as shown in Fig.6-13 (a), oxygen vacancies are homogeneously distributed in the whole nano-island and act as donors in ZnO materials,³⁵ leading to evenly distributed current as shown in the C-AFM image of Fig.6-7 (b). Oxygen vacancies in ZnO should occur in three different charge states: V_o , V_o^\bullet , and $V_o^{\bullet\bullet}$.⁵¹ V_o has captured two electrons and is electrically neutral relative to the lattice. V_o^\bullet has trapped one electron and is positively charged, while $V_o^{\bullet\bullet}$ does not capture any electron and is doubly positively charged. During the electroforming process as shown in Fig.6-13 (b), oxygen vacancies around the anode (C-AFM tip) lose the captured electrons and become positively charged, and then they move toward the cathode (substrate) and accumulate there, becoming a virtual cathode. At the same time, an oxidation reaction would happen around the anode according to^{52, 53}



where O_o denotes oxygen ions on regular lattice sites. These $V_o^{\bullet\bullet}$ will also begin to move toward the virtual cathode, while interstitial oxygen ions are drawn to the anode and result in the production of oxygen gas there. The main routes for the oxygen movement and consequently oxygen vacancy movement should be along the surface and

the edge of the nano-island because oxygen grain-boundary diffusion is 3 to 4 orders of magnitude greater than oxygen volume diffusion in ZnO.⁴¹ Finally, oxygen vacancy conductive filaments are created along the edge of the nano-island as schematically viewed in Fig.6-13 (c), which is the completion of the electroforming process indicated by a sudden increase of current in the I - V characterization (Fig.6-5 (a)). The formation of oxygen vacancy filaments is proved by the current distribution in the C-AFM image result as shown in Fig.6-7 (c) and the accumulation of ZnO and Zn metal on the tip, which indicates the reaction of redox, as shown in Fig.6-8. After electroforming, when the external voltage sweeps back to a less negative bias than V_{RESET} , V_O is electron-occupied and becomes electrically neutral. Due to electron shielding effect,⁵⁴ neutral V_O cannot capture charged interstitial O^{2-} effectively. When the bias voltage reaches V_{RESET} and is kept at V_{RESET} or a more negative value than V_{RESET} for enough time, as shown in Fig.6-5 (a), V_O loses its captured electrons and becomes $V_O^{\bullet\bullet}$, causing a significant increase of capturing probability of $V_O^{\bullet\bullet}$ to O^{2-} ,⁵⁴ as schematically shown in Fig.6-13 (d). The recombination between $V_O^{\bullet\bullet}$ and O^{2-} easily occurs near the edge of the nano-island, where oxygen ions are supplied from the ambient. This recombination is corresponding to absorption of oxygen reported in other publications.⁵⁵ Finally the filaments of oxygen vacancy are ruptured as schematically shown in Fig.6-13 (e) during the RESET process which is indicated by the sudden decrease of the current (Fig.6-5 (a)). At the same time, oxidation reaction in equation (3) keeps happening so that oxygen vacancies are continuously supplied. During the RESET process, many oxygen vacancies are dragged

to the C-AFM tip. This causes the Zn ions around the tip to leave the ZnO lattice and transfer onto the surface of the tip as a result of the external electric field. These metal ions stay there as a metallic layer after getting electrons from the negative biased tip, which can be proved by the result shown in Fig.6-8 (b).

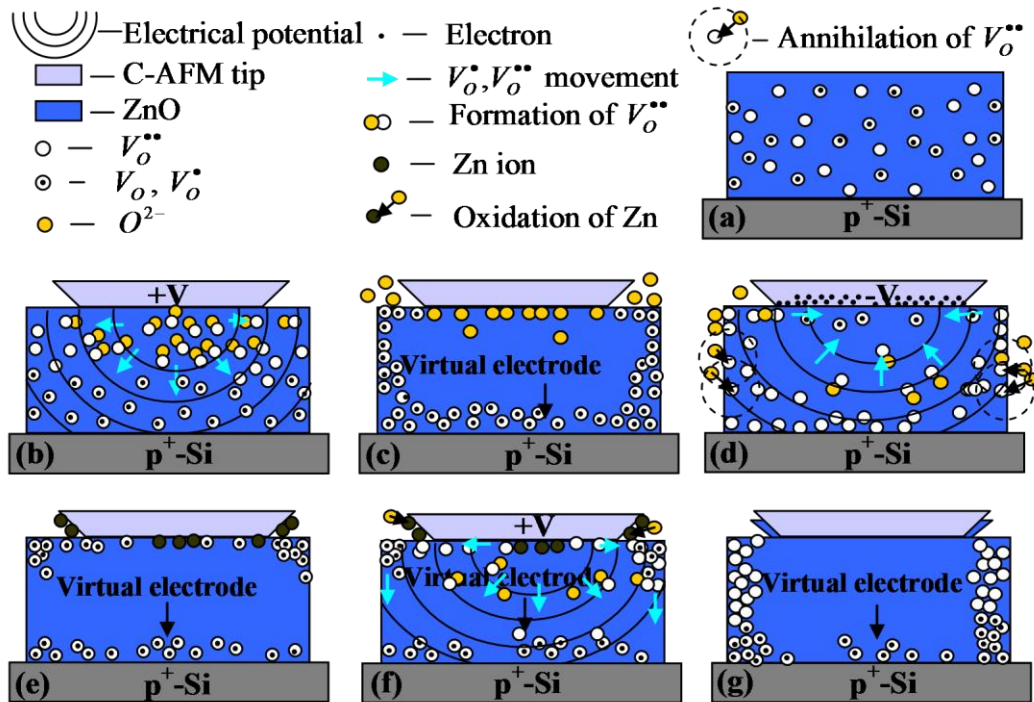


Figure 6-13. Schematic illustration of the resistive switching mechanism of the ZnO nano-island resistive memory: (a) homogeneously conductive initial state, (b) electroforming process for oxygen vacancy generation and filament formation by movement of oxygen ions or oxygen vacancies, (c) electroformed state, (d) RESET process for oxygen vacancy annihilation and filament rupture by moving oxygen ions to V_O , (e) OFF state, (f) SET process, and (g) ON state.

After the RESET process, as shown in Fig.6-13 (f), when voltage sweeps back to a positive bias, oxygen vacancies are continuously created by the oxidation of the lattice oxygen ions, which is corresponding to desorption of oxygen.⁵⁵ All oxygen vacancies are then pushed away by the electric field from the tip mainly along the surface and edge of the nano-island and gather there to restore the filaments or create new ones, and switch the resistive memory to ON-state (Fig.6-13 (g)). Meanwhile, oxygen ions are drawn back to the surface of the ZnO nano-island near the tip where they recombine with some Zn ions which are pushed back from the tip by the electric field. During this SET process, some of the Zn ions on the surface of the tip are also oxidized. As a result, a mixture layer of ZnO and Zn metal is left on the surface of the C-AFM tip. If the *I-V* characterization is performed for enough times by one tip, all Zn metals on the tip should be oxidized. This picture of creation and rupture process of redox controlled oxygen vacancy filaments can also be inferred from the morphology change of the nano-island as shown in Fig.6-4 (f). According to Fig.6-7 and Fig.6-13, it can be concluded that grain edge plays a very important role in the formation and rupture of the conducting filaments consisting of oxygen vacancies in ZnO nano-scale resistive memories with cell diameters of 20~60nm. This conclusion means that oxygen vacancy is a surface-related defect, as reviewed by Djuricic and Leung.⁵⁶

6.4 Conclusion

Large memory window resistive switching behavior was observed in ZnO nano-island resistive memories. Redox-controlled conducting filament formation/rupture

consisting of oxygen vacancies, which is regarded as a possible mechanism for resistive memories at the macroscopic scale, was proved through various electrical and imaging results to be also responsible for the switching behavior of the ZnO nano-island resistive memory with a dimension of as small as 20nm. Furthermore, C-AFM results have revealed that the conducting filaments are formed on the edges of ZnO nano-island and can have a size on the order of 5nm, suggesting that ZnO-based RRAM is a promising technology for future nonvolatile memory at the scaled technology.

6.5 References

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Chapter 7: Conclusion

In summary, an introduction to flash memory and the methodologies for it has been shown. First a bottom up approach for the aligned epitaxial growth of Si NCs on 1-dimensional (1-D) HfO₂ ridges created by the growth of HfO₂ thin film on CNTs was demonstrated. Periodic alignment of Si dots on the 1-D HfO₂ ridge was observed, which can be controlled by varying different growth conditions, such as growth temperature, growth time, and disilane flow rate. The alignment was stipulated to be a cause of the high strain 1-D ridge on the HfO₂ film, which favors the formation of Si seeds over the surrounding flat HfO₂ area.

A memory structure based on self-aligned Si NCs grown over Al₂O₃ covered parallel-aligned CNTs by gas source molecular beam epitaxy was also achieved. Electrostatic force microscopy characterizations directly prove the charging and discharging of discrete NCs through the Al₂O₃ layer covering the CNTs. A CNT field effect transistor based on the NC/CNT structure was fabricated and characterized demonstrating evident memory characteristics. Direct tunneling and Fowler-Nordheim tunneling phenomena were observed at different programming/erasing voltages. Retention was demonstrated to be on the order of 10⁴ s. Although there is still plenty of room to enhance the performance, the results suggest that CNT-based NC memory with diminutive CNTs and NCs could be an alternative structure to replace traditional floating gate memory.

A CNT/Pt NC floating gate transistor with ambipolar characteristics was fabricated. It showed large memory window with backgate sweeping past half the sweeping range. An electrostatic simulation showed that programming and erasing from a backgate has similar effect to a top gate due to the fringing fields into the CNT. The current response to a sinusoidal signal was measured at 0V. It showed that after programming and erasing the ambipolar memory can be tuned to have either rectifying or non-rectifying behavior. Furthermore a binary signal was used to test the performance of the charge stored in the floating gate showing multiple modes of operation. This experiment showed that this technology could be used to expand the field of floating gate memory into RF circuitry.

Bipolar resistive switching behavior was observed in epitaxial ZnO NCs with base diameters and heights ranging around 30 and 40 nm, respectively. All four different states (initial, electroformed, ON and OFF) of the nano-scale resistive memories were measured by conductive atomic force microscopy immediately after the voltage sweeping was performed. Auger electron spectroscopy, and other experiments were also carried out to investigate the switching mechanism. The formation and rupture of conducting filaments induced by oxygen vacancy migration are responsible for the resistive switching behaviors of ZnO resistive memories at the nano-scale. Resistive memory is one of the most promising candidates for next generation non-volatile memory technology due to its variety of advantages such as simple structure and low power consumption. These measurements move ZnO technology closer to those future goals.