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# High-Temperature Thermoelectric Characterization of III–V Semiconductor Thin Films by Oxide Bonding

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A device fabrication and measurement method utilizing a SiO<sub>2</sub>–SiO<sub>2</sub> covalent bonding technique is presented for high-temperature thermoelectric characterization of thin-film III–V semiconductor materials that suffer from the side-effect of substrate conduction at high temperatures. The proposed method includes complete substrate removal, high-temperature surface passivation, and metallization with a Ti–W–N diffusion barrier. A thermoelectric material, thin-film ErAs:InGaAlAs metal/semiconductor nanocomposite grown on a lattice-matched InP substrate by molecular beam epitaxy, was transferred onto a sapphire substrate using the oxide bonding technique at 300°C, and its original InP substrate, which is conductive at high temperatures, was removed. Electrical conductivities and Seebeck coefficients were measured from room temperature to 840 K for this material on both the InP and sapphire substrates, and the measurement results clearly show that the InP substrate effect was eliminated for the sample on the sapphire substrate. A strain experiment has been conducted to investigate the effect of strain on electrical conductivity.

**Key words:** High-temperature measurements, thermoelectric, oxide bonding, substrate removal

## INTRODUCTION

Recently, much attention has been drawn to high-temperature material characterization of semiconductor thin films for thermoelectric power generation, photovoltaic energy conversion, and other high-temperature applications.<sup>1–4</sup> Since the efficiency of these energy conversion applications relies heavily on the carrier transport properties of the materials used, it is very important to characterize the materials with a high degree of accuracy in the working temperature range of each specific application. Thin-film semiconductor materials are ideally suited for many of these applications,

because they can be grown with high quality and stability at high temperatures, and their fundamental properties including band structures are well understood.

InGa(Al)As doped with Er grown by molecular beam epitaxy (MBE) has demonstrated its usefulness in thermoelectric energy conversion, with reduced thermal conductivity below the alloy limit due to effective phonon scattering by ErAs nanoparticles.<sup>5</sup> Recently, it has also been reported that the ErAs nanoparticles formed in InGa(Al)As can enhance the thermoelectric power factor by effective electron scattering under special conditions.<sup>6,7</sup> These *n*-type and *p*-type ErAs:InGa(Al)As materials have been used to build thermoelectric power generator modules to generate an output power density

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of  $2.5 \text{ W/cm}^2$ ,<sup>8</sup> or a total output power of  $5.5 \text{ W}$  when the materials were segmented with  $\text{Bi}_2\text{Te}_3$ .<sup>9</sup>

However, electrical conductivity and Seebeck coefficient measurements at high temperatures have been impeded for this material, because the InP substrate used for the material growth becomes electrically conductive at high temperatures due to thermal excitation of free charge carriers, even though it is semi-insulating at room temperature, and it is very difficult to separate this substrate effect from the overall measurement.

Herein, we report an approach to eliminate the substrate effect for thin-film ErAs:InGa(Al)As metal/semiconductor nanocomposite material by using a  $\text{SiO}_2$ - $\text{SiO}_2$  covalent bonding technique. Surface passivation and metallization suitable for high-temperature measurements are also proposed. We present successful measurements of high-temperature properties of such thin films from room temperature up to  $840 \text{ K}$  with no substrate effect. The proposed device fabrication technique may be used for characterizing any semiconductor thin films that require the removal of substrate and/or other parasitic conduction effects. The strain on the thin film induced by thermal expansion mismatch between the thin film and the sapphire substrate is calculated, and a sample-bending apparatus is used to measure the dependence of electrical conductivity on tensile strain in the thin film. It is shown that the strain change on the thin film accounts for the discrepancy in electrical conductivity between the two samples on the InP and sapphire substrates at room temperature, and the discrepancy is estimated to be only within 2% at  $840 \text{ K}$ .

## DEVICE FABRICATION

Films ( $2 \mu\text{m}$  thick) of  $\text{ErAs}:(\text{InGaAs})_{0.8}(\text{InAlAs})_{0.2}$  lattice-matched to an InP substrate were grown on  $520\text{-}\mu\text{m}$ -thick semi-insulating an InP substrate by MBE at a growth temperature of  $490^\circ\text{C}$ . Erbium was codeposited during the growth of the semiconductor matrix with total Er volume fractions of 0.3% and 0.6% in  $(\text{InGaAs})_{0.8}(\text{InAlAs})_{0.2}$ . At these volume fractions, ErAs islands are formed in the semiconductor matrix.<sup>10,11</sup> Rocksalt-structured ErAs precipitates of  $2.4 \text{ nm}$  average diameter were observed to be randomly distributed in the matrix by transmission electron microscopy (TEM).<sup>12</sup>

Recently a low-temperature, strong  $\text{SiO}_2$ - $\text{SiO}_2$  covalent wafer-bonding technique has been reported.<sup>13</sup> This bonding technique was originally developed for large-scale III-V semiconductor-to-silicon wafer bonding, but can generally be used to bond any two solid material surfaces, provided that their surface roughness is sufficiently low. We have utilized this bonding technique for the bonding of a III-V epitaxial film and a sapphire wafer with little modification of the process. The reactive hydrophilic surface and structural porosity of  $\text{SiO}_2$  layers make the oxide a good bonding interface layer and

decrease the temperature required for strong covalent bonding. The bonding was annealed at  $300^\circ\text{C}$  for 2 h to increase the bond strength. This annealing temperature is quite low compared with those of other conventional bonding techniques, which are often as high as  $1000^\circ\text{C}$ . Lowering the bonding temperature is very important, because strain induced by thermal expansion mismatch between the two bonded substrates can degrade material quality and change the properties of the materials involved.<sup>14</sup> We will analyze the effect of strain on the measurement results in the next section.

For high yield from the bonding process, ultralow surface roughness is required. The surface roughness of the commercial sapphire wafer used in the bonding process was as low as  $5 \text{ \AA}$ , and the  $30\text{-nm}$ -thick plasma-enhanced chemical vapor deposition (PECVD)  $\text{SiO}_2$  that was used as a bonding interface layer had a peak-to-peak roughness less than  $10 \text{ \AA}$ , which is in a suitable range for bonding. However, the III-V InGaAlAs epitaxial layer grown by MBE had surface oval defects which can be as high as  $2 \mu\text{m}$  from the epitaxial surface. These defects generally originate from indium and/or gallium droplets formed on the surface of the substrate during the oxide desorption process before growth.<sup>15</sup> In order to remove those defects from the film, a photolithography process was performed to form a  $20\text{-}\mu\text{m}$ - to  $30\text{-}\mu\text{m}$ -diameter open hole of photoresist around each oval defect. Then, the sample was dipped in  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (1:5:15) to etch the open area down to the substrate and remove the oval defects.

The device fabrication steps utilizing the  $\text{SiO}_2$ - $\text{SiO}_2$  covalent bonding technique are illustrated in Fig. 1. Prior to bonding,  $0.5\text{-}\mu\text{m}$ -deep  $6\text{-}\mu\text{m}$ -wide in-plane channels were inscribed on the sapphire substrate using inductively coupled plasma (ICP) dry etching with  $\text{BCl}_3/\text{Cl}_2$  gases under  $200 \text{ W}$  radio frequency (RF) power. These in-plane channels are used as efficient outgassing paths for by-product gases such as  $\text{H}_2\text{O}$  and hydrogen generated during bonding. After thorough solvent cleaning of the defect-removed thin film and the channeled sapphire substrate, a  $30\text{-nm}$ -thick  $\text{SiO}_2$  bonding interface layer was deposited on the surface of both the thin film and the sapphire substrate using a PECVD Plasma-Therm model 790 system with precursor gases of 2%  $\text{SiH}_4$  diluted in He, and  $\text{N}_2\text{O}$  by  $13.56 \text{ MHz}$  source excitation at  $250^\circ\text{C}$ . The thickness of the  $\text{SiO}_2$  layer was chosen so as to keep the surface roughness below  $10 \text{ \AA}$  for high-yield bonding. The  $\text{SiO}_2$  layers were then baked at  $200^\circ\text{C}$  for 2 h to drive undesirable gas molecules out of the oxide layers.

After the post-baking, the  $\text{SiO}_2$  layers were cleaned in a modified RCA solution of  $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (0.2:1:5) at  $80^\circ\text{C}$  for 10 min, and in turn, in solvent solutions of acetone, isopropyl alcohol, and deionized water. Next, the two  $\text{SiO}_2$  layers were treated with an  $\text{O}_2$  plasma of  $39 \text{ W}$  RF power with  $26 \text{ sccm}$   $\text{O}_2$  flow rate and  $15 \text{ mTorr}$  pressure for 45 s.

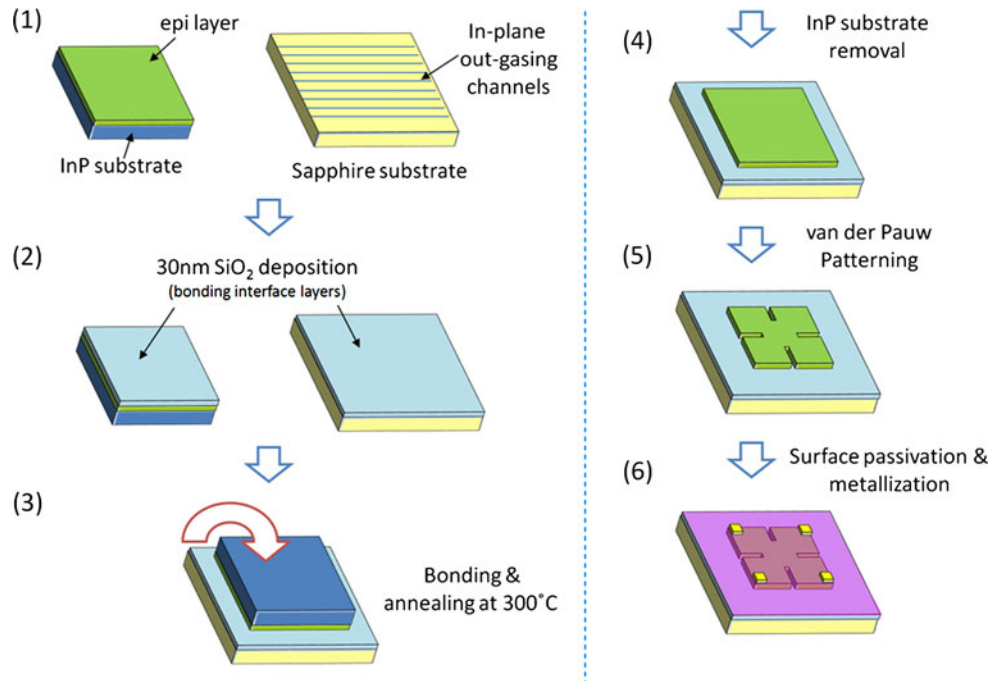


Fig. 1. Device fabrication steps for the van der Pauw (vdP) samples that were used for electrical conductivity and Seebeck coefficient measurements at high temperatures.

This  $O_2$  plasma treatment is necessary to suppress void formation at the bonding interface during the  $300^\circ\text{C}$  anneal and to activate Si–O bonds on the surface. Several activation steps were performed immediately after the  $O_2$  plasma treatment: the first step was dipping the two samples in diluted HF solution (0.025% HF) for 1 min, and the second was dipping them in  $NH_4OH$  for 2 s. The HF solution forms reactive Si–F bonds on the  $SiO_2$  surface. It does not etch the  $SiO_2$  layers because of the very low HF concentration. The  $NH_4OH$  converts Si–OH to Si– $NH_2$  bonds so that more reactive bonding legs can participate in the bonding with the mating surface.<sup>14</sup> Manual attachment between the two samples was carried out immediately after the two activation steps by pressing the InP substrate and the sapphire substrate together with the two  $SiO_2$  layers facing each other. The spontaneously bonded sample was then annealed at  $300^\circ\text{C}$  under pressure of 1.5 MPa for 2 h in a commercial Suss SB6E wafer bonder to enhance the bond strength.

As shown in step 4 in Fig. 1, the InP substrate was finally etched off in a solution of  $HCl:H_2O = 2:1$  at room temperature to leave only the  $2\text{-}\mu\text{m}$  thin film and a total 60 nm  $SiO_2$  interfacial layer on the sapphire substrate. Figure 2 shows the thin film bonded on a  $1\text{ cm} \times 1\text{ cm}$  sapphire plate after InP substrate removal. In the microscopic view of the bonded surface in Fig. 3, one can see open holes in the thin film where the oval defects were removed by wet etching. A square cloverleaf-shaped van der Pauw (vdP) pattern<sup>16</sup> was fabricated on the  $2\text{-}\mu\text{m}$  epitaxial layer by reactive ion etching (RIE) with  $Cl_2$

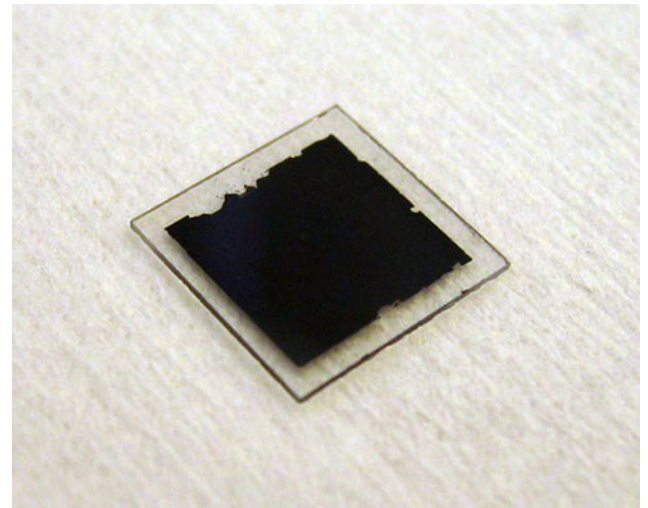


Fig. 2. A picture of a thin film bonded on a  $1\text{ cm} \times 1\text{ cm}$  sapphire plate after the original InP substrate was removed by wet etching.

gas, as shown in step 5 in Fig. 1, after which surface passivation and metallization were performed.

High-temperature surface passivation or encapsulation is needed to prevent the III–V epitaxial layer from decomposing at temperatures above the growth temperature. Silicon nitride deposited by ICP PECVD with  $N_2$  precursor as a nitrogen source is known to be a good candidate for surface passivation.<sup>17,18</sup> ICP silicon nitride contains less hydrogen than that deposited by PECVD, which normally uses  $NH_3$  precursor instead of  $N_2$ , and hydrogen is

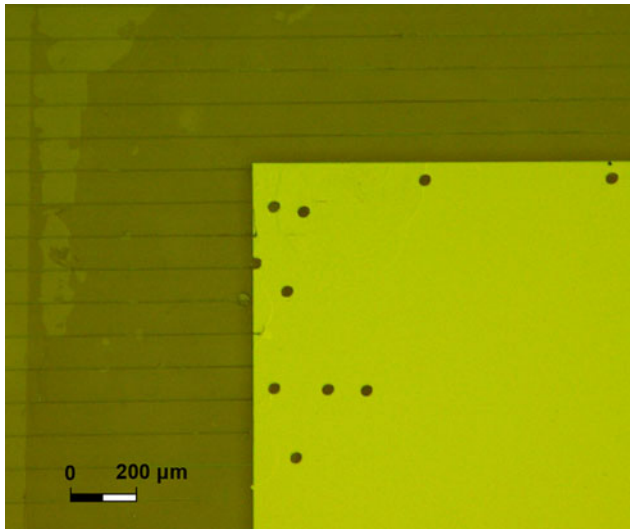


Fig. 3. Microscopic view of the surface of the thin film bonded onto a microchanneled sapphire plate. The small open circular holes on the thin film indicate where oval defects were removed for surface flattening before bonding. Microchannels with  $100\ \mu\text{m}$  spacing are shown on the sapphire plate, and the dark area is the  $\text{SiO}_2$  layer deposited on the sapphire plate, used as a bonding interface material.

the main cause of surface blistering on the nitride at high temperatures.<sup>19</sup> However, ICP silicon nitride deposition is very sensitive to native oxide on the III-V epitaxial layer. In particular, the semiconductor matrix containing Al is vulnerable to surface oxidation, and thus ICP silicon nitride may not be properly deposited on the III-V thin films. We have found that buffered HF (BHF) dipping and *in situ*  $\text{SF}_6/\text{Ar}$  plasma treatment can effectively remove the oxide on the surface and help deposit the ICP silicon nitride on III-V compound semiconductors.  $\text{SF}_6$  plasma converts the thin native  $\text{AlO}_x$  layer into  $\text{AlF}_3$ , which is removed by a subsequent Ar plasma. Immediately after dipping in BHF for 1 min, the sample was loaded into a commercial Unaxis ICP deposition chamber, and cleaned *in situ* with an  $\text{SF}_6$  plasma at 20 W RF bias for 30 s and a subsequent Ar plasma at the same RF power for 60 s, all at  $250^\circ\text{C}$ . A 2000 Å silicon nitride layer was then deposited with 100% silane and  $\text{N}_2$  gases diluted in Ar at 50 W RF bias at  $250^\circ\text{C}$ . Another layer of 1000 Å PECVD  $\text{SiO}_2$  was deposited on top of the ICP silicon nitride to reduce the tensile strain in the silicon nitride at high temperatures.

High-temperature metallization requires a good diffusion blocking barrier metal to prevent contact metals from diffusing into the semiconductor thin film at high temperatures. Thin Ti-W-N deposited by reactive direct-current (DC) sputtering from a Ti-W target in Ar- $\text{N}_2$  ambient gas mixture has been reported to be a good diffusion barrier between GaAs and Au up to  $750^\circ\text{C}$ .<sup>20</sup> We successfully deposited a 500 Å Ti-W-N film on the ErAs:InGaAlAs epitaxial layer by reactive DC sputtering using

a Ti-W (90/10 at.%) target in an Ar- $\text{N}_2$  (25 sccm/1.5 sccm) gas mixture at 200 W and 10 mTorr as a high-temperature diffusion barrier. Before the sample was taken out of the sputtering chamber, a very thin gold layer was deposited to prevent oxidation of the Ti-W-N. An additional 5000-Å-thick gold probing layer was then deposited by using an electron beam evaporator. Four Ti-W-N/Au contacts of  $150\ \mu\text{m} \times 150\ \mu\text{m}$  size were fabricated at the four corners of the vdP pattern, as shown in step 6 in Fig. 1. The total size of the square cloverleaf-shaped vdP pattern was  $5\ \text{mm} \times 5\ \text{mm}$ .

## HIGH-TEMPERATURE MEASUREMENTS

Both electrical conductivities and Seebeck coefficients of the substrate-removed samples of 0.3% and 0.6% ErAs:InGaAlAs were measured from room temperature up to 840 K. Four-probe vdP measurements for electrical conductivity were conducted by causing an electric current to flow through two adjacent contacts and measuring the voltage across the other two contacts.<sup>16</sup> During the measurements, the sample sat on a heating block equipped with a cartridge heater inside. The cartridge heater was connected to an external temperature controller, which controlled the temperature of the heater to a set point using proportional-integral-derivative (PID) feedback control by reading the thermocouple built into the heater. Highly thermally conductive silver paint was applied evenly between the sample and the heating block for efficient and uniform heating of the sample. All the heating parts except the temperature controller were placed in a vacuum chamber, and the pressure was maintained below  $1 \times 10^{-4}$  Torr over the entire temperature range during the measurements. A type K thermocouple was used to measure the temperature directly on the sample surface. The sample was given sufficient time to allow its temperature to stabilize at each temperature point measured.

Seebeck coefficients of the samples were measured in the same system, but two heating blocks were used in order to generate a temperature gradient across the sample. The sample was placed diagonally across the two heating blocks so that one cloverleaf of the sample was heated by one block while its diagonal counterpart was heated by the other block. By setting the two heating blocks at different temperatures with a 5 K to 8 K maximum difference, voltage as a function of temperature difference was obtained, and the slope in the linear relationship gave us the Seebeck coefficient at each temperature. Two type K thermocouples were used to measure the temperature difference directly on the sample, and two electrical probes were used to measure the voltage between the two contacts at different temperatures. Before collecting data points, the two temperatures of the sample were stabilized for sufficient time until the variation of each temperature became less than 0.1 K.

## RESULTS AND ANALYSIS

Figure 4 shows a comparison between the electrical conductivities of the substrate-removed sample on a sapphire substrate and the original sample on an InP substrate. The electrical conductivity of the InP substrate was also measured and plotted after multiplying by the thickness ratio (inset to Fig. 4). In order to make ohmic contact when the electrical conductivity of the InP substrate was measured, a highly doped thin film was grown on the InP substrate, and patterned at the four edges. Then, the contact metals were deposited on the thin-film mesas instead of directly on the InP substrate.

When one measures the electrical conductivity of a thin film grown epitaxially on a substrate, the actual conductivity measured ( $\sigma_{\text{total}}$ ) is the sum of the electrical conductivity of the thin film and a parasitic term from the substrate given by

$$\sigma_{\text{total}} = \sigma_f + \sigma_s \cdot \frac{t_s}{t_f}, \quad (1)$$

where  $\sigma_f$  and  $\sigma_s$  are the electrical conductivities of the thin film and the substrate, respectively, and  $t_f$  and  $t_s$  are the thicknesses of the thin film and the substrate, respectively. Note that the parasitic term from the substrate is multiplied by the thickness ratio.

As the InP substrate is semi-insulating at room temperature, its electrical conductivity is as low as  $1 \times 10^{-4} \Omega^{-1} \text{cm}^{-1}$  at room temperature, while the thin-film conductivity is about  $350 \Omega^{-1} \text{cm}^{-1}$ . Therefore, the substrate has no effect on the measured electrical conductivity at low temperatures. However, as temperature increases, the electrical

conductivity of the substrate increases exponentially due to thermal excitation of free carriers and becomes significant. As shown in the inset to Fig. 4, the substrate parasitic term increased exponentially with temperature and became significant at above 600 K. This substrate effect was clearly seen in the measured electrical conductivity of the sample on an InP substrate above 600 K. However, the sample on a sapphire substrate showed no such substrate effect.

The substrate effect was also apparent in the Seebeck measurements for the thin film on an InP substrate (Fig. 5). At low temperatures, the Seebeck coefficient of the original sample on an InP substrate was almost identical to that of the bonded sample on a sapphire substrate. Above 580 K, however, the Seebeck coefficient of the original sample suddenly increased with temperature, which is due to the substrate effect. The total (measured) in-plane Seebeck coefficient of the two parallel layers is described by

$$S_{\text{total}} = \frac{S_f \cdot \sigma_f + S_s \cdot \sigma_s \cdot t_s/t_f}{\sigma_f + \sigma_s \cdot t_s/t_f}, \quad (2)$$

where  $S_f$  and  $S_s$  are the Seebeck coefficients of the thin film and the substrate, respectively. The Seebeck coefficient of the InP substrate remains very high in the temperature range because of its low electrical conductivity, and its contribution to the total Seebeck coefficient increases with temperature mainly due to the exponential increase of its conductivity, which is clearly shown in Fig. 5, where the Seebeck coefficient of the thin film on an InP substrate suddenly increases above 600 K due to the substrate contribution, while this is not observed for the bonded sample.

Figure 6 shows electrical conductivity measurement results for the  $\text{ErAs}:(\text{InGaAs})_{0.8}(\text{InAlAs})_{0.2}$

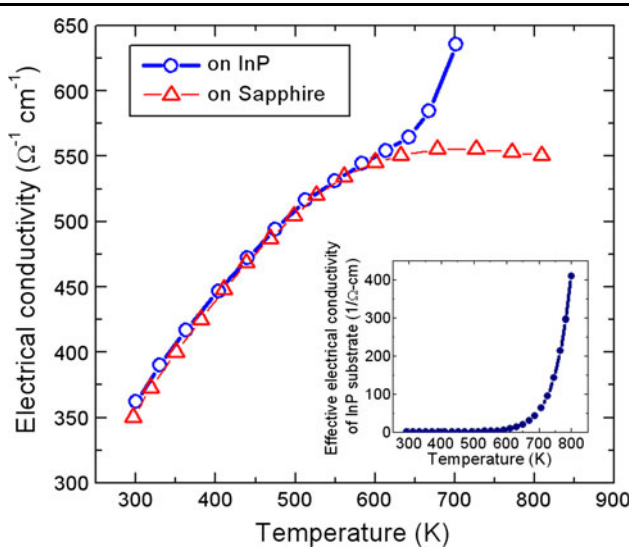


Fig. 4. Electrical conductivities of thin films of 0.6% ErAs:InGaAlAs on an InP substrate (circles) and a sapphire substrate (triangles). The inset shows the effective electrical conductivity [electrical conductivity multiplied by the thickness ratio of the substrate to the thin film ( $=520 \mu\text{m}/2 \mu\text{m}$ )] of the InP substrate only.

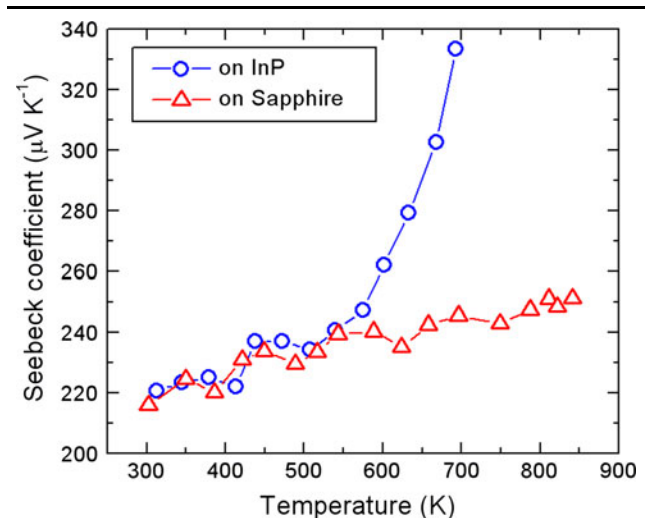


Fig. 5. Seebeck coefficients of thin films of 0.3% ErAs:InGaAlAs on an InP substrate (circles) and a sapphire substrate (triangles).

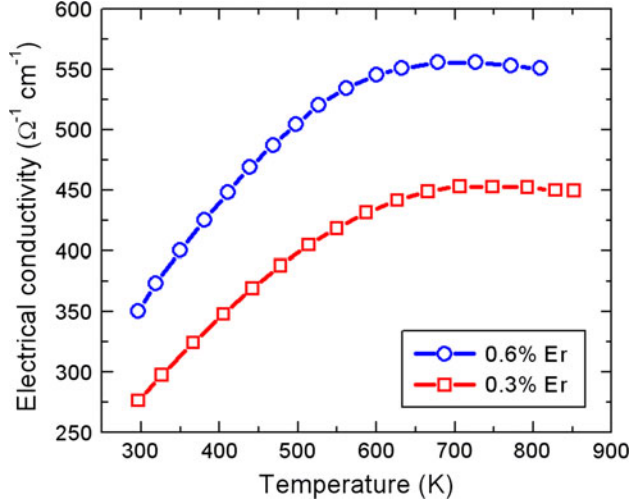


Fig. 6. Electrical conductivity versus temperature of  $2 \mu\text{m}$  ErAs:(InGaAs) $_{0.8}$ (InAlAs) $_{0.2}$  thin films with 0.3% and 0.6% Er concentrations bonded on sapphire substrates.

with 0.3% and 0.6% Er concentrations on sapphire substrates from room temperature to 840 K. Figure 7 shows the Seebeck coefficients of the two samples in the same temperature range. It is seen that both the electrical conductivity ( $\sigma$ ) and the Seebeck coefficient ( $S$ ) increased with temperature. The thermoelectric power factor, which is defined as  $S^2\sigma$ , also increased with temperature and reached  $3.17 \times 10^{-3} \text{ W m}^{-1} \text{ K}^{-2}$  with an electrical conductivity of  $550 \Omega^{-1} \text{ cm}^{-1}$  and a Seebeck coefficient of  $240 \mu\text{V K}^{-1}$  at 840 K for the 0.6% Er sample, and  $2.81 \times 10^{-3} \text{ W m}^{-1} \text{ K}^{-2}$  with an electrical conductivity of  $450 \Omega^{-1} \text{ cm}^{-1}$  and a Seebeck coefficient of  $250 \mu\text{V K}^{-1}$  at 840 K for the 0.3% Er sample.

Strain is one of the important factors that can change the band structures of semiconductor materials. It is known that compressive strain generally increases the bandgap and reduces the carrier density as well as the electrical conductivity in III-V semiconductor materials, while tensile strain affects those properties in the opposite way.<sup>21</sup> Strain is induced in the ErAs:InGaAlAs thin film when the film is cooled to room temperature after bonding onto a sapphire substrate at  $300^\circ\text{C}$  because of the thermal expansion mismatch between the thin film and the sapphire substrate. To calculate this strain, the bimetallic thermostat model was applied.<sup>22</sup> We assume that the strain on the thin film is zero at the annealing temperature,  $300^\circ\text{C}$ , because the bonds are so weak at room temperature before annealing that they are broken and rearranged when heated to the annealing temperature, maintaining zero strain at the interface. Once the bond is strengthened by the heat treatment at  $300^\circ\text{C}$ , the two mating surfaces do not slide against each other as temperature changes afterward, but the whole samples are mechanically bent to compensate for the mismatch of thermal strains. The

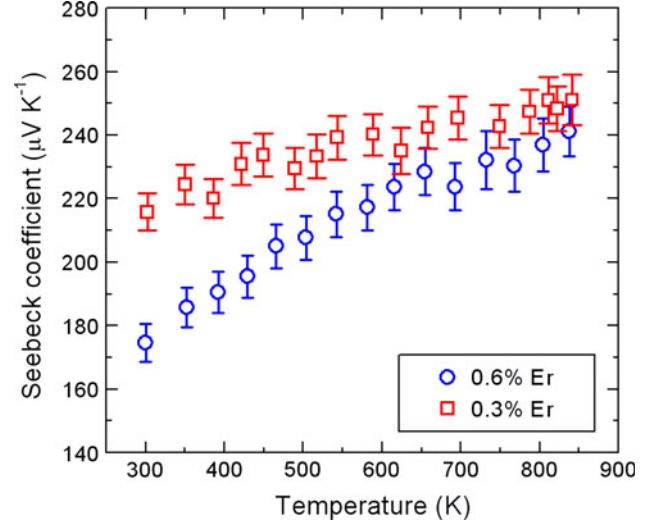


Fig. 7. Seebeck coefficient versus temperature of  $2 \mu\text{m}$  ErAs:(InGaAs) $_{0.8}$ (InAlAs) $_{0.2}$  thin films with 0.3% and 0.6% Er concentrations bonded on sapphire substrates.

stress parallel to the interface, i.e., in the  $x$ -direction, on the thin film induced by the mechanical bending after it has cooled from the annealing temperature is given by<sup>22</sup>

$$P_x = \frac{\Delta\alpha \cdot \Delta T}{\lambda t_f} \left[ 1 + \frac{3(t_f + t_s)D_f}{t_f D} \right], \quad (3)$$

where  $\Delta\alpha = \alpha_s - \alpha_f$  is the difference of thermal expansion coefficients between the sapphire substrate and the thin film,  $\Delta T$  is the temperature change, and

$$\begin{aligned} D_f &= \frac{E_f t_f^3}{12(1 - \nu_f^2)} \\ D_s &= \frac{E_s t_s^3}{12(1 - \nu_s^2)} \\ D &= D_f + D_s \\ \lambda &= \frac{1}{12} \left[ \frac{t_f^2}{D_f} + \frac{t_s^2}{D_s} + \frac{3(t_f + t_s)^2}{D} \right], \end{aligned}$$

where  $E_f$  and  $E_s$  are the Young's moduli, and  $\nu_f$  and  $\nu_s$  are the Poisson's ratios of the thin film and the substrate, respectively. The actual stress parallel to the interface depends on the position in the  $x$ -direction and tends to zero at the edge of the bonded surface, but it remains largely constant along most of the thin film except near the edge. The stress perpendicular to the interface is zero at all positions.

The biaxial strain parallel to the interface was then finally calculated using Eq. 3 as

$$\varepsilon_x = \frac{(1 - \nu_f) \cdot P_x}{E_f}. \quad (4)$$

The properties used for strain calculation are presented in Table I, and are all assumed to be

**Table I. Properties of ErAs:InGaAlAs, sapphire (c-plane) substrate, and InP (001) substrate used for strain calculation**

	ErAs:InGa(Al)As <sup>a</sup>	Sapphire (c-Plane)	InP (001) Substrate
Thermal expansion coefficient, $\alpha$ (K <sup>-1</sup> )	$6.0 \times 10^{-6}$	$7.4 \times 10^{-6b}$	$5.5 \times 10^{-6b}$
Young's modulus, $E$ (N/m <sup>2</sup> )	$6.73 \times 10^{10}$	$3.45 \times 10^{11}$	$6.11 \times 10^{10}$
Poisson's ratio, $\nu$	0.33	0.29	0.36
Thickness, $t$ ( $\mu$ m)	2.0	430	520

<sup>a</sup>All from the properties of InGaAs lattice-matched to InP. <sup>b</sup>Averaged from room temperature to 300°C.

independent of temperature. Temperature-averaged values were used for thermal expansion coefficients. Based on the properties in Table I, the room-temperature strain parallel to the interface on the ErAs:InGaAlAs thin film bonded on a sapphire substrate was found to be  $-2.9 \times 10^{-4}$ , which is compressive. On the other hand, the thin film on the original InP substrate also experiences strain because the thermal expansion coefficients of the thin film and the InP substrate are not the same, although they are lattice matched. The strain induced in the thin film on the original InP substrate when it is cooled from the annealing temperature was calculated using Eq. 4 to be  $1.0 \times 10^{-4}$ , which is tensile. Therefore, the total strain change on the thin film after the bonding was the difference of the two calculated strains, i.e., compressive strain of  $3.9 \times 10^{-4}$  at room temperature. The magnitude of the strain decreases as the sample temperature increases, and becomes zero when the temperature reaches the annealing temperature, 300°C.

In order to study the effect of strain on electrical conductivity, a sample-bending apparatus was built to apply a mechanical tensile strain to the thin film on a sapphire substrate. A schematic of a sample bent by the apparatus is illustrated in Fig. 8 with some parameters defined to calculate how much strain is applied. The center of the backside of the sapphire substrate is pushed upward by a screw from the bottom by a height  $a$ , while the four edges are clamped by holder arms. The length of the thin film is elongated from  $l$  to  $l'$  by the push-up, and thus a tensile strain is applied to the thin film. Assuming that  $a$  is much smaller than  $l$ , the tensile strain parallel to the surface can be calculated using the parameters defined in Fig. 8 as

$$\varepsilon = \frac{l' - l}{l} \approx \frac{d}{2r} = \frac{4ad}{l^2}. \quad (5)$$

The room-temperature electrical conductivity was measured at varying strain for the 0.6% ErAs:InGaAlAs film bonded on a sapphire substrate to study the effect of strain on the electrical conductivity. Figure 9 shows the measured electrical conductivity as a function of tensile strain. The electrical conductivity of the sample was  $350 \Omega^{-1} \text{cm}^{-1}$  at room temperature without any

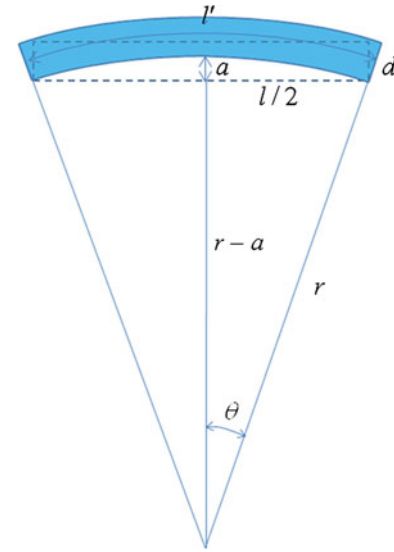


Fig. 8. Schematic diagram of a bending experiment. A thin film of thickness  $d$  and length  $l$  is at the position described by the dotted lines at rest. When pushed upward at the bottom center by the height  $a$ , the thin film is bent up and elongated to length  $l'$  with tensile strain.

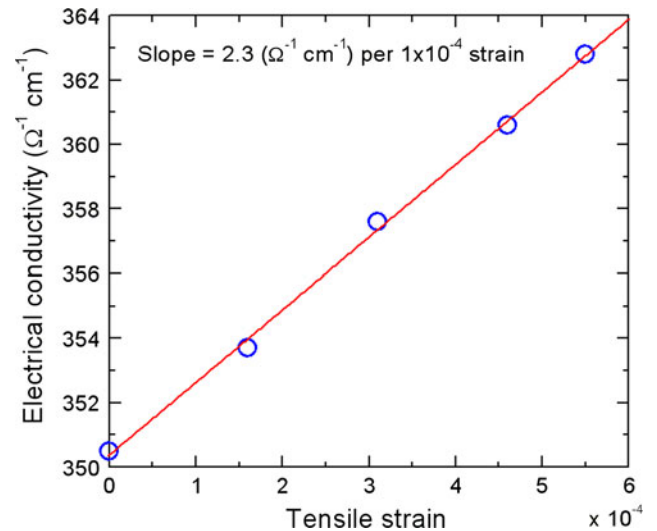


Fig. 9. Room-temperature electrical conductivity versus tensile strain for the 0.6% ErAs:InGaAlAs thin film bonded on a sapphire substrate.



intentional bending. However, as the sample bending intensified, the electrical conductivity increased linearly with tensile strain, as shown in Fig. 9. The conductivity increase due to tensile strain was  $2.3 \Omega^{-1} \text{ cm}^{-1}$  per  $1 \times 10^{-4}$  strain. If one recalls that the calculated strain change due to thermal expansion mismatch after bonding was  $3.9 \times 10^{-4}$ , the total conductivity change should be  $(2.3/10^{-4}) \times (3.9 \times 10^{-4}) = 8.97 \Omega^{-1} \text{ cm}^{-1}$ , which closely matches the measured difference,  $9.5 \Omega^{-1} \text{ cm}^{-1}$ , between the two samples on the InP and the sapphire substrates at room temperature shown in Fig. 4.

The strain effect is reduced as temperature increases up to the bonding temperature,  $300^\circ\text{C}$ , because the compressive strain on the bonded film decreases with increasing temperature, and finally becomes zero at the bonding temperature. Therefore, the decreasing strain makes the discrepancy in electrical conductivity decrease with temperature up to the bonding temperature, or until substrate conduction starts to affect the conductivity in the sample on the InP substrate. Beyond the bonding temperature, the strain becomes tensile, and the magnitude of the tensile strain increases with increasing temperature. The conductivity change due to the tensile strain at 840 K was calculated to be  $8.7 \Omega^{-1} \text{ cm}^{-1}$ , assuming the same increasing rate of conductivity per strain as in Fig. 9. This change is less than 2% of the conductivity value,  $550 \Omega^{-1} \text{ cm}^{-1}$ , measured at 840 K.

## CONCLUSIONS

We have established a device fabrication method based on  $\text{SiO}_2$ - $\text{SiO}_2$  bonding to prepare samples for high-temperature measurements of thermoelectric and electrical properties of thin-film III-V semiconductors, especially for materials that are affected by substrate parasitic conduction at high temperature. This sample preparation method includes high-temperature surface passivation with ICP PECVD  $\text{SiN}_x$  and PECVD  $\text{SiO}_2$  layers, and high-temperature metallization with a Ti-W-N diffusion barrier. Electrical conductivities and Seebeck coefficients of  $2 \mu\text{m}$  0.3% and 0.6% ErAs:InGaAlAs thin films were measured up to 840 K, and the 0.6% Er sample showed a thermoelectric power factor of  $3.17 \times 10^{-3} \text{ W m}^{-1} \text{ K}^{-2}$  at 840 K with no substrate effect included. The discrepancy in the electrical conductivities between the original thin film on the InP substrate and the one bonded to a sapphire substrate was mainly attributed to the effect of strain. The discrepancy was, however, quite small, estimated as within 2% at 840 K. The proposed sample fabrication and measurement methods can potentially be used in many applications, including various energy conversion applications, that utilize thin-film semiconductor materials at high temperatures.

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