UNIVERSITY OF CALIFORNIA, SAN DIEGO

Comprehensive Reduction of Real and Complex Distribution Feeder Models

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Engineering Sciences (Mechanical Engineering)

by

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2018

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University of California, San Diego

2018

DEDICATION

This thesis is dedicated to anyone who is underprivileged, under-educated, or oppressed but knows there is something bigger for them. You can accomplish anything or be anyone if you put in the required time. You are not trapped where you are now. Fight to make the world a place you want to live in. Don't let anyone stop you.

EPIGRAPH

The person who acquires the ability to take full possession of their mind may take possession of anything else to which they are justly entitled.

—Andrew Carnegie

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

In my time at UCSD I was fortunate to work with a world class set of researchers, who I must thank for helping me grow as a researcher, but more importantly as an individual.

First, I would like my advisor, Jan Kleissl. Jan's kind and calm nature is truly rare in this world, but is a model that I would like to see adopted. He was always available when needed and understanding of complexities involved in a grad students life. I am sure having a different advisor would of made my graduate experience a much less enjoyable one.

This work would not be complete without acknowledging my postdoc and freind Vahid R. Disfani. The massive donation of time Vahid gave to my education and research is the sole reason I was able to complete my degree in an unfamiliar field in under four years. I am eternally grateful and look forward to a continued partnership in the future.

Similarly, I would like to acknowledge Hamed Valizedeh Haghi for his contribution to my work. Despite the brevity, our time together has been extremely productive. Simply speaking with him has provided a whole world of education.

San Diego, thank you for providing beautiful nature and year-round mild weather. Thank you also for being so ridiculously expensive that I never got to comfortable on a graduate student salary.

Finally, I need to thank my family and freinds. To my father, mother, brother, stepfather, stepmother, aunts, and grandparents: thanks you for the continued support, you all know how much you mean to me, and I know you are enjoying the fruits of my hard work as much as I am. To my girlfriend Christine, thank you for the day to day sanity measures and giving up your whole life to move out west and allow me to chase my dreams.

The text in Chapter 1 is sampled from i) Multiphase Distribution Feeder Reduction, Pecenak, Z.K., Disfani, V.R., Reno, M., Kelissl, J., *IEEE Transactions on Power Systems*, 2017; ii) Inversion Reduction Method for Real and Complex Distribution Systems, Pecenak, Z.K., Disfani, V.R., Reno, M., Kelissl, J.,; iii) Aggregation of Voltage Dependant Inverters during

Distribution Feeder Reduction, Pecenak, Z.K., Haghi, H.V., Disfani, V.R., Reno, M., Kelissl, J.,. The dissertation author is the primary investigator and author of all the articles.

The text and data in Chapter 2, in full, is a reprint of the material as it appears in Multiphase Distribution Feeder Reduction, Pecenak, Z.K., Disfani, V.R., Reno, M., Kelissl, J., *IEEE Transactions on Power Systems*, 2017. The dissertation author is the primary investigator and author of this article.

The text and data in Chapter 3, in full, is submitted to *IEEE Transactions on Power Systems* under the title Inversion Reduction Method for Real and Complex Distribution Systems, Pecenak, Z.K., Disfani, V.R., Reno, M., Kelissl, J.,.The dissertation author is the primary investigator and author of this article.

The text and data in Chapter 4, in full, is in preperation for submition to *IEEE Transactions on Power Systems* under the title Aggregation of Voltage Dependant Inverters during Distribution Feeder Reduction, Pecenak, Z.K., Haghi, H.V., Disfani, V.R., Reno, M., Kelissl, J.,.The dissertation author is the primary investigator and author of this article.

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SELECTED PUBLICATIONS

Pecenak, Z.K., Haghi, V.H., Disfani, V.R., Reno, M., Kleissl, J. "Aggregation of Voltage Dependant Inverters During Distribution Network Reduction", *IEEE Trans. on Power Sys., submitting*, 2018.

Pecenak, Z.K., Disfani, V.R., Reno, M., Kleissl, J. "Inversion Reduction Method for Real and Complex Distribution Feeder Models", *IEEE Trans. on Power Sys., submitted*, 2018.

Pecenak, Z.K., Disfani, V.R., Reno, M., Kleissl, J. " Multiphase Distribution Feeder Reduction", *IEEE Trans. on Power Sys.*, 2017.

Pecenak, Z.K., Disfani, V.R., Reno, M., Kleissl, J. " Smart Inverter Impacts on California Distribution Feeders with Increasing PV Penetration: A Case Study", *IEEE PESGM*, 2017.

Pecenak, Z.K., Mejia, F., Kurtz, B., Evans, A., Kleissl, J. "Simulating Irradiance Enhancement Dependence on Cloud Optical Depth and Solar Zenith Angle", *Solar Energy*, 136, 2016.

ABSTRACT OF THE DISSERTATION

Comprehensive Reduction of Real and Complex Distribution Feeder Models

by

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Doctor of Philosophy in Engineering Sciences (Mechanical Engineering)

University of California, San Diego, 2018

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The US power grid is an engineering marvel. However, it was not designed with the consideration of renewable energy, energy storage, two way electricity transfer from electric vehicles, advanced control devices, or advanced metering systems. In order to properly integrate such devices, power system planning studies in which the proposed device is simulated under yearly operation is performed on a real/existing circuit model are performed. However, the studies are extremely intensive with respect to computational and temporal resources due to: i) the size and complexity of real circuits ii) The daily and seasonal variation in load consumption and available renewable resources iii) The number of operating states of the device.

Model reduction is a common approach in big data applications to reduce the burden.

However, much like the grid itself, traditional methods of circuit reduction are not designed for the growing complexity of distribution side circuits. Specifically, there are no methods in literature that consider circuits with i) unbalance in loading and generation between phases ii) unbalance in distribution line impedances between phases iii) mutual coupling between phases iv) shunt capacitance in distribution lines v) multiple voltage levels. Further, topics like reduction of forecasted generation/consumption time series or aggregation of voltage-controlled devices have not been discussed.

In this thesis, a circuit reduction technique that is specifically formulated for the complexities of real distribution feeders is introduced. The comprehensive methodology is derived from first principles to overcome all of the limitations of circuit reduction techniques listed above. Detailed algorithms of our recommended implementation are given for increase the utility to researchers.

An extensive validation is performed on several real circuit to develop a granular understanding of error sources. It is shown that for even the largest publicly available models, the method is highly accurate, with time savings of up to 99% per simulation, while being flexible enough to handle a range of modeling or control complexities.

Chapter 1

Introduction

The aging infrastructure of the US electric grid combined with increasingly severe weather caused by climate change is threatening the reliability of electric delivery. Furthermore, the cost to rebuild and improve the infrastructure is putting pressure on tight state budgets [3]. This and environmental concerns have caused investor owned utilities (IOUs) and policy makers to invest in the next generation of grid deployable devices to improve reliability, voltage and frequency regulation, and advanced metering capabilities. Therefore, emerging technologies of distributed energy resources (DER) such as distributed photovoltaic (PV) systems, other distributed generators (DG), energy storage systems (ESS), and electric vehicle (EV) charging infrastructure will soon enter distribution grids at high penetrations.

In addition to evaluation of economic benefits and costs associated with integration of DER, their technical impacts such as voltage and frequency must be studied in realistic scenarios. Numerical simulations are generally easy to set up and allow investigations of a large number of configurations. However, a typical utility distribution feeder model contains a node for every customer and therefore consists of thousands of buses. While a single power flow completes after a few seconds on a workstation, consideration of multiple distribution feeders, large parametric analyses, or investigation at fine time scales, simulation time can become prohibitive. While

previously it may have been sufficient for a utility to consider a mininimum and maximum load case to optimize voltage regulators to ensure voltage compliance, the emergence of high penetration of PV introduces challenges to this paradigm: (i) weather and seasonal variations of solar generation are typically examined using 8760 hourly times in a year (ii) some PV impacts such as tap operations can only be accurately benchmarked through simulation at time steps commensurate with tap operation control delays and cloud passages (seconds) (iii) worst cases are increasingly hard to define (high load and low solar and high solar variability), motivating a probabilistic framework for allocating future PV installations [4] and for decision-making in general.

So far, these scenarios have primarily materialized in distribution system research [5, 6, 7]. However, in the near future, utilities and their consultants will likely adopt these practices. DG interconnection studies performed by utilities on proposed installations that do not pass the initial screening requirements can then result in delays on the project due to long simulation times [8, 9]. Further, in-depth studies of the dynamic and transient behaviors of several devices in complex systems are not feasible without the aid of super computers.

This predicament closely parallels the issues faced in the study of big data, where observing the full set of data is infeasible. In that field, model or dimensional reduction is a popular approach to overcome this problem [10]. A similar approach has been explored in power systems, where the circuit to be studied is reduced to a smaller equivalent.

In fact, the concept of model reduction can be traced back to the introduction of Kron reduction in 1939 [11]. This simplistic method proposes a methodology to remove parts of the circuit with negligible powerflow through them. The method is mathematically exact, and very accurate, but suffers from lack of general usage.

The field of model reduction was improved with the introduction of the Ward reduction technique a decade later [12]. The technique which uses matrix representations of the system properties finds equivalent current injections for a reduced circuit and solves the powerflow given

that as input. However, the Ward reduction requires an initial solution to the power flow (which increases computational cost) and assumes fixed current loads, which is not representative of common electric loads.

A slew of other methods have been developed in the period between Ward reduction and present day. In reference [13] four of the more popular network reduction techniques are discussed and compared for performance in static power flow simulations: i) Ward reduction [12], ii) Kron Reduction [11], iii) Dimo's Method [14], and iv) Zhukov's reduction [15]. For the two feeders investigated (IEEE 14 bus and IEEE 118 bus), all methods were shown to produce significant error in voltage due to reduction (> 0.01 pu). Surprisingly, the Ward reduction method produced the lowest error overall.

However, all of the methods introduced above are designed for transmission networks which tend to be balanced systems designed with symmetrical components. Applying these methods to distribution feeders is not possible due to the imbalanced nature of phases of distribution systems.

The first attempt at reduction of distribution models was proposed in [16]. The methodology splits and aggregates load consecutively into neighboring buses using an impedance weighting. The accuracy of the method is tested against a 1000-node realistic feeder, where the maximum absolute deviation of voltage magnitudes between the reduced and original feeder is less than 103 V. However, as stated by the authors, the method is only applicable to simplified distribution networks without any unbalanced load or PV, unbalanced wire impedances, mutual coupling, or shunt capacitance and is still based on a constant current assumption. Moreover, in the load and PV aggregation process, the algorithm proposed in [19] does not consider the original positions of loads and PV to simulate of spatial variability. For these reasons, application of the methodology to real feeders results in large errors.

The segmentation method introduced in reference [17] introduces the use of a constant power assumption to the literature on distribution network reduction. The methodology recursively

replaces model segments between two buses of interest with characteristic equations representing a simpler topology. The methodology is tested on Feeder J1 [18] and produces a small max voltage error of ($O(10^{-3})$). However the authors make no mention of error with changing load conditions or reduction across different voltage levels, and an initial power flow is still needed as a system input.

To the author's knowledge there are no other works focused on circuit reduction for distribution feeders. The work in this thesis addresses the shortcomings in a single methodology that can reduce circuits with

- multiphase connections through out the entire network
- mutual coupling between multiphase unbalanced lines
- unbalanced loads and generation
- spatial variation in load and generation
- shunt capacitance in distribution lines
- multiple voltage levels
- voltage shifting transformers

that accounts for changing demand and generation without requiring an initial powerflow. This is addressed in chapters 2 and 3 of this thesis. For the method developed, novel algorithms for converting between elementary power systems equations and commercial power system solver formats are given.

In Chapter 4, the first attempt at reduction of control devices which are dependent on local voltage measurements is attempted. Building on the advanced circuit reduction algorithm, we integrate a novel voltage estimation technique to replace the required measurements, which produces equivalent control behavior.

In Chapter 5, closing remarks are made about the work, including future work and other uses for the circuit reduction technique developed.

Chapter 2

Multiphase Distribution Feeder Reduction

2.1 Introduction

The aging infrastructure of the US electric grid combined with increasingly severe weather caused by climate change is threatening the reliability of electric delivery. Furthermore, the cost to rebuild and improve the infrastructure is putting pressure on tight state budgets [3]. This and environmental concerns have caused investor owned utilities (IOUs) and policy makers to invest in the next generation of grid deployable devices to improve reliability, voltage and frequency regulation, and advanced metering capabilities. Therefore, emerging technologies of distributed energy resources (DER) such as distributed photovoltaic (PV) systems, other distributed generators (DG), energy storage systems (ESS), and electric vehicle (EV) charging infrastructure will soon enter distribution grids at high penetrations.

In addition to evaluation of economic benefits and costs associated with integration of DER, their technical impacts such as voltage and frequency must be studied in realistic scenarios. Numerical simulations are generally easy to set up and allow investigations of a large number of configurations. However, a typical utility distribution feeder model contains a node for every customer and therefore consists of thousands of buses. While a single power flow completes after

a few seconds on a workstation, consideration of multiple distribution feeders, large parametric analyses, or investigation at fine time scales, simulation time can become prohibitive. While previously it may have been sufficient for a utility to consider a mininimum and maximum load case to optimize voltage regulators to ensure voltage compliance, the emergence of high penetration of PV introduces challenges to this paradigm: (i) weather and seasonal variations of solar generation are typically examined using 8760 hourly times in a year (ii) some PV impacts such as tap operations can only be accurately benchmarked through simulation at time steps commensurate with tap operation control delays and cloud passages (seconds) (iii) worst cases are increasingly hard to define (high load and low solar and high solar variability), motivating a probabilistic framework for allocating future PV installations [4] and for decision-making in general.

So far, these scenarios have primarily materialized in distribution system research [5, 6, 7]. However, in the near future, utilities and their consultants will likely adopt these practices. DG interconnection studies performed by utilities on proposed installations that do not pass the initial screening requirements can then result in delays on the project due to long simulation times [8, 9]. Further, in-depth studies of the dynamic and transient behaviors of several devices in complex systems are not feasible without the aid of super computers.

This dilemma has driven research to develop analytical methods to reduce the computational time required for large systems simulations while maintaining the accuracy of the solutions. A classical method for reducing system size is through the use of Kron reduction techniques, where buses with either no current or voltage are removed from the circuit [11]. While Krons reduction is valid and useful, the amount of reduction that is achievable in most systems is limited. Several authors have proposed reductions of the bulk electric transmission system through the use of equivalent collector systems, power injection matrix reduction, and bus aggregation [19, 20]. However, these methods fail to address the special characteristics of distribution systems such as multiphase connections, unbalanced loads, and mutual impedance.

Several other approaches in the literature propose analytical methods to entirely remove the need for a power flow solver. In [21], a method using base case circuit information is developed to find the optimal two-bus equivalent system of a transmission system for voltage stability analyses. Despite the high speed and accuracy of the method, the resulting circuit offers little flexibility to carry out investigations on other aspects of the power grid beyond transmission voltage stability. Another two-bus equivalent circuit formulation is proposed in [22] which is composed of a slack bus, equivalent impedance, and a single aggregated PV and load bus. The two-bus system allows quick and accurate investigation of voltage extrema in the circuit due to high variability of PV power output. However, the major drawback of this method is the fact that it is only able to simulate a single bus at a time and does not offer the flexibilitiy for comprehensive studies considering the coordinated behavior of several devices.

In addition to speeding up QSTS simulations, circuit reduction has been a research interest for several other applications. Specifically, methods have been proposed to reduce the circuit models for real-time control or hardware-in-the-loop (HIL) testing environments [23] that cannot handle the complexity and number of buses in a full distribution system model. Detailed dynamic analysis of large distribution systems is also often impractical in electromagnetic transient programs without network reduction [24]. With more DER being installed, there has also been a focus to expand the circuit reduction methods developed for equivalencing large wind farms for transmission dynamic [25], voltage ride-through [26], and harmonic studies [27]. These types of co-simulations with both transmission and distribution often reduce the complexity of the distribution system model by aggregating distributed generation into an equivalent dynamic model [28]

A novel methodology to reduce a balanced distribution feeder to any desired set of buses is presented in [16]. The methodology splits and aggregates load consecutively into neighboring buses using an impedance weighting. The accuracy of the method is tested against a 1000-node realistic feeder, where the maximum absolute deviation of voltage magnitudes between

the reduced and original feeder is less than 10^{-3} V. However, as stated by the authors, the method is only applicable to simplified distribution networks without any unbalanced load or PV, unbalanced wire impedances, mutual coupling, or shunt capacitance. Moreover, in the load and PV aggregation process, the algorithm proposed in [16] does not consider the original positions of loads and PV to simulate of spatial variability. For these reasons, application of the methodology to real feeders results in large errors.

This paper builds upon [16] and resolves most of its limitations. An analytical method is proposed to reduce complex multiphase distribution feeders to a subset of buses (the critical buses (CB)) of interest. That is, the algorithm is applicable to *p*-phase distribution feeders with unbalanced loads and PV, unbalanced wire impedance, and mutual coupling between phases. The work is further extended through preserving the spatial diversity of solar and load on the circuit in the reduction process. The accuracy of the reduction is investigated on a real California feeder in reference to the complete simulation. Also, the sensitivity of voltage errors to location of the CB, types of loads, solar irradiance, PV penetration level, and bus distance from substation is investigated. Finally, the computational cost savings are quantified.

Thus, the contributions of this paper to the literature on network reductions are as follows:

1. Development of the first methodology to reduce real and complex distribution feeders which are unbalanced in nature. Such feeders can include:
   (a) multiphase connections through out the entire network
   (b) mutual coupling between multiphase unbalanced lines
   (c) unbalanced loads and generation
   (d) spatial variation in load and generation
2. The mathematical derivation and algorithm to implement the methodology are provided.
3. A novel methodology for aggregating temporal and spatial variation of load and generation

across the network.

4. Development of a topology detection algorithm, which serves as a platform for manipulating values between buses.

5. Quantification of reduction errors for multiple load types, load conditions, and topology.

The rest of the paper is organized as follows. Section 2.2 explains the mathematical formulation of the reduction method. Section 3.5 proposes the algorithms to reduce the feeder to the desired CB. The simulation results and validation of the accuracy of the reduction method are provided in Section 3.6, along with a discussion on the computational advantages of the reduction. Section **??** concludes the paper.

2.2 Analytical Approach

2.2.1 Assumptions

We assume a radial network in a p-phase configuration with n buses and m nodes where a node refers to the individual phases of connections on a bus, such that $m \leq p * n$. For the purpose of clarity, the derivation and analysis is performed for a 3 phase system with multiphase connections (p=3).

Consistent with [16, 12, 29, 30], the power injections and absorption on load and PV buses are assumed to be fixed current for the purpose of mathematical derivation (eq. 2-10). This assumption causes errors for constant PQ and constant impedance loads as well as for the PV systems which are typically modeled as constant PQ. The fixed current assumption is supported by research on conservation voltage reduction (CVR) [18], which showed that every 1% reduction in voltage leads on average to a 0.8% reduction in real power (CVR=0.8), while fixed current loads would cause CVR=1%. In spite of the error, methods using this assumption have shown to

provide higher accuracy than other leading methods [31, 13, 32]. Further, the results provided in [33] demonstrate that the load type selected has minor effects on the simulation results.

However, it should be noted that the load types used in the feeder are kept during the aggregation process, as opposed to being changed to constant current. This is carried out by aggregating loads into groups of like load types in the final reduced feeder. The impacts of using different load types on the voltage error between the original and reduced feeder are investigated in Section 3.6.

In our work it is assumed that neutral connections could be provided by local grounding at any bus. Thus, the line models in this work do not include the neutral wire. In our algorithm, all loads are transformed to the equivalent Y-connected loads to derive the individual loads connected between each phase and ground. These loads define the equivalent single-phase loads on the reduced feeder. Further, the secondary side of the substation transformers are grounded and it remains the same in the reduced feeder since there is no reduction on transformers. Further, perfect grounding is assumed at each bus, thus neglecting the return current in the system, which can lead to inaccuracies under highly imbalanced conditions in models with imperfect grounding.

Finally, line capacitance is not treated in this model and assumed to be zero, thus rendering the method inaccurate for models with non-zero values. Reduction of shunt capacitance is a focus of future work.

2.2.2 Reduction Method

A bus is composed of several nodes N_i, representing the phases of connection. In a real multiphase distribution feeder, the number of phases between adjacent buses is often different, especially away from the main branch. Furthermore, PV and load on a bus are not necessarily evenly distributed between phases. The reduced feeder is required to maintain the original distribution of PV, load, and impedance by phase, thus it is necessary to aggregate the feeder at the phase level. Our comprehensive feeder reduction algorithm addresses all these special

characteristics of distribution feeders.

The method proposed in this paper, which is based on defining the line impedance by Z matrices, is a highly generalized reduction technique applicable to distribution feeders with multiphase connections through out the entire network, mutual coupling between multiphase unbalanced lines , unbalanced loads and generation , spatial variation in load and generation It employs a recursive bus reduction technique which gradually removes non-critical buses (NCB) until only the set of selected CB remain (see section 2.3.2). At every step, one NCB is removed and its load and PV systems are allocated between the adjacent CB, while total PV and load is preserved.

Fig. 2.1 shows the feeder structure at one of the intermediate feeder reduction steps in order to conceptualize the different types of reduction, which are described in Section 3.5 in detail. The objective in this feeder reduction is to remove the NCB while maintaining the voltage on the CB.

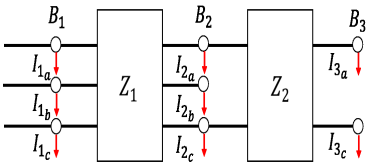


Figure 2.1: Depiction of three bus subsection of the feeder in which the middle bus, B_2, is connected upstream to a 3 phase bus B_1 and connected downstream to a 2-phase bus B_3. The red arrows represent current flow out of the nodes.

Z_1 and Z_2 are multi-phase line impedance matrices, e.g.

$$Z_1 = \begin{bmatrix} Z_{1,aa} & Z_{1,ab} & Z_{1,ac} \\ Z_{1,ba} & Z_{1,bb} & Z_{1,bc} \\ Z_{1,ca} & Z_{1,cb} & Z_{1,cc} \end{bmatrix} \tag{2.1}$$

where the diagonal elements denote the self-impedances of all phases a, b, c and the off-diagonal elements are associated with the mutual impedance between different phases, which are not

necessarily identical. The procedure is demonstrated through two scenarios;

2.2.3 Type 1: End bus Reduction

First, assume that buses B_2 in Fig. 2.1 is CB and the objective is to remove the bus B_3 which is NCB. If I_i and V_i respectively denote the 3-phase net current injection vectors and 3-phase voltage vectors on bus B_i, we have:

$$\begin{bmatrix} V_{3,a} \\ 0 \\ V_{3,c} \end{bmatrix} = \begin{bmatrix} V_{2,a} \\ 0 \\ V_{2,c} \end{bmatrix} - \begin{bmatrix} Z_{2,aa} & 0 & Z_{2,ac} \\ 0 & 0 & 0 \\ Z_{2,ca} & 0 & Z_{2,cc} \end{bmatrix} \times \begin{bmatrix} I_{3,a} \\ 0 \\ I_{3,c} \end{bmatrix} \tag{2.2}$$

$$\begin{bmatrix} V_{2,a} \\ V_{2,b} \\ V_{2,c} \end{bmatrix} = \begin{bmatrix} V_{1,a} \\ V_{1,b} \\ V_{1,c} \end{bmatrix} - \begin{bmatrix} Z_{1,aa} & Z_{1,ab} & Z_{1,ac} \\ Z_{1,ba} & Z_{1,bb} & Z_{1,bc} \\ Z_{1,ca} & Z_{1,cb} & Z_{1,cc} \end{bmatrix} \times \begin{bmatrix} I_{2,a} + I_{3,a} \\ I_{2,b} \\ I_{2,c} + I_{3,c} \end{bmatrix}. \tag{2.3}$$

From (2.2) and (2.3) the voltage vectors V_1 and V_2 can be written as functions I_2 and I_3 which exclude V_3. Therefore, the bus B_3 can be removed from the feeder by just transferring its current injections to B_2.

2.2.4 Type 2: Middle Bus Reduction

In this type of reduction, B_1, B_2, and B_3 are three consecutive buses in one of the intermediate reduction steps where B_2 is the NCB to be removed, B_3 is CB, and B_1 can be a CB or NCB. Without loss of generality, let us assume a special case where the line between B_2 and

B_3 is also three-phase, *i.e.* $Z_2 \in \mathbb{C}^{3\times 3}$. Thus, we have:

$$V_3 = V_2 - Z_2 \times I_3 \tag{2.4}$$

$$V_2 = V_1 - Z_1 \times (I_2 + I_3). \tag{2.5}$$

Replacing voltage parameters corresponding to B_2 by the parameters of the neighboring buses, the voltage vector V_3 is represented as below

$$\begin{aligned} V_3 = V_1 - Z_1 \times (I_2 + I_3) - Z_2 \times I_3 = \\ V_1 - (Z_1 + Z_2) \times (I_3 + (Z_1 + Z_2)^{-1} \times Z_1 \times I_2), \end{aligned} \tag{2.6}$$

which implies a single three-phase line between B_1 and B_3 with an impedance matrix equal to Z_{eq}=Z_1+Z_2, while the new load at B_3 includes a portion of load from the removed bus in addition to its original load. Due to the symmetry of the example network, the load on bus B_1 must be updated to I_1+$(Z_1$+$Z_2)^{-1} \times Z_2 \times I_2$. Therefore, total feeder loads remain the same.

In general, if any of the lines between the original buses lack some phases, the process is slightly different. In such conditions, the equivalent line includes only the common phases between Z_1 and Z_2. All loads on the phases which are just connected to one of adjacent buses must be transferred to the same phase of that bus.

As a general case, it is assumed here that the number of phases of the lines Z_1 and Z_2 are not the same, *e.g.* $Z_1 \in \mathbb{C}^{3\times 3}$ and $Z_2 \in \mathbb{C}^{2\times 2}$. These lines connect three buses with phase nodes $\phi(B_1) = \{a,b,c\}$, $\phi(B_2) = \{a,b,c\}$, and $\phi(B_3) = \{a,c\}$ as depicted in Fig. 2.1. For a NCB with multiphase connections, such as the given example, it is necessary to identify the phases common and not common to both lines.

To avoid zero determinants in the inversion of Z_{eq}, a reduced verion of the matrices is introduced. Assuming that Z_1^r and Z_2^r are the reduced format of Z_1 and Z_2 which only includes the elements corresponding to phases $\{a,c\}$=$\phi(B_1) \cap \phi(B_2) \cap \phi(B_3)$, the equivalent impedance is

equal to $Z_1^r + Z_2^r$, as defined in (2.7).

$$Z_{eq} = \begin{bmatrix} Z_{1,aa} & Z_{1,ac} \\ Z_{1,ca} & Z_{1,cc} \end{bmatrix} + \begin{bmatrix} Z_{2,aa} & Z_{2,ac} \\ Z_{2,ca} & Z_{2,cc} \end{bmatrix} \tag{2.7}$$

Since there is no connection between B_1 and B_3 through the uncommon phase, any elements corresponding to this phase in the equivalent impedance disappear.

For uncommon phases, all load and PV connected to the middle bus are transferred to the bus which includes the uncommon phase. For example, all load and PV on phase b of bus B_2 are transferred to phase b of bus B_1 (Fig. 2.1). However, the load and PV on common phases of the middle bus are allocated between the other two buses according to the impedance matrices of Z_1^r and Z_2^r.

$$\begin{bmatrix} I_{3,a} \\ I_{3,c} \end{bmatrix}^{\text{new}} = \begin{bmatrix} I_{3,a} \\ I_{3,c} \end{bmatrix} + Z_{eq}^{-1} \times \begin{bmatrix} Z_{1,aa} & Z_{1,ac} \\ Z_{1,ca} & Z_{1,cc} \end{bmatrix} \times \begin{bmatrix} I_{2,a} \\ I_{2,c} \end{bmatrix} \tag{2.8}$$

$$\begin{bmatrix} I_{1,a} \\ I_{1,c} \end{bmatrix}^{\text{new}} = \begin{bmatrix} I_{1,a} \\ I_{1,c} \end{bmatrix} + Z_{eq}^{-1} \times \begin{bmatrix} Z_{2,aa} & Z_{2,ac} \\ Z_{2,ca} & Z_{2,cc} \end{bmatrix} \times \begin{bmatrix} I_{2,a} \\ I_{2,c} \end{bmatrix} \tag{2.9}$$

$$I_{1,b}^{\text{new}} = I_{1,b} + I_{2,b} \tag{2.10}$$

2.2.5 PV and load allocation

To aggregate time-series load shapes a complex matrix $W \in C^{(3n \times 3n)}$ maps the PV or load from nodes of NCB to the CB nodes which it is transferred to. The elements W_{jj} are initialized as 1 if there is a PV/load on that node, and it is 0 otherwise. In each step of feeder reduction W is updated to represent the contribution of PV/load from the removed NCB onto the phases of the CB and rows corresponding to NCB are removed.

For middle bus reduction we define the ratio matrices $R_1 \in \mathbb{C}^{3\times3}$ and $R_2 \in \mathbb{C}^{3\times3}$. Matrix elements corresponding to the common phases between the three buses are equal to elements of the reduced matrices, $R_1^r = Z_{eq}^{-1} Z_2^r$ and $R_2^r = Z_{eq}^{-1} Z_1^r$. For the elements of R_1 and R_2 corresponding to the uncommon phases off-diagonal elements are all zero, except elements corresponding to common phases with only bus, in which the element is one. For the example shown in Fig. 2.1 the ratio matrices R_1 and R_2 are:

$$R_1 = \begin{bmatrix} r^r_{1,aa} & 0 & r^r_{1,ac} \\ 0 & 1 & 0 \\ r^r_{1,ca} & 0 & r^r_{1,cc} \end{bmatrix}, R_2 = \begin{bmatrix} r^r_{2,aa} & 0 & r^r_{2,ac} \\ 0 & 0 & 0 \\ r^r_{2,ca} & 0 & r^r_{2,cc} \end{bmatrix} \tag{2.11}$$

The ratio matrices R_1 and R_2 express how load and PV on the middle bus are allocated between the other buses:

$$w_{B_1} = w_{B_1} + R_1 \cdot w_{B_2}, w_{B_3} = w_{B_3} + R_2 \cdot w_{B_2} \tag{2.12}$$

The weight submatrices $w \in \mathbb{C}^{3\times3}$, corresponding to the elements of W representing the two CBs are updated to reflect the phase-wise addition of PV/load from the NCB (B_2) whose rows are removed.

For end bus reduction where B_3 is to be removed, w_{B_2} will be updated to $w_{B_2} + w_{B_3}$ and the rows corresponding to B_3 are removed.

Following the reduction to the final set of nodes, W can be used to map the original PV/load time series profiles to the reduced set.

2.3 Feeder Reduction Algorithm

2.3.1 Introduction

The steps of the feeder reduction of a large and complex distribution feeder are broken out next. The procedure of bus selection by the user and the algorithm is discussed (section 2.3.2). The steps of recursively removing NCB from the branches of the feeder following the analytical approach of section 2.2.3 is given in section 2.3.3. A novel approach to handling the reduction between multiphase connections with mutual coupling is discussed in section 2.3.4 based on the methodology of section 2.2.4. The weighting system to maintain solar and load variability proposed in 2.2.5 is implemented in section 2.3.5.

2.3.2 Critical Bus Selection and Identification

CB are defined as the buses that are to remain in the final reduced feeder configuration. While the number of CB can range from one bus to all of the buses, generally CB are a small subset of the total buses of the feeder. There are three types of CB; i) user-selected CB, ii) CB that host special equipment, and iii) topology CB.

User-selected CB are those of interest to the particular study being performed, such as the location where a large PV system is to be interconnected. CB that host special equipment are buses with shunt capacitors, voltage regulators, and distribution transformers, which are automatically classified as CB.

Based on this initial set of CB, the algorithm must select additional CB which are required to preserve the topology of the feeder. Topology CB are buses on the junctions between branches with CB. The algorithm identifies the topology of the feeder to determine where the user-selected CB or CB with special equipment are located, selects the topology CB, and determines which buses must be removed. A modified version of the recursive topology detection algorithm proposed in [34] has been adopted in this paper.

In the method, adjacent buses to any bus i, as identified through connected phases in the line data or the admittance matrix, form the full set of neighbor buses N_i. Among the neighbors of bus i, the closest one towards the substation is called the parent of bus i (P_i). The remaining buses of N_i form its children set C_i. The offspring set of bus i, denoted by Ω_i, is recursively defined as the union of the children of bus i (C_i) and their offspring set i.e. $\Omega_i = C_i \bigcup (\bigcup_{k \in C_i} \Omega_k)$. The ancestor set of bus i, which is denoted by Λ_i, also has a recursive definition of the bus i's parent and its parent's ancestors, *i.e.* $\Lambda_i = P_i \bigcup \Lambda_{P_i}$.

The full algorithm is presented in **Algorithm 1**. The algorithm starts from the substation $(i = 1)$, finds its children and updates the sets of global variables Λ and Ω. The algorithm is then repeated for each child until the entire network is processed.

Algorithm 1 Topology Detection

Initialize $\Lambda_i = \emptyset$ and $\Omega_i = \emptyset$
identify any bus connected to bus i to form the neighbor set M_i.
Define the children set $C_i = \{k : k \notin \{i\} \cup \Lambda_k\}$
for any bus l in C_i **do**
  let $P_l = i$ and $\Lambda_l = \{i\} \cup \Lambda_i$
  let $i = l$ and run **Algorithm 1**
  $\Omega_{P_i} = \Omega_{P_i} \cup \{i\} \cup \Omega_i$
end for
Return the sets Λ_i and Ω_i

After the feeder topology is detected, among the common ancestors of each pair of critical buses, the one with higher distance from the substation is considered as the junction of those two critical buses and is added to the list of critical buses. It is notable that the substation bus must be always a critical bus.

2.3.3 Branch Reduction, End Bus

Following the concept of graph theory the feeder is considered as a tree where the buses and distribution lines are equivalent to vertices and edges, and the part of the feeder that interconnects the CB is the main tree which just includes the ancestors of all critical buses. The

first objective in the feeder reduction algorithm is to remove all NCB off the main tree. The loads and PV on these NCB are aggregated on the closest CB belonging to the main tree.

Algorithm 2 elaborates how the buses off the main tree are reduced, where $w_i \in \mathbb{R}^{(3\times n)}$ consists of three rows of the matrix of W corresponding to the different phases of bus i.

Algorithm 2 Reduction Off Main Tree

Identify the feeder topology (obtain the sets Λ_i and Ω_i for all buses i)
Form the set of CB
Form the set of all buses on the main tree, $T = \bigcup_{i\in CB} \Lambda_i$
Initialize the set of NCB: $R = \emptyset$
for any CB $i \in T$ **do**
  for any $l \in C_i$ if Ω_l excludes any critical bus **do**
    let $R = R \cup \{l\}$, $w_i = w_i + w_l$, and $w_l = 0$
    for any bus k downstream of bus i ($k \in \Omega_l$) **do**
      let $R = R \cup \{k\}$, $w_i = w_i + w_k$, and $w_k = 0$
    end for
  end for
end for
Remove the buses belonging to R from the feeder
Remove the row vectors w_r from matrix W for any $r \in R$

Fig. 2.2 also illustrates a case where the buses off the main tree are reduced on the CB. After this step, the remaining feeder includes all CB and some NCB which reside on the main tree.

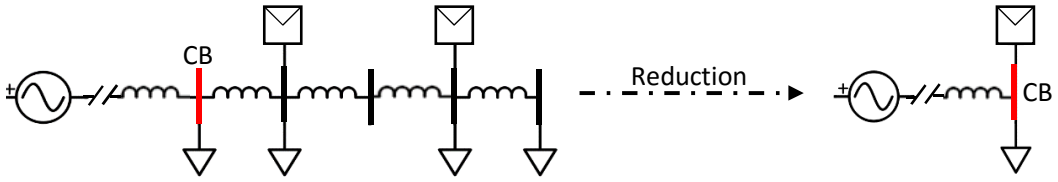


Figure 2.2: A conceptual depiction of the removal of all NCB beyond a CB. The load (triangles) and PV (squares) from the removed NCB are aggregated to the CB. This process is carried out recursively for all CB off the main tree.

2.3.4 Main Tree Reduction, Middle Bus

The impedance that connects the remaining buses composes the characteristic impedance of the reduced circuit and thus must be aggregated as opposed to removed. The methodology as described in 2.2.4 is shown for a simple three bus system, but for larger feeders the process is carried out in the reduction by successively removing NCB parents of CB until the NCB are completely removed from the circuit. **Algorithm 3** summarizes the reduction of the NCB on the main tree.

Algorithm 3 Reduction On Main Tree

Identify the new feeder topology reduced by **Algorithm 2**
Form the set of CB
Initialize the set of NCB: $R = \emptyset$
for any $i \in$ CB **do**
  Sort Λ_i based upon distance from substation ascendingly
  for any $k \in \Lambda_i$ (in order) **do**
    if $((\{k\} \bigcup \Omega_j) - (\{i\} \bigcup \Omega_i))$ which excludes any CB **then**
      let $w_i = w_i + R_2 \cdot w_k$ and $w_{P_k} = w_{P_k} + R_1 \cdot w_k$
      let $w_k = 0$ and $R = R \bigcup \{k\}$
    end if
  end for
end for
Remove the NCB belonging to R from the feeder
Remove the row vectors w_r from matrix W for any $r \in R$

2.3.5 The Final Reduced Feeder

The final configuration contains only CB which are connected through a set of equivalent distribution lines. Fig. 2.3 displays the CB identified by the algorithm following the user-selection of nine CB. The algorithm chose on additional CB due to the presence of a capacitor and 9 topological CB.

The CB are composed of nodes with various weighting vectors. The final matrix W is used both to calculate the equivalent PV and load sizes and to compute the aggregate generation

and demand profiles on the final set of CB. Normalizing the generation and demand profiles based on the equivalent sizes of PV and load generates the temporal PV and load loadshapes. The reduced system contains less PV generators with larger individual capacities than the original system.

An executable to run the feeder reduction code has been uploaded to [35]. Details of the operations and limitations are given there.

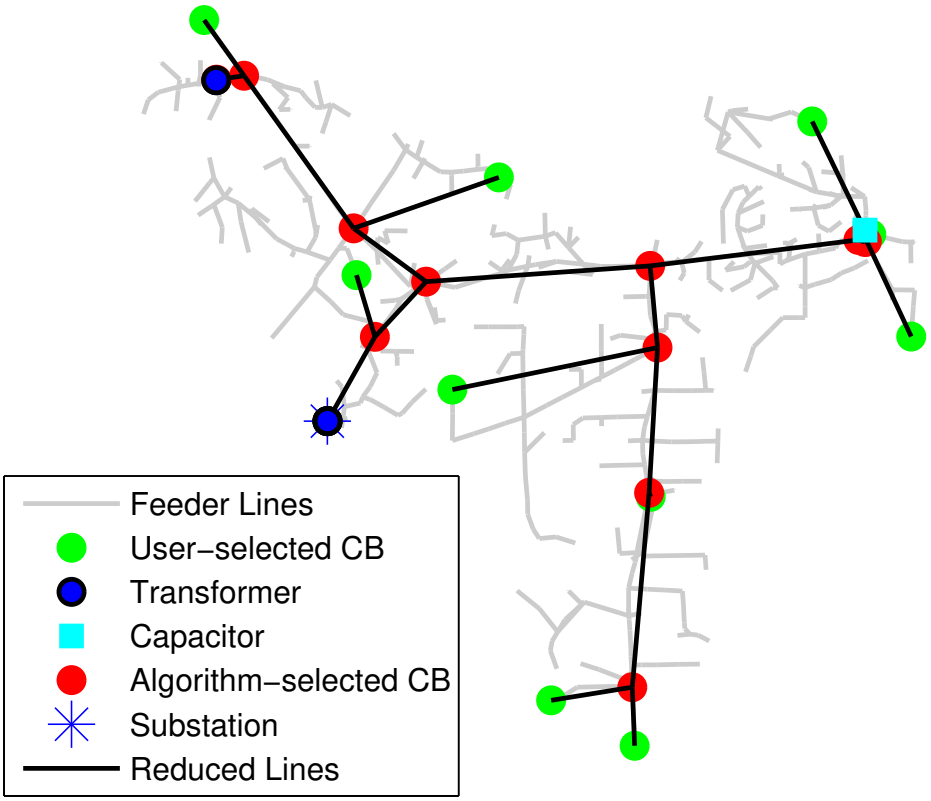


Figure 2.3: Reduced (black) California distribution feeder overlayed on the full distribution feeder (grey). Initially nine buses were user-selected as CB and the algorithm selected the additional buses.

2.4 Validation

2.4.1 Distribution Feeder

To evaluate the accuracy of the proposed circuit reduction algorithm, a stochastic sensitivity analysis was performed on a real medium voltage (MV) California distribution feeder with 621 multi-phase buses, two distribution transformers, one large capacitor bank (1350 KVAr), 364 distributed rooftop PV systems, and 471 loads. Each load operates under the same time-series shape scaled by its peak load, while each PV time-series is uniquely determined using a sky imager according to the method introduced in [6]. The feeder lines are modeled with zero shunt capacitance, and all neutral connections are assumed to be grounded perfectly. Feeder reduction simulations are run in OpenDSS [36] for one day with a time resolution of 30s.

A one-year QSTS with 1-minute resolution for each solar deployment is the standard simulation setting that DOE considers for solar planning studies to capture effects of PV fluctuations [9]. Therefore, one-year QSTS simulations with 30-sec resolution in this paper is commensurate with the minimum requirements set by DOE. Given that these standards will guide academia and industries in future solar planning for both research and implementation projects; the authors conclude that these settings are relevant to show the reduction of the computation expenses through the proposed algorithm.

2.4.2 Sensitivity Analysis

Error metrics

Given the importance of voltage in QSTS simulations, errors are defined as the difference in voltage of each CB from the identical node in the full feeder configuration: $E_j(t) = V_{\text{full}_j}(t) - V_{\text{reduced}_j}(t)$, where j indicates a node, and t indicates a time step. Mean ($\overline{E_j}, \overline{\overline{E}}$) absolute error metrics are used to elucidate the voltage difference as a function of the different circuit

configurations:

$$\overline{E}_j = \frac{1}{T}\Sigma_{t=1}^{T}|E_j(t)| \tag{2.13}$$

$$\overline{\overline{E}} = \frac{1}{J}\Sigma_{j=1}^{J}|\overline{E}_j| = \frac{1}{J}\frac{1}{T}\Sigma_{j=1}^{J}\Sigma_{t=1}^{T}|E_j(t)| \tag{2.14}$$

Simulation scenarios

The sensitivity to the following feeder conditions was analyzed: (i) Two days with the highest (01/18/2015) and lowest (12/26/2014) aggregate load; (ii) PV generation profiles from a mostly clear day (12/19/2014) and a day with overcast clouds in the morning and partly cloudy conditions in the afternoon (12/12/2014); (iii) PV penetrations of 50% and 100% where PV penetration is defined as the ratio between the installed rated PV capacity and the peak rated load on the feeder and is increased/decreased by scaling each PV system up or down by the same factor; (iv) Three different load types (constant-power, constant-impedance, and fixed-current magnitude) to observe the effect of deviating from the fixed current load used in which the algorithm. It is worth mentioning that the fixed-current magnitude load type used in OpenDSS differs from the assumption of fixed complex current which is used in the derivation.

The combination of these conditions results in $(2 \times 2) \times 2 \times 3 = 24$ feeder configurations.For each of these 24 baseline configurations, 1,000 reduction simulations are run. For each reduction simulation, the number of user-selected CB is randomly selected between 2 and 50. The CB locations are also randomly selected. Topology CB are then selected by the algorithm as described in section 3.5. The three buses with distribution transformers or capacitor banks are always CB.

Over all j and all configurations (24,000 simulations and on average 28 CB per simulation) the root-mean square deviation (RMSD) is 2.11×10^{-4} p.u., mean bias error (MBE) is 3.46×10^{-4} p.u., and the maximum observed error is 0.0113 p.u. (or 1.13%).

Sensitivity load type

Fig. 2.4 gives the histogram of errors for all simulations of each load type. Each load exhibits a strong peak around 0 error and errors greater than $\pm 1 \times 10^{-3}$ p.u. occurs for less than 0.5% of all nodes. Overall the difference in error imposed by using different load types is small. Contrary to the expected behavior, the largest peak at zero error occurs for the constant power load types, followed by constant current load types and then constant impedance load types. The increase in error for constant current load types is due to the fact that the derivation assumes the current is constant in both magnitude and angle, where the OpenDSS models fixed current magnitude only.

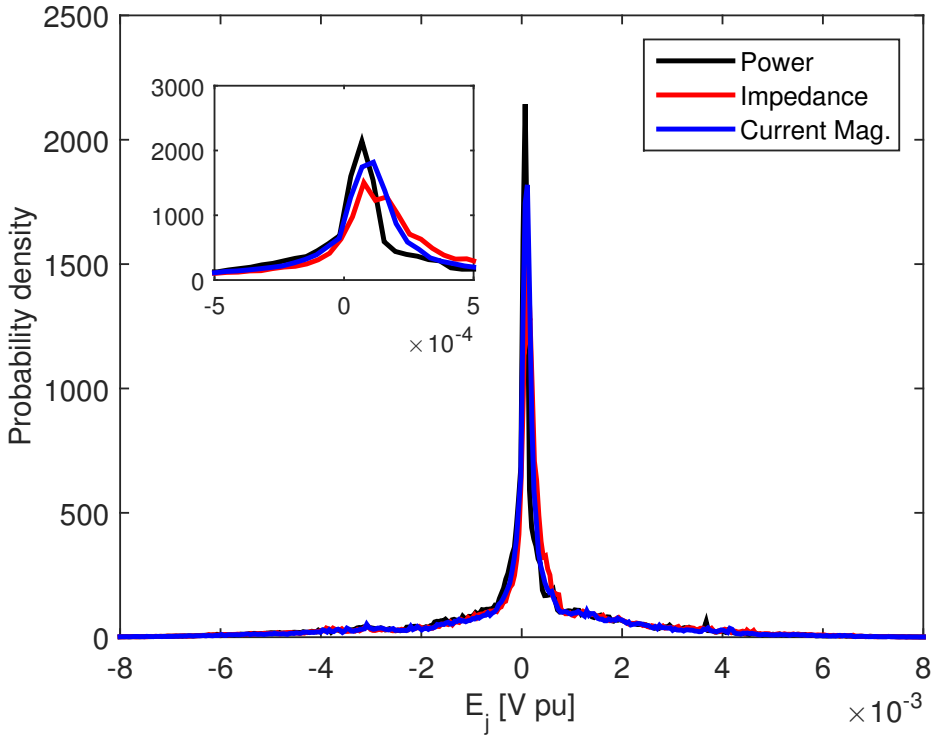


Figure 2.4: PDF of error for each load type. All nodes in each simulations corresponding to each load are represented in the function (i.e 8,000 simulations $\times$ $\approx$50 nodes). The inset plot provides a zoomed view of the histogram with x-axis limits of $\pm 5 \times 10^{-4}$

Sensitivity to loading

When comparing error as a function of the node net load (Fig. 2.5) we again see little change in error as a function of load type used. For all load types, the lowest error is seen for buses with near zero net load. As the net load deviates from zero, the error increase with some symmetry in both directions. The increase for large positive and negative net load is indicative of the constant current assumption used being a significant source of error, which is more noticeable for large amounts of generation/consumption.

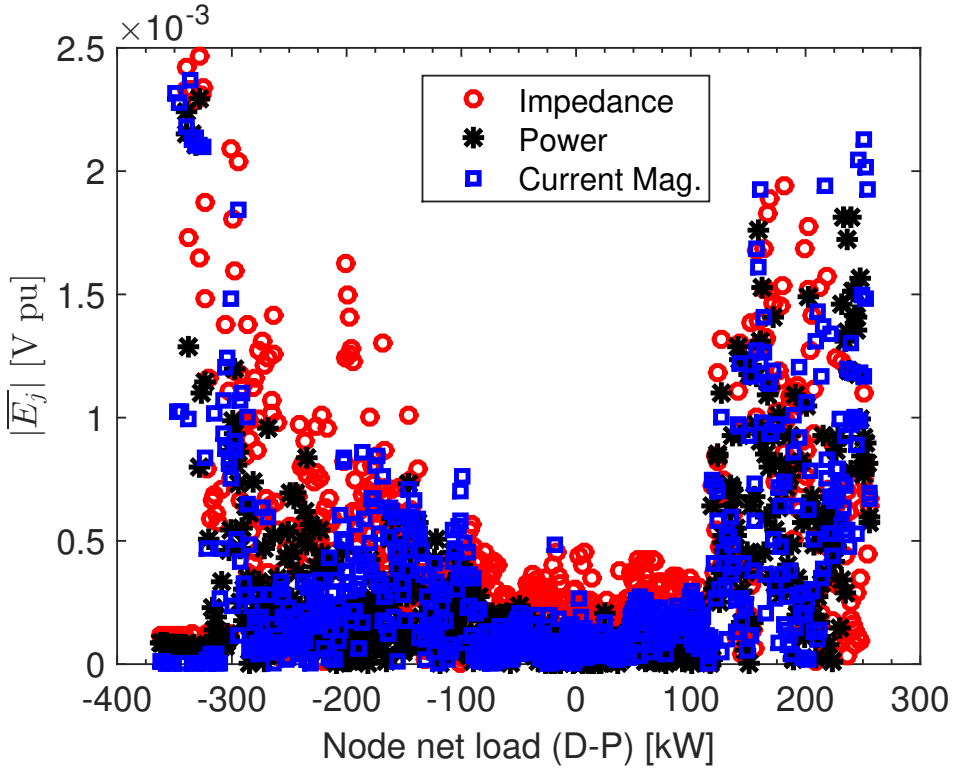


Figure 2.5: Mean error of node voltage plotted as a function of net load on the bus. The mean is taken by binning all net loads in 1 W bins and averaging all errors in the bin.

Sensitivity to distance

Finally, mean error as a function of distance from the substation (Fig. 2.6), supports the conclusion that the load type has little effect on the error. However, we do see a strong correlation

with increasing distance away from the substation. This behavior is consistent with intuition since the voltage at the substation is a set value dependent on the upstream conditions, whereas buses at the end of the feeder are subject to an accumulation of reduction error.

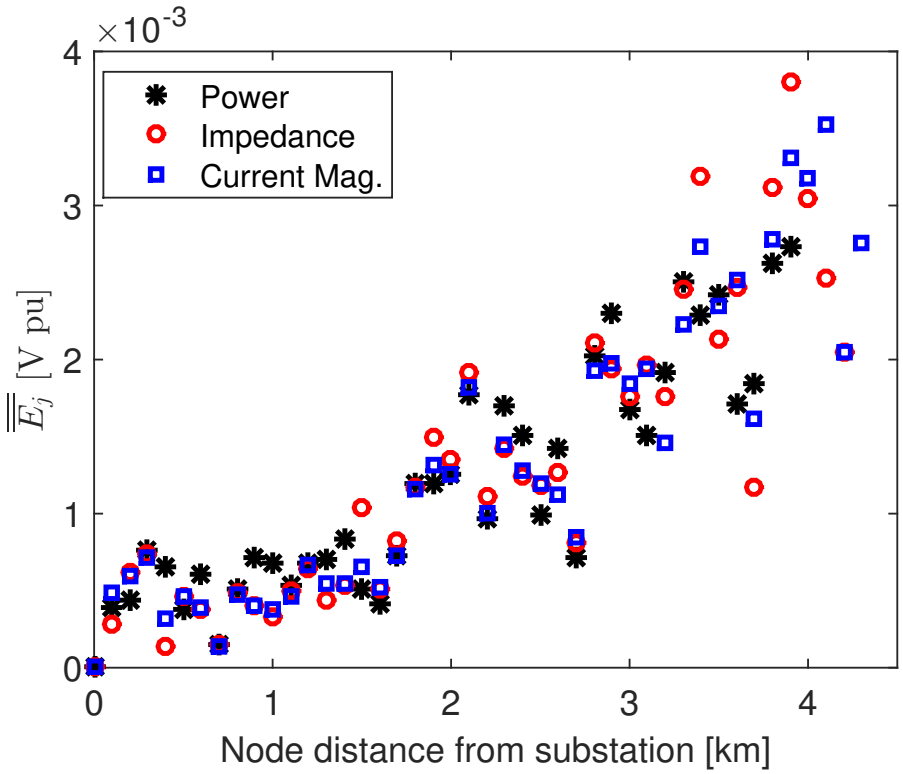


Figure 2.6: Mean error of node voltage plotted as a function of distance of the node from the substation. The mean is taken by binning all nodes into 100m bins and taking the average of all nodes in that bin across all simulation time steps.

Sensitivity to number of critical buses

1,000 additional simulations were performed by randomly selecting number and location of CBs with the number ranging from 1 to the full set of 621. Given the small sensitivity to the parameters considered in the previous section, the analysis is carried out with constant impedance loads (highest error) on 12/26/2014. Figure 2.7 shows that, as expected, the error in voltage decreases as less buses are removed from the circuit. Non-zero error is noticed for the case of zero buses removed (i.e. the circuit is re-written with no modification), as a result of the stopping

criteria of the solver.

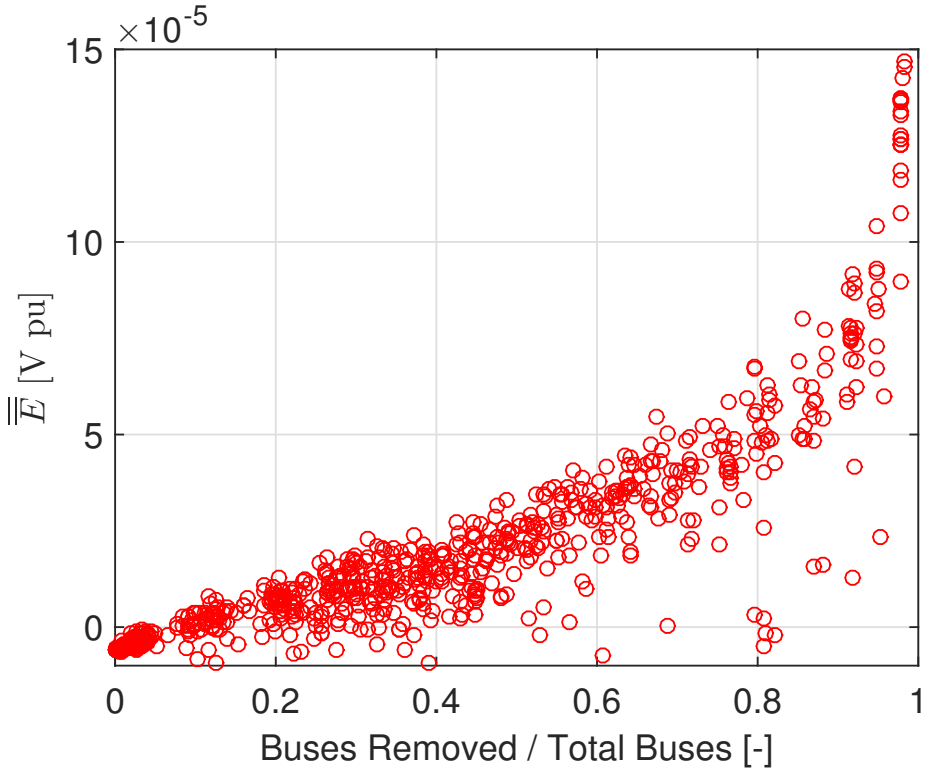


Figure 2.7: Average daily error plotted against the total number of buses removed in the simulation. Each point corresponds to error averaged across all time steps and all buses in each simulation, as defined by equation 2.14. 1,000 simulations were configured under HS50 with constant impedance loads.

2.4.3 Computational Expense

Since the ultimate objective of feeder reduction is increased computational speed, the computational cost associated with reducing and simulating different sized feeders was investigated. Simulations were run on a desktop with an Intel(R) Core(TM) i7-4770 processor and 32 GB RAM. Fig. 2.8 plots the computational time required to reduce the 621 bus feeder as well as the computational time to simulate a full day of QSTS at 30 s resolution for the resulting feeder. Both lines show an increase in time with an increase in the number of buses remaining in the system with slopes 0.18 and 0.021 seconds/bus for reduction and simulation, respectively.

Fig. 2.8 indicates that the time to reduce the feeder is about 9 times that of a short QSTS simulation run. However, the reduction time is a one-time cost which quickly pays back when long-term or parametric studies are conducted. For year long simulations at 30 s resolution (Table 3.1) simulation time decreases by 31% for only a 20% reduction of buses. Savings greater than 90% are observed for system that reduce 96% of buses. At 621 buses the present feeder was relatively small; larger relative computing time savings are expected for larger feeders. It is noted, t_red increases as fewer buses are reduced. The increase in time is a result of the structure of the algorithm which loops through each bus CB during each step of the reduction. More CB leads to more loops in topology detection, end bus reduction, critical bus reduction, as well as the conversion of the circuit back to a form which can be interpreted by a power flow solver. While the latter part is specific to the OpenDSS solver, it is expected to scale similarly for other solvers.

Table 2.1: Computational expense associated with reduction of the original feeder (t_{red}) and simulation of the reduced feeder (t_{sim}) as presented in Fig. 2.8. The yearly simulation time is extrapolated from the one-day simulation time for 30s time steps.

User selected buses	% red.	t_{red} (s)	$t_{\text{sim}}^{\text{day}}$ (s)	$t_{\text{sim}}^{\text{year}}$ (min)	$1-\frac{t_{\text{sim}}^{\text{year}_\text{i}}}{t_{\text{sim}}^{\text{year}_\text{1}}}$
621 (Full)	-	-	15.68	95.4	-
500	20%	86.0	10.5	65.0	31%
400	36%	66.2	10.3	63.6	33%
300	52%	53.6	9.5	58.4	39%
200	67%	37.4	7.5	46.0	52%
100	84%	13.7	5.6	34.2	64%
50	92%	10.9	3.4	20.7	78%
20	96%	6.8	1.9	9.4	90%
10	98%	4.6	1.2	7.6	92%
1	99.8%	3.1	0.6	3.7	96%

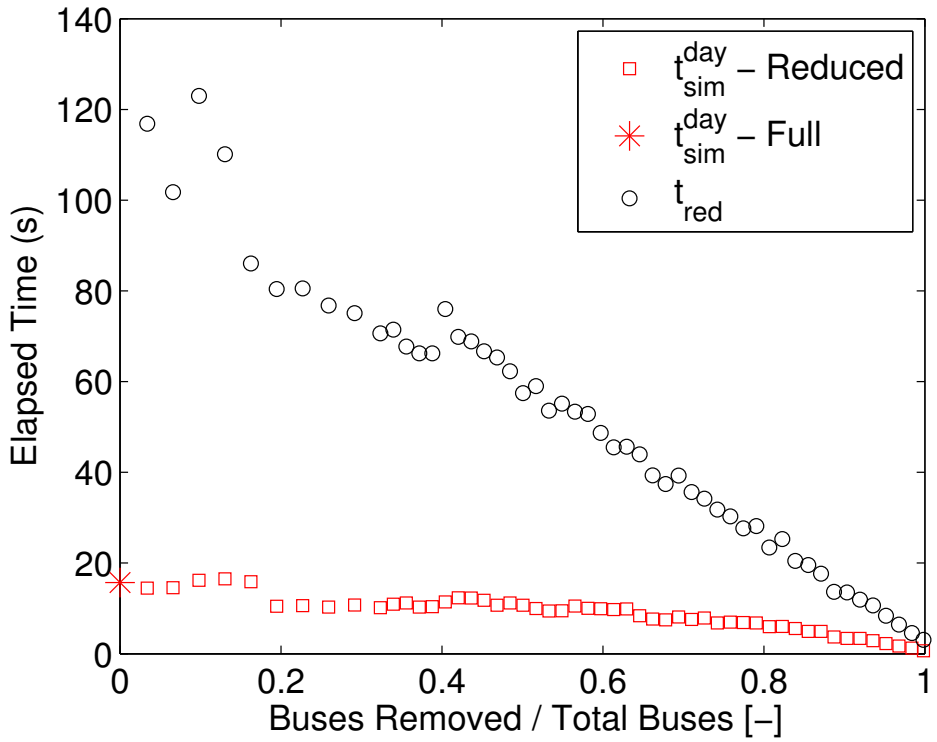


Figure 2.8: Computation time to reduce the 621 bus feeder to a subset of CB (black) and the QSTS time (red) associated with the reduced feeder for simulating one day at 30 s timesteps. A different simulation set was used to control for time delays due to communication with external storage devices.

2.5 Conclusion

A comprehensive method to reduce large realistic distribution feeders is proposed. The algorithm is sophisticated enough to handle complex configurations such as

1. multiphase connections through out the entire network
2. mutual coupling between multiphase unbalanced lines
3. unbalanced loads and generation
4. spatial variation in load and generation

through manipulation of the full impedance matrix. The method is also unique through the

retention of geographic variance in both PV generation and load consumption by a phase and impedance-weighted impact.

A sensitivity analysis was performed on a real California distribution feeder, which accounted for differences in solar generation, load consumption, penetration level, load type, and number of CB. The algorithm is shown to maintain the CB voltages with a maximum error of 1.13% and an rMSE of 0.21% in bus voltage. The largest contributor to error was found to be the distance of the bus from the substation due to aggregation errors. The error is weakly correlated with the load type used in the simulation.

The reduction provides significant time savings. For example, greater than 90% reduction in simulation time was found for feeders which reduced the number of buses by at least 96%, while reducing only 20% of the total buses resulted in a 31% time savings for simulating one year at 30s time steps.

The potential critical buses for a distribution feeder include, but are not limited to, the buses which 1) host sensitive loads such as hospitals, 2) host voltage regulation devices such as smart inverters or capacitors, 3) host power flow controllers such as battery management systems, or 4) show maximum and minimum voltage magnitudes.

Future improvements to the method will focus on reducing the time associated with reduction, automation of CB selection, and handling of advanced distribution modeling elements. Consideration of distribution line shunt capacitance, reduction of secondary transformers, imperfect neutral grounding, and alternative forms of generation are essential to real world application. Further, even though it has been shown here to have little effect, a reduction scheme which does not rely on the constant current assumption will be developed.

The text and data in Chapter 2, in full, is a reprint of the material as it appears in Multiphase Distribution Feeder Reduction, Pecenak, Z.K., Disfani, V.R., Reno, M., Kelissl, J., *IEEE Transactions on Power Systems*, 2017. The dissertation author is the primary investigator and author of this article.

Chapter 3

Inversion Reduction Method for Real and Complex Distribution Systems

3.1 Introduction

The introduction of distributed energy resources (DER) into distribution networks en masse has transformed the study of power systems. Utility scale planning studies must consider the uncertainty in these resources and devise mitigation techniques under a plethora of operating conditions [37].

As more DERs are employed to meet the renewable generation goals being set globally [38], the complexity of these studies will compound. For a current example, the proposal of the Western Energy Imbalance Market will require voltage and phase information of the entire western interconnection simultaneously [39]. As a result, solutions to reduce the time required to carry out such studies are becoming increasingly important [16, 40, 20, 41]. Network reduction provides a means for reducing the complexity and associated time of the systems being studied.

In reference [13] four of the more popular network reduction techniques are discussed and compared for performance in static power flow simulations: i) Ward reduction [12], ii) Kron

Reduction [11], iii) Dimo's Method [14], and iv) Zhukov's reduction [15]. For the two feeders investigated (IEEE 14 bus and IEEE 118 bus), all methods were shown to produce significant error in voltage due to reduction (> 0.01 pu), while the Ward reduction method produced the lowest error overall. However, the Ward reduction requires an initial solution to the power flow (which increases computational cost) and assumes fixed current loads. All of the methods are designed for transmission networks which tend to be balanced systems designed with symmetrical components.

Recently, a body of work specifically tailored to distribution feeder simplification has been introduced. The segmentation method introduced in reference [17] introduces the use of a constant power assumption to the literature on distribution network reduction. The methodology recursively replaces model segments between two buses of interest with characteristic equations representing a simpler topology. The methodology is tested on Feeder J1 [18] and produces a small max voltage error of ($O(10^{-3})$). However the authors make no mention of error with changing load conditions, and an initial power flow is still needed as a system input.

A distribution feeder reduction technique for balanced distribution systems is proposed in [16] which does not require an initial power flow solution. Load and PV is aggregated recursively between a subset of buses until the entire network is reduced. When implemented in OpenDSS [36], the method produced negligible voltage error for the distribution feeder investigated. However, the feeder is modeled with no imbalance in generation or loading, symmetric impedance between buses without mutual coupling, and negligible shunt capacitance, and only a single voltage level, which is unrealistic. Further no mention of reduction across voltage levels is mentioned, requiring transformer nodes to be kept in the reduced model, which increases computational cost.

In [1], the method proposed in [16] was enhanced to allow mutual coupling and imbalance in line impedance, and imbalance in loading. In addition, a weighting scheme preserved spatial and temporal variations in load and generation in the reduced feeder. Extensive validation on

a 3-phase 621 bus feeder with unbalance in load, generation, and line loading was performed. Errors were ($O(10^{-3})$) and the simulation time for a year long integration study was reduced by up to 96%.

Despite the improvements in applicability and accuracy in [1], it preserved a number of assumptions from previous methodologies: 1) While individual load models are preserved during the reduction process, the reduction methodology is formulated based on the assumption of fixed current loads which do not accurately represent common loads; 2) Shunt capacitance is ignored, which is a critical part of realistic distribution networks; 3) Reduction across voltage transformers is not possible, requiring the inclusion of extra buses in the reduced feeder; 4) The recursive nature of the algorithm causes the reduction times to scale with feeder size.

To overcome these limitations, a disparate and novel technique for reduction of multi-phase unbalanced distribution feeders is presented here. The reduction methodology is a Gauss elimination matrix inversion technique which is derived using a more common fixed power model assumption for loads and generators.

The inversion reduction methodology is the first to demonstrate that the use of Guassian elimination techniques for reduction of feeders automatically considers complexities of multiphase unbalanced systems. In fact the methodology is shown to be a generalization of [1], with additional terms which facilitate the aggregation of load and generation across voltage transformers and the inclusion of shunt impedance in lines and buses.

The contributions of this paper to the literature on distribution network reductions are as follows:

1. Development of a methodology which does not require power flow simulation or measured data

2. Improving on existing methods to account for complexities such as

    - shunt capacitance in distribution lines

- feeders with multiple voltage levels
- reduction based on power (not current)

3. Reduction through a single calculation as opposed to a recursive formulation, rendering the method easier to implement and reducing computational cost

4. Algorithm for transforming admittance matrix to circuit elements as required by commercial power flow solvers

The rest of the paper is organized as follows. Section 3.2 briefly introduces the methodology in [1] to facilitate the comparison of the methods. In Section 3.3, we derive the new inversion reduction methodology. Section 3.4 demonstrates the inversion reduction on a simple 3 bus system and compares the proposed methodology with the method from [1]. The algorithm to implement is given in Section 3.5. Section 3.6 discusses the error sources associated with the method and its assumptions. Section **??** concludes the paper.

3.2 Review of Reference [1]

3.2.1 Introduction

The approach in [1] was a recursive method, which for a set of desired or critical buses (CB), looped through all the non-critical buses (NCB) and eliminated them by moving current injections to neighboring buses. For any set of neighboring buses i, j, k, where j is between buses i and k, we can write the p-phase voltage vector for buses j and k as follows:

$$V_j = V_i + Z_{ij}(I_j + I_k) \tag{3.1}$$

$$V_k = V_j + Z_{jk}I_k, \tag{3.2}$$

where $V \in \mathbb{C}^{p\times 1}$ and $I \in \mathbb{C}^{p\times 1}$ are the vectors of voltages and current injections of the p-phase bus, and $Z \in \mathbb{C}^{p\times p}$ is the full impedance matrix of the line connecting the buses, where the diagonal elements denote self impedances and off-diagonal elements denote mutual impedances between different phases of the line.

3.2.2 End Bus Removal

An "end-bus" reduction of k onto j can be performed if there are no CB downstream of k. From equation (3.1), the voltage at bus j does not depend on V_k or Z_{jk}. Thus bus k and the line connecting j to k can be removed from the circuit, while I_k is moved onto bus j.

$$I_j^{\text{new}} = I_j + I_k \tag{3.3}$$

Note equation (3.1) is only a function of $Z_{i,j}$, not Z_{jk}, indicating that the impedance between buses j and k is simply removed from the reduced circuit.

3.2.3 Middle Bus Removal

Removing the middle bus j from the circuit (dubbed "middle-bus" reduction) requires re-arranging equations 3.2 and 3.1 as follows:

$$V_k = V_i - Z_{i,j} \times (I_j + I_k) - Z_{j,k} \times I_k \tag{3.4}$$

$$V_k = V_i - (Z_{i,j} + Z_{j,k}) \times (I_k + (Z_{i,j} + Z_{j,k})^{-1} \times Z_{i,j} \times I_j) \tag{3.5}$$

We can restate equation (3.5) the form given in equation (3.6)

$$V_k = V_i - Z_{\text{eq}} \times I_k^{\text{new}} \tag{3.6}$$

where,

$$Z_{eq} = Z_{i,j} + Z_{j,k} \tag{3.7}$$

$$I_k^{\text{new}} = I_k + (Z_{\text{eq}})^{-1} \times Z_{i,j} \times I_j \tag{3.8}$$

As indicated in (3.6) to remove bus j, bus i is connected to bus k through an equivalent line with impedance equal to the summation of the two original lines. Further, a contribution of I_j is transferred to bus k according to the ratio of impedance between j and k to the equivalent impedance ($Z_{eq}^{-1} \times Z_{ij}$).

A similar relationship holds for the updated current on bus i, where $I_i^{\text{new}} = I_i + (Z_{\text{eq}})^{-1} \times Z_{j,k} \times I_j$.

3.2.4 Spatial and Temporal Variation in Load / Generation

The resulting reduced feeder is composed of loads and generation on the CBs, which are based on the aggregated current injections from the removed buses. However, the load and generation on the reduced feeder is only valid for the snapshot of loading conditions used during the reduction process. To remove the need for reduction after every change in load and generation, a weight matrix $W \in \mathbb{C}^{M \times M}$, where M is the set of nodes in the original feeder, is introduced. Initially, $W_{ii} = 1$, while $W_{ij} = 0$, indicating that all loads are on their own node. As reduction progresses, W is updated by removing rows corresponding to nodes which are removed from the circuit and adding the values to the node that the load is being aggregated to. Any non-zero W_{ij} in the final $W \in \mathbb{C}^{m \times M}$ indicates the ratio of current injection on node i which now resides on node j. Here m is the set of nodes in the reduced feeder.

3.3 Inversion Method Derivation

3.3.1 Circuit reduction

Here, a new approach to reducing a distribution feeder is proposed, which is formulated as a Gauss elimination inversion technique and is carried out in a single calculation, as opposed to looping through all CB in the circuit. A constant power load model is assumed, which is more representative of industrial and residential loads than the more common fixed current assumption, which is most applicable to special lighting load. The load model assumption is solely used for derivation purposes, while individual load models are retained in the reduction.

The inversion reduction methodology is applicable to both radial and meshed feeders. The choice of reduced feeder network and the topology detection algorithms differ for meshed or radial system. This paper presents the reduction algorithms for radial feeders. The application to meshed feeders will be a topic of future work.

For the original or full feeder (subscript "o"), the vector of complex voltages of each node is given as $V_o \in \mathbb{C}^{M\times 1}$ and the vector of complex current injections at each node is $I_o \in \mathbb{C}^{M\times 1}$. The two variables are related through Ohm's law by the system admittance matrix $Z_o \in \mathbb{C}^{M\times M}$

$$V_o = Z_o \times I_o. \tag{3.9}$$

Briefly, it should be noted that the relations given in (3.9) represents just the system admittance and power injection. Traditionally, this relation uses a swing bus where the first element of I_o is a variable. In our formulation, the swing bus is not needed and if no load is present on the first node, that entry is zero. Similarly, we define a reduced feeder (subscript "r") with complex voltage vector of all m nodes of the reduced feeder $V_r \in \mathbb{C}^{m\times 1}$, complex current injection vector $I_r \in \mathbb{C}^{m\times 1}$, and impedance matrix $Z_r \in \mathbb{C}^{m\times m}$. Akin to (3.9) we observe $V_r = Z_r \times I_r$.

Requiring voltage equivalence before and after reduction at all buses in the reduced feeder

(i.e. the CB of the full feeder) yields

$$V_{o,\mathrm{CB}} = V_r, \tag{3.10}$$

where $V_{o,\mathrm{CB}}$ is the subset of voltages in the full feeder corresponding to the CB. $V_{o,\mathrm{CB}}$ is the product of the impedance matrix with NCB rows removed $Z_{o,CB} \in \mathbb{C}^{m\times M}$ and the current injection vector I_o. Inserting (3.9) into (3.10) we obtain

$$Z_{o,\mathrm{CB}} \times I_o = Z_r \times I_r. \tag{3.11}$$

To remove the dependence on current, we introduce the vectors of complex power for each node, $S_o \in \mathbb{C}^{M\times 1}$ and $S_r \in \mathbb{C}^{m\times 1}$ in the full and reduced feeders, respectively.

$$S_o = \tilde{V_o} \otimes I_o^* \tag{3.12}$$

$$S_r = \tilde{V_r} \otimes I_r^*, \tag{3.13}$$

where the superscript $*$ represents the conjugate operation and $\otimes$ is element-wise multiplication. $\tilde{V_o}$ and $\tilde{V_r}$ are complex vectors representing base complex voltage for the original and reduced feeders, where voltage magnitudes and angles are defined based on the nominal transformer ratios and phase shifts due to the type of transformers.

Note that the base voltage vectors could be replaced with actual voltage values, which would result in a more accurate reduction. However, this would require solving an initial power flow solution and changing loading conditions would still result in errors.

Solving for current

$$I_o = (\tilde{V_o}^{\mathrm{inv}} \otimes S_o)^* \tag{3.14}$$

$$I_r = (\tilde{V_r}^{\mathrm{inv}} \otimes S_r)^* \tag{3.15}$$

where $\tilde{V_o}^{\text{inv}}$ and $\tilde{V_r}^{\text{inv}}$ denote the element-wise inversion of the vectors $\tilde{V_o}$ and $\tilde{V_r}$ respectively. Substituting (3.14), (3.15) into (3.11) and solving for the vector of powers in the reduced system

$$S_r = \tilde{V_r} \otimes [(Z_r^{-1} \times Z_{o,CB})^* \times (\tilde{V_o}^{inv} \otimes S_o)]. \tag{3.16}$$

As for an arbitrary matrix A and two arbitrary vectors B and C, one can prove that $A \times (B \otimes C) = A \times diag(B) \times C$ and $B \otimes (A \times C) = diag(B) \times A \times C$, we rewrite (3.17) as

$$S_r = diag(\tilde{V_r}) \times (Z_r^{-1} \times Z_{o,\text{CB}})^* \times diag(\tilde{V_o}^{\text{inv}}) \times S_o, \tag{3.17}$$

indicating that for a chosen Z_r we can define a new set of equivalent loads and generation powers. Although the choice of Z_r is not unique, a logical choice is to simply remove the matrix rows and columns corresponding to the nodes that were removed from the system. That is, the admittance matrix for the reduced feeder $Y_r = Z_r^{-1}$ is composed of equivalent impedances between the remaining buses. This is discussed in detail in section 3.5.

3.3.2 Spatial and Temporal Variation in Load/Generation

Similar to [1], a weighting matrix $W = S_r/S_o$ is adopted to aggregate original powers onto CB. From equation (3.17), $W \in \mathbb{C}^{m \times M}$ is

$$W = diag(\tilde{V_r}) \times (Z_r^{-1} \times Z_{o,CB})^* \times diag(\tilde{V_o}^{inv}) \tag{3.18}$$

Note that removing the nominal voltage matrices from W (i.e. assuming $\tilde{V_r} = \tilde{V_o}$), yields $W_o = (Z_r^{-1} \times Z_{o,CB})^*$ which produces the same weighting matrix as in reference [1]. The addition of the nominal voltage matrices allows for the mapping of load and generation profiles across different voltage levels (i.e. across transformers).

3.3.3 Load / Generation Model Mapping

Generators and loads can be modeled in a variety of different ways. For example, OpenDSS has 7 options to model feeder loads and 7 options to model generators in addition to a model for PV. To retain these models through the reduction process, S_o can be defined as a matrix, where each column indicates a different load type (i.e. $S_o \in \mathbb{C}^{M \times X}$ where X is the number of load types on the feeder).

3.4 Example reduction of 3 bus system

3.4.1 Two lines

To illustrate a feeder reduction, a sample feeder is shown in Fig. 3.1. First, a single phase, three bus system connected by two lines is chosen to provide direct comparison to the methodology formulated in [1] and to provide intuition about the relationship between the original and reduced circuit. However, the methodology is applicable to any M bus, p-phase phase system. We define the system as follows:

$$\tilde{V_o} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, S_o = \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} \tag{3.19}$$

$$Z_o = \begin{bmatrix} \frac{1}{z_{11}} + \frac{1}{z_{12}} & -\frac{1}{z_{12}} & 0 \\ -\frac{1}{z_{12}} & \frac{1}{z_{12}} + \frac{1}{z_{22}} + \frac{1}{z_{23}} & -\frac{1}{z_{23}} \\ 0 & -\frac{1}{z_{23}} & \frac{1}{z_{23}} + \frac{1}{z_{33}} \end{bmatrix}^{-1} \tag{3.20}$$

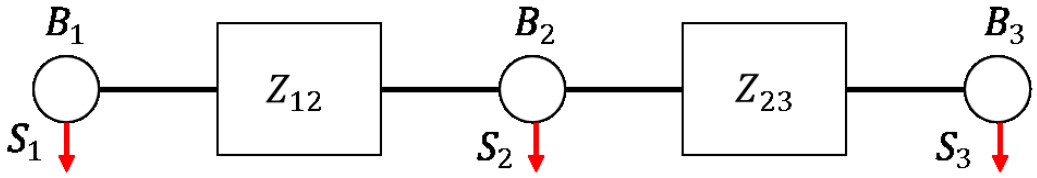


Figure 3.1: Line model depicting a single phase 3 bus system connected by two lines. Each bus B injects power S_B. The impedance between a bus and its neighbor is denoted as Z_{ij}, while shunt impedance is noted as Z_{ii}.

End bus reduction through removal of bus 3

To remove bus B_3, the rows and columns corresponding to B_3 in the admittance matrix can be removed to generate Z_r. Likewise, $\tilde{V}_r$ is equivalent to $\tilde{V}_o$ with the omission of the row and column corresponding to V_3. Solving (3.17) yields the power vector for loads and generators in the reduced feeder.

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_2^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 + S_3 \frac{1}{1+\frac{z_{23}}{z_{33}}} \frac{V_2}{V_3} \end{bmatrix} \tag{3.21}$$

The equation indicates that the power on B_1 remains the same ($S_1^{\text{new}} = S_1$). However, at B_2 a scaled power of B_3 with respect to both voltage and impedance is added. The scaling with respect to voltage accounts for change in phase and voltage magnitude, allowing loads to be aggregated across transformers, which can then be removed from system. The scaling due to impedance accounts for the shunt impedance on the bus, which was neglected in [12], and is a result of the full impedance matrix being used to calculate the updated loads.

For the special case of no shunt impedance ($z_{33} = \infty$) and no voltage change between B_2

and B_3, we recover

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_2^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 + S_3. \end{bmatrix} \tag{3.22}$$

Assuming $S_i = V_i I_i^*$, we in fact recover the form given in (3.3), indicating that the new methodology is a generalization of the methodologies proposed in [1, 16], but accounts for shunt impedance and changes in voltage phase and angle between nodes.

The impedance between B_1 and B_2 remains unchanged, while the impedance between B_2 and B_3 is removed from the circuit.

Middle bus reduction through removal of Bus 2

If it is desired to remove B_2 from the circuit and only keep B_1 and B_3, we formulate the new impedance matrix by removing the rows and columns of Z_o corresponding to B_2. Solving (3.17) with the given values for the updated power vector yields

$$S_r = \begin{bmatrix} S_1^{new} \\ S_3^{new} \end{bmatrix} = \begin{bmatrix} S_1 + S_2 \times \frac{z_{23}}{z_{12}+z_{23}+\frac{z_{12}\times z_{13}}{z_{22}}} \frac{V_1}{V_2} \\ S_3 + S_2 \times \frac{z_{12}}{z_{12}+z_{23}+\frac{z_{12}\times z_{13}}{z_{22}}} \frac{V_3}{V_2} \end{bmatrix}. \tag{3.23}$$

By removing the middle bus, the power of the loads on both remaining buses are modified due to the aggregation of the power from the removed bus. As observed in end bus reduction, the aggregated power is a function of both the shunt impedance of the removed bus, and the voltage ratio between the buses.

Here the impedance between B_1 and B_3 takes the form of an equivalent impedance

$$Z_{13_{eq}} = (z_{12} + \frac{z_{12} \times z_{23}}{z_{22}} + z_{23}). \tag{3.24}$$

For the special case when there is no shunt impedance ($z_{22} = \infty$) and the voltage level is the same, we recover

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_3^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 + S_2 \times \frac{z_{23}}{z_{12}+z_{23}} \\ S_3 + S_2 \times \frac{z_{12}}{z_{12}+z_{23}} \end{bmatrix} \tag{3.25}$$

and

$$Z_{13_{\text{eq}}} = (z_{12} + z_{23}) \tag{3.26}$$

Assuming $S_i = V_i I_i^*$, we recover the exact form of (3.7) and (3.8).

3.4.2 Line and transformer

To illustrate the ability to reduce across simple transformers, a two-winding transformer is introduced connecting B_2 and B_3 (Fig. 3.2).

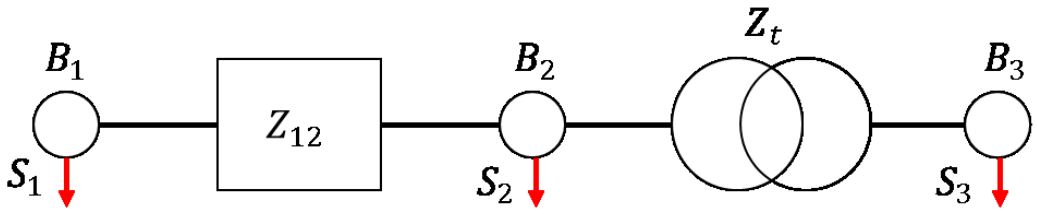


Figure 3.2: Line model depicting a single phase 3 bus system connected by one line and one two-winding transformer with impedance Z_t.

The admittance matrix for the system with a transformer with voltage ratio $n = V_2/V_3$ is

$$Z_o = \begin{bmatrix} \frac{1}{z_{11}} + \frac{1}{z_{12}} & -\frac{1}{z_{12}} & 0 \\ -\frac{1}{z_{12}} & \frac{1}{z_{12}} + \frac{1}{z_{22}} + \frac{1}{z_t} & -\frac{n}{z_t} \\ 0 & -\frac{n}{z_t} & \frac{n^2}{z_t} + \frac{1}{z_{33}} \end{bmatrix}^{-1}. \tag{3.27}$$

Removing the end bus removes the transformer from the circuit. The new power is

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_2^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 + S_3 \frac{1}{1+\frac{z_t}{z_{33}}} \frac{1}{n} \frac{V_2}{V_3} \end{bmatrix}. \tag{3.28}$$

Removing the middle bus requires the line between B_1 and B_2 to be replaced with an equivalent transformer. The new powers are

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_3^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 + S_2 \frac{z_{22} z_t}{z_{12} z_{22} + z_{12} z_t + z_{22} z_t} \frac{V_1}{V_2} \\ S_3 + S_2 \frac{n z_{12} z_{22}}{z_{12} z_{22} + z_{12} z_t + z_{22} z_t} \frac{V_3}{V_2} \end{bmatrix}. \tag{3.29}$$

The reduced admittance matrix becomes

$$Y_r = \begin{bmatrix} z_{11_{eq}} + z_{t_{\text{eq}}} & -n z_{t_{\text{eq}}} \\ -n z_{t_{\text{eq}}} & z_{22_{\text{eq}}} + n^2 z_{t_{\text{eq}}} \end{bmatrix}, \tag{3.30}$$

where the subscript "eq" indicates an equivalent impedance composed of the original impedances.

For this 3-bus system, the impedances are represented parametrically as:

$$Z_{11_{eq}} = \frac{z_{12}z_{22} + z_{11}z_t + z_{12}z_t + z_{22}z_t}{z_{11}(z_{12}z_{22} + z_{12}z_t + z_{22} * z_t)} \tag{3.31}$$

$$Z_{t_{\text{eq}}} = \frac{z_{22}}{z_{12}z_{22} + z_{12}z_t + z_{22}z_t} \tag{3.32}$$

$$Z_{22_{\text{eq}}} = \frac{n^2 z_{12}z_{33} + z_{12}z_{z22} + z_{12}z_t + z_{22}z_t}{z_{33}(z_{12}z_{22} + z_{12}z_t + z_{22} * z_t)} \tag{3.33}$$

The reduction logic is the same for more complex transformers (i.e. multiple winding, Δ-Y connections, split phase, etc...), however the form of $z_{t_{\text{eq}}}$ will differ.

3.5 Algorithm

3.5.1 Populate admittance, voltage, and power matrices

A circuit configuration is converted into an equivalent configuration for the reduced circuit as shown in Fig. 3.3. The feeder topology and CBs are determined as in [1].

An input file with feeder specifications is parsed and a circuit object is created that organizes the input data into the admittance matrix ($Y_o \in \mathbb{C}^{M\times M}$), the complex base voltage vector ($\tilde{V_o} \in \mathbb{C}^{M\times 1}$), the load power ($S_{o_{\text{load}}} \in \mathbb{C}^{M\times X}$), and the generation power ($S_{o_{\text{gen}}} \in \mathbb{C}^{M\times X}$) matrices.

As described in Section 3.3 the matrix form of the powers are used to map different load model types. For a given load or generator on a bus i with of model x, an entry in the power matrix for that element is given in S_o at row i, column x.

3.5.2 Reduce

First, the network is reduced by translating the nodal admittance matrix of the original feeder ($Y_o \in \mathbb{C}^{M\times M}$) to an equivalent admittance matrix ($Y_r \in \mathbb{C}^{m\times m}$) that describes the reduced circuit. This reduction is accomplished by calculating the impedance matrix for the full feeder

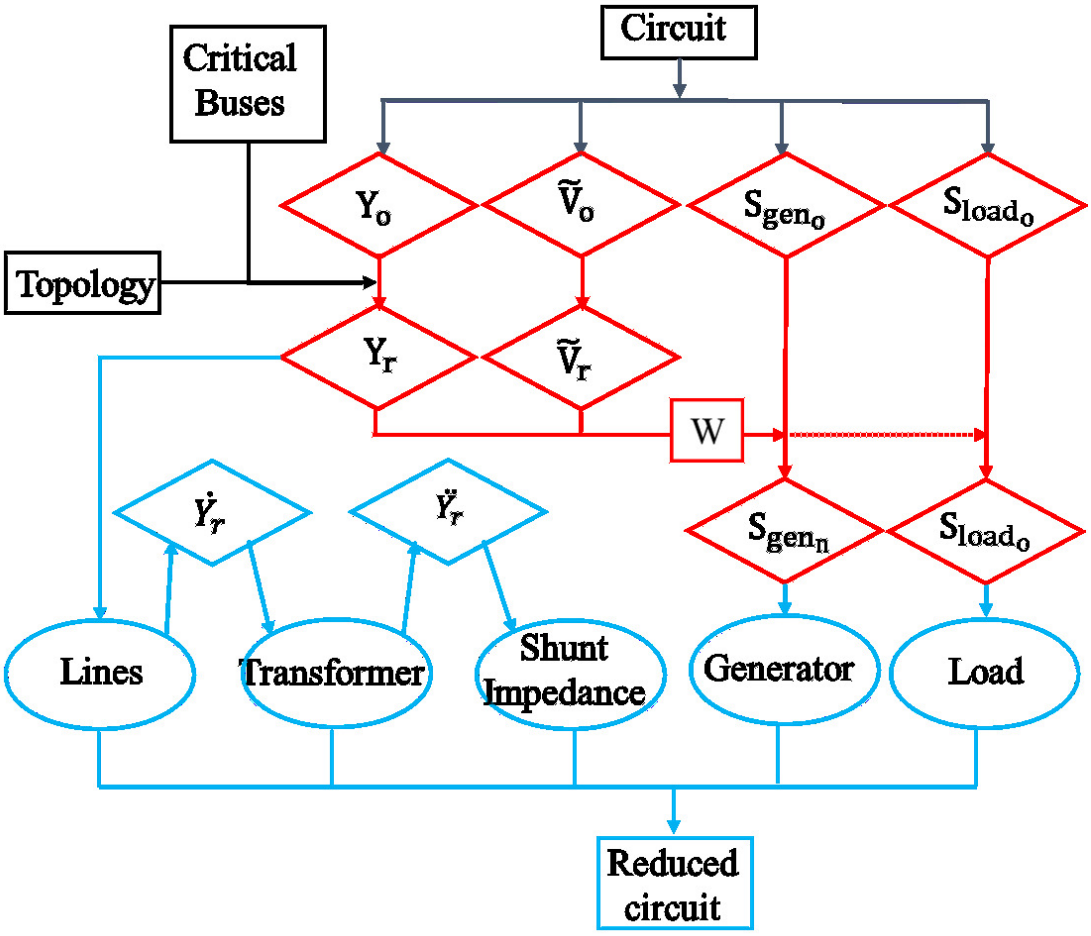


Figure 3.3: Flowchart of the reduction algorithm. Colors show: (black) breakdown of the original model into its elementary parts; (red) Reduction of parts to equivalents; and (blue) building the reduced model from elementary parts.

($Z_o = Y_o^{-1} \in \mathbb{C}^{M\times M}$) and removing all rows and columns not corresponding to CB to create the impedance matrix of the reduced feeder ($Z_r \in \mathbb{C}^{m\times m}$). The reduced admittance matrix is then realized through inversion of the impedance matrix ($Y_r = Z_n^{-1} \in \mathbb{C}^{m\times m}$). The nominal voltages at the CB are equal to the voltages at the corresponding buses in the original feeder ($\tilde{V}_r = \tilde{V}_{o,\text{CB}}$). All other voltage entries are removed.

Second, incorporating the reduced network, the full network, and the voltage vectors, the weighting matrix W is found using (3.18). A matrix $S_n \in \mathbb{C}^{m\times X}$ representing the load (or generation) powers on each node is found by multiplying W with the original power matrix $S_o \in \mathbb{C}^{M\times X}$ (equation (3.17)).

3.5.3 Rebuild

In general, the power flow equations could be solved directly using the reduced admittance matrix and power vectors, and the rebuild step introduced below would be redundant. However, power flow solvers require specific input formats for the circuit. Thus translating the reduced matrices into a form that is representative of the new network, namely i) loads, ii) generators, iii) distribution lines, iv) transformers, and v) shunt impedance (including capacitors and reactors) improves the integration of the methodology with existing software.

Loads and generator power matrices, S, are in order of the nodes, thus a load or generation object follows directly from the reduced power matrix. Rewriting the reduced network, on the other hand, is more challenging, as it requires analyzing the new feeder topology and nodal admittance matrix Y_r. The admittance matrix is sparse and convoluted. For a bus i connected to a bus j, the terms Y_{ij} can represent the admittance between the two buses contributed from a distribution line or a transformer (or both) for different phases. The terms Y_{ii} represent both the shunt connected admittances as well as the impact of the connection between bus i and bus j; see (3.20) and (3.27). We follow the procedure below:

Distribution Lines

For a bus i, all connected downstream buses are identified. For the p-phase connection between bus i with nodes I and downstream bus j with nodes J, the impedance, $z \in \mathbb{C}^{p\times p}$, between the buses is given by $z_{IJ} = Y_{IJ}^{-1}$. The corresponding resistance and reactance of the lines are then expressed as the real and imaginary parts of the matrix, respectively. The length of the line is calculated by the difference between the distances of bus i and j from the substation, as identified in the initial topology detection. The full network is developed by repeating the process above for each downstream bus and for each bus i. This process is summarized in **Algorithm 4**.

Algorithm 4 Retrieve lines from Y_r

```
Given Y_r
for bus i ∈ CB do
    Identify node set I that corresponds to bus i
    Identify any bus connected downstream to bus i to form the neighbor set N_i.
    for any bus j in N_i do
        Identify node set J that correspond to bus j
        if V_I=V_J then
            Find line impedance: z_line = Y_IJ^-1
            Find line length: L_ij = L_1i − L_1j
            Write line between bus i and bus j
        end if
    end for
end for
Calculate Y_L, admittance matrix of only line network
Subtract lines from Y_r: Ẏ_r = Y_r − Y_L
```

Transformers

In the new feeder, a transformer is needed to connect CB at different voltage levels, generally replicating transformers in the original circuit. For when both buses adjacent to a transformer are removed, the transformer is removed from the circuit, akin to the distribution lines. However, reduction then results in adjacent CB with different voltage bases (i.e. a CB

on the primary side adjacent to one on the secondary side of the feeder). A new transformer composed of the aggregate impedance between the two buses must be created.

To isolate just the transformer, distribution lines are removed from Y_r, resulting in a new matrix $\dot{Y}_r$. The impedance of the transformer found in $\dot{Y}_r$ depends on both the number of windings w, the phases p, and the connection type (i.e $\Delta-\Delta$, $\Delta-Y$, etc..). In general, however, a transformer connected between a bus i and j is comprised of the entries of $[Y_{ii}, Y_{ij}, Y_{ji}, Y_{jj}] \in \mathbb{C}^{p\times p}$. A connection detection algorithm is employed to determine the connection type of the transformer. The reconstruction of transformers is summarized in **Algorithm 5**.

Shunt Impedance

In the admittance matrix, the term $Y_{ii} \in \mathbb{C}^{p\times p}$ of a bus i is composed of the shunt impedance on the bus as well as the contribution of connected buses

$$Y_{ii} = 1/z_{ii} + \Sigma_{j=1}^{J} 1/z_{ij}, \tag{3.34}$$

where J is the number of buses connected to bus i. The connection admittance between each bus i and j (i.e. $Y_{ij} \in \mathbb{C}^{p\times p}$) is represented by,

$$Y_{ij} = -1/z_{ij} \tag{3.35}$$

Thus, the shunt impedance on bus i (z_{ii}) can be calculated as,

$$z_{ii} = \frac{1}{Y_{ii} + \Sigma_{j=1}^{J} Y_{ij}} \tag{3.36}$$

which is effectively accomplished through admittance matrix subtraction ($\ddot{Y}_r$), leaving just the shunt terms. See **algorithm 6**.

Algorithm 5 Retrieve Transformers from Y_r

Given $\dot{Y}_r$
for bus $i \in$ CB **do**
  Identify node set I that corresponds to bus i
  Identify any bus connected downstream to bus i in the neighbor set N_i.
  for any bus j in N_i **do**
    Identify node set J that correspond to bus j
    if $V_I \neq V_J$ **then**
      Find $z_{\text{t}} = \begin{bmatrix} Y_{II}^{-1} & -Y_{IJ}^{-1} \\ -Y_{JI}^{-1} & Y_{JJ}^{-1} \end{bmatrix}$
      Identify connection type (i.e. $\Delta - \Delta$, etc...)
      Transform z_{t} to winding impedance (see [42])
      Write transformer between i and j
    end if
  end for
end for
Calculate Y_{Tr}, admittance matrix of only transformer network:
Subtract transformers from $\dot{Y}_r$: $\ddot{Y}_r = \dot{Y}_r - Y_{Tr}$

Algorithm 6 Retrieve shunt impedance from $\ddot{Y}_r$

Given $\ddot{Y}_r$
for bus $i \in$ CB **do**
  Identify node set I that correspond to bus i
  Find shunt impedance: $z_{\text{shunt}} = Y_{II}^{-1}$
  Write shunt component
end for

3.6 validation

3.6.1 Strategy

The error due to reduction was detailed extensively for a single feeder in [1], where the error was most correlated with bus distance from substation, the number of buses removed, and net load on the bus. The new methodology shows the same trends for most feeders.

However, given the flexibility of the methodology proposed in this paper, the dependence of the error on feeder size, topology, and modeling complexity can also be assessed.

First, we validate the method by comparing results on the feeder examined in [1], referred to here as "UCSD A". Next, we examine the voltage error and savings in computing time on six disparate and publicly available feeder models: EPRI 5 and 7* [43], EPRI K1, J1, M1 [44], and IEEE 8500 [45]. The feeder models are summarized in Table 3.1. The EPRI 7* model has load aggregated at the feederhead as allocation factors were not considered in our algorithm. The model is useful as it shows that error for a feeder with a low number of loads to be moved and aggregated is dominated by translation of the model back to the powerflow solver.

Here, all results are shown for a snapshot simulation (not a time series) using the full capacity of load (greatest net load). Based on the results of [1], we expect the error to be less for most actual time-series scenarios.

As in [1], OpenDSS [36] is used to solve the power flow for both the original and reduced circuit. The error from reduction is defined as the difference in nodal voltage for the node in the power flow of the original circuit and in the reduced circuit.

3.6.2 Comparison to reduction in [1] on feeder UCSD A

Comparing to the reduction maximum voltage error from reference [1] of $O(10^{-3})$, the inversion reduction has $O(10^{-5})$ error, which is negligible for practical applications (Fig. 3.5). As the UCSD A feeder does not include the secondary side (no transformers), the reduction in

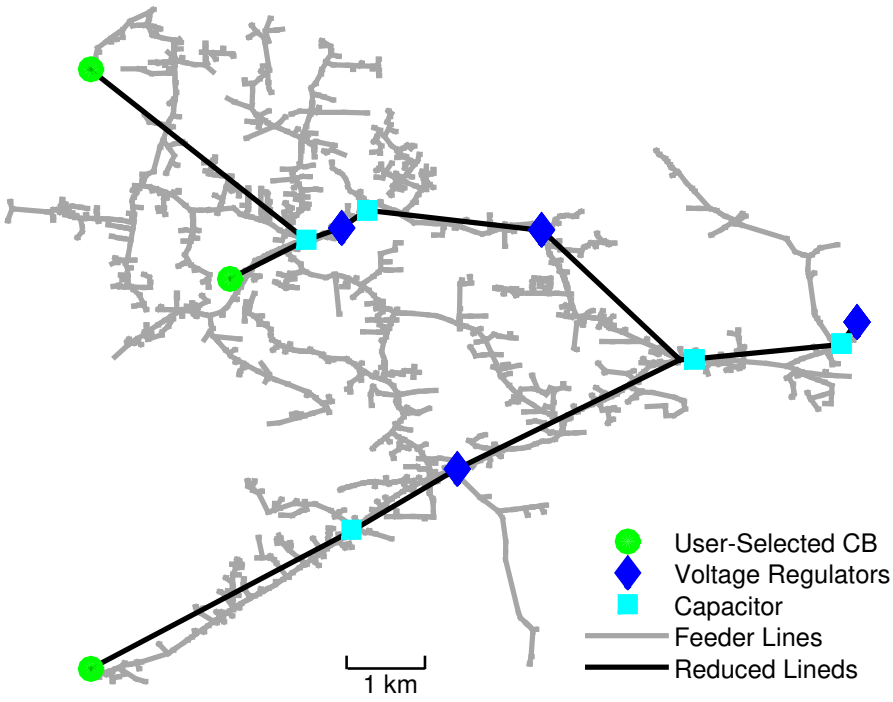


Figure 3.4: IEEE 8500 test feeder (grey) and reduced equivalent (black) for three critical buses that were selected to be in areas where voltage extremes are expected.

Table 3.1: Characteristics of the 7 feeders investigated using the reduction methodology. All feeders studied are publicly available.

Feeder	Nodes	Length [km]	Model complexity
UCSD A	1302	4.3	Only one voltage level
Feeder K1	1751	7.1	Large distributed capacitor bank
EPRI 7*	2452	4.1	Aggregated load at feeder head
Feeder M1	3153	3.5	High shunt capacitance
EPRI 5	3437	5.2	Low complexity model
Feeder J1	4245	18.1	Large PV system at feeder end
IEEE 8500	8531	18.2	Extremely detailed transformers

error can be attributed to the inclusion of shunt capacitance into the load aggregation and network re-construction and the constant power assumption (compared to fixed current in [1]).

Counter-intuitively, when no buses are removed the error is non-zero error. This is due to the implementation of the power flow solver, i.e. differences in how the feeder is originally modeled and how the algorithm represents it using simplified elements. If solely the new admittance matrix and power vectors were used to solve the power flow, we would expect the error to be zero.

The time required to reduce the circuit is also less for the inversion reduction (Fig. 3.6). This is expected, as the inversion reduction is based on Gaussian elimination, as opposed to a recursive method. In both methods the inclusion of more CB in the reduction increases the required reduction time. In the inversion method, more CB increases the size of the system inversion during reduction (see (3.17), whereas [1] is required to loop through more buses.)

3.6.3 Validation on the complete set of feeders

As observed in Fig. 3.7, the maximum error for any feeder (the worst case) never exceed 0.008 pu. The greatest errors occur for the two largest feeders J1 [44] and IEEE 8500 [45]. Again, non-zero error is noted for zero buses removed, for the reasons discussed previously. The lowest error occurs in the EPRI 7 Feeder [43], where the maximum error actually decreases with increasing buses removed. The low error in the EPRI 7 circuit is due to the fact that all

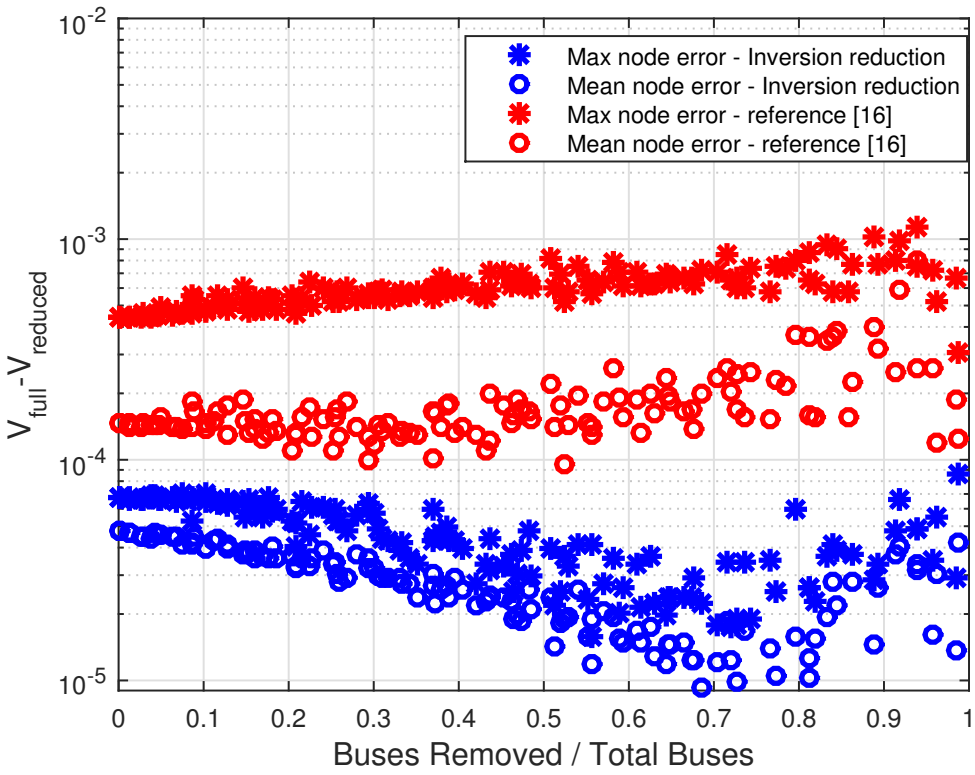


Figure 3.5: Comparison of voltage error (maximum and average of all nodes) when reducing the "UCSD A" feeder with the recursive methodology proposed in reference [1] against the inversion reduction introduced in this work.

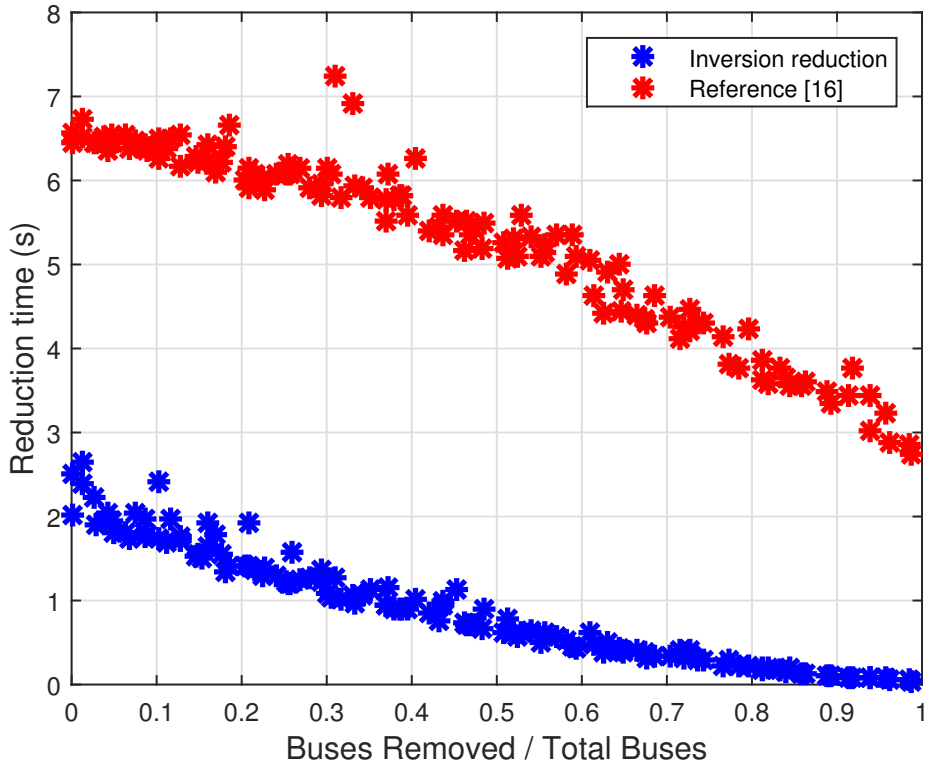


Figure 3.6: Comparison of computational time for reducing the ”UCSD A” feeder with the methodology proposed in reference [1] against the inversion reduction. Simulations are run on a desktop with Intel(R) Core(TM) i7-4770 processor with 32 GB RAM.

of the load is modeled at the feeder head, thus there is no movement of load from reduction. Since the reduction produces simplified representations of detailed models, the error due to mis-representation of elements is reduced as more buses are removed. Although not shown here for brevity, the mean error for each feeder follows the same trend with number of buses removed but is generally one order of magnitude lower, with the exception of EPRI 7 Feeder where the error is nearly identical to maximum error. In general, we see that longer feeders tend to have greater error, which is consistent with the findings in [1] where error increases with node distance from the substation.

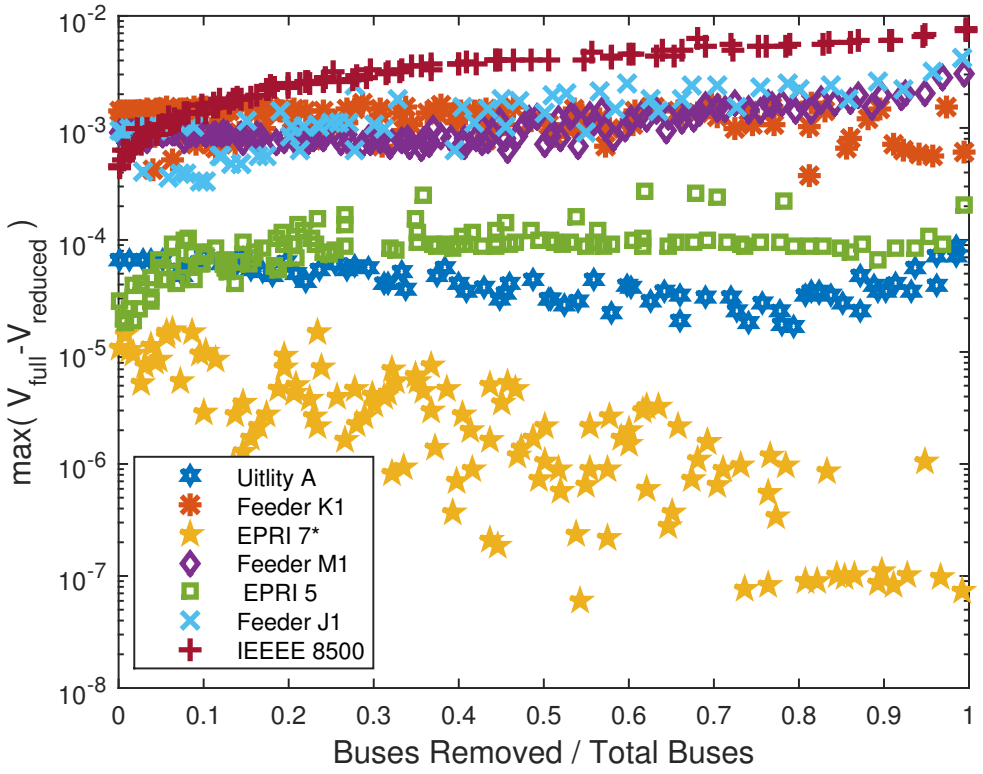


Figure 3.7: Error as a function of the number of buses removed for each of the seven feeders studied. Note the *y*-axis is logarithmic and represents the maximum difference between all node voltages between the reduced and the full feeder.

Reduction time for all feeder increases with the number of nodes in the original circuit, and decreases as more buses are removed, consistent with [1] and as observed in the previous

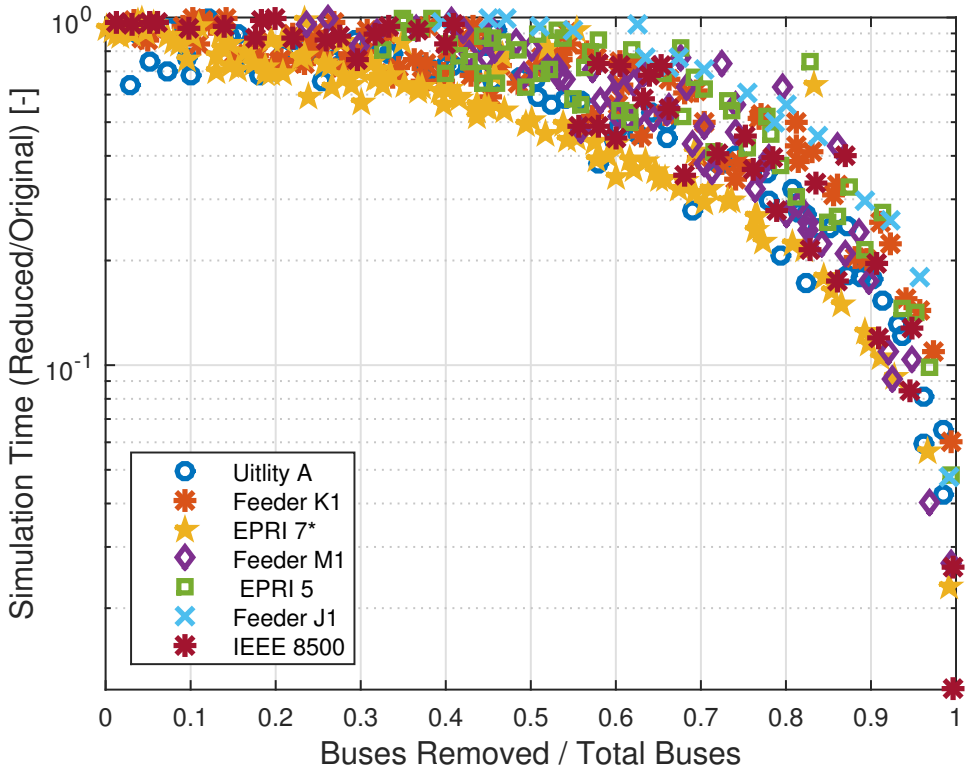


Figure 3.8: The ratio of snapshot simulation time for the reduced circuit to the original circuit as a function of buses removed from the circuit for each feeders studied.

section.

Relative power flow time savings (Fig. 3.8) are independent of feeder model. Power flow solvers time is directly proportional to feeder size, thus reducing a certain percentage of buses should reduce a similar percentage of simulation time. Specifically, decreases in simulation time is exponential as more buses are removed. For a single user-selected CB, the power flow time savings for all feeders exceed 99%.

3.7 Conclusions

A novel and general feeder reduction methodology based on Gaussian elimination, known as the inversion reduction method is proposed. The method is specifically designed to handle all of the complexities of distribution feeder models, including unbalance in loading, large shunt capacitance, and unique transformer configurations. The method is derived from first principles. A simple illustrative example demonstrates that the methodology is a generalization of the methodology proposed previously by the authors. Algorithmic details are provided.

The inversion reduction is compared against the previously proposed methodology on the same feeder and shown to be superior in both error and the speed of reduction. The methodology is then demonstrated on 6 additional feeders varying in topology, size, and modeling complexity. The maximum voltage error is small regardless of feeder size or complexity (< 0.008 p.u.).

The text and data in Chapter 3, in full, is submitted to *IEEE Transactions on Power Systems* under the title Inversion Reduction Method for Real and Complex Distribution Systems, Pecenak, Z.K., Disfani, V.R., Reno, M., Kelissl, J.,.The dissertation author is the primary investigator and author of this article.

Chapter 4

Aggregation of Voltage Dependant Inverters during Distribution Feeder Reduction

4.1 Introduction

Power system studies are becoming increasingly complex and computationally expensive due to a growing number of variable connected devices. Simplification of the power system models is an effective method to counteract this problem [41, 20, 22]. In fact, it has been observed that powerflow solution time decreases monotonically as the number of buses in the reduced model are decreased, where the greatest time saving are observed for a 1 bus equivalent system [1].

Recently, a body of literature focused on the simplification of distribution feeders for the power flow problem has been developed. The segmentation method introduced in reference [17] proposes a data driven approach in which power flow results, or measured data, can be used to represent a portion of the circuit. The method showed high accuracy on realistic feeders. However

the method only allows for the aggregation of shunt connected loads and distribution lines, while more complex devices (i.e. capacitors, transformers, regulators, PV systems, etc..) are preserved, restricting the size of the reduced feeder.

The method developed in the works [16, 1] proposes using the nodal voltage equation to reduce the circuit to a subset of buses with aggregated load and generators. The methodology is shown to be applicable to a wide number of feeders and produces low error. However, similar to [17], capacitors and transformers cannot be aggregated, and require the preservation of additional buses. Reference [46] introduces the inversion reduction technique which improves on the methods of [16, 1] by allowing for the reduction of capacitors and transformers, in addition to loads, PV systems, and distribution lines. Thus a only a minimal number of buses need to be retained.

However, changes in regulation now allow for DG to assist in voltage regulation. For example, PV inverters can modify their active/reactive power autonomously using the point of PV connection voltage as the control input. This poses a problem for reduction methods, as it requires buses of PV connection to be retained, thus increasing the number of buses in the reduced circuit. This problem has not been addressed in circuit reduction literature before.

In this work, we propose the first methodology formulated to aggregate these inverters to other buses, while i) maintaining the feeder voltages with the original circuit ii) producing the same modifications in power output. The methodology works, in short, by adjusting the control voltage measurement to replicate the voltage of the original bus. A scheme to implement the methodology for time series applications where changing load and generation lead to changing voltage shift is introduced which relies on estimation of voltage, generated from the use of voltage sensitivities.

Specifically, the contributions of this work to the literature on circuit reduction is:

- The first methodology to aggregate voltage controlled devices on the distribution system
- Introduce reduction of generators with inverter sizes not equivalent to generator size (i.e.

over/under-sized)

- Design of QSTS which uses voltage sensitives in parallel with powerflow solver as input to control problem

The paper is organized as follows. Section 4.2 introduces the reduction scheme from reference [46] that is used in this work. Section 4.3 first introduces the voltage control schemes discussed in this paper by PV inverters, then details the methodology of aggregating inverters during circuit reduction which is tested on a small feeder with one inverter. Section 4.4 introduces the algorithm used to extend the methodology of inverter aggregation to general time series applications and validates the methodology on a real medium voltage California circuit with 364 inverters for 24 hours of real operating characteristics.

4.2 Circuit Reduction Overview

Circuit reduction is implemented to create an equivalent smaller feeder which maintains the voltage of a subset of buses that are desired to study, while others are ignored. Typically, the logic is characterized by removing buses, distribution lines, and transformers of the circuit, while the loads, capacitors, and generators on the circuit are aggregated to the remaining buses. New lines and transformers are created to connect the remaining buses, which represent the original connection between the buses. New aggregate loads, capacitors, and generators are created at each bus which are composed of portions of the original load, distributed according to their expected powerflow.

The inversion reduction technique is used in this paper as introduced in reference [46]. The methodology is summarized below, while the modification made to how PV is aggregated is introduced in the following subsection (See 4.3.2). For the detailed derivation and validation, the reader is directed to the reference.

The reduction begins by writing the nodal voltage equation for the original circuit (eq. (4.1)), as well as a reduced equivalent circuit composed of only critical buses (CB) in the original circuit (eq. (4.2))

$$V_o = \mathbf{Z_o} I_o \tag{4.1}$$

$$V_r = \mathbf{Z_r} I_r \tag{4.2}$$

where the subscripts o and r represent the original and reduced circuits, respectively. As per the objective of the reduction, we desire to make the voltage of the CB in the original circuit equivalent to the buses of the reduced circuit (i.e. $V_o(CB) = V_r$). Thus we can write

$$\mathbf{Z_{o,CB}} I_o = \mathbf{Z_r} I_r \tag{4.3}$$

where $\mathbf{Z_{o,CB}}$ is the impedance matrix with all rows removed except those that correspond to the critical nodes.

To remove the dependence on current, a constant power assumption is introduced using eq. (4.4)

$$S = \mathbf{diag}(\tilde{V}) I^* \tag{4.4}$$

where the superscript $*$ represents the conjugate. Substituting eq. (4.4) into eq. (4.4), and simplifying yields a vector of equivalent power injections in the reduced circuit (S_r).

$$S_r = \mathbf{W} \times S_o \tag{4.5}$$

where $\mathbf{W} = \mathbf{diag}(\tilde{V_r}) \times (\mathbf{Z_r}^{-1} \times \mathbf{Z_{o,CB}})^* \times \mathbf{diag}(\tilde{V_o})^{-1}$.

A separate vector (S_r) is created for loads, generators, and PV's whose entries represent

an aggregate power injection on a bus.

The reduced impedance network ($\mathbf{Z_r}$) is formed by simply removing the rows and columns of $\mathbf{Z_o}$ that do not correspond to CB.

$$\mathbf{Z_r} = \mathbf{Z_o}(CB, CB) \tag{4.6}$$

4.3 Inverter Aggregation Principles

4.3.1 Inverter control schemes

Changes in California rule 21 and IEEE 1547 [2] allow for the modification of power output from distributed generators (DG) to assist in voltage regulation. The DG inverters, which use power electronics to control power output are an ideal source for this control scheme. Due to a lack of communication network in the distribution grids, these inverters typically operate in an autonomous manner where power output is determined based on a specified control curve that is programmed into the inverter at the time of production.

A number of autonomous voltage control schemes have been proposed which can be categorized broadly as i) voltage dependent and ii) voltage agnostic. Methods that are voltage agnostic include fixed power factor, power factor scheduling, fixed VAr output, and frequency-droop control. These control schemes are characterized by modifying power output where the voltage is not the dependent variable of the control curve. This class of inverter control poses no problem to the reduction scheme, since the output is independent of the bus to be removed.

However, the second class of inverter control schemes, whose control action is dependent on local voltage conditions create a unique challenge. The nature of circuit reduction, which removes buses that are not of interest, is contradictory to the control scheme which relies on the voltage information of that bus. These control schemes include Volt/VAr, Volt/Watt, and voltage droop control. Volt/VAr control is the focus of our work, and an example of Volt/VAr curve is

given is in figure 4.1.

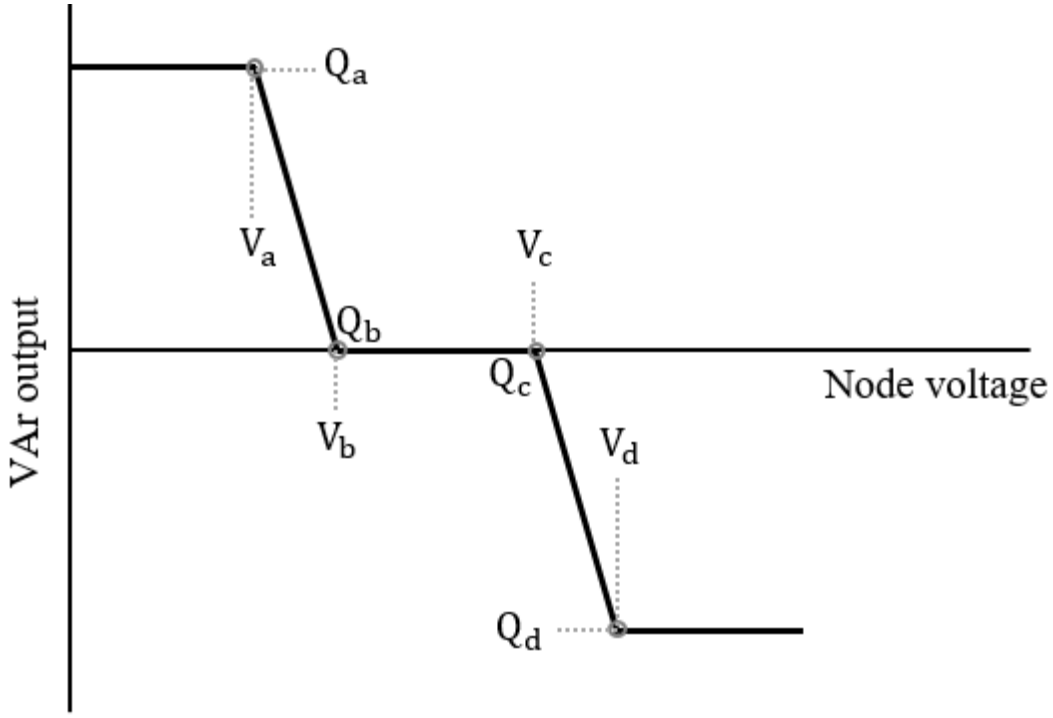


Figure 4.1: Depiction of the category B type volt/VAr curve as defined by the IEEE 1547 standard [2].

4.3.2 Aggregation of Inverters

PV/Inverter aggregation

As is posed in eq. (4.5), the PV systems ($S_{r_{pv}}$) are aggregated equivalents composed of the original PV systems ($S_{o_{pv}}$). However, the reduction formulation can be changed to retain information about the movement of individual PV systems through the modification given in eq. (4.7).

$$\mathbf{S_r} = \mathbf{W} \times \mathbf{diag}(S_o) \tag{4.7}$$

In this equation, $\mathbf{S_r}$ takes the form of a matrix with dimensions of $N \times M$. Here, each row represents a node on the reduced circuit and the columns represent a node in the original circuit. Each entry represents a single PV system that is being transfered from the original node to the reduced node. Therefore, in this approach, several PV systems are co-located at a single node in the reduced system. For consistency, we note that the summation of row of $\mathbf{S_r}$ (or all the PV systems) results in the vector form of eq. (4.5) (i.e. $\sum \mathbf{S_r} = S_r$).

The inverters can be aggregated in a similar way by considering their power rating $\bar{S}$. A similar form to eq. (4.7) is introduced to aggregate the inverters in eq. (4.8).

$$\bar{\mathbf{S}}_{r_d} = \mathbf{W} \times \mathbf{diag}(\bar{S}_o) \tag{4.8}$$

Implementation of both equations (4.7) and (4.8) into the reduction methodology created in [46] and summarized in section 4.2 gives the final reduction methodology applied in this paper.

Inverter curve shift

However, the movement of inverter and PV systems described above does not address the control curve associated with an inverter, which is dependent on the voltage of the node it was originally located on. Therefore, for the controller to be equivalent when transferred to a new bus, a voltage shift which relates the voltage of the original node to the new node should be applied to the voltage at which the controller acts (see Fig. 4.2). Hereafter, the voltage shift is referred to as the voltage difference addend (VDA).

To determine the correct VDA, we leverage the voltage drop equations introduced in references [16, 1, 46], which form the basis of distribution feeder reduction techniques.

For any three bus system with neighboring buses i, j, k, where j is between buses i and k,

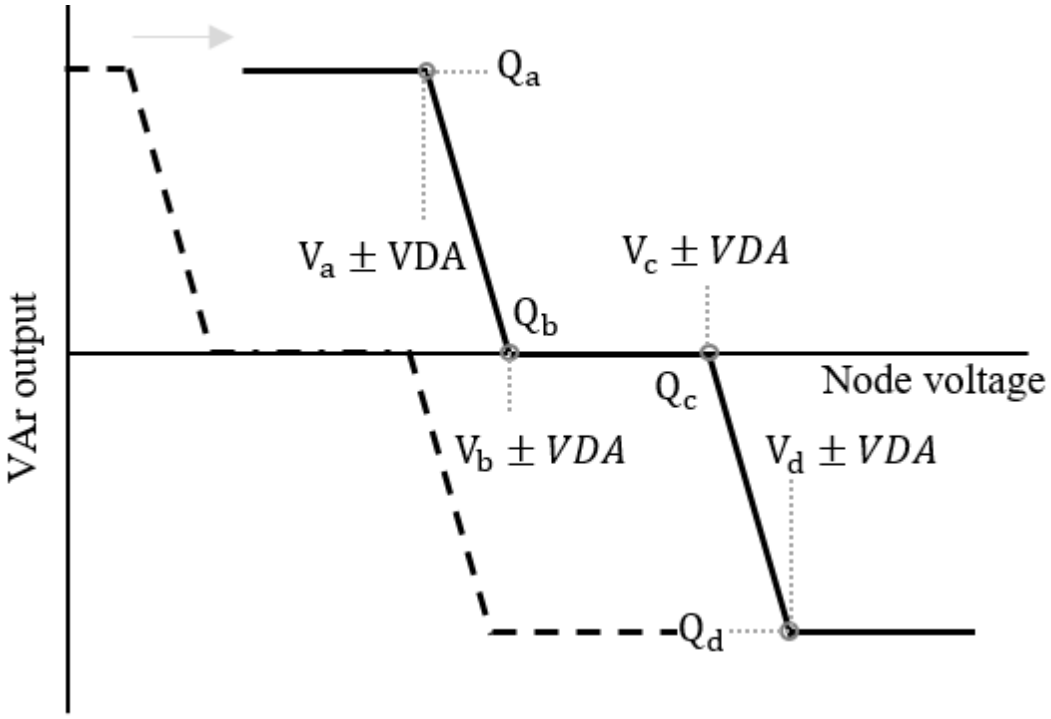


Figure 4.2: Depiction of the effect of applying the VDA to the Volt/VAr curve. The original curve is given by the dotted lines and the updated curve is given by the solid lines. The shape of the curve remains the same, however the voltage at which the inverter activates is ”shifted”.

we can write the p-phase voltage vector for buses j and k as follows:

$$V_j = V_i + \mathbf{Z_{ij}}(I_j + I_k) \tag{4.9}$$

$$V_k = V_j + \mathbf{Z_{jk}} I_k, \tag{4.10}$$

where $V \in \mathbb{C}^{p\times 1}$ and $I \in \mathbb{C}^{p\times 1}$ are the vectors of voltages and current injections of the p-phase bus, and $\mathbf{Z} \in \mathbb{C}^{p\times p}$ is the full impedance matrix of the line connecting the buses, where the diagonal elements denote self impedances and off-diagonal elements denote mutual impedances between different phases of the line.

We can define the voltage change between buses as:

$$\Delta V_{ji} = V_j - V_i = \mathbf{Z_{ij}}(I_j + I_k) \tag{4.11}$$

$$\Delta V_{kj} = V_k - V_j = \mathbf{Z_{jk}} I_k, \tag{4.12}$$

$$\Delta V_{ki} = V_k - V_i = \mathbf{Z_{jk}} I_k + \mathbf{Z_{ij}}(I_j + I_k), \tag{4.13}$$

For any inverter moved between the set of neighboring buses, equations (4.11 - 4.13) can be applied to determine the appropriate VDA. However, determining these equations becomes complex algorithmically for larger systems with differing topologies and large distance of inverter movement.

Systematically, we can write the voltage drop using the nodal voltage equations, as given in eq. (4.14).

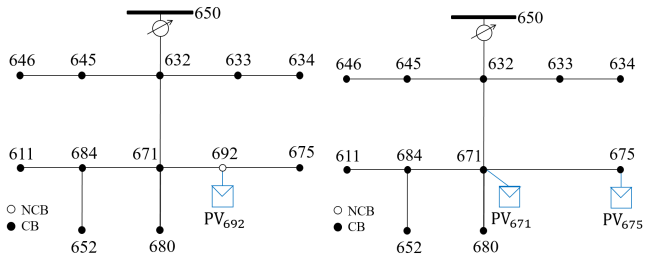
$$V_o = \mathbf{Z_o} \times I_o. \tag{4.14}$$

Therefore the voltage drop between any two buses can quickly be determined by subtracting the rows of (4.14). In addition, the use of this form of equation includes the effect of moving controllers across lines with negligible shunt capacitance and voltage shifting transformers.

It is important to note that the currents considered in (4.14) are the rated currents. As will be discussed in following sections, this has the effect of only making the VDA only applicable to the case of full loading. However, this is rare in practice, and the current loading must be considered to calculate the VDA for the current conditions. However, we begin using the rated current as a first proof of concept.

4.3.3 Snapshot case study

The reduction of a simple system with only one inverter is examined using a snapshot powerflow to determine the validity of the VDA method. The analysis is carried out using the IEEE 13 bus circuit [47], with a three phase PV system added to bus 692. The PV system, labeled PV_{692} is a 600kW system with a unity inverter sizing ratio (inverter AC power / PV DC power = 1). The PV is 3.5 times the size of the load on the bus and is outputting half of it's rated power (i.e. assumed irradiance of 500 W/m^2). All loads are operating at their rated power (i.e. highest loading). OpenDSS [36] is used to solve the powerflow and apply the control.



(a) (b)

Figure 4.3: Depiction of the IEEE 13 bus system studied. (a) The original circuit was retrofitted with a PV system at bus 692. (b) The reduced circuit with bus 692 removed results in two PV systems on the neighboring buses (buses 671 and 675).

A depiction of the IEEE13 bus feeder with the added PV_{692} is given in Fig. 4.3.a. Here, we are removing only the bus with the inverter. The equivalent reduced circuit is one in which the PV is split between the two neighboring buses, creating two new systems (PV_{671},PV_{675}) as

observed in Fig. 4.3.b. To account for voltage differences across bus phases, individual inverters are applied to each phase of the resulting PV systems.

A depiction of the VDA modified control curves for each phase of the resulting PV systems is given in Fig. 4.4. In all cases, we observe that VDA is positive for downstream bus (675) and negative for the upstream bus (671). A larger shift is noted for the control curves on phase A of the inverters relative to the other two phases indicating a larger voltage difference.

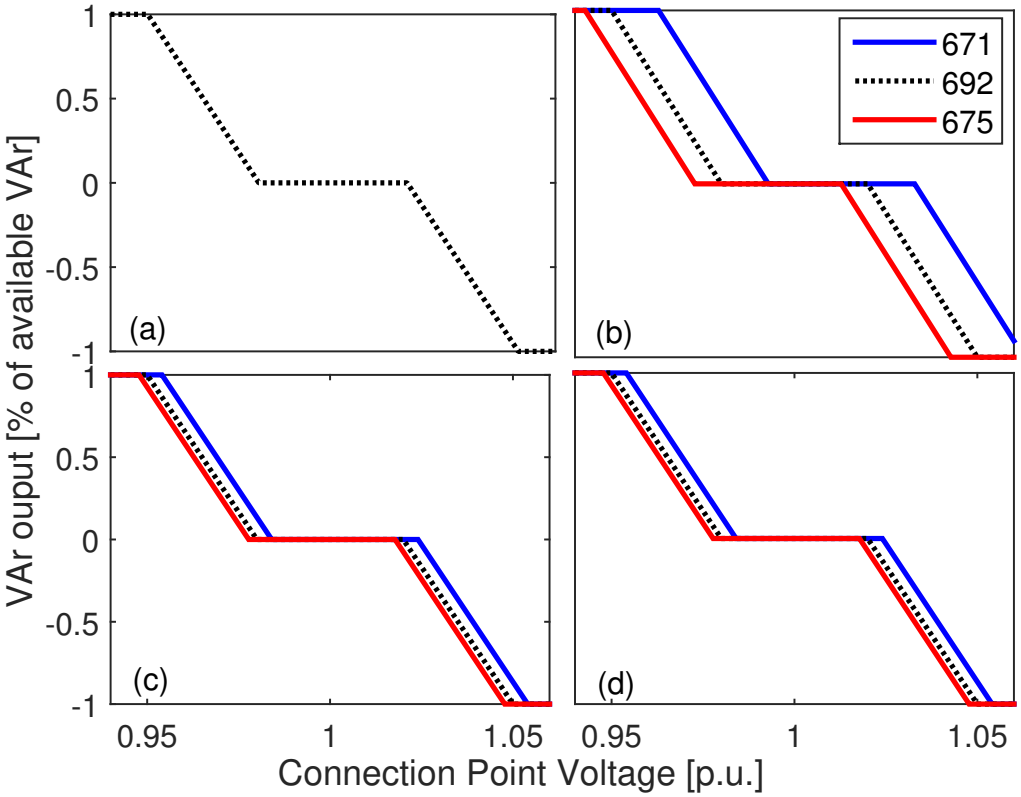
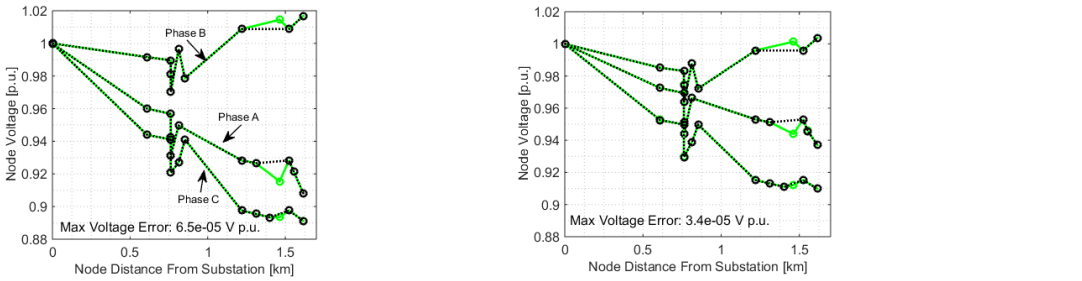


Figure 4.4: The VoltVAr curves for the PV systems. (a) The three phase curve for the original system, used as reference for the modified curves. The VDA modified curve for PV PV_{671} and PV_{675} for (b) Phase A (c) Phase B (d) Phase C.

For system equivalence from the control perspective, it is desired that the two smaller PV inverters control results in equivalent nodal voltages and equivalent reactive power support. A comparison of the voltage between the reduced and original feeder voltage is compared for the i) uncontrolled powerflow (Fig. 4.5.a); ii) the controlled powerflow (Fig. 4.5.b). Without

Volt/VAr control bus 692 experiences an unacceptable voltage (< 0.95 p.u.) for both phases a and c. VoltVAr control raises the feeder voltages.

Consistent with references [1, 46] the reduction produces little error for a circuit without Volt/VAr control applied. However here we present low error in the nodal voltage when the Volt/VAr control is applied. For the snapshot used, the reduction voltage error is actually decreased when the control action is applied.



(a) (b)

Figure 4.5: Voltage plotted as a function of distance for all nodes of the original circuit (green) and the reduced circuit (dashed black).

As per the objective of the VDA approach, the sum of reactive power produced from inverters on PV_{671} and PV_{675} is nearly identical to the reactive power output from the inverter on PV_{692}. The largest error is observed for phase b and is to the normalization of a small number (i.e. negligible reactive power output). In addition the reactive power provided from the substation and the reactive power loSSEs are nearly identical for both the full and reduced feeders.

4.4 Time Series Simulation of Aggregated Network

4.4.1 Framework overview

The trademark of QSTS involves studying the feeder under varying loading conditions. However, the VDA methodology as introduced above is only applicable for the loading considered

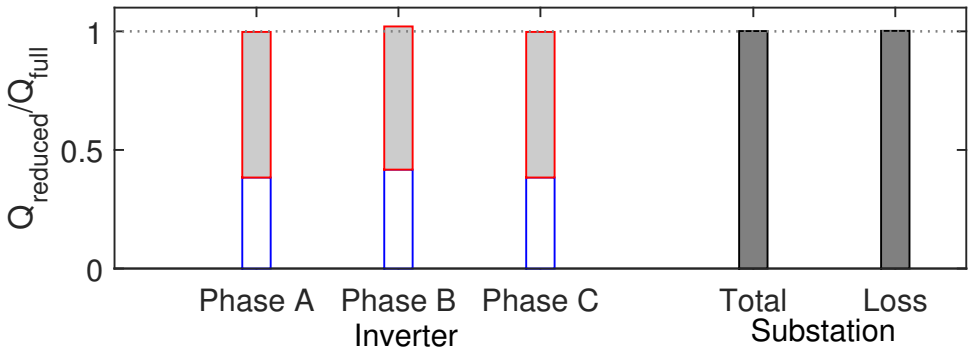


Figure 4.6: Reactive power injection and loSSEs of the reduced circuit normalized by the results of the original circuit.

during the reduction (typically rated loading). To extend the applicability of the methodology to general studies, a correction to the VDA must be applied considering the updated loading.

Our proposed framework is to include the VDA update directly in the QSTS framework and is introduced visually through the flowchart in Fig. 4.7. On the left hand side, a typical QSTS logic is introduced. The QSTS is solved as follow: After the initial compilation of the circuit, the solver begins iteratively solving the powerflow for a predefined number of time-steps where loading conditions are known. Within the solution loop at each time step the loading is given as input and the powerflow solution is obtained. The solution to the powerflow is then given as an input to the controller which iteratively solves the control problem. The loop is broken after all timesteps have been solved.

In our framework, an update step is added in parallel to the powerflow update and solution process that updates the VDA for each inverter. The updater is given the current loading for the original circuit as input, which is used to estimate the change in nodal voltage of each bus in the original circuit. The VDA for each curve is determined by the difference between the estimated voltage between the original PV bus and the one it is aggregated to in the reduced feeder.

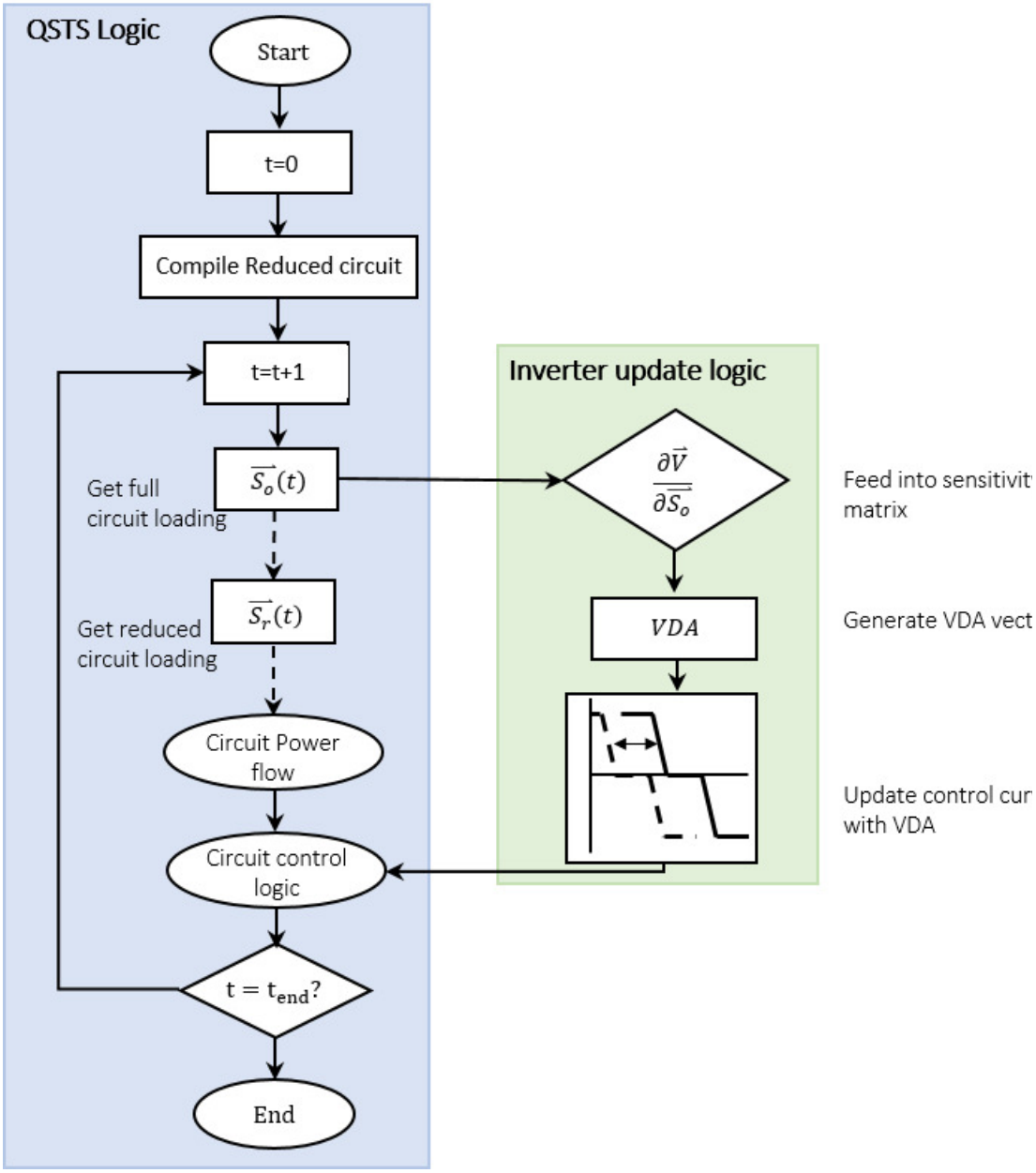


Figure 4.7: Flowchart describing a typical QSTS logic (left, blue box) with a parallel updater which corrects the VDA that is applied to each curve.

4.4.2 voltage estimation

Explanation

The VDA is calculated by the voltage difference between the bus that the PV is located in the original circuit and of the bus it is moved to in the reduced circuit. Therefore, an estimate of nodal voltages of the full circuit considering the current loading is needed a priori for the VDA to be calculated.

To this purpose we introduce a voltage estimation technique which is based on voltage sensitivities and the concept of distribution factors. Both voltage sensitivities and distribution factors have been used classically as a means for fast voltage estimation [48, 49, 50, 51].

To produce the voltage estimate, non-linear sensitivity equations are used which model the effect of varying load consumption or generator output on the voltage of each node on the network. For each individual load and generator in the circuit, it's consumption/generation is varied from its rated value to zero power output in increments of 2% power change with all other loads/generators operating at full capacity. For each increment, the voltage of each node on the circuit is recorded. A polynomial equation is used to model the change in each nodal voltage to change in power delivered/consumed of the single load.

For any node $m \in M$, we model the nodal voltage change due to change in apparent power (S) for a given load $\ell \in L$ using a polynomial of degree C as given in (4.15).

$$V^{(\ell,m)} = a_o^{(\ell,m)} + a_1^{(\ell,m)} S_\ell + a_2^{(\ell,m)} S_\ell^2 + \cdots + a_C^{(\ell,m)} (S_\ell)^C \tag{4.15}$$

where a represents the coefficients of the polynomial. The term $a_o^{(\ell,m)}$ represents the voltage of the node at full load consumption. Thus the remaining portion of the right hand side gives the

voltage deviation caused by a drop in the loading (S_ℓ). Therefore, we can write

$$\Delta V^{(\ell,m)} = a_1^{(\ell,m)} S_\ell + a_2^{(\ell,m)} S_\ell^2 + \cdots + a_C^{(\ell,m)} S_\ell^C \tag{4.16}$$

Note, if a first order polynomial is used, the linear sensitivity factors commonly found in literature is recovered. The extra terms are used to account for nonlinearity in load models. Here, a similar form is used to represent changes in voltage to changes in generation. The polynomial fitting is completed off line and is assumed to be representative for a fixed feeder configuration.

For fast estimation of voltage a 3 dimensional function is created as depicted in Fig. **??**. The marginal change in voltage at each node from each load is represented by the matrix $\partial \mathbf{V}/\partial \mathbf{S} \in \mathbb{C}^{M \times L+G}$ is created, where L and G are the number of loads and generators in the system, respectively. The total predicted change nodal voltage ($\partial V \in \mathbb{C}^{M \times 1}$) is found by summing along both the second dimensions. The final predicted voltage vector ($\tilde{V} \in \mathbb{C}^{M \times 1}$) is given by addition of voltage of each node at full loading with the change due to current loading, $\tilde{V} = a_o + \partial V$

The VDA for any PV system that was moved from a node m_o in the original circuit to a node m_r in the reduced circuit can then be calculated by eq. (4.17).

$$VDA = \tilde{V}_{m_o} - \tilde{V}_{m_r} \tag{4.17}$$

Benchmark

To test the accuracy of the method, we compare the voltage prediction to real powerflow results for 53 days (11/25/2014-1/16/2015) on a real California MV distribution feeder. The feeder studied was first introduced in [52], but was also studied in [1, 46, 53]. The feeder has 621 multi-phase buses, two distribution transformers, one large capacitor bank (1350 KVAr), 364 distributed rooftop PV systems, and 471 loads. The feeder lines are modeled with shunt capacitance, and all neutral connections are assumed to be grounded perfectly.

Each load on the feeder operates under the same time-series shape scaled by its peak load, while each PV time-series is uniquely determined using a sky imager according to the method introduced in [52]. The time-series are of 30s resolution for both irradiance and demand, which marks the resolution of the powerflow simulation over the period. the rational behind using 30s time resolution is discussed in reference [1].

In the model, all loads and generator operate at constant power factor, meaning that changes in real power correlate to a specific value of reactive power. For loads that do not operate in this manner, a separate entry for both the active and reactive component of the load should be considered in $\partial \mathbf{V}/\partial \mathbf{S}$. Further, we fit the equation with a third order equation.

The confidence intervals on difference in estimated nodal voltage and actual powerflow solution are given in Fig. 4.8. For the 52 days, the maximum voltage estimation error is on the order of 10^{-4}. Estimated error can be observed to be correlated to the shape of load consumption (00:00-7:00; 17:00-24:00) and PV generation (7:00-17:00).

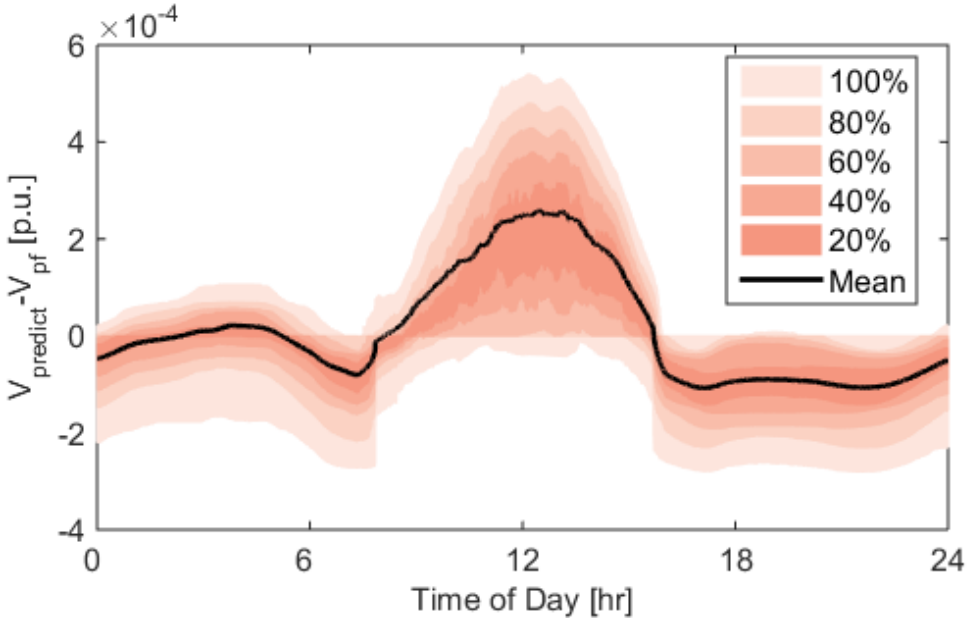


Figure 4.8: Confidence interval (0-100) plot of prediction error over 53 test period. Lighter shading indicate less likelyhood.

4.4.3 QSTS case study

The VDA time series framework is tested on the real medium voltage California distribution feeder introduced in section 4.4.2 for the 24 hour period on 11/21/2014. The study day was chosen due to 1) Not being in the set used for the benchmark analysis; 2) a large increase from mid-day low load to night time peak; and 3) partly cloudy irradiance profile throughout the day.

The demand and irradiance data were gathered as introduced in section 4.4.2. A depiction of the normalized demand and irradiance timeseries profiles for one load and one PV system are given in Fig. 4.9. The simulation resolution is again 30s.

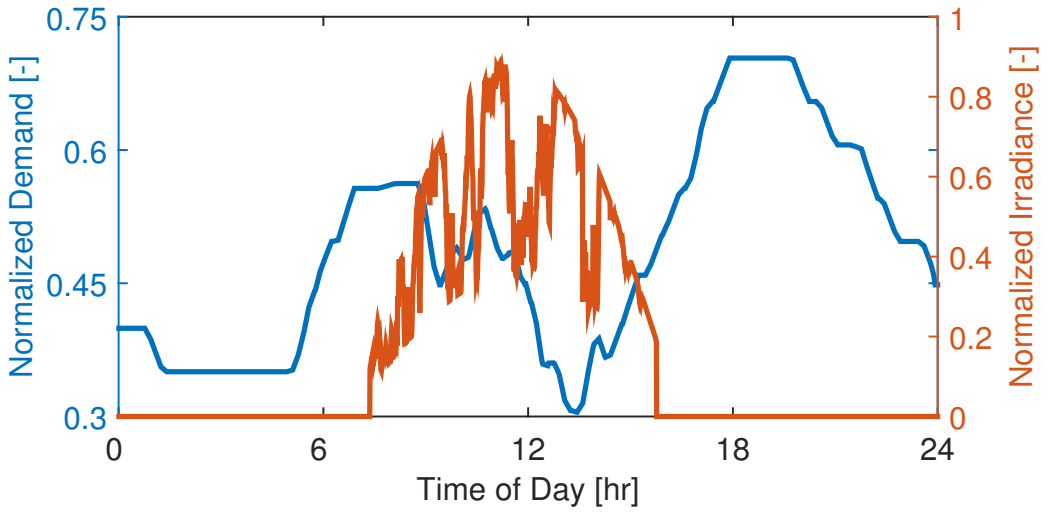


Figure 4.9: Double axis time series plot of the loading for the simulation day. (left, dash-dot blue) Demand shape for all loads in the circuit. (right, solid red) PV profile for a single PV in the circuit.

The methodology is tested by reducing the feeder to 300 randomly selected buses from the original 621 (52% reduction). Due to inverter splitting as discussed in section 4.3.3, the original 364 inverters resulted in 700 equivalent systems. The topology of the feeders is given in Fig. 4.10

The effect of Volt/VAr control on the circuit is observed in Fig. 4.11. During the middle of the day ($\approx 10:00-14:00$), the maximum voltage reaches 1.035 V p.u. which exceeds the upper voltage limit of the deadband (1.02 V p.u.; Fig. 4.4.a). When Volt/VAr control is applied,

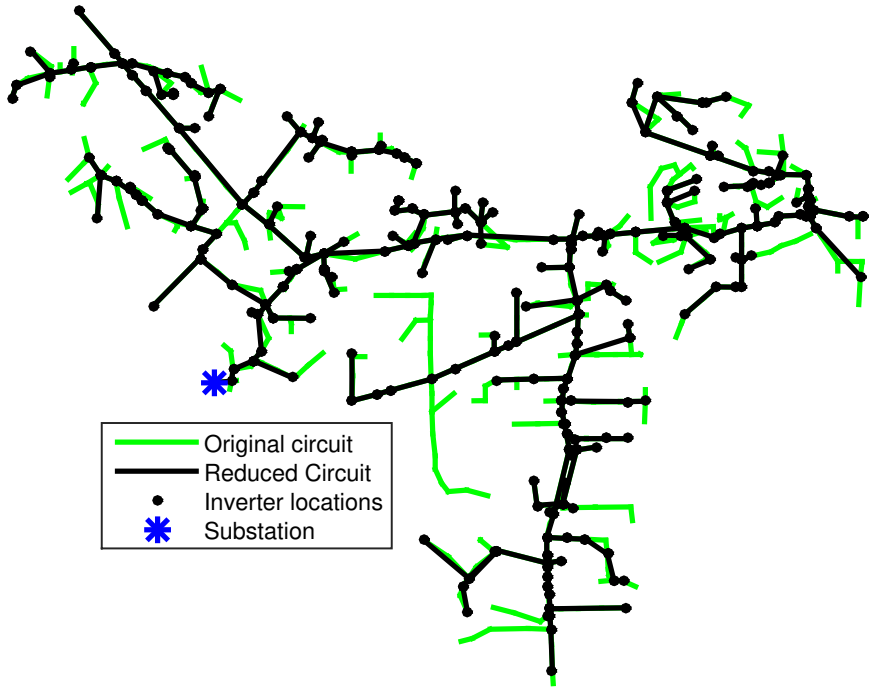


Figure 4.10: The original and reduced circuit topology with the location of inverters given for the reduced circuit.

the voltage is lowered to 1.025. During the evening peak loading ($\approx 17:00-23:00$), the voltage reaches a low of 0.97 V p.u.. When Volt/VAr control is applied, the voltage is raised to 0.98 V p.u..

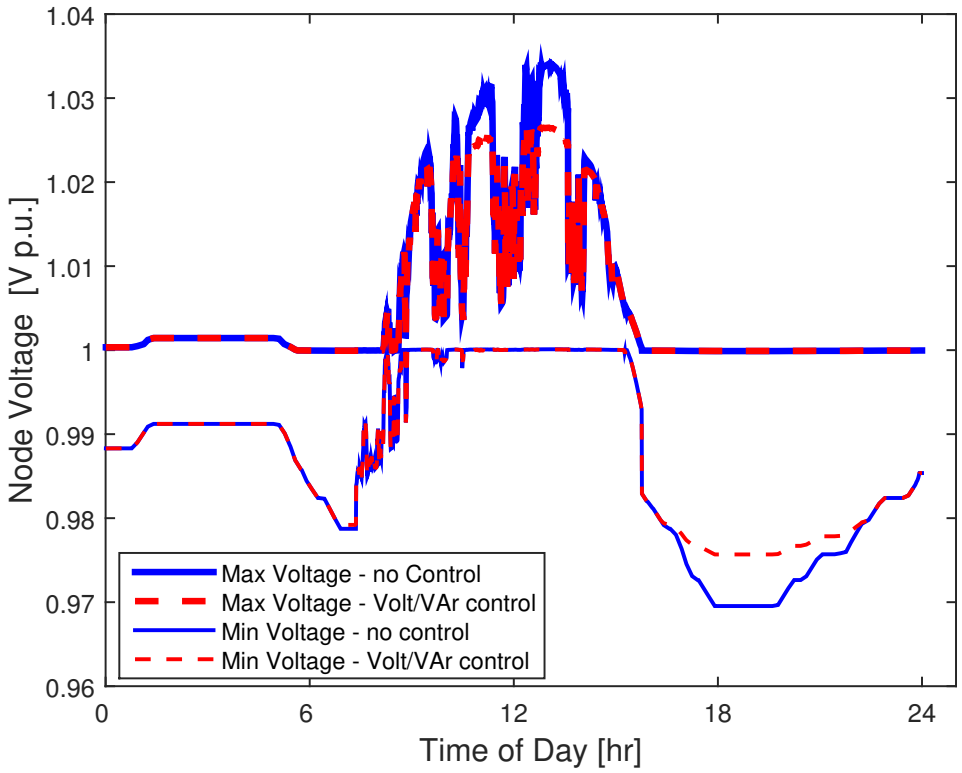


Figure 4.11: Voltage time-series for the full feeder for the day studied for the (blue) uncontrolled inverters and the (red) controlled inverters.

The total inverter reactive power output time series is plotted in Fig. 4.12 on the left handed axis. During the middle of the day, the inverters absorb power to reduce the voltage. In the afternoon, the inverters inject reactive power to increase the voltage.

The difference between the total reactive power injection from the full circuit and the reduced circuit with equivalent inverters is plotted on the right side of the axis. For all injections, the error is less than 1%. The error is positively correlated with the total inverter injection.

The nodal voltage error (Fig. 4.13) incurred from reduction without Volt/VAr control is generally small, with a maximum error of -2×10^{-5} which is consistent with reference [46].

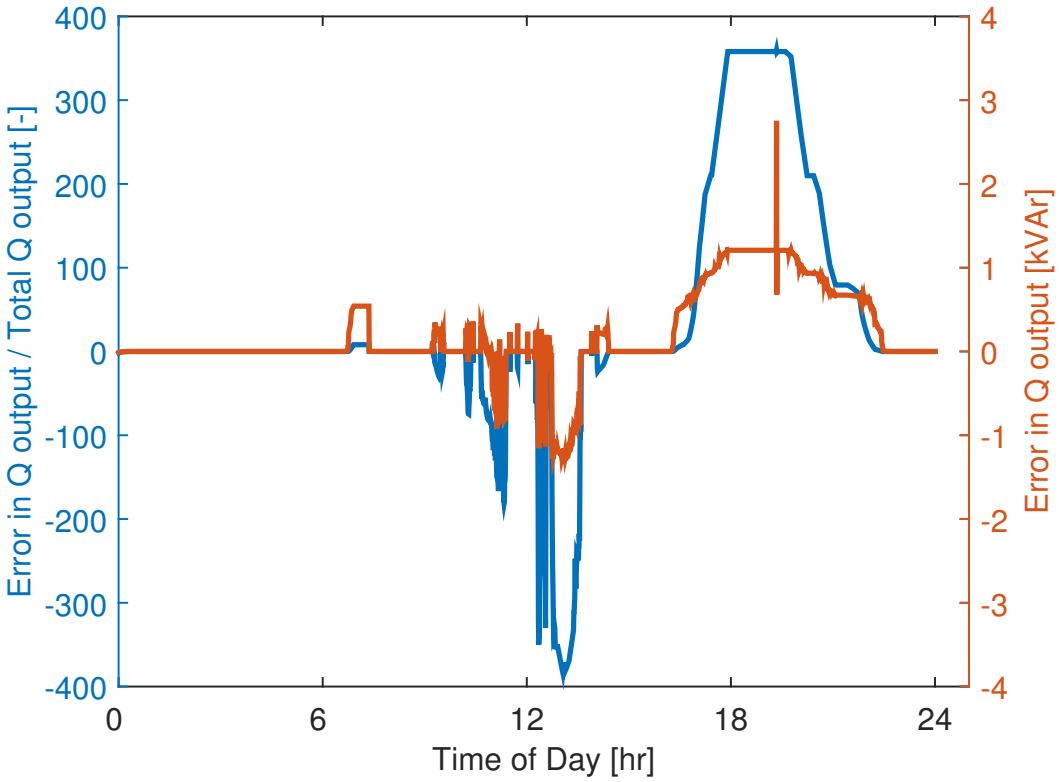


Figure 4.12: Double axis plot representign reactive power in the full and reduced circuit. (left) Total reactive power input from inverters timeseries. (right) difference between total inverter reactive power output between the reduced circuit and original circuit.

When Volt/VAr control is applied, the absolute maximum error is reduced to 1×10^{-5}. During the periods when reactive power is injected or consumed by the inverter, the error is decreased to near zero.

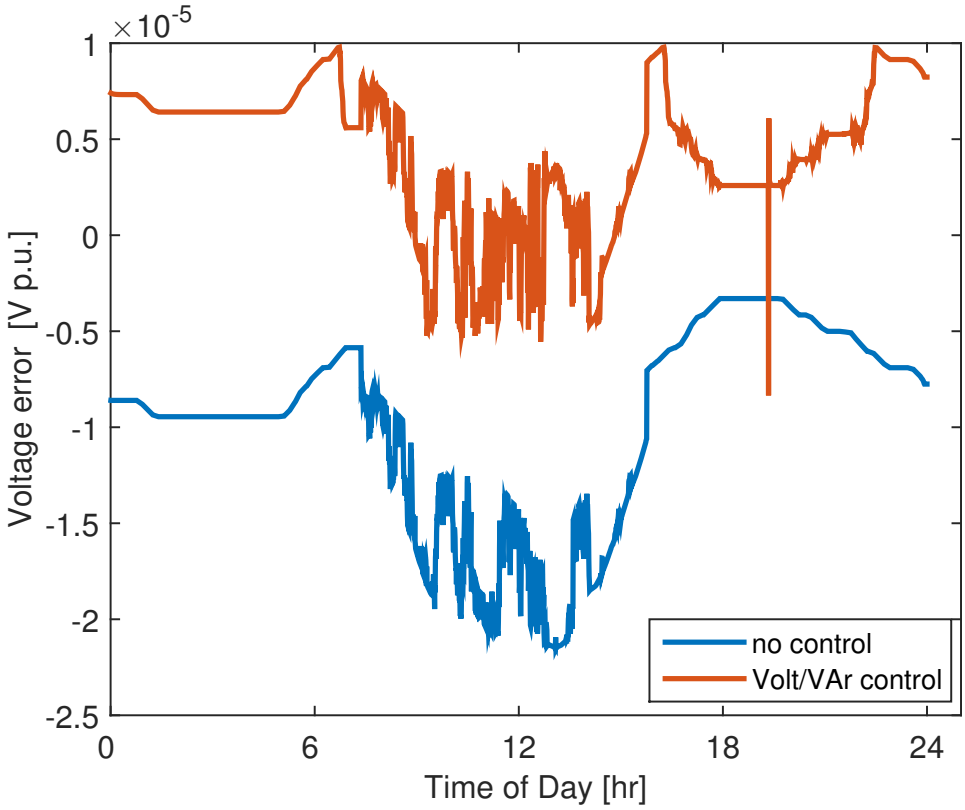


Figure 4.13: Maximum nodal voltage error between the reduced and original circuit when (blue) no control is applied and (red) when Volt/VAr control is applied.

4.5 Conclusions

In this work, the inclusion of voltage controlled inverters in circuit reductions is considered for the first time. Traditionally voltage controlled devices require the inclusion of excessive buses in the reduced circuit, as the their voltage information is used as input to the controlled devices. The device studied in this work is Volt/VAr controlled PV inverters whose power is modified in an attempt to regulate local voltage, however the methodology is extend-able to other control

schemes that depend on local voltage measurements.

The methodology works by modifying the circuit reduction technique introduced in reference [46] to retain individual PV system / inverter systems on each node, as opposed to the traditional composite systems. A shift to the control curve of each individual inverter, dubbed the voltage shift addend, is applied that links the expected voltage on the original inverter bus to that which is measured on the aggregated bus. A voltage sensitivity based estimation technique is employed to generate the addend for general time series application with changing feeder loading.

The method is shown to be highly accurate for a 24 hour simulation on a real California distribution feeder with 52% of the circuit removed. The total inverter output is shown match the original circuit, with a maximum difference of less than 2 kVAr regardless of inverter output. The maximum nodal voltage error for the period is always less than $1 * 10^{-5}$ [V p.u.], which actually improves the error due just to reduction ($2.2 * 10^{-5}$ [V p.u.]).

Chapter 5

Closing remarks

5.1 Recap

In this work, a state-of-the-art circuit reduction technique that is designed specifically for realistic and complex distribution feeders is introduced. The methodology is only the technique that is designed to reduce circuits with i) multiphase connections through out the entire network ii) mutual coupling between multiphase unbalanced lines iii) unbalanced loads and generation iv) spatial variation in load and generation v) shunt capacitance in distribution lines vi) multiple voltage levels vii) voltage shifting transformers, that accounts for changing demand and generation without requiring an initial powerflow.

In Chapter 2, the core of the method is introduced using a recursive technique to remove buses systematically which adresses points i)-iv) above. The topology detection algorithm is introduced which is used through out the work. Detailed algorithms of implementation are given such that the reader could easily implement the method. A detailed validation was carried out on a real California distribution feeder to gain understanding of the error in the method with respect to load model used, net load, nodal distance from substation, and with respect to the number of buses removed from the circuit. For all scenarios low error was observed, with a maximum error

of .0113 V p.u. Finally, up to 96% time savings of a year long simulation were observed.

In chapter 3 of the thesis, an advanced feeder reduction technique which uses linear algebra, as opposed to recursion, is introduced referred to as the inversion reduction technique. The nature of the method allows for the inclusion of points v) -vii) into the methodology. An algorithm is given that introduces the logic for translating from an impedance matrix to full definitions required by a commercial powerflow solver. Compared to the previous method, inversion reduction incurs one less order of magnitude error and takes half the time to complete the reduction. Given the flexibility of the method, validation is also carried out on 7 publicly available distribution feeder models. Low error is observed regardless of feeder size with a maximum error of 0.007 V. p.u. for the IEEE 8500 node feeder.

In chapter 4, we introduce the first methodology for reduction of voltage dependent control devices such as smart inverters. The method uses a novel voltage control measurement shift addend to augment the measured voltage to reflect the voltage to it's original bus. The methodology is observed for a single inverter movement, and actually reduces the error from reduction compared to the control scheme. To extend the methodology to be applicable for time series applications, a voltage estimation technique is introduced to represent voltage shifts given a current loading. The methodology is shown to produce low error for the scenario tested.

5.2 Future Work

The reduction thus far has been focused on reducing the time required to QSTS power-flow simulations. However, this is only one of the problems in power system literature that is experiencing the computational burden due to increasing model complexity. Due to it's nature as a network reduction technique, the methodology can be extended to any problem which uses a network.

One such problem is state estimation (SE). The SE problem as introduced by Fred

Schwappe in 1968 is ”a data processing algorithm for converting redundant meter readings and other available information into an estimate of the state of an electric power system” [54, 55, 54]. Typically, a solver such as weighted least squares is applied to fins the solution. However, more sophisticated solvers such as semi-definite programming (SDP) are becoming popular. SDP is a linearization technique in which the the solution is convex and therefore a global optimum is guarenteed However, the time required to solve the SDP-SE can become infeasible quickly for even moderately sized circuits [34].

Circuit reduction has the potential to solve the problem by aggregation of measurements. The basic idea is introduced in Fig. 5.1, where measurements are aggregated during reduction.

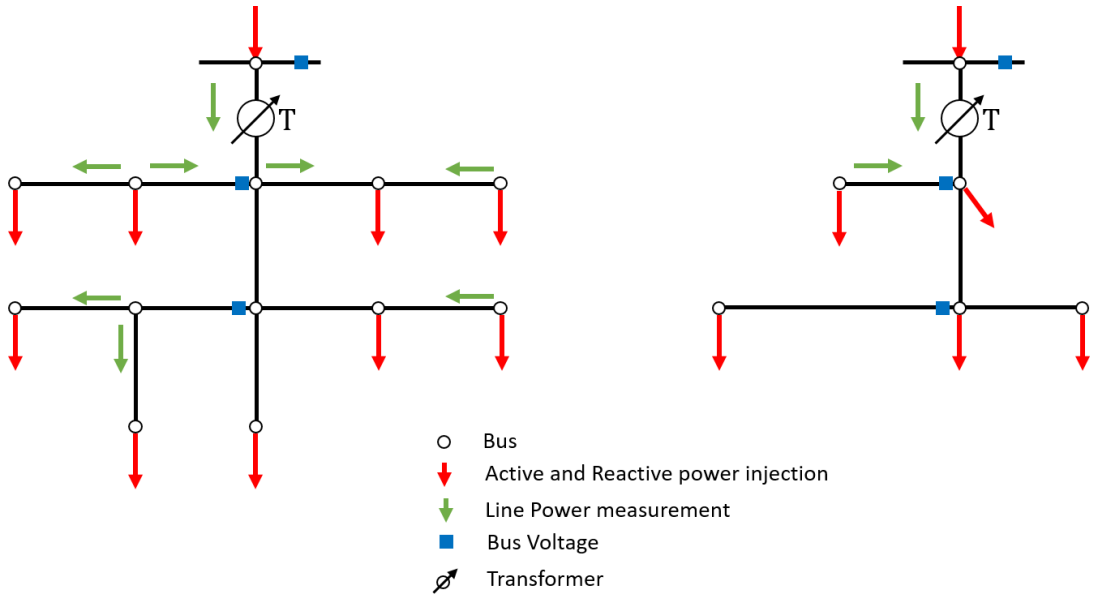


Figure 5.1: Conceptual depiction of reduction of measurements along a feeder.

The principal behind the reduction for SE is that current measurements can be treated in the same manner that injections are in chapter 2. In addition, the uncertainties of the measurements must be considered.

For end bus reduction, current measurements (I) and uncertainties (σ) can simply be aggregated to the nearest critical bus. This is described in (5.1) and (5.2)

$$I_{CB}^{new} = I_{CB}^{old} + I_{B_1} + ... + I_{B_N} \tag{5.1}$$

$$\sigma_{CB}^{new^{(2)}} = \sigma_{CB}^{old^{(2)}} + \sigma_{B_1}^{(2)} + ... + \sigma_{B_N}^{(2)} \tag{5.2}$$

where $B_{1...N}$ represents the set of downstream buses from the CB.

For middle bus reduction, we can write the current injection reduction to a neighboring bus as in terms of it's complex components

$$I_1^{new} = I_{1_d}^{new} + jI_{1_q}^{new} = (I_{1_d}^{old} + jI_{1_q}^{old}) + (R_{1_d} + jR_{1_q})(I_{2_d} + jI_{2_q}) \tag{5.3}$$

where $R_1 = z_{12}(z_{12} + z_{23})^{-1}$. Simplifying the equation and separating real and complex parts yields,

$$I_{1_d}^{new} = I_{1_d}^{old} + R_{1_d}I_{2_d} - R_{1_q}I_{2_q} \tag{5.4}$$

$$I_{1_q}^{new} = I_{1_q}^{old} + R_{1_q}I_{2_d} + R_{1_d}I_{2_q} \tag{5.5}$$

and the equivalent for uncertainty is found to be

$$\sigma_{1_d}^{new^{(2)}} = \sigma_{1_d}^{old^{(2)}} + R_{1_d}\sigma_{2_d}^{(2)} - R_{1_q}\sigma_{2_q}^{(2)} \tag{5.6}$$

$$\sigma_{1_q}^{new^{(2)}} = \sigma_{1_q}^{old^{(2)}} + R_{1_q}\sigma_{2_d}^{(2)} - R_{1_d}\sigma_{2_q}^{(2)} \tag{5.7}$$

as in 2.2.4, an equivalent form is derived for B_3.

Voltage measurements for buses that are to be removed could simply be discarded. However, greater redundancy in measurement is preferred by the state estimators, and thus

removing measurements is undesirable. To retain the information, we propose the use of a VDA approach as introduced in 4, where aggregated measurements are updated to reflect the voltage of the bus they are moved to.

In addition to state estimation, the circuit reduction has potential to benefit the optimal powerflow (OPF) solution speed and availability. The OPF problem is used to determine the optimal generation output for a circuit considering network constraints, present demand, and energy costs. The problem is an optimization built on top of a power balance equality powerflow model.

Network reduction has already been applied to aid the OPF problem in references [20, 41, 56]. However, as in traditional powerflow, these methods have focused on transmission type systems where the bulk of power is transacted. However, with decentralization of generation and the proliferation of microgrids, it will likely become necessary to run OPF for distribution side circuits.

The circuit reduction technique is an obvious choice to be extended to this problem. The format of keeping individual generators as introduced in 4.3.2 should be used. In addition, the VDA approach should be used to maintain voltage constraints through reduction. To this point, the author does not have a suggestion for maintaining line power constraints.

Appendix A

Voltage Sensitivity Modeling

A.1 Modeling node voltage versus load consumption

The use of voltage sensitivity and distribution factors for voltage prediction have been analyzed analytically in references [48, 50]. Here, a numerical approach for the feeder and methodology considered is given.

In Fig. A.1 the node with the largest voltage change in the circuit (node 1008) is analyzed. For this scenario, all loads are varied from no consumption to 2 times the rated loading and the change in node voltage is recorded. This is analyzed for three distinct load models.

Polynomials of order 1-3 are fit to the lines. The goodness of fit of these lines are represented using common statistical measures such as i) sum of squares due to error (SSE); ii) Coefficient of determination (r^2); iii) Root mean square error (RMSE) [57].

From both table A.1 and the figure, it is observed that load model effects the linearity of the change ion voltage with loading, where the constant impedance load model is the most linear and the constant power (P+jQ) is the most non-linear. Regardless, it is observed that for all load models the quadratic polynomial provides a high degree of fit.

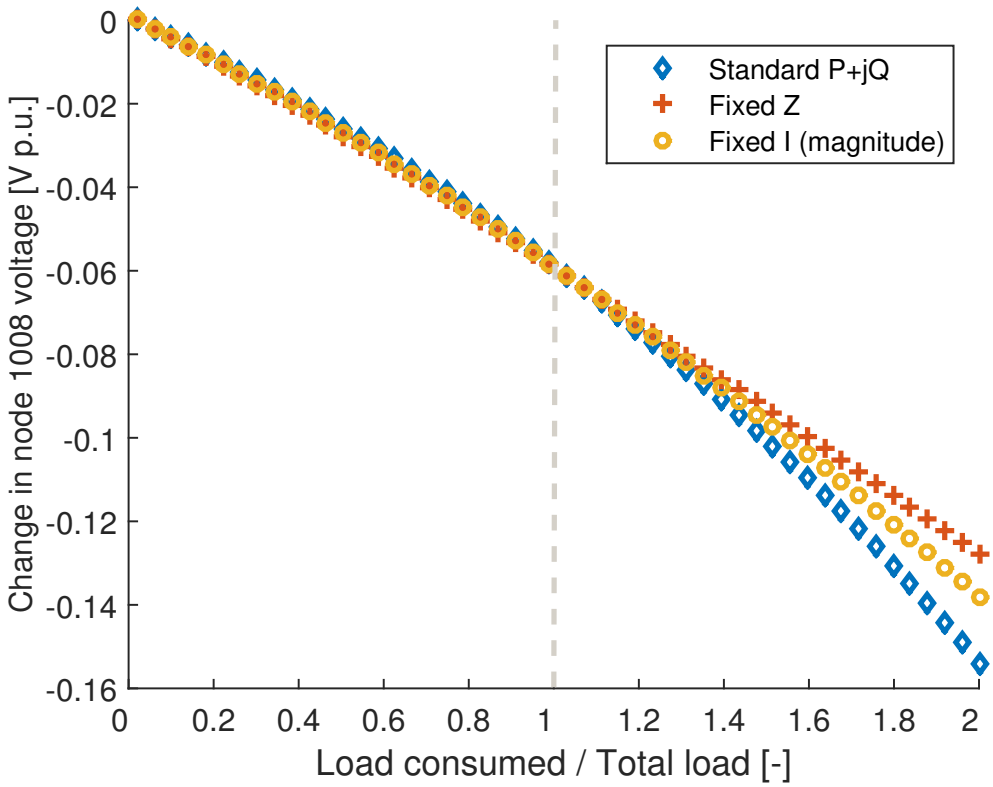


Figure A.1: The load change in node 1008 due to the change in total feeder loading. Three different load models are observed for each load: i) Constant power loads; ii) constant impedance loads; iii) Constant current magnitude loads.

Table A.1: Goodness of fit measures for increasing order of polynomial model fits to the change in voltage of node 1008 with respect to change in feeder loading (Fig A.1).

		P+JQ	Fixed Z	Fixed I
Linear	SSE	$1.4 * 10^{-3}$	$1.5 * 10^{-5}$	$4.7 * 10^{-7}$
	RMSE	$5.5 * 10^{-3}$	$5.6 * 10^{-4}$	$1.0 * 10^{-4}$
	r^2	.984	.999	.999
Quadratic	SSE	$7 * 10^{-5}$	$3.6 * 10^{-6}$	$1.3 * 10^{-8}$
	RMSE	$2.8 * 10^{-4}$	$2.75 * 10^{-4}$	$1.2 * 10^{-5}$
	r^2	.998	.999	.999
Cubic	SSE	$4.1 * 10^{-4}$	$2.4 * 10^{-7}$	$8.4 * 10^{-10}$
	RMSE	$2.9 * 10^{-3}$	$7.2 * 10^{-5}$	$4.3 * 10^{-6}$
	r^2	.995	.999	.999

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