UNIVERSITY OF CALIFORNIA SAN DIEGO

# VCO-based ADCs for Low Power Precision Sensor Interfaces

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Jiannan Huang

Committee in charge:

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2021

The dissertation of Jiannan Huang is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2021

DEDICATION

*To my family, friends, and the one and only Bear I love*

# EPIGRAPH

行到水穷处，坐看云起时。*/Where water ends, clouds rise.*

—王维（*Wang Wei)*

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ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor and mentor, Professor Patrick Mercier. After meeting with Prof. Mercier during the campus visit event back in 2016, I knew you and your group is the right place for me, even though I had other schools visits lining up. Without your support, this dissertation could never possibly be finished. Throughout this Ph.D. journey, I received not only technical support from you, but, more importantly, I learned valuable skills outside of circuit design. Your ability of explaining technical, abstract, and complex materials using accurate yet easy-to-grasp language is something I forever need to learn. You serve as a role model in my professional career. Thanks to you, I become not only better at circuit design, but also a more well-rounded person in general.

I would also like to extend my sincere gratitude to the other committee members, Prof. Gert Cauwenberghs, Prof. Chung-Kuan Cheng, Prof. Drew Hall, and Prof. Tze-Chien Hsueh for serving in my doctoral committee, and Prof. Prasad Gudem for participating in my Qualifying Exam, and Prof. Peter Asbeck for being in my Preliminary Exam.

I have had the honor of spending my time with many great talents in the Energy Efficient Microsystems group, who offered not only help, but shared joy and sorrow, and to whom I owe my thanks. In particular, I would like to express my thanks to Xiaoyang Wang, who is the first EEMS colleague I met. We shared many hardworking nights before tapeouts. I don't know about you, but I found your presence in the office a source of motivation for me. Your dedication and hardworking always motivate me. I'd also like to thank Hui Wang, Po-han Peter Wang, Dhongue Lee, Cooper Levy, Julian Warchall, Sally Safwat Amin, and Jiwoong Park, who were the "big brothers" to me and shared many useful advice and guidance when I first joined the group. It's also my honor to have these wonderful friends and colleagues who joined the group at about the same time as me: Nader Fathy, Hongsen Yang, Bao Huu Lam, Hossein Rahmanian, and Abdullah Abdulslam, Special thank is reserved for you, Nader, who has done an excellent job as the server admin and completely transformed our server into such a smooth and organized platform that is

so essential for our daily work. Also, it's exciting to see new blood joining the EEMS group and carry on the tradition of high volume ISSCC publications every year: Nevo Magnezi, Cihan Berk Gungor, Nikhil Harsha Maganti, Shihkai Kuo, Brian Liu, and Brian Lazaro Wuerstle.

The next-door BioEE group that is just a short walk from our office has shared some significant time during my Ph.D. journey as well. Specifically, I would like to thank Corentin Pochet who had many insightful technical discussions with me and is a really nice person to work with. Also, I owe my thank to Edwin Hsu who, despite being many years senior than me, is always willing to share his circuit insights and answer my questions. I enjoyed our friendship together. I should, of course, also thank my "lunch buddies" Da Ying, Xiahan Zhou, Haowei Jiang in the BioEE group. We had numerous lunches together at the Price Center with really bad food but good company. Overall, I enjoyed the casual conversations with you guys whenever I took a short walk to your office.

I would like to thank all other friends who I spent time with, especially my roommates and tennis buddies. They filled my Ph.D. life with joy and fun.

This acknowledgement is not complete without expressing my deepest gratitude to my family and girlfriend for their unyielding love, support, and encouragement, To my parents, Mingqi and Xiaomei: your steadfast faith in me has been a never-ending source of motivation, even though we are thousands of mile apart. My only regret is that you are unable to attend my commencement and witness my graduation because of the pandemic. To my beautiful girlfriend, Fan: you have been with me each and every step of the way in this journey. The last five years have been the best of my life because of you.

I dedicate this dissertation to my family and girlfriend for their forever love and support.

The material in this dissertation is based on the following papers which are either published or has been submitted for publication.

Chapter 1, in part, is based on Section I of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-

Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021, and Section I of the paper entitled "A 178.9-dB FoM 128-dB SFDR VCO-Based AFE for ExG Readouts with a Calibration-Free Differential Pulse Code Modulation Technique" submitted to the IEEE Journal of Solid-State Circuits. The dissertation author is the primary investigator and author of these papers.

Chapter 2, in part, is based on Section II of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021. The dissertation author is the primary investigator and author of this paper.

Chapter 3, in part, is based on Section II and Section III of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021. The dissertation author is the primary investigator and author of this paper.

Chapter 4, in part, is based on Section IV and Section V of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021. The dissertation author is the primary investigator and author of this paper.

Chapter 5, in part, is based on sections of the paper from Jiannan Huang, and Patrick P. Mercier, "A 178.9-dB FoM 128-dB SFDR VCO-Based AFE for ExG Readouts with a Calibration-Free Differential Pulse Code Modulation Technique" submitted to the IEEE Journal of Solid-State Circuits. The dissertation author is the primary investigator and author of the paper.

Chapter 6, in part, is based on the paper from Jiannan Huang, and Patrick P. Mercier, "A 94.2-dB SNDR 142.6-$\mu$W VCO-based Audio ADC with a Split-ADC Differential Pulse Code

Modulation Architecture" submitted to the IEEE Solid-State Circuits Letters. The dissertation author is the primary investigator and author of the paper.

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## PUBLICATIONS

**J. Huang**, P. P. Mercier, "A 178.9-dB FoM 128-dB SFDR VCO-Based AFE for ExG Readouts with a Calibration-Free Differential Pulse Code Modulation Technique", *Journal of Solid-State Circuits (JSSC)*, Submitted.

**J. Huang**, P. P. Mercier, "A 94.2-dB SNDR 142.6-$\mu$W VCO-based Audio ADC with a Split-ADC Differential Pulse Code Modulation Architecture", *Solid-State Circuits Letter (SSCL)*, Submitted.

**J. Huang**, P. P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation", *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 56, no. 4, pp. 1046-1057, Apr. 2021.

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C. Pochet, **J. Huang**, P. P. Mercier, D. A. Hall, "A 400-mVpp, 92.3 dB-SNDR, 1kHz-BW, 2nd-order VCO-based ExG-to-Digital Front-End Using a Multiphase Gated-Inverted Ring-Oscillator Quantizer", in Proc. *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021.

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ABSTRACT OF THE DISSERTATION

**VCO-based ADCs for Low Power Precision Sensor Interfaces**

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2021

Professor Patrick P. Mercier, Chair

VCO-based ADCs has long existed as an alternative way of digitization of analog signal. Thanks to its time-domain operation, VCO-based structures using phase domain signal processing have become very promising in highly scaled CMOS processes. The general idea is that since voltage-domain quantization is increasingly difficult to do well in scaled CMOS processes with low supply voltages, it is potentially a better idea to exploit what scaled CMOS processes are very good at: having lots of small transistors that switch fast. Thus, translating input voltage variations to a corresponding phase/frequency variation puts information into the time domain, which can be easily quantized via simple digital circuitry. On the other hand, one well known issue of VCOs is the non-linear voltage-to-frequency transfer characteristic, particularly when

input amplitude is large. The distorted frequency output ultimately translates to a distorted digital output, which limits the maximal achievable spurious free dynamic range of the ADC.

This dissertation presents a new architecture for VCO-based ADCs called differential pulse code modulation (DPCM) that virtually eliminates the VCO V-to-F nonlinearity by substantially reducing the signal amplitude that the VCO sees so that the VCO operates in the small signal linear region. By using this technique along with other calibration and circuit schemes, three prototype ICs (in which two are for bio-signal and one for audio signal) were fabricated and measured. They all achieved significantly better linearity not only amongst VCO-based ADCs, but also free of any measurable distortions in the output spectra, thus enabling a virtually distortion-less VCO-based ADCs suitable for high dynamic range precision sensing applications.

# Chapter 1

# Introduction

## 1.1 Motivation for VCO-based ADCs in Sensing Applications

As health care and Internet-of-Things (IoT) industries continue to grow, there is an increasing demand for advanced sensor interfaces in a broad range of applications such as wearable devices, autonomous vehicles, environmental monitors, and beyond. Ultimately, the underlying electronics for sensor interfaces play an important role in determining the overall system performance. Specifically, the analog front-end (AFE) which is responsible for signal conditioning and sometimes also digitization is a key design block that often dominates metrics such as noise and power of the system. More importantly, pragmatic adoption of sensor devices requires the AFE to handle input artifacts resulting from motion, electrode offsets, and so on. As a result, these requirement presents the following challenges for AFEs used in sensing applications:

1) *Low Power:* Since most such devices are battery-powered, the AFE must consume very little power, especially when potentially large arrays of sensors are integrated into a single device.

2) *Low Noise:* As the first stage in the signal acquisition chain, the AFE itself must have low input-referred noise (in the $\mu$V range) to ensure high signal-to-noise ratio (SNR).

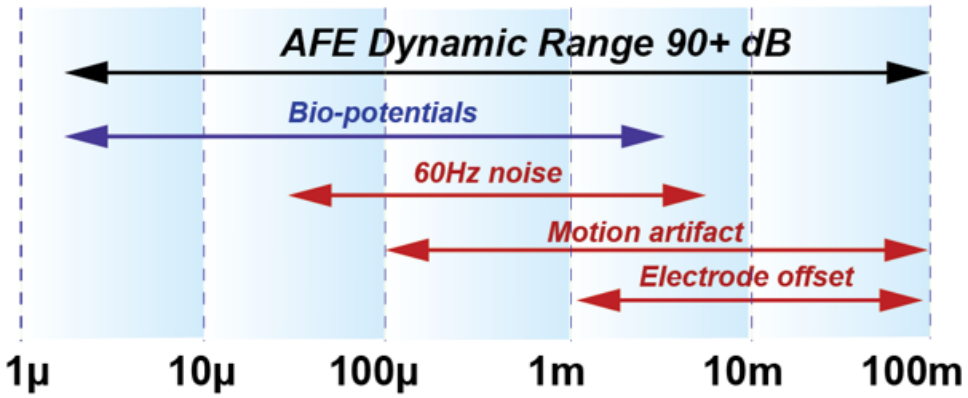



**Figure 1.1**: High dynamic range requirement due to the presence of artifacts.

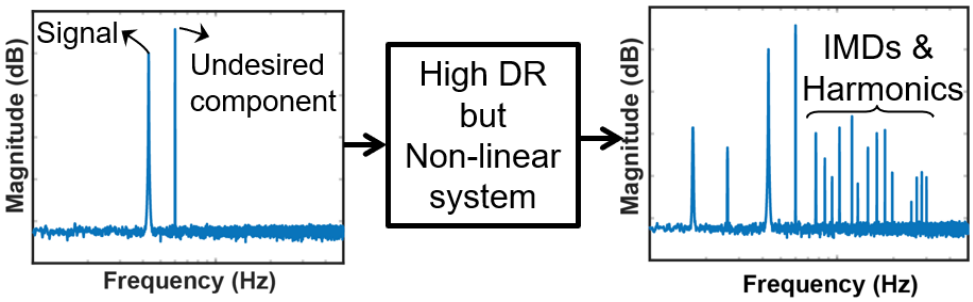
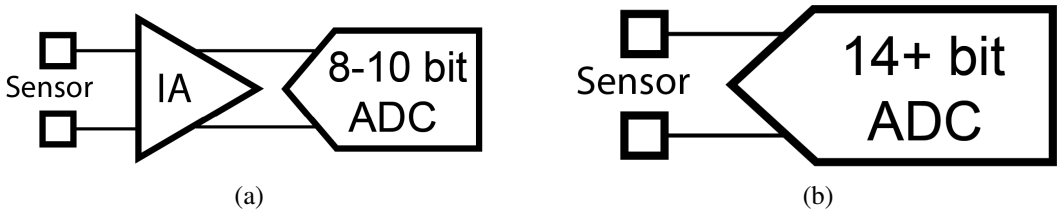



**Figure 1.2**: Signal and undesired component passing through a high DR but non-linear system.

3) *High Input Impedance:* The AFE needs to have a high input impedance so that the signal is not attenuated due to voltage division with the sensor's source (e.g., electrode) impedance.

4) *Wide Dynamic Range (DR):* As shown in Fig. 1.1, even though the signal of interest such as bio-potentials may have a small amplitude up to a few mV, undesired components such as motion and stimulation artifacts can easily reach 100s of mV, pushing the overall DR of the AFE beyond 90 dB to avoid saturation.

5) *High Linearity:* While high DR enables capturing the signal in the presence of undesired components without saturating the AFE, non-linearity results in lots of inter-modulation distortions (IMD) and harmonics, as illustrated in Fig. 1.2. This creates difficulty in post-processing the output to filter out undesired components. On the other hand, for a highly linear design, simple post-processing (such as low pass filtering or notch filtering) can be




(a) (b)

**Figure 1.3**: High level block diagram of (a) traditional IA + ADC structure, and (b) ADC-direct structure.

applied to easily remove the unwanted components because there is little inter-modulation products or higher order harmonics thanks to the low total harmonic distortion (THD).

The traditional AFE design approach involves a dedicated instrumentation amplifier (IA) followed by a medium resolution analog-to-digital converter (ADC), as shown in Fig. 1.3(a). The IA needs to have a high-pass characteristic with sub-1 Hz cutoff [2] to filter out low frequency artifacts. This results in a relaxed DR requirement for the subsequent ADC thanks to the removal of artifacts and the gain of the amplifier. However, the overall DR of this approach is still limited because the IA can be saturated when artifacts move in band. Therefore, to cancel large in-band artifact and to achieve sub-1 Hz high-pass cutoff, it often requires feedback using large area-consuming capacitors [3, 4] and sometimes even off-chip components [5, 6]. This severely limits the usefulness of this approach in today's miniaturized and high-density sensor interfaces. To address the area issue and to increase the DR, recent designs have proposed the use of a mixed-signal DC servo loop to cancel in-band artifacts and to create the ultra-low high-pass cutoff in the digital domain [7–9]. Albeit effective in reducing area, the power consumption of this structure at the system level remains high due to the separation of the gain stage and conversion stage.

On the other hand, more recently the literature has seen adoption of the so called ADC-direct structure as shown in Fig. 1.3(b) where the IA and ADC are combined to form a single high-resolution ADC responsible for digitizing all signal components, including artifacts. By utilizing quantization noise shaping and oversampling techniques well established in the ADC

community, very high DR can be achieved [10–22] to cover the full range in Fig. 1.1. Yet, unlike standard high resolution ADCs, ADC-direct AFEs have special requirements: they must continue to support a high input impedance to enable direct coupling to small electrodes (or other applications where instrumentation amplifiers are required), and they must feature a low input-referred noise (IRN) - ideally down to the $\mu$V level. Nevertheless, thanks to the highly integrated nature, this topology often offers the best trade-off among noise, power, area, and DR. However, the challenge with existing ADC-direct AFEs is that they rely heavily on voltage domain building blocks such as amplifiers and integrators, which suffers from headroom issues as the supply voltage continues to reduce in scaled processes, where it is desired to integrate all functionality, including the AFE, in a single SoC. Moreover, large area-consuming capacitors are often needed to either suppress the $kT/C$ sampling noise in discrete-time (DT) implementations or maintain the linearity of Gm-C filter in continuous-time (CT) cases [23].

As an alternative, to further exploit the benefits of scaled CMOS process, time-domain variants have become very promising, since they potentially offer a mostly digital architecture that overcomes the reduced intrinsic gain and voltage headroom issues found in voltage-domain counterparts. Specifically, VCO-based structures using phase domain signal processing have become very promising in implementing next-generation sensor interfaces. The general idea is that since voltage-domain quantization is increasingly difficult to do well in scaled CMOS processes with low supply voltages, it is potentially a better idea to exploit what scaled CMOS processes are very good at: having lots of small transistors that switch fast. Thus, translating input voltage variations to a corresponding phase/frequency variation puts information into the time domain, which can be easily quantized via simple digital circuitry.

In addition, VCO-based quantizers can be shown to be mathematically equivalent to a $1^{st}$ order $\Delta\Sigma$ modulator [24]. Therefore, it is possible to achieve a very high signal-to-quantization-noise ratio (SQNR). However, VCOs also have their own design challenges, as is illustrated in the following section.

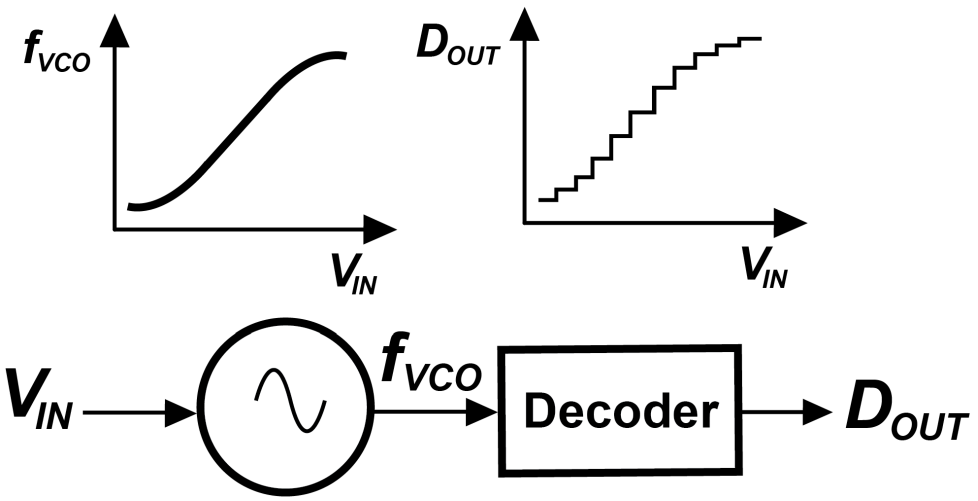



**Figure 1.4**: High level illustration of the VCO-based quantizer exhibiting nonlinear voltage-to-frequency conversion.

## 1.2 Challenges and Existing Solutions

On the other hand, one well known issue of VCOs is the non-linear voltage to frequency (V-to-F) transfer characteristic, particularly when input amplitude is large, as illustrated in Fig. 1.4. The distorted frequency output, $f_{\mathrm{VCO}}$, ultimately translates to a distorted digital output, $D_{\mathrm{OUT}}$, which limits the maximal achievable spurious free dynamic range (SFDR) of the ADC and can become a problem for sensor applications requiring high linearity. Even in the linear input range, the slope (i.e., $K_{\mathrm{VCO}}$) can be very sensitive to process, voltage, and temperature (PVT) variations.

To overcome the above issues, various designs have been proposed in the past [25–28]. In [25], the authors reported a simple open-loop VCO-based sensor readout circuit that achieves a good noise and power performance. But the open-loop structure limits the usable input amplitude to a few milli-volts due to the nonlinear V-F conversion. To address this, [26] adopts digital calibrations to correct for the non-linearity. However, the foreground calibration will interrupt the normal operation of the AFE and does not track temperature drift and supply variations. In [27, 29], the VCO quantizer is embedded in a $2^{\mathrm{nd}}$ order $\Delta\Sigma$ loop, thus improving linearity by reducing the signal swing at the VCO input. Albeit successful in reducing VCO non-linearity, such

architectures inevitably contain other conventional voltage-domain building blocks to achieve the $2^{nd}$-order noise shaping, which defeats the purpose of employing VCOs in the first place. In [28], the authors reported a hybrid PLL-$\Delta\Sigma$ sensor front-end by leveraging the similarities between a conventional analog PLL and a $2^{nd}$ order $\Delta\Sigma$ ADC with VCO quantizer. Though high dynamic range and low power are achieved, the AFE suffers from a low input impedance of 222 k$\Omega$, which makes it unsuitable for many sensing applications.

As can be seen from the existing VCO-based designs, none of them are able to simultaneously meet the demands presented by the challenges listed in Section 1.1, while fully exploiting the phase-domain advantages offered by highly-scaled CMOS process technology.

## 1.3 Dissertation Overview

This dissertation presents a new circuit architecture for VCO-based ADCs that enables a virtually distortion-less output spectrum. Architecture description, circuit analysis. and measurement results are given for three prototype VCO-based ADCs. The dissertation consists of seven chapters.

Towards a distortion-less VCO-based ADC, chapter 2 describes the proposed differential pulse code modulation (DPCM) architecture utilized to improve VCO V-to-F linearity. To overcome $K_{VCO}$ variation, a background gain calibration is described in Chapter 3. Based on the DPCM architecture and gain calibration, a VCO-based ADC targeting ExG wearable sensing application is presented in Chapter 4. To further improve power efficiency, Chapter 5 covers a calibration-free DPCM architecture which significantly relaxes digital power consumption while offering a virtually distortion-less output spectrum. A discussion of precision sensing application is not complete without the inclusion of audio band. Chapter 6 extends the DPCM concept to the audio band and presents a VCO-based audio ADC. Finally, concluding remarks are given in Chapter 7 along with areas of future research.

Chapter 1, in part, is based on Section I of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021, and Section I of the paper from Jiannan Huang, and Patrick P. Mercier, "A 178.9-dB FoM 128-dB SFDR VCO-Based AFE for ExG Readouts with a Calibration-Free Differential Pulse Code Modulation Technique" submitted to the IEEE Journal of Solid-State Circuits. The dissertation author is the primary investigator and author of these papers.

# Chapter 2

# Improving Linearity with Differential Pulse Code Modulation

This chapter will build-up to the eventual final DPCM architecture by first reviewing the operation of a basic open-loop VCO-based quantizer, then introducing the DPCM concept, and finally describing several modifications to the DPCM architecture to ease circuit design constraints and provide robustness against supply variation.

## 2.1 Basic Open-Loop VCO-Based Quantizer

The basic VCO-based quantizer is the open loop structure shown in Fig. 2.1. It consists of a VCO whose output frequency is ideally proportional to the input voltage, $V_{\mathrm{IN}}$. Since phase is the integral of frequency, a phase ramp, $\phi(t)$, is also generated with its slope being the instantaneous frequency. $\phi(t)$ is then sampled to obtain the phase samples, $\phi[n]$, which subsequently are quantized by a phase quantizer to get $\phi_d[n]$. Finally, a $1^{\mathrm{st}}$ order difference circuit takes the difference between two successive $\phi_d[n]$ to obtain the output, $D_{\mathrm{OUT}}[n]$, which is a digital representation the average frequency (therefore also the input voltage) within one

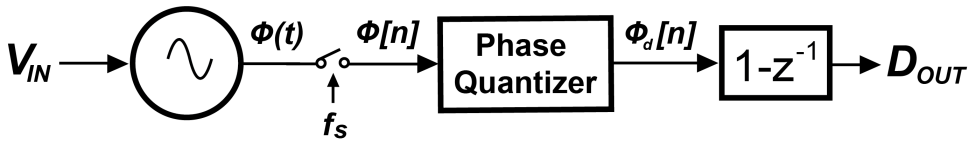



**Figure 2.1**: Conceptual block diagram of the basic open loop VCO quantizer.

sampling period.

To see why there is a 1st order quantization noise shaping, we note that the quantized phase samples, $\phi_d[n]$, can be expressed as:

$$\phi_d[n] = \phi[n] + e_q[n], \tag{2.1}$$

where $e_q[n]$ represents the quantization error associated with the quantized phase sample $\phi_d[n]$. Since $D_{\mathrm{OUT}}[n]$ is the difference of successive $\phi_d[n]$, we can express $D_{\mathrm{OUT}}[n]$ as follows by plugging in (2.1):

$$\begin{aligned} D_{\mathrm{OUT}}[n] &= \phi_d[n] - \phi_d[n-1] \\ &= \phi[n] - \phi[n-1] + (e_q[n] - e_q[n-1]) \\ &= G_{\mathrm{ADC}}\overline{V_{\mathrm{IN}}} + (e_q[n] - e_q[n-1]), \end{aligned} \tag{2.2}$$

where $G_{\mathrm{ADC}}$ is the signal gain from input voltage to digital output and $\overline{V_{\mathrm{IN}}}$ is the average input voltage within one sampling period. From (2.2), indeed the 1st order quantization noise shaping can be observed since the input signal passes through linearly, while the quantization error is temporally subtracted.

It is instructive to derive an expression for the ADC gain, $G_{\mathrm{ADC}}$, which depends on the actual implementation of the VCO quantizer. One simple implementation with decent linearity is shown in Fig. 6.5. This circuit consists of an input V/I converter driving a current-starved ring oscillator followed by a counter-based phase decoder. The phase decoder is composed

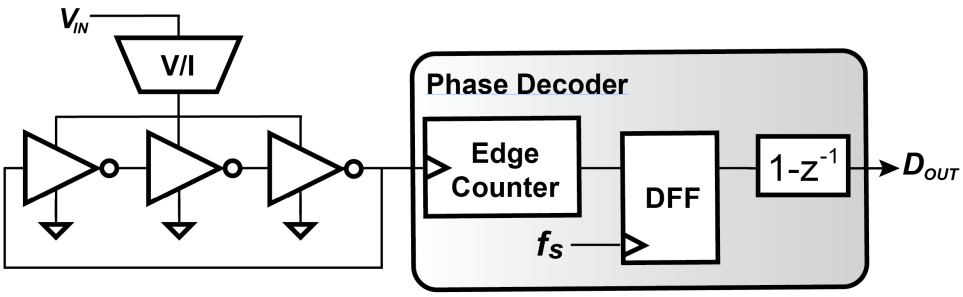



**Figure 2.2**: A simple implementation of the basic VCO quantizer.

of an edge counter clocked by one stage output of the ring. Therefore, the counter output represents a quantized version of the instantaneous phase, $\phi(t)$. The remaining D flip-flop (DFF) and $1-z^{-1}$ block perform sampling and differencing operation, respectively, to obtain $D_{\mathrm{OUT}}$. Equivalently, $D_{\mathrm{OUT}}$ can be viewed as counting the number of VCO edges within one sampling period. Therefore, it can be expressed as:

$$\begin{aligned} D_{\mathrm{OUT}} &= f_{\mathrm{VCO}}/f_s \\ &= K_{\mathrm{VCO}}V_{\mathrm{IN}}/f_s, \end{aligned} \tag{2.3}$$

where $f_{\mathrm{VCO}}$ is the output frequency of the VCO, and $K_{\mathrm{VCO}}$ is the VCO tuning gain. It follows that

$$G_{\mathrm{ADC}} = \frac{D_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{K_{\mathrm{VCO}}}{f_s}. \tag{2.4}$$

For a current-starved inverter ring with $N$ stages and load capacitance $C_{\mathrm{load}}$ at each stage, $K_{\mathrm{VCO}}$ can be shown to be [25]:

$$K_{\mathrm{VCO}} = \frac{G_m}{NC_{\mathrm{load}}V_{\mathrm{swing}}}, \tag{2.5}$$

where $G_m$ is the transconductance of the V/I, and $V_{\mathrm{swing}}$ is the output swing.

It is also of interest to derive the SQNR for this basic VCO-based quantizer. For an input

sinusoid with amplitude $A$, the SQNR is given by [25]

$$\text{SQNR} = 9A^2 \left(\frac{N}{\pi} K_{\text{VCO}}\right)^2 \frac{f_s}{f_B^3} \tag{2.6}$$

$$= 9A^2 \left(\frac{G_m}{\pi C_{\text{load}} V_{\text{swing}}}\right)^2 \frac{f_s}{f_B^3}, \tag{2.7}$$

where $f_B$ is the signal bandwidth. The intuition behind (2.7) is that SQNR is directly related to how fast the VCO can push edges through inverters. As CMOS process continues to scale, both $C_{\text{load}}$ and $V_{\text{swing}}$ reduce, thereby increasing SQNR. This shows a clear advantage for VCO-based quantizers in today's deep sub-micron CMOS process.

Furthermore, using the VCO circuit parameters ($N = 3$, $K_{\text{VCO}} = 120$ MHz/V, $f_s = 32$ kHz and $f_B = 500$ Hz) presented in Chapter 4, the achievable SQNR with an input amplitude $A = 100$ mV is calculated to be 115 dB according to (2.6). This shows that even a simple implementation with only 1$^{\text{st}}$ order noise shaping and moderate oversampling ratio (OSR) can provide sufficient SQNR.

In practice, however, VCOs exhibit significant V-to-F distortion at large input amplitudes. Also, $K_{\text{VCO}}$ can be very sensitive to process, voltage, and temperature (PVT) variations. To address these issues, this work improves upon the basic open-loop structure by applying the DPCM theory to achieve high linearity and adopts background gain calibration to eliminate the effect of $K_{\text{VCO}}$ variations.

## 2.2 Differential Pulse Code Modulation

DPCM is a waveform coding technique in the field of compression theory widely used to reduce the data rate in, for example, transmitting speech or video signals. Figure 2.3 shows a conceptual block diagram of DPCM. The predictor is designed to exploit the correlation between adjacent samples of input signal, so that the quantizer only need to process a small prediction error,

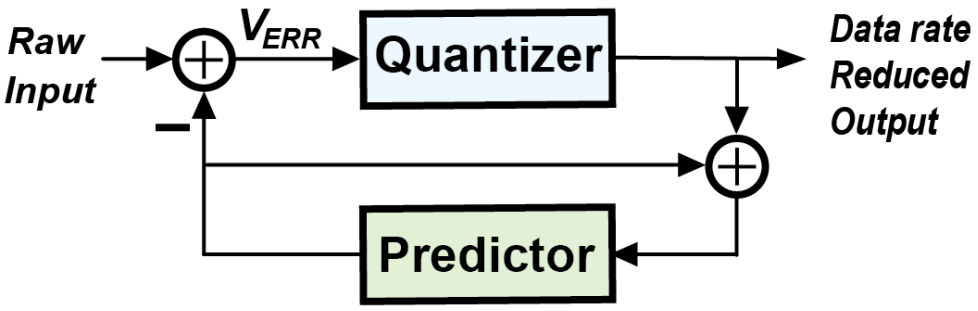



**Figure 2.3**: Conceptual block diagram of DPCM.

$V_{\mathrm{ERR}}$. In conventional DPCM implementations, this allows the output data rate to be significantly reduced.

Inspired by this concept, we apply DPCM to the basic open-loop VCO quantizer from Fig. 6.5 by wrapping it inside the DPCM configuration, as shown in Fig. 2.4(a). To maintain proper signal conversions, a DAC is inserted in the feedback path. The key idea behind this is to reduce VCO non-linearity by substantially lowering the signal swing that the VCO sees through DPCM. Specifically, oversampling increases the correlation between successive input samples. This allows the predictor to make better predictions, which in turn leads to a smaller prediction error reaching the VCO [14, 30]. As a result, the V-to-F conversion of the VCO becomes very linear thanks to the small swing.

To gain more insights of the architecture and to quantify the swing reduction, it is useful to understand its discrete-time model shown in Fig. 2.4(b). where $P$ is the transfer function of the predictor. It is obtained by replacing the VCO quantizer and DAC with gain blocks and delays. Although the VCO quantizer is represented only as a gain block, $G_{\mathrm{ADC}}$, for simplicity, we should still keep in mind that it has inherent $1^{\mathrm{st}}$ order quantization noise shaping embedded in it. Note that there are two paths $P_1$ (in orange) and $P_2$ (in purple) in this block diagram. The path gains

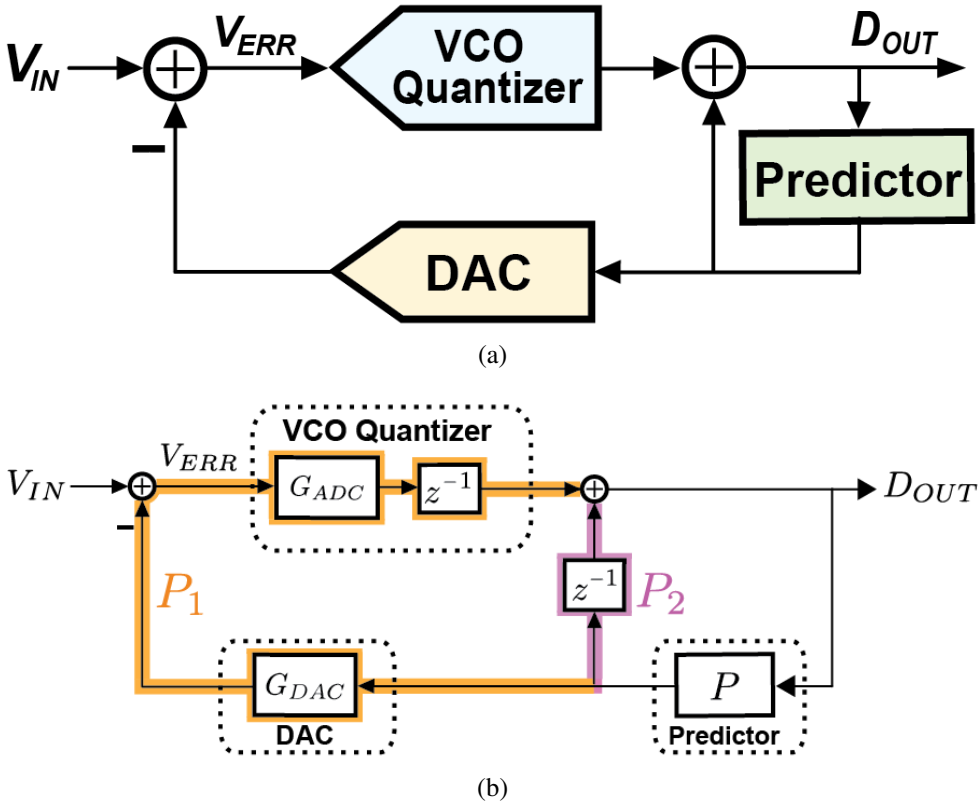



**Figure 2.4**: (a) VCO-based ADC implementation of DPCM, and (b) the corresponding discrete-time model.

can be expressed as

$$P_1 = -G_{\mathrm{ADC}} G_{\mathrm{DAC}} z^{-1}, \tag{2.8}$$

$$P_2 = z^{-1}, \tag{2.9}$$

For the moment, let us assume that the path gain magnitudes of the two paths are equal ($|P_1| = |P_2|$). It follows that

$$G_{\mathrm{ADC}} G_{\mathrm{DAC}} = 1. \tag{2.10}$$

Ensuring equality between these two path gain magnitudes will be important momentarily.

There are two transfer functions worth a detailed look before proceeding to the eventual

final circuit architecture. The first is from $V_{\text{IN}}$ to $D_{\text{OUT}}$. From Mason's gain formula, we have

$$\frac{D_{\text{OUT}}}{V_{\text{IN}}} = \frac{G_{\text{ADC}}z^{-1}}{1+Pz^{-1}(G_{\text{ADC}}G_{\text{DAC}}-1)} \tag{2.11}$$

$$= G_{\text{ADC}}z^{-1}, \tag{2.12}$$

where (2.12) eliminates the denominator in (2.11) by substitution of the aforementioned equality in (2.10). The result is just the undisturbed VCO quantizer gain. In other words, it is as if the two paths cancel and no feedback exists, so that $V_{\text{IN}}$ goes through undisturbed to the output (again, with 1$^{\text{st}}$ order noise shaping still intact).

Another transfer function that deserves closer attention is from $V_{\text{IN}}$ to $V_{\text{ERR}}$, which relates the overall system input to the VCO input. The transfer function is given by

$$\frac{V_{\text{ERR}}}{V_{\text{IN}}} = \frac{1-G_{\text{ADC}}G_{\text{DAC}}Pz^{-1}}{1+Pz^{-1}(G_{\text{ADC}}G_{\text{DAC}}-1)} \tag{2.13}$$

$$= 1-Pz^{-1}, \tag{2.14}$$

where, again, the equal path gain magnitude assumption greatly simplifies the expression. Depending on how the predictor is designed, we can obtain different expressions for the transfer function. If $P$ is simply unity, then we get $1-z^{-1}$, a 1$^{\text{st}}$ order high-pass. If, instead, $P = 2-z^{-1}$, the transfer function becomes

$$\frac{V_{\text{ERR}}}{V_{\text{IN}}} = 1-\left(2-z^{-1}\right)z^{-1}$$

$$= \left(1-z^{-1}\right)^2, \tag{2.15}$$

which is a 2$^{\text{nd}}$ order high-pass response of the input signal to the input of the VCO quantizer. For a system with 32x OSR, such a transfer function provides at least 40 dB attenuation in the signal band, as shown in Fig. 2.5. This mathematically shows that the DPCM technique substantially

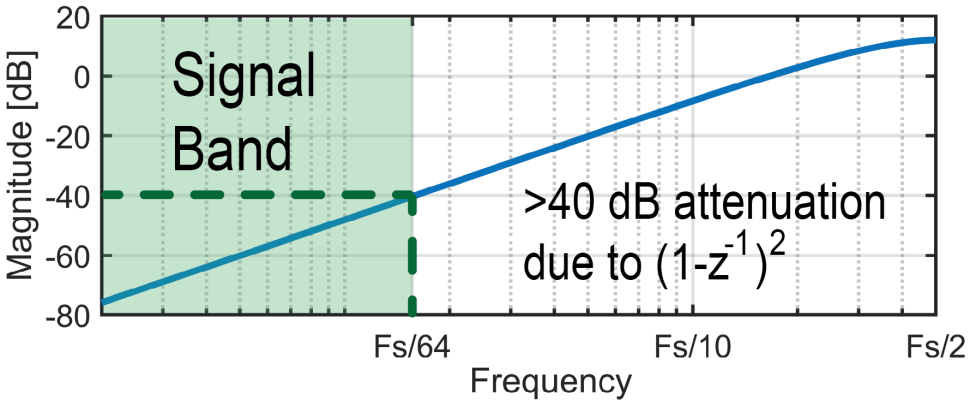



**Figure 2.5**: Magnitude plot of the $(1-z^{-1})^2$ high-pass response showing at least 40 dB attenuation in the signal band for a system with 32x OSR.

reduces the swing that the VCO sees by at least 40 dB, thereby maximizing linearity through feedback. To avoid confusion with the noise transfer function (NTF) of a 2nd order ΔΣ modulator, which also has the form $\left(1-z^{-1}\right)^2$, it should be noted that the 2nd order high-pass in this context is NOT used to shape quantization noise, but instead to shape the signal incident to the VCO so that it has low swing. The overall ADC remains a 1st order quantization noise shaped system, with the noise shaping occurring due to the VCO quantizer.

## 2.3 Feedback Path Considerations

With the feed-forward path (i.e., VCO quantizer) design greatly relaxed by DPCM, let us seek an architectural approach to also relax the feedback path, specifically the DAC, since its linearity directly impacts the system's linearity, similar to the case in ΔΣMs [31]. It turns out that with little modification on the architecture, the DAC resolution requirement can be relaxed. This is accomplished by introducing truncators as shown in Fig. 2.6, where a digital right-shifter (RS) is inserted before the DAC so its input bit-width is directly reduced by β. Another left-shifter (LS) of the same shifting amount, β, is also inserted to restore the loop dynamics. Of course, truncation error $E_T$ is introduced. To find out if $E_T$ adds noise to the system output, $D_{\mathrm{OUT}}$, it is worth noting that $E_T$ travels along the two paths $P_1$ and $P_2$ before summing to reach $D_{\mathrm{OUT}}$. Recall

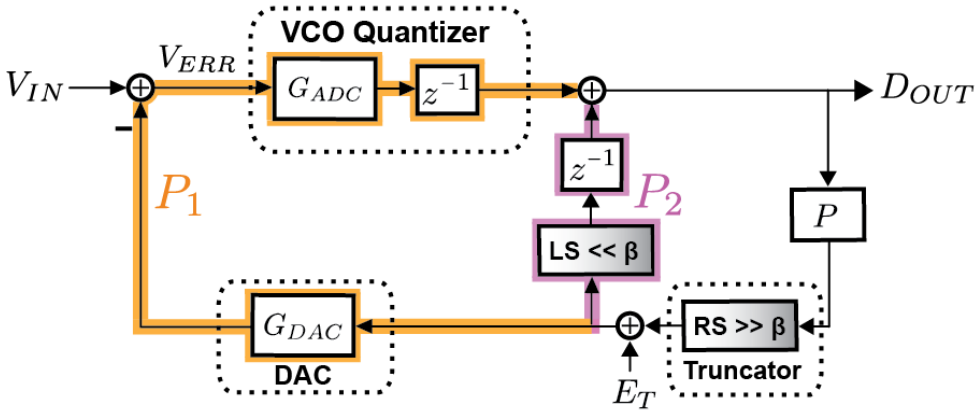



**Figure 2.6**: Insertion of digital truncators in the DPCM architecture to reduce DAC resolution requirement.

our assumption of $|P_1| = |P_2|$. With the insertion of truncators, we need to modify (2.10) to be

$$G_{\text{ADC}}G_{\text{DAC}} = 2^{\beta} \tag{2.16}$$

such that $|P_1| = |P_2|$ is satisfied. In this case, the two paths have equal magnitude but opposite signs. Therefore, $E_T$ is cancelled at $D_{\text{OUT}}$, and does not negatively impact the system. The drawback of this approach is that it increases the step size of the DAC, which means a higher swing for $V_{\text{ERR}}$. This imposes an upper limit on β.

Chapter 2, in part, is based on Section II of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021. The dissertation author is the primary investigator and author of this paper.

# Chapter 3

# VCO Gain Calibration

## 3.1 Background Calibration

So far, we have seen the various benefits brought by the application of DPCM in the VCO-based AFE. There is, however, one key question that remains unanswered: how to make $|P_1| = |P_2|$, especially across PVT variation? To answer this, for the purpose of better understanding, we refer back to the original discrete-time model without shifters in Fig. 2.4(b). In this case, it can be shown that (2.10) needs to hold to ensure $|P_1| = |P_2|$. In practice, however, the gain product, $G_{\mathrm{ADC}}G_{\mathrm{DAC}}$, may deviate from unity. The solution is to add a gain error correction (GEC) logic, which is tasked with continuously tracking and correcting the gain. At a high level, it works by first finding an estimate, $\hat{G}$, for the gain product, $G_{\mathrm{ADC}}G_{\mathrm{DAC}}$. Then the gain product is normalized by $\hat{G}$ to make it unity.

As shown in Fig. 3.1, the GEC is added right after the VCO quantizer. Since the GEC uses a dither-based calibration approach [24, 32, 33], a linear feedback shifter register (LFSR) is used to generate a two level ($\pm 1$) random sequence, $d$, with zero mean. The GEC works as follows. To start with, $d$ is injected into the DAC and the GEC. As a result, the GEC input, $u$, can

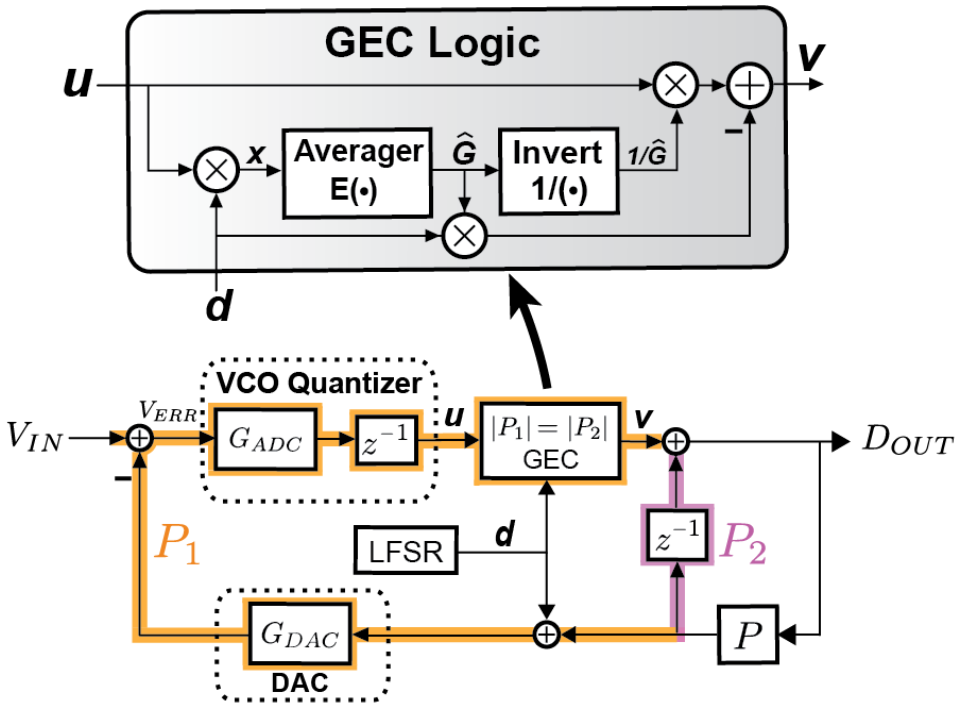



**Figure 3.1**: Block diagram of the gain error correction logic to ensure $G_{\text{ADC}}G_{\text{DAC}} = 1$.

be expressed as

$$u = G_{\text{ADC}}G_{\text{DAC}} \cdot d + c, \tag{3.1}$$

where $c$ is a term that lumps all components uncorrelated with $d$. The next step is to perform correlation, which is nothing but the multiplication between $u$ and $d$. Noting that $d^2 = 1$, we have the result $x$ given by

$$\begin{aligned} x &= u \cdot d \\ &= G_{\text{ADC}}G_{\text{DAC}} \cdot d^2 + c \cdot d \\ &= G_{\text{ADC}}G_{\text{DAC}} + c \cdot d. \end{aligned} \tag{3.2}$$

Next, we pass $x$ to an averager to find its average, $\text{E}[x]$. Since $c$ represents terms uncorrelated with $d$, the product, $c \cdot d$, on average is zero. Therefore, $\text{E}[x]$ serves as the estimate for

$G_{\mathrm{ADC}}G_{\mathrm{DAC}}$. This is shown by equations as follows

$$\begin{aligned} \mathrm{E}[x] &= \mathrm{E}[G_{\mathrm{ADC}}G_{\mathrm{DAC}}] + \mathrm{E}[c \cdot d] \\ &= \mathrm{E}[G_{\mathrm{ADC}}G_{\mathrm{DAC}}] = \hat{G}. \end{aligned} \tag{3.3}$$

After obtaining the gain estimate, $\hat{G}$, for $G_{\mathrm{ADC}}G_{\mathrm{DAC}}$, we normalize $u$ by first inverting $\hat{G}$ and then multiplying by the reciprocal. Finally, $d$ is subtracted from the normalized $u$ to obtain a gain-calibrated and dither-free output, $v$.

The dither-based gain calibration approach enables continuous tracking and correcting of $G_{\mathrm{ADC}}G_{\mathrm{DAC}}$ so that the assumption of $|P_1| = |P_2|$ is satisfied. Moreover, GEC is all digital with background operation so that the AFE remains functional during calibration.

## 3.2 Recursive Implementation

Though the GEC can be implemented according to the block diagram in Fig. 3.1, there are two practical difficulties: 1) the averager needs to average approximately one million samples to effectively cancel components uncorrelated with $d$, which means an enormous amount of storage elements; 2) the inversion to find reciprocal involves a division operation, which can be hardware expensive.

To address these concerns, the GEC is implemented in a recursive manner as shown in Fig. 3.2. The averager is replaced by a least-mean-square (LMS) engine from adaptive filter theory [34] to perform gain estimation. At the core of the LMS engine is the following recursive equation:

$$G[n+1] = G[n] + \mu d[n]\left(u - d[n]G[n]\right), \tag{3.4}$$

where $\mu$ is a scaling factor, and $G$ is recursively updated according to (3.4) and eventually

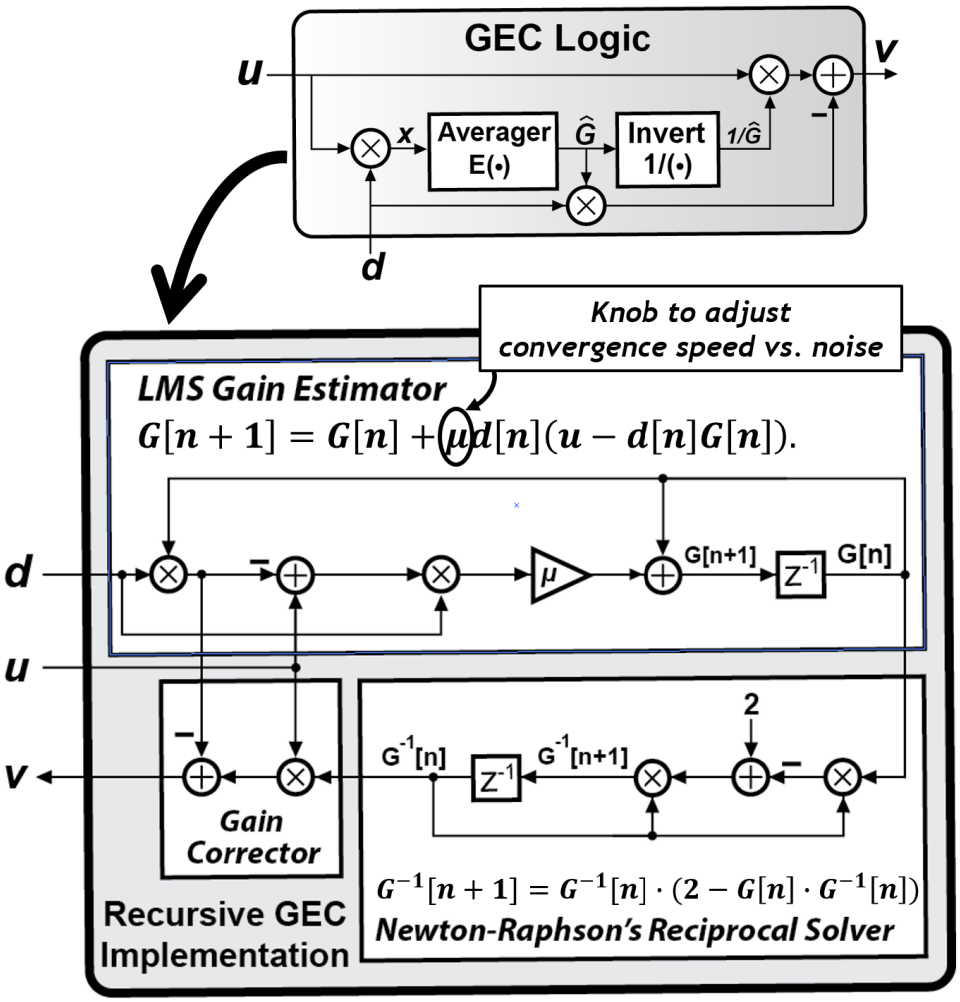



**Figure 3.2**: Recursive implementation of the GEC logic.

converges to $\hat{G}$. To have an intuitive understanding without too much maths in adaptive filter theory, note that $u - d[n]G[n]$ represents terms uncorrelated with $d$. Hence, the product (or correlation) $d[n] \cdot (u - d[n]G[n])$ will in average become zero as $G[n]$ approaches the actual gain to be estimated. Since $G[n]$ is also updated by $d[n](u - d[n]G[n])$ at every recursion to obtain the next $G[n+1]$, (3.4) has the tendency to converge and stay around the actual gain.

$\mu$ controls the update step size and serves as a knob to trade off between convergence speed and the amount of fluctuation (noise) when converged. Compared to the original averager implementation, the hardware cost for the LMS engine is very minimal. There is no need for

massive storage components, and the two multiplications in Fig. 3.2 can be reduced to sign flippers because they both involve $d$, which is just $\pm 1$.

To find the reciprocal efficiently, we adopt the Newton-Raphson's algorithm to compute the reciprocal recursively. In general, Newton-Raphson's method can be applied to find the root of a real-valued function, $f(x) = 0$. In the case of a reciprocal function, this leads to the following recursive equation:

$$G^{-1}[n+1] = G^{-1}[n] \cdot \left(2 - G[n] \cdot G^{-1}[n]\right). \tag{3.5}$$

By continuously running (3.5), the reciprocal can be found with high accuracy using only two multipliers.

Compared to other dither-based calibration in the literature [24,32], this approach provides a smooth convergence with no jumps, which reduces calibration-induced artifacts. The total hardware cost is 3 multipliers, 4 adders, 2 sign flippers, and a few scalers. Due to the low rate (32 kHz) operation, the total power consumption of GEC is only 150 nW. Furthermore, the propagation delay from $u$ to $v$ is only 50ns (or 0.16% clock cycle) because neither the LMS engine nor the reciprocal solver is in the GEC's critical path. The critical path only involves logics in the gain corrector block, which includes one adder and one multiplier.

Chapter 3, in part, is based on Section II and Section III of the paper from Jiannan Huang, and Patrick P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation" published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021. The dissertation author is the primary investigator and author of this paper.

# Chapter 4

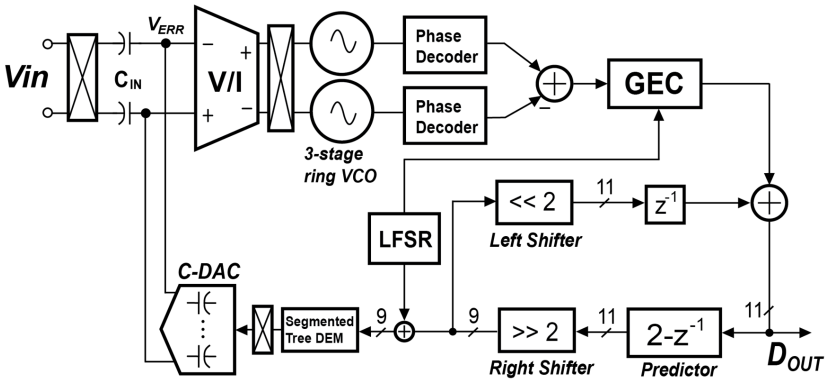
# Circuit Implementation and Measurement

Based on the DPCM theory applied to VCO-based ADCs, along with the VCO gain calibration technique, this chapter presents a prototype IC [35] implementation and its measurement results.

## 4.1 Implementation Details

### 4.1.1 Overall Circuit Structure

Figure 4.1 shows the simplified circuit schematic together with key circuit parameters. The signal bandwidth of this prototype is 500 Hz to meet the needs of most high-precision low-frequency sensor readouts. The sampling frequency, $f_s$, is 32 kHz, which corresponds to an OSR of 32. This ensures more than 40 dB of swing reduction for the VCO quantizer through the DPCM feedback loops. Chopping is employed to mitigate flicker noise, with the chopping frequency chosen also to be 32 kHz to simplify clock generation. The input signal is ac-coupled to the VCO quantizer, which is implemented based on Fig. 6.5 but in a differential fashion. The feedback path employs a capacitive DAC (CDAC) to close the loop because of its low noise and




| Parameter | Value |
|---|---|
| Bandwidth | 500 Hz |
| Fs | 32 KHz |
| $F_{CHOP}$ | 32 KHz |
| $C_{IN}$ | 5 pF |
| $C_{DAC}$ | 500 fF |

**Figure 4.1**: Circuit schematic of the proposed VCO-based AFE and a summary of key circuit parameters.

high energy efficiency. The input range of the AFE is given by

$$\text{Input Range} = \frac{C_{\text{DAC}}}{C_{\text{IN}}} \cdot V_{\text{REF}}, \tag{4.1}$$

where $C_{\text{IN}}$, $C_{\text{DAC}}$, and $V_{\text{REF}}$ are the ac-coupling capacitance, the total CDAC capacitance, and the reference voltage of the CDAC, respectively. The IRN is given by

$$\overline{v_{ni}^2} = \left(\frac{C_{\text{IN}} + C_{\text{DAC}} + C_{\text{V/I}}}{C_{\text{IN}}}\right)^2 \cdot \overline{v_{ni,vco}^2}, \tag{4.2}$$

where $C_{\text{V/I}}$ is the capacitance looking into the V/I, and $\overline{v_{ni,vco}^2}$ is the input-referred noise of the VCO quantizer. From (4.1) and (4.2), we can see that a higher ratio between $C_{\text{IN}}$ and $C_{\text{DAC}}$ trades off IRN for input range. In this prototype, we choose the ratio to be approximately 10 in favor of lower IRN. This yields a 250 $\text{mV}_{\text{pp}}$ input range with $V_{\text{REF}} = 1.2$ V.

The amplitude of $V_{\text{ERR}}$ is dictated by the 2$^{\text{nd}}$ order high-pass filtering from DPCM, the DAC step size, and the dither injected to the DAC. Since the dither, $d$, is chosen to be 1 LSB of the DAC, the expression for the peak amplitude of $V_{\text{ERR}}$ is given by

$$V_{\text{ERR,peak}} = V_{\text{IN}}\left(1 - z^{-1}\right)^2 + \Delta_{\text{DAC}}/2 + d \tag{4.3}$$

$$= V_{\text{IN}}\left(1 - z^{-1}\right)^2 + \frac{3}{2}\Delta_{\text{DAC}}. \tag{4.4}$$

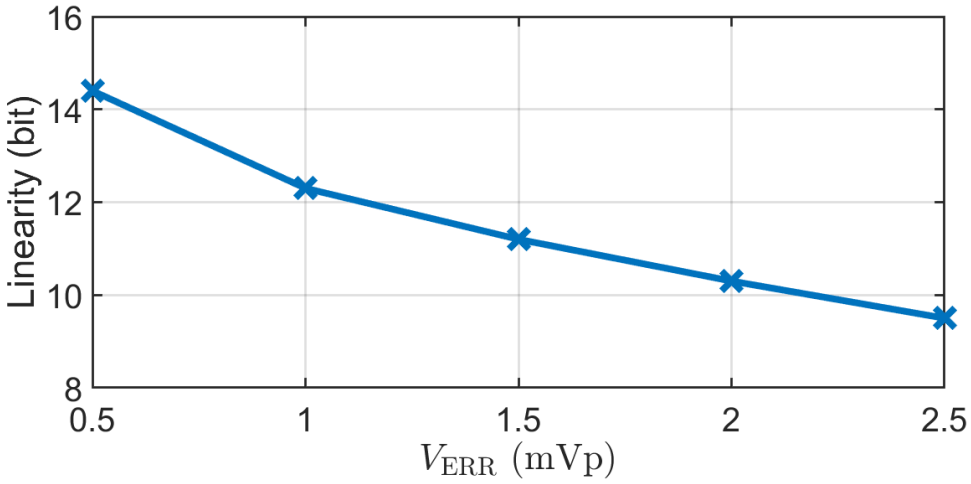



**Figure 4.2**: Feed forward path linearity as a function of $V_{\mathrm{ERR}}$

The feed forward path's (V/I & ring osc.) linearity vs. $V_{\mathrm{ERR}}$ amplitude is shown in Fig. 4.2 per Monte Carlo simulations. In order to ensure over 16-bit linearity for the entire AFE, system level simulation shows that the feed forward path needs to have at least 10-bit linearity. Therefore, the amplitude of $V_{\mathrm{ERR}}$ is restricted to 2 mVp. This imposes a lower limit on the DAC resolution, which is found to be 9-bit. In this work, we target an SQNR beyond 100 dB (17-bit). Using (2.7), it can be shown that $D_{\mathrm{OUT}}$ needs to be 11-bit at OSR $= 32$ to achieve the 17-bit SQNR target. This implies the DAC would have been 11-bit without the truncation technique. Based on the above, the truncation amount $\beta$ is chosen to be 2, therefore relaxing the DAC's resolution from 11 to 9 bits.

### 4.1.2 V/I Converter

The V/I converter is responsible for converting the input voltage to a current, which then feeds the subsequent ring oscillators. Though DPCM ensures a small input swing which relaxes the V/I's linearity requirement, its noise performance remains very critical for the overall system. This implies a low noise for the V/I itself and a large $G_m$ to attenuate VCO noise when input-referred. Figure 4.3 shows the circuit schematic of the employed V/I converter, which is

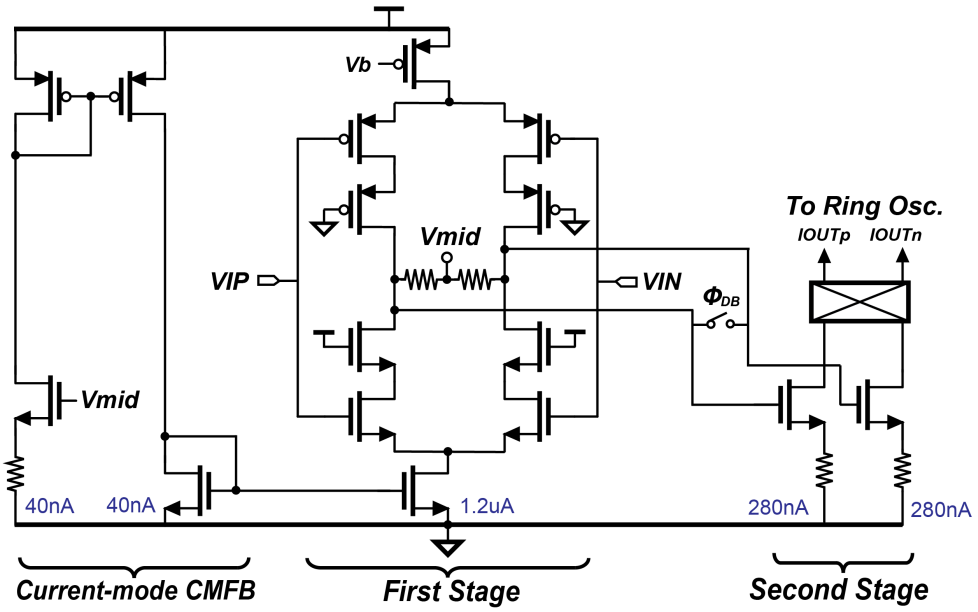



**Figure 4.3**: Circuit schematic of the V/I converter.

implemented as a two stage structure.

The first stage is a current-reuse topology which doubles the $G_m$ compared to a conventional differential pair. To avoid gate leakage, the input transistors are thick oxide devices which has a minimal channel length of 300 nm as opposed to 60 nm for core devices. This results in a large gate area (therefore high $C_{\mathrm{V/I}}$) since the devices are sized with a high W/L ratio to maximize $g_m$. To mitigate the signal attenuation due to capacitive division between $C_{\mathrm{IN}}$ and $C_{\mathrm{V/I}}$, we include cascodes in the first stage whose purpose is not to boost gain but is instead to provide isolation between the first stage input and output, which mitigates the Miller effect from the $C_{\mathrm{gd}}$ of the input transistors, thereby reducing $C_{\mathrm{V/I}}$.

It is worth noting that a deadband switch $\phi_{\mathrm{DB}}$ is added at the output. While the feedback path is processing the signal to be fed back, the switch closes briefly to allow the summing node to fully settle. The duration of switch closing depends on the propagation delay of the GEC, the predictor, and the DAC. Fortunately, the total delay is less than 150 ns, which is only 0.5% of a clock cycle so there is minimal signal loss due to deadband switch closing.

The second stage is a source-degenerated common source structure to ensure good linearity.

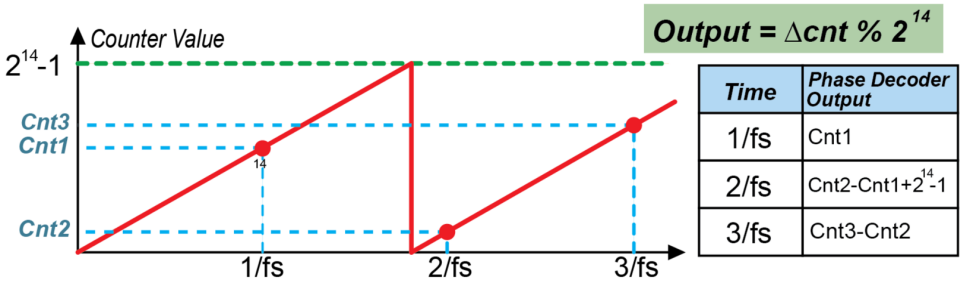



**Figure 4.4**: Illustration of the counter operation with modulo operation.

Its bias current is defined by the current-mode common mode feedback (CMFB) circuit which is a 7x scaled down replica of the second stage. The bias voltage, $V_{\text{mid}}$, comes from the resistive average of the first stage output. This ensures a well-defined bias current for the second stage as well as the subsequent ring oscillators.

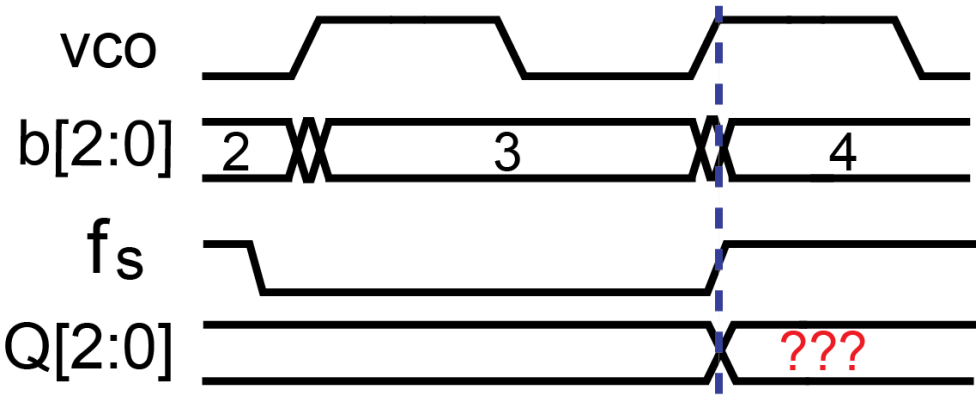
Overall, the V/I consumes 1.3 $\mu$A current and achieves an IRN density of 40 nV/rtHz and a Gm of 18 $\mu$S according to simlation. This ensures a low noise from the V/I itself and a large attenuation of noise from the following VCO.

### 4.1.3 VCO Phase Decoder With Gray-Code Encoding

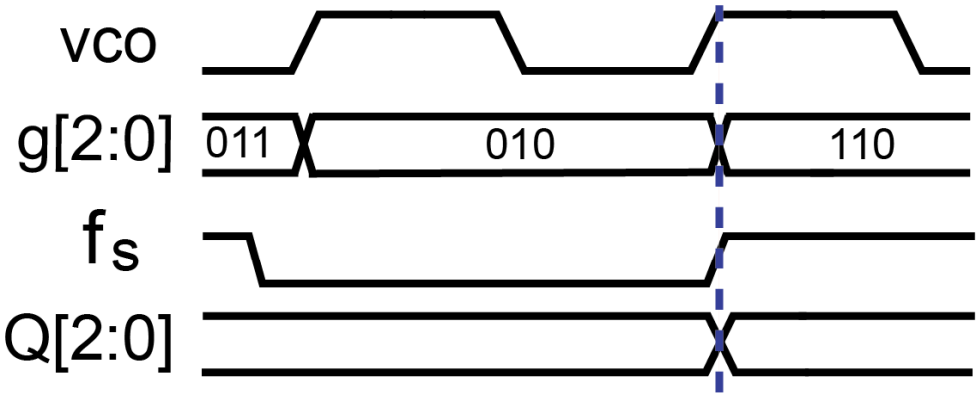
The VCO and phase decoder are implemented based on the principle described in section II-A. Figure 4.4 illustrates the operation of the 14-bit counter implemented in this work. The counter is not reset and is designed to wrap around when overflow occurs. To correct for wrap-around errors, a modulo operation is taken on the phase decoder output. It can be shown that overflow is not an issue as long as the counter wrap-around occurs at most once per sampling period, which is satisfied providing

$$f_{\text{osc}} < f_s \times 2^{14}. \tag{4.5}$$

However, there is one issue with the topology in Fig. 6.5. The counter output, which is in the VCO's clock domain, is asynchronous with respect to the DFF's sampling clock, $f_s$. This may




(a)




(b)

**Figure 4.5**: (a) Binary encoding results in unknown DFF output Q if $f_s$ coincides with VCO transition, and (b) gray-code encoding results in well defined Q in the same situation.

potentially cause unknown DFF outputs if the rising edge of $f_s$ coincides with counter transitions, as illustrated in the 3-bit counter example in Fig. 4.5(a), where $b$ is the counter output and $Q$ represents DFF output. This is because the binary output, $b$, can have more than one bit flips at each VCO edge. Due to circuit non-idealities such as clock skews, the bit-flips happen at slightly different times with respect to the rising edge of $f_s$. This results in intermediate values being mistakenly sampled.

To address this issue, we propose the use of gray code to encode the counter output as shown in Fig. 4.6, where binary-to-gray encoder and gray-to-binary decoder are added before and after the DFFs, respectively. Gray encoding is designed such that consecutive numbers differ

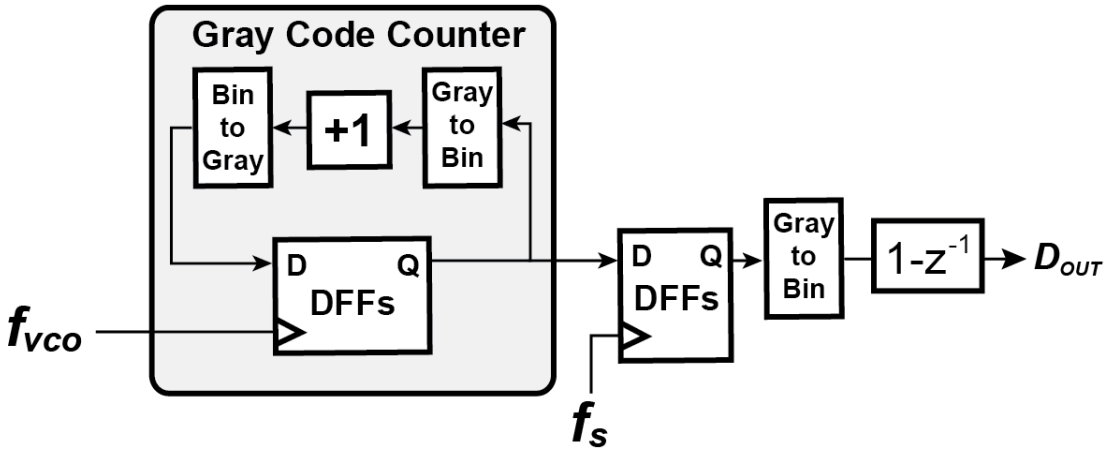



**Figure 4.6**: VCO phase decoder with gray-code encoding.

by only one bit. This ensures that there is only one bit that flips during transitions as shown in Fig. 4.5(b) so there is no intermediate values that could be sampled by mistake. It is worth noting that metastability can occur in both binary and gray code cases when $f_s$ samples right at counter transitions. But since there is only one bit-flip in the case of gray code, no matter which direction this bit resolves to, the maximal error is limited to one.

The gray code encoder and decoder can be simply implemented with a few XOR gates [36], so the overhead of this scheme is negligible.

### 4.1.4 Capacitive DAC

This work adopts a charge redistribution CDAC to close the loop, as shown in Fig. 4.7. Compared to resistive and current steering implementations, CDACs consume zero static current. Furthermore, it interfaces naturally with the ac-coupled input. Dynamic element matching (DEM) logic is used to encode the 9-bit input to generate a 26-bit control bus for the segmented unit DAC cells. Chopping is performed by XORing the DEM output with the chopping clock. The unit capacitor is implemented as custom-drawn metal-oxide-metal finger capacitor whose capacitance is extracted to be 1fF by a commercially available EDA tool. In order to lower the parasitic capacitance to ground, only one layer of relatively high level metal (M7) is used. Also, to provide

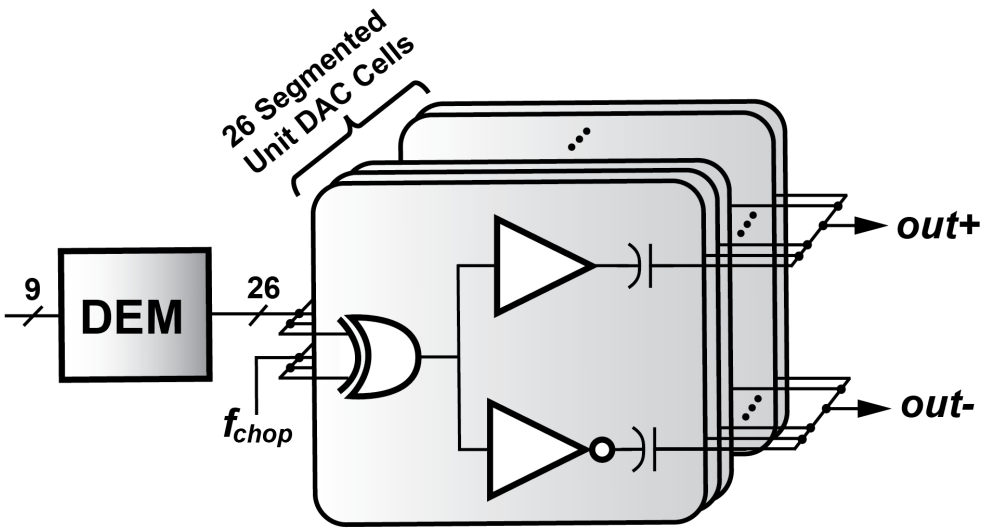



**Figure 4.7**: Schematic of the charge redistribution DAC.

better matching, double minimal width and spacing are used for the fingers at the price of a relatively low capacitance density. Note that mismatch between the extracted value and the actual total capacitance is not an issue, because this only results in variation in $G_{\mathrm{DAC}}$, which is tracked and corrected by the GEC.

The mismatch among each unit capacitor, however, can be a serious issue which can degrade linearity. Though the resolution requirement is reduced to 9 bits thanks to the truncation technique, it is still challenging to maintain good matching without the use of other techniques. Therefore, we employ the use of segmented-tree DEM from [37, 38], as shown in Fig. 4.8. Compared to the traditional data weighted averaging (DWA) DEM which outputs 512 controls for a 9-bit DAC, the segmented-tree structure needs only 26 output controls by assigning the unit DAC cells with different weights. Moreover, it has the benefit of no spurious tones which increases SFDR. At the clock rate $f_s$ = 32 kHz, the segmented tree DEM consumes only 40 nW and has a very low propagation delay of 30 ns or 0.1% clock cycle.

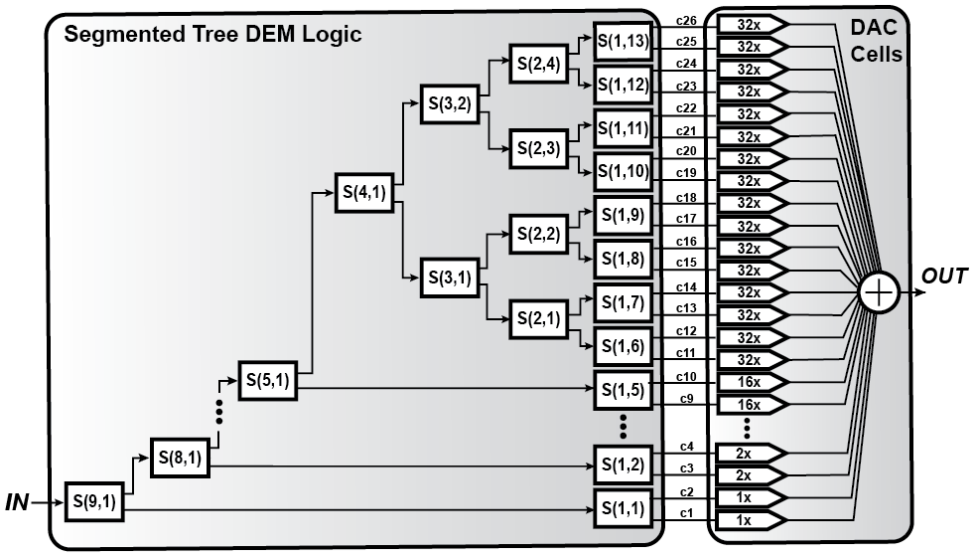



**Figure 4.8**: Segmented tree DEM structure.

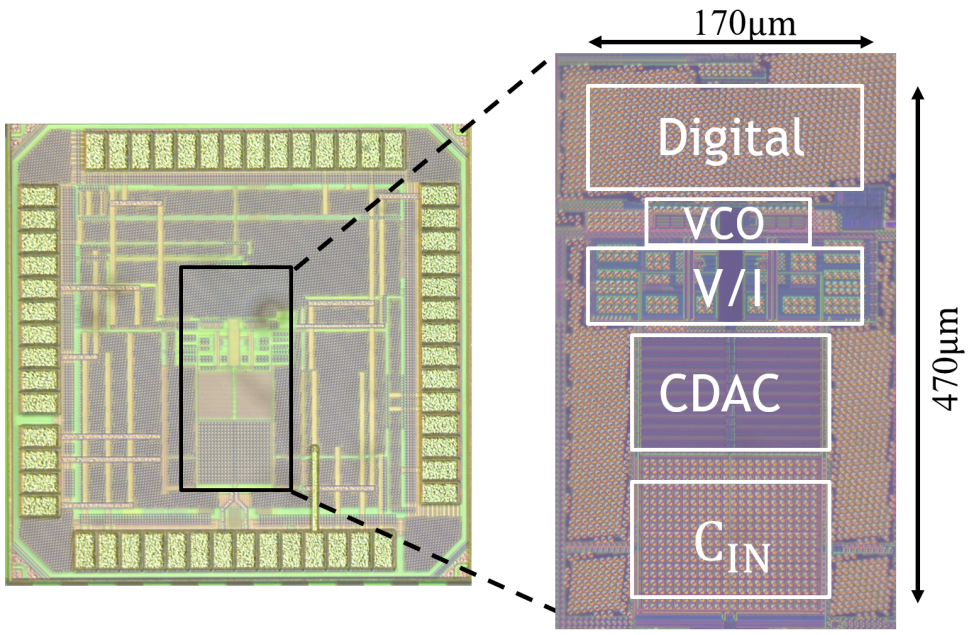



**Figure 4.9**: IC micrograph of the AFE.

| Block | Supply [V] | Power [µW] |
|---|---|---|
| V/I | 1.2 | 1.61 |
| VCO | 0.7 | 0.44 |
| CDAC | 1.2 | 0.29 |
| Digital | 0.7 | 0.84 |
| **Total** | N/A | 3.18 |

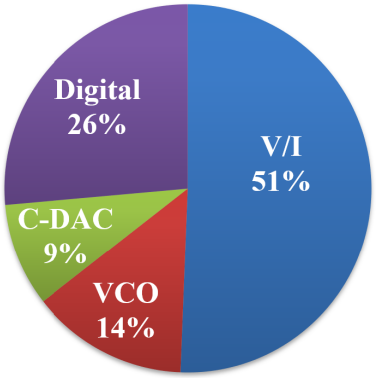



**Figure 4.10**: Power consumption breakdown of the AFE.

## 4.2 Measurement Results

Fabricated in a 65 nm LP process, the AFE occupies an area of 0.08 $mm^2$. Figure 4.9 shows the chip micrograph of the AFE. The digital parts including phase decoder, GEC, and DEM are synthesised and placed and routed on-chip by commercially available EDA tools. The V/I and CDAC operate under a 1.2 V analog supply, while the VCO and digital parts operate under a 0.7 V supply. The total power consumption is measured to be 3.2 $\mu$W with the power break down shown in Fig. 4.10. The input impedance, $Z_{IN}$, is measured to be 4 MΩ, which is primarily limited by the switched-capacitor impedance formed by the input choppers. To further boost $Z_{IN}$, the auxiliary buffer technique from [11] can be applied. The PSRR measured with a 50 $mV_{pp}$ ripple at 60 Hz injected to the supplies is 89 dB. The CMRR measured with a 250 $mV_{pp}$ common mode input at 60 Hz is 98 dB.

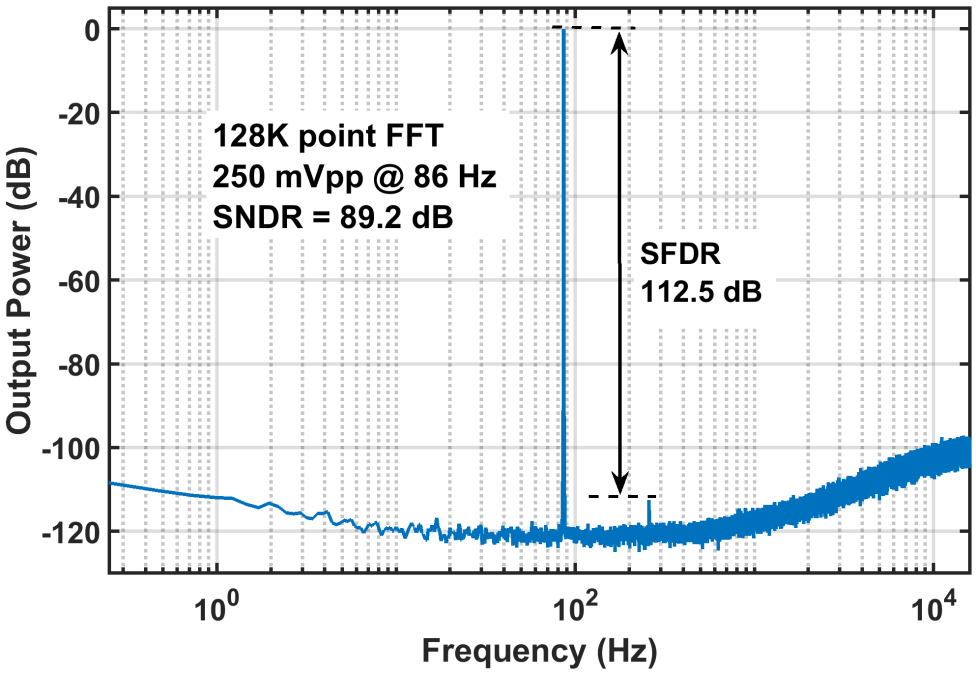



**Figure 4.11**: Output spectrum of the AFE with a sinusoid input.

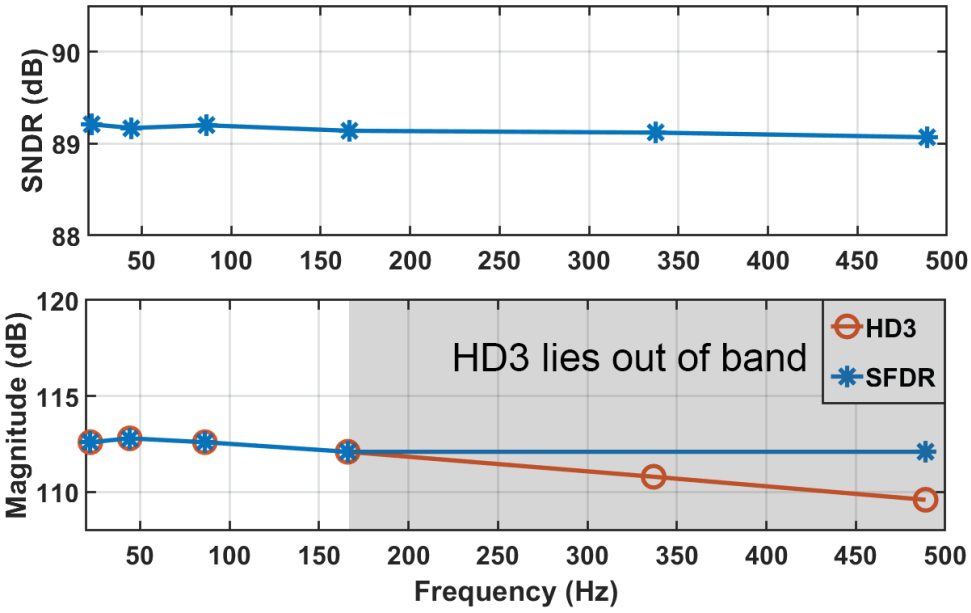



**Figure 4.12**: SNDR and SFDR (HD3 versus frequency. SFDR is limited by HD3 only, which lies out of band for $f_{in}$ beyond 166Hz.

The AFE is characterized with a sinusoidal input at 86 Hz with an amplitude of 250 $mV_{pp}$.

As shown in Fig. 5.14, the output spectrum is measured by averaging 4 segments of a 128k point FFT with 50% overlap. The spectrum shows the expected 1$^{st}$ order quantization noise shaping from the VCO quantizer. The resulting SNDR is 89.2 dB. The SFDR is limited by the third harmonic, which is 112.5 dB below the fundamental. This demonstrates the lowest reported distortion level for VCO-based ADCs among prior arts and clearly shows the effectiveness of DPCM in reducing distortion. The SNDR and SFDR versus input frequency is shown in Fig. 4.12. The SFDR is limited only by HD3, which lies out of band for $f_{\text{in}}$ beyond 166Hz. It should be noted that the result is better than that reported in the conference proceedings [39] because it turns out that our measurement was originally limited by distortions from the signal generator. After replacing with an audio signal generator (APx555), we eliminate distortion from the source and obtain this result.

Figure 4.13 compares the output spectra with and without features enabled. If GEC is disabled, a significant increase in noise floor can be observed, which degrades SNDR to 76.1 dB. This is because the assumption of $|L_1| = |L_2|$ no longer holds, which leads to incomplete cancellation of truncation error, $E_S$. If we disable DEM instead, SNDR reduces to 77.9 dB because of distortions resulting from CDAC capacitor mismatch.

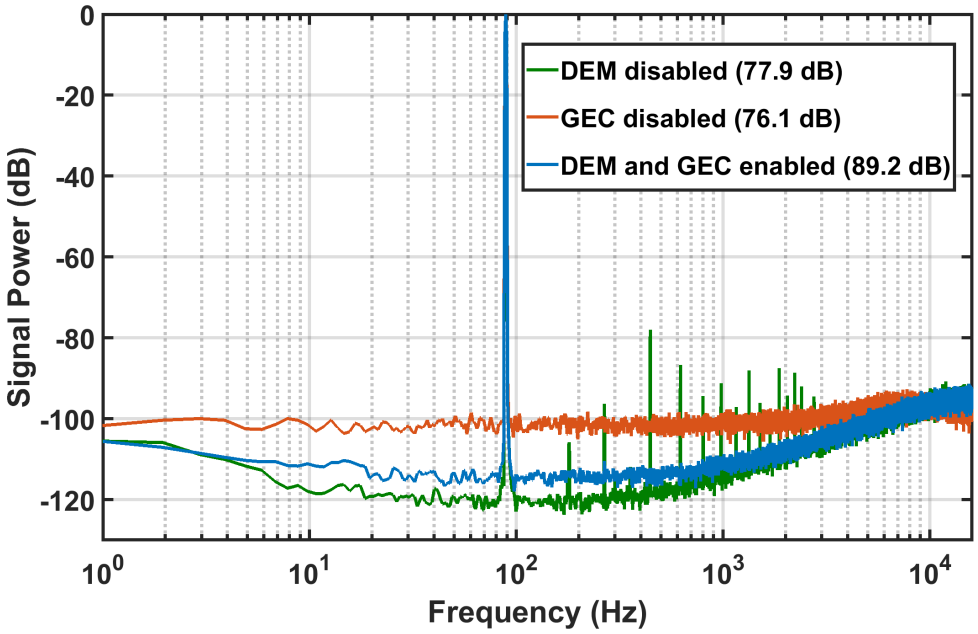



**Figure 4.13**: Spectrum comparison with the enable/disable of DEM and GEC.

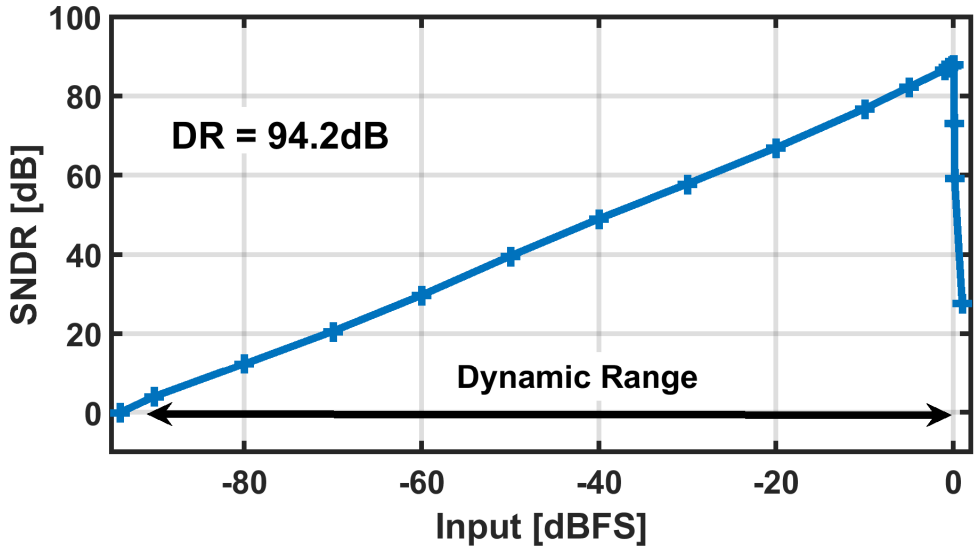



**Figure 4.14**: Measured SNDR vs. input amplitude.

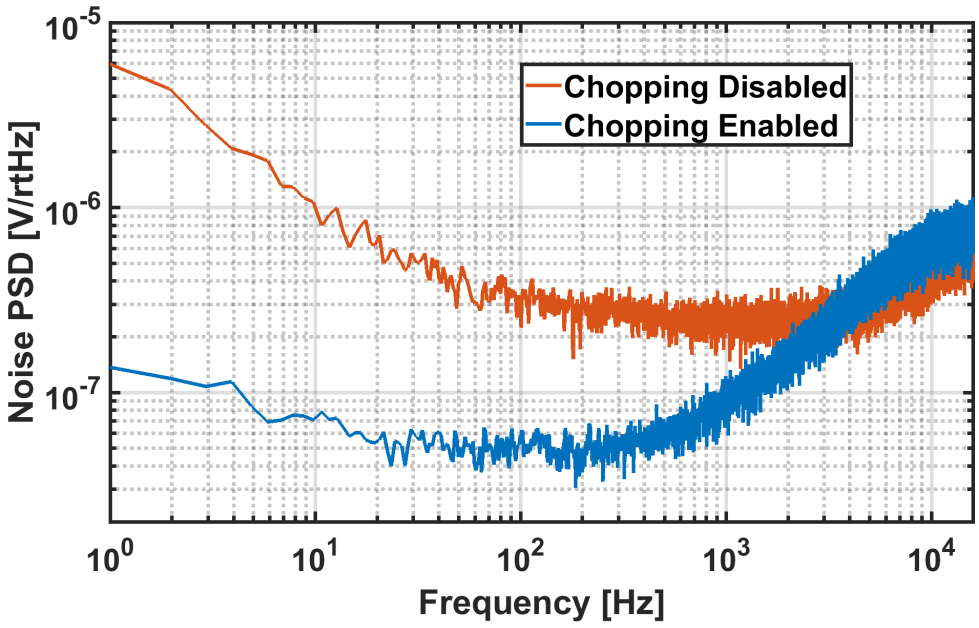
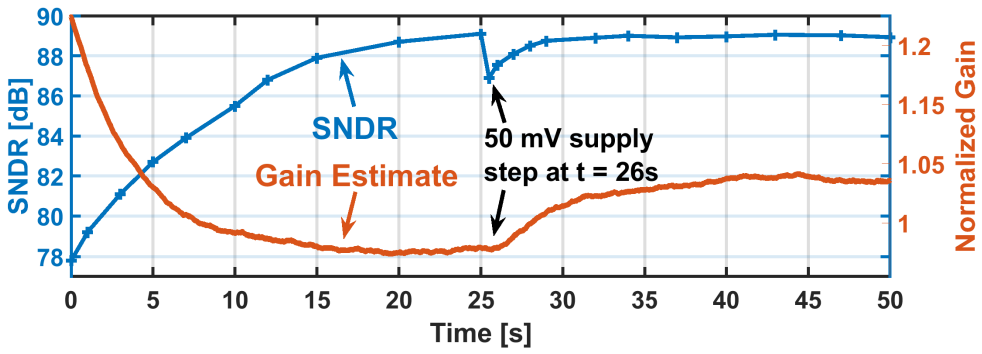



**Figure 4.15**: IRN spectrum measurement with and without chopping.

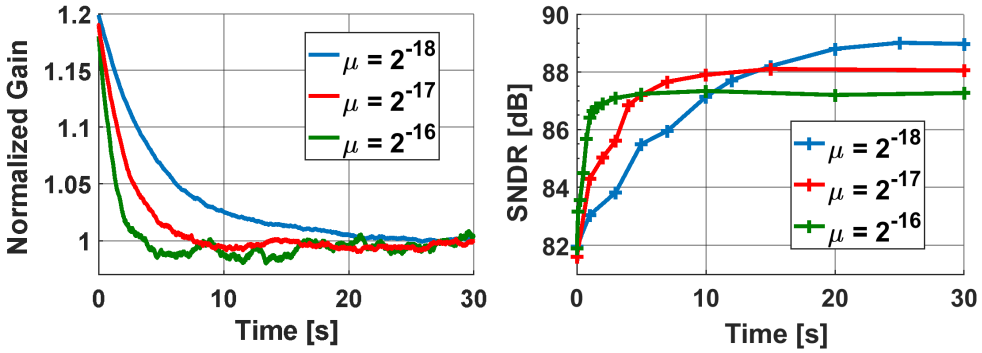
The DR of the prototype is obtained by measuring SNDR vs. input amplitude. The result is shown in Fig. 4.14, where 94.2 dB DR is achieved. This provides the AFE with great flexibility to detect small bio-potentials while tolerating large artifacts.

The IRN spectrum of the AFE is shown in Fig. 4.15. With chopping disabled, the integrated IRN in the signal band is 16.6 $\mu V_{rms}$ and is dominated by flicker noise. After enabling chopping, IRN reduces to 1.18 $\mu V_{rms}$ which corresponds to a noise density of 53 nV/rtHz. Despite being greatly suppressed by the V/I, residual flicker noise from the VCO is visible because it is not chopped. Overall, the system is thermal noise limited and is dominated by noise from the V/I.

Figure 4.16(a) shows the estimated gain, $\hat{G}$, and SNDR over time. It can be seen that the initial gain estimate is higher than the actual gain, which causes a low initial SNDR. But as $\hat{G}$ converges to the correct value, SNDR steadily climbs up to the peak value. To find out the GEC's performance under voltage variations, an intentional supply voltage step is introduced at $t = 26$ s which increases $K_{VCO}$. This causes an immediate dip in SNDR, which then restores back up as GEC detects this change and re-converges to a new gain value that reflects the supply step.




(a)




(b)

**Figure 4.16**: (a) Estimated gain and SNDR over time showing robust operation against supply variation, and (b) tradeoff between convergence speed and peak SNDR with different $\mu$.

This shows that the GEC tracks supply variations, demonstrating the robust operation of the AFE. Figure 4.16(b) shows the impact on convergence speed and peak SNDR due to different $\mu$ in the LMS engine. As can be seen, a smaller $\mu$ results in a slower convergence rate but a higher peak SNDR because of less fluctuation of gain estimate. If a fast convergence is desired, $\mu$ can be set higher through the SPI interface to achieve convergence in as fast as 2 seconds at a price of 2 dB lower SNDR. This shows that $\mu$ serves as a useful knob to allow tradeoff between convergence speed and peak SNDR, which provides flexibility to meet the needs of different applications.

**Table 4.1**: Comparison With State-of-the-Art Sensor Front-ends.

| | [11] JSSC'18 | [12] VLSI'19 | [13] VLSI'18 | [14] JSSC'18 | [26] JSSC'17 | [28] CICC'19 | **This Work** |
|---|---|---|---|---|---|---|---|
| **Topology** | CCIA+3rd order CTDSM | Hybrid CT-DT DSM | 3rd order CTDSM | 2nd order CTDSM | Open-loop VCO-based | 2nd order VCO-PLL Hybrid | **VCO-based with DPCM** |
| **$F_s$ (Hz)** | 400K | 200K | 12.8K | 32K | 3K | 2.5M | **32K** |
| **Area ($mm^2$)** | 0.053 | 0.48 | 0.55 | 0.024 | 0.135 | 0.025 | **0.08** |
| **Bandwidth (Hz)** | 5K | 100 | 300 | 500 | 200 | 10K | **500** |
| **Supply (V)** | 1.2 | 1.8 | 1 | 0.8 | 1.2 (A)<br>0.45 (D) | 0.8 (A)<br>0.6 (D) | **1.2 (A)**<br>**0.7 (D)** |
| **Input range ($mV_{PP}$)** | 200 | 720 | 360 | 260 | 100 | 100 | **250** |
| **Power ($\mu$W)** | 7.3 | 73.8 | 6.5 | 0.8 | 7 | 4.5 | **3.2** |
| **IRN ($nV/\sqrt{Hz}$)** | 90 | 98 | 265 | 44 | 367 | 36 | **53** |
| **NEF** | 8.5 | 24 | 26 | 1.81 | 61 | 3.5 | **4.06** |
| **SNDR (dB)** | 78 | 66.2 | 84.3 | 66.1 | 75.2 | 78.5 | **89.2** |
| **THD (dB)** | -81 | -68.8 | -104.7 | -71 | -79 | -91 | **-112.5** |
| **DR (dB)** | 81 | 108.3 | 92.3 | 92 | 80 | 79 | **94.2** |
| **CMRR (dB)** | - | 109 | 84 | 81 | 68 | 83 | **98** |
| **$Z_{IN}$ (MΩ)** | 1520 | 34 | 39 | 20 | ∞ | 0.22 | **4** |
| **FOM (dB)** | 166.4 | 127.5 | 160.9 | 154 | 150 | 172 | **171.2** |

$\text{FOM} = \text{SNDR} + 10\log\frac{\text{BW}}{\text{Power}}$

## 4.3 Comparison and Conclusion

Table 6.1 summarizes the performance and compares this work with other state-of-the-art sensor front-ends. Thanks to the DPCM architecture, the total harmonic distortion (THD) of this work is by far the lowest amongst prior arts. Importantly, this work demonstrates the best overall tradeoff among power, noise, linearity, and input impedance for ADC-direct AFEs.

We have presented an ADC-direct VCO-based AFE for sensing applications that provides over 90 dB of DR to simultaneously resolve both small signals and large artifacts. To overcome non-linearities brought by the VCO-based approach, a DPCM-inspired architecture is adopted to limit the swing that the VCO sees, thus preserving linearity across a large input dynamic range. As a result, we achieve the lowest distortion among VCO-based sensor front-ends, demonstrating the usefulness of DPCM theory in circuit design. In addition, background gain calibration is employed to overcome the gain variation of VCOs to arrive at a robust design. Overall, the AFE achieves very high linearity and high dynamic range while maintaining low power and low noise

for sensing applications.

Chapter 4, in part, is based on Section IV and Section V of the paper from Jiannan Huang, and Patrick P. Mercier, “A 112-dB SFDR 89-dB SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation” published in the IEEE Journal of Solid-State Circuits, volume 56, number 4, pages 1046-1057, April 2021. The dissertation author is the primary investigator and author of this paper.

# Chapter 5

# Calibration-Free DPCM

In Chapter 2, we have seen the usefulness of DPCM in reducing VCO V-to-F non-linearity by lowering the swing that the VCO sees. A dither-based VCO gain calibration described in Chapter 3 is employed to ensure a proper loop dynamic. In Chapter 4, we demonstrated a prototype IC that achieves close to state-of-the-art performance. The bottleneck of this work is that the overall power efficiency can still be improved from both the digital and analog sides. To address this, in this chapter, we present a second-generation version of [35] and an expanded version of [40] that, along with various other techniques, offers the following key improvements:

1) a significant reduction of power consumption enabled by eliminating the need for gain error calibration to arrive at a calibration-free DPCM architecture;

2) a single low-voltage supply enabled by replacing the two-stage V/I design in [35] with a simple differential pair, thus leading to a mostly digital design that facilitates direct biomedical SoC integration; and

3) an increased SQNR resulting from a coarse-fine phase decoding scheme with a resampling technique to avoid metastability.

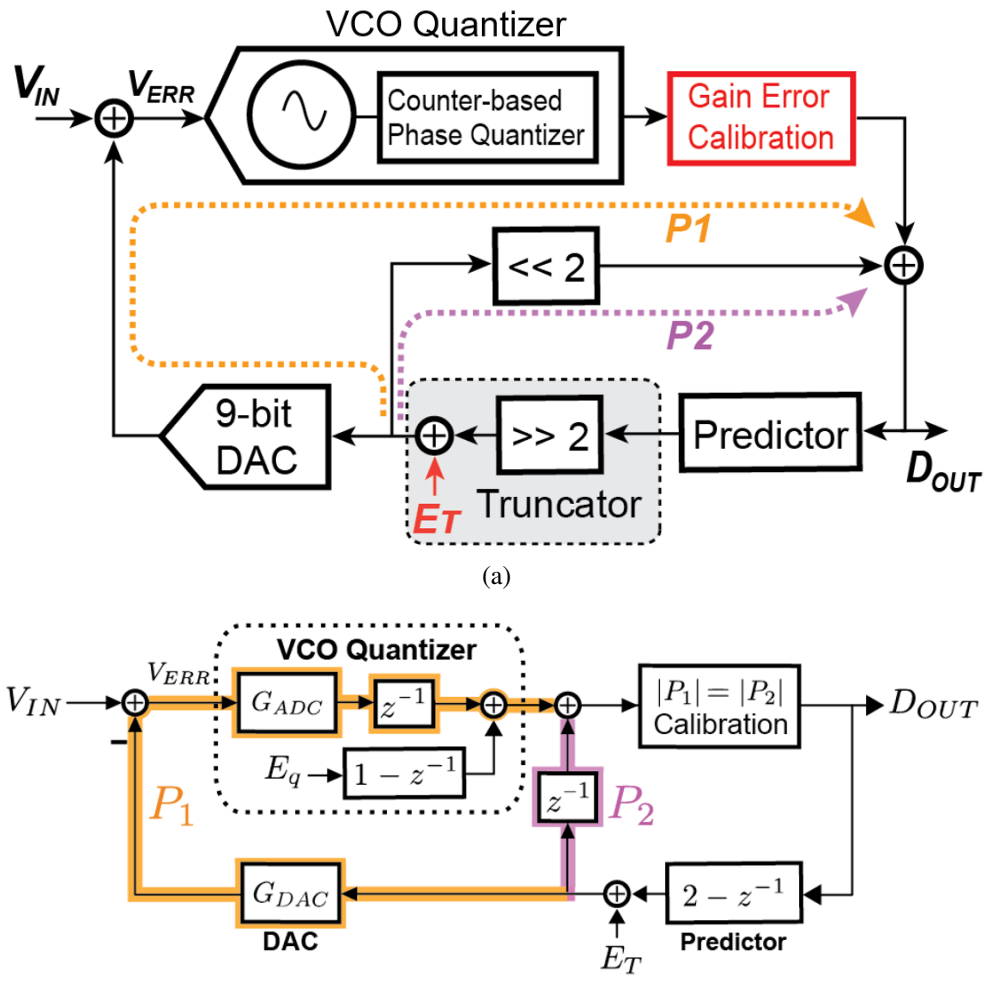



**Figure 5.1**: (a) Prior-art VCO-based AFE with a calibrated DPCM architecture, and (b) discrete-time model of the prior-art.

## 5.1 Limitations of Gain Calibration

Recall the gain calibrated DPCM architecture repeated here in Fig. 5.1(a). Note that the two paths, $P_1$ and $P_2$ (highlighted in orange and purple, respectively), from the input of the DAC to the system output, $D_{\mathrm{OUT}}$. Thanks to the DPCM architecture, the design requirements of the feedforward path (namely the VCO quantizer) are significantly relaxed. However, the DAC in the feedback path needs to have a high resolution (11-bit in [35]) due to the wide DR requirement. The wide bit-width presents significant challenges for the unit DAC element matching, which

compromises the overall linearity.

To address this issue, [35] employed a truncator right before the DAC to reduce its bit-width by two. Although the DAC resolution requirement is relaxed, this also introduces truncation error, $E_T$, to the system, which degrades SNR. To mitigate the effect of $E_T$, [35] adopted a gain error calibration (GEC) logic to calibrate for equal path gain magnitudes (i.e., $|P_1| = |P_2|$). To see why GEC is needed in [35], it is useful to understand the discrete-time model of this prior-art as shown in Fig. 5.1(b).

In Fig. 5.1(b), the quantization noise, $E_q$, is $1^{\text{st}}$-order shaped (i.e., by a $1-z^{-1}$ transfer function) due to the inherent noise shaping capability of the VCO quantizer. Also, the predictor's transfer function, $P$, is chosen to be $2-z^{-1}$. Note that $E_T$ travels along the two paths $P_1$ and $P_2$ before summing to reach $D_{\text{OUT}}$. Since GEC ensures $|P_1| = |P_2|$ and $P_1$ is negative, the two paths have equal magnitudes but opposite polarity. Therefore, $E_T$ is cancelled before reaching the output as long as path gain magnitudes are matched. This enables the designer to reduce the bit-width of the DAC without compromising performance.

Another benefit of equal path gain magnitudes is that it simplifies the loop dynamics. From Fig. 5.1(b), it can be observed that $|P_1| = G_{\text{ADC}}G_{\text{DAC}}$ and $|P_2| = 1$. While $P_2$ path gain is fixed at 1, $P_1$ path gain can vary due to the VCO. Since GEC enforces $|P_1| = |P_2|$, it follows that:

$$G_{\text{ADC}}G_{\text{DAC}} = 1. \tag{5.1}$$

With (5.1), both the signal transfer fuction (STF) and quantization noise transfer function (NTF) can be greatly simplified [35]. First, for the STF from $V_{\text{IN}}$ to $D_{\text{OUT}}$, we have:

$$\frac{D_{\text{OUT}}}{V_{\text{IN}}} = \frac{G_{\text{ADC}}z^{-1}}{1+Pz^{-1}(G_{\text{ADC}}G_{\text{DAC}}-1)} \tag{5.2}$$

$$= G_{\text{ADC}}z^{-1}. \tag{5.3}$$

Second, the NTF from $E_q$ to $D_{\mathrm{OUT}}$ is given by:

$$\frac{D_{\mathrm{OUT}}}{E_q} = \frac{1-z^{-1}}{1+Pz^{-1}(G_{\mathrm{ADC}}G_{\mathrm{DAC}}-1)} \tag{5.4}$$

$$= 1-z^{-1}, \tag{5.5}$$

where $P$ is the predictor's transfer function. In (5.2) and (5.4), the denominators are reduced to unity thanks to (5.1), and the loop dynamic simplifies to that of a standard $1^{\mathrm{st}}$-order $\Delta\Sigma$ modulator.

The aforementioned results hinge on the GEC ensuring $|P_1 = |P_2|$. The GEC in [35] uses a correlation-based calibration approach, which requires a large number of samples to "correlate out" the input signal, thereby resulting in a long (>10 s) convergence time. In addition, the GEC logic requires quite a few wide bit-width multipliers, which are power hungry and significantly add to the digital power consumption.

Last, but not least, it is impossible to achieve exact path gain matching due to the finite digital bit-widths. Better matching inevitably requires wider bit-widths. Hence, a tradeoff exists between path gain matching and digital power consumption. There are two consequences due to the unmatched gains. First, the simplified transfer functions (5.3) and (5.5) are no longer the case; an analysis of the general loop dynamics dictated by (5.2) and (5.4) is needed. Second, when path gains are not matched, $E_T$ leaks to the output, thereby degrading SNR. Figure 5.2 compares the simulated output spectra between the case of matched path gains (i.e., $G_{\mathrm{ADC}}G_{\mathrm{DAC}} = 1$) and 10% unmatched path gains (i.e., $G_{\mathrm{ADC}}G_{\mathrm{DAC}} = 0.9$). It is clear that leaked $E_T$ significantly reduces SNR in this example by an astounding 26 dB. As a result, only a 2-bit truncation was employed in [35] so as to limit $E_T$ power due to concerns of incomplete $E_T$ cancellation.

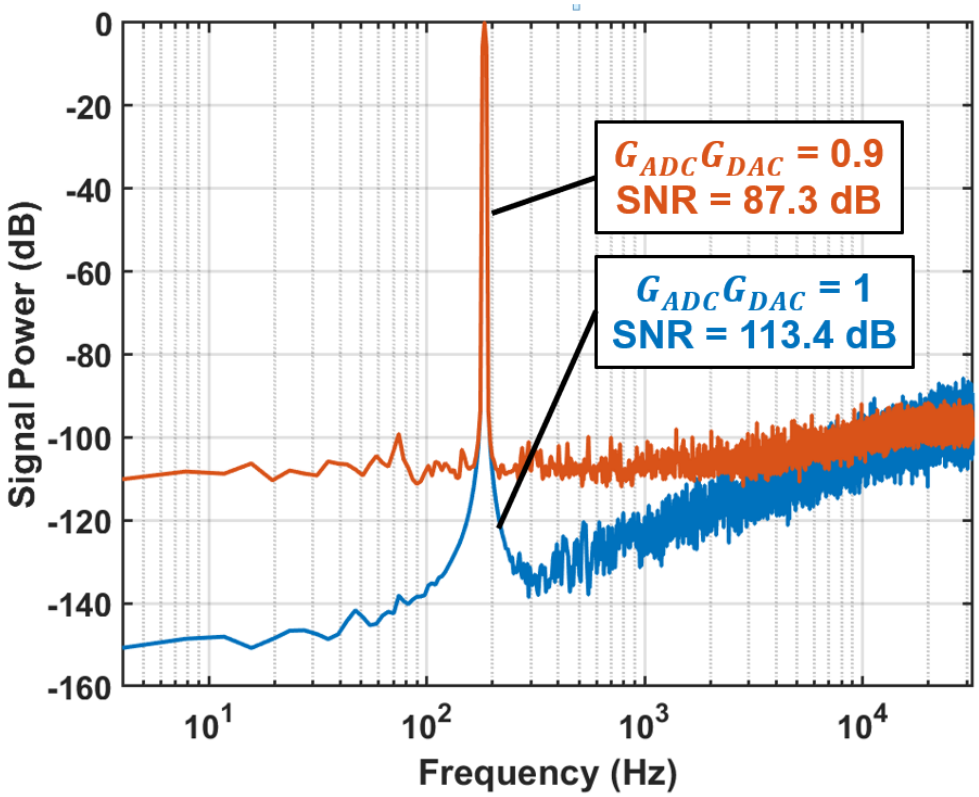



**Figure 5.2**: Comparison of simulated output spectra between matched path gains (blue) and 10% unmatched path gains (orange).

## 5.2 Loop Dynamics without Calibration

The key to understanding the loop dynamics without calibration is to revisit the general STF and NTF expressions given by (5.2) and (5.4), respectively. First, the stability of the system can be analyzed with the aid of the root locus plot as shown in Fig. 5.3, where $G_{\mathrm{ADC}}G_{\mathrm{DAC}}$ varies from 0.8 to 1.3. Here it can be seen that the poles start as complex conjugate pairs inside the unit circle and then converges to the real axis. As $G_{\mathrm{ADC}}G_{\mathrm{DAC}}$ approaches 1.3, the poles become close to the border of the unit circle. It can be shown that as long as $G_{\mathrm{ADC}}G_{\mathrm{DAC}} < 1.34$, stability can be guaranteed. Thus, the nominal $P_1$ path gain in this work is designed to be 0.9 to have extra margin for stability.

Now that stability can be ensured, the next focus is on the shape of the magnitude plots of STF and NTF under path gain variation, which in this case is shown in Fig. 5.4. It can be

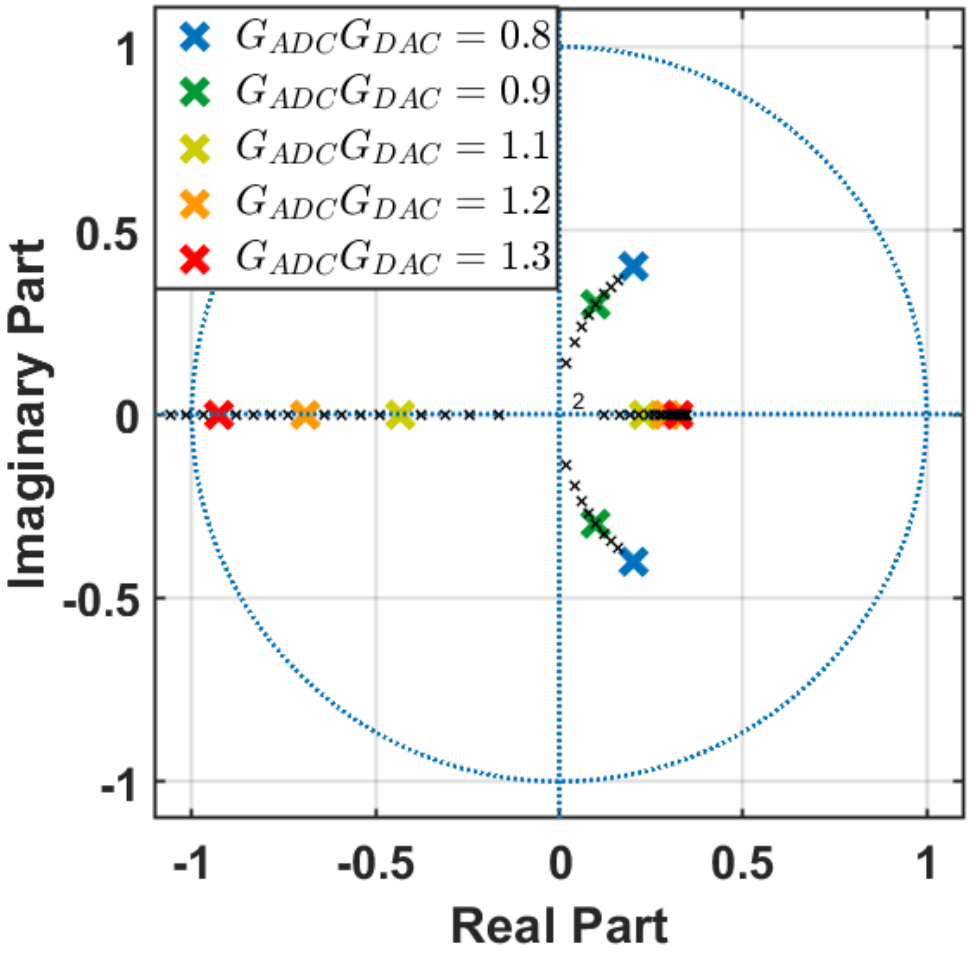



**Figure 5.3**: Root locus plot of the pole location with varying $P_1$ path gain.

observed that when $G_{\text{ADC}}G_{\text{DAC}} = 1$ (i.e., matched path gains) the STF and NTF correspond to the shapes of the simplified expressions given by (5.3) and (5.5). When $G_{\text{ADC}}G_{\text{DAC}}$ deviates from unity (e.g. 0.7 and 1.3), some divergence at high frequency can be observed. However, within the signal band at low frequency, both the STF and NTF maintain their shapes and do not change much with path gain variation.

The above analyses indicate that, as long as the system is stable, the SQNR of a calibration-free system should be close to the case where calibration is employed to ensure equal path gains. Thus, a GEC correction loop is not actually required for loop dynamics or SQNR reasons, if a high-DR DAC is available. Unfortunately, this is not usually the case, and thus more investigations

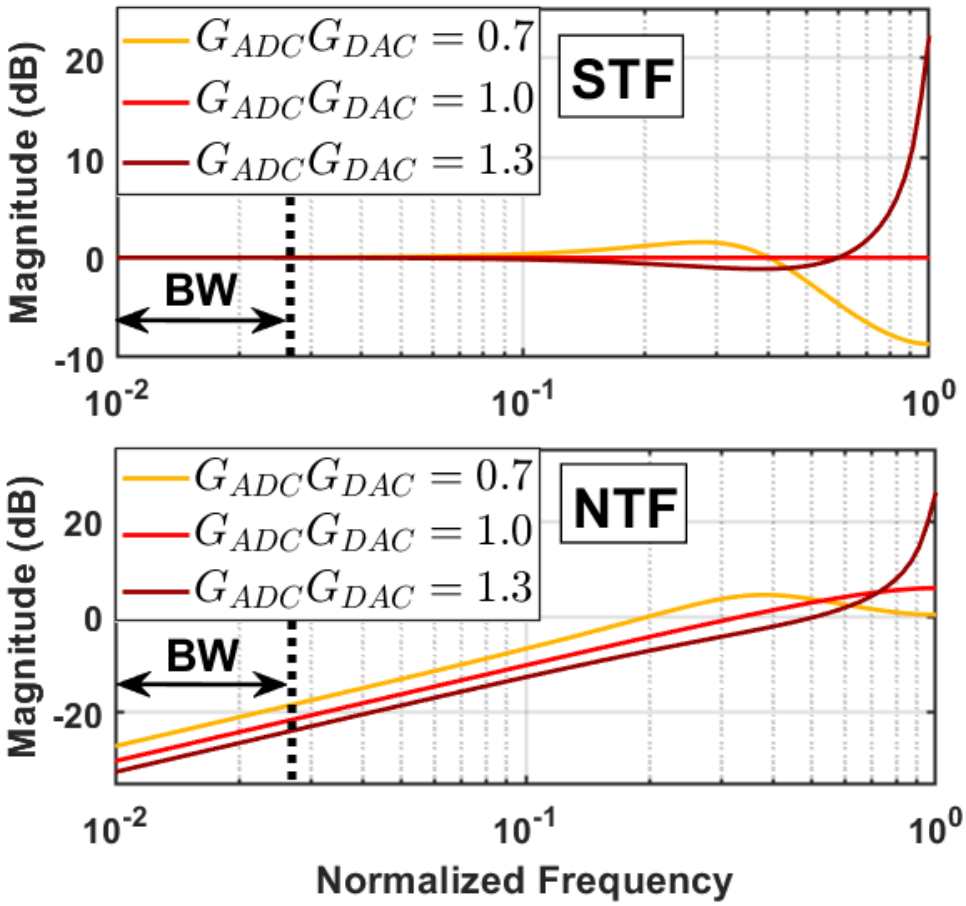



**Figure 5.4**: Magnitude plots of the STF and NTF with varying $P_1$ path gain.

are required.

## 5.3 Truncation Error Shaping

The other issue that must be addressed resulting from the lack of calibration is the $E_T$ leakage. Recall that $E_T$ travels along $P_1$ and $P_2$ and then sums to reach the output. Hence, any path gain mismatch causes $E_T$ to leak to the output, thereby causing significant SNR degradation as shown in Fig. 5.2. The increased noise floor is due to the leaked $E_T$.

Fortunately, there is a simple technique to circumvent this issue: truncation error shaping. In this work, the basic truncator in Fig. 5.1 is replaced by a $1^{st}$-order digital $\Delta\Sigma$M, which is

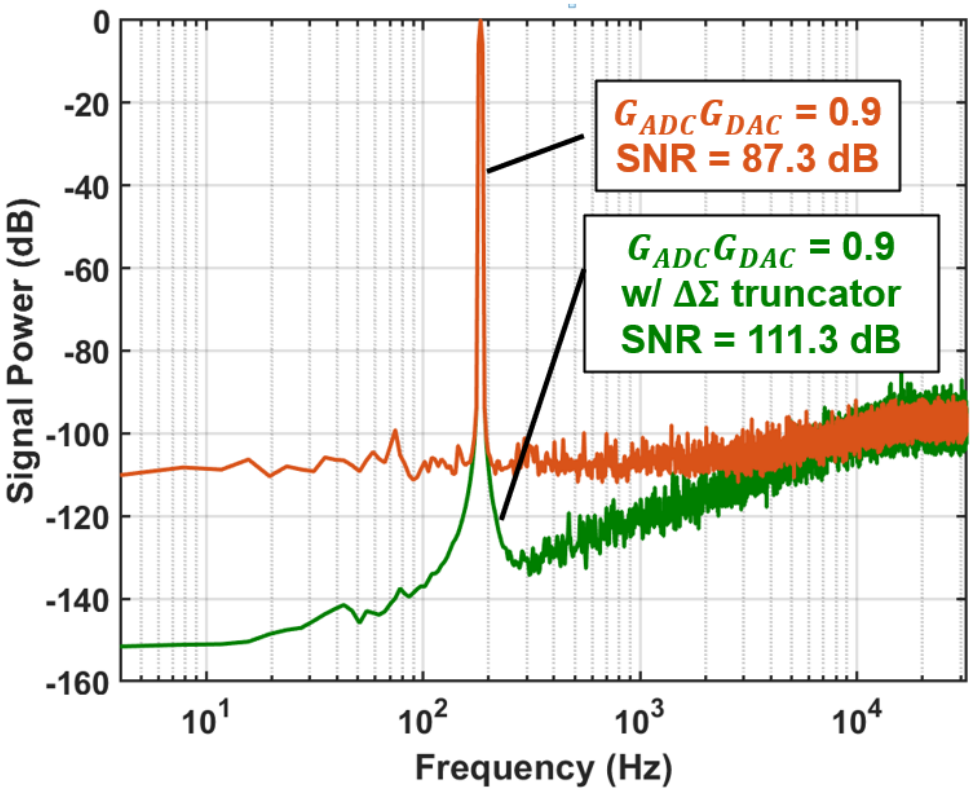



**Figure 5.5**: Comparison of simulated output spectra with 10% path gain mismatch between the case of a regular truncator (orange) and a ΔΣ truncator (green).

expected to shape $E_T$ out of the signal band. Indeed, this is confirmed by the simulated output spectra shown in Fig. 5.5, which compares the case of a regular truncator (orange) and a ΔΣ truncator (green), both with the same 10% path gain mismatch. Clearly, the SNR is restored back to over 110 dB after utilizing the ΔΣ truncator. Note that this is still 2.1-dB lower than the ideal case where path gains are matched, due to the residual shaped $E_T$ in the signal band. However, this has a negligible impact on performance since it is significantly lower than the thermal noise floor.

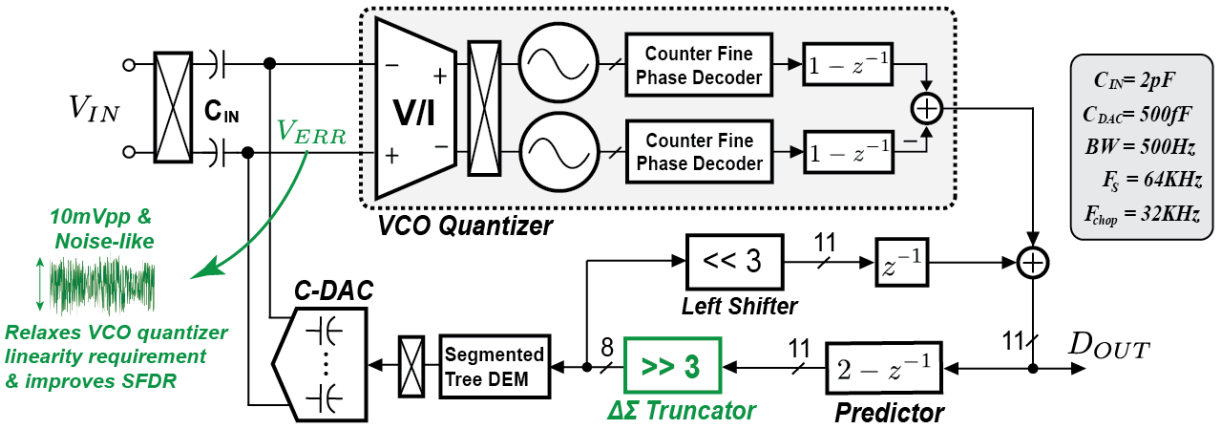



**Figure 5.6**: Simplified circuit schematic of the proposed AFE.

## 5.4 Circuit Implementation

Figure 5.6 shows the simplified circuit schematic of the AFE. Thanks to the now high-pass shaped $E_T$, a more aggressive truncation of 3 bits is made possible, thereby further reducing the DAC resolution to 8 bits compared to [35]. Moreover, the shaped $E_T$ makes the VCO quantizer input, $V_{\mathrm{ERR}}$, noise-like, in addition to being already small-swing. The noise-like $V_{\mathrm{ERR}}$ further improves the spurious-free dynamic range (SFDR) of the overall system because non-linearity acting on noise does not generate tones [41].

The AFE has a signal bandwidth of 500 Hz while the sampling frequency, $f_s$, is 64 kHz, corresponding to an oversampling ratio (OSR) of 64. Chopping is employed to mitigate flicker noise and the chopping clock, $f_{\mathrm{chop}}$, is set to half $f_s$. The ΔΣ truncator uses the standard error feedback architecture [31] to achieve 1$^{\mathrm{st}}$-order noise shaping. The ratio between the input capacitance, $C_{\mathrm{IN}}$, and total C-DAC capacitance, $C_{\mathrm{DAC}}$, is set to 4, which enables a wider linear input range at the price of a higher input-referred noise (IRN) [35]. The C-DAC implementation and the dynamic element matching (DEM) block are similar to that presented in [35].

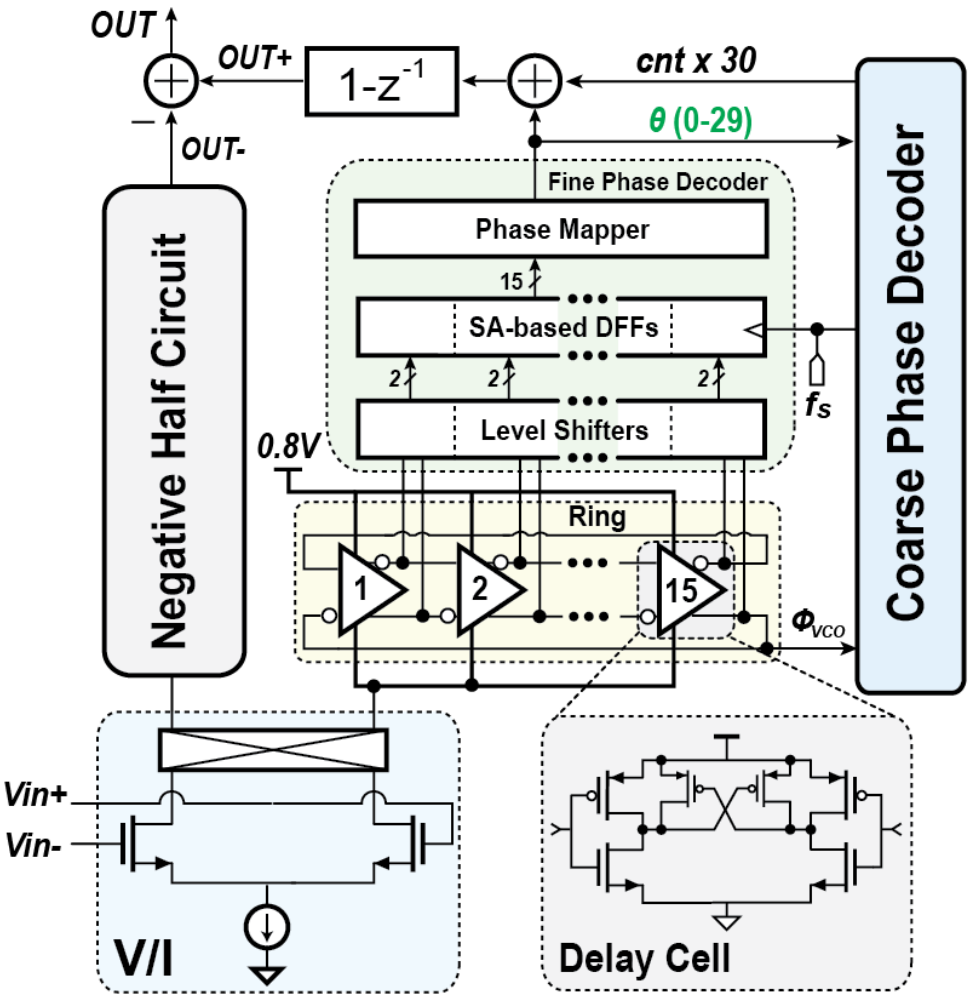



**Figure 5.7**: Simplifeid schematic of the VCO Quantizer.

### 5.4.1 VCO Quantizer with a Coarse Fine Phase Decoder

Figure 5.7 shows the schematic of the VCO quantizer, which consists of a V/I converter followed by a current-starved ring oscillator (RO). The phase outputs of the RO are then translated into a digital word via a coarse-fine phase decoder. The coarse-fine configuration enables a much smaller phase quantization step down to a single inverter delay while accommodating a wider RO center frequency range.

Thanks to the low swing at the V/I input, the V/I is implemented simply as a differential pair with the RO directly stacked on top. Such configuration enables a straightforward current-

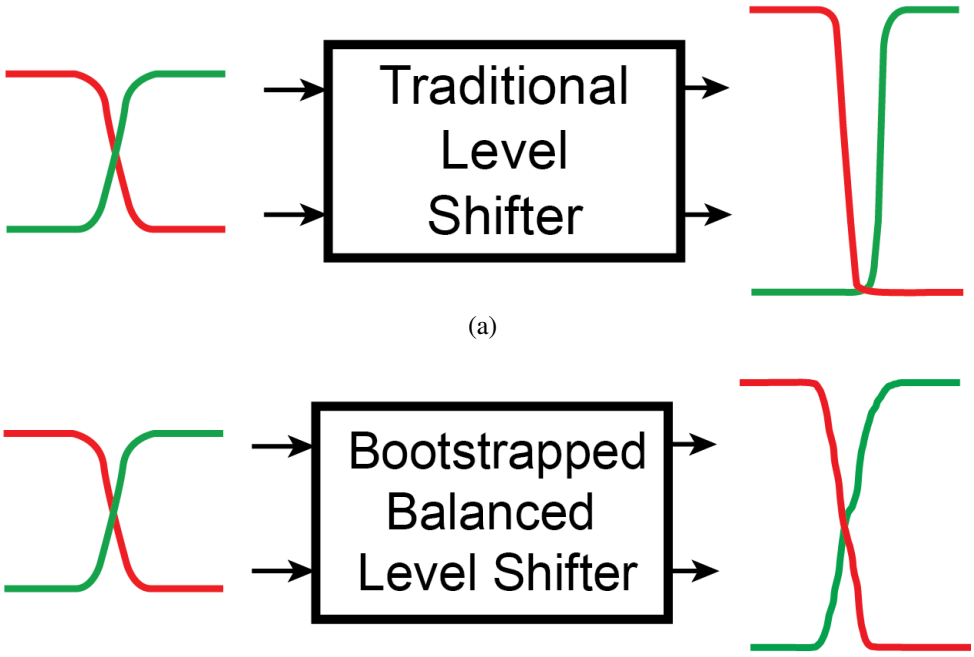
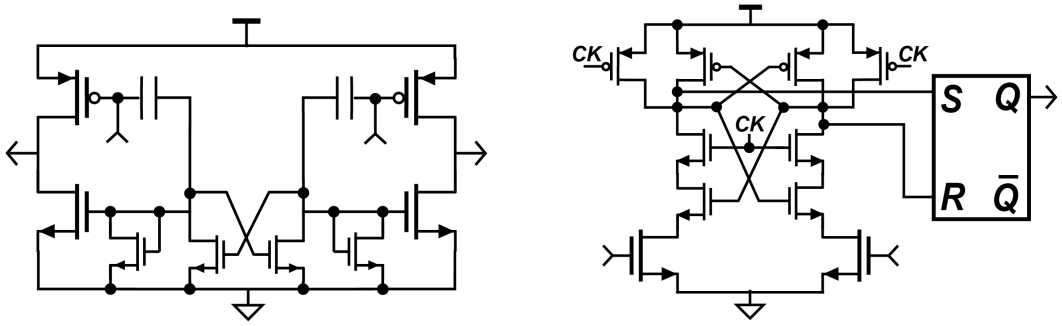



**Figure 5.8**: (a) Output waveform of a traditional level shifter producing unbalanced outputs, and (b) output waveform of the bootstrapped level shifter producing balanced outputs.

reuse between the V/I and the RO, thereby improving current efficiency. As a result, there is no extra current consumed by the RO. The RO has 15 stages, where each delay stage is implemented as a pseudo-differential coupled inverter pair. The inverters are sized relatively large to minimize flicker noise from these devices.

The fine phase decoder taps each stage of the RO. Since the RO has a low 0.8 V supply and is current-starved at the tail, level shifters are needed to convert the 300 mV swing to full rail-to-rail. While traditional level shifters have no problem of performing level shifting from 300 mV to 800 mV, they have issues producing unbalanced outputs given a balanced input. This is illustrated in Fig. 5.8(a), where unbalanced outputs may result in a brief moment of simultaneous lows (or highs) due to the ratioed logic nature of the traditional level shifter, This causes metastability for the subsequent flip-flop when sampling the level-shifted outputs right at the simultaneous lows (or highs).

To address this concern, a balanced bootstrapped level shifter (Fig. 5.9(a)) [42] is




(a) (b)

**Figure 5.9**: (a) Schematic of the balanced bootstrapped level shifter, and (b) schematic of the SA-based DFF.

employed that produces balanced outputs given balanced inputs while reliably performing level shifting. The capacitors in Fig. 5.9(a) is implemented using MOS capacitors. The simulated level shifted waveform is shown in Fig. 5.8(b), which ensures no simultaneous lows (or highs), thereby reducing error in the subsequent sampling operation. To further lower the chance of metastability, a sense-amplifier (SA)-based D flip-flop (DFF) is utilized, as shown in Fig. 5.9(b). Finally, a digital phase mapper maps the 15 sampled RO outputs into a fine phase, $\theta$, which ranges from 0-29 representing the 30 quantized phase levels in $2\pi$.

In Fig. 5.7, one delay stage output, $\phi_{\mathrm{VCO}}$, is used to keep track of phase wrap-around in the coarse phase decoder. A simple yet problematic implementation can be a counter clocked by $\phi_{\mathrm{VCO}}$ whose output is sampled by $f_s$. The sampled counter output is then multiplied by 30 and summed with $\theta$ to form the complete quantized phase. The issue with this implementation lies in the potential metastability problem when sampling the counter output, since the counter (which is in the RO's clock domain) updates asynchronously with respect to $f_s$. To solve this problem, the following resampling technique is proposed.

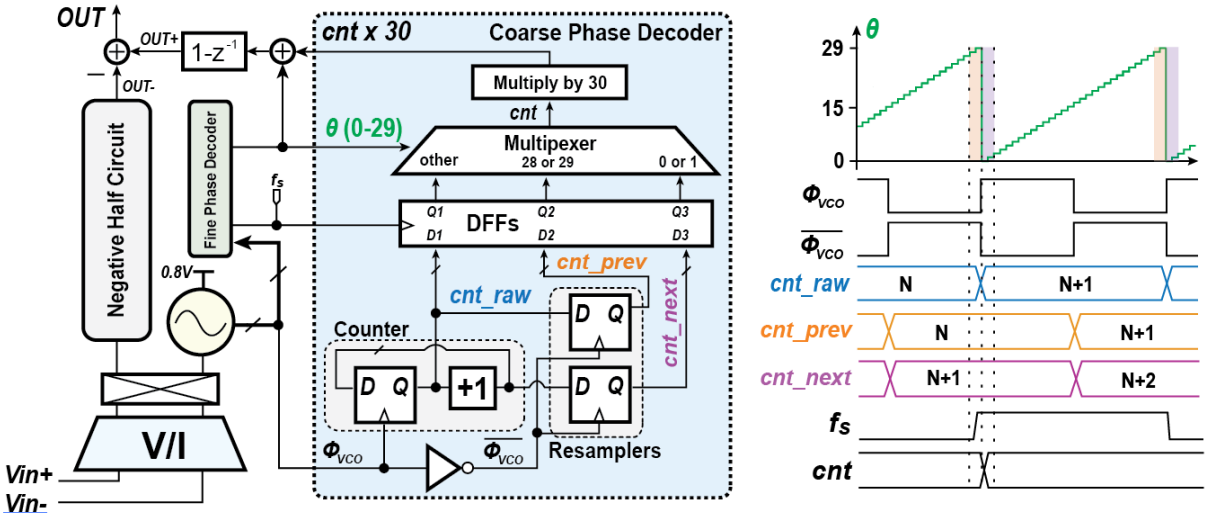



**Figure 5.10**: Implementation and illustration of the resampling technique to avoid metastability.

### 5.4.2 Resampling Technique

Figure 5.10 shows the implementation of the coarse phase decoder with the resampling technique to avoid the aforementioned metastability problem. The RO output, $\phi_{VCO}$, is still used to clock a counter so as to record the number of whole $2\pi$ cycles. The counter output is named *cnt_raw*. What's unique here is that an inverted version of $\phi_{VCO}$ called $\overline{\phi_{VCO}}$ is used to clock two resamplers (implemented as DFFs) which sample *cnt_raw* and *cnt_raw* + 1. In other words, the counter output and the next count are resampled at the falling edge of $\phi_{VCO}$. The respective resampled outputs are named *cnt_prev* and *cnt_next*. Next, *cnt_raw*, *cnt_prev*, and *cnt_next* are all sampled by $f_s$ and then multiplexed according to $\theta$.

As shown in the timing diagram in Fig. 5.10, *cnt_raw* updates from $N$ to $N+1$ when $\theta$ wraps around. At the previous falling edge of $\phi_{VCO}$, *cnt_prev* and *cnt_next* updates to $N$ and $N+1$, respectively. Since $f_s$ is asynchronous with respect to $\theta$, it could happen that the rising edges of $f_s$ and $\phi_{VCO}$ coincide. In this case, sampling *cnt_raw* with $f_s$ could cause ambiguity and DFF metastability. Fortunately, this only happens when $\theta$ wraps around from 29 to 0. In other words, when $\theta = 28$, 29, 0, or 1, metastability is likely to happen. Therefore, based on the value of $\theta$, *cnt_raw*, *cnt_prev* or *cnt_next* is selected. For example, if $\theta = 0$ or 1 (indicating

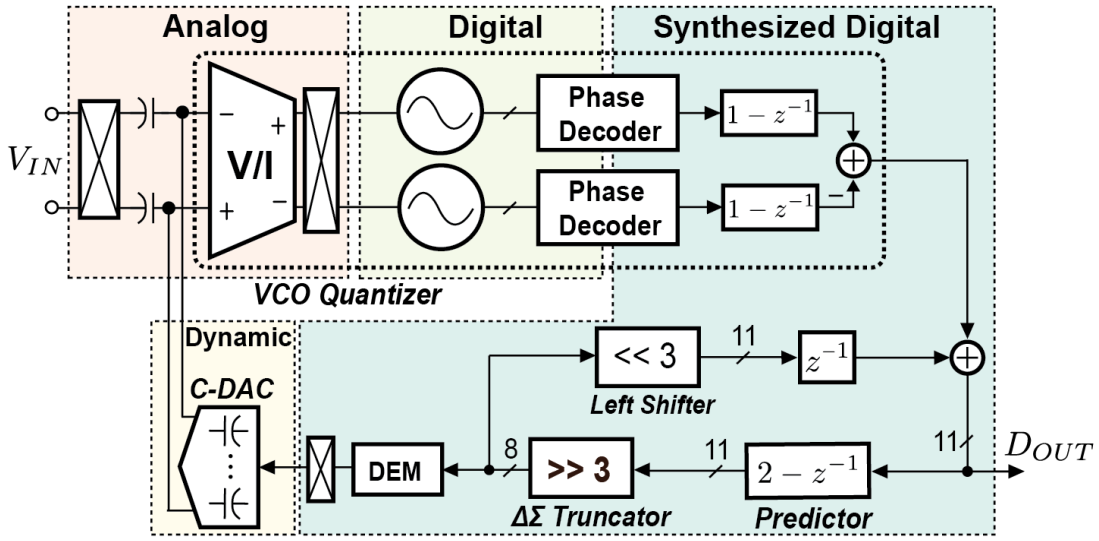



**Figure 5.11**: Partition of digital, dynamic, and analog circuitry showing a highly digital system.

the RO just enters the next $2\pi$ cycple), the multiplexer selects *cnt_next*. Similarly, if $\theta = 28$ or 29, *cnt_prev* is selected. For all other $\theta$ values, *cnt_raw* is selected because there is no danger of metastability. Since *cnt_next* and *cnt_prev* are already available at the previous falling edge of $\phi_{VCO}$, no metastability will occur.

### 5.4.3 Highly Digital System

The AFE is a highly digital system with very minimal analog circuitry. Most of the circuit blocks are dynamic if not digital, as shown in Fig. 5.11. The truncator, predictor, DEM logic, coarse phase decoder, and part of the fine phase decoder are implemented using standard digital synthesis flow. The only analog block with static current is a simple differential pair. The highly digital nature allows the AFE to be directly integrated into a low-power biomedical SoC.

## 5.5 Measurement Results

### 5.5.1 Electrical Evaluation

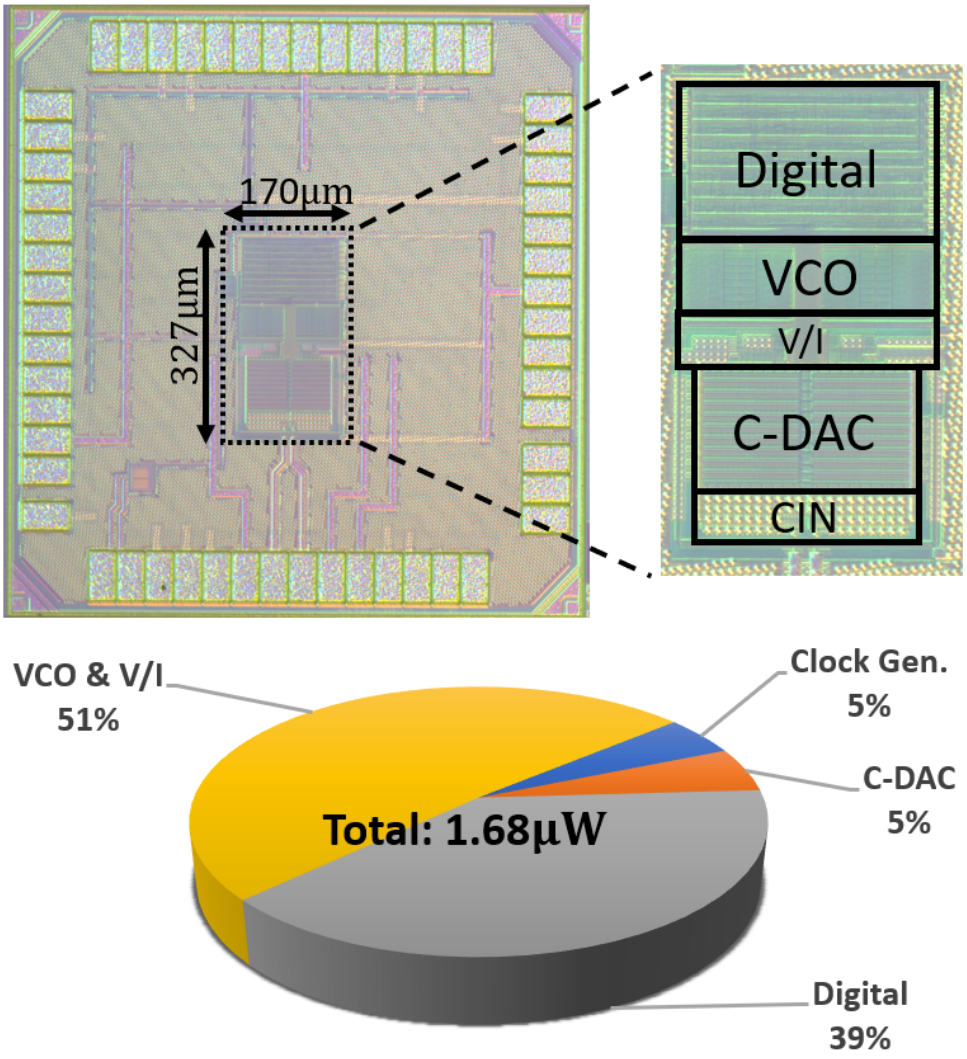



**Figure 5.12**: Chip micrograph and power breakdown of the AFE.

The prototype AFE is fabricated in a 65-nm LP process, and occupies 0.056 mm$^2$. The chip micrograph and power breakdown are shown in Fig. 5.12. The AFE draws a total of 1.68 $\mu$W of power from a single 0.8 V supply. As can be seen from Fig. 5.12, the power consumption is dominated by the V/I converter, which is also the dominant IRN contributor. The input impedance

is a function of $f_{chop}$ and $C_{IN}$ and is measured to be greater than 8 MΩ. The PSRR measured with a supply ripple of 50-$mV_{pp}$ at 60 Hz is 83 dB. The CMRR measured with a 400-$mV_{pp}$ common-mode input at 60 Hz is 97 dB.

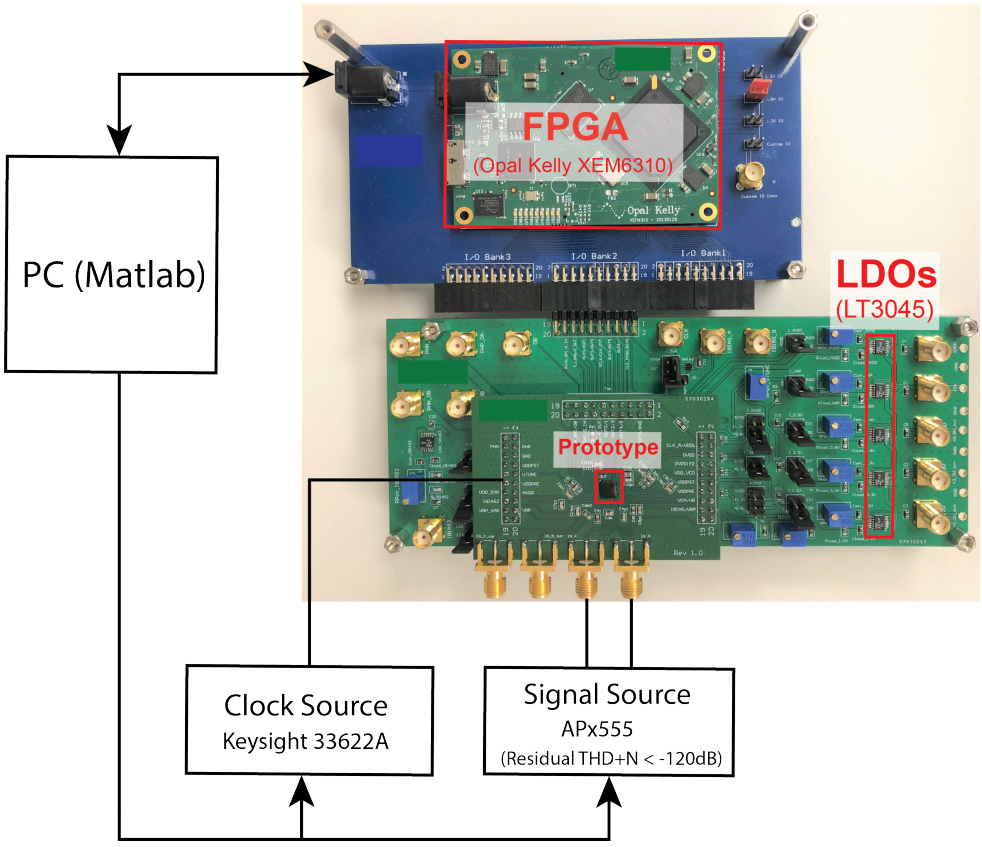



**Figure 5.13**: Output spectrum measurement setup.

The measurement setup of the output spectrum measurement is shown in Fig. 5.13. To minimize non-linearity from the signal source, an APx555 audio analyzer capable of generating a single tone specified at a residual THD+N<-120 dBc is used as the signal source. The measured output spectrum with a 460-$mV_{pp}$ sinusoidal input at 90 Hz is shown in Fig. 5.14. As can be seen, even with a 4M-point FFT, there is no measurable distortion tones, which suggests a noise-floor limited SFDR of 128 dB. In the two-tone test, two tones at 60 Hz and 105 Hz are injected to the AFE. Note that the APx555's two tone generator uses an internal DAC specified at a residual THD+N<-110 dBc, which is 10-dB higher than its single-tone generator. The resulting spectrum

is shown in Fig. 5.15, demonstrating intermodulation tones that are at least 116 dB below the signal of interest, which may in fact be limited by the test equipment. The achieved linearity here will prove very useful in facilitating artifact post-processing in ExG recording.

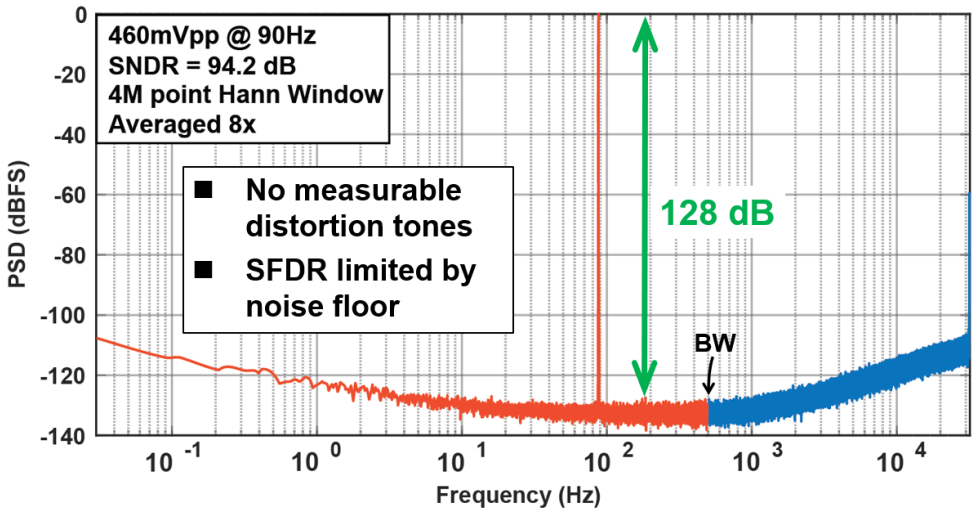



**Figure 5.14**: Measured output spectrum of the AFE showing a virtually distortion-less spectrum.

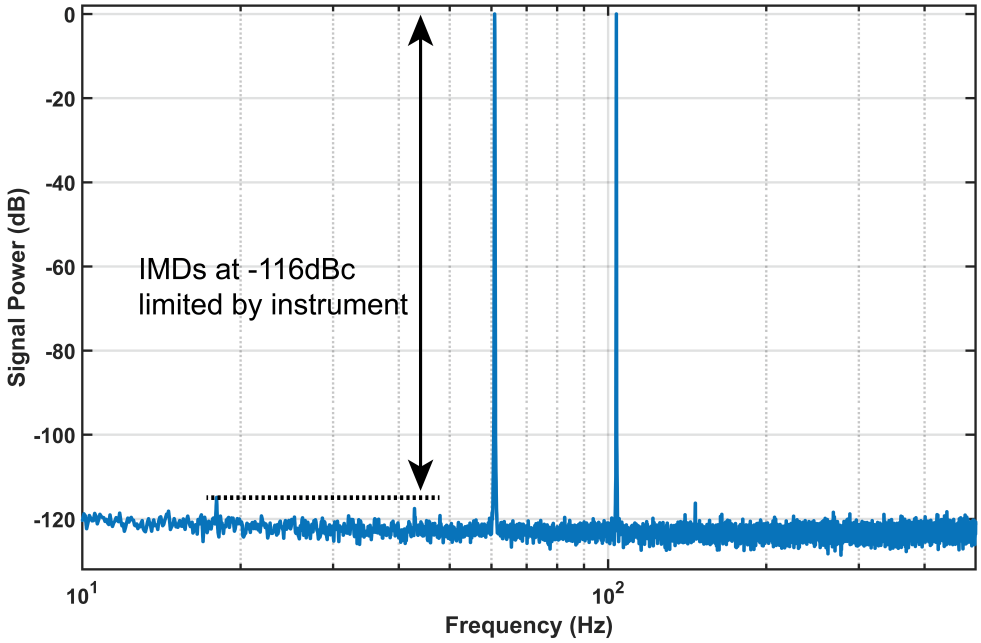



**Figure 5.15**: Measured output spectrum of the two-tone test.

The measured SNDR versus input amplitude is shown in Fig. 5.16, demonstrating a peak

SNDR of 94.2 dB and a DR of 95.1 dB. The SNDR versus different input signal frequency is shown in Fig. 5.17, which indicates little variation with input frequency. The integrated IRN over 500 Hz of bandwidth is 2.64 $\mu V_{rms}$.

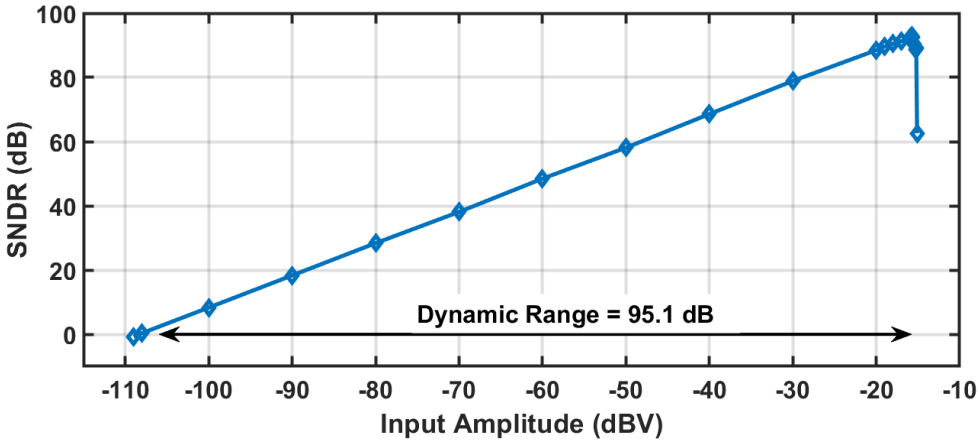



**Figure 5.16**: Measured SNDR versus input amplitude.

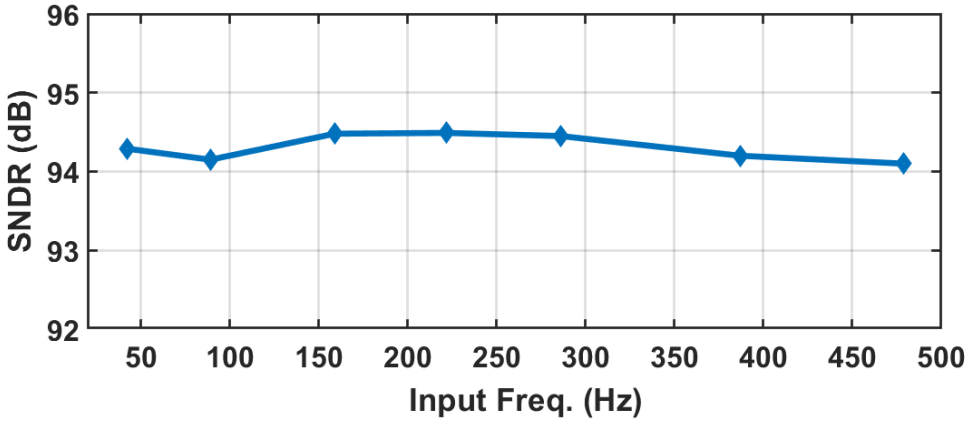



**Figure 5.17**: Measured SNDR versus input frequency.

Recall the loop dynamic plots in Fig 5.4 with varying $P_1$ path gain. To validate the analysis in measurement, $P_1$ path gain is intentionally adjusted by tuning the V/I bias current, which changes $G_{ADC}$. The resulting spectra when $P_1$ is adjusted to 0.7 and 1.3 are shown in Fig. 5.18, where close matching can be observed between the measured spectra and the theoretically predicted NTFs. In addition, the measured SNDR maintains over 92 dB for $\pm 30\%$ of $P_1$ variation

as shown in Fig 5.19, confirming the efficacy of the ΔΣ truncator even with a large path gain mismatch.

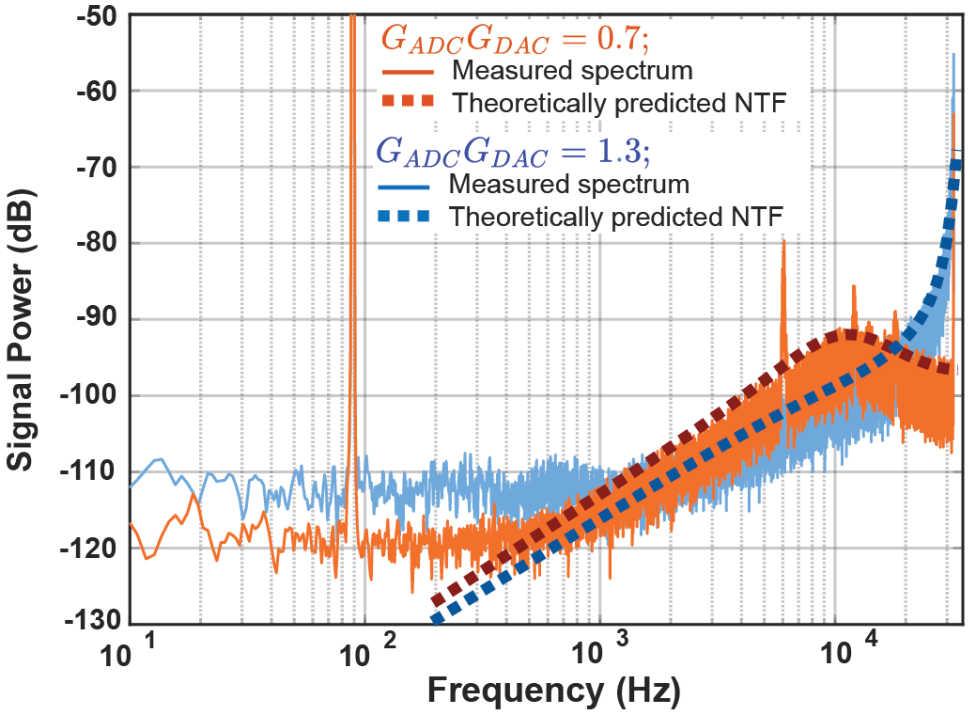



**Figure 5.18**: Measured spectra at two different $P_1$ path gains which closely match the theoretically predicted NTFs.

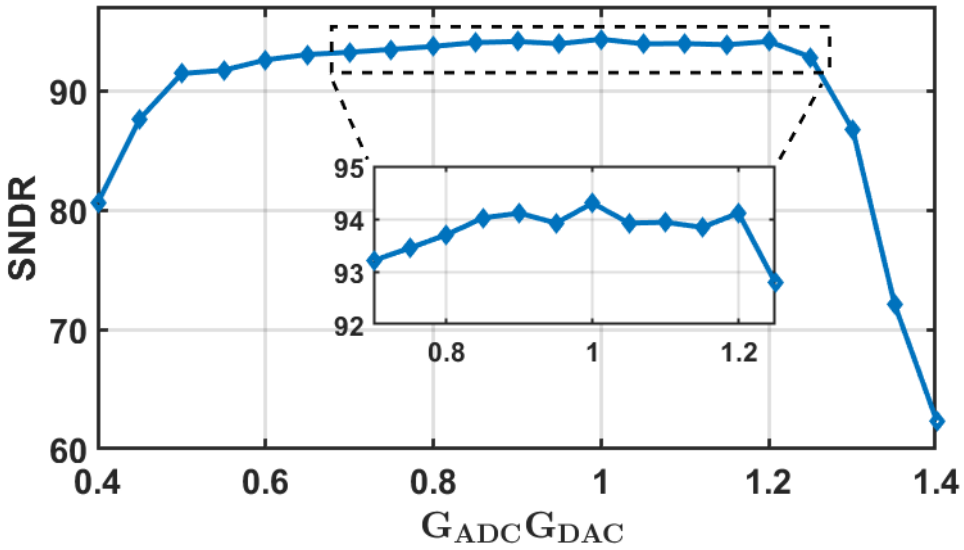



**Figure 5.19**: Measured SNDR versus varying $P_1$ path gains.

### 5.5.2 ExG Validations

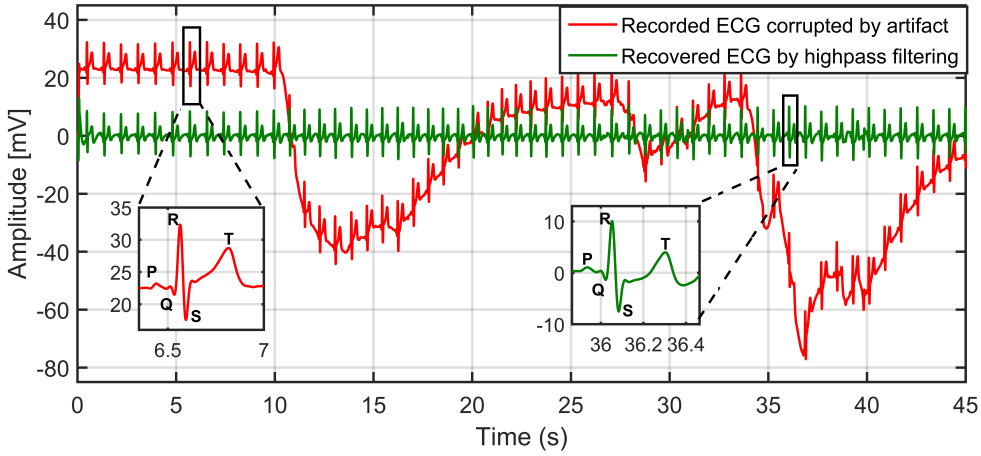



**Figure 5.20**: ECG recording corrupted by motion artifacts (red), and recovered waveform after high-pass filtering (green).

To validate the AFE in actual ExG readout applications, electrocardiogram (ECG) and electrooculogram (EOG) are performed. Specifically, motion artifacts and stimulation are introduced during the recording to demonstrate the usefulness of the AFE's wide DR and high linearity.

The ECG recording is conducted on an ambulatory human subject via a on-body three-lead configuration using 3M red dot electrodes. Two electrodes connected to the input terminals of the AFE are each attached to one arm of the subject. A third electrode served as the ground is attached to the right leg. During the recording, the subject is instructed to freely move his body (e.g., running in place, jumping, etc.) so as to intentionally induce motion artifacts. Figure 5.20 shows the recorded waveform where the red curve represents the raw ECG recording. The wide DR enables unsaturated capturing of ECG waveform corrupted by over 100 mV of motion artifact. In some regions of the curve, it can be seen that the ECG characteristics are barely recognizable. Fortunately, thanks to the high linearity of the AFE, the artifacts are easily removed by post-processing the red curve with a 3$^{rd}$-order high-pass filter. The green curve is the filtered waveform where ECG morphologies are completely recovered even in some of the most corrupted

areas.

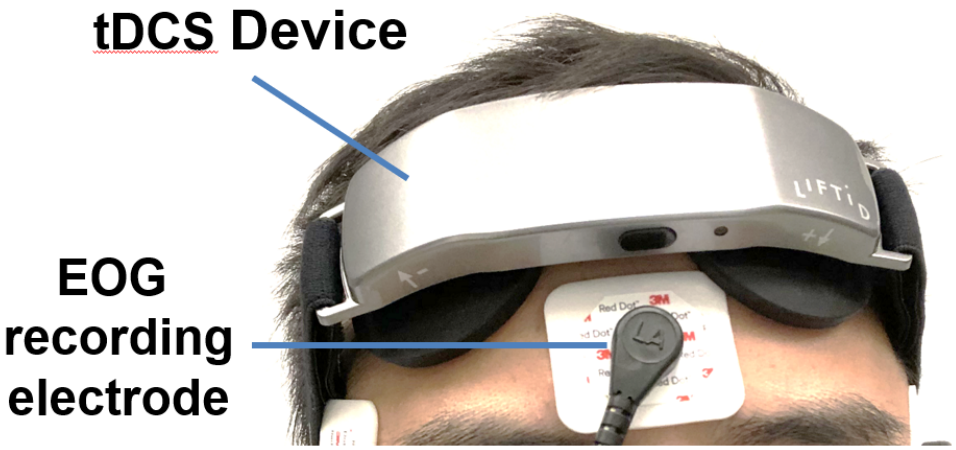



**Figure 5.21**: EOG measurement setup with the subject wearing the tDCS device.

To demonstrate recording capability under stimulation, EOG measurement is performed with the subject wearing a transcranial direct current stimulation (tDCS) device, as shown in Fig. 5.21. The tDCS device applies a constant direct current delivered via electrodes on the head. When the device turns on, there is a slow ramp up phase of the direct current. Since the tDCS device is located very close to the EOG recording site, the tDCS ramp-up serves as a stimulation artifact that disturbs EOG recording. Figure 5.22 shows the recorded EOG waveforms. The red curve is recorded with the subject closing his eyes while turning on the tDCS device. The slope is due to the tDCS stimulation current ramp-up. This recording serves as a baseline. The green curve is recorded under the same condition but now with the subject opening and moving his eyes. Some bumps and dips are visible on the green curve relative to the red. Thanks to the wide DR, EOG signal can be easily recovered by taking the difference between the red and the green, which yields the blue curve. The mV level EOG characteristics corresponding to certain eye movements such as eye gaze and eye blink are clearly identifiable.

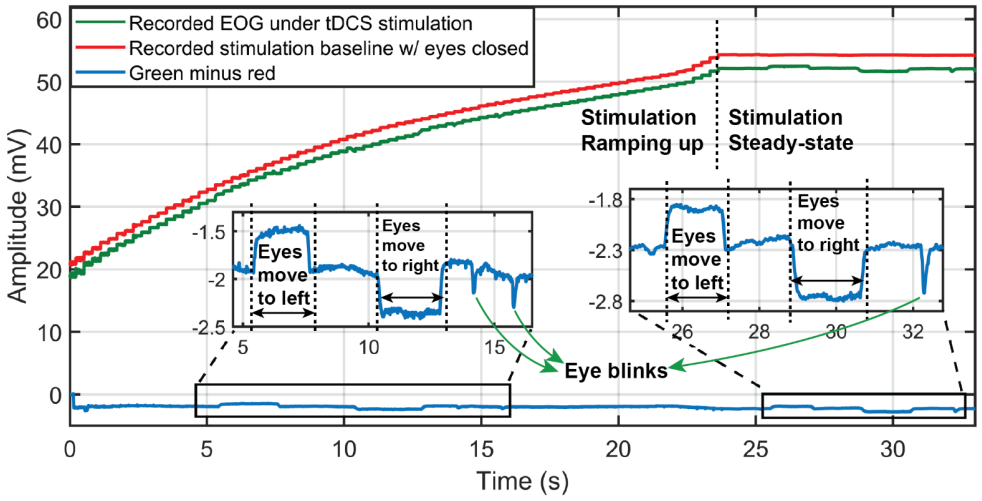



**Figure 5.22**: Two EOG recordings under tDCS stimulation ramp-up: baseline eyes-closed recording (red); and eyes-moving recording (green). EOG signal (blue) is recovered by subtracting the red curve from the green curve.

## 5.6 Comparison and Conclusion

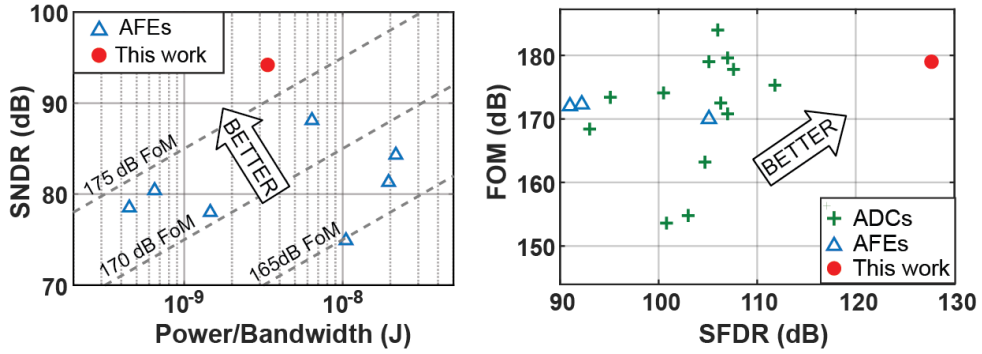



**Figure 5.23**: Survey of AFEs comparing FoM (left); and survey of both AFEs and ADCs (with $<$ 20 kHz BW) from [1] comparing FoM and SFDR (right).

Table 6.1 summarizes the performance of the AFE and compares it with other state-of-the-art AFEs for bio-sensing applications, including two voltage domain CTΔΣMs [11, 13] and four VCO-based designs [27–29, 35]. The calibration-free DPCM architecture achieves significant power savings while offering the widest linear input range of 460 $mV_{pp}$. To visually compare our work to others, Fig. 5.23 (left) compares the Schreier FoM amongst state-of-the-art AFEs. This work achieves an SNDR-based FoM of 178.9 dB, advancing state-of-the-art by 4.2 dB while

**Table 5.1**: Comparison With State-of-the-Art AFEs.

| | [13] VLSI'18 | [11] JSSC'18 | [28] JSSC'20 | [27] JSSC'20 | [29] ISSCC'21 | [35] JSSC'21 | **This Work** |
|---|---|---|---|---|---|---|---|
| **Topology** | $3^{rd}$ order CTDSM | CCIA+$3^{rd}$ order CTDSM | $2^{nd}$ order VCO-PLL Hybrid | $2^{nd}$ order VCO-based | $2^{nd}$ order VCO-based | VCO-based with DPCM | **VCO-based with DPCM** |
| **$F_s$ (Hz)** | 12.8k | 400k | 2.5M | 1.28M | 200k | 32k | **64K** |
| **Bandwidth (Hz)** | 300 | 5k | 10k | 10k | 1k | 500 | **500** |
| **Supply (V)** | 1.0 | 1.2 | 0.8(A), 0.6(D) | 1.0 | 1.2(A), 0.8(D) | 1.2(A), 0.7(D) | **0.8** |
| **Power ($\mu$W)** | 6.5 | 7.3 | 4.5 | 6.5 | 5.8 | 3.2 | **1.68** |
| **Input Range ($mV_{PP}$)** | 360 | 200 | 100 | 300 | 400 | 250 | **460** |
| **IRN ($nV/\sqrt{Hz}$)** | 265 | 90 | 36 | 95 | 110 | 53 | **118** |
| **NEF** | 26 | 8.5 | 3.5 | 9.3 | 10.1 | 4.06 | **6.58** |
| **SNDR (dB)** | 84.3 | 78 | 78.5 | 80.4 | 92.3 | 89.2 | **94.2** |
| **SFDR (dB)** | 104.7 | 81 | 91 | 92.2 | 110.3 | 112.5 | **128** |
| **DR (dB)** | 92.3 | 81 | 79 | 81 | 92.3 | 94.2 | **95.1** |
| **CMRR (dB)** | 84 | - | 83 | 76 | 89 | 98 | **97** |
| **$Z_{IN}$ (M$\Omega$)** | 39 | 1520 | 0.22 | $\infty$@DC | 60 | 4 | **8** |
| **FOM (dB)** | 160.9 | 166.4 | 172 | 172.3 | 174.7 | 171.2 | **178.9** |

FOM$=$ SNDR$+10\log($BW$/$Power$)$

offering a sufficiently high input impedance suitable for ExG recordings. Figure 5.23 (right) compares the FoM and SFDR amongst both AFEs and precision low speed ADCs from [1]. Not only does this work compares favorably against other ADCs in terms of FoM, it also clearly stands out against both AFEs and ADCs when it comes to SFDR, demonstrating an ultra high linearity with a VCO-based structure.

An ADC-direct VCO-based AFE for ExG readout applications is presented in this chapter. Based upon the calibration-free DPCM architecture, VCO nonlinear V-F transfer is minimized by operating the VCO in the small signal region. A significant digital power saving is achieved thanks to the absence of gain calibration made possible by the $\Delta\Sigma$ truncator allowing a wide range of path gain mismatch. The coarse-fine phase decoder enables a boosted SQNR while the resampling technique avoids metastability issues from combining coarse and fine phase. A single 0.8 V supply with no dedicated analog supply and a mostly digital structure enable direct integration into biomedical SoC. As a result, a state-of-the-art FoM of 178.9 dB is achieved with a virtually distortion-less output spectrum. The wide DR and high linearity enable the AFE to record ExG signals with large motion/stimulation artifacts while offering straightforward digital

back-end post-processing to retrieve clean ExG signals.

Chapter 5, in part, is based on sections of the paper from Jiannan Huang, and Patrick P. Mercier, “A 178.9-dB FoM 128-dB SFDR VCO-Based AFE for ExG Readouts with a Calibration-Free Differential Pulse Code Modulation Technique” submitted to the IEEE Journal of Solid-State Circuits. The dissertation author is the primary investigator and author of the paper.

# Chapter 6

# A VCO-based ADC for Audio Band

## 6.1 Extending DPCM to Audio Band

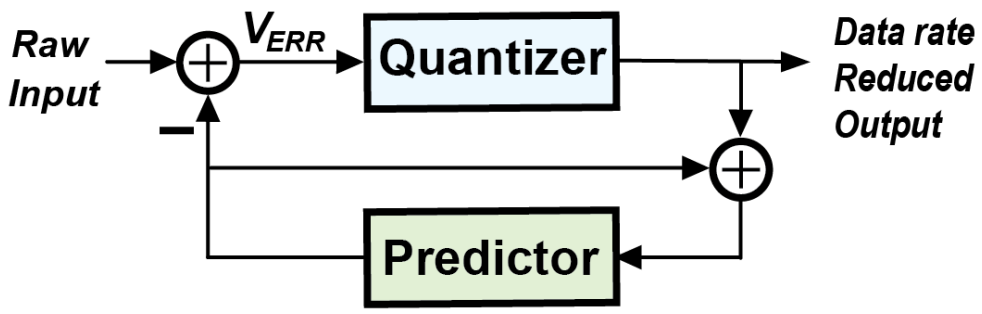
Many emerging mobile and Internet of Things (IoT) devices require digital capture of audio across a large dynamic range, with high linearity, all at low power consumption. For cost and size reasons, it is generally desirable to integrate such an analog-to-digital converter (ADC) into the same die as the main system-on-chip (SoC), which is typically implemented in a deep-submicron CMOS process with a low supply voltage. In addition, it is typically desired to operate such an SoC from a low supply voltage for energy efficiency reasons.

Although traditional $\Delta\Sigma$ modulators are able to provide a DR well above 100 dB [43], they face increasing challenges at low supply voltages and in deep-submicron processes, where the intrinsic gain and voltage headroom continue to drop. To overcome these challenges, several techniques have been proposed to improve conventional $\Delta\Sigma$ modulators. In [44], OTA-stacking was adopted to boost the noise efficiency of the fist stage integrator, but a complex 4-stage feedforward compensated amplifier is required to provide the needed 90 dB gain. Similarly, [45] used a negative-$R$-assisted integrator to reduce thermal noise. However, the mismatch between the negative-$R$ and the input resistor can lead to degraded performance.

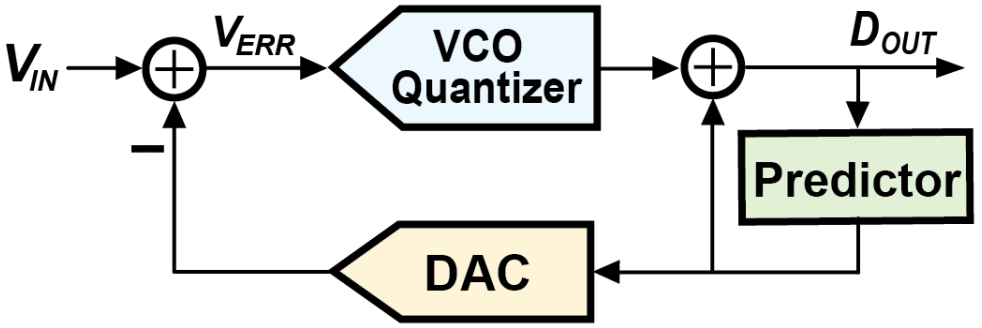
As an alternative, time domain processing techniques benefiting from scaled CMOS are gaining popularity. It is especially useful in facilitating large SoC integration thanks to its mostly digital architecture. In particular, voltage-controlled oscillator (VCO)-based ADCs are attractive due to their inherent $1^{st}$-order quantization noise shaping property [46]. VCOs, however, exhibit a nonlinear voltage-to-frequency (V-to-F) transfer response, which leads to distortion. Also, even in its linear range, the V-to-F gain, $K_{VCO}$, is sensitive to process, voltage, and temperature (PVT) variations.

In the literature, [46, 47] proposed VCO-based ADCs for MEMS microphones: [46] introduced a mostly digital $2^{nd}$ order noise shaping architecture offering a wide DR, while [47] employed a coarse-fine quantization technique enabling a sufficient signal-to-quantization-noise ratio (SQNR) with only a $1^{st}$ order noise shaping. However, both designs are open-loop, which suffer from the aforementioned V-to-F distortion and ultimately limit the achievable SNDR to less than 80 dB. To address this issue, the literature has recently seen adoption of the differential pulse code modulation (DPCM) architecture [35, 40], which is able to substantially reduce the signal swing seen at the VCO input, thereby significantly improving the linearity of the VCO. By using DPCM, [35, 40] demonstrated superior performance using VCOs as analog front-ends (AFE) for bio-readout applications with a bandwidth of 500 Hz.

In this chapter, we extend the use of DPCM to the audio band. In accommodating the increased speed, along with various circuit level changes, two main techniques are proposed that include: 1) a deterministic background gain calibration approach enabled by a split-ADC structure [48], which offers a much lower propagation delay and faster convergence speed; and 2) a hybrid dynamic element matching (DEM) that provides less delay and less in-band mismatch noise towards improved VCO-based ADC performance at up to 20 kHz of bandwidth.




(a)




(b)

**Figure 6.1**: (a) General DPCM block diagram, and (b) block diagram of applying DPCM to a VCO-based ADC.

## 6.2 Challenges with the Audio Band

As mentioned in Chapter 2, DPCM is a coding technique widely used to perform compression. Fig. 6.1(a) depicts the general DPCM structure, where the predictor in the feedback path exploits the correlation between adjacent input samples so that the quantizer only needs to process small prediction error, $V_{\mathrm{ERR}}$. By the same token, when applying DPCM to VCO-based ADCs as shown in Fig. 6.1(b), the VCO quantizer sees a small swing, thereby reducing the V-F distortion since now the VCO operates in the small-signal linear region.

In Chapter 2, we quantify the swing reduction that the VCO sees with the help of the discrete-time model shown in Fig. 6.2, where the VCO quantizer and DAC are replaced by gain blocks and delays. It is worth noting that there are two paths, $P_1$ and $P_2$ (highlighted in orange and purple, respectively), where the gain of $P_1$ is highly sensitive to PVT due to the VCO. Therefore, a

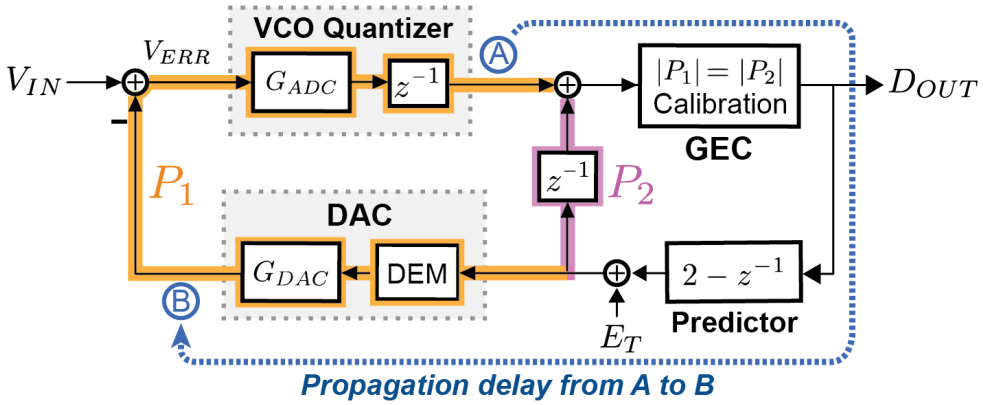



**Figure 6.2**: Discrete-time model of the VCO-based ADC with DPCM.

correlation-based gain error calibration (GEC) logic is used to ensure equal path gain magnitudes (i.e., $|P_1| = |P_2|$). Since $|P_2| = 1$, the goal of GEC is to ensure

$$|P_1| = 1. \tag{6.1}$$

Given (6.1), it was shown in [35] that the transfer function from $V_{\text{IN}}$ to $D_{\text{OUT}}$ is simply

$$\frac{D_{\text{OUT}}}{V_{\text{IN}}} = G_{\text{ADC}} z^{-1}. \tag{6.2}$$

With the predictor's response chosen to be $2 - z^{-1}$, the transfer function from $V_{\text{IN}}$ to $V_{\text{ERR}}$ is given by

$$\frac{V_{\text{ERR}}}{V_{\text{IN}}} = \left(1 - z^{-1}\right)^2, \tag{6.3}$$

which is a 2$^{\text{nd}}$-order highpass, thereby providing significant swing reduction at the VCO input (at low frequency, given a certain oversampling ratio (OSR)). For example, with 32x OSR, the swing reduction is at least 40 dB in the signal band.

To ease the feedback DAC design, [35] adopted digital truncation right before the DAC to shorten the DAC bit-width. Though relaxing the DAC's resolution requirement, the resultant truncation error, $E_T$, is introduced as shown in Fig. 6.2. Fortunately, $E_T$ travels along $P_1$ and $P_2$

with opposite polarity and equal magnitudes (as is enforced by GEC). Therefore, $E_T$ is canceled when summed at $D_{\mathrm{OUT}}$.

However, the GEC, though tracking and correcting VCO gain variation, incurs significant overhead due to the correlation-based approach involving multiple wide multipliers. This results in an extra power dissipation, a long convergence time, and, more importantly, a long propagation delay, which becomes a problem for the audio band where the clock speed is increased. This is explained as follows.

In deriving (6.2) and (6.3) using Fig. 6.2, zero propagation delay is assumed from the VCO quantizer output (node A) to the DAC output (node B). However, in practice, as is the case in [35], there are propagation delays primarily from the GEC and the DEM logic (accounting for 80% of the total delay) on the order of 150 ns. In [35], this delay is negligible as it is only 0.5% of one clock period given the 32 kHz clock speed and is taken care of by simply zeroing out the forward path during the 150 ns window. It is, nonetheless, a serious issue when porting [35] to the audio band. Assuming a reasonable clock speed of 2 MHz for the audio ADC, the 150 ns delay represents 30% of the 500 ns clock period. If we again zero out the forward path for 150 ns, we would attenuate the signal by 3.1 dB.

Reference [40] sought to address the above issues by removing GEC all together and adding noise shaping to the truncator to shape $E_T$ out of band. Although a large portion of the propagation delay is gone in such a design, the VCO gain is not corrected and is free to drift with supply and temperature at some performance penalty. While potentially not an issue for bio-readouts with well controlled ambient temperature, the variation of $K_{\mathrm{VCO}}$ must be tracked and corrected for audio applications, which require consistent high performance.

Therefore, the challenge associated with applying DPCM to the audio band is how to perform a background gain calibration to track and correct $K_{\mathrm{VCO}}$ while maintaining a small propagation delay relative to one clock period.

## 6.3 Design Architecture and Implementation

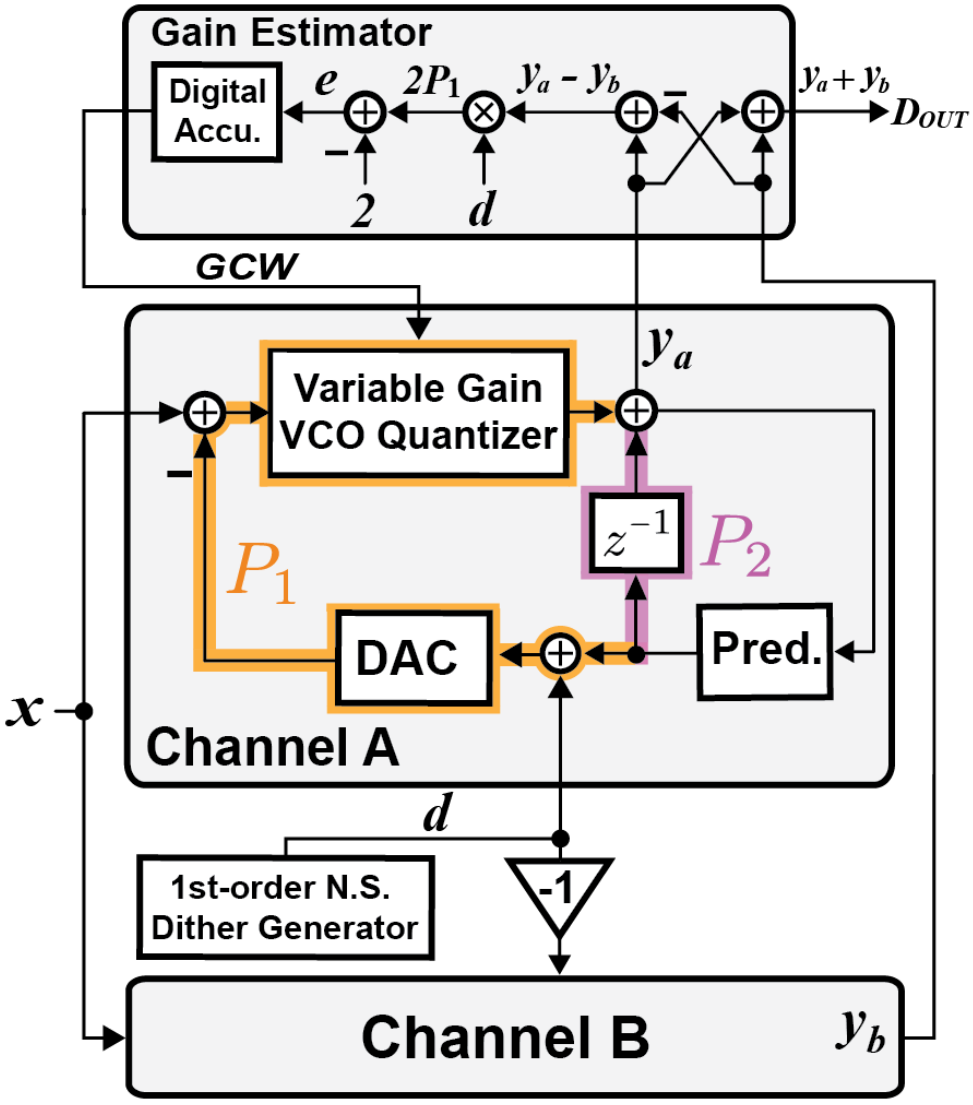



**Figure 6.3**: Split ADC architecture.

As mentioned above, the main source of delay is from the GEC and the DEM logic. In this work, a deterministic gain calibration approach using a split-ADC architecture is employed to reduce GEC delay, while a hybrid DEM is proposed to reduce the DEM delay. This section describes their respective details.

### 6.3.1 Deterministic GEC with Split-ADC

Figure 6.3 shows the split-ADC architecture where the ADC is split into two identical sub-ADCs converting the same input signal, $x$. A dither generator produces a two-level 1$^{\text{st}}$-order highpass-shaped sequence, $d$, with zero mean. $d$ is then injected to both channels with opposite polarity via a DAC. The resulting channel A and B output, $y_A$ and $y_B$, can be approximated by

$$\begin{aligned} y_A &= G_A \cdot x + P_{A1} \cdot d, \\ y_B &= G_B \cdot x - P_{B1} \cdot d, \end{aligned} \tag{6.4}$$

where $G_A$ is the sub-ADC gain of channel A and $P_{A1}$ is the $P_1$ path gain of channel A, similarly for channel B. The overall ADC output, $D_{\text{OUT}}$, is obtained by summing $y_A$ and $y_B$:

$$D_{\text{OUT}} = (G_A + G_B) \cdot x + (P_{A1} - P_{B1}) \cdot d, \tag{6.5}$$

where $d$ is largely cancelled. Thanks to $d$ being high-pass shaped, any residual $d$ due to mismatch has minimal impact on in-band SNR.

As shown in the gain estimator block in Fig. 6.3, $P_1$ gain estimation is performed by taking the difference between $y_A$ and $y_B$. Assuming matched channels, the difference is simply $2P_1 \cdot d$. Noting that $d^2 = 1$, $2P_1$ can be extracted by multiplying with $d$. Since $d$ takes only values of $\pm 1$, this multiplication is simply sign flipping. Next, recalling (6.1), the $P_1$ gain error, $e$, is obtained by subtracting 2. Finally, a digital accumulator integrates $e$ and generates a gain control word (GCW) to adjust $K_{\text{VCO}}$ of the variable gain VCO quantizer.

In practice, mismatch exists between the two channels. In this case, it can be shown that $e$ is given by

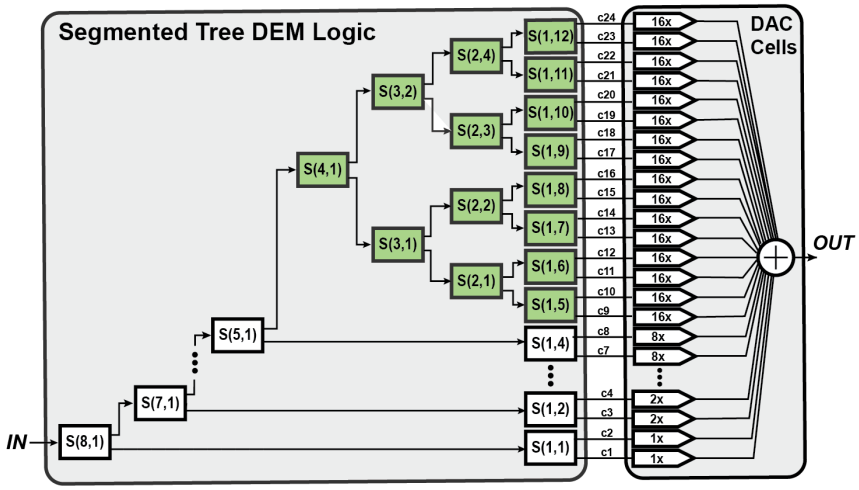
$$e = \Delta G \cdot x \cdot d + (P_{A1} + P_{B1} - 2), \tag{6.6}$$

where $\Delta G = G_A - G_B$. Two issues exist due to mismatch. First, there are residual converted

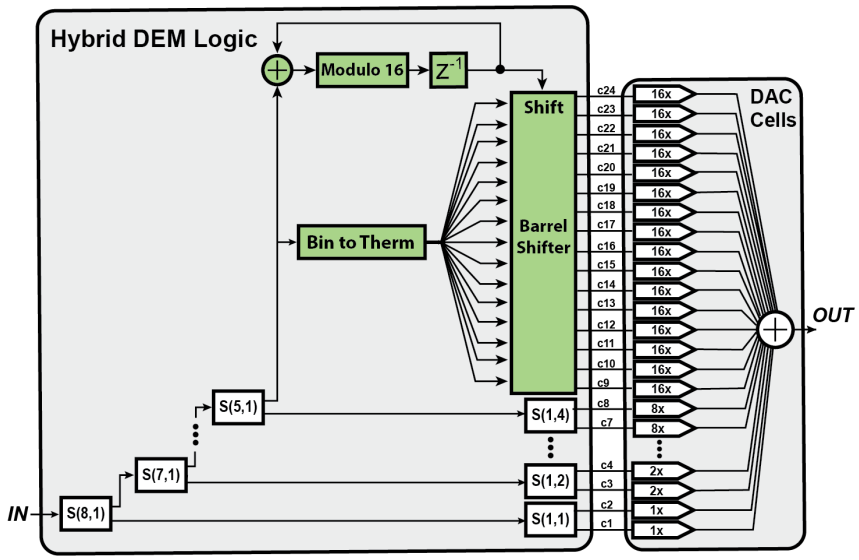
samples, $\Delta Gx$, due to incomplete subtraction. Fortunately, Monte Carlo simulation shows a $3\sigma$ channel gain mismatch of 2.3%. Therefore, $\Delta Gx$ is very small in amplitude and is readily de-correlated out. Second, the estimator is indifferent to the $P_1$ gain of individual channel and only sees the averaged $P_1$ of the two channels, as can be seen in the second term of (6.6). This causes the estimator to converge to the mean of the two channels' $P_1$. This, however, is also a minor issue thanks to the small mismatch between channels.

With this GEC approach, the calibration is taken out of the sub-ADCs, adding no delay to the inner loops while desirably maintaining operation in the background. In addition, the split-ADC architecture enables great reduction of convergence time by significantly reducing the magnitude of the unknown ADC input signal during the calibration process. Finally, gain adjustment is performed inside the VCO, avoiding the need for hardware-expensive multiplication and division, thereby saving area and power.

### 6.3.2 Hybrid DEM




(a)




(b)

| | Propagation Delay (ns) | # Std. Cells | Area ($\mu m^2$) | Power ($\mu W$) @ 2MHz |
|---|---|---|---|---|
| **Tree** | 38.07 | 420 | 1185.1 | 1.68 |
| **Hybrid** | 23.41 | 282 | 896.4 | 1.11 |

(c)

**Figure 6.4**: (a) Segmented-tree DEM, (b) proposed hybrid DEM, and (c) key metrics comparison summary from digital synthesis reports.

In [35], a segmented-tree DEM is used to linearize the DAC, as shown in Fig. 6.4(a), which offers a 1st-order mismatch shaping while enabling much fewer control lines (24) via segmentation when compared to data weighted averaging (DWA) requiring 256 controls for an 8-bit DAC. Nonetheless, DWA is found useful when the DAC resolution is small due to its simple structure. On the other hand, the tree DEM has 8 levels of switching logics, implying long propagation delay and more logic gates. To optimize the tree DEM, a hybrid DEM is utilized, where the nonsegmenting switching logic shaded in green are replaced by a 16-bit DWA logic, as shown in Fig. 6.4(b). Combining the benefits of both worlds, the hybrid DEM offers 40% less delay while maintaining 24 control wires. Both DEMs were synthesized using digital circuit design tools, and the synthesis report indeed verifies the benefits of the hybrid DEM, as summarized in Fig. 6.4(c): lower propagration delay, area, and power. In addition, simulation shows that the hybrid DEM provides about 1dB less in-band mismatch noise, which is not surprising as DWA in theory offers 6 dB better SNDR than the tree DEM [31].

### 6.3.3 Circuit Implementation

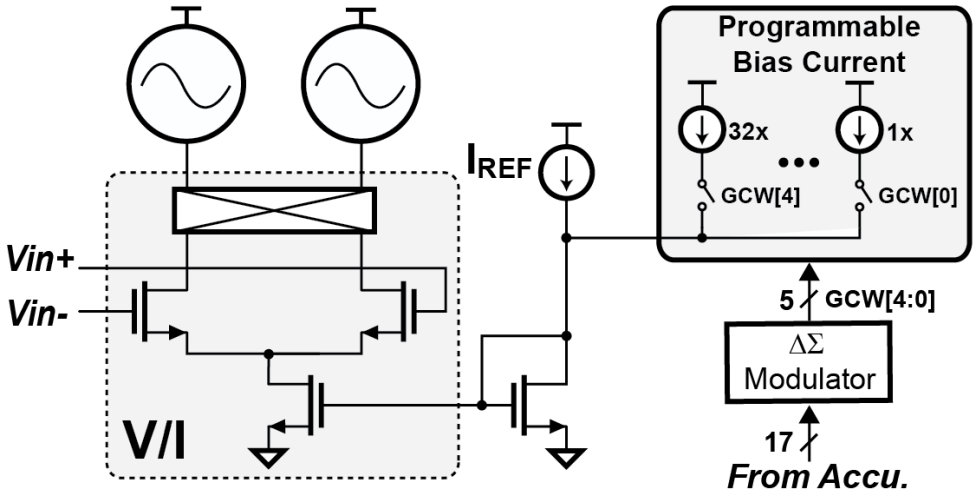



**Figure 6.5**: Schematic of the variable gain VCO quantizer.

The ADC has a signal bandwidth of 20 kHz. The sampling frequency, $f_s$, is 2 MHz,

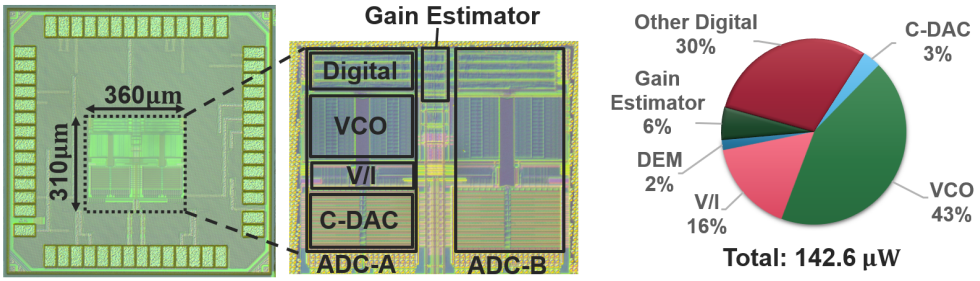


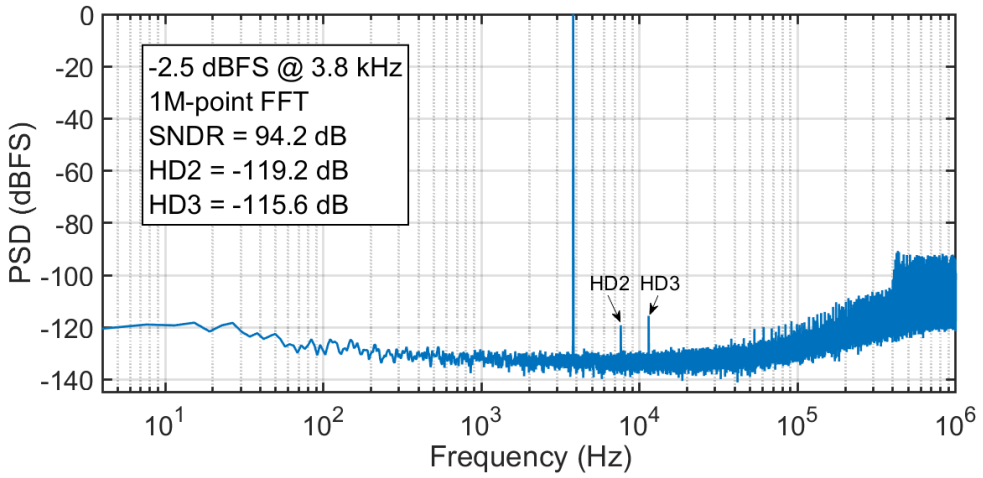

**Figure 6.6**: ADC chip micrograph and power break down.

corresponding to an OSR of 50. The proposed techniques significantly reduces the loop delay to 30 ns, accounting for only 6% of one sampling period. The sub-ADC's implementation is similar to that in [35] with a multi-tap phase decoder and a $\Delta\Sigma$ truncator. The main difference lies in the VCO quantizer, which, in this work, allows adjustable $K_{\mathrm{VCO}}$ as programmed by GCW. The $K_{\mathrm{VCO}}$ is proportional to the $G_m$ of the V/I converter [35]. Thus, as shown in Fig. 6.5, $K_{\mathrm{VCO}}$ is adjusted by tuning the bias current through the V/I converter, which in turn changes the $G_m$. The $K_{\mathrm{VCO}}$ tuning range is $\pm 40\%$ to cover a wide range of operating conditions. 5-bit tuning resolution is implemented, corresponding to a 2.5% step size, which is found to provide a good tradeoff between hardware cost and calibration artifacts. To generate the 5-bit GCW, a digital $\Delta\Sigma$M is used to modulate the 17-bit accumulator output from the gain estimator.

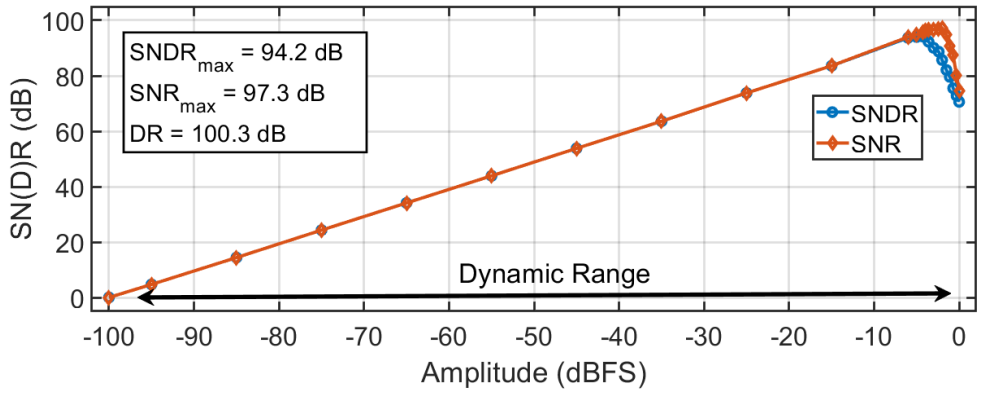
## 6.4 Measurement Results

The ADC is fabricated in a 65-nm LP process; the chip micrograph and power breakdown are shown in Fig. 6.6. It can be seen that the VCO consumes the most power because it is also the dominant noise contributor. The digital circuitry, in total, takes up 38% of power consumption, which is expected to be lower with process scaling. The two sub-ADC channels are laid out side-by-side with close proximity to improve matching. The overall active area is 0.11 $\mathrm{mm}^2$.

To minimize noise and distortion from the signal source, an audio generator (APx555b) buffered by an OPA1632 fully differential driver is used to drive the ADC. Figure 6.7 shows the




(a)




(b)

**Figure 6.7**: (a) Measured output spectrum of the ADC, (b) SN(D)R versus input amplitude.

measured output spectrum at peak SNDR and the SN(D)R versus input amplitude, demonstrating 94.2-dB SNDR and 100.3-dB DR. Thanks to the DPCM architecture, the ADC achieved 115.6 dB SFDR, which is limited by HD3. The out-of-band spurs are due to the shaped DAC mismatches by the DWA used in the hybrid DEM. Since they are out of band, there is little impact on SNDR. The PSRR measured with a 60 Hz supply ripple is 83 dB. The CMRR measured at 60 Hz with full-scale input is 76 dB.

**Table 6.1**: Performance Summary and Comparison With Prior-Arts.

| | [44] | [45] | [46] | [47] | This work |
|---|---|---|---|---|---|
| **Architecture** | DSM | DSM | VCO | VCO | **VCO** |
| **Technology** | 65 | 65 | 130 | 130 | **65** |
| **Area** | 0.39 | 0.14 | 0.04 | 0.04 | **0.11** |
| **Fs [MHz]** | 7.2 | 8 | 20 | 2.4 | **2** |
| **BW [kHz]** | 24 | 24 | 20 | 20 | **20** |
| **Supply [V]** | 1.2 | 1.2 | 1.8 | 1.2 | **1.0** |
| **Power [$\mu$W]** | 139 | 68 | 560 | 240 | **142.6** |
| **SFDR [dB]** | 113.7 | 110.2 | 60* | 85* | **115.6** |
| **SNR [dB]** | 102.0 | 94.8 | - | - | **97.3** |
| **SNDR [dB]** | 100.9 | 94.1 | 76.6 | 73.8 | **94.2** |
| **DR [dB]** | 104.8 | 98.2 | 98.5 | 97 | **100.3** |
| **FoM$_{\text{SNDR}}$ [dB]** | 183.3 | 179.5 | 152.1 | 153 | **175.7** |
| **FoM$_{\text{DR}}$ [dB]** | 187.2 | 183.6 | 174 | 176.2 | **181.8** |

$\text{FoM}_{\text{SNDR}} = \text{SNDR} + 10\log(\text{BW}/\text{Power})$

$\text{FoM}_{\text{DR}} = \text{DR} + 10\log(\text{BW}/\text{Power})$

* SFDR estimated from output spectrum.

## 6.5 Comparison and Conclusion

Table 6.1 summarizes the performance of this ADC and compares it with prior-art. Thanks to the DPCM structure, this work exhibits significantly better linearity, thereby achieving over 20-dB better SNDR-based FoM amongst VCO-based ADCs. When compared to voltage-domain $\Delta\Sigma$Ms, this work also achieves competitive performance while offering process scalability and

potentially lower supply operation not easily achieved in voltage-domain converters.

The split-ADC architecture eliminates the GEC block in the timing-critical sub-ADCs while providing a deterministic calibration approach that offers fast convergence with background operation. The hybrid DEM combines advantages from both traditional DWA and segmented-tree DEM. It enables a small propagation delay with lower power consumption and better in-band mismatch noise at the price of slight increase in out-of-band spur levels.

Chapter 6, in part, is based on the paper from Jiannan Huang, and Patrick P. Mercier, "A 94.2-dB SNDR 142.6-$\mu$W VCO-based Audio ADC with a Split-ADC Differential Pulse Code Modulation Architecture" submitted to the IEEE Solid-State Circuits Letters. The dissertation author is the primary investigator and author of the paper.

# Chapter 7

# Summary and Future Work

## 7.1 Summary of Dissertation

VCO-based quantizers have been long been proposed and widely used in the literature. Despite its attractiveness in highly scaled CMOS process, the inherent non-linear V-to-F response prevents its use in many high resolution precision applications. This dissertation presents the DPCM architecture for VCO-based ADCs that enables a virtually distortion-less output spectrum. To demonstrate the efficacy of the architecture, we have presented three prototype ICs in which two are for high DR ExG sensing application and one for precision audio application, all achieving state-of-the-art performance with ultra-low distortions.

Chapter 2 introduces the DPCM concept used to improve VCO linearity. The basic open-loop VCO quantizer is described, followed by the detailed description of the DPCM architecture applied to VCO based ADCs. In addition, considerations on relaxing the feedback path design is presented.

Another issue facing VCO-based designs is the sensitivity to PVT variations. In Chapter 3, a background gain calibration along with its implementation is presented to overcome VCO gain variation. This brings about benefits such as a simplified loop dynamics and a cancellation

of truncation error.

Based on the gain calibrated DPCM, a prototype ADC targeting bio-sensing applications with a 500 Hz signal bandwidth is presented in Chapter 4. It achieved over 90 dB of DR sufficient to simultaneously resolve both small signals and large artifacts. The calibrated DPCM architecture is adopted to limit the swing that the VCO sees, thus preserving linearity across a large input dynamic range. As a result, we achieve the lowest distortion among VCO-based sensor front-ends, demonstrating the usefulness of DPCM theory in circuit design.

Chapter 5 presents a improved second-generation version of the above. The improved performance is primarily attributed to the elimination of gain calibration, which significantly improves power efficiency. As a result, a state-of-the-art FoM of 178.9 dB is achieved with a virtually distortion-less output spectrum.

Finally, in Chapter 6, the DPCM theory is extended to the audio band where a VCO-based ADC for the audio application is presented. Necessary considerations and changes are discussed to accommodate the higher speed. Again, thanks to the DPCM structure, this prototype exhibits significantly better linearity compared to prior VCO-based audio ADCs, thereby achieving over 20-dB better SNDR-based FoM. It also offers process scalability when compared to voltage-domain ΔΣMs.

## 7.2 Areas of Future Work

There are certainly room for improvement and thus areas for future research. The DPCM technique is the primary technique used in improving the linearity of VCO-based ADCs. Though effective, there are some issues with this technique that requires future work.

To begin with, the DPCM technique so far has only been applied to low bandwidth VCO-based ADCs. There are practical difficulties that prevents its use in higher signal band as follows: As the clock frequency increases, the clock period is reduced, which leaves little time

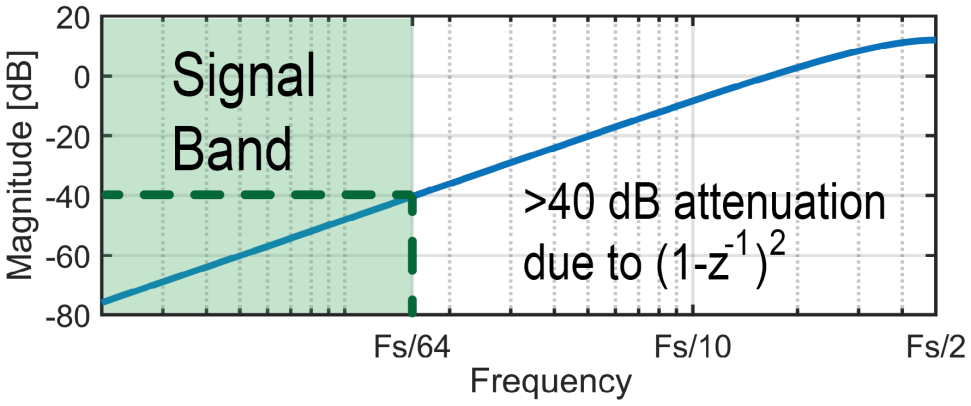



**Figure 7.1**: Magnitude plot of the $(1-z^{-1})^2$ high-pass response showing at least 40 dB attenuation in the signal band for a system with 32x OSR.

for the system to generate a feedback value. The VCO quantizer, predictor, and the DAC all have propagation delays that becomes significant as clock speed increases. In Chapter 6, some methods are proposed to reduce this propagation delay such as removing the GEC from the inner loop and adopting a hybrid DEM. However, these do not solve the problem fundamentally. Instead, similar to how excess loop delay (ELD) is compensated in a conventional ΔΣM, additional feedback branches can be considered. This requires a detailed analysis using a hybrid DT-CT model, which can be very useful in deriving a complete mathematical model for the DPCM system.

Moreover, though the DPCM architecture can reduce the amplitude of in-band signal hitting the VCO, it is less effective for out-of-band signals. Recall the second-order highpass response repeated here in (Fig. 7.1), which shows the transfer function from system input to VCO input. It can be seen that only low frequency signals are attenuated by the second order highpass response. Any high frequency components in the signal are not attenuated as much. This can potentially be a problem for ADCs used in wireless communication systems where there might be out-of-band blockers present in the ADC input. These high out-of-band blockers might be orders of magnitude higher in amplitude than the in-band signals, which could still incur significant non-linearity in the VCO. The resulting intermodulation tones could fall in-band. Therefore, possible ways to overcome this issue is worth investigating so that the DPCM techniques can be

extended to even higher frequency bands.

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