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Graphene for Future ESD Protection Circuits and Ultrasound Transducer Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Qi Chen

December 2017

Dissertation Committee:
Dr. Albert Wang, Chairperson
Dr. Ming Liu
Dr. Sheldon Tan

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Qi Chen
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The Dissertation of Qi Chen is approved:

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Committee Chairperson

University of California, Riverside

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I would like to thank the Department of Electrical and Computer Engineering at University of California, Riverside, especially the members of my dissertation committee, Dr. Ming Liu and Dr. Sheldon Tan, for their supports on my dissertation research. I would thank all my laboratory mates with whom I have conducted researches together, Fei Lu, Rui Ma, Chenkun Wang, Feilong Zhang and Cheng Li. I would also like to thank my research collaborators at University of California, Los Angeles, Dr. Wei Zhang, Jimmy Ng and Prof. Ya-Hong Xie, for the joint efforts. During our collaboration, I have learned valuable lessons from their experiences in the graphene material synthesis and device fabrication. I want to acknowledge the National Science Foundation for its support for my PhD research. I would like to express my deepest gratitude to my family. Thanks for their generous and endless love to me. They are always with me when I went through tough situations and provided encouragement and supports to me.

My research outcomes were published in IEEE Transactions of Electron Devices (TED), IEEE Electron Device Letters (EDL), Micro & Nano Letters, and several technical conferences including IEEE International Reliability Physics Symposium (IRPS) and IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS).

To my family for all the supports.

ABSTRACT OF THE DISSERTATION

Graphene for Future ESD Protection Circuits and Ultrasound Transducer Applications

by

Qi Chen

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, December 2017
Dr. Albert Wang, Chairperson

Electrostatic discharge (ESD) can easily damage integrated circuits (IC) and electronics systems [1-6]. It is hence imperative to investigate the ESD fundamentals and develop robust ESD protection solutions for semiconductors and ICs. Conventional on-chip ESD protection structures for ICs rely on in-Si PN-junction-based devices, which have many inherent disadvantages, making them unsuitable for future ICs at nano nodes.

Both novel ESD device structures and robust ESD interconnects are critical to on-chip ESD protection designs. In this dissertation, I report research outcomes of transient and systematic characterization of graphene ribbon (GR) used as interconnects for on-chip ESD protection circuits for future ICs. A large set of GR wires with varying and practical dimensions were fabricated using chemical vapor deposition (CVD) method and characterized by transmission line pulsing (TLP) and very fast TLP (VFTLP) measurements. This research indicates that, with its unique properties, e.g., high thermal conductivity and high current handling capability, graphene ribbons may be used as interconnects for on-chip ESD protection circuits, replacing existing aluminum and copper

metal interconnects. I also report a novel above-IC graphene-based nano-electromechanical system (gNEMS) transient switch ESD protection mechanism and structure. TLP testing confirms the new gNEMS ESD protection concept, showing dual-polarity transient ESD switching effect with a response time down to 200ps. This novel gNEMS switch is a potential ESD protection solution to realize above-Si ESD protection designs through 3D heterogeneous integration in the back end of line (BEOL) of ICs.

The third part of my PhD research was to explore using graphene to make novel ultrasound transducers. Ultrasound imaging utilizes ultrasonic acoustic waves to monitor organs and tissues, which has been widely used in biomedical diagnosis, such as in obstetrics and gynecology, cardiology, urology and cancer detection areas. Capacitive micro-machined ultrasound transducers (CMUT) are recently used for ultrasound imaging systems. CMUTs have advantages over piezoelectric micro-machined ultrasound transducers (PMUTs). CMUT can be fabricated by standard IC fabrication processes, making it possible to make high-performance, lost-cost and compact ultrasounic system-on-s-chip (SoC) for hand-held ultrasound imaging systems for various biological and medical applications. One key disadvantage of existing CMUT structures is the relatively low frequency, well below 100MHz as reported, hence, poor imaging resolution. I report the first concept of a graphene CMUT structure with a resonant frequency around/beyond 110MHz, making it possible to develop ultra-high resolution hand-held ultrasound imaging products for healthcare applications.

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Chapter 1 Introduction to Graphene

1.1 Graphene Material

Graphene [7, 8] is a flat monolayer of carbon atoms tightly packed into 2D honeycomb hexagonal lattice. It is the building blocks for other dimensional carbon-based materials.

In 2004, Andre Geim and Konstantin Novoselov from University of Manchester exfoliated the single layer graphene by micro-exfoliation method using the Scotch tape [9]. From then on, graphene has been widely researched in the material, chemical, physics and electrical engineering areas. This two dimensional graphene material exhibits exceptionally high crystal and electronic quality and reveals a cornucopia of new physics and potential applications.

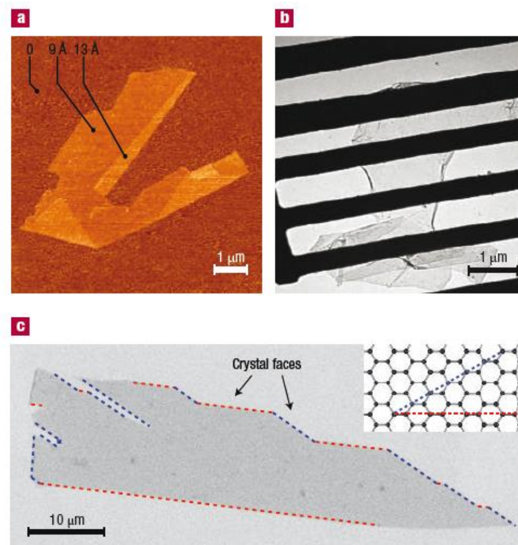


Figure 1. 1 Graphene materials under optical microscopy [7].

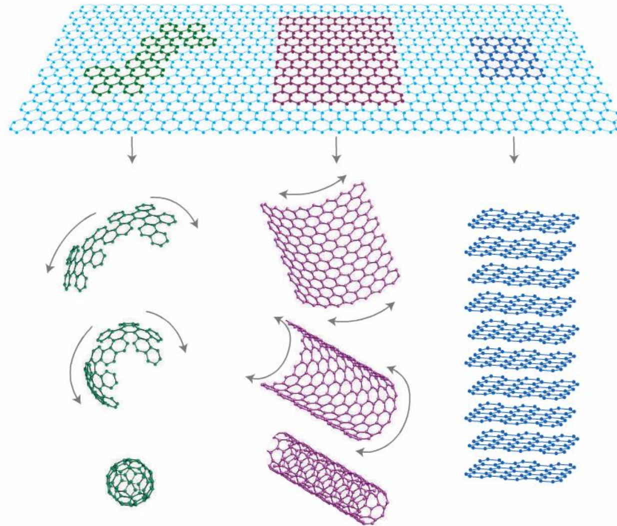


Figure 1. 2 Graphene lattice structures. It is the building blocks for other carbon allotropes. 2D graphene can be wrapped up into 0D fullerences, rolled into 1D nanotubes and stacked into 3D graphite [7].

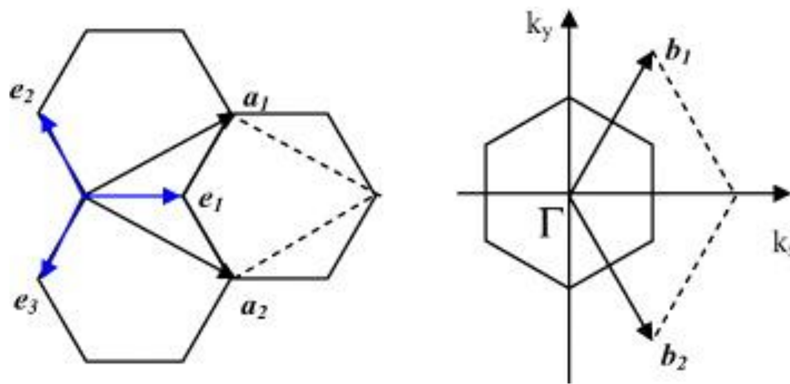


Figure 1. 3 Graphene lattice structures and primitive vectors in real space and reciprocal lattice [7].

Graphene is a flat monolayer of carbon atoms and has two-dimensional (2D) honeycomb lattice. As shown in Figure 1.3, the structure can be seen as a triangular lattice with a basis of two atoms per unit cell [40]. Carbon-carbon distance is a=1.42Å.

1.2 Graphene Synthesis

There are a few techniques [22-27] to grow graphene developed in past few years including micro-exfoliation [22], chemical vapor deposition (CVD) [23-25], epitaxial growth, chemical reactions and so on.

Mechanical exfoliation, also known as the "scotch tape method," is the most well-known way of producing graphene. Graphene can be exfoliated by simply folding Scotch tape by several times until it reaches to one atomic layer thickness. There are several pros for micro-exfoliated graphene membranes, the technique is simple and low cost and compared with CVD grown graphene, it has better material quality, as a result, this method is widely used in academic researches. However, there are some drawbacks (Table 1.1), usually the exfoliated graphene flakes has small size and irregular shapes, so it is not suitable for the commericial high-end electric applications.

Table 1. 1 Pros and Cons for the micro-exfolation method to produce graphene.

Pros	Cons
Simple; Scotch-tape	Small size (up to tens of microns)
Low-cost	Irregular shapes
Better quality (vs. CVD)	Azimuthal orientation is not well controlled
Academic researches	Not use for commercial high-end electronic applications

In this project, we use chemical vapor deposition (CVD) method to produce graphene. Compared with micro-exfoliation method, which uses a strip of Scotch tape to exfoliate graphene, it has several pros, we can use CVD method to grow large scale of graphene flakes, so it can be used in large area applications. The CVD grown graphene is structurally coherent. However, the CVD method also has several drawbacks, such as the CVD membrane has multi-domain structures and grain boundaries, so the quality of graphene is degraded and has lower conductivity. Besides, a transfer process is needed for the device fabrications, so the process is complicated and high cost.

Table 1. 2 Pros and Cons for the CVD method to produce graphene.

Pros	Cons
Large scale production	Graphene transfer needed, quality degraded
Large area applications (transparent electrode)	Multi-domain structure, lower quality, effects of grain boundaries, lower conductivity
Structurally coherent	High-cost

1.3 Graphene Properties

Graphene is a two-dimensional material with exceptional mechanical and electronic properties [9, 10, 40]. The graphene material has outstanding physical properties. For electrical properties, the graphene has unique ambipolar transportation properties, meaning that graphene can be controlled by external voltages as electron or hole doped materials (Figure 1.4), the carrier mobility μ can exceed 15,000 cm^2/Vs even under ambient

conditions [9]. In addition, graphene is one of the strongest materials in the world and the Young's modulus of can achieve up to 1 TPa. Furthermore, monolayer of graphene can transmit 97.7% of the light [7], so the monolayer graphene is semi-transparent, it can be used as large area of electrodes for solar cells and photo conductors.

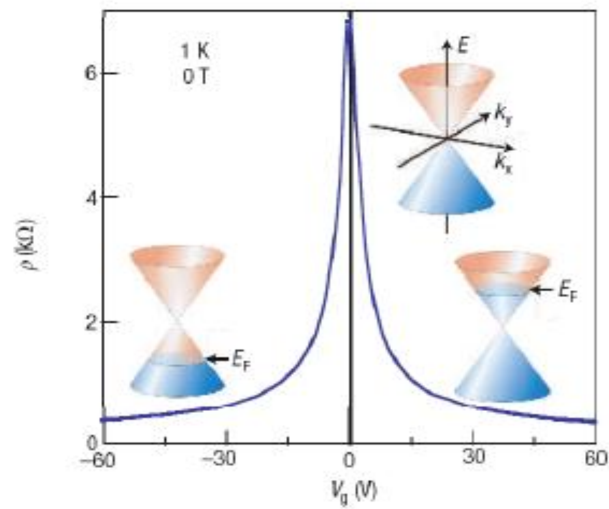


Figure 1. 4 Ambipolar transportation in graphene [8].

1.4 Graphene Applications

Graphene has shown wide range of applications including interconnects [11, 12], integrated circuits [9], MEMS and NEMS sensors and resonators [41-43], optoelectronics [7], electrodes and flexible flat panels [8]. It is very promising for the next generation semiconductor technologies.

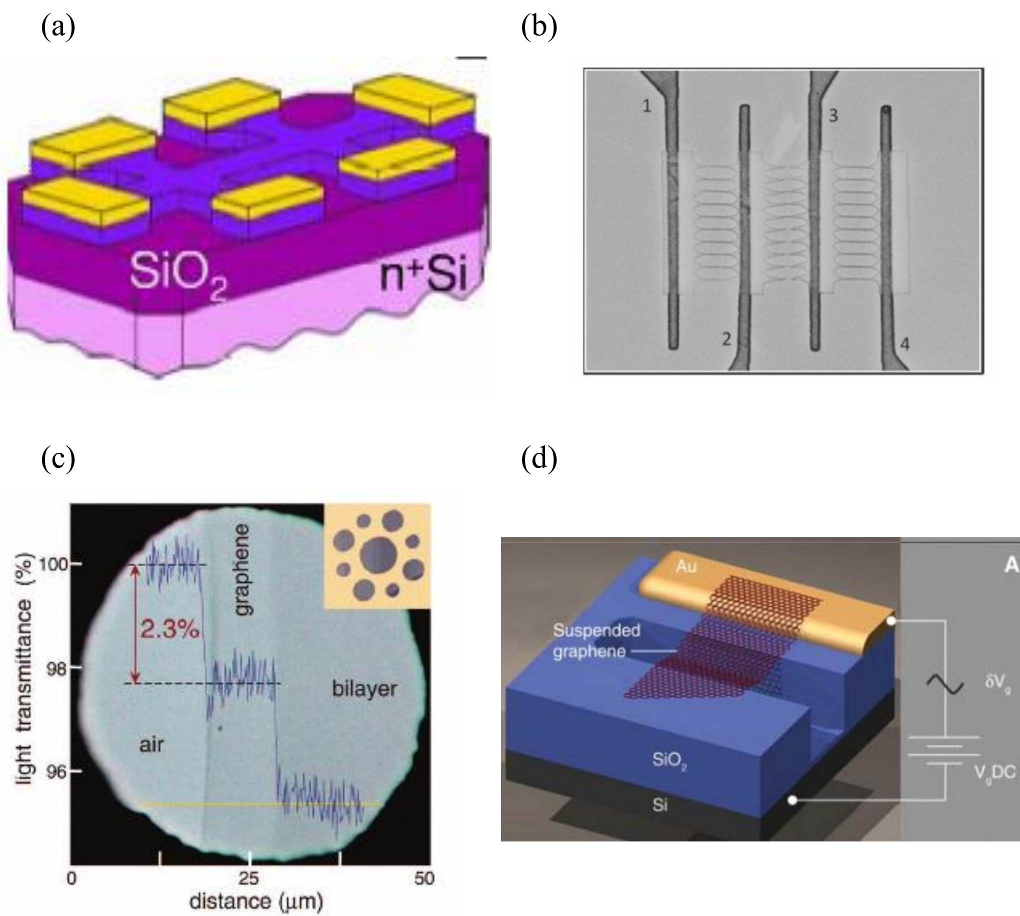


Figure 1. 5 Graphene applications for (a) transistors [9], (b) interconnects [11], (c) electrodes [8] and (d) resonators [41].

1.5 Graphene for ESD Protection Circuits

The ultimate solutions to the technical challenges of ESD protection design for advanced CMOS ICs shall be a new breed of ESD protection mechanisms and structures, which feature orders of magnitude lower leakage and parasitics, excellent current surge handling capability and sufficiently fast response time. We propose two transformative grapheme-based ESD protection solutions: 1) graphene ESD interconnects; 2) graphene nano-electromechanical system (NEMS) ESD switch device.

Graphene [7, 8], with its one atomic layer thickness and 3-5 orders of magnitude higher electron mobility [9] over that of any metal, is in many senses the thinnest and the most conductive membrane, which is ideal for ESD discharging. The high carrier mobility and possible doping-improved carrier density properties shall be ideal to achieving extremely low ESD discharging R_{ON} and to eliminating the devastating ESD overheating problem. The thin layer results in the smallest mass per unit area of any membrane achievable and thus the fastest response time of an NEMS switch [10].

Most importantly, the new NEMS ESD interconnects and switch concept is completely different from any existing ESD protection mechanisms and structures, hence, open a door to a much broader design space to achieve both robust ESD protection level and ultra-low parasitic effects, both are the primary challenges in modern ESD designs. When replacing an electronic function with mechanical means, it is important to examine the time response. The time response required for modern ESD function is on the order of 10^{-10}-10^{-9}seconds [1]. To this end, the extremely low density and the very high elastic

moduli of graphene renders the response time to be on the order of 10^{-10} second, adequate to meet the ESD requirements.

Another key advantage for graphene NEMS ESD switch is that it will eliminate the significant leakage current inherent to any existing ESD structures, which is a major technical challenge to design of ultra-low power high-reliable ICs for mobile electronics. In addition, we explored using multiple-layer graphene for optimizing the mechanical response by tailoring the rigidity and durability of grapheme ESD interconnects, and to improve ESD conductance and thus ESD current carrying capability, as well as the mechanical strength of NEMS ESD switches.

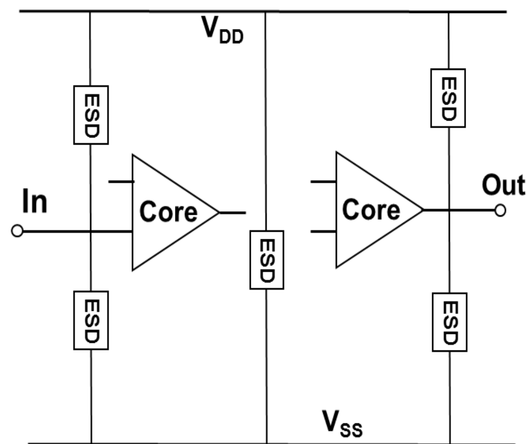
The proposed novel graphene NEMS ESD switch concept offers a revolutionary solution to the most challenging ESD design problem today. Our new graphene NEMS ESD switch concept is completely different from any reported PN junction-based devices [1-6], primarily for signal processing applications.

Chapter 2 Introduction to Electrostatic Discharge (ESD) Protection

2.1 ESD Protection for ICs

ESD (electrostatic discharge) is an extremely fast discharging phenomenon occurring when two charged objects are brought into proximity and electrostatic charges transfer in between [1]. The resulting high current (to 40Amps) and high voltage (to 20KV) may damage or degrade IC (integrated circuit) parts [1]. ESD damages consist of catastrophic and latent failures with the former causing immediate IC malfunction due to thermal breakdown or MOSFET gate dielectric rupture and the latter causing IC degradation and future failure. ESD-induced failures become one of most important reliability problems in the semiconductor IC field. According to industry statistics, ESD-induced damages account for 35-50% of all IC field failures, resulting in billions of dollars of loss annually to the IC industry [2-6].

ESD occurs when objects of different potential are brought together and electrostatic charges transfer in between, resulting in huge current (to ~500A) and voltage (to ~50kV) surges, which can easily damage integrated circuits (IC) and systems. Today, ESD failure is the most devastating reliability problem to ICs, accounting for up to 50% of total failures and causing the industry billions of dollars annually [1]. It is hence imperative to investigate the ESD fundamentals and develop robust ESD protection solutions for sub-45nm technologies. In general, ESD damages include hard and soft failures with the former causing immediate IC malfunction due to overheating by the huge current transients or dielectric breakdown induced by the large voltage surges, while the latter resulting in unpredictable lifetime problem [2, 3].



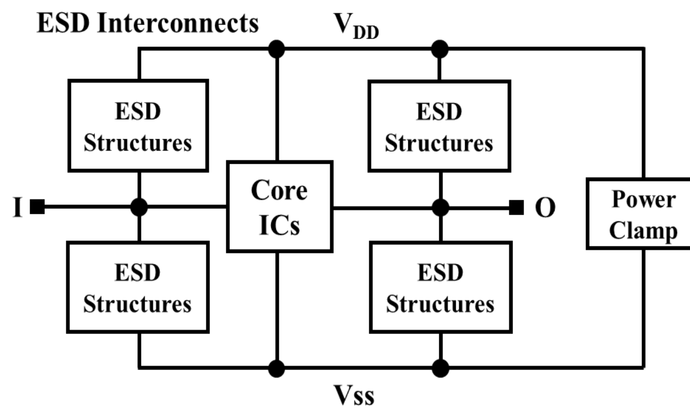


Figure 2. 1 Complete full-chip ESD protections including ESD structures and ESD interconnect at each pin against all possible ESD stressing modes.

As IC technologies continue advance into sub-100nm domain, on-chip ESD protection circuit design rapidly emerges as a major design challenge, particularly for parasitic sensitive analog, mixed-signal (AMS) and multi-GHz RF ICs [2]. In principle, on-chip ESD protection works in the way that an ESD protection unit is connected between a pair of IC pins facing ESD stresses, e.g., I/O to ground (GND). The ESD protection structure remains off in normal IC operation. When an ESD transient appears at the I/O

pin, it will trigger the ESD protection unit and form a low-impedance conducting path to shunt the large ESD current efficiently without generating too much heat and to clamp the I/O voltage to a sufficiently low level to avoid any dielectric rupture, hence provides ESD protection.

2.2 ESD Protection Designs

ESD protection design becomes more challenging as IC technology scaling down continues to beyond-28nm era and IC complexity evolves [2, 3]. On one hand, demand for ESD robustness, especially for consumer electronics, such as smartphones, never stopped [4]. However, it is very difficult to keep the normal ESD protection level for sub-28nm technologies because the extremely small feature size means high vulnerability to ESD failures. On the other hand, the ESD-induced parasitic effects, such as capacitance (C_{ESD}), are becoming unbearable to high-performance ICs [2, 4]. Revolutionary ESD protection solution is therefore in demand [5, 6]. Figure 2.1 depicts a typical on-chip ESD protection scenario where ESD protection structures are connected to pads by metal interconnects to form low-impedance discharging paths under ESD stressing. Clearly, on-chip ESD protection depends on both the ESD protection structures and the ESD metal interconnects on a chip.

On-chip ESD protection is required for all ICs, which is typically placed at I/O and power lines to protect ICs against any ESD damages. In principle, ESD protection works in two basic ways: to provide active low-impedance (low-R_{ON}) discharging paths to shunt the huge ESD currents without over-heating and to clamp the pad-voltage to a safe

level to avoid dielectric breakdown [1]. The basic ESD protection mechanisms include the simple diode-type turn-on and efficient I-V snapback for ggNMOS and silicon controlled rectifier (SCR) [1, 2]. Figure 2.2 shows typical I-V characteristics for diode, ggNMOS and SCR.

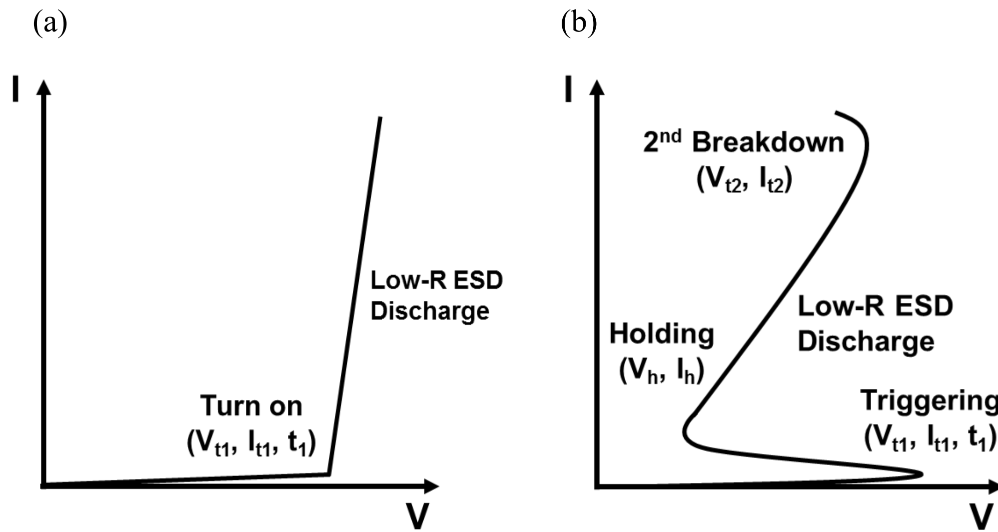


Figure 2. 2 Typical non-snapback (a) and snapback I-V (b) characteristic for an ESD protection structure where ESD-critical parameters are defined for triggering threshold (V_{t1}, I_{t1}, t_1), holding point (V_h, I_h), discharging impedance (Ron) and thermal breakdown (V_{t2}, I_{t2}).

2.3 ESD Testing Models and Equipment

ESD testing models are classified per their origins: Human body model (HBM) depicts human induced ESD failures [1-6]. Machine model (MM) describes machinery related ESD damages [1]. Charged device model (CDM) simulates extremely fast device self-induced ESD failures [1, 2]. Several *IEC* standards were adapted to simulate very fast and strong transient discharging phenomena (including ESD bursts and lightning, etc.) at both IC and system levels [1]. Alternatively, a new non-destructive transmission-line pulsing (TLP) testing model and very-fast TLP (VFTLP) model were developed to characterize instantaneous I-V behaviors under ESD stressing, which is critical to the proposed research [1-6].

Figure 2. 3 TLP and VFTLP test equipment in this study.

2.4 Motivation for Above IC ESD Protection Structure

Often, though an ESD protection structure may be designed to handle strong ESD surges, the metal interconnects may be the weak point, resulting in low ESD protection level for the whole chip. In addition, excessive ESD metal interconnects, required for robust ESD protection, introduce more parasitic effects. For typical ESD protection, the transient ESD currents can easily reach to 1.33A for basic protection level of 2kV of human body model (HBM) and 5.75A for ESD protection level of 500V per charged device model (CDM) [2]. Compared with normal current level of a few µA for ICs, the danger of metal overheating by ESD surges is obvious. Apparently, improvement over traditional Al or Cu interconnects will be critical to whole-chip ESD protection designs. From practical design view point, the maximum current handling capability data (I_{max}) provided in a foundry process design kit (PDK), typically characterized under DC and AC stressing, are over conservative for transient ESD protection designs, readily by 30X and 5X. Hence, transient ESD characterization for ESD interconnects, using TLP and VFTLP testing, is essential for real-world full-chip ESD protection designs.

Traditional in-Si PN-type ESD protection structures (Figure 2.4) have inherent disadvantages at sub-45nm and nano nodes, such as parasitic junction leakage (I_{leak}), easily being a few tens of nA for typical ESD structures and becoming intolerable to ICs at nano nodes [3-6]. It hence calls for novel ESD protection mechanisms and structures for future ICs. A revolutionary ESD protection concept may be an ideal zero-leakage mechanical switch built above Si that is triggered by ESD transients.

Successful ESD protection requires accurate design of all ESD-critical parameters, i.e., triggering voltage, current and response time (V_{t1}, I_{t1}&t_1); holding voltage and current (V_h&I_h); discharging resistance (R_{ON}); thermal breakdown voltage and current (V_{t2}&I_{t2}); etc.; in order to optimize and predict ESD protection designs on chip [1, 2].

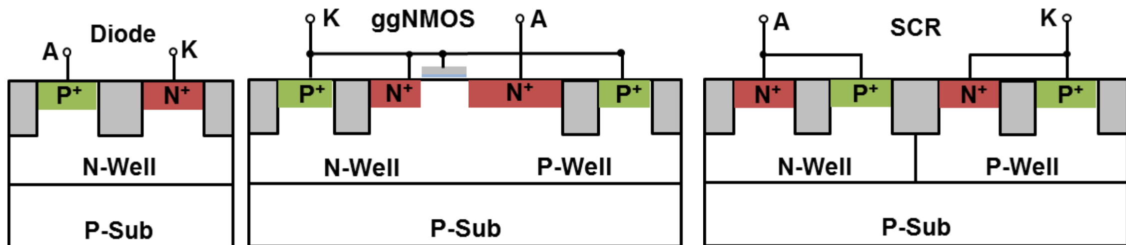


Figure 2. 4 Typical ESD protection structures including diode, ggNMOS and SCR.

Chapter 3 Graphene ESD Interconnects

3.1 Motivation

Graphene is considered as a potential replacement for metal interconnects of ICs due to its unique properties [7, 8]: First, graphene has high carrier mobility and current handling capability, i.e., I_{max}~10^8A/cm^2, which is about 10 times higher than Cu [11]. Second, graphene features exceptional thermal conductivity, i.e., (κ=4.84~5.30×10^3W/m·K), being about 13X that of Cu [12], which can effectively suppress the troublesome overheating effect in metal interconnects. Third, extraordinary mechanical strength qualifies graphene as reliable interconnects. While these superb material properties make graphene attractive for IC interconnects, they are even more interesting to ESD interconnects. The high I_{max} of GR makes it not only more suitable for robust ESD protection, but also possible for using much less interconnect coverage, readily being 10X less, for a given ESD protection target. The latter translates into much lower parasitic C_{ESD} and small layout area, both are critical to advanced ICs at nano nodes [2]. For ESD protection, the high thermal conductivity means much reduced overheating under ESD stressing. Additionally, graphene film may be used as a heat spreader around an ESD protection structure to rapidly spread out the ESD-induced heat, hence, greatly reduce the possibility of ESD-induced hot spot effect that is the root cause to ESD thermal failure because Si is poor in thermal conduction, especially under VFTLP ESD stressing. The outstanding mechanical strength also makes GR a perfect candidate for interconnects, which is often a weak point for on-chip ESD protection. Nevertheless, to qualify GR as ESD interconnects, a systematic and statistical transient ESD characterization is required.

While graphene materials have been widely studied for various electronic applications, there is little report on transient characterization of GR for ESD protection, not to mention any comprehensive and statistical studies. Graphene sheet resistance and contact resistance with metal pads have been studied in [13, 14]. GR failure mechanisms, including Joule heating and graphene oxidation, and reliability analysis were reported in [15, 16]. [17, 18] report small signal modeling for graphene interconnects. Hybrid interconnects with graphene were reported [19, 20]. More recently, exfoliated graphene ribbon characterized by TLP testing was reported [21], which, however, has several limitations: It was essentially a one-device characterization of 15 different GR samples, each having different dimensions (length, L; width, W; and number of layers, N). Second, the GR samples used have impractical small dimensions of L=2.4-5.5μm and/or W=0.6-15μm. Third, the method used for stability/repeatability study, i.e., stressed by 1200 pulses, was TLP pulses with increased pulse heights (by stepping up with a ΔV) within one full TLP sweeping cycle (two full TLP sweeping routines used up to right before reaching to the thermal breakdown current threshold, i.e., I_{t2}, in typical TLP testing). We believe that this technique is insufficient for true reliability characterization, which should be done by repeating the full TLP sweeping cycles, each consists of numerous number of TLP pulses with increased ΔV. Fourth, the single-device testing data reported, while interesting, are not very useful, especially considering that the GR samples used were too short and narrow, which may over-estimate GR properties because graphene film quality of large dimensions (needed for any practical applications) are still very unstable using current fabrication.

3.2 Graphene ESD Interconnects

3.2.1 Structure and Operation Mechanisms

Figure 3.1 illustrates a conceptual on-chip ESD protection scenario using GR interconnects. GR wires connect ESD structures with pads. During ESD events, large ESD transients will discharge through GR interconnects and ESD devices. Hence, the GR interconnects must survive the ESD surges.

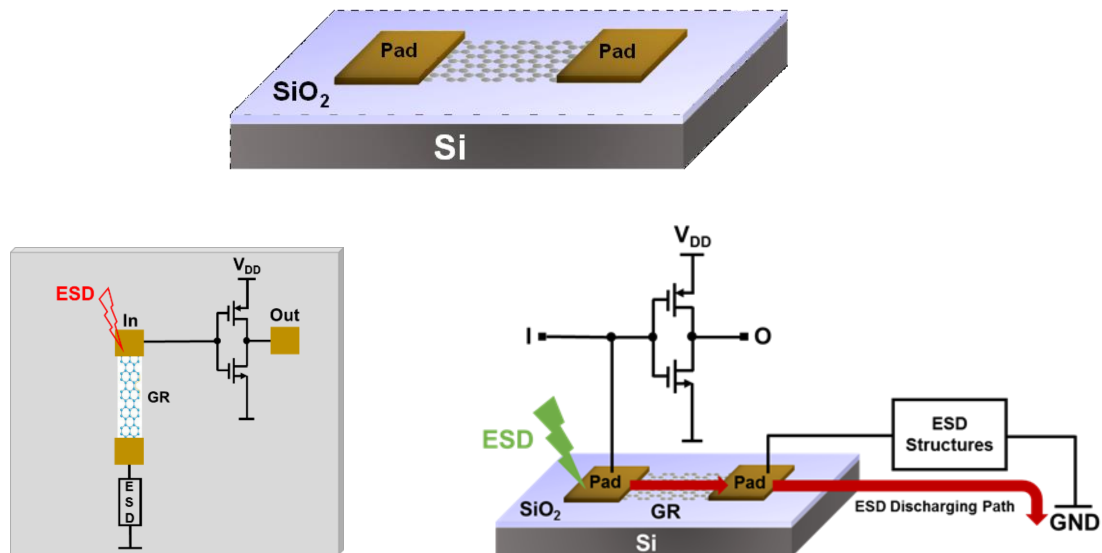


Figure 3. 1 A conceptual on-chip ESD protection scenario using GR interconnects. GR wires connect ESD structures with pads. During ESD events, large ESD transients will discharge through GR interconnects and ESD devices. Hence, the GR interconnects must survive the ESD surges.

3.2.2 Fabrication

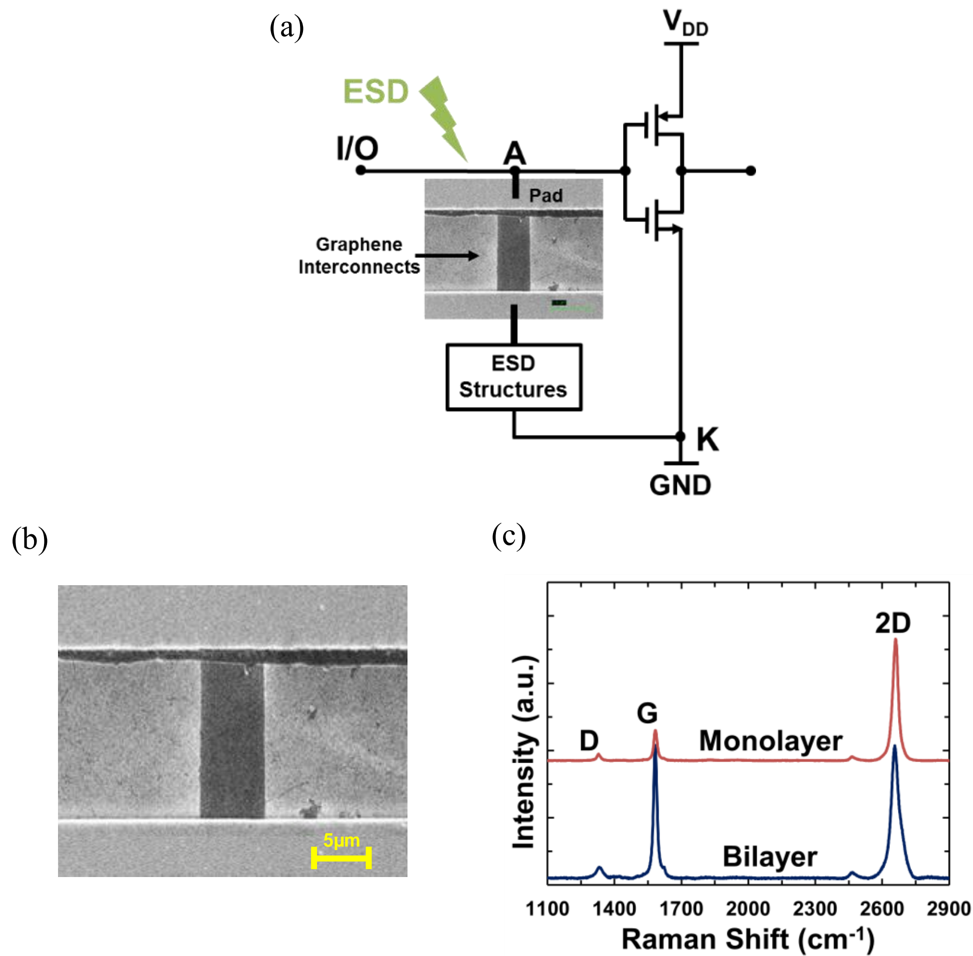


Figure 3. 2 (a) Graphene ESD interconnects protection mechanisms. (b) SEM image of a bilayer GR wire (vertical dark stripe) of L=12µm and W=5µm. (c) Raman spectrums for monolayer and bilayer GR samples where G peak reveals number of graphene layers [28, 29].

Monolayer and bilayer graphene films were grown by chemical vapor deposition (CVD) method, suitable for large area graphene fabrication for real-world ICs, where 25 micron-thick copper foil was used as the catalyst (2×2 inch square). The CVD growth was carried out at a pressure of 20 Torr with CH_4 (~20 sccm) (higher flux of ~60sccm for bilayer) and H_2 (~1000 sccm). The graphene sheets were then transferred onto SiO_2 (300nm)/Si substrates. Raman analysis was used to confirm quality and number of graphene layers grown. Graphene films were patterned by reactive plasma etching (RIE) into GR samples. Ti/Pd/Au (0.5/30/50nm) pads were deposited by E-beam evaporation. Figure 3.2 shows a fabricated GR structure and its Raman analysis.

3.3 Characterization & Discussions

3.3.1 Design Splits & Testing Conditions

For a comprehensive and statistical study of GR ESD interconnects, a large set of GR samples (~6000) were designed and fabricated. Table 3.1 summarizes the GR sample design splits in this work. Critically, long (L=9/12/22/30/50μm) and wide (W=3/5/10μm) GR wires are designed for two reasons: First, if a GR wire is too short and narrow, it may not catch material defects because the current graphene film growth process is far from mature. Second, the GR wires should have dimensions suitable for real-world ICs to ensure useful results.

Table 3. 1 A summary for GR sample design splits.

Layers	L (μm)	W (μm)	Sample number
Mono-/Bilayer	9	3/5/10	~6000
	12		
	22		
	30		
	50		

Comprehensive and systematic transient characterizations were conducted using TLP (Barth Model 4002) and VFTLP (Barth Model 4012) to emulate HBM and CDM ESD behaviors, respectively. For reliable testing results and statistical analysis, at least ten parts were tested for each sample for every testing condition. Table 3.2 summarizes the testing set-ups and conditions. The stressing pulses feature varying pulse rise time and duration, i.e., t_r = 0.2/2/10ns and t_d = 75/100/150ns for TLP testing; t_r =100/200/400ps and t_d =1/5/10ns for VFTLP mode, respectively. Two ESD zapping modes were used: The *Gradual* stressing is a traditional method that is a full-zapping cycle consisting of a series of pulses with the height increasing gradually with a step of ΔV and the zapping cycle completes when it reaches the thermal breakdown threshold. The new *Abrupt* zapping method applies a single pulse with its height corresponding to the thermal breakdown point,

which is obtained for a given GR wire in advance. Temperature effect was investigated by measurements across a wide temperature range of T = -30°C to +110°C.

Table 3. 2 A summary for TLP and VFTLP testing conditions.

Testing Conditions		Tester Set-up		
Zapping	T (°C)	Methods	t_d (ns)	t_r (ns)
Gradual/ Abrupt	-30/+110	TLP	75, 100, 150	0.2, 2, 10
		VFTLP	1, 5, 10	0.1, 0.2, 0.4

3.3.2 Graphene Resistance

The total resistance (R_T) of GR samples were first extracted by transmission line measurement [13, 14, 36], including resistance of the graphene segment (R_G) and contact resistance (R_C), as given by,

$$R_T = R_G + 2R_C + 2R_M \tag{3.1}$$

where R_M is metal pad resistance ($R_M << R_G$). From statistical analysis for measured R_T for GR wires with varying length and width, R_G and R_C can both be extracted. Figure 3.3 shows statistics for a large group of bilayer GR wires with varying length of L= 9/12/22/30/50

μm and a fixed W= 5 μm by DC testing, from which R_C≈188Ω and graphene sheet resistance of ~650Ω/□ were extracted respectively.

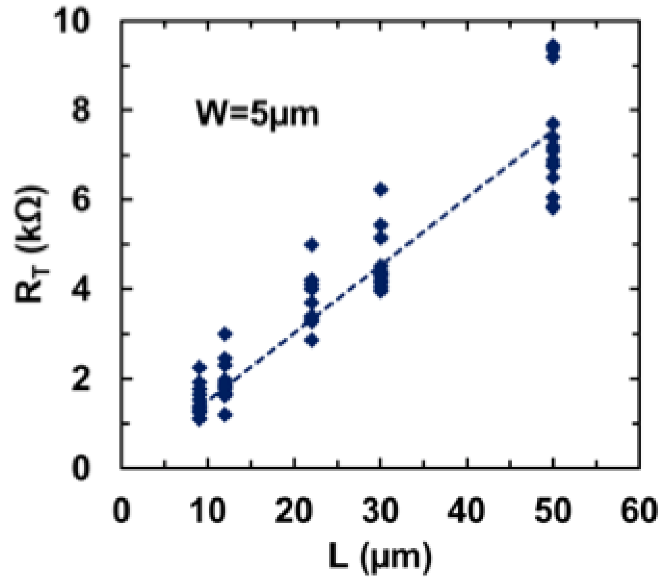
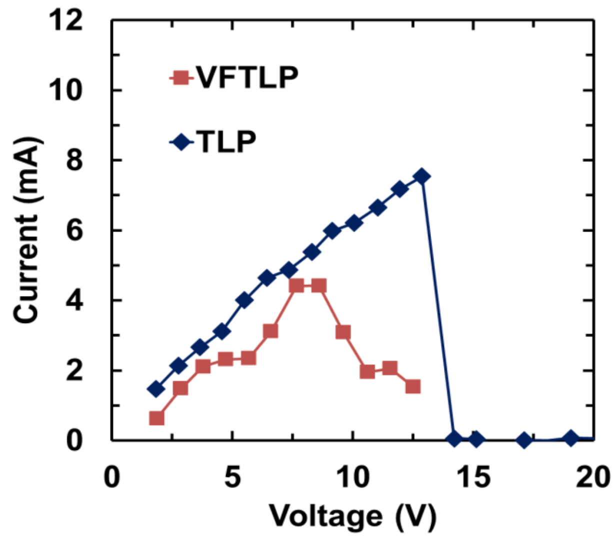


Figure 3. 3 Statistics analysis for R_T for GR wires of varying L (W=5 μm) by measured by DC stressing results in R_C ~ 188Ω and GR sheet-R ~ 650Ω/□.

3.3.3 Transient ESD Testing

The GR robustness is determined by the maximum sustainable *critical* current (I_C, or its *critical* current density, J_C) corresponding to the thermal failure point when I_C drops abruptly, and the corresponding *critical* voltage is V_C. Figure 3.4 compares transient I-V curves by TLP and VFTLP testing for a sample GR wire (L = 12μm, W = 5μm). It is observed that J_C ~ 10^8 A/cm^2 for both TLP and VFTLP is substantially higher than J_C ~10^7 A/cm^2 for DC testing [37, 38]. It is noted that the measured J_C values show a wide

distribution across samples, which may be attributed to two factors: the GR sample quality may not be well-controlled due to current graphene growth processes, especially for volume production of large size graphene films; and GR test results may be very sensitive to TLP/VFTLP testing conditions. Therefore, one should focus on statistics analysis instead of single sample.



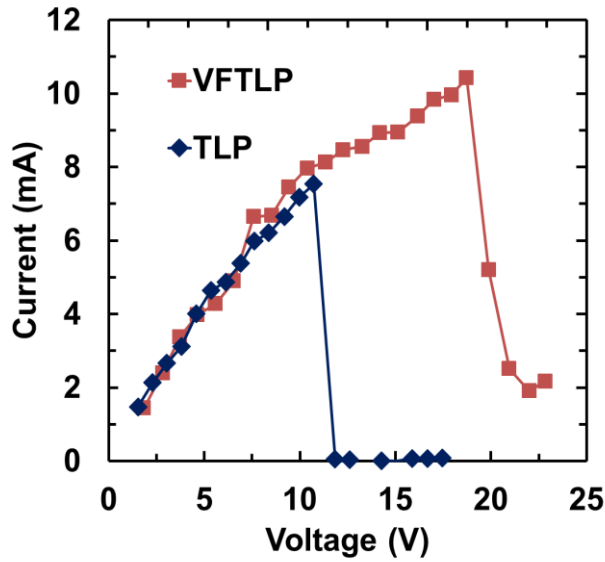


Figure 3. 4 Two typical transient I-V characteristics by TLP and VFTLP for a bilayer GR sample (L=12μm, W=5μm) at room temperature reveals ESD failure threshold (I_C) corresponding to an abrupt current drop.

3.3.4 ESD Characteristics versus GR Dimensions

GR Length

Figure 3.5 presents the measured transient I-V characteristics by TLP testing (t_r=10ns & t_d=100ns) for a set of bilayer GR samples with a fixed W= 5μm and varying L of 12/22/30/50μm. It is observed that the critical V_C increases substantially (from 10V to 35V) with increased L, which is attributed to increased resistance for longer wires.

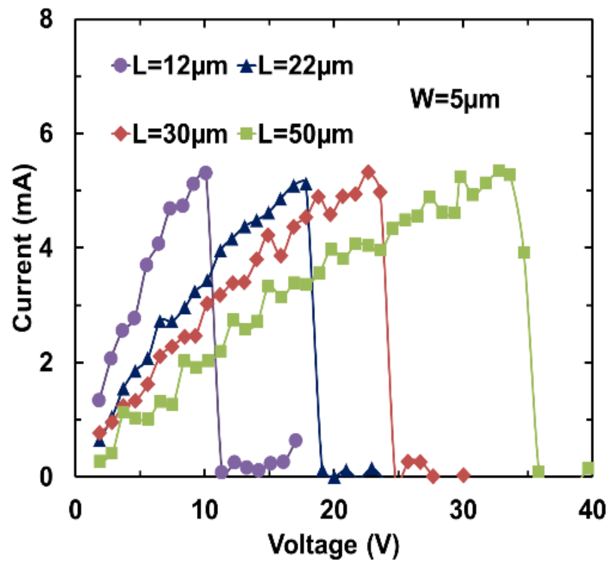


Figure 3. 5 Transient I-V curves for GR wires with varying L (fixed W=5μm) by TLP testing shows that V_C increases substantially with L.

Figure 3.6 depicts the statistical characteristics of J_C and V_C versus L (W = 3μm) for a group of GR samples by TLP testing. It is found that V_C increases monotonically for

longer L (because $V_C \propto J_C \times L$), same as in Figure 3.5. The measured J_C reaches to a very high level of ~10^8 A/cm^2, suggesting superb ESD current handling capability of GR wires. However, contrary to the belief that J_C should be independent of L, the measured statistics show slight decrease of J_C as L increases, which is attributed to possibly more defects in longer GR samples (e.g., structural and contamination) that is because the graphene quality is still a challenging issue with graphene growth processes today. A fitting equation is proposed to model this characteristic,

$$J_c \propto AL^{-B} \qquad (3.2)$$

where A and B are fitting parameters. We found that statistical analysis based on measurements of large volume of GR samples is critical to obtaining reliable and meaningful testing results, impossible if using single-sample testing approach.

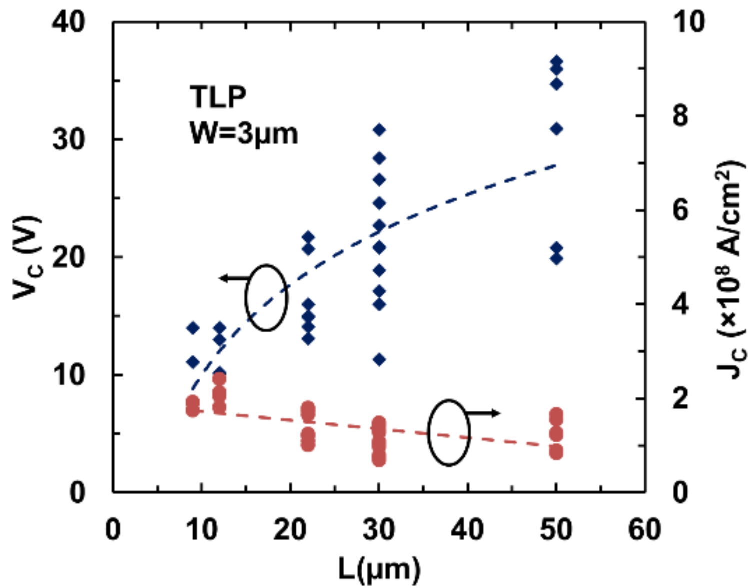


Figure 3. 6 Statistics for TLP testing results of GR samples with varying L (fixed W=3 μm) confirm that V_C increases significantly with L. However, J_C only shows little dependence on GR wire length.

Figure 3.7 depicts the statistical trends of V_C and J_C versus L for GR samples of W = 3μm measured by VFTLP testing. It is clear that V_C increases significantly as L increases due to resistance change. However, J_C seems to be almost independent of L for VFTLP testing results, as expected for high-quality graphene films, which is different from the case for TLP testing. Considering that VFTLP has a much shorter pulse duration (t_d=5ns) as opposed to t_d=100ns for TLP testing, the shorter VFTLP stressing duration may make the GR discharging less sensitive to fabrication-induced defects in GR wires.

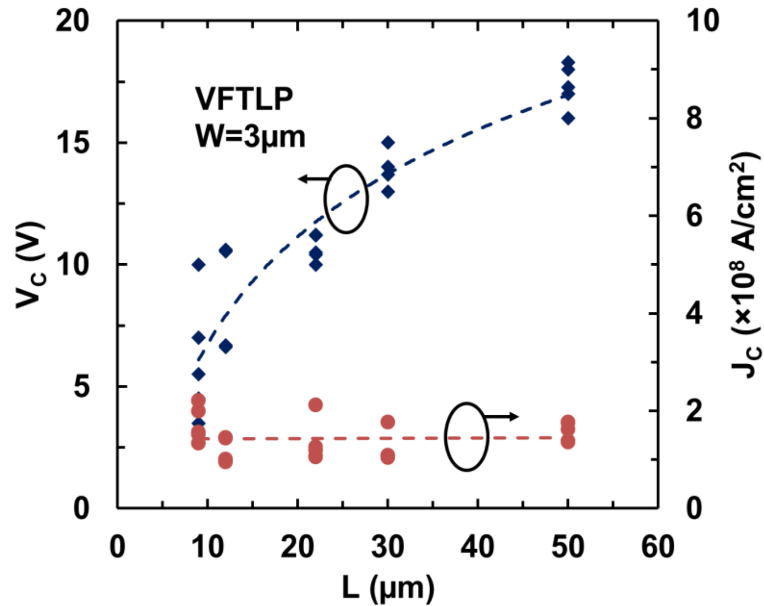


Figure 3. 7 Statistics for VFTLP results of GR wires of the same size show that V_C increases significantly with L, while J_C is almost independent of L.

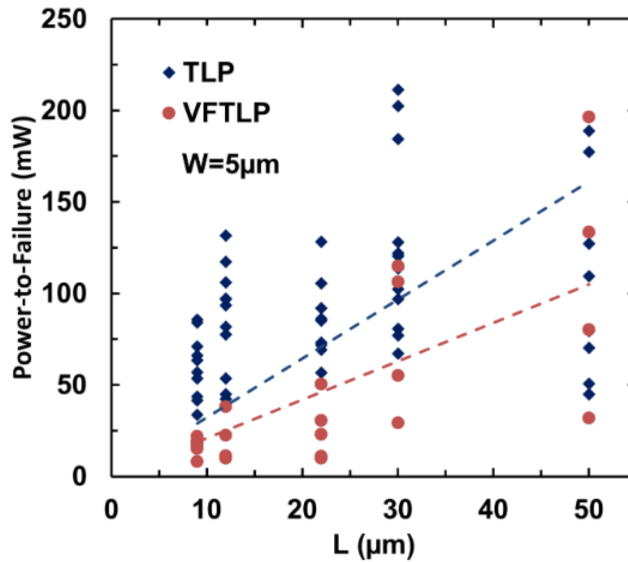


Figure 3. 8 Statistics, by TLP and VFTLP measurements, of power-to-failure of GR samples with a fixed W=5µm and varying L shows that PC increases with L.

Figure 3.8 compares the statistics data of the power-to-failure, i.e., the maximum sustainable power ($P_C=I_C \times V_C$), of GR samples with a fixed W=5µm and varying L, obtained from both TLP and VFTLP testing. It is clear that the measured P_C increases as L increases for both TLP and VFLTP results, which is again due to the increase in GR resistance. It is interesting to observe that P_C from TLP testing is clearly higher than that from VFTLP zapping (e.g. $P_C \approx$ 100mW by TLP for a GR of L=12µm and W=5µm, while $P_C \approx$ 40mW for VFTLP), which means that GR ESD interconnects may be more vulnerable to VFTLP zapping. This may be related to the fact that, considering an estimated thermal time constant of ~13ns for GR wires [17-21], thermal equilibrium in GR wires under TLP stressing may be reached, which did not occur during ultra-fast VFTLP zapping, hence, local over-heating (i.e., hot spots) occurs under VFTLP stressing that leads to a lower P_C.

Width

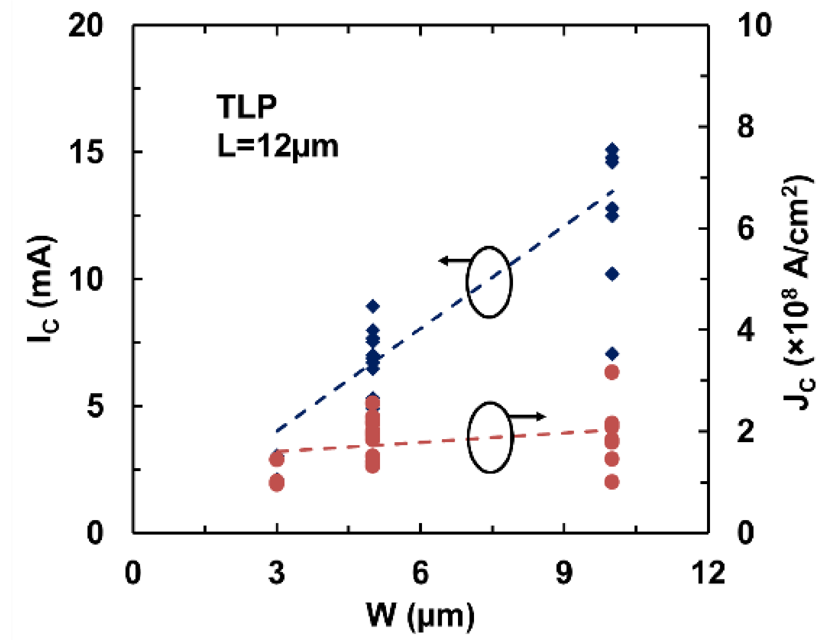


Figure 3. 9 Statistics for I_C and J_C for GR samples of a fixed L=12μm and varying W obtained by TLP (t_d=100ns, t_r=10ns) shows a clear dependence of I_C on W, however, J_C (~1.8×10^8 A/cm^2) seems to be insensitive to W.

Figure 3.9 gives measured statistical I_C/J_C ~ W behaviors for GR samples (L = 12μm) obtained by TLP testing, which shows that I_C increases almost linearly with W due to reduction in resistance as W increases. Meanwhile, J_C seems to be insensitive to W (the slight variation may be associated with changes in defects as W increases, related to processes, which is not as significant as the case with varying L).

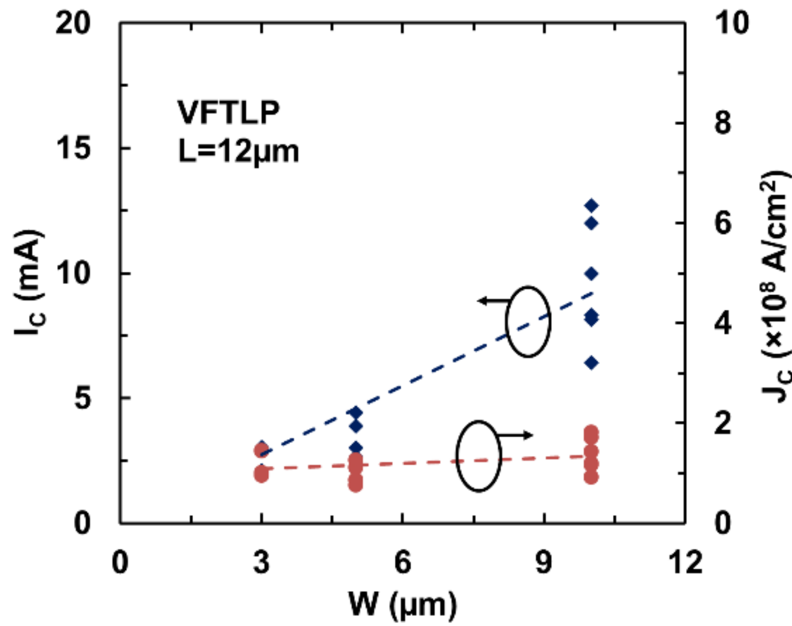
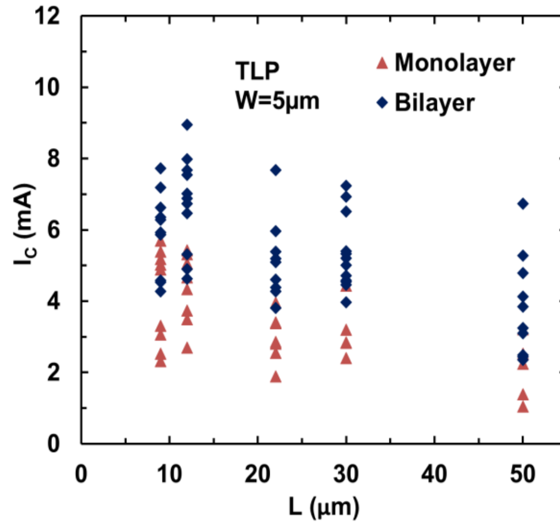


Figure 3. 10 Statistics for I_C and J_C versus W for GR samples of a fixed L=12μm and varying W obtained by VFTLP (t_d=5ns, t_r=0.2ns) shows clear dependence of I_C on W, however, J_C (~1.6×10^8 A/cm^2) is almost independent of W.

Figure 3.10 presents the measured statistics for I_C/J_C ~ W characteristics of GR samples (L = 12μm) obtained by VFTLP zapping, which also shows a strong dependence of I_C on W. However, the measured J_C is almost independent of W, attributed to short VFTLP pulsing.

Graphene Layers

(a)



(b)

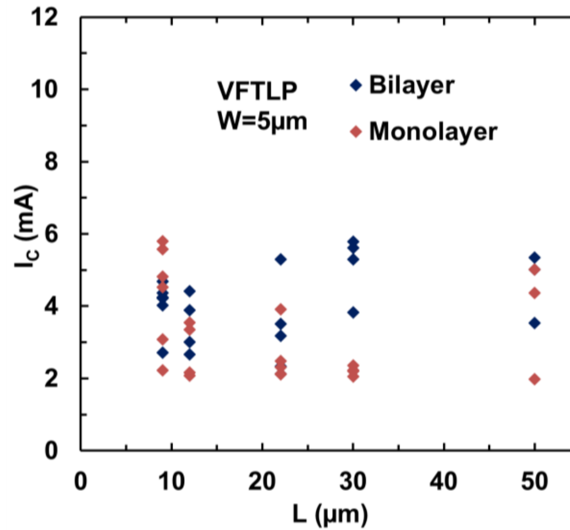


Figure 3. 11 Statistics on I_C behaviors for GR samples of W=5 µm, varying L and number of graphene layers (monolayer and bilayer) obtained by (a) TLP & (b) VFTLP testing show the layer number impact on ESD robustness: bilayer GR wires are stronger than monolayer GR wires as expected.

Influence of number of graphene layers on transient ESD behaviors of GR wires were studied. Figure 3.11 (a) gives the statistics for I_C relationship with the number of layers for GR samples (varying L and fixed W= 5μm) measured by TLP testing. It is readily observed that bilayer GR wires can carry much higher current than monolayer GR wires do. For all samples, I_C decreases as L increases, which agrees with the observation for other samples discussed previously. Figure 3.11 (b) depicts the statistics of VFTLP zapping results for GR wires, which also shows that bilayer GR wires are stronger than monolayer devices. However, probably due to the much shorter VFTLP pulse duration, the measured I_C was sensitive to L. These statistical results suggest that multilayer GR wires may be used in practical designs for enhanced ESD performance.

3.3.5 ESD Characteristics versus Pulse Rise Time and Duration

Because ESD thermal runaway is directly related to the energy accumulation during ESD stressing, it is important to study any influence of ESD pulse waveforms on ESD discharging behaviors. TLP and VFTLP zapping with varying t_d and t_r, as depicted in Table III, were then conducted for GR samples. Figure 3.12 (a) depicts the measured J_C behaviors under different t_d for TLP pulsing (fixed t_r =10ns), which clearly shows that J_C drops (from 2.4×10^8 A/cm^2 to 1.5×10^8 A/cm^2) as TLP pulse becomes wider, apparently due to the energy accumulation within an ESD pulse. The measured statistics also shows that P_C decreases dramatically (from 100mW to 30mW) as t_d increases. Figure 3.12 (b) gives the statistical analysis of measured J_C with respect to t_r, also showing a clear relationship, though less than observed for varying t_d as expected.

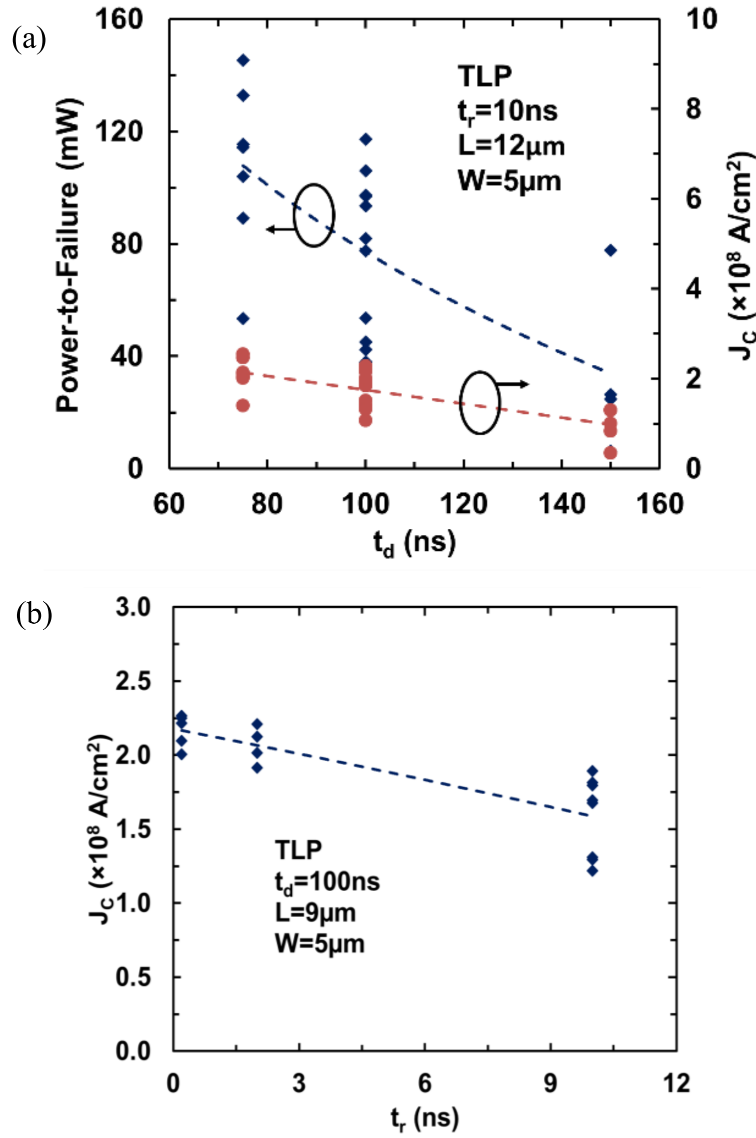


Figure 3. 12 (a) Statistics of $J_C \sim t_d$ characteristics by TLP (t_d = 75/100/150ns & t_r=10ns) for GR samples (L=12µm, W=5µm) shows strong impact of t_d: J_C decreases (from 2.4×10^8 A/cm^2 to 1.5×10^8 A/cm^2) as t_d increases. Similar phenomenon was also observed for the measured P_C. (b) Statistics of $J_C \sim t_r$ characteristics by TLP (t_r = 0.2/2/10ns & t_d=100ns) for GR samples (L=9µm, W=5µm) shows a strong impact of t_r on J_C (decreasing from 2.2×10^8 A/cm^2 to 1.5×10^8 A/cm^2).

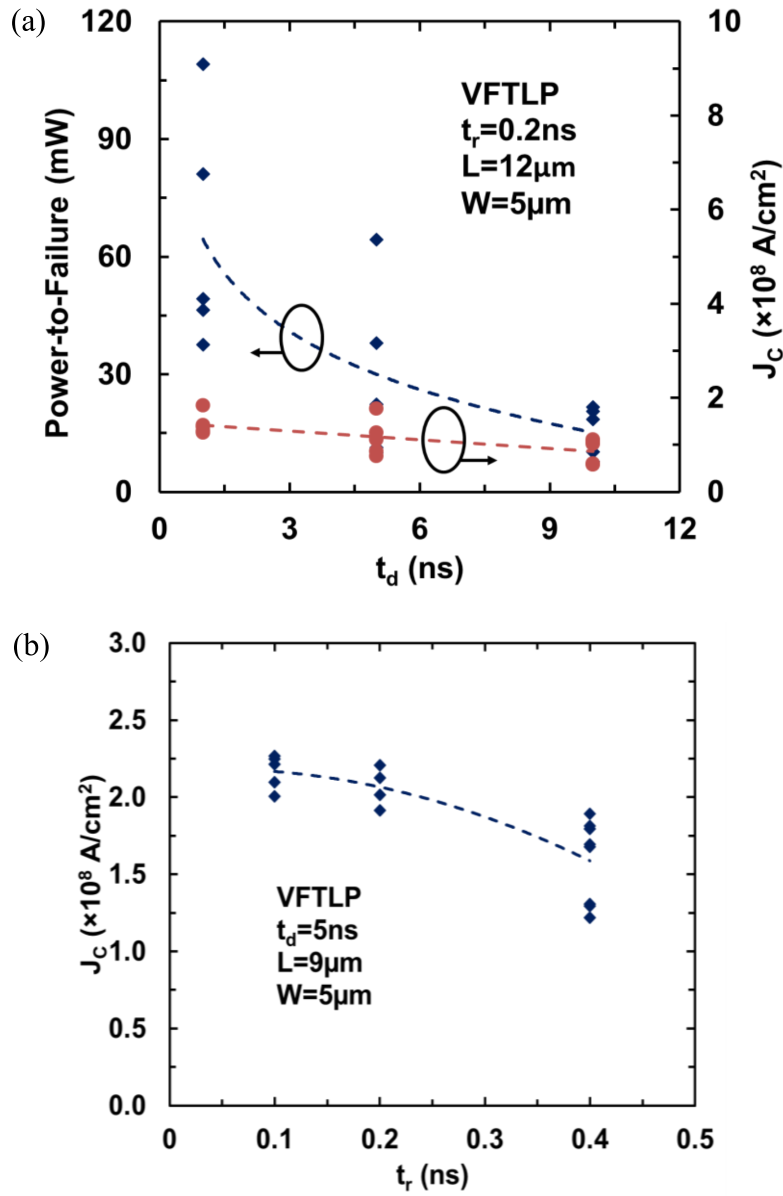


Figure 3. 13 (a) Statistics of $J_C \sim t_d$ characteristics by VFTLP (t_d = 1/5/10ns & t_r=0.2ns) for GR samples (L=12μm, W=5μm) shows s strong impact of t_d: J_C decreases (from 1.5×10^8 A/cm^2 to 0.2×10^8 A/cm^2) as t_d increases. Similarly, P_C also decreases for longer VFTLP pulses. (b) Statistics of $J_C \sim t_r$ characteristics by VFTLP with varying t_r (0.1/0.2/0.4ns & t_d=5ns) for GR samples (L=9μm, W=5μm) shows strong dependence of J_C on t_r.

Similar phenomena were observed for statistic measurement results by VFTLP zapping. Figure 3.13 (a) presents the measured statistics of $J_C \sim t_d$ relationship by VFTLP zapping with varying t_d (fixed t_r =200ps) for GR samples (L=12μm, W=5μm), which shows that J_C decreases (from 1.5×10^8 A/cm^2 to 0.2×10^8 A/cm^2) as t_d increases. Similarly, the measured P_C drops dramatically (from 60mW to 10mW) for longer VFTLP pulses. Figure 3.13 (b) depicts the measured statistics for J_C with varying t_r of VFTLP pulses where a strong dependence is readily observed. The overall dependence of measured J_C on t_r and t_d of TLP and VFTLP pulse waveforms for GR wires can be better appreciated in the 3D spectrum maps given in Figure 3.14.

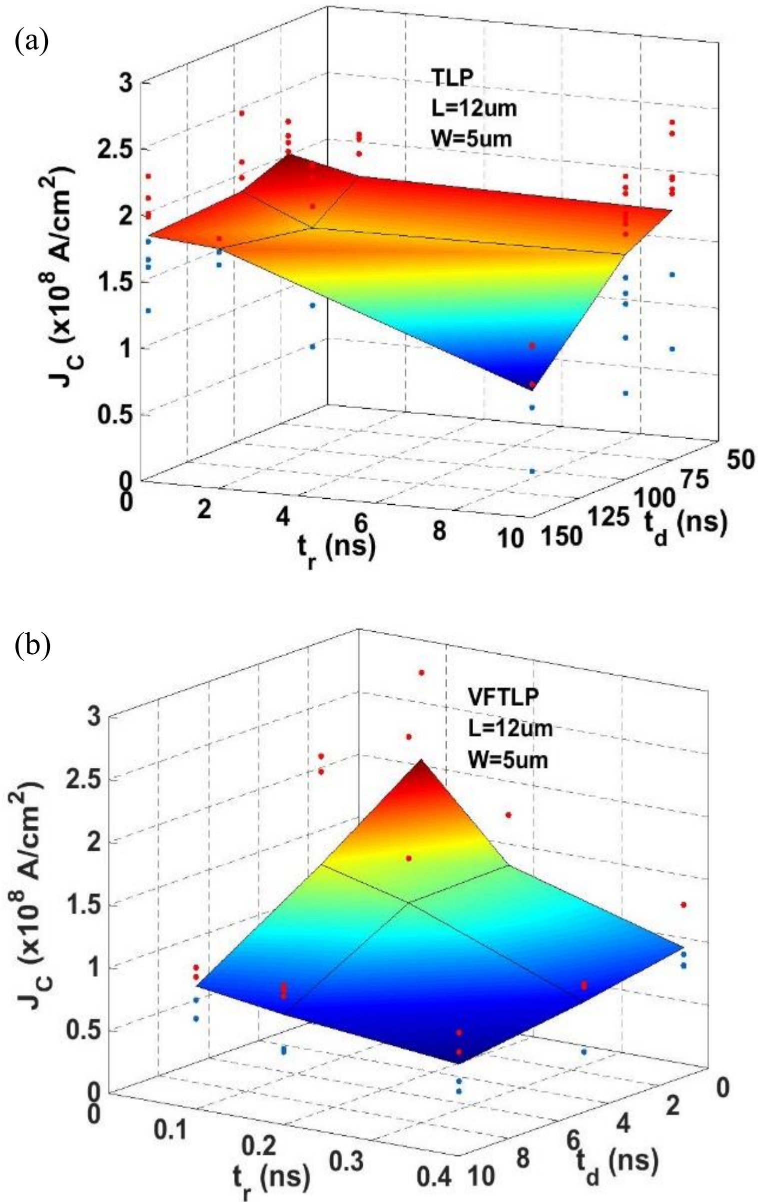


Figure 3. 14 A 3D statistics map for measured J_C distribution against varying t_d (75/100/150ns) & t_r (0.2/2/10ns) by (a) TLP testing and varying t_d (1/5/10ns) & t_r (100/200/400ps) by (b) VFTLP testing for GR sample (L=12μm, W=5μm) clearly show degradation of J_C with longer t_d and t_r.

3.3.6 ESD Characteristics versus Temperature

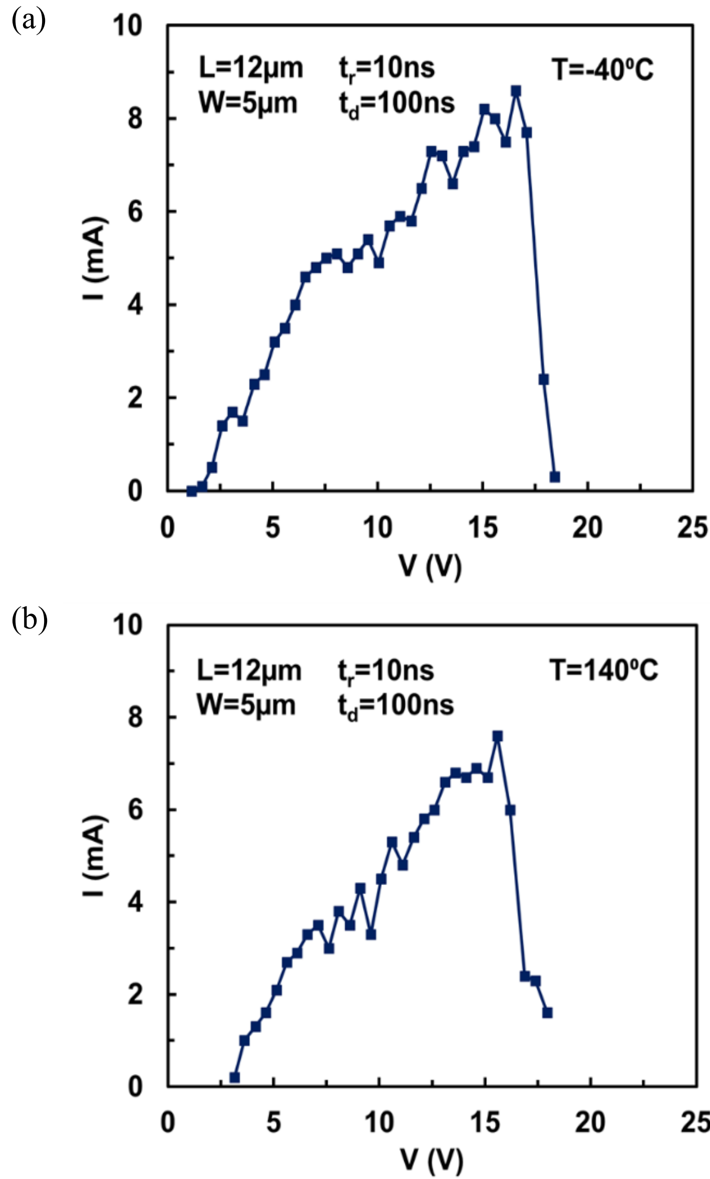


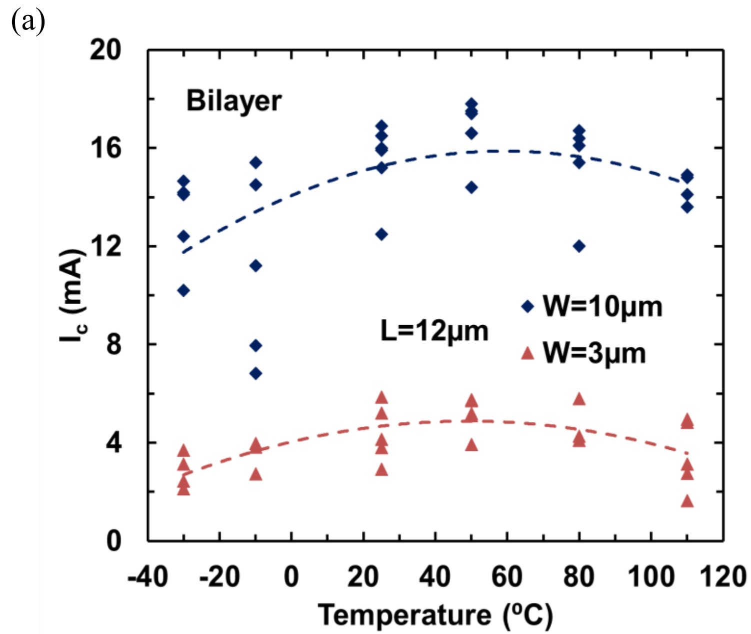
Figure 3. 15 (a) Measured transient I-V curve for a bilayer GR sample (L=12µm, W=5 µm) by TLP at T= -40°C shows exceptional J_{t2}~$2.46x10^8 A/cm^2$. (b) Measured I-V curve for a bilayer GR sample (L=12µm, W=5 µm) by TLP at T= +140°C shows exceptional J_{t2}~$2.17x10^8 A/cm^2$.

The GR robustness is determined by the breakdown current (I_{t2}, or current density, J_{t2}) where the current drops abruptly in a transient I-V curve by TLP testing, and the corresponding breakdown voltage is V_{t2}. Figure 3.15 (a) presents the I-V curve for a GR sample (L=12μm, W=5μm) by TLP (t_d=100ns, t_r=10ns) at T= -40℃, showing V_{t2} ~16.56V and I_{t2}~8.6mA, or, J_{t2}~2.46x10^8A/cm^2. Figure 3.15 (b) depicts an I-V curve a sample GR (L = 12μm, W = 5μm) by TLP at T= +140℃, showing J_{t2} ~ 2.17×10^8 A/cm^2. The measured transient current handling capability is exceptional high as expected for graphene wires.

Temperature evaluation is critical to IC operations. Comprehensive TLP characterization (t_d=100ns, t_r=10ns) was conducted for both monolayer and bilayer GR samples across a wide temperature range of -30ºC to +110ºC. Figure 3.16 depicts statistics of measured I_C across the temperature range for bilayer and monolayer GR wires, respectively. It is obvious that wider GR samples can carry higher ESD currents across the temperature range. It is found that a bell shape of I_C ~ T curves clearly exists based on the statistics of a large number GR samples. This observation suggests that there may exist an optimal temperature treatment condition (i.e., T ≈ 50~60ºC) to improve ESD current handling capability of GR wires. This optimal temperature condition may be associated with two possible competing factors: On one hand, thermal annealing by gradual temperature increase and a thermal equilibrium effect may improve material quality of GR wires. On the other hand, continuous heating up GR wires in open air testing condition, as in this work, may affect graphene film quality (e.g., conductivity possibly affected by Coulomb scattering due to temperature variation [39]). Consequently, a bell shape may

exist for $I_C \sim T$ curves, which may reveal a means to improve the quality of GR wires for enhanced ESD robustness during sample preparation.

(a)



(b)

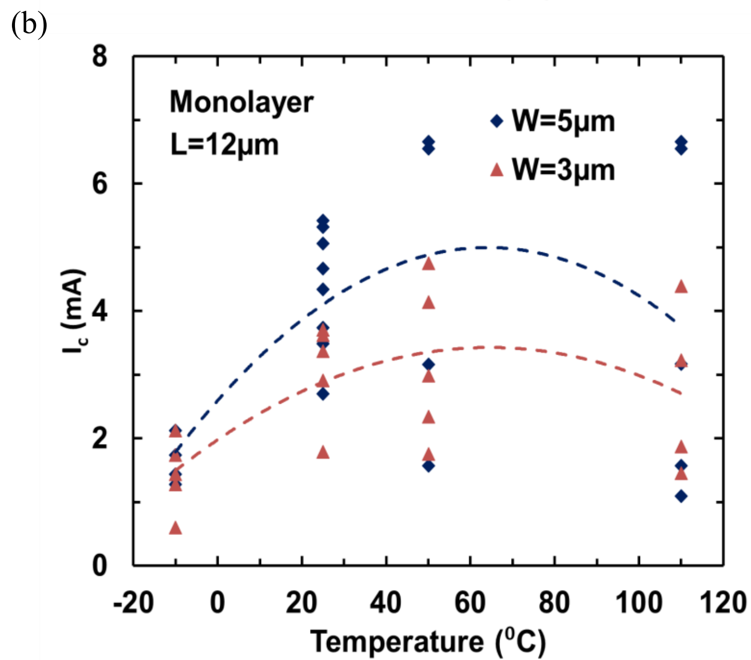


Figure 3. 16 Statistics for measured I_C~T behavior (-30ºC to +110ºC) for (a) bilayer & (b) monolayer GR wires by TLP testing suggests that optimal temperature treatment (T~50ºC) may exist to improve ESD robustness.

Temperature effects were then studied statistically across a wide temperate of T= -40ºC to 140ºC and a large set of GR samples. Figure 3.17 presents the statistics for the measured J_{t2} against varying temperature by TLP (t_d=100ns, t_r=10ns), showing a peak at T = ~80ºC, which suggests a possible optimal treatment temperature of T ~ 80ºC to maximize the J_{t2} of GR wires. It is also observed that J_{t2} seems to be higher at T~ -40°C. The temperature effects of graphene ESD interconnects may be understood according to the scattering mechanism. At low temperature, graphene is dominated by long-range interactions (Coulomb Scattering), including charged impurities in graphene films and in the supporting insulator substrates (SiO_2 in this work). At high temperature, short-range interactions are more significant in graphene films related to neutral defects, roughness and phonons. When a graphene film is heated, short-range scattering dominates, likely due to adsorbate volatilization and/or phonon scattering, resulting in higher carrier mobility, hence, possibly improving GR wire conductivity.

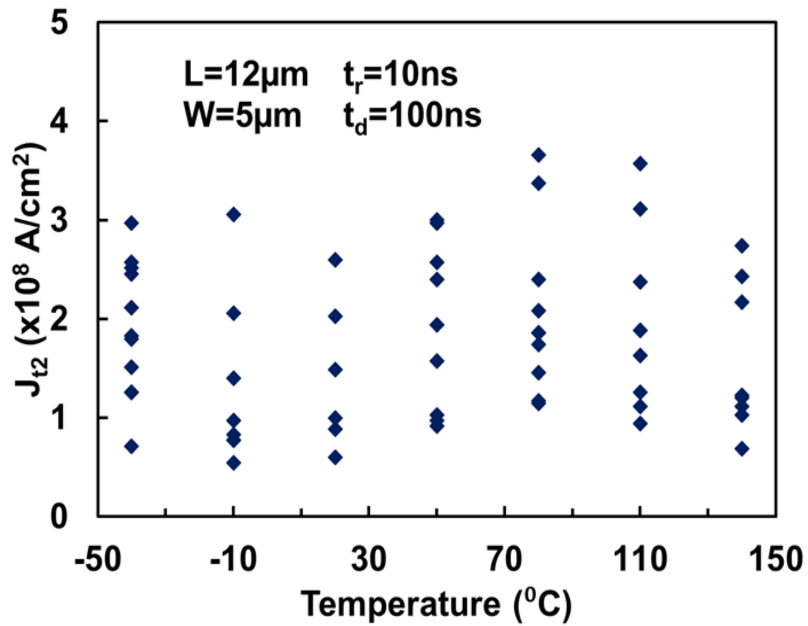


Figure 3. 17 Statistics for TLP-measured J_{t2} data against temperature variation (-40ºC to 140ºC) for bilayer GR samples suggests that possibly optimal temperature treatment may exist to improve ESD robustness of GR interconnects (T~80ºC).

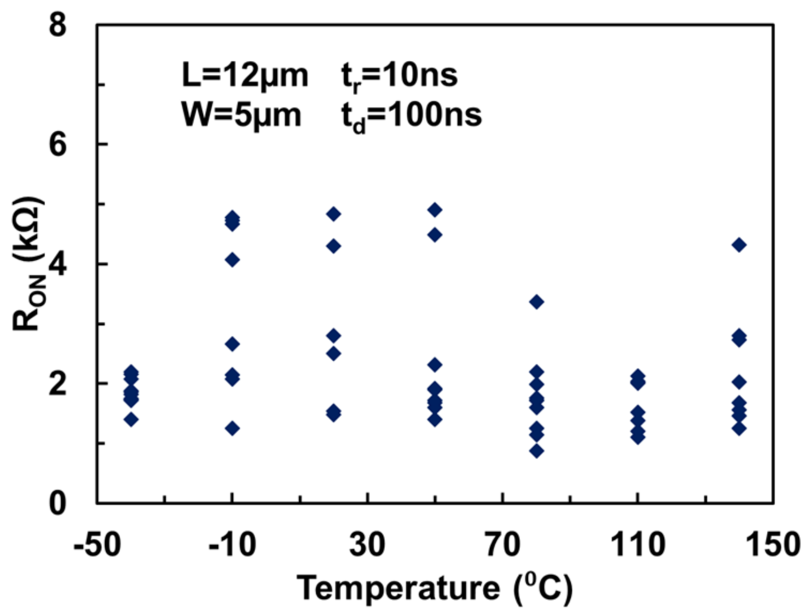


Figure 3. 18 Statistics for TLP-measured ESD discharging R_{ON} for varying temperature (-40ºC to 140ºC) shows slight improvement at lower temperature at -40ºC and degradation at higher temperature of +140ºC.

This conduction improvement may be observed from the measured ESD discharging resistance (R_{ON}) against temperature shown in Figure 3.18. However, at much higher temperature (~140 ºC), the overheating in the substrate may make graphene easier to breakdown (carbon-oxygen thermal failure), hence degrades the GR performance. On the other hand, at extreme low temperature, the heat sink of the substrate would carry away the heat induced by ESD surges in the GR interconnects, resulting in an improvement of the graphene ESD performance again. These opposite behavior trends against temperature would reach to a balance in GR wires under ESD stressing under varying temperature, hence, leads to a possible optimum ESD GR wires treatment temperature as observed in Figure 3.17.

3.3.7 ESD Characteristics versus Zapping Methods

Reliability of GR samples fabricated in this work was studied using a new *Abrupt* zapping method. Traditionally, a *Gradual* zapping method has been used in TLP zapping where, within a full-zapping cycle, zapping continues by gradually stepping up the TLP pulse height from 0V until reaching to the ESD breakdown point (I_C or J_C) with an incremental step of ΔV. The new Abrupt zapping method works differently: after knowing the ESD failure threshold of a given GR wire, TLP zapping will be conducted in 2 steps, i.e., starting at 0V, then abruptly applying a high pulse with the height corresponding to the estimated ESD failure threshold point. After an abrupt zapping cycle, the stressed GR wire will be checked to determine if it is still working (i.e., not damaged by a TLP pulse). This Abrupt zapping method was applied to a large number of GR samples of varying dimensions and the Survival Rate was obtained based on statistics of the measured results. Figure 3.19 gives a 3D statistical map for GR samples of different L that were zapped by TLP pulses of varying strength (pulse height, or, the zapping current density, J). It is observed that for GR wires of a given L, the sample survival rate drops dramatically as higher TLP pulses were applied for zapping; meanwhile, at a fixed TLP zapping strength, the survival rate decreases as L increases, which is likely due to more defects in longer GR wires associated with fabrication impaction. The survival rate reflects reliability of the GR wire samples. It is also noted that the measured J_C level of $25\sim125\times10^6$ A/cm^2 by Abrupt zapping is generally substantially lower than J_C of several 10^8 A/cm^2 by Gradual zapping. Several factors may contribute to this phenomenon, including thermal equilibrium, stressing pulse gradient and non-thermal failure effects, which are being investigated now.

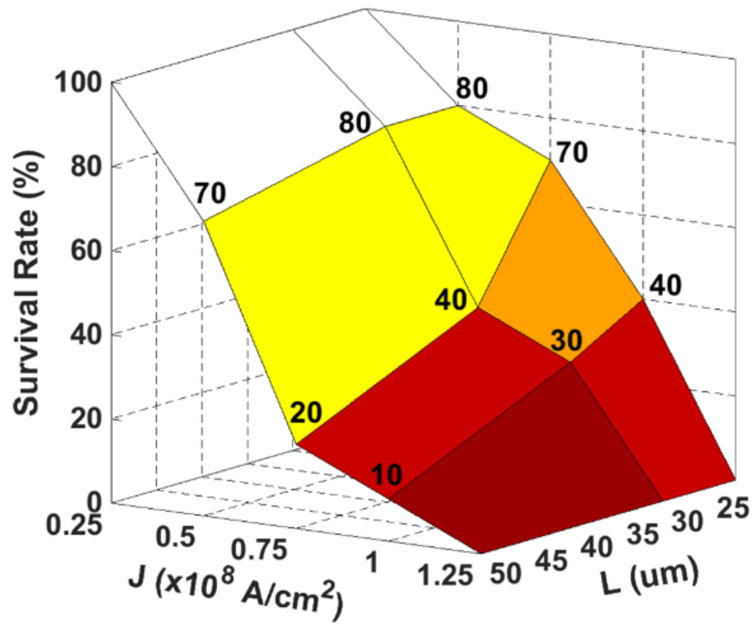


Figure 3. 19 A 3D statistical map for GR survival rate with respect to GR wire length and zapping current level for GR samples of varying L (fixed W=5μm) obtained by Abrupt TLP zapping method.

3.4 Failure Analysis

Raman spectroscopy was performed to monitor the failure process of GR samples under TLP stressing. Figure 3.20 shows the Raman scanning map for a GR wire of L= 12μm before and after TLP zapping where the Raman D-peak intensity is an indicator for defect accumulation within the GR wire stressed [34, 25]. The ESD failure development process is readily observed in Figure 3.20. It is believed that, before TLP stressing, defects are mainly located along the boundaries of graphene grown by CVD method. After TLP stressing, localized defects were developed and formed a *fault line* across a GR wire, which is the failure signature observed as shown in Figure 3.21.

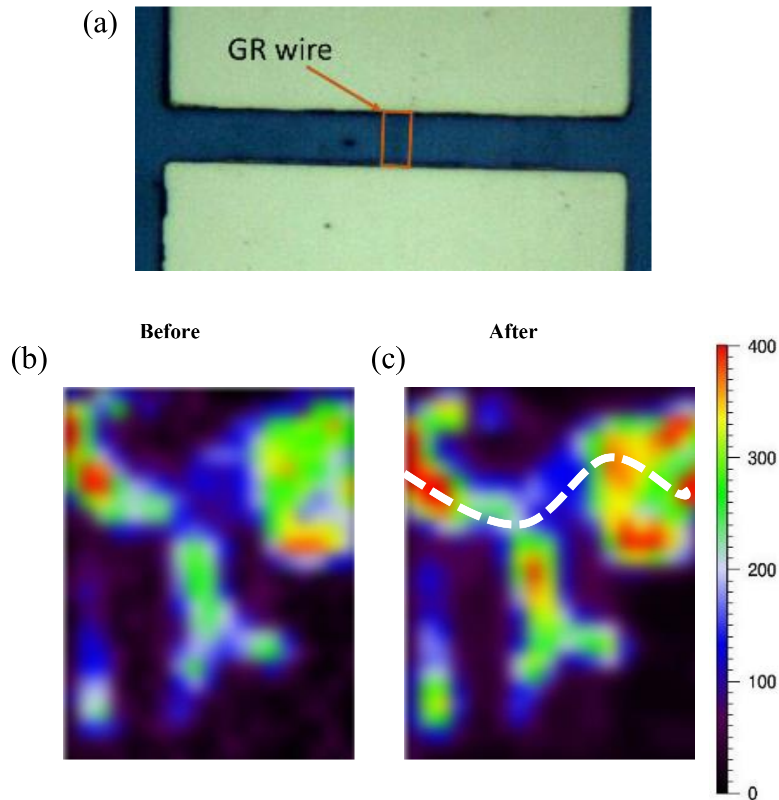


Figure 3. 20 D-peak intensity in Raman spectrum for a GR sample (L=12μm, W=5μm) before and after TLP zapping breakdown illustrates defect development, leading to ESD failure: (a) optical microscopy for GR wire; (b) D-peak intensity before breakdown; (c) D-peak intensity after breakdown.

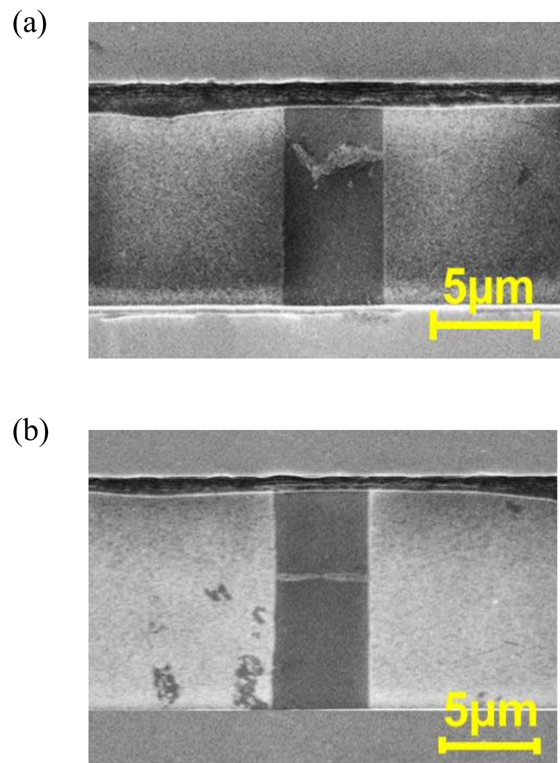


Figure 3. 21 SEM images show the failure signature that is a fault line across the GR wire after ESD zapping breakdown: (a) GR wires (L=9μm, W=5μm) by TLP zapping (t_d=100ns, t_r=10ns); (b) GR wires (L=12μm, W=5μm) by VFTLP stressing (t_d=5ns, t_r=0.2ns).

3.5 Conclusion

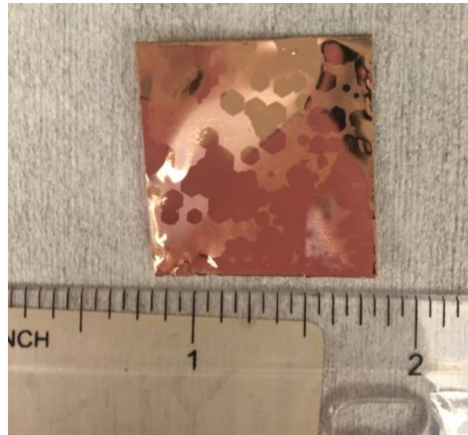
We report a comprehensive characterization and statistical analysis of GR wires by TLP and VFTLP zapping for ESD evaluation. A large number of GR samples (~ 6000) with varying and practical dimensions (L=9/12/22/30/50μm and W=3/5/10μm, monolayer and bilayer) were characterized. Comprehensive TLP and VFTLP testing was performed using varying transient ESD pulses (t_r=0.2/2/10ns & t_d=75/100/150ns for TLP; t_r=100/200/400ps & t_d=1/5/10ns for VFTLP) across a wide temperature range (T= -40/+140 °C). The statistics reveal ESD robustness dependence of wire dimensions, pulse shapes and temperature of GR samples, offering insights for practical designs. TLP and VFTLP zapping shows higher transient J_C of ~10^8 A/cm^2 compared with reported DC J_C of ~10^7 A/cm^2 for GR wires. It suggests that GR wires are potential candidates for ESD interconnects for future on-chip ESD protection designs. Due to process and test effects, statistical variation is observed, e.g., a standard deviation of 0.38 (TLP, 10ns/100ns) and 0.23 (VFTLP, 0.2ns/5ns) in J_C for samples of L=12μm and W=5μm, respectively.

3.6 Single Crystalline Graphene ESD Interconnects

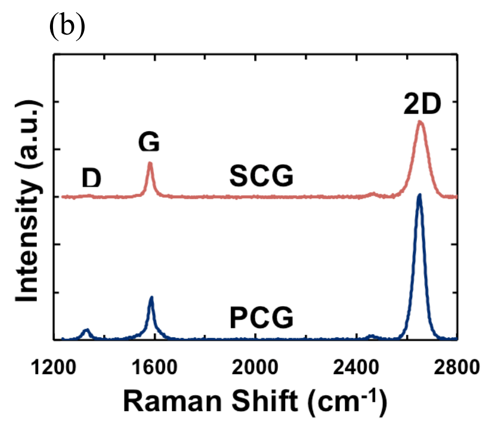
We report systematic transient characterization of single-crystalline graphene (SCG) interconnects for electrostatic discharge (ESD) protection for integrated circuits (IC). Single-crystalline graphene ribbons were fabricated by CVD method with practical dimensions and characterized by transmission line pulsing (TLP) and very-fast TLP (VFTLP) measurements. Comprehensive TLP and VFTLP testing with varying pulse rise time (t_r) and duration (t_d) was performed. Measurement statistics show improvement of ESD protection capability compared with poly-crystalline graphene (PCG) ESD interconnects. Specifically, ESD current handling density (J_{t2}) of SCG wires is up to ~10^9 A/cm^2, about three times higher than that for PCG ESD interconnects.

SCG films as shown in Figure 3.22 (a) were grown by chemical vapor deposition (CVD) method [53, 54], suitable for large area graphene fabrication for real-world ICs. Raman analysis was used to confirm quality of graphene films. Figure 3.22 (b) compares SCG and PCG, where the D-peak intensity depicting the defects level in graphene material [34, 35] that shows a much reduced peak for SCG, suggesting better material quality for SCG. For the device fabrication, Cr/Au (20/120nm) pads (100x100µm^2) were first deposited by sputtering. SCG films were then transferred onto SiO_2 (300nm)/Si substrates and patterned by oxygen plasma into ribbons with the dimensions designed for various length (L=9/12/22µm) and width (W=3/5/10µm). Figure 3.22 (c) shows fabricated metal pads covered by SCG sheets before patterning. The domain size of the single-crystalline graphene is about 2~5mm [56].

(a)



(b)



(c)

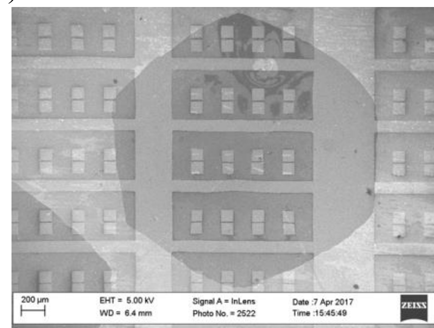


Figure 3. 22 (a) Single-crystalline graphene (SCG) on coppor films. (b) Raman Analysis of the PCG and SCG graphene films. (c) SEM images of metal pads covered by SCG film.

Graphene sheet resistance was first extracted by transmission line measurement [13, 14] for both poly-crystalline and single-crystalline interconnects including graphene resistance (R_G) and contact resistance (R_C). Figure 3.23 shows statistics for a large group of monolayer graphene wires with varying length of L= 9/12/22 μm and a fixed W=5μm by DC testing, from which, the single-crystalline graphene sheet resistances is extracted as R_s≈650Ω/□, smaller than the poly-crystalline graphene sheet resistance of 910Ω/□.

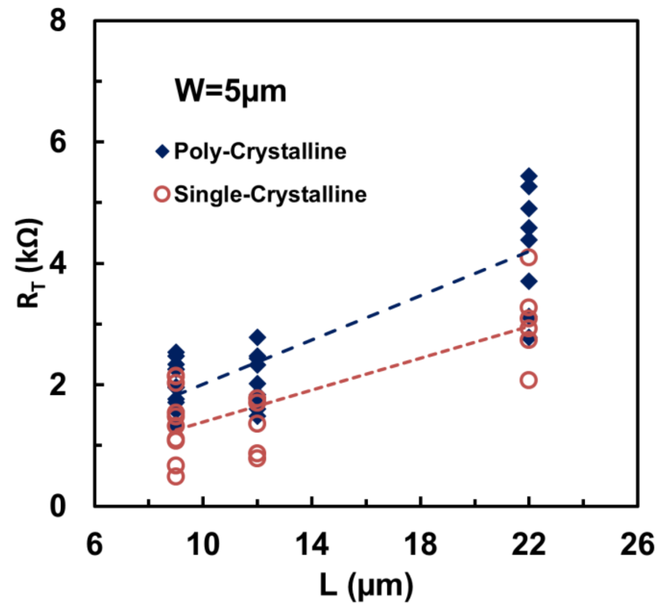


Figure 3. 23 Statistics analysis for graphene wire total resistance for varying L (W=5μm) by DC testing. Graphene sheet resistances are extracted to be 650Ω/□ (SCG) and 910Ω/□ (PCG).

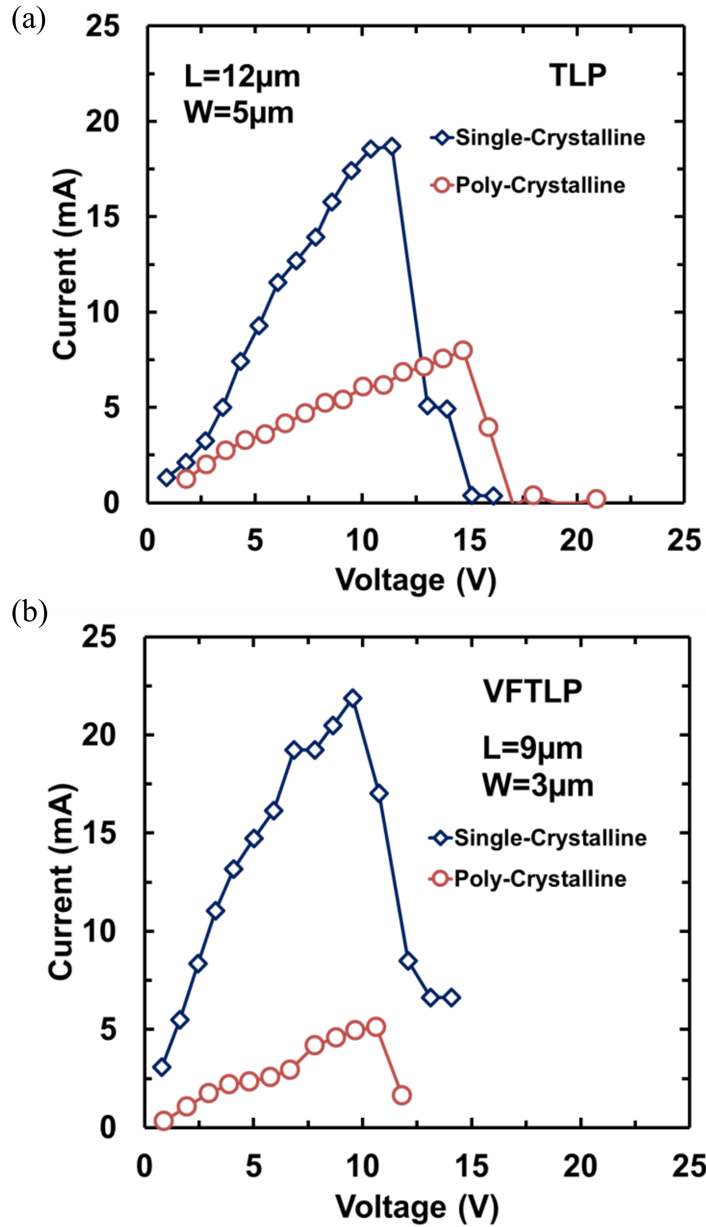


Figure 3. 24 (a) Comparison of TLP transient I-V characteristics for SCG and PCG interconnects samples (L=12μm, W=5μm) shows improved ESD capability for SCG. (b) VFTLP I-V curves for SCG and PCG samples (L=9μm, W=3μm) shows I_{t2} of SCG interconnects is much improved over PCG wires.

The graphene ESD interconnects robustness is determined by the maximum sustainable current (I_{t2}, and its current density, J_{t2}) corresponding to the thermal failure point when I_{t2} drops abruptly. Figure 3.24 (a) compares transient I-V curves by TLP testing (t_r=10ns, t_d=100ns) for SCG and PCG wire samples (L = 12µm, W = 5µm). It is readily observed that I_{t2} (I_{t2}=18.7mA, J_{t2} = 1.06×10^9 A/cm^2) for SCG is substantially higher than that of PCG (I_{t2}=7.97mA, J_{t2} =4.55×10^8 A/cm^2). The observed improvement in ESD capability for SCG wires over PCG wires is about 2.5 times. Figure 3.24 (b) presents VFTLP I-V curves (t_r=0.2ns, t_d=5ns) for SCG and PCG wire samples (L=9µm, W=3µm). It also shows that J_{t2} = 2.08×10^9 A/cm^2 for SCG is much improved than that of PCG interconnects (J_{t2} =4.85×10^8 A/cm^2).

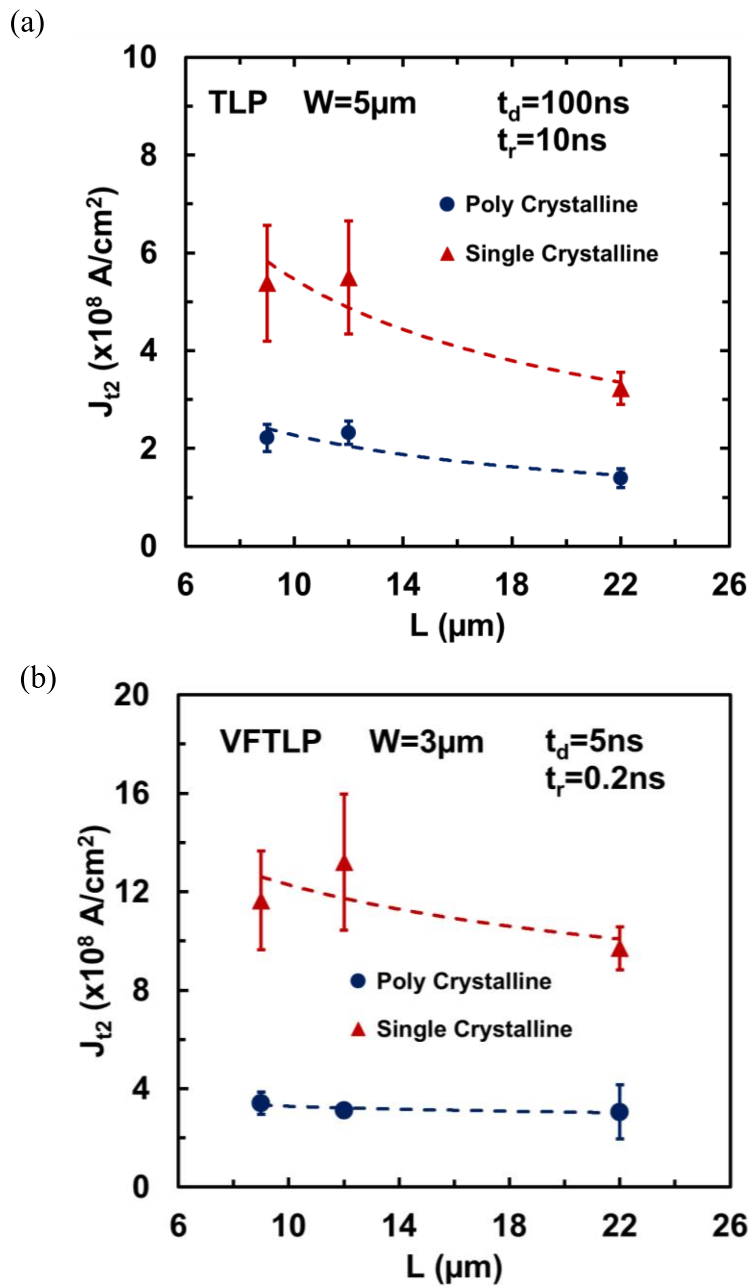


Figure 3. 25 Statistics for (a) TLP and (b) VFTLP testing results of SCG and PCG interconnects shows that J_{t2} of SCG is higher than that for PCG wires. J_{t2} decreases as L increases.

Figure 3.25 (a) depicts the statistical characteristics of J_{t2} versus L (W=5μm) for a group of SCG and PCG samples by TLP testing. It is readily observed that J_{t2} of SCG is ~3 times higher than that of PCG ESD interconnects, suggesting much better ESD current handling capability of SCG wires. In addition, the measured statistics show slight decrease of J_{t2} as L increases. We suspect that although SCG has nearly no grain boundaries within its domain size, however, defective sites along the wire surface still exist that may be introduced by the fabrication process. As a result, we assume longer graphene samples possibly carry more defective sites, making longer wires easier to breakdown. Figure 3.25 (b) depicts the statistics for VFTLP testing results of both SCG and PCG samples with varying L (fixed W=3 μm), confirming that SCG is stronger than the PCG graphene too.

Figure 3.26 (a) shows the measured J_{t2} behaviors under different t_d of TLP pulsing (fixed t_r =10ns) for a set of SCG interconnects samples, which clearly shows that J_{t2} drops substantially (from 6×10^8 A/cm^2 to 4×10^8 A/cm^2) as TLP pulse becomes wider, apparently due to the energy accumulation within an ESD pulse. Figure 3.26 (b) presents the measured statistics of $J_{t2} \sim t_d$ relationship by VFTLP zapping with varying t_d (fixed t_r=200ps) for SCG ESD interconnects samples (L=9μm, W=10μm), which shows that J_{t2} decreases (from 1×10^9 A/cm^2 to 4×10^8 A/cm^2) as t_d increases.

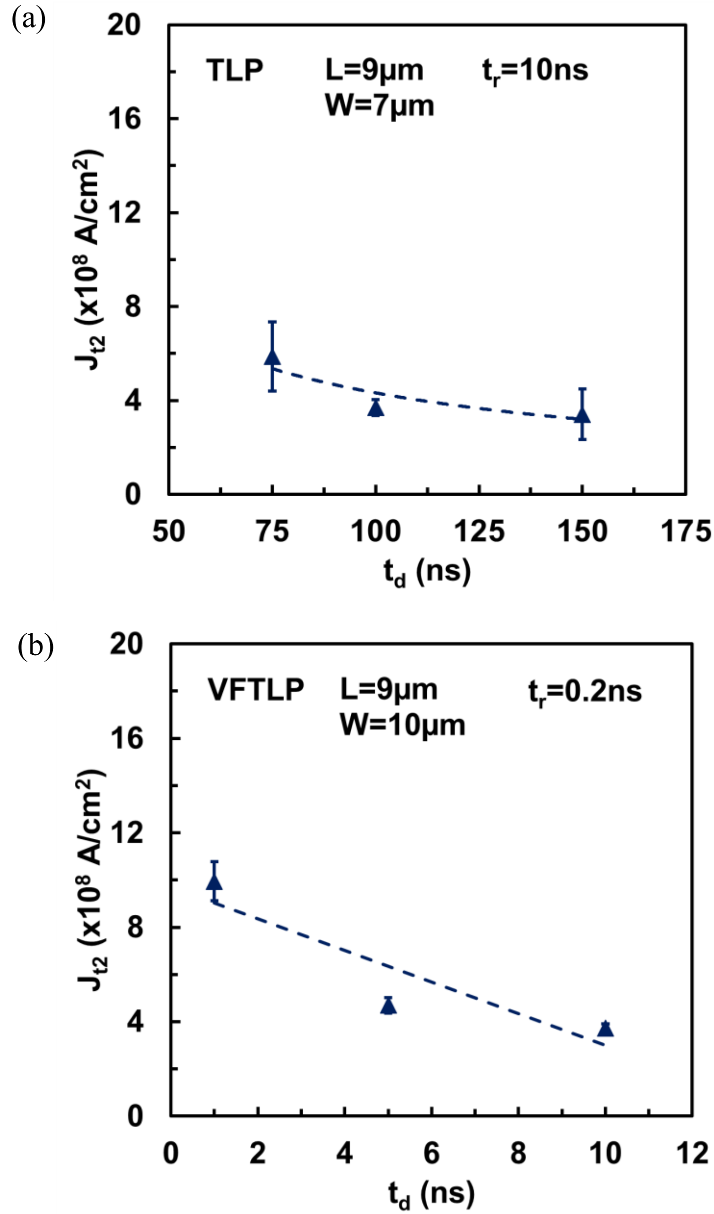


Figure 3. 26 (a) Statistics of J_{t2} ~ t_d characteristics by TLP testing (t_d = 75/100/150ns, t_r=10ns) for SCG samples (L=9µm, W=7µm) shows that J_{t2} decreases as t_d increases. (b) Statistics of J_{t2} ~ t_d characteristics by VFTLP testing (t_d = 1/5/10ns, t_r=0.2ns) for SCG samples (L=9µm, W=10µm) also shows impact of t_d.

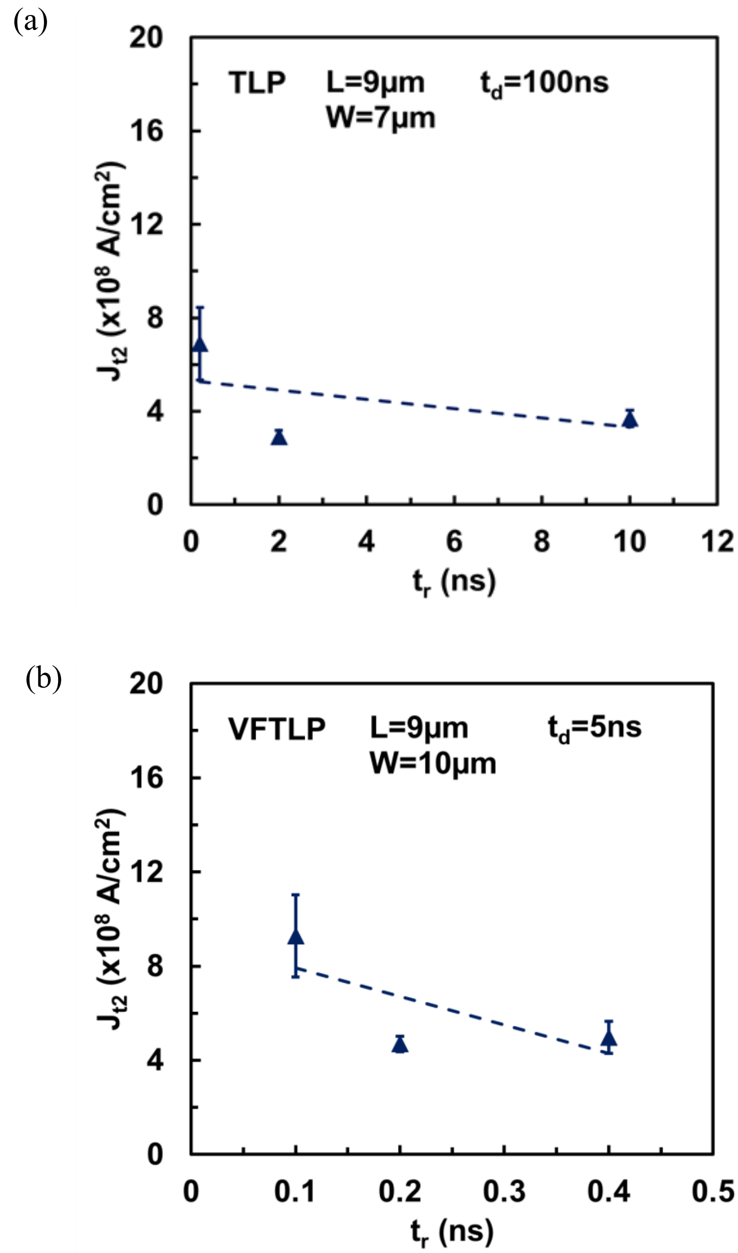


Figure 3. 27 (a) Statistics of $J_{t2} \sim t_r$ characteristics by TLP testing (t_r = 0.2/2/10ns for fixed t_d=100ns) for SCG wires. (b) Statistics of $J_{t2} \sim t_r$ characteristics by VFTLP testing with varying t_r (0.1/0.2/0.4ns at fixed t_d=5ns) for SCG samples (L=9μm, W=10μm). Dependence of J_{t2} on t_r is observed.

Figure 3.27 (a) gives the statistical analysis of measured J_{t2} with respect to t_r for a set of SCG wires (L=9µm, W=7µm), stressed by TLP surges. It shows a clear relationship: as t_r increases from 0.2, 2 to 10ns, J_{t2} decreases from 7×10^8 A/cm^2 to 4×10^8 A/cm^2. Similar phenomena were observed for statistic measurement results by VFTLP zapping as depicted in Figure 3.27 (b) where J_{t2} drops from 9×10^8 A/cm^2 to 5×10^8 A/cm^2 when t_r increases from 0.1, 0.2 to 0.4ns.

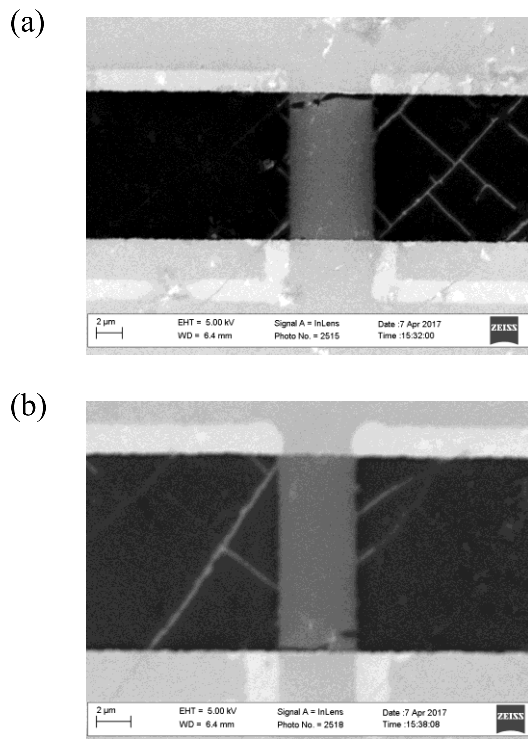


Figure 3. 28 ESD failure signature by SEM images for SCG ESD interconnects samples after ESD zapping. (a) graphene wires (L=9µm, W=5µm) by TLP zapping (t_d=100ns, t_r=10ns), and (b) graphene wires (L=9µm, W=3µm) by VFTLP stressing (t_d=5ns, t_r=0.2ns).

The ESD failure development process is readily observed in Figure 3.28. It shows the failure signature for the SCG ESD interconnects for both TLP and VFTLP stresses. After TLP stressing, localized defects developed to form a fault line across the graphene ribbon wires, causing breakdown of the ESD interconnects [31-33]. Fault line is found across the near pad regions of the graphene samples, likely because the stress between the graphene ribbons and the metal pad may induce some cracks along the graphene-pad transition regions, causing breakdown by ESD stresses.

We report a comprehensive characterization and statistical transient analysis of SCG wires by TLP and VFTLP zapping measurement for ESD evaluation. A large number of graphene wire samples with varying and practical dimensions were conducted. Comprehensive TLP and VFTLP measurements were performed using transient pulses of different rise time and duration. The statistical analysis show that SCG ESD interconnects have ultra-high ESD current handling capability, up to ~10^9 A/cm^2, much higher than that of PCG ESD interconnects. The statistics suggest that SCG wires have good potential to be used as robust ESD interconnects for future ICs.

Chapter 4 Graphene NEMS ESD Switch

4.1 Graphene NEMS ESD Switch

4.1.1 Concept & Structure

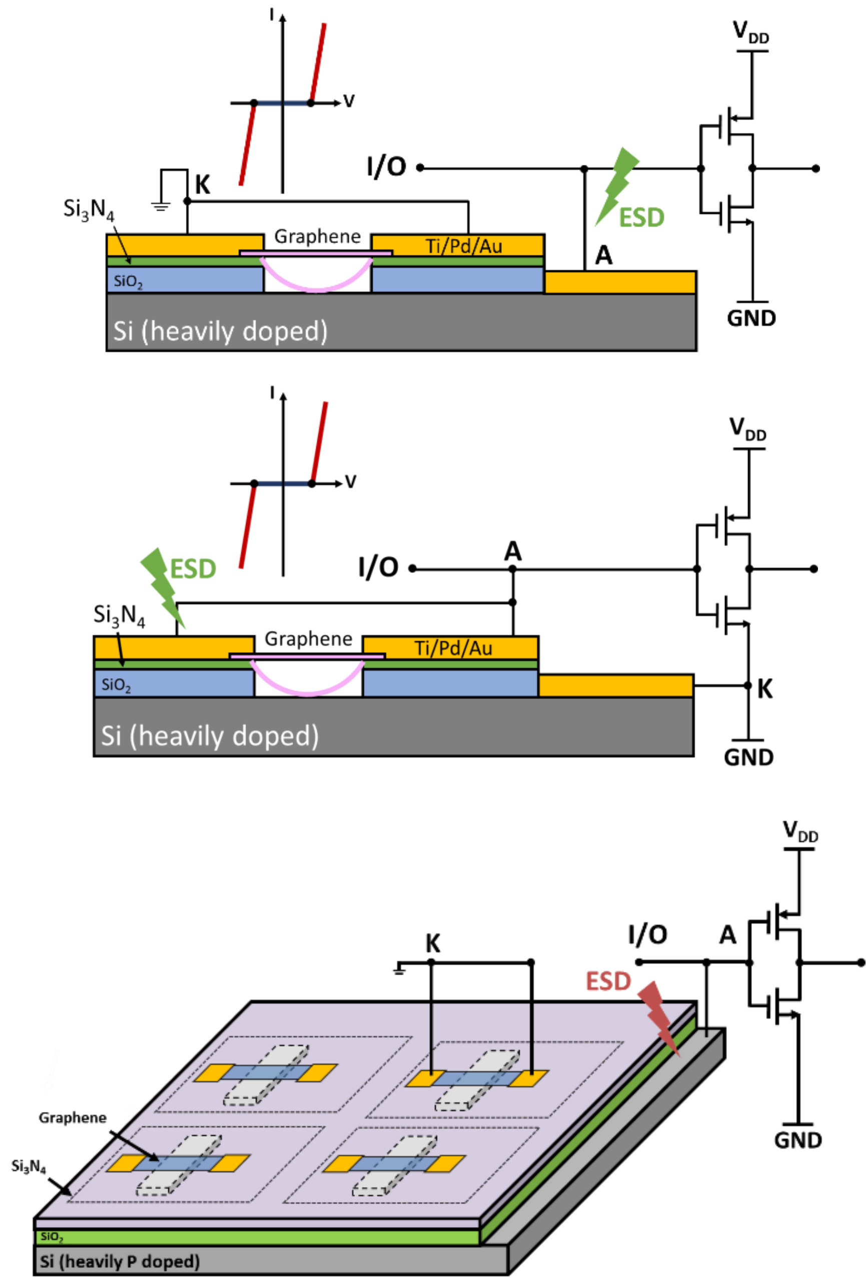


Figure 4. 1 Cross-section and 3D view with circuit scenario for the new gNEMS switch ESD protection structure. The normal-OFF switch can be turned on by pulling down the graphene membrane by ESD pulses. The inset illustrates an ideal ON-OFF I-V behavior for the gNEMS ESD switch.

We introduced a new non-traditional concept of graphene gNEMS ESD switch with initial ESD protection mechanism confirmed in transient ESD testing. As illustrated in Figure 4.1, a gNEMS switch is a two-terminal mechanical switch structure consisting of a graphene membrane on top of an air chamber. The two terminals (anode, A; cathode, K) are the graphene membrane on top and a conductor at the bottom of the air chamber, which are connected to the I/O pads and ground (GND) or power bus (V_{SS} and V_{DD}) pads on a chip. During normal IC operation, the new graphene ESD device remains OFF without affecting ICs. When an ESD surge occurs at I/O, the induced electrostatic force will pull down the suspended graphene membrane and when the graphene membrane touches the bottom, the gNEMS switch is turned ON to discharge the ESD pulses, hence protects ICs.

4.1.2 Properties

Graphene were widely investigated to make electron devices due to its high electron mobility (~5000 $cm^2/V\text{-}s$) [9, 40], however, with little practical success due to its zero bandgap nature. On the other hand, its excellent mechanical properties, e.g., Young's modulus of ~ 1T Pa [10] and light mass density, make it possible to build graphene-based mechanical devices. For example, low-current DC graphene mechanical switching phenomena were reported recently [41-43]. Targeting for low static power dissipation for ICs, the reported DC graphene switches have major problems: it has slow switching time (~40ns) and can only survive a few switching times before failure [44-46]. We report the first dual-polarity transient graphene NEMS (gNEMS) switch ESD protection mechanism and structures in the papers [48-52].

Graphene has many desired properties for potentially excellent ESD protection, including very high electron mobility and thermal conductivity, and super strong mechanical strength [10]. Potential graphene-based ESD protection may offer non-traditional ESD protection mechanism and robust ESD protection without introducing significant ESD-induced parasitic effects that will affect IC performance, meanwhile, reduce the chip size by above-IC 3D heterogeneous integration. We report design, characterization and statistical analysis of a new 3D above-IC graphene NEMS switch structure as on-chip ESD protection solution. (NEMS)

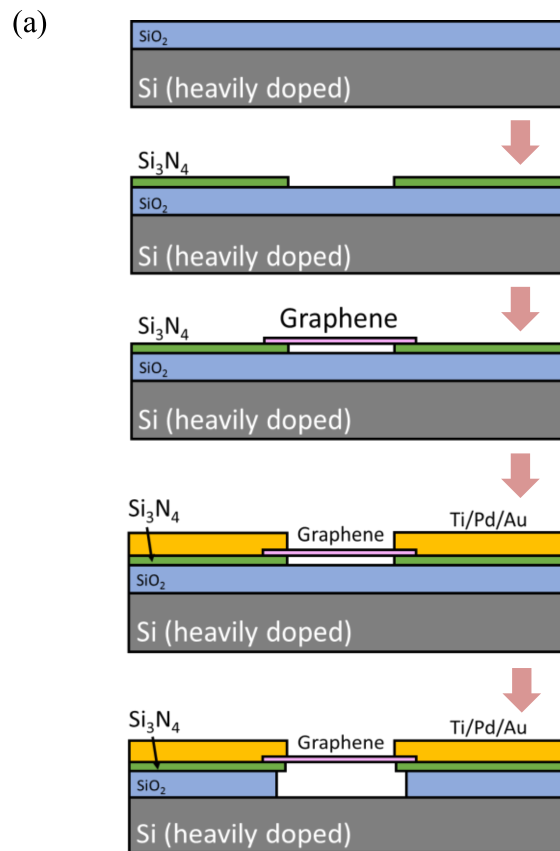
Unlike traditional in-Si PN-junction-based ESD structures, the new gNEMS is a mechanical switch that can ideally eliminate the ESD-induced leakage and minimized the ESD-induced capacitance and noises. Additionally, the gNEMS ESD switch is a dual-

directional ESD discharging device, which means fewer ESD devices will be needed for an IC chip because normally there are multiple ESD devices required per pad to ensure full-chip ESD protection. Further and more uniquely, the new gNEMS switch is made in the back-end module of CMOS through 3D heterogeneous integration. Hence, the two features together mean that the new above-IC gNEMS ESD structures do not consume a large Si die area as the case of using traditional in-Si PN-type ESD structures, which is equivalent to "scaling down" that cannot be achieved for ESD structures using traditional in-Si PN-based ESD structures over the past decades. This novel above-IC ESD structure takes full advantage of using 3D heterogeneous integration to develop More-Than-Moore solutions for future ICs.

4.1.3 Fabrication

A fully CMOS-compatible device fabrication process flow is critical to achieving 3D heterogeneous integration of the proposed gNEMS switches with ICs, hence realize the novel above-IC ESD protection concept.

(a)



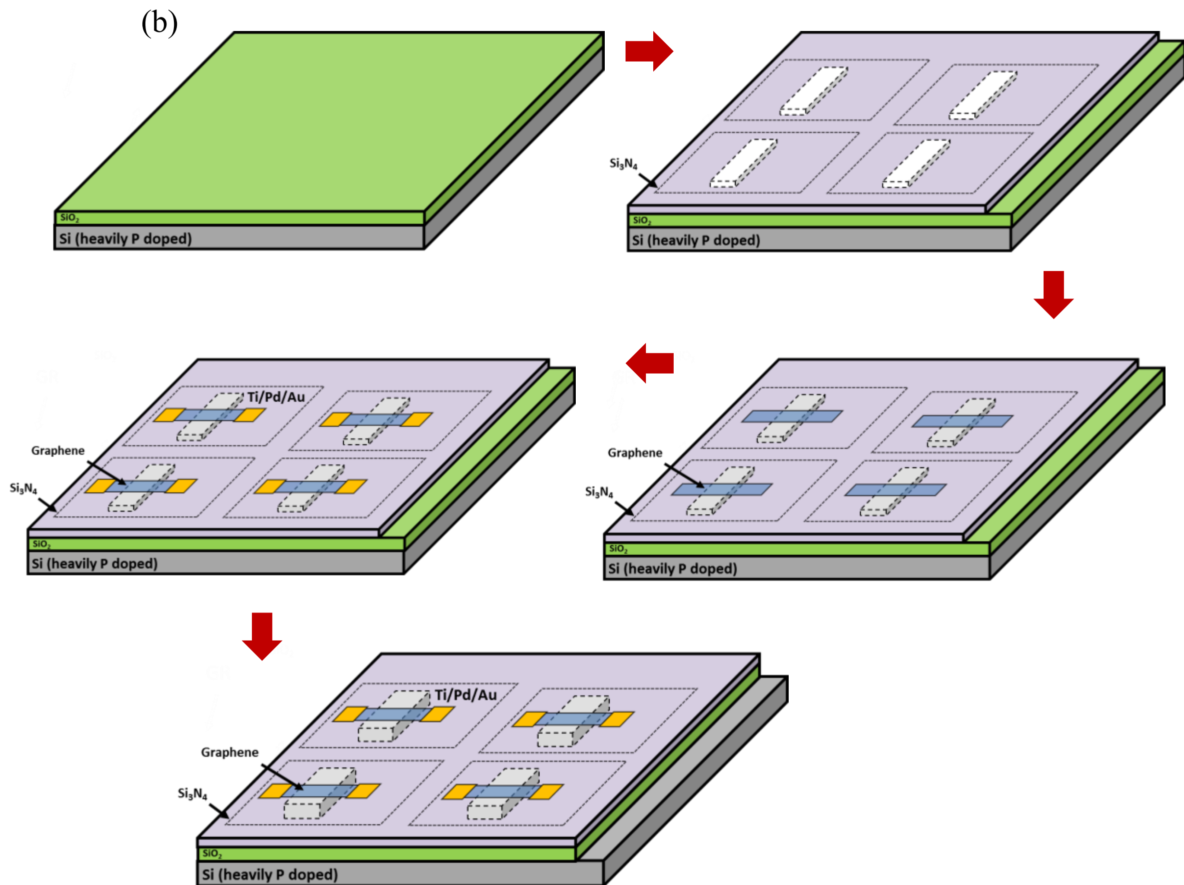


Figure 4. 2 A new CMOS-compatible fabrication flow for making gNEMS ESD switch devices.

A fully CMOS-compatible device fabrication process flow is critical to achieve 3D heterogeneous integration of the proposed gNEMS switch structures with ICs, hence realize the novel above-IC ESD protection concept. Figure 4.2 (a) illustrates the device fabrication process flow developed in this work. First, a Si_3N_4 thin layer of 100nm was grown on a heavily doped p-type Si wafer by low pressure chemical vapor deposition (LPCVD), followed by etching to define the gNEMS vacuum chamber. Si_3N_4 was used to

prevent graphene lift-off from electrode pads during SiO_2 etching. Second, single (or many) layer graphene film was grown by CVD method, which allows large area graphene film fabrication, followed by was characterization using Raman spectroscopy (Figure 4.3a). The graphene film was then transferred to the Si substrate. Next, the graphene film was patterned by oxygen plasma to form graphene beams (or other shapes as desired). The top electrodes were made of Ti/Pd/Au (5/30/50nm) by deposition. To avoid graphene sticking to the bottom SiO_2, the graphene membrane was released using hydrofluoric (HF) steaming due to the hydrophilic property of monolayer graphene [41]. The new gNEMS switch was then formed and its gap depth can be readily controlled by HF steam etching time. Figure 4.3 (b & c) shows the SEM image of a gNEMS ESD switch fabricated, which clearly shows the suspended graphene membrane over the cavity.

Figure 4.2 (b) illustrates the new CMOS-compatible process flow that we developed to fabricate gNEMS ESD devices for 3D review. First, a thin layer of 100nm-thick Si_3N_4 was grown by LPCVD on a heavily doped p-type Si wafer followed by etching to form an air chamber. Second, single layer graphene grown by CVD method was transferred to the Si substrate. Next, graphene was patterned by oxygen plasma etching. Then, a Ti/Pd/Au (5/30/50nm) layer was deposited to form the contact for the graphene ribbons. Finally, the graphene membrane was released by HF steam etching. A dual-directional above-IC gNEMS ESD switch is hence formed as shown in Figure 4.2 (b). This post-CMOS process module can be readily integrated into normal CMOS fabrication flows.

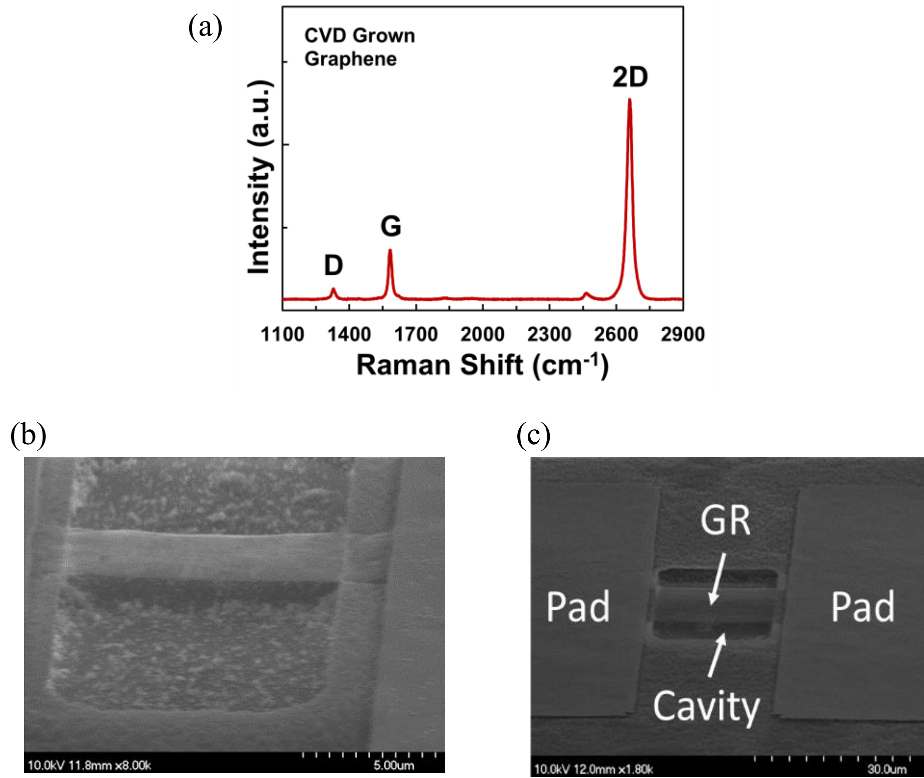


Figure 4. 3 (a) Raman spectroscopy showing monolayer graphene film. (b) & (c) SEM image of a fabricated gNEMS ESD switch device showing a suspended graphene ribbon (L=10µm, W=3µm) over the air chamber.

4.2 Characterization & Discussions

4.2.1 Design Splits & Testing Conditions

Comprehensive transient ESD characterization and statistical analysis of the gNEMS ESD switches were conducted using TLP measurement (Barth Model 4002) to emulate HBM ESD behaviors. Influences of TLP pulse shapes on gNEMS device performance were characterized using varying TLP pulse rise time and duration, i.e., t_r = 0.2/2/10ns and t_d = 75/100/150ns, as shown in Table 4.1. In this work, we focused on critical ESD discharging behaviors of gNEMS switch structures, including ESD triggering voltage (V_{t1}), ESD discharging resistance (R_{ON}), and ESD failure current ($I_{t2,}$ and its current density J_{t2}). It is noted that the measured ESD-critical parameter values show a wide distribution across samples for two possible factors: the GR sample quality is not well-controlled yet due to current graphene growth processes and GR testing is very sensitive to TLP testing conditions. Therefore, statistical analysis is more meaningful.

After initial discovery of the transient ESD discharging behavior for the new gNEMS switch, further systematic characterization of the gNMES structures were conducted using a large set of gNEMS devices, which is a critical task for design and optimization of gNEMS ESD structures for practical ESD protection circuits. We report a comprehensive measurement and statistical analysis of gNEMS structures by fast TLP testing human body model (HBM) ESD protection. The focus of this work is to get into the statistical insights into the transient ESD discharging I-V behaviors and the influences of the gNEMS design dimensions (graphene ribbon length, L, and width, W) and the ESD pulse waveforms (pulse rise time, t_r, and duration, t_d) of the TLP tester, which are critical

to practical ESD protection designs. Table 4.1 summarizes the gNEMS design splits and TLP testing conditions. The TLP tester used in this work is Barth Model 4002. Various device parameters (i.e., design splits) were used for the gNEMS prototypes, including chamber depth (d=350nm), graphene membrane film length (L= 7/10/15/20μm) and width (W=5/7/10μm).

Table 4. 1 gNEMS design splits and TLP testing conditions.

L (μm)	W (μm)	t_d (ns)	t_r (ns)
5/7/10/15	3/5/7/10/15	75/100/150	0.2/2/10

4.2.2 DC Testing

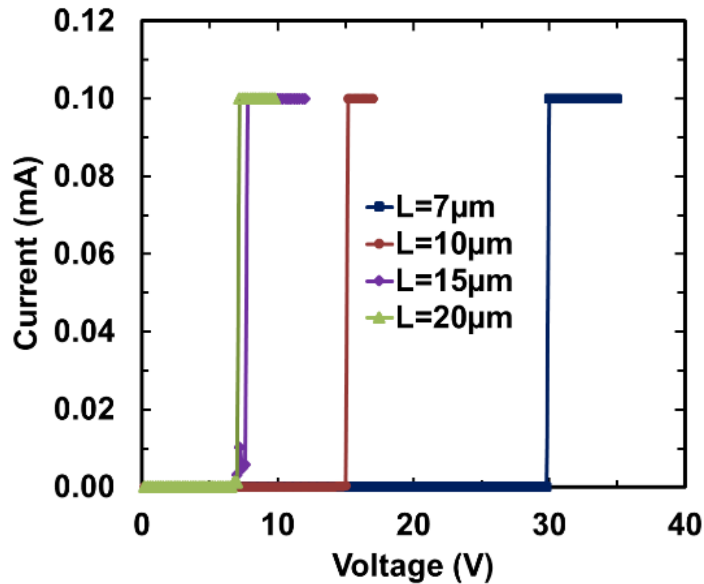


Figure 4. 4 DC sweeping test for sample gNEMS devices shows static switching effect with V_{ON} affected by the graphene membrane length (7.0, 7.6, 15, 29.8V).

Static switching effect was first characterized by applying a DC bias. Figure 4.4 shows the DC switching behaviors for sample gNEMS devices. Dependence of the turn-on voltage (V_{ON}) on the chamber depths and graphene membrane beam lengths are readily observed.

4.2.3 Transient TLP Testing

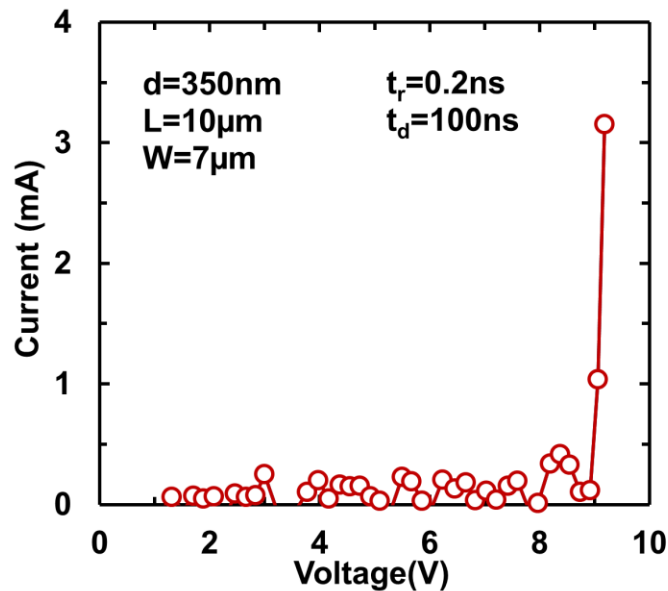


Figure 4. 5 Measured I-V curve by TLP pulsing for a prototype gNEMS device shows transient ESD switching with a fast response time down to 200ps.

Fig. 4. 5 depicts measured ESD discharging I-V curve of a graphene NEMS ESD switch device (L=10μm, W=7μm & d=350nm) under a TLP stressing pulse (t_r=0.2ns & t_d=100ns). Before ESD triggering, the measured leakage current is as low as pA level, which resolves the inherent leakage problem associated with all in-Si ESD protection structures. The gNENS ESD switch is triggered at V_{t1}~8.92V to discharge the TLP surge,

showing an ESD transient current handling capability of at least I_{t2}~3.15mA, or, J_{t2}~1.28x10^{8}A/cm^2, equivalent to a HBM ESD protection capability of ~1500V/μm^2, at least two orders of magnitude higher than the most robust in-Si SCR ESD protection structure (~7.5V/μm^2). In addition, the gNEMS switch shows ultra-fast ESD discharging behavior, responding to a TLP ESD pulse of t_r=200ps.

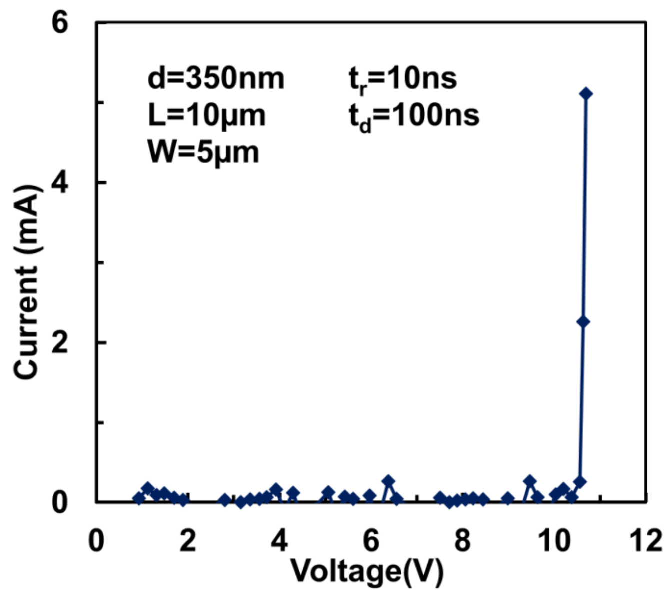


Figure 4. 6 Measured transient ESD I-V curve for a sample gNEMS switch by TLP stressing.

Figure 4.6 gives a transient I-V curve for a sample gNEMS switch (L=10µm, W=5µm, air chamber depth d=350nm) under TLP stressing (t_d=100ns, t_r=10ns), which clearly shows the desired ESD discharging I-V characteristics. The measured leakage current in the OFF state is ultra-low, I_{leak} ~ 1pA, due to the non-PN-type mechanical switch mechanism. The measured ESD triggering is V_{t1} ~ 10.4V and the ESD current handling

capability, I_{t2}>5mA, is very high, or, a current density of $J_{t2} \sim 2.9 \times 10^{8}$A/cm^{2}, much higher than any traditional in-Si PN-type ESD protection structures.

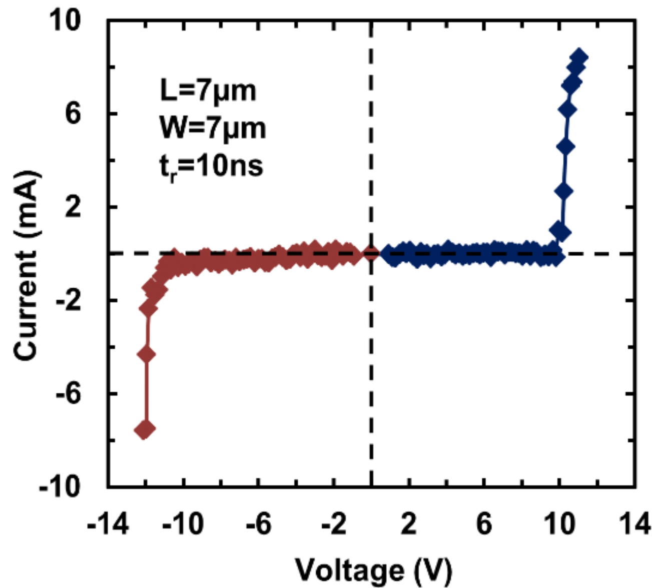


Figure 4. 7 Measured I-V curve by TLP for a prototype gNEMS device shows near symmetric I-V switching behaviors desired for ICs. The slight asymmetry is attributed to the asymmetric prototype device structure used.

Figure 4.7 depicts a near symmetric switching I-V behavior, which is highly desirable for full-chip ESD protection to reduce ESD device head counts [1-2], hence ESD area size and parasitic effects. The transient switching effect induced by fast ESD pulse may be quite different from static switching set by a DC bias in that DC switching may be triggered by graphene mechanical and electrostatic forces, while transient switching shall be greatly affected by extra pull force associated with the large and sudden change in electrostatic force density induced by an ESD pulse. Hence, a lower V_{t1} threshold and much fast switching time are expected that were confirmed in TLP testing.

4.2.4 Device Dimension Effects

Graphene Length

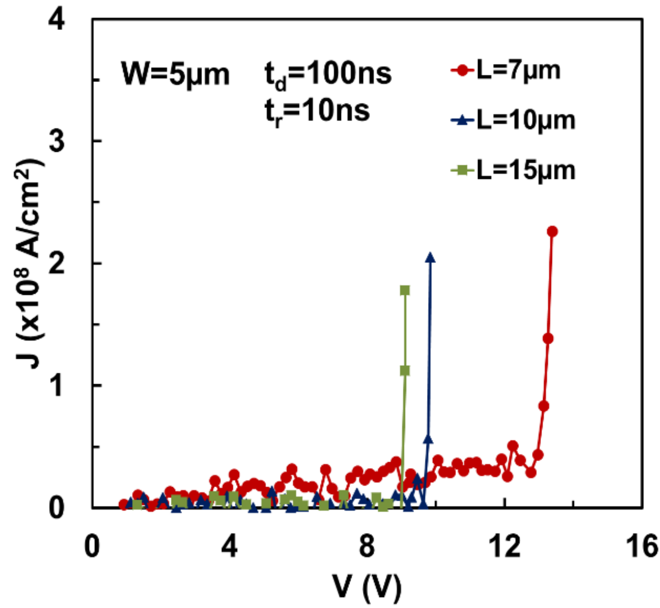


Figure 4. 8 Measured transient J~V characteristics of gNEMS switches with different graphene length (L=7/10/15µm, W=5µm) by TLP testing show that V_{t1} increases as L decreases.

Figure 4.8 shows the measured transient J-V characteristics by TLP testing (t_r=10ns, t_d=100ns) for a set of gNEMS samples with varying length of L = 7/10/15µm for a given W=5µm. It is observed that the ESD V_{t1} decreases (12.8V, 9.6V to 9V) and J_{t2} drops (2.26, 2.05 to 1.78 x10^8 A/cm^2) as L increases. This is attributed to an increased resistance and, possibly, more defects in longer graphene ribbons. This observeation is confirmed in statistical analysis.

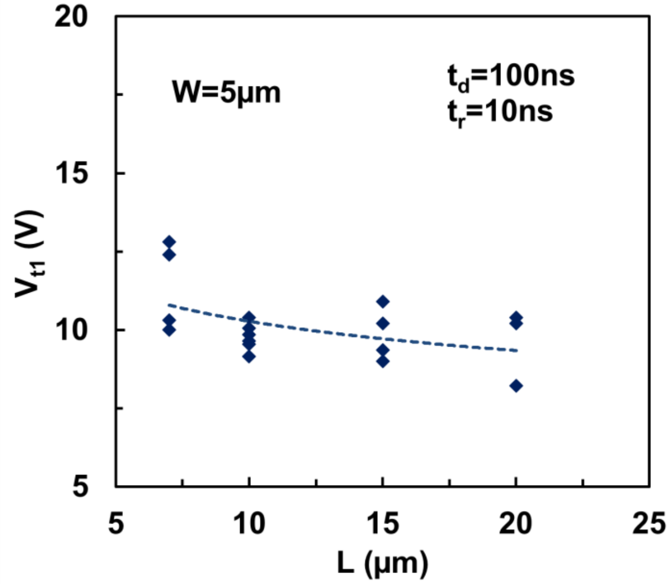


Figure 4. 9 Statistical V_{t1} ~ L (W=5μm) for gNEMS devices from TLP measurement shows a monotonic relationship.

Figure 4.9 gives the statistical characteristics of V_{t1} versus L (W =5μm) for a group of gNEMS samples by TLP testing. It is found that V_{t1} decreases monotonically as L desreases. To model the gNEMS triggering behavior, the equation for pull-in voltage of a conventional MEMS electromechanical switch is utilized [44-46],

$$V_{pull\text{-}in}=(8K_{eff}\times d_0^3/(27\varepsilon_0\times A_{eff}))^{1/2} \quad (4.1)$$

where K_{eff} is the effective stiffness of the membrane that is proportional to the membrane aspect ratio of W/L^3, d_{00} is the gap distance at zero bias voltage, ε_0 is the free space electrical permittivity and A_{eff} is the effective area for the deflection membrane related to L. Hence, the pull-in voltage of a conventional MEMS switch is proportional to $\sqrt{1/L^2}$. For the new gNEMS switch under fast ESD transient stressing, we propose a model for its ESD triggering voltage as,

$$V_{t1} \sim (1/L^{\gamma})^{1/2} \tag{4.2}$$

From the statistic V_{t1} ~ L behavior, the fitting number $\gamma\gamma$ can be extracted, depicting the critical relationship between the transient ESD V_{t1} and the graphene membrane length L.

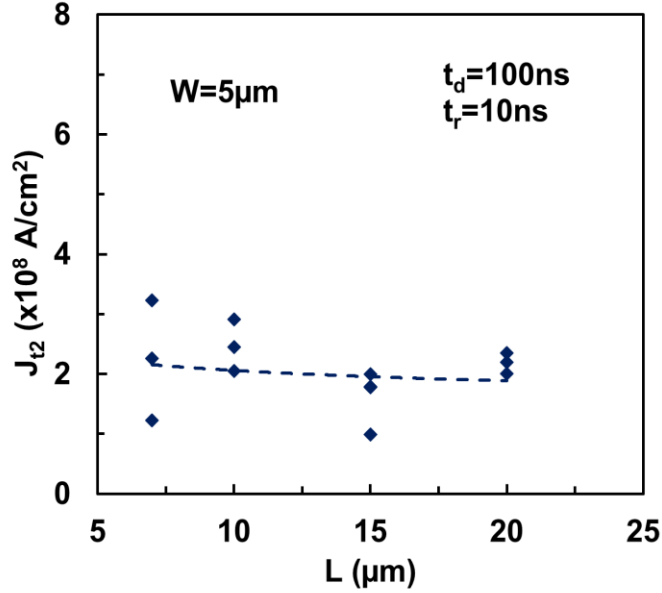


Figure 4. 10 Statistical J_{t2} ~ L characteristics of gNEMS switches (W=5μm) by TLP testing shows that J_{t2} slightly degraded for longer graphene ribbons.

Figure 4.10 presents the measured statistical behavior of ESD J_{t2} versus L for the gNEMS switches (W=5μm) by TLP testing. The measured peak ESD current density, J_{t2}, reaches to a very high level of ~10^8 A/cm^2, suggesting superb ESD current handling capability of the new gNEMS switch, apparently attributed to the graphene properties. It is observed that the ESD J_{t2} decreases slightly as L increases, which may be attributed to more defects in longer graphene membranes associated with the graphene film quality (structural and/or from contamination). This problem may be resolved by improving the

graphene growth processes in future. Figure 4.11 shows the trench of V_{t1} and J_{t2} as the relationships of graphene length L at the trench depth of d=750nm.

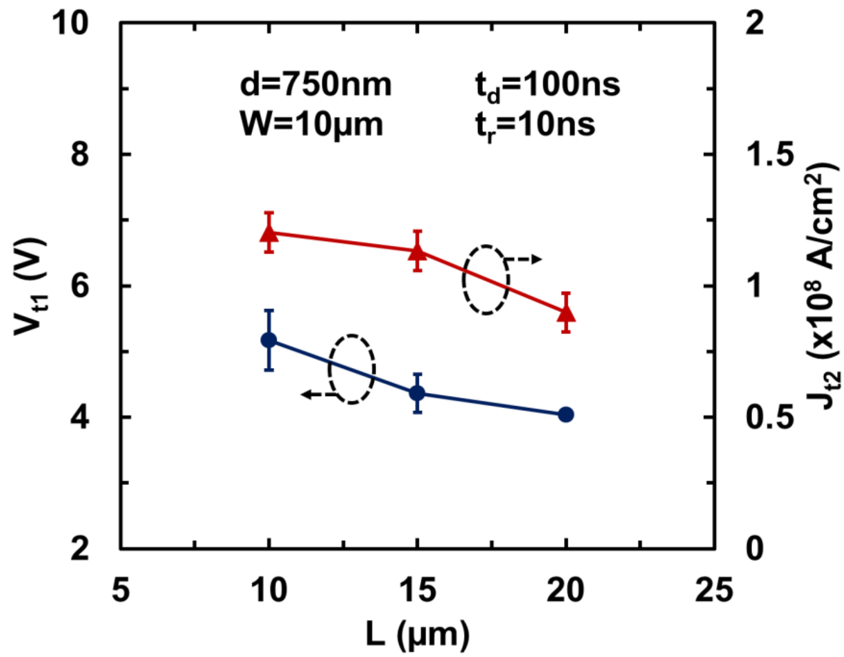


Figure 4. 11 Statistical J_{t2} ~ L characteristics of gNEMS switches (W=5μm) by TLP testing shows that J_{t2} slightly degraded for longer graphene ribbons.

Graphene Width

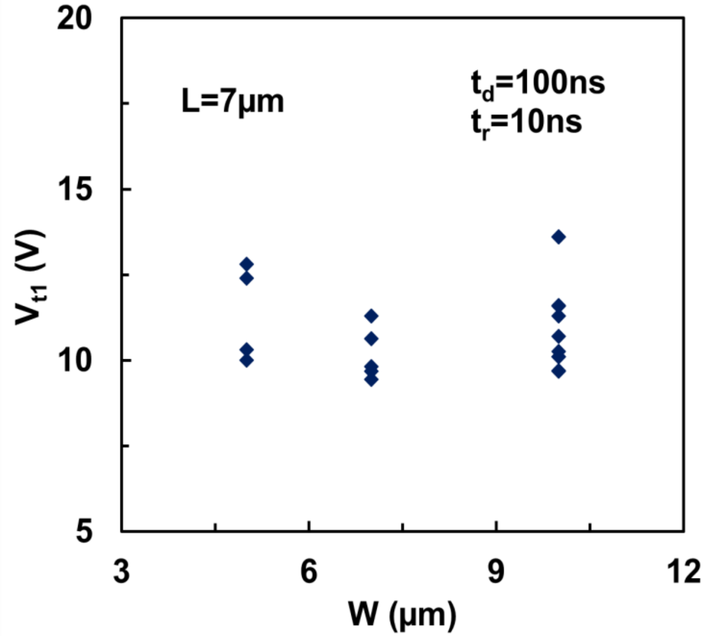


Figure 4. 12 Statistical Vt1 ~ W characteristics (L=7µm) for gNEMS devices (d=350nm) by TLP testing suggests that Vt1 seems to be insensitive to W.

Figure 4.12 depicts the measured statistical V_{t1} ~ W behaviors for gNEMS switch samples (L = 7µm) obtained by TLP testing. It seems that the ESD triggering voltage V_{t1} is insensitive to the graphene ribbon width W. Figure 4.13 presents the measured statistical characteristics of I_{t2} ~ W for gNEMS switches (L = 7µm) obtained by TLP testing. It is observed that the ESD current handling capability, I_{t2}, increases with the graphene membrane width W as expected. Figure 4.14-Figure 4.16 shows the graphene membrane width effects for gNEMS switches with trench depth of 750nm.

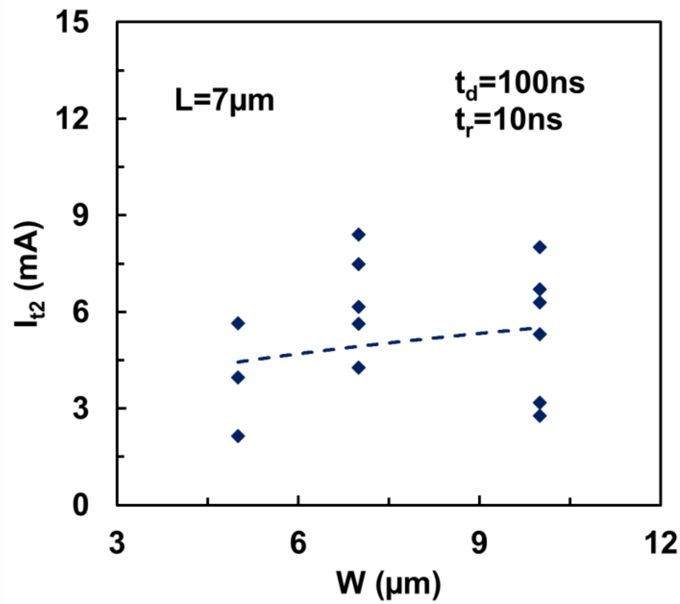


Figure 4. 13 Statistical I_{t2} ~ W characteristics (L=7μm) for gNEMS devices (d=350nm) by TLP testing shows dependence of ESD I_{t2} on W.

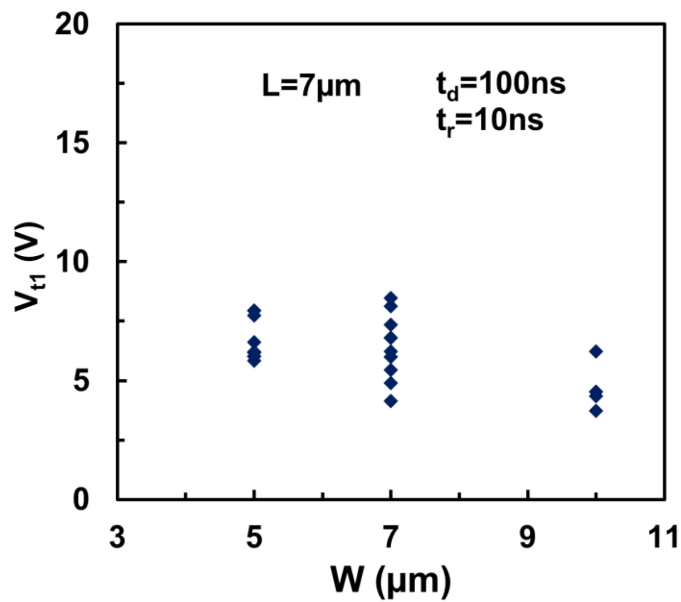


Figure 4. 14 Statistical I_{t2} ~ W characteristics (L=7μm) for gNEMS devices (d=750nm) by TLP testing shows dependence of ESD I_{t2} on W.

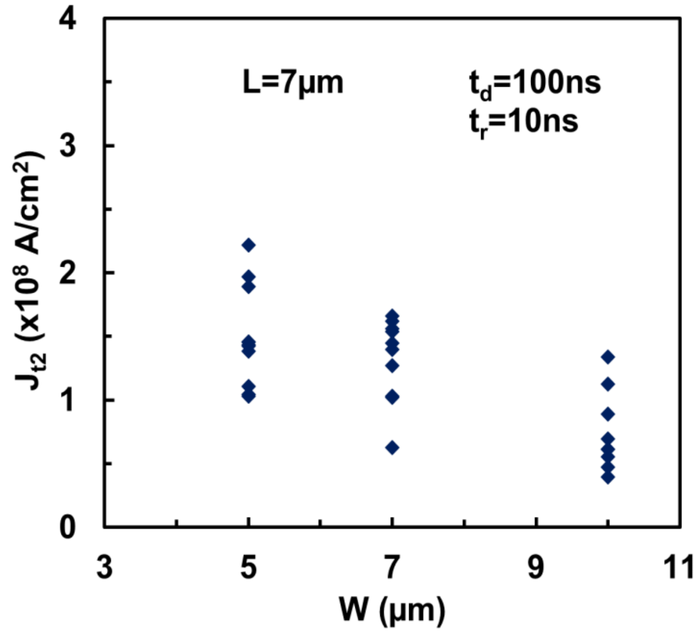


Figure 4. 15 Statistical I_{t2} ~ W characteristics (L=7μm) for gNEMS devices (d=750nm) by TLP testing shows dependence of ESD I_{t2} on W.

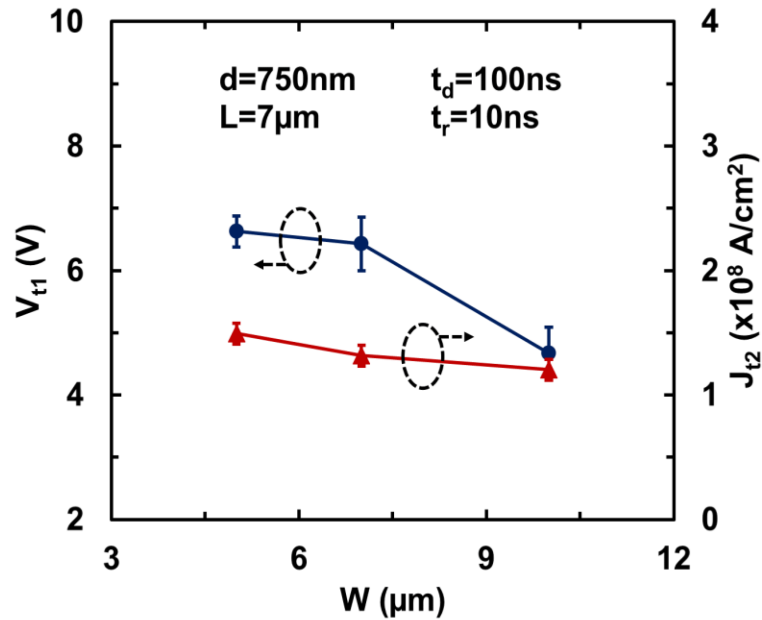


Figure 4. 16 Statistical I_{t2} ~ W characteristics (L=7μm) for gNEMS devices by TLP testing shows dependence of ESD I_{t2} on W.

Trench Depth

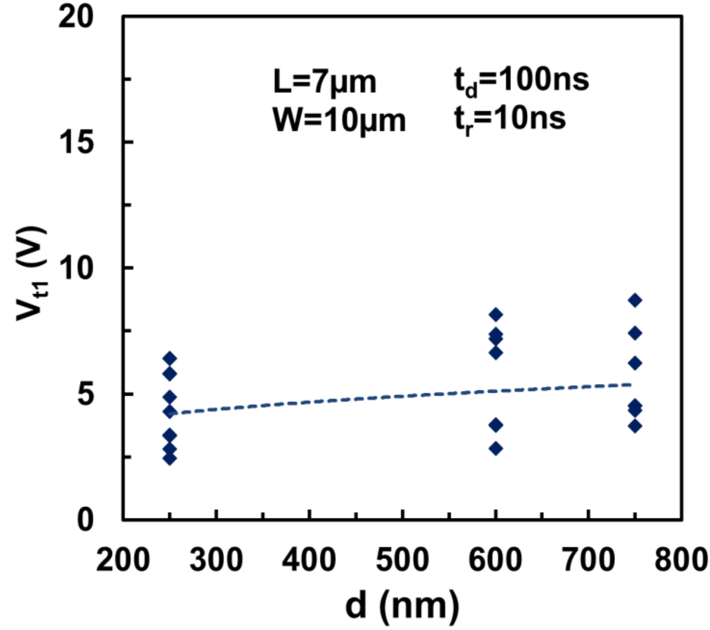


Figure 4. 17 Statistics for V_{t1} versus trench depth (d=250/600/750nm) for gNEMS switch samples of a fixed L=7µm and W=10µm obtained by TLP testing (t_d=100ns, t_r=10ns).

Figure 4.17 depicts the statistical characteristics of V_{t1} versus trench depth d (L=7µm, W = 10µm) for a group of gNEMS samples by TLP testing (t_r=10ns, t_d=100ns). It is found that V_{t1} increases monotonically as trench depth increases. This is because it requires a higher triggering voltage for graphene membrane touching down to bottom to discharge the ESD surges at larger trench depth. A fitting equation is also proposed from Equation 3 to model this characteristic,

$$V_{t1} \sim (d^{\beta})^{1/2} \qquad (4.3)$$

where β is the fitting parameter to describe the V_{t1} dependence of the gNEMS trench depth. Here, β is extracted as ~1.36 in Figure 4.17, smaller than the dependence of pull-in voltage and trench depth (β=3) in conventional MEMS switches by DC triggering [44-46]. This is

also attributed to the graphene membrane over the trench triggered by transient ESD surges, opposed to the conventional MEMS switches.

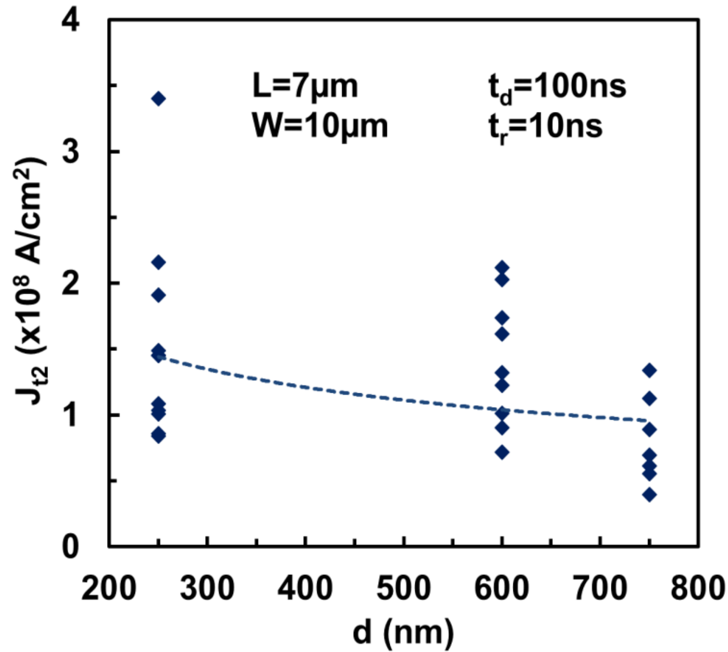


Figure 4. 18 Statistics for J_{t2} of gNEMS samples with varying trench depth (d=250/600/750nm) of a fixed L=7µm, W=10µm obtained by TLP (t_d=100ns, t_r=10ns).

Figure 4.18 gives measured statistical J_{t2} ~ d behaviors for gNEMS switch samples (L = 7µm, W = 10µm) obtained by TLP testing. The measured J_{t2} with high level of ~10^8 A/cm^2, also demonstrating high ESD robustness of gNEMS switches. The measured statistics show slight decrease of J_{t2} as trench depth increases, which is possibly because at increased depth, graphene ribbons bend at larger curvatures, that may induce more defects along the graphene, as a result, making graphene easier to breakdown, hence, the J_{t2} degrades.

R

The measured transient dependence of the ESD discharging resistance (R_{ON}) on the dimensions of gNEMS switches by TLP testing is depicted Figure 4.19. For the group of gNEMS devices measured, with varying graphene membrane sizes (L×W from 7µm×5µm to 15µm×10µm), a strong relationship between the gNEMS device size and R_{ON} is observed. In general, it seems that R_{ON} is lower for a larger gNEMS device. The contribution factors may be involving: First, as the graphene membrane size increases, the contact area of graphene, when pulled down to touch the bottom electrode by the electrostatic force, will increase, resulting in a reduced contact resistance, hence a lower R_{ON}. Second, as the graphene membrane becomes larger, more defects may exist in the graphene film that may degrade the conduction. This observation suggests that quality control of graphene growth and device structure designs are important for optimization of the gNEMS switch structures for ESD protection.

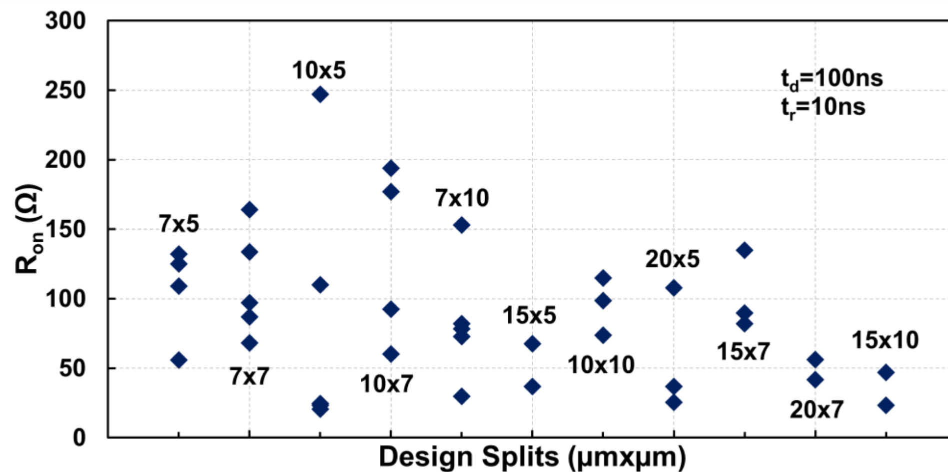


Figure 4. 19 Measured ESD discharging R_{ON} distribution for sample gNEMS devices shows dependence of the device dimensions.

4.2.5 ESD Pulse Shape Effects

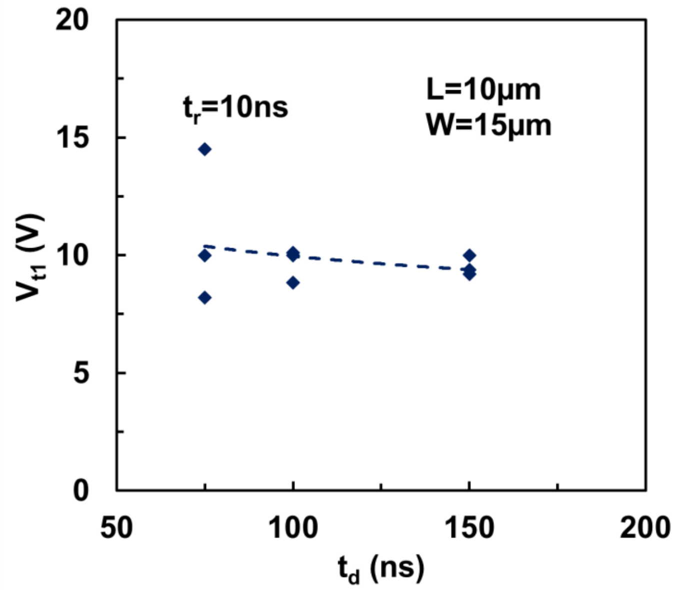


Figure 4. 20 Statistics of V_{t1} ~ t_d characteristics by TLP testing (t_d = 75/100/150ns at t_r=10ns) for gNEMS switch samples (L=10μm, W=15μm) shows influence of t_d on transient ESD triggering voltage.

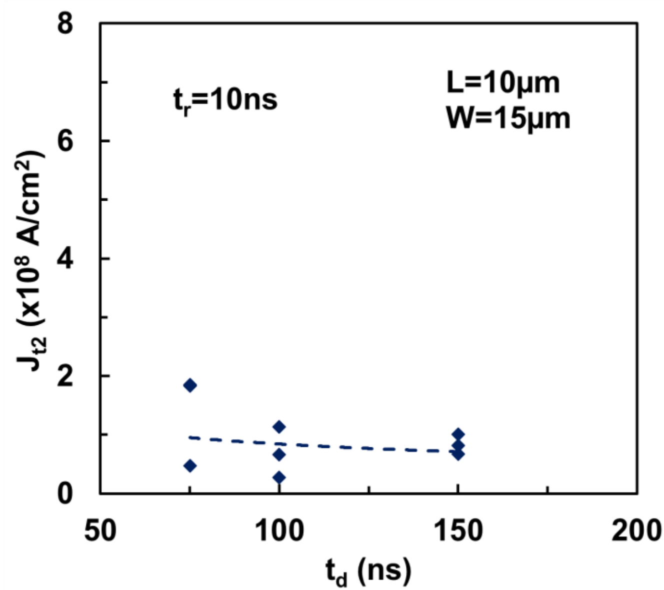


Figure 4. 21 Statistics of J_{t2} ~ t_d characteristics by TLP testing (t_d = 75/100/150ns at t_r=10ns) for gNEMS switch samples (L=10μm, W=15μm) shows influence of t_d on ESD discharging capacity J_{t2}.

For the very fast transient ESD discharging characteristics, it is important to investigate the gNEMS switching behaviors under different TLP testing conditions, which was conducted by using TLP pulses with different waveform rise time (t_r) and duration (t_d) in this work for a large group of gNEMS devices. Figure 4.20 depicts the measured statistical ESD V_{t1} behaviors under different t_d of TLP pulse (fixed t_r =10ns), which clearly shows that V_{t1} drops as TLP pulse becomes wider. This behavior is attributed to a longer graphene response time to a shorter TLP pulse, which hence requires a stronger electrostatic force to trigger the gNEMS switch under a shorter ESD pulse. Figure 4.21 presents the measured statistical J_{t2} ~ t_d relationship by TLP zapping with varying t_d (fixed t_r =10ns) for gNEMS switch samples (L=10μm, W=15μm). It is observed that the ESD current handling capability, J_{t2}, decreases slightly as t_d increases, likely due to the more energy accumulation for a longer ESD pulse. Figure 4.22 shows the relationships of V_{t1} and J_{t2} with t_d at gNEMS trench depth of d=750nm.

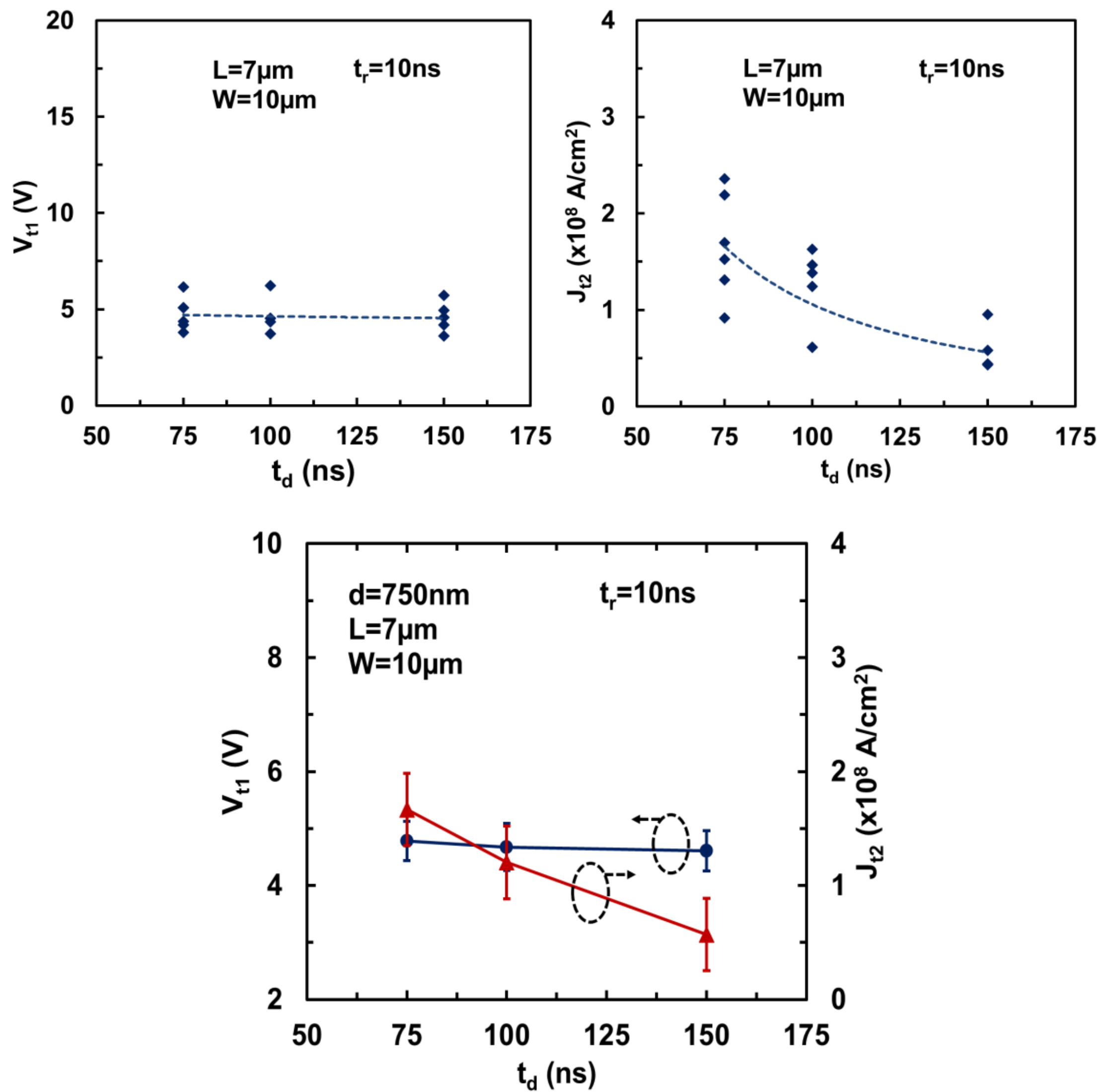


Figure 4. 22 Statistics of J_{t2} ~ t_d characteristics by TLP testing (t_d = 75/100/150ns at t_r=10ns) for gNEMS switch samples (L=10μm, W=15μm) shows influence of t_d on ESD discharging capacity J_{t2}.

Figure 4.23 shows the statistics of measured V_{t1} with respect to t_r and Figure 4.24 depicts the statistical J_{t2} related to t_r of the TLP pulses. Since the rise time of the TLP pulse waveform is much smaller than its duration, no obvious influences of t_r on the ESD triggering and current handling capability of the gNEMS devices was observed. Figure 4.25 shows the relationships of V_{t1} and J_{t2} with t_r at gNEMS trench depth of d=750nm.

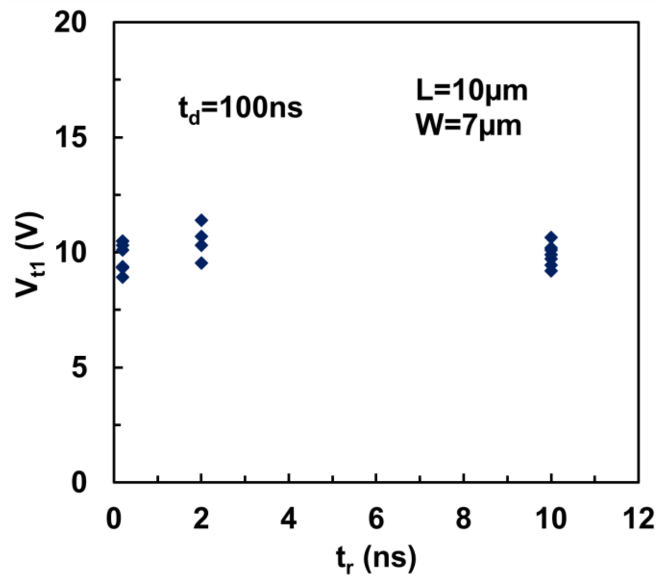


Figure 4. 23 Statistics of V_{t1} ~ t_r characteristics by TLP testing (t_r = 0.2/2/10ns at t_d=100ns) for gNEMS switch samples (L=10µm, W=7µm).

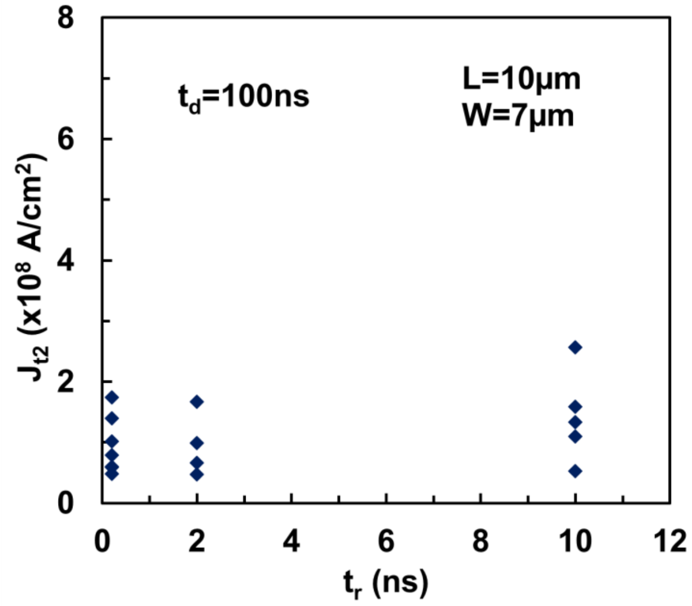


Figure 4. 24 Statistics of J_{t2} ~ t_r characteristics by TLP testing (t_r = 0.2/2/10ns at t_d=100ns) for gNEMS switch samples (L=10µm, W=7µm).

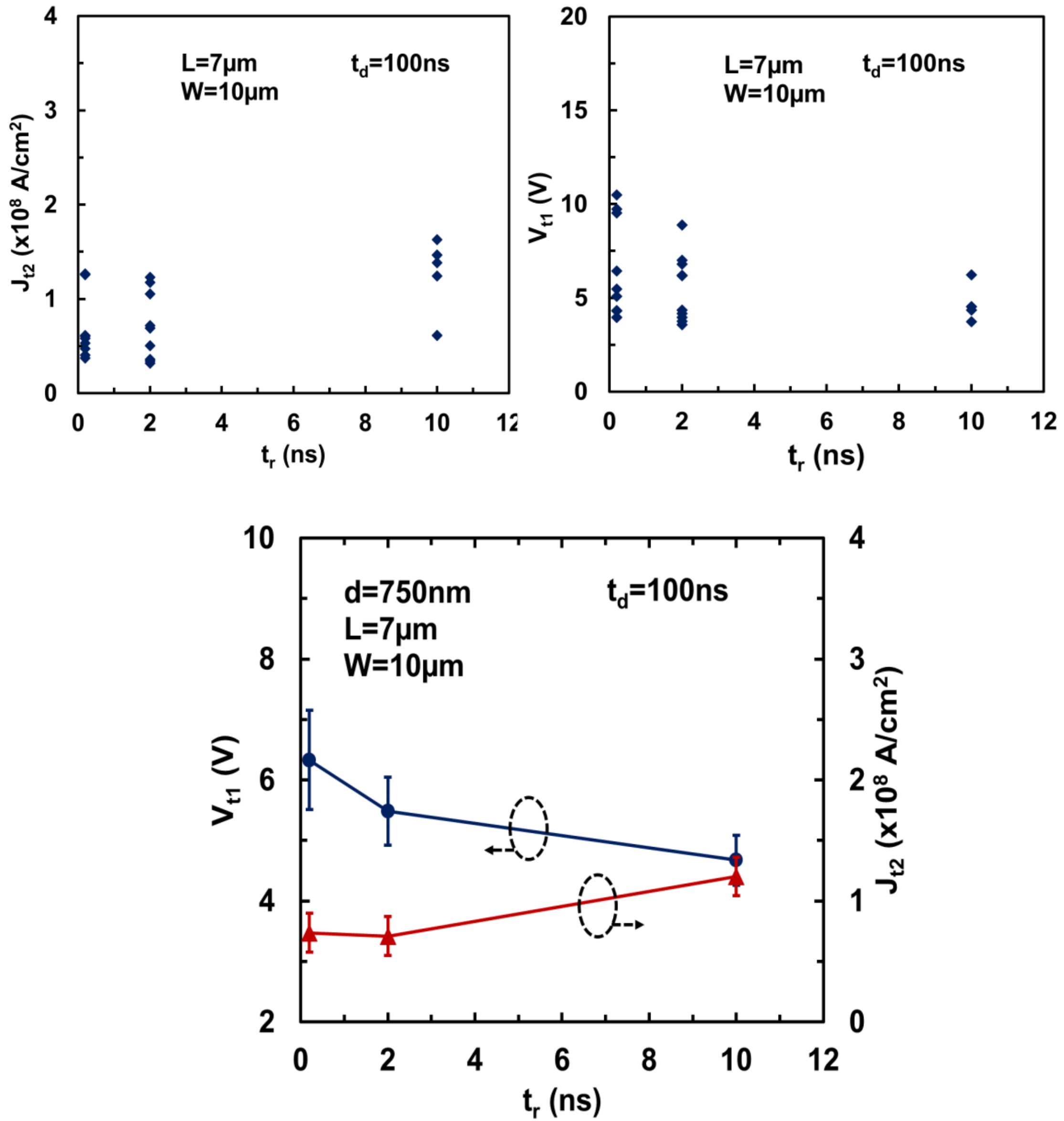


Figure 4. 25 Statistics of $V_{t1} \sim t_r$ characteristics by TLP testing (t_r = 0.2/2/10ns at t_d=100ns) for gNEMS switch samples (L=10µm, W=7µm).

4.2.6 Temperature Test

Figure 4.26 shows that the gNEMS device works at up to T=110ºC. TLP characterization (t_d=100ns, t_r=10ns) was conducted for graphene switch samples at different temperature points of -10ºC and +110ºC. Graphene NEMS ESD switch works at up to T=-10ºC/110ºC. Clearly showing the robustness of graphene switch working in extreme temperatures (at least -10ºC/110ºC).

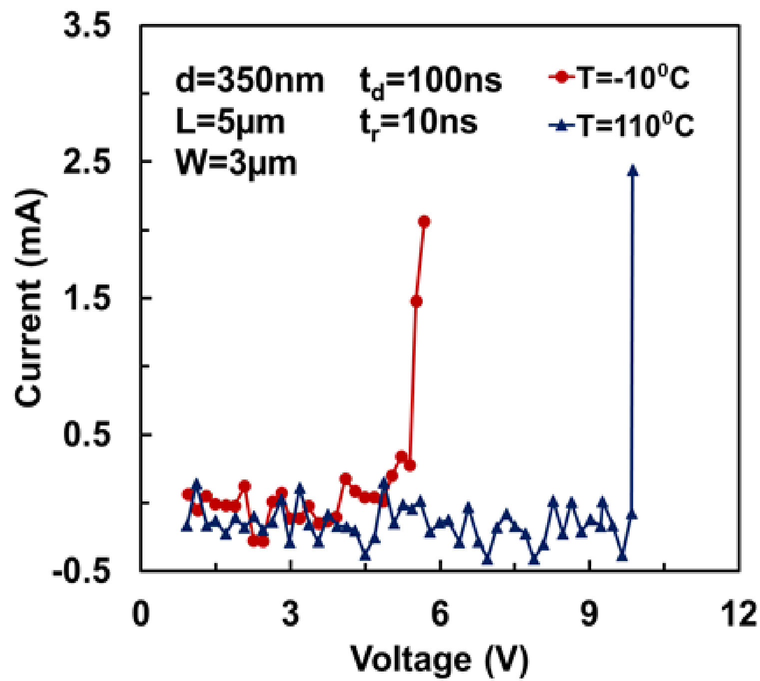


Figure 4. 26 Graphene NEMS switch tested in extremely high and low temperatures.

4.2.7 Reliability Test

Reliability of the new gNEMS switch structures were characterized by repeating ESD switching tests by TLP and VFTLP stressing. It was observed that the sample gNEMS devices maintained good switching property after 30 switching stress tests. The gNEMS devices may further improved by design optimization in order to qualify gNEMS switches for practical ESD protection designs. Our on-going optimization research include graphene growth, switch structures and fabrication processes. For example, graphene quality must be controlled for better switch reliability and dielectric leakage has to be avoided.

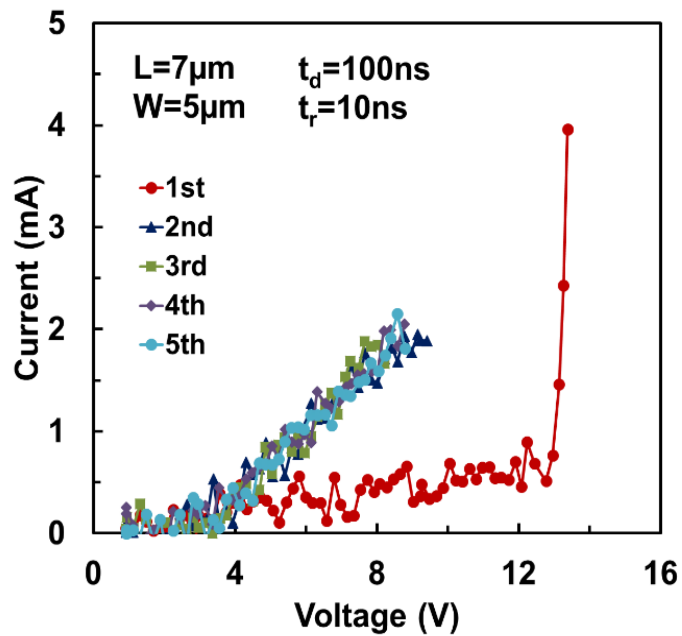


Figure 4. 27 TLP characteristic of graphene ESD switch (L=7μm, W=5μm) for 5 times. V_{t1} degrades after the second test. The R_{ON} increases due to the leakage from dielectrics.

Robust graphene ESD switch is required for reliable ESD protection solution. Here, multiple times ESD zapping was performed to study the robustness of the new graphene ESD switch. From Figure 4.27, one graphene ESD switch sample was tested by TLP for 10 times, the switching effect was degraded after first time zapping, the V_{t1} decreased from 12.8V to 4V and R_{ON} ramps up largely. This is probably due to that graphene is not able to reverse back to the original locations by the graphene-contact stickiness change after electrostatic charge induced vibration. In addition, graphene mechanical and electrical properties are modified by the Joule heating induced defects redistribution and destruction. Furthermore, the leakage current enlargement is probably from the dielectrics, caused by ESD pulses. The undesirable degradation can be solved by improving the CVD-grown graphene quality, dielectric quality and better graphene-contact quality. Over 30 successive ESD zapping was performed to our graphene ESD switch device without inspecting device failures, ensuring the robustness of the new switching device.

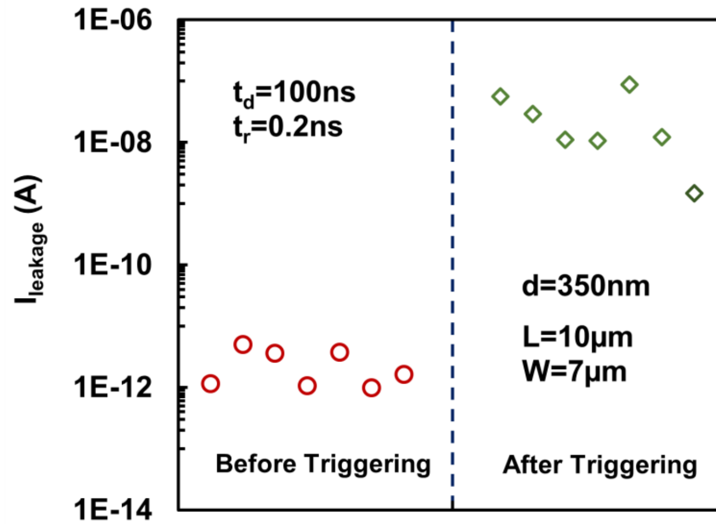


Figure 4. 28 DC leakage current testing of graphene ESD switch (d=350nm, L=10μm, W=7μm) before and after triggering. The leakage current ramps up after the device turns on.

The DC leakage test is performed after each TLP cycle (DC voltage is set as 0.5V). Figure 4.28 shows the DC leakage current before and after gNEMS switch triggering for several devices with same dimensions. In the figure, before device turns on, the leakage current is as low as pA, ensure the extemely low parasitics of this device. While after triggering, the leakage current ramps up larger to the orders of 10^{-8} A. This is probably due to that graphene is not able to reverse back to the original locations by the graphene-contact stickiness change after electrostatic charge induced vibration. In addition, graphene mechanical and electrical properties are modified by the Joule heating induced defects redistribution and destruction. Furthermore, the leakage current enlargement is probably from the dielectrics, caused by ESD pulses. The undesirable degradation can be solved by

improving the CVD-grown graphene quality, dielectric quality and better graphene-contact quality, ensuring the robustness of the new switching device.

4.3 Failure Analysis

Figure 4.29 shows the SEM images after graphene switch failures by TLP stresses (t_d=100ns, t_r=10ns), It is readily observed that a major vacancy appears across the graphene ribbons and a graphene islands shows at the center of the basil regions. This is probably due to the graphene sticked to the trench bottom during vibration. We suspect that the failure mechanism is not only from the thermal failures, but also from non-thermal effects including mechanical breakdowns.

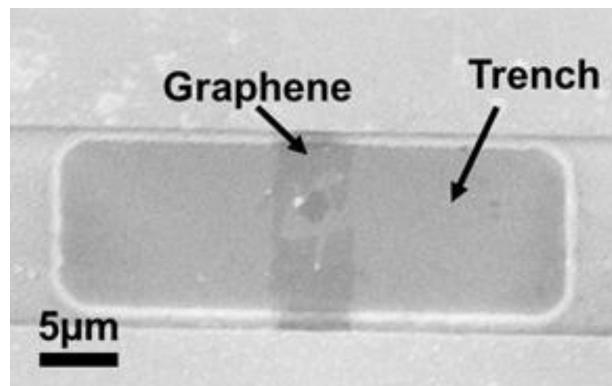


Figure 4. 29 SEM image of graphene ESD switch (d=350nm, L=10μm, W=5μm) after TLP stressing. Graphene ribbon shows an explicit discontinuous vacancy by the transient pulses, indicating the graphene switch breakdown.

4.4 Conclusion

We report the first transient graphene gNEMS ESD switch concept. Experiments shows ultra-fast ESD switching effect of 200ps and the ESD triggering V_{t1} can be controlled by design splits. A CMOS-compatible process flow was developed to allow 3D heterogeneous integration with ICs. The novel above-IC gNEMS ESD switch structure offers a revolutionary on-chip ESD protection solution for future ICs

We also report a comprehensive characterization and statistical analysis of graphene NEMS switch structures for ESD protection by transient TLP measurements. It is found that the new graphene mechanical switch can be used as a transient ESD protection structure. Measurement statistics reveals the details of dependence of transient ESD behaviors on gNEMS device dimensions and pulse shapes of TLP waveforms, which provide insights for design optimization of the new gNEMS switch structures for ESD protection. The non-traditional above-IC gNEMS switch is a typical More-Than-Moore device solution that can be integrated into CMOS through 3D heterogeneous integration for future ICs at nano nodes.

Chapter 5 Graphene Ultrasound Transducer

5.1 Introduction and Motivation

5.1.1 Ultrasound Imaging System

Ultrasound imaging utilizes ultrasonic acoustic waves to monitor organs and blood movements inside bodies, widely used in the obstetrics and gynecology, cardiology, urology and cancer detection areas [57-62]. In an ultrasound imaging system, a transducer transmits ultrasonic signals into bodies, by moving the transducer across the body surface or rotating inserted probes, ultrasound can reach tissue boundaries (e.g. between fluid, tissue and hard bones) and then reflect back. The echo waves are picked up by the transducer and sent to electronic systems. Electronic system can record the sound speed in tissues (~1,540 m/s) and the time for each sound echo. By processing the reflected waves distances and intensities, two-dimensional images can be shown on the display screen [57, 58]. The CPU includes the microprocessors, memories, batteries, power supplies and signal processing units.

In addition to 2D imaging, 3D ultrasound and Doppler ultrasound imaging are also developed for observing blood flow, fetus and early detection of tumors [59]. Unlike X-ray, ultrasonic imaging provides real-time and non-ionization radiation exams of bodies, however, it will introduce heat into the tissues and then cavitation may form; the long term side-effect remains unknown especially to fetus [58]. In an ultrasound imaging system, transducer is the core part, used to send ultrasound and receives the echoes [60-62], represented by two operation modes, one is the transmission mode, converting electrical

signals to acoustic waves (ultrasound); another is the receiving mode, which receives the ultrasound, and transmits it into electrical signals.

A basic ultrasound machine has the following parts: transducer probe - probe that sends and receives the sound waves; central processing unit (CPU) - computer that does all of the calculations and contains the electrical power supplies for itself and the transducer probe; transducer pulse controls - changes the amplitude, frequency and duration of the pulses emitted from the transducer probe; display - displays the image from the ultrasound data processed by the CPU; keyboard/cursor - inputs data and takes measurements from the display; disk storage device (hard, floppy, CD) - stores the acquired images; printer - prints the image from the displayed data. In the market, Standard ultrasound imaging machines has been used in clinics, manufactured by Philips and GE, which is not designed for home-made usage. A new portable ultrasound imaging system has been released by some companies, but the ultrasonic transducer has operation frequency lower than 30MHz, still not cheap enough and not easy to be used by household. The trend for the ultrasound imaging system is moving from the portable to wearable systems. It is highly needed in the industry and market for a high performance, wearable, user-friendly and low cost ultrasonic transducer systems.

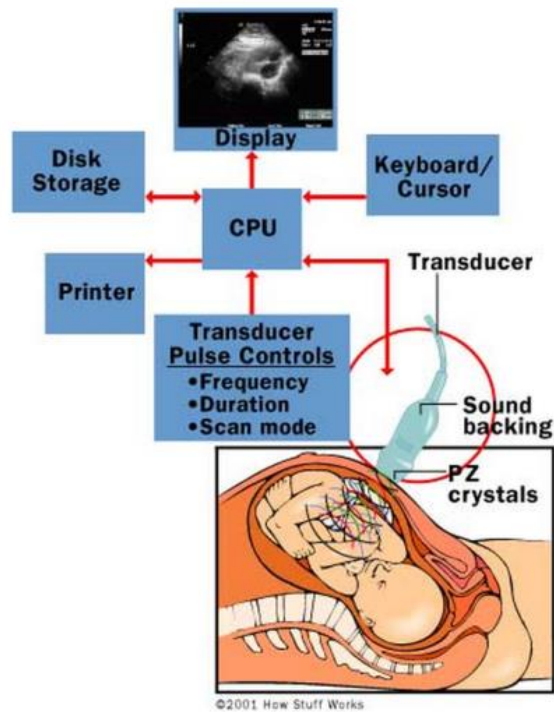


Figure 5. 1 Ultrasound imaging system [57].

Sound (Acoustic) waves propagate in the longitudinal motion instead of transverse motion. Medical waves are all longitudinal compression waves. (Both compressional and shear waves can travel into a solid, but soft tissue only support compressional waves). Ultrasound refers to wave frequencies higher than 20kHz, which is the limit of human hearing. In the field of medical imaging, frequencies 100 times higher than human audible sound, typically 2 to 20MHz are used [63] (Table 5.1). Ultrasound devices operate with frequencies from 20 kHz up to several gigahertz [60, 61]. The speed of sound in different materials is determined by material density and compressibility. In image applications, the speed of ultrasound is assumed to be 1540m/s in soft tissues. The acoustic impedance (Z) is used to characterize opposition in the acoustic flow in the ultrasound. For water, Z is

$1.48*10^6$ kg/m-s (1.48MRayl), most tissues are within ten percent of this value [63]. Ultrasound experiences scattering and reflection when propagating into human bodies. There are two types of reflected waves with respect to the reflecting surfaces. The Specular reflector refers to the echoes, which are intense, and angle dependent, originating from relatively large and regularly shaped objects with smooth surfaces. The acoustic scattering arises from objects that are size of wavelength or smaller, which are relatively small, weakly reflective, irregularly shaped objects like blood cells [63].

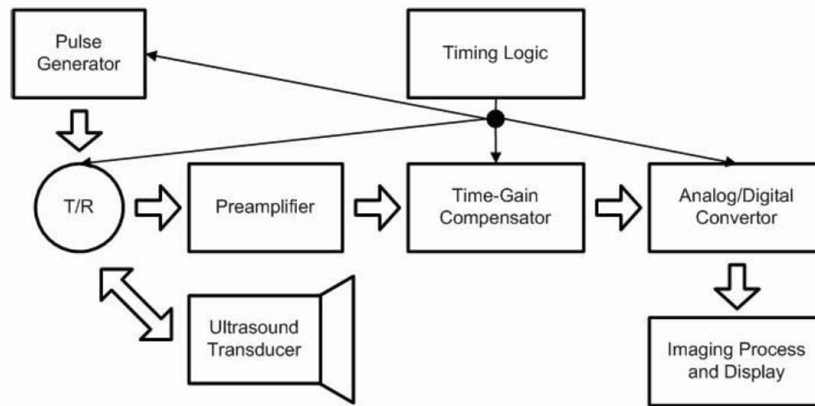


Figure 5. 2 Ultrasound imaging system with pulse generators and IC components.

In addition to the reflected waves, waves can also be absorbed by tissues and fluids. Usually higher frequencies of ultrasound have short wavelengths and are absorbed easily, as a result, high frequencies ultrasound are used for the superficial body structures and low frequencies are used for those that are deeper [60, 61]. Higher frequencies give better resolution and more detailed images, but the higher frequency sound loses energy more quickly as it travels through the body so the depth of penetration is less. The operator usually uses as high a frequency as possible. Ultrasound of these frequencies does not travel through air, so a layer of water-based coupling medium is used between probe and skin.

We understand that higher frequencies give better resolution and more detailed images, but the higher frequency sound loses energy more quickly as it travels through the body so the depth of penetration is less. For portable ultrasound systems, higher frequency (>50MHz) is able to detect the superficial tissues such as the ocular tumors and glauscoma, offering better resolutions. In addition, it can be used as biomicroscopy for low depth microscopies.

Table 5. 1 Ultrasound frequencies with depth and human body tissues detections [57-62].

Frequency (Hz)	Depth	Tissues
2.5MHz		Deep abdomen, obstetric and gynaecological
3.5MHz		General abdomen, obstetric and gynaecological
5MHz		Vascular, breast, pelvic imaging
1-6MHz	4-5cm	Deeper structures such as liver and kidney Infraclavicular and popliteal regions
3-7MHz		Peripheral vascular imaging
7.5MHz		Breast, thyroid
10MHz		Breast, thyroid, superficial veins, superficial masses
7-18MHz	2-3cm	Superficial: muscles, tendons, testes, breast, thyroid and parathyroid glands nerves in the interscalene, supraclavicular and axillary regions
20-60MHz		Intravascular imaging (probes) atherosclerotic plaque, angioplastic
50-100MHz	8-9mm	Biomicroscopy: anterior chamber of the eye, glauscoma, ocular tumors/ Small animal imaging(mice, zebrafish)

5.1.2 Ultrasound Transducers

Bulk Piezoelectric Ultrasound Transducer

Transducers containing piezoelectric materials based on piezoelectric effect are the most widely used for ultrasonic imaging. The direct piezoelectric effect means charged separation caused by mechanical stress, while the converse piezoelectric effect refers to the occurrence of stress and strain when electric field is applied. When electrical signal is applied to transducers, they vibrate or change shape rapidly, producing ultrasound that emits outward. Conversely, when the echo ultrasound hits the transducers, they convert into electrical signals [64-67].

The piezoelectric coupling coefficient k represents the ability of a piezoelectric material to transform electrical energy to mechanical energy and vice versa, depending on the shape and quality of the material. In the transducer design, a high k is preferred in order to have a higher energy conversion. Another important parameter of the piezoelectric material is the acoustic impedance (~30MRalys), which is much higher than tissues (~1.5MRalys), causing substantial acoustic energy loss during wave propagation and bad resolution and sensitivity, usually an acoustic matching layer is applied in the transducer design to reduce the impedance mismatching, but not perfectly avoid this problem [68-70]. For this kind of transducer (Bulk Piezoelectric Transducer), the longitudinal vibration mode (d33-mode) of the piezoelectric material is utilized. Thus the anti-resonant frequency of the transducer is related to the thickness of the piezoelectric layer and the longitudinal velocity of sound in the poling direction of the piezoelectric material. This direct

dependence of the resonant frequency on the layer thickness therefore limits the transducer geometry and structure for specific applications.

Today, Bulk piezoelectric transducers still dominate the commercialized medical imaging tools, but there are still challenges toward the development of the on-chip transducers design. (1) The first challenge is the piezoelectric materials, which are required to have high operation frequency, high electrical and mechanical coupling efficient, low acoustic impedance, and good thermal stability, and also be non-toxic and low cost. As a result, it is crucial to select the appropriate category and property of the piezo-materials. Piezo-materials include the organic and inorganic materials. Single crystal including quartz, relaxor based materials and poly-crystalline materials consist of the inorganic family. For organic materials, piezo-composites are the most widely used materials in medical imaging applications [68-70]. (2) The second challenge is to develop IC compatible fabrication process and integrate the transducer array with IC. In the current state work, transducer arrays or single element are built separately with CMOS wafers, and not integrated into the IC backend flow. In order to scale down the chip size for the portable and wearable applications of ultrasound machines, it is required to provide solutions for integration of electrical circuitry with transducer wafers. The ultrasound transducer array is not able to be integrated with IC back end flow, which is a bottleneck for continuing scaling down the chip size and the modern ultrasound imaging instruments [70]. (3) The ultrasound transducer is not compatible with the standard CMOS fabrication process, due to most of the costly and toxic piezoelectric materials, which is hard and expensive to fabricate [69, 70].

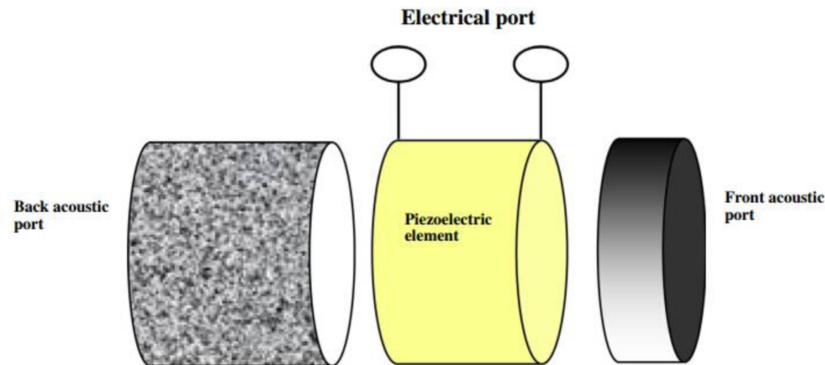


Figure 5. 3 Structure of bulk piezoelectric ultrasound transducer [68].

Piezoelectric Micro-machined Ultrasound Transducer (PMUT)

Micromachined ultrasound transducers (MUTs) are the counterparts of the bulk piezoelectric transducers in the imaging applictions. The MUT family includes capacitive micromachined ultrasonic transducers (CMUTs) based on the flexural vibrations caused by suspended membrane and the substrate attractions by electrostatic force, and piezoelectric micromachined ultrasonic transducers (PMUTs) based on material deformations caused by d31- or d33-mode excitation of a piezoelectric membrane.

Although PMUT shows good performance in medical imaging applications, it still meets big challenges including (1) PMUTs array is hard to operate over 30MHz without degrading other performances due to the uniformity and crosstalk between individual element, as a result, the axial resolution is only in the sub-10um range, not able to detect ultra-small tissues [69]; (2) The second challenge is the PMUT transducer array design. Compared with single element transducer, PMUT arrays have a wider image field of view. Single element ultrasonic transducer operation frequency is easier to achieve over 100MHz. However, for arrays, high-frequency (over 30MHz) is still a challenge.

Consequently, the future trend is to design arrays with higher operation frequency. In order to improve the operation frequency, some parameters and fabrication process need to consider. For transducer arrays without kerfs between each element, there is no physical separation between elements. The crosstalk between adjacent elements will significantly degrade performances due to high electromechanical coupling; the signal coupled between adjacent elements will increase the effective element width and the ring down time of the pulse. The method to solve this problem is mechanically isolate the individual elements, this is so-called the kerfed multi-element arrays [78-81]. Kerfed arrays provide a higher sensitivity at the focus compared to the kerfless structure, as lateral clamping reduces the amplitude of vibration of the elements in the case of the kerfless array. However, the operation frequency would be harmed by the kerfs, with the same material; the element pitch of the arrays will be in inverse proportion to the operating frequency, leading to difficulty to build arrays.

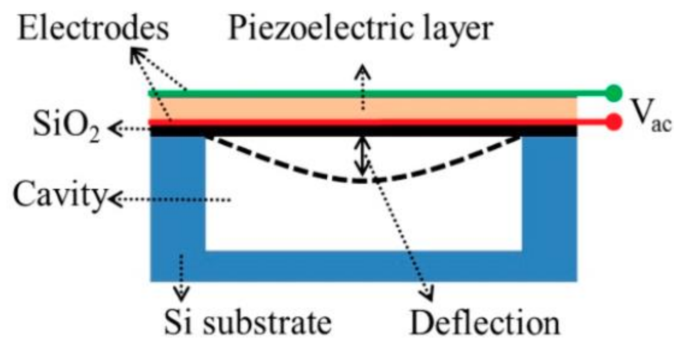


Figure 5. 4 Structure of a typical PMUT design where a piezoelectric membrane is onto a cavity [69].

In the inorganic piezoelectric material family, for quartz, a promising piezoelectric material is AlN, with the potential for high frequency applications (>50MHz-100MHz), and is non-toxic and stable under high temperature (up to 1000°C) [74-77]. Conventionally, ultrasound transducer is based on the bulk materials which is expensive to fabricate transducer arrays and hard to coupling with air and liquids. By thin film AlN technology, the transducer can be fabricated by integrated circuits manufacturing technology, providing solutions for electronics integration.

Recently, PMUT using AlN as the active piezoelectric layer has been reported [74-77] due to AlN is deposited by low temperature sputtering process, which is compatible with deposition onto CMOS wafers. 1 μ m thick AlN film was deposit onto 1um SiO_2 layer and 5x5 PMUT array have the membrane area of around 200 μ m for each element. The resonant frequency was measured as 220 kHz, which is not high enough for detections [74]. High frequency operation of AlN based PMUT has also been demonstrated [75, 80]. Thin transducer thickness (<10 μ m) and small element dimensions (<50 μ m) are required for high frequency applications. The resonant frequency reported over 50MHz [76]. 9x9 and 72x9 PMUT array have been fabricated on SOI wafers with 50 μ m PMUT diameter and 70 μ m pitch, the resonant frequency is 10.4MHz [77].

However, AlN has some drawbacks as the piezoelectric materials, the piezoelectricity of AlN can only be achieved with single crystals or with strong crystal orientation (001), and the piezoelectric coupling efficient is relatively low (0.2). As a result, some engineering techniques should be implemented to improve the overcome the weak of

AlN. For example, a curved AlN PMUT was designed to boost the electromechanical coupling and acoustic pressure, 2um thick AlN was deposit onto the substrate with size of 140 μ m, the measured center frequency is 2.19MHz [74]. 2.31MHz AlN PMUT has been fabricated with piston shape, in order to improve the sensitivity of PMUT [82].

Capacitive Micro-machined Ultrasonic Transducers (CMUT)

Using capacitive ultrasound transducers is another way in ultrasound imaging [83-85]. A metalized membrane is suspended over a cavity with heavily doped Si as back gate to form a capacitor structure. When a voltage is applied across the capacitor, the metalized suspended membrane is attracted toward the cavity by the electrostatic force, while an intrinsic force inside the membrane will drive the membrane back, accordingly, ultrasound can be generated by alternating electrical signals. Conversely, under a constant bias voltage, the membrane can detect the echo ultrasound and the capacitance change induces the electrical output change.

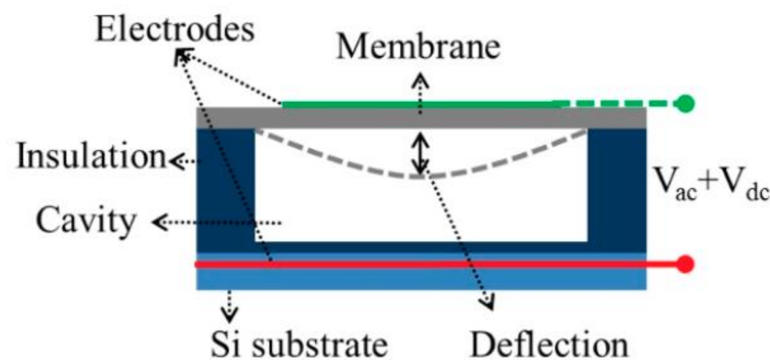


Figure 5. 5 Structure of a typical CMUT design [83].

CMUT was invented from 1990s [83] and have been extensively developed and researched in the following years, with comparable performances and advantages over PMUTs. CMUT is based on capacitive change induced by flexural vibration of electrostatically-actuated micro-machined plates such as Si, Poly-Si, Si_3N_4 etc. Compared to PMUT, CMUT has intrinsically low mechanical impedance, suitable for air-coupled applications, so as to have a better acoustic matching. In addition, CMUT has broadband behavior and wide temperature tolerance. Furthermore, CMUT can be fabricated with high volume production compared with PMUT, CMUT can be integrated with hundreds elements in small areas, to form a highly miniaturized system; CMUT can also have considerably improved product uniformity when compared with PMUT, it is easy and effective to make arrays of arbitrary size and pitch. CMUT can be fabricated by standard silicon IC fabrication process, providing a low cost way manufacture, a big potential to have high level of integration and scalability. CMUT has the compatibility between micro-electromechanical systems and standard integrated circuits technologies, able to integrated with IC by monolithic integration and chip-to-chip bonding process [86-88]; it has the ability to integrate closely with essential drive electronics.

CMUTs have now extensively developed with competing and advantageous performances to PMUTs [83-85]. CMUT can be fabricated by standard silicon IC fabrication process, providing a low cost way manufacture, a big potential to have high level of integration and scalability. Another promising feature of CMUT is wide bandwidth, so that has a high resolution for ultrasound imaging [83]. However, CMUT

arrays can only operate with low frequency under 30MHz, hard to be utilized for small feature detections [85].

5.1.3 Motivation

In the state-of-the-art researches, for the piezoelectric materials, it is expensive to fabricate the high quality materials, and the dominant materials used in the current states are toxic, which is essentially might not be good for fetus and pregnancy detections, besides, the fabrication process of the dominant piezoelectric materials is not compatible with IC, providing a bottleneck for the IC integrations. For the transducer arrays, although high frequency operations have been demonstrated by some groups, it is still a big challenge to design ultrahigh frequency applications (>30MHz) with fine resolutions able to detect small and superficial tissues. Another problem is the IC integration, although PMUT based ultrasonic transducer systems are widely researched and developed in the industries, however, PMUTs has not been able to integrate with the electronic circuits, unable to have small chips for portable and wearable systems.

The needs in the market drive the ultrasound imaging system to be able to IC integration, environmentally friendly, miniaturization, make the ultrasound machine to become portable and wearable. Through the CMOS compatible process, the PMUT system can be integrated onto the same chip of electronic circuits on a flexible substrate. Here we propose use AlN as the piezoelectric materials, which are able to be fabricated by standard silicon process; AlN film can be deflected over a cavity, which is designed to improve the electromechanical coupling and the sensitivity of the transducers, considering the relatively

low piezoelectric coupling efficiency. Then the PMUT wafer is integrated with ultrathin CMOS wafer to form a SoC system.

For PMUT, we propose a SoC design for high frequency piezoelectric transducers. Here we use AlN as the piezoelectric materials, although with relatively low electrical mechanical coupling coefficient, we adopt the substrate back etching method to the AlN arrays to compromise the low piezoelectric coupling efficient. One important advantage for AlN is the ability to be compatible with standard CMOS processes. Moreover, we use the chip to chip bonding method to integrate the PMUTs with IC chips by metal connects without thorough wafer via, the cost is large reduced without sacrificing the nice performance of PMUT. Moreover, the PMUT SoC can be fabricated onto a flexible and bendable Si substrate, which is highly promising for future wearable clinic devices with ultra-small chips and new user platforms.

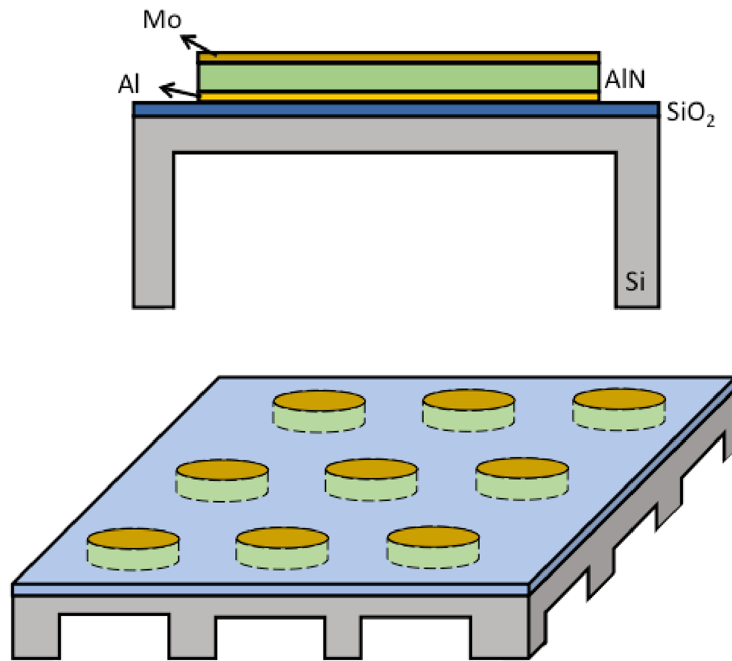


Figure 5. 6 Proposed AlN PMUT with single element and array design.

Dimensions:

Mo: Top electrode thickness t_{MO}: 120nm

Al: Bottom electrode thickness t_{Al}:120nm

AlN: Piezoelectic thickness t_{AlN}: 500-1000nm (800nm is a good choice), diameter d_{AlN}: 5μm-10μm

SiO_2: thickness d_{SiO2}: 100nm

Si Supporting bridge thickness d_{Si}: 2μm

Figure 5.6 shows the AlN PMUT we proposed for the ultrasound transducer. The fabrication process of an AlN PMUT array can be described as follows. First, 100nm SiO_2 was grown onto the 2-inch wafer (thickness ~279µm) by plasma-enhanced chemical vapor deposition (PECVD). Second, use standard photolithography to define the PMUT arrays and use sputtering to deposit 120nm Al as bottom electrodes. Third, deposit a thin layer of 500-1000nm (design splits) AlN onto the substrate by sputtering, it is believed that the piezoelectric properties of AlN is very related to the film quality, which can be controlled in the sputtering process, such as the crystal orientation, deposition pressure, speed and temperature. Fourth, use sputtering to deposit 120nm Mo as the top electrode. After the three sputtering process, the photoresist should be lift-off by acetone. Fifth, standard photolithography techniques were used to create pillars and cavities on the backside of the wafer. The wafers were then etched with the anisotropic silicon etchant ethylenediamine pyrocatechol (EDP) at 110 ◦C for 5.5 h to form Si/SiO_2 bridges. The thickness of the Si bridges is around 2µm. Figure 5.7 depicts the proposed MEMS wafer with PMUT array integrated with CMOS wafer by the wafer bonding.

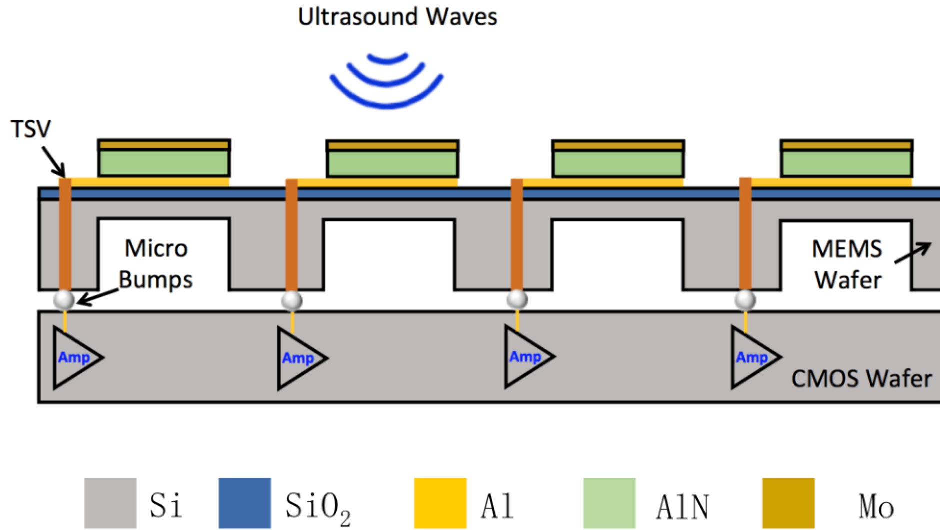


Figure 5. 7 Proposed SoC for PMUT MEMS wafer integrated with CMOS wafer.

From the state-of -the-art researches of CMUT, although CMUT is able to fabricated with standard CMOS process and integrated with IC, current states of center frequency of CMUT arrays are hard to achieve high operation frequencies over 30MHz, which is essential for high resolution and superficial tissue detections. Here we propose to use novel 2D materials as suspended membrane, which has large potential for ultra-high frequency resonation and applications, promising for future ultrasound sensors for imaging, which is not able to have ultrahigh resolution, but inserted into human body to detect inner body organs with non-toxic and human compatible materials.

Graphene micro-resonators were reported recently [41-43]. With a sheet mass density of ~7x10^{-19} g/m^2, a breaking strength of 43 N/m for defect free graphene [55], and a near zero bending stiffness, mechanical response in the sub-nano-second (nS) range can be achieved for properly engineered graphene strips of micrometers (µm) dimension. Graphene micro-machined capacitors can be readily achieved using Standard Si fabrication

techniques. The sub-nS response provides real-time imaging useful to monitor blood flows and tumors in the bodies. Furthermore, graphene does not have the “fatigue” behavior of typical bulk materials, thus is immune to the reliability concerns stemming from metal fatigue in conventional MEMS devices. In addition, the resonant frequency of graphene resonator has demonstrated to reach over 70MHz [41], beneficial for eye and skin imaging with high resolution. Furthermore, through the CVD growth of graphene, large area graphene CMUT arrays are able to be fabricated. In addition, graphene is flexible and transparent, so that it could be integrated as future flexible displays, touch screens and wearable devices. We propose to add the electrical readout and integrate the graphene CMUT arrays with circuits on a flexible substrate. In addition, it is of fundamental scientific interest to examine the ultrasound response by the graphene CMUT. We will investigate the electrical and mechanical properties of graphene membrane under ultrasound pressures both experimentally and through modeling.

For CMUT, we propose a graphene capacitive ultrasonic transducer device with circuit readouts, utilizing graphene as the suspended membrane of the capacitor structure. Graphene, with its extremely high strength (young’s modulus), stiffness, thermal conductivity and low mass density [7, 8], is ideal for suspended membrane for ultrasound applications. The resonant frequency of graphene membrane is reported over 70MHz [41], which is super promising for high frequency and high resolution medical imaging. In addition, the thin layer results in the smallest mass per unit area of any membrane achievable and thus the fastest response time of the ultrasonic sensor, providing a real-time signal processing of ultrasound images. Besides, we will use CVD method to growth

graphene by large scale instead of micro-exfoliation methods and develop graphene CMUT in CMOS fabrication process, providing a way to design graphene CMUT arrays with SoC. The proposed novel graphene CMUT concept, if successful, offers a great solution to the most challenging ultrasonic transducer design problem today.

5.2 Graphene CMUT

Beyond piezoelectric material based transducers, using capacitive ultrasound transducers is another way in ultrasound imaging. A metalized membrane is suspended over a cavity with heavily doped Si as back gate to form a capacitor structure. When a voltage is applied across the capacitor, the metalized suspended membrane is attracted toward the cavity by the electrostatic force, while an intrinsic force inside the membrane will drive the membrane back, accordingly, ultrasound can be generated by alternating electrical signals. Conversely, under a constant bias voltage, the membrane can detect the echo ultrasound and the capacitance change induces the electrical output change.

CMUTs have now extensively developed with competing and advantageous performances to PMUTs. CMUT can be fabricated by standard silicon IC fabrication process, providing a low cost way manufacture, a big potential to have high level of integration and scalability. Another promising feature of CMUT is wide bandwidth, so that has a high resolution for ultrasound imaging. However, CMUT arrays can is hard to operate with ultra-high frequency over 30MHz, hard to be utilized for small feature detections.

By Moore's Law, ultrasound imaging and ultrasonic transducer technology is driven to be faster, smaller and easier to use. Besides faster signal processing and larger data storing memory is needed for signal processing parts, a new transducer system is

envisioned, which features higher operation frequency, better resolution, on-chip integration and real-time signal transmission. For CMUT, it has great potential to be fabricated by standard IC process, but the operation frequency is still not high enough to achieve better resolution for high frequency range detections like the ophthalmology, dermatology and intravascular imaging.

Graphene CMUT has been reported recently [86-88], however, with no electrical readouts (use silver conductive paint to connect with the measurement setup instead of metal pads). In addition, there is no direct evidence of graphene response of ultrasound signals. Hence, it is hard to integrate the graphene CMUT device into IC for practical applications. Here, we reported the first graphene CMUT with electrical readouts and demonstrated its capability for integration into IC back-end for future biomedical imaging applications.

5.2.1 Structure & Operation Mechanism

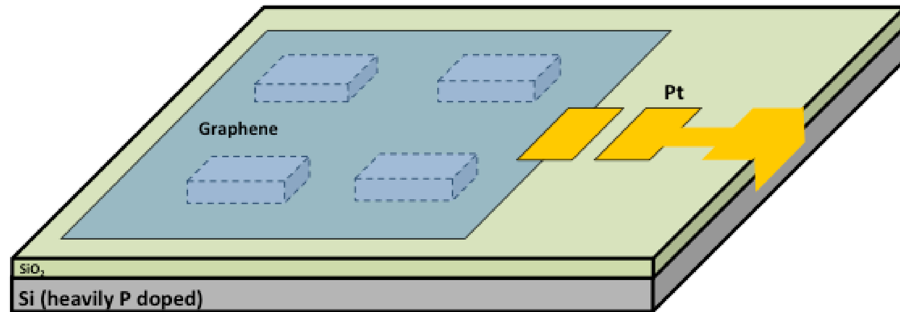


Figure 5. 8 3D scenario of the new graphene CMUT structure. Cavity arrays are covered by a large graphene membrane. One Pt pad is connected to graphene sheet as the top electrode and the other pad is contacted with the bottom.

For CMUT, we propose a graphene capacitive ultrasonic transducer device with electrical readouts, utilizing graphene as the suspended membrane over a large cavity arrays and two metal pads as the top and bottom electrode. Figure 5.8 illustrates the novel graphene CMUT structure and mechanism with electrical readouts. The graphene CMUT consists of one layer of graphene on top of the dielectrics and heavily doped Si substrate, the graphene layer covers the cavity arrays connected by metal electrodes. The capacitive structure includes the carefully fabricated graphene, the gap between the graphene and bottom heavily doped Si (heavily P doped Si as bottom electrode).

For the graphene based ultrasound transducer, the top electrode is connected with ground (GND), while the bottom terminal is connected to I/O on the chip. In the transducer transmission mode (T/R switch in the transmission mode), pulse generator sends out series

AC pulses, AC signal can drive the graphene sheet downwards by electrostatic force between graphene and bottom electrode, while the intrinsic mechanical stress and strain would drive the graphene backwards. Continuously, the mechanical vibration of graphene can trigger the particle movement in the air or other mediums, generating ultrasound if the movement is very fast. Inversely, in the receiving mode (T/R switch in receiving mode), the ultrasound (particle movement) can push and pull the graphene sheet, which inducing the capacitance change of the graphene CMUT, the electric circuits can readout this capacitance variance and send the signal to amplifiers and electrical units on chip.

5.2.2 Properties

This graphene CMUT has unique features, including: First, two dimensional graphene instead of bulk materials is used as the deflection membrane in the CMUT design with stand-out mechanical properties (0.5TPa Young's modulus [10]), it improves the reliability for the transducers, without introducing too many defects and dislocations in the membrane deflection as opposed to bulk materials. Second, graphene has excellent thermal dissipation capability (κ~4840-5300 W/m-K, ~35x higher than Si [16]) and thermal stability, which is able to spread out the heat very fast, avoiding thermal failure in the operation and generated from other IC components. Third, the low mass density of graphene makes the graphene can vibrate superfast in the chamber, inducing ultrahigh resonant frequency (able to achieve>80MHz [41], for conventional CMUT, resonant frequency over 30MHz is still a challenge), which is a great benefit for ultrahigh resolution detections in ultrasound medical imaging. Fourth, by carefully designing the device structure parameters especially for graphene dimensions and chamber gap distance,

graphene movements can induce higher capacitance variance if the chamber gap can be narrowed down further, which supply higher sensitivity in the CMUT design. Fifth, graphene can be engineered into nanometer dimensions, the graphene nanoribbon capacitor would have much smaller in size, and hence can greatly reduce the parasitic effect, which is a big problem for high performance CMUT today. Sixth, graphene can be readily designed into array structures, with the improvement fabrication process for large area and continuously CVD growth methods and much developed lithography techniques, the limited chip area can integrate hundreds of graphene CMUT elements in sub-10um size, the improved uniformity and integrated graphene CMUT is advantageous for future transducer design. Seventh, the graphene CMUT fabrication process is simple and compatible to standard CMOS process, and ready to IC integrations, making the core IC design and layout more simple and easier. Eighth, in the operation, for conventional CMUT, the suspended membranes are charged by the driven voltage, electrostatic charge might damage human tissues, in this configuration, the bottom electrode is connected with the supply voltage, while the graphene membrane is connected with ground, somehow provide a safer testament in the ultrasound imaging detections. In addition, large area and continuous CVD grown graphene is pre-transferred onto the substrate to make sure the possibility for large array design of graphene CMUTs used for medical imaging applications. In addition, the thin layer results in the smallest mass per unit area of any membrane achievable and thus the fastest response time of the ultrasonic sensor, providing a real-time signal processing of ultrasound images. Besides, we used CVD method to growth graphene by large scale instead of micro-exfoliation methods and developed

graphene CMUT in CMOS fabrication process, providing a way to design graphene CMUT arrays with SoC. The proposed novel graphene CMUT concept offers a great solution to the most challenging ultrasonic transducer design problem today.

5.2.3 Fabrication

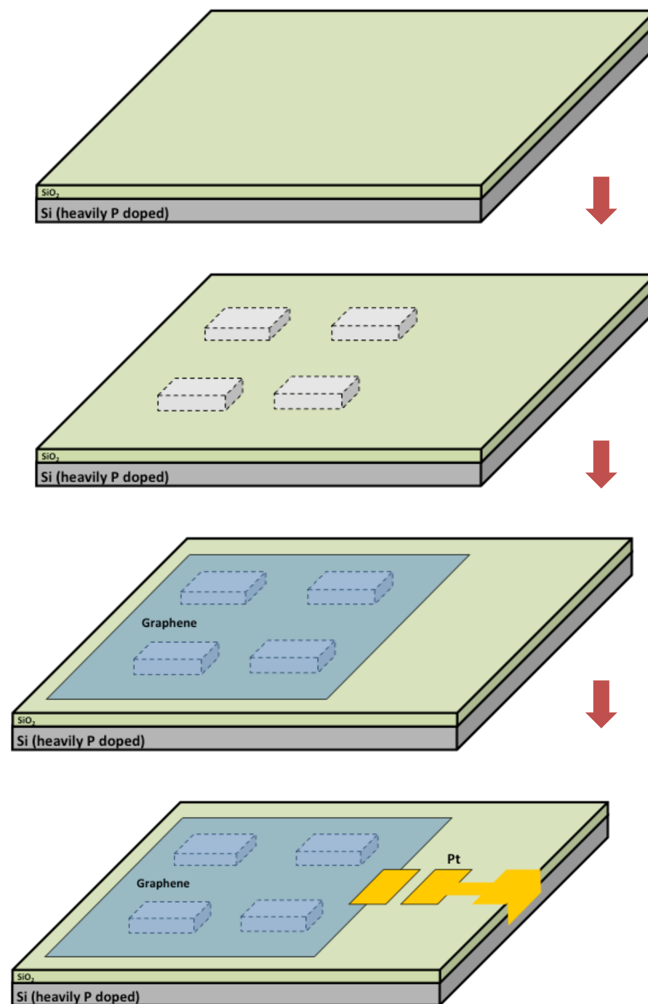


Figure 5. 9 Fabrication process of the new graphene CMUT device.

A fully CMOS-compatible device fabrication process flow is critical to achieving 3D heterogeneous integration of the proposed graphene CMUT with ICs, hence realize the novel concept. Figure 5.9 illustrates the device fabrication process flow developed in this work. First, a SiO_2 layer of 1um is grown on a Si (heavily doped p-type) substrate by plasma enhanced chemical vapor deposition (PECVD). The SiO_2 was then patterned by reactive ion etching (RIE) to define the cavity arrays. Next, single layer graphene film was produced by CVD method, suitable for making large area graphene film, followed by Raman evaluation (Figure 5.10d). The graphene film was then transferred onto the trenched substrate and dried for overnight in order for the suspension over the cavities (Thousands of pillars to make sure graphene suspension). Next, top and bottom pads are deposit by focused ion beam (FIB). This FIB dry deposition and etching process is adopted to avoid liquid environment of graphene membrane and reduce the fabrication process of patterning and e-beam evaporation, which may introduce many defects and cracks into graphene. Specifically, a milling current of 30kV/1nA is adopted to deposit the top (cover the graphene membrane) and bottom electrodes (100nm thickness, Platinum, 100μmx100μm) with center-to-center distance of 150μm. Then, FIB etch mode (30kV/50pA) is used to etch a small trench from the SiO_2 surface to the bottom heavily doped silicon and a connection metal line (1um thickness) is finally deposit to connect the second pad to the bottom. Figure 5.10 shows SEM image of a graphene CMUT and the bottom pad connection.

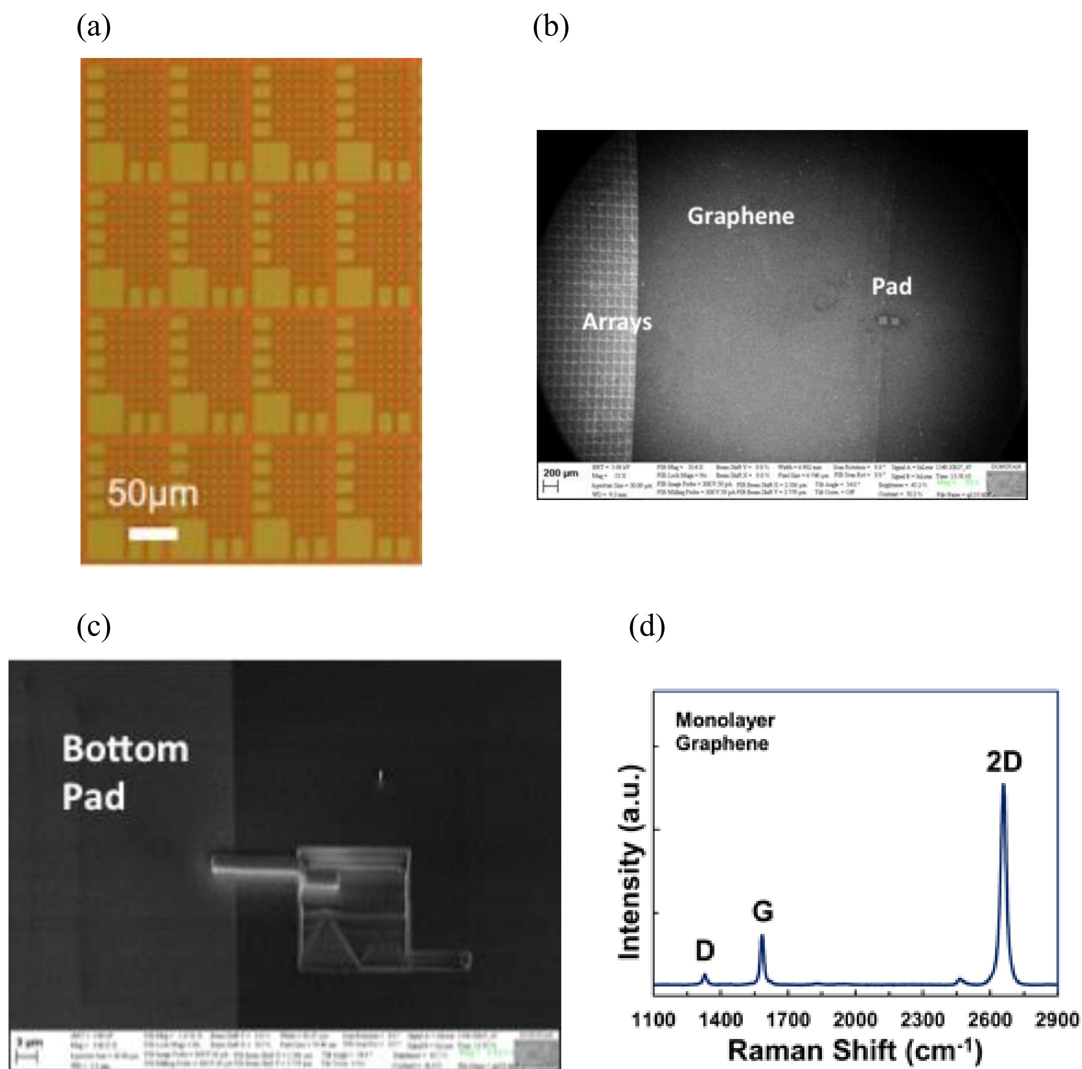


Figure 5. 10 (a) The cavity pattern of one of the repeating cells (4x4 cells). (b) & (c) SEM images of the graphene CMUT arrays and the top and bottom pads devise. (d) Raman Spectroscopy image of the monolayer graphene membrane. The ratio of the 2D and G peak intensities denotes the number of layers of graphene sheet.

5.3 Characterization & Discussions

5.3.1 C-V Measurement

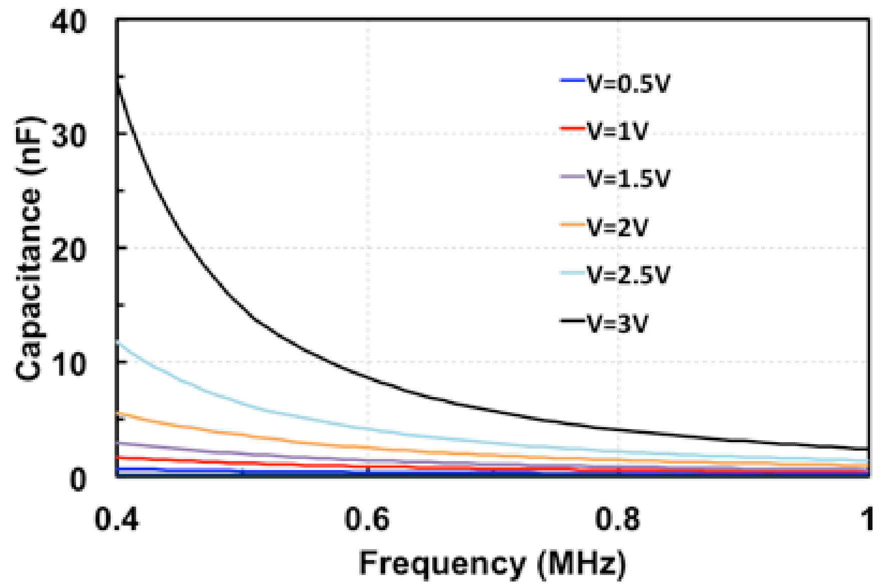


Figure 5. 11 Capactiance~frequency and voltage measurement of graphene CMUT device by LCR meter.

The capacitance of the graphene CMUT is a first measure of its electrical properties. It provides the capacitance of the transducer, which is crucial to the electrical signal readouts of the graphene CMUT when impinged by the ultrasounds. The reason we devise the array structure is that, for an individual graphene capacitor device (graphene L=10μm, W=10μm and trench depth d=550nm) we fabricated in [48-52], the graphene intrinsic capacitance is estimated to be ~1.61fF, while the parasitic from the pads is ~ 2.7pF, which is around 1000 times larger than the graphene capacitance, as a result, it is extremely

hard to detect the small capacitance variance of graphene response itself. However, the array design can overcome this parasitic problem of the graphene switch.

Figure 5.10 (a) shows the cavity patterns of one of the repeating cells. In each of the cell, there are several square pillars with depth of ~1μm and various dimensions, which are used to suspend the graphene membrane. For each graphene CMUT device, there are 133x200 repeating cells, consequently, the graphene intrinsic capacitance is estimated as ~2.3nF and the parasitic capacitance (graphene-SiO_2-bottom electrode) is ~4.8nF and the pad capacitance can be neglected due to the large graphene arrays. So, the graphene response is large enough to be detected by the measurement equipment due to it is comparable to the parasitic capacitance.

Figure 5.11 shows the capacitance-frequency measurement with various bias voltages of graphene CMUT by LCR meter. First, it is observed that as frequency sweeps from 400Hz to 1MHz, the graphene CMUT capacitance decreases from nF to pF, which is due to the electrons in the graphene membrane cannot catch up with the input AC signals of the LCR meter. Second, as the bias voltage increases from 0.5V to 3V, capacitance of the graphene CMUT increases evidently shows graphene membrane deflects downside due to the electrostatic force between graphene ribbon and bottom electrode. The inception of the graphene capacitor and C-V measurement enhances the capability of graphene CMUT as the ultrasound transducer for ultra-high frequency application, considering the voltage controlled capacitance variations, fast response time and robust and reliable graphene NEMS.

5.3.2 S-Parameter Measurement

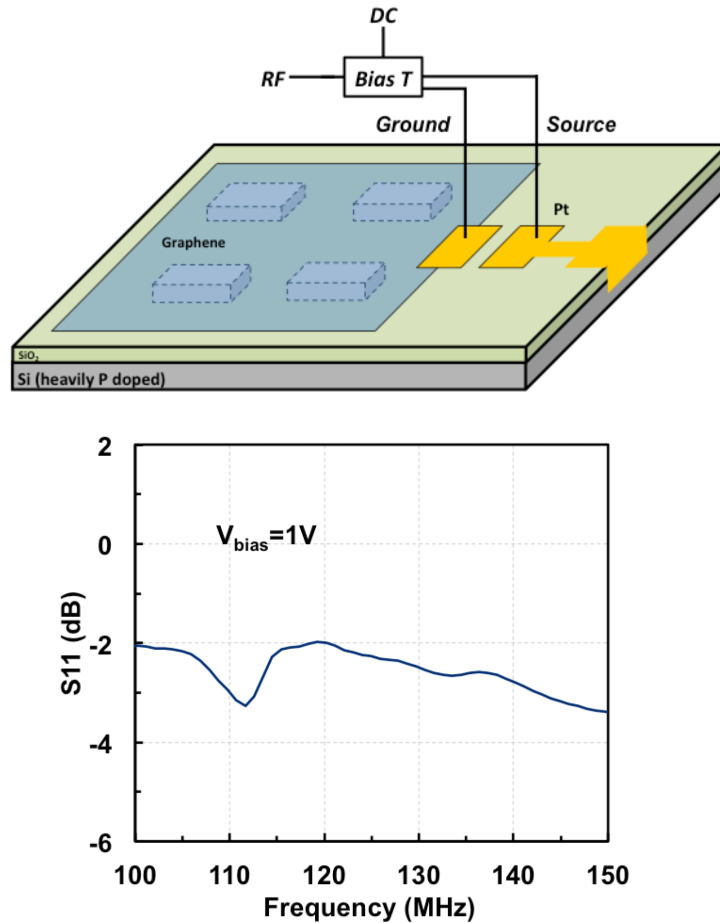


Figure 5. 12 (a) Measurement setup of the graphene CMUT for the network analyzer. (b) S11 parameter for the graphene CMUT device with frequency of 100-150MHz shows a peak value at 110MHz with a bias voltage of 1V.

The circuit used to drive and detect the mechanical oscillation of the graphene is shown in Figure 5.12 (a). A RF drive with generated by a network analyzer Agilent E8363B, and a DC voltage bias are combined using a bias tee and applied to the bottom electrode. Figure 5b shows the measured S11 of a monolayer graphene CMUT device as a function

of drive frequency, measured at room temperature. The mechanical resonance appears as a peak of 1.2 dB in amplitude at the frequency of ~110MHz. S11 parameter indicates how much power is reflected back to the source. At the resonant frequency, maximum power is transferred to the CMUT due to the resonance of CMUT mechanical frequency and sent-in RF frequency (RF Force), which determines the system resonant frequency. In addition, when the graphene CMUT resonates, the graphene membrane deflects at the maximum position, making the impedance lowest, so that most of the energy can transfer into the next stage of network, as a result, S11 shows the minimum value at the resonant frequency.

5.3.3 Z-Parameter

The electrical input impedance of a transducer is a measure of its electrical and mechanical properties. It provides the resonant frequency of the transducer in air as well as its capacitance. These two data are the first checkpoints between the measurements and predictions. The electrical input impedance can be deducted by the S11 parameter measured by the network analyzer. The real and imaginary parts of the electrical input impedance of an array element are shown in Figure 5.13. The resonant frequency of the array element was measured as ~114MHz in air from the real part of the impedance.

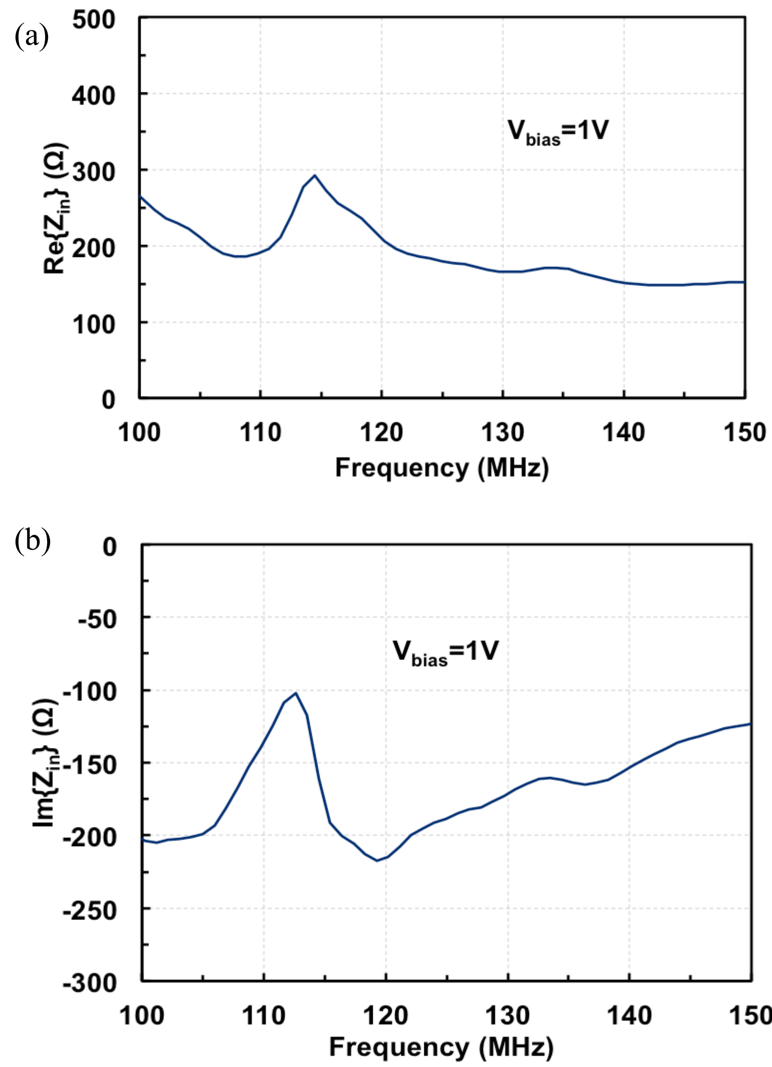


Figure 5. 13 (a) Real part of the input impedance of the graphene CMUT with a bias voltage of 1V. (b) Imaginary part of the input impedance for this graphene CMUT device.

5.4 Modeling & Simulation

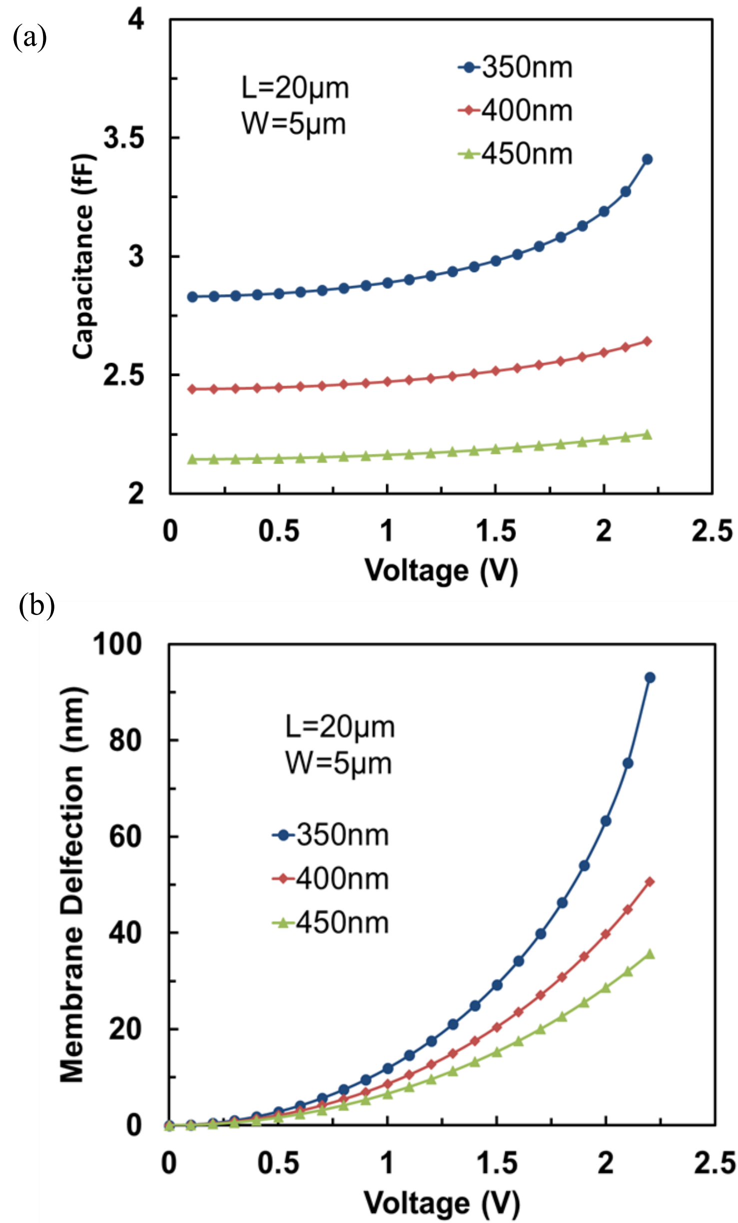


Figure 5. 14 Simulated (a) gNEMS switch capacitance and (b) graphene membrane deflections over a cavity cell of the graphene CMUT with bias voltage sweeping from 0V to 2.5V.

We also conducted COMSOL modeling studies to investigate the electromechanical behaviors of graphene CMUTs cell. Figure 4 describes the maximum membrane deflection and capacitance as the relationships of the trench depth (350/400/450nm) of one graphene CMUT cell (L=20μm, W=5μm), it shows that, as bias voltage increases, the graphene membrane is more deflected towards the bottom by the electrostatic force, establishing the knowledge for improving the electro-mechanical coupling for graphene CMUT performances by adjusting multiple parameters in structures.

The resonant frequency of graphene CMUT has also been modeled by the equation in [41].

$$f = \left\{ \left(A\sqrt{\frac{E}{\rho}} \times \frac{t}{L^2}\right)^2 + \frac{0.57 \times A^2 T}{\rho L^2 W t} \right\}^{1/2} \tag{5.1}$$

Here, f is the resonant frequency of graphene beam with lateral tension T; A is the clamping coefficient and A=1.03 for double clamped beams; E is Young's modulus and E=1TPa for graphene; ρ is the mass density of graphene; 2200kg/m^3; t, L and W is the suspended graphene thickness, sheet length and sheet width; T is the tension between graphene and the SiO_2 surface. Tension is likely results from the fabrication process, where the friction between the graphite and the oxide surface during graphene membrane transfer process stretches the graphene sheets across the trench. Here in this model, the tension between graphene and oxide (T, fitting number) is set to be as 10μN, much larger than the 13nN in [41], because in the literature, it is only a single graphene MEMS resonator, here we actually has a array with thousands of pillars, so the tension should be much larger.

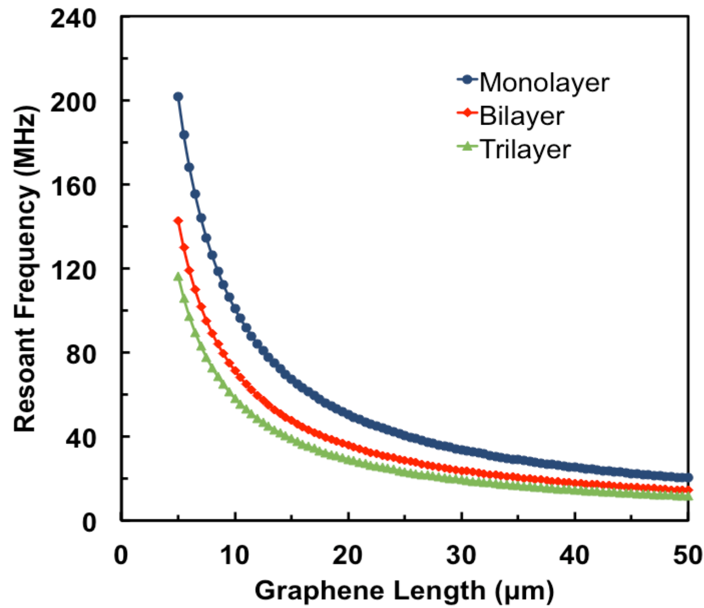


Figure 5. 15 Graphene CMUT resonant frequency as relationship with grpahene length and graphene layers.

Figure 5.15 shows the graphene CMUT resonant frequency as relationship with grpahene length and graphene layers. From the figure, as graphene length increases from 5µm to 50µm, (graphene width is set as 9µm), the resonant frequency reduced. In addition, as graphene membrane thickness increases from 0.3nm (single layer graphene), 0.6nm (bilayer graphene) to 0.9nm (Tripple layer graphene), the resonant frequency decreases. Also, with single layer graphene (0.3nm) with dimension of W=9µm, L=9µm, the resonant frequency is ~110MHz, similar with our measurement value (114MHz).

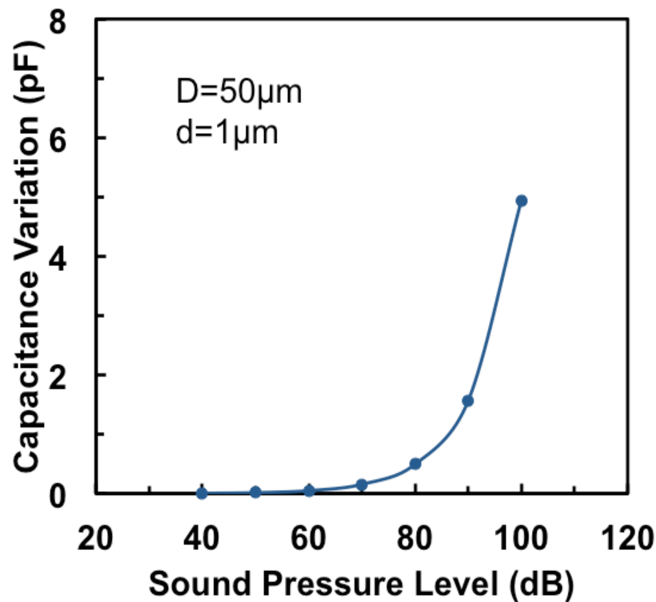


Figure 5. 16 Estimated capacitance variance of the graphene chamber with the relationship of the sound pressure level of the ultrasound.

The transmit/receive behavior of a graphene CMUT can be characterized in the ultrasound measurement. Usually, the transducer is biased at a certain DC voltage. A ultrasound speaker is placed near the graphene CMUT. The acoustic wave that bounces back from the reflector will cause a capacitance change across the CMUT. The ultrasound speaker has certain sound pressure level (can convert into ultrasound power). The pressure at the surface of the graphene CMUT can be inferred from this pressure level.

In order to estimate the capacitance change of the graphene CMUT with the ultrasound response, the sensitivity is used to describe the graphene response to the ultrasound. Figure 5.16 shows the estimated capacitance variance of the graphene individual chamber with the relationship of the sound pressure level. For a graphene cell

of 50μm diameter and trench depth of 1μm, the sensitivity is ~2.47pF/Pa [71, 72], which corresponds to a 5pF capacitance variation with the 100dB SPL of the ultrasound.

5.5 Conclusion

In this section, we presented the design and fabrication of the graphene CMUT arrays and showed the experimental characterization results. The results demonstrate that graphene CMUT array indeed has a resonant frequency of 110MHz. We also provide the complete fabrication process of the graphene CMUT arrays, which is able to integrate with the IC back-end. This graphene CMUT with ultra-high resonant frequency is promising for future ultrasound sensor applications for medical imaging.

Chapter 6 Conclusion

In conclusion, we provided a revolutionary solution to the next generation ESD protection circuits solutions, as for using graphene material for both interconnects and novel ESD protection structures.

For graphene ESD interconnects, in summary, this comprehensive and systematic characterization work reveals important insights that are critical to future design and optimization of graphene interconnects. Considering that the measured resistance of graphene wires is higher than the metal interconnects, it is expected that the resistance of the graphene wires can be much reduced by improving synthesis methods and adopting new interconnect structures to enable practical applications. Although it is still a challenge to ensure the low resistance of graphene interconnects for whole-chip ESD protection circuits, with great properties of graphene including high thermal conductivity and high current handling capability, it is possible to be one of the promising candidates of interconnects for on-chip ESD protections.

For graphene NEMS ESD switch, we report comprehensive characterization and statistical analysis of gNEMS switch structures by transient TLP zapping for ESD discharging. The systematic TLP testing was conducted to understand the details of ESD discharging behaviors related to the device dimensions and TLP pulsing conditions. The statistics reveal the mechanism and performance of the new gNEMS ESD switch structures fabricated using a CMOS-compatible process. It is believed that the novel above-IC gNEMS ESD switch, fabricated in the BEOL deck of IC dies through 3D heterogeneous integration, will resolve the disadvantages inherent to traditional in-Si PN-based ESD

protection structures, making it a potential on-chip ESD protection solution for next-generation ICs at nano nodes.

In addition, we also reported a new graphene based capacitive ultrasound micomachined transducer (CMUT) for ultrasound imaging applications. We proposed to use graphene as the vibration membrane in order to improve the resonant frequency of the transducer to offer a better resolution to the ultrasound imaging. Promisingly, the graphene CMUT is compatible to the CMOS fabrication flow and can be integrated with the IC components, the graphene material is non-toxic and human compatible, which is promising for future ultrasound transducer design not only can provide ultra-high resolution but also implantable into the human body and supply deep tissue imaging.

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