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Authors

Wang, Ya
Li, Peng
Lai, Suming

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Robust and Efficient Transistor-Level Envelope-Following Analysis of PWM/PFM/PSM DC-DC Converters

Ya Wang, Peng Li, *Fellow, IEEE,* and Suming Lai

Abstract—The envelope-following (EF) simulation of practical dc-dc converters is challenging due to the presence of digital behavior, strong nonlinearity, complex frequency module schemes, and feedback loops. This paper presents a novel EF method for time-domain analysis of dc-dc converters-based upon a numerically robust time-delayed phase condition to track the envelopes of circuit states under a varying switching frequency. We further develop an EF technique that is applicable to both fixed and varying switching frequency operations, thereby providing a unifying solution to converters with pulse width modulation, pulse frequency modulation, and pulse skipping modulation. By adopting three fast simulation techniques, our proposed EF method achieves higher speedup without composing the accuracy of the results. The robustness and efficiency of the proposed method are demonstrated using several dc-dc converter and oscillator circuits modeled using the industrial standard BSIM4 transistor models. A significant runtime speedup of up to 30*X* with respect to the conventional transient analysis is achieved for several dc-dc converters with strong nonlinear switching characteristics.

Index Terms—DC-DC converter, envelope-following simulation, fixed frequency, varying frequency.

I. Introduction

HIGHLY efficient dc-dc converters are indispensable in today's low power microprocessors, embedded systems and portable devices [1]. However, the simulation of these circuits is generally very challenging due to the existence of complex dynamics, widely spread time scales (e.g., fast switchings with slowly varying amplitudes), and feedback control. These difficulties render the use of the standard transient analysis very inefficient, for instance, by forcing the stepsize to be very small.

The time-domain envelope-following (EF) method is well suited for the simulation of such circuits with a multirate

Y. Wang and P. Li are with the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: pli@tamu.edu).

S. Lai was with the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843 USA. He is now with Maxim Integrated, San Diego, CA 92121 USA.

characteristic [2]–[4]. The efficiency of EF stems from the fact that it efficiently traces the slowly varying envelope of the circuit by skipping many fast changing switching cycles in between. An EF method is introduced in [2] to simulate open-loop switching power converters with a fixed clock frequency and the general difficulty in simulating closed-loop switching converters is discussed. Silveira *et al.* [4] extended this method for closed-loop converters and the problem of quasialgebraic variables is addressed. Liu *et al.* [5] introduced a method that exploits the parallelism in the EF method and parallelize the Newton update solving part to boost the simulation performance. In [6] quadratic and exponential approximations of the envelope are used in EF simulation. However, only fixed-frequency pulse width modulation (PWM) converters are targeted. To analyze variable-frequency converters, Kato *et al.* [7] approximate variations of the switching period by assuming that the envelope stepsize is an integer multiple of the last switching period of each EF step, which is not true in general. Another EF method for closed-loop converters is proposed in [8] for a specific type of converters with multiple switching intervals with a fixed clock (switching) period. The key limitation of [7] and [8] is that the entire converter is treated simplistically as a linear switched network with each switching interval modeled using a linear state transition function. No runtime speedups over transient analysis have been reported in both papers.

Oscillators have also been targeted by EF methods. Maffezzoni [9], [10] used the insightful concept of Poincar*é* map to predetermine cycle time and estimate local truncation error (LTE) to predict the future envelope step. However, this method is specifically designed for simulating high-Q oscillators and assumes that cycle time does not change through one envelope step, which may limit the envelope stepsize and cause loss of efficiency simulating converter circuits. Mei and Roychowdhury [3] presents an elegant EF technique for oscillators where cycle time and envelope step are considered as two extra unknowns and two additional time-derivative-based phase conditions are introduced. However, when applied to dc-dc converter analysis, this technique may suffer from reduced robustness due to the presence of strongly nonlinear switching activities in the dc-dc converter and high numerical noise levels inherent in the evaluation of time-derivatives of the nodal voltages required for the adopted phase conditions.
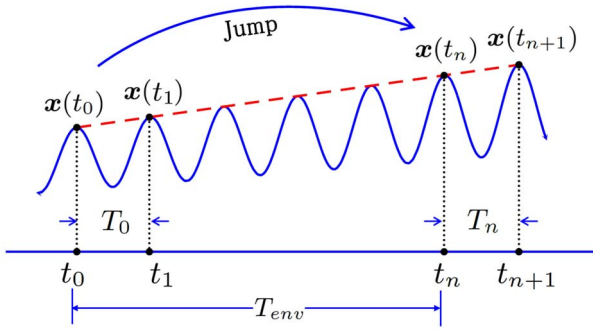
Fig. 1. Basic EF method. t_0, t_1, t_n, and t_{n+1} are four time points at equal phase and satisfy both $t_1 = t_0 + T_0$ and $t_{n+1} = t_n + T_n$.

In this paper, we develop a robust and efficient EF method to provide a unifying solution to the simulation of dc-dc converters with both transient and steady state behaviors under a constant or varying switching frequency. Of our particular interest are real-life dc-dc power converters that are operated with complex modulation controls, e.g., PWM, pulse frequency modulation (PFM), or pulse skipping modulation (PSM). Even with the standard transient analysis, these circuits are very challenging to simulate due to the coexistence of multirate nature, strong nonlinearities, hard switching activities, digital/memory and hysteretic effects, and strong feedback control. These characteristics significantly stress the robustness and efficiency requirements of the applied EF method and prevent us from using techniques that have been shown to be successful for oscillators such as [3].

At the core of our new EF algorithm is a novel time-delayed phase condition that provides robust tracking of the circuit envelope in the transient phase, under a varying switching frequency. We further develop a mechanism that can smoothly track the transitions between the transient and steady state phases, thereby providing a unifying solution to the EF simulation of both modes of operation. The implementation of three fast simulation techniques improves the efficiency of the algorithm without compromising the accuracy of the results. The proposed method can be transparently applied to PWM, PFM, and PSM converters under a constant or varying switching frequency. We demonstrate the excellent robustness, generality, and efficiency of the proposed technique using several dc-dc converters and oscillator circuits.

II. ENVELOPE FOLLOWING METHODS

We review the basic backward-Euler-based EF method for converters with a constant switching frequency (e.g., PWM converters). An electronic circuit can be described using a standard differential-algebraic equation

$$\dot{\boldsymbol{q}}(\boldsymbol{x}) + \boldsymbol{f}(\boldsymbol{x}) = \boldsymbol{u}(t) \qquad (1)$$

where $\boldsymbol{x} \in \mathbf{R}^N$ is a vector of state variables, $\boldsymbol{q}$ is a nonlinear charge function, $\boldsymbol{f}$ describes the resistive nonlinearities, and $\boldsymbol{u}(t)$ is the excitation to the circuit [11].

The output voltage of converters such as PWM converters demonstrates fast switching activities with a slowly varying amplitude as a result of load change, a characteristic that is well suited for EF analysis [12]. As shown in Fig. 1, denote the constant switching cycle of the circuit at t_0 by T_0 and switching cycle at t_n by T_n. The switching cycle is known as a constant, so we have $T_0 = T_n$. Denote the state variable at time t by $\boldsymbol{x}(t)$, accordingly the state at time t_0 by $\boldsymbol{x}(t_0)$ and that at t_n by $\boldsymbol{x}(t_n)$. Then define t_n as the time point that is n cycles after t_0, namely $t_n = t_0 + nT_n$, so that circuit at t_n has the same phase as at t_0. By the EF method, starting from a given $\boldsymbol{x}(t_n)$, we simulate the circuit for one cycle T_n to get another state vector of equal phase $\boldsymbol{x}(t_{n+1}) = \boldsymbol{x}(t_n + T_n)$. As shown in Fig. 1, if the amplitude of the circuit response changes slowly enough, a line can be drawn to pass through these three equal-phase points, implying that

$$\frac{\boldsymbol{x}(t_n) - \boldsymbol{x}(t_0)}{nT_n} = \frac{\boldsymbol{x}(t_{n+1}) - \boldsymbol{x}(t_n)}{T_n}. \qquad (2)$$

Note that $\boldsymbol{x}_{n+1}$ can be evaluated as $\boldsymbol{x}_{n+1} = \phi(\boldsymbol{x}_n, t_n, T_n)$, where ϕ is the state transition function of the circuit. Now (2) can be written as

$$\frac{\boldsymbol{x}(t_n) - \boldsymbol{x}(t_0)}{nT_n} = \frac{\phi(\boldsymbol{x}(t_n), t_n, T_n) - \boldsymbol{x}(t_n)}{T_n}. \qquad (3)$$

The only unknown in this equation is $\boldsymbol{x}_n$, which can be solved by any nonlinear solution method such as Newton–Raphson method.

Starting from a known initial state $\boldsymbol{x}(t_0)$, one may skip a large number of switching cycles which is $T_{\text{env}} = nT_n$ as in Fig. 1, to directly solve for the state $\boldsymbol{x}(t_n)$. To move one step forward, the same procedure is restarted by treating the solved $\boldsymbol{x}(t_n)$ as the new initial state $\boldsymbol{x}(t_0)$ and $\boldsymbol{x}(t_{n+1})$ as $\boldsymbol{x}(t_1)$, respectively. However, this basic EF method assumes that the switching cycle does not change, which prevents its application to circuits with dynamically changing switching frequencies like PFM dc-dc converters, which are the focuses of the next section.

III. TIME-DELAYED PHASING TRACKING FOR CIRCUITS WITH VARIABLE SWITCHING FREQUENCIES

For the types of circuits of interest here, the varying switching frequency is set by a specific modulation or tuning mechanism. As such, the switching period T_n is not known *a priori* and must be treated as an unknown variable. Another consequence of the varying frequency is that the skipped time interval between t_0 and t_n may not be an integer number of cycles, i.e., it is generally true that $T_{\text{env}} \neq nT_n$. To see the issues involved, we rewrite (2) slightly as

$$\frac{\boldsymbol{x}(t_n) - \boldsymbol{x}(t_0)}{T_{\text{env}}} = \frac{\boldsymbol{x}(t_{n+1}) - \boldsymbol{x}(t_n)}{T_n} \qquad (4)$$

where the three unknown variables are $\boldsymbol{x}(t_n)$, T_n, and T_{env}. Since there are $N+2$ unknowns and only N equations [N being the dimensionality of (4)], this system is under-determined. In fact, (4) alone does not guarantee $\boldsymbol{x}(t_0)$, $\boldsymbol{x}(t_n)$, and $\boldsymbol{x}(t_{n+1})$ being at the same phase. Varying switching frequencies introduce significant challenges to EF. We propose a novel and
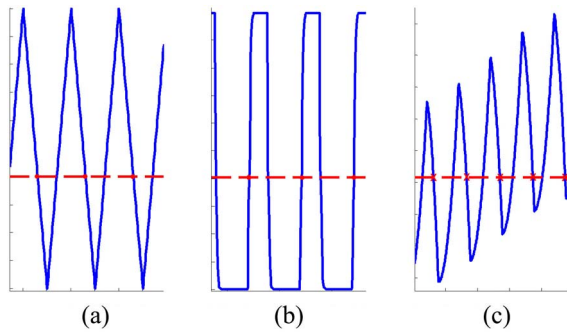
Fig. 2. Three typical voltage waveforms in a dc-dc converter. (a) External triangular signal. (b) Typical internal signal driving power switches. (c) Typical output response with both frequency and amplitude modulation. Specific level crossing times may be used to define equal phase conditions (red dashed lines).

Fig. 3. Slope function and equal-phase points.

numerically robust technique for tracking the phase of circuits operating under a changing switching frequency.

A. Challenges and Possible Solutions

Several existing EF methods address varying switching or oscillation frequencies. In the oscillator simulation technique of [9], T_n is predetermined during the integration process by using the notion of Poincaré map. With T_n computed, T_{env} is set to be an integer multiple of T_n. However, the underlying assumption that T_n remains unchanged within one envelope step is not true in general and can potentially prevent use of large envelope stepsizes for transient phases of the circuit. In addition, it is not always possible to determine T_n by Poincaré map as suggested in [13]. This situation could be worse for dc-dc converters with digital behaviors and hard switching activities. Mei and Roychowdhury [3] addressed this problem in oscillator simulation by adding two extra phase conditions at t_n and t_{n+1} by constraining the time derivatives of a nodal voltage at these two points. Though proved effective for oscillators, this technique may not be suitable for dc-dc converters due to the presence of digital characteristics and sharp signal transitions, which exacerbate the numerical noise inherent in the numerical evaluation of time derivatives.

Fig. 2 shows waveforms of three typical nodes in dc-dc converters. Fig. 2(a) shows the external triangular signal that is used in the PWM dc-dc converter of Fig. 12. Fig. 2(b) shows a typical internal voltage signal that drives the metal–oxide–semiconductor switches in both PWM and PFM dc-dc converters. Fig. 2(c) depicts a typical output waveform with a varying amplitude during the transient phase of a PWM/PFW dc-dc converter. Common properties of these representative signals are that: they all have discontinuous first derivatives; and there are long periods of time in which the first-order derivative of a signal is either very large or approximately constant. These characteristics present practical challenges for the aforementioned EF techniques developed for oscillators.

On the other hand, sharp signal changes in a converter indicate certain controlled-switching events that are taking place in the circuit. These switching activities reliably reflect the onset or ending of a specific mode of operation and can be in principle leveraged to robustly identify equal-phase points
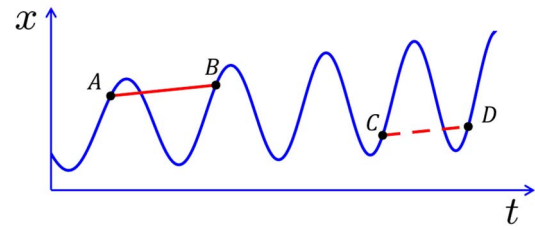
that shall be sampled by an EF method. Clearly, the main challenge here is to achieve such in a numerically robust manner. For example, we may purposely choose to monitor one or multiple internal signals with large sharp swings and use the moments at which such signals cross given critical threshold levels to determine the sampling time instants for EF, as shown in Fig. 2 by the dashed lines. For instance, the output of the set-rest (SR)-latch of the PFM converter used in the experimental section (Fig. 16) can be a good choice as its switching activities reveal the on or off states of the power switches. However, using fixed signal crossing levels is problematic for signals that experience amplitude modulation as in Fig. 2(c).

B. Robust Monitoring of Phase Change

Motivated by the above discussion, we introduce a new equal-phase condition that can capture both frequency and amplitude variations in a converter. To do that, we begin with a definition of slope function $\text{slp}(\cdot, \cdot)$. Slope function is defined by two points over a given period. As shown by points A and B in Fig. 3, the slope function of A and B is

$$\text{slp}(A, B) = \frac{x(B) - x(A)}{t(B) - t(A)} \tag{5}$$

where $x(A)$ and $x(B)$ are the amplitudes of points A and B, $t(A)$ and $t(B)$ the time instants of A and B. The slope function is useful in defining equal-phase condition because the slope function of two equal-phase points can be used to find other equal-phase points in the vicinity. For example in Fig. 3, assume that A and B are already known as equal-phase points, i.e., they mark the beginning and ending of one switching cycle. In this case, $\text{slp}(A, B)$ is in fact the cycle-slope of the signal during the corresponding switching period. Then, points C and D are also equal-phase points if and only if $\text{slp}(A, B) - \text{slp}(C, D) = 0$ is satisfied. Note that this new phase condition is a more general case of the scheme that is based on crossing times of fixed signal threshold levels discussed at the end of Section III-A.

When computing slope function to find points with equal phase, we monitor one or multiple internal circuit nodes (branches), or phase monitoring nodes (or branches). To robustly specify equal-phase points, we assume that phase monitoring nodes are provided by the designer and exposed to the simulation algorithm. In general, these nodes can be chosen rather easily by leveraging a very minimum amount of design knowledge. For instance, for PFM controlled dc-dc converters, a natural choice is the regulated output node that drive internal comparators to alter the switching behavior. Using the idea of
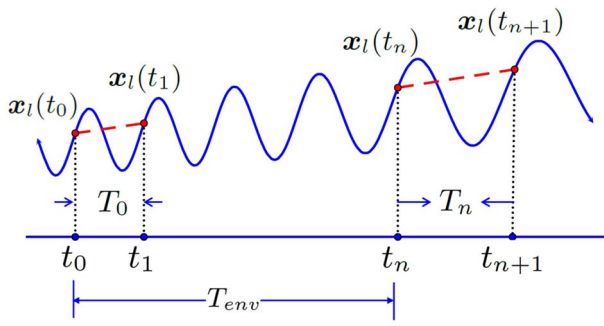
Fig. 4. Equal-phase points defined by equal slope function value are shown in the dashed lines.

Fig. 5. Time delayed phase tracking method.

slope function, we now formally define the proposed equal-phase condition. As shown in Fig. 4, denote the voltage of a phase monitoring node by x_l. Four nodes involving the envelope can then be denoted by $x_l(t_0)$, $x_l(t_1)$, $x_l(t_n)$, and $x_l(t_{n+1})$. Under the assumption that the variance of the envelope slope within one step is small, the equal-phase condition can be defined as

$$\frac{x_l(t_{n+1}) - x_l(t_n)}{T_n} - \frac{x_l(t_1) - x_l(t_0)}{T_0} = 0. \tag{6}$$

Note that results from previous envelope cycle $x_l(t_0)$ and $x_l(t_1)$ are already available and are at equal phase. When (6) is satisfied, the value of slope function of $x_l(t_n)$ and $x_l(t_{n+1})$ is equal to that of $x_l(t_0)$ and $x_l(t_1)$, meaning that $x_l(t_n)$ is at the equal phase as $x_l(t_{n+1})$.

Since the system needs two phase conditions, we simply apply (6) to another phase monitoring node, denoted by x_k. Now the new system of EF formulation is

$$\frac{x(t_n) - x(t_0)}{T_{env}} - \frac{x(t_{n+1}) - x(t_n)}{T_n} = 0$$
$$\frac{x_l(t_{n+1}) - x_l(t_n)}{T_n} - \frac{x_l(t_1) - x_l(t_0)}{T_0} = 0$$
$$\frac{x_k(t_{n+1}) - x_k(t_n)}{T_n} - \frac{x_k(t_1) - x_k(t_0)}{T_0} = 0. \tag{7}$$

Here, to distinguish between two different cycle periods, we denote the period at t_0 by T_0 (already known at this time) and one at t_n by T_n.

While (7) appears to be robust, a close examination reveals that (7) has a fundamental problem. Note that the lth row of the first equation and the second equation in (7) have the shared term $(x_l(t_{n+1}) - x_l(t_n))/T_n$. Similarly, $(x_k(t_{n+1}) - x_k(t_n))/T_n$ is shared by the kth row of the first equation and the third equation. Substituting the last two equal-phase equations into the lth and kth rows of the first equation leads to

$$\frac{x_l(t_n) - x_l(t_0)}{T_{env}} - \frac{x_l(t_1) - x_l(t_0)}{T_0} = 0$$
$$\frac{x_k(t_n) - x_k(t_0)}{T_{env}} - \frac{x_k(t_1) - x_k(t_0)}{T_0} = 0 \tag{8}$$

which correspond to forward Euler integration of the envelope of x_l and x_k, respectively. The explicit forward Euler method is not A-stable and has much degraded stability region. It is rarely used in practice. The formulation of (7) effectively
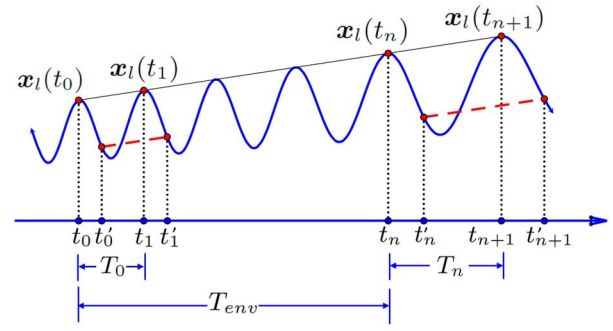
applies the explicit forward Euler type integration to the two phase monitoring nodes, a problem that shall be remedied by an improved equal phase condition introduced next.

C. Time-Delayed Equal-Phase Condition

A deep investigation reveals that the above problem stems from the fact that the introduced two phase conditions do not provide fully independent new constraints of the circuit state. In (7), shared terms involving envelope states exist between the lth row of the first equation and the second equation, and between the kth row of the first equation and the third equation. Such sharing renders the phase conditions and the backward-Euler-based EF equation constrain a common set of state variables and may manifest itself in several different ways. If the phase conditions are constructed by forcing the two monitored nodal voltages (or branch currents in general) to cross a predetermined level at equal phase points, a special case of the more general phase conditions adopted in (7), it can be shown that the equal phase equations would be identical to the lth and kth rows of the first equation of (7), rendering the full system underdetermined. As discussed already, the more general formulation of (7) immediately reduces the integration of two monitoring nodes to forward Euler while the deeper cause of this phenomenon is due to the sharing.

The key observation behind our solution to the above problem is to note that an equal-phase condition needs not to be defined at the beginning nor end of each cycle; it can be forced anywhere within a cycle. This observation leads to a new equal-phase condition, termed time-delayed phase condition, resulting in a new EF formulation:

$$\frac{x(t_n) - x(t_0)}{T_{env}} - \frac{x(t_{n+1}) - x(t_n)}{T} = 0$$
$$\frac{x_l(t'_{n+1}) - x_l(t'_n)}{T_n} - \frac{x_l(t'_1) - x_l(t'_0)}{T_0} = 0$$
$$\frac{x_k(t'_{n+1}) - x_k(t'_n)}{T_n} - \frac{x_k(t'_1) - x_k(t'_0)}{T_0} = 0 \tag{9}$$

where $t'_0 = t_0 + \alpha T_0$, $t'_1 = t_1 + \alpha T_0$, $t'_n = t_n + \alpha T_n$, and $t'_{n+1} = t_{n+1} + \alpha T_n$. $\alpha \in (0, 1)$ is a constant factor used to delay the sampling time of phase condition, as illustrated in Fig. 5. In (9), the first equation represents the same backward-Euler style equation involving the state variables at a set of four

points t_0, t_1, t_n, and t_{n+1}. In contrast, the last two equations specify the equal-phase condition at a different set of four points with each delayed by a fraction of the respective cycle time from the corresponding point in the first set. The two equal-phase condition in (9) constrain a different set of state variables from ones that are in the first equation. The new state variables that are forced to be at an equal phase are the future states of the corresponding variables in the first equation and are related to the latter variables through the nonlinear state transition characteristics of the converter excited by the external input.

D. Robust Numerical Solution

Our proposed EF method is described in (9) and the unknown vector that needs to be solved is

$$X = \left[x^T(t_n), T_n, T_{\text{env}} \right]^T. \tag{10}$$

To solve the system in (9) by the Newton–Raphson method, we need to evaluate the Jacobian matrix properly which involves computation of the sensitivities of each term in (9) with respect to any of the three unknown variables. The evaluation of sensitivities is done by computing the corresponding partial derivatives. Most of them are straightforward to evaluate except for those terms that involve the state transition function, explained as follows. Since in every Newton–Raphson iteration an inner-loop transient run from t_n to t'_{n+1} is performed in order to get $x(t_{n+1})$ and $x(t'_{n+1})$, the desired sensitivities terms can be accumulated through every transient step [12]. For convenience of notation, denote $x(t_n)$ by x_0 [not to be confused with $x(t_0)$ in Fig. 1] and the state at the kth step of the inner-loop transient simulation by x_k, (1) can be written as

$$\frac{q(x_k) - q(x_{k-1})}{h_k} + f(x_k) = u(t_k) \tag{11}$$

at the kth step of the transient simulation, with a stepsize of h_k. Differentiating (11) with respect to x_0 gives

$$\frac{\partial x_k}{\partial x_0} = \left[\frac{1}{h_k} \frac{\partial q(x_k)}{\partial x_k} + \frac{\partial f(x_k)}{\partial x_k} \right]^{-1} \left[\frac{1}{h_k} \frac{\partial q(x_{k-1})}{\partial x_{k-1}} \frac{\partial x_{k-1}}{\partial x_0} \right]. \tag{12}$$

Note that $(1/h_k)((\partial q(x_k))/(\partial x_k)) + ((\partial f(x_k))/(\partial x_k))$ is the Jacobian matrix of (1) and is available from the transient simulation. Starting from $(\partial x_0/\partial x_0) = I$, applying (12) repeatedly at every transient step and accumulating the results will give all the desired sensitivity terms with respect to x_0 along the way including $((\partial x_{n+1})/\partial x_0)$ in the end. Other sensitivity terms can be found in a similar way. Differentiating (11) with respect to T_n and T_{env} gives

$$\frac{\partial x_k}{\partial T_n} = \left[\frac{1}{h_k} \frac{\partial q(x_k)}{\partial x_k} + \frac{\partial f(x_k)}{\partial x_k} \right]^{-1} \left[\frac{1}{h_k} \frac{\partial q(x_{k-1})}{\partial x_{k-1}} \frac{\partial x_{k-1}}{\partial T_n} + \frac{\partial u(t_k)}{\partial T_n} + \frac{q(x_k) - q(x_{k-1})}{h_k T_n} \right] \tag{13}$$

and

$$\frac{\partial x_k}{\partial T_{\text{env}}} = \left[\frac{1}{h_k} \frac{\partial q(x_k)}{\partial x_k} + \frac{\partial f(x_k)}{\partial x_k} \right]^{-1} \left[\frac{1}{h_k} \frac{\partial q(x_{k-1})}{\partial x_{k-1}} \frac{\partial x_{k-1}}{\partial T_{\text{env}}} + \frac{\partial u(t_k)}{\partial T_{\text{env}}} \right]. \tag{14}$$

Starting from $(\partial x_0/\partial T_n) = 0$ and $(\partial x_0/\partial T_{\text{env}}) = 0$, all sensitivity terms with respect to T_n and T_{env} can also be accumulated by applying (13) and (14) repeatedly.

IV. UNIFYING PHASE TRACKING

An EF method transparently applicable to a variety of converters with PWM, PFM modulation or a combination of thereof, is highly desirable. In fact, a PFM converter may effectively operate under a constant switching frequency in steady state. We consider steady-states of PFM converters to motive the need for a new unifying phase condition.

A. Problems With Steady State EF Analysis

To see why the formulation of (9) may not be applied to steady state, we examine the following partial derivatives of the two phase conditions. Denote the first phase condition in (9) by g_1 and the second one by g_2. It can be shown that

$$\frac{\partial g_1}{\partial T_{\text{env}}} = \frac{1}{T_n} \left(\frac{\partial x_l(t'_{n+1})}{\partial T_{\text{env}}} - \frac{\partial x_l(t'_n)}{\partial T_{\text{env}}} \right) \tag{15}$$

$$\frac{\partial g_2}{\partial T_{\text{env}}} = \frac{1}{T_n} \left(\frac{\partial x_k(t'_{n+1})}{\partial T_{\text{env}}} - \frac{\partial x_k(t'_n)}{\partial T_{\text{env}}} \right). \tag{16}$$

When the circuit gets settled in steady state under constant input excitations, $((\partial u(t_k))/(\partial T_{\text{env}})) = 0$. According to (14), the sensitivity terms of (15) and (16) are both zero, implying that both phase conditions do not constrain unknown T_{env} and (9) becomes under-determined as a result. The root cause of this pathological situation is that the circuit appears to be autonomous in steady sate with its current/future states only depend on its past states, but not on time.

B. Phase Condition for Steady State

As a first step to addressing the above problem, we adopt a new steady state phase condition that involves T_{env} by noting that cycle T becomes a constant in steady state

$$T_n - T_0 = 0 \tag{17}$$

where T_0 is the cycle time at time t_0. Also in steady state, T_{env} is an integer multiple of T

$$T_{\text{env}} - nT_n = 0 \tag{18}$$

where n is the number of cycles skipped in one EF step. Replacing two phase conditions in (9) by (17) and (18) yields

$$\frac{x(t_n) - x(t_0)}{T_{\text{env}}} - \frac{x(t_{n+1}) - x(t_n)}{T_n} = 0$$
$$T_n - T_0 = 0$$
$$T_{\text{env}} - nT_n = 0. \tag{19}$$

The system described in (19) is equivalent to the classic EF algorithm for circuits with fixed switching frequencies described in (2), which can be used to reliably solve any steady state solutions.

C. Smooth Circuit State Tracking and Unifying Phase Condition

Till this point, we have developed two separate EF problem formulations in (9) and (19), respectively for transient and steady states. However, a circuit may transition between the two modes of operation back and forth and such transitions may be smooth and are not known *a priori*. Clearly, a unifying formulation is desirable. Denote the first phase condition in (9) by g_{11} and the phase condition described in (17) by g_{12}, namely

$$g_{11} = \frac{x_l(t'_{n+1}) - x_l(t'_n)}{T_n} - \frac{x_l(t'_1) - x_l(t'_0)}{T_0} \quad (20)$$

$$g_{12} = T_n - T_0. \quad (21)$$

Similarly, denote the second phase condition in (9) by g_{21} and the phase condition described in (18) by g_{22}, namely

$$g_{21} = \frac{x_k(t'_{n+1}) - x_k(t'_n)}{T_n} - \frac{x_k(t'_1) - x_k(t'_0)}{T_0} \quad (22)$$

$$g_{22} = T_{\text{env}} - nT_n. \quad (23)$$

The key idea in developing a unifying solution is to define a set of weighted new phase conditions

$$g_1 = \beta g_{11} + (1 - \beta)g_{12}$$
$$g_2 = \beta g_{21} + (1 - \beta)g_{22} \quad (24)$$

where $\beta \in [0, 1]$ is a continuous internal parameter that continuously tracks the current circuit mode of operation, as illustrated in Fig. 6. Using this new phase conditions, the unifying formulation of the EF problem is

$$T_{\text{env}}\big[x(t_{n+1}) - x(t_n)\big] - T_n[x(t_n) - x(t_0)] = 0$$
$$\beta g_{11} + (1 - \beta)g_{12} = 0$$
$$\beta g_{21} + (1 - \beta)g_{22} = 0. \quad (25)$$

We now discuss the significance and the implementation of the internal parameter β. Since the transitions between transient and steady states may not be abrupt, the goal behind the introduction of β is to provide a formal mathematical mechanism to track such transitions smoothly. As such, β is continuous valued in [0, 1]. Furthermore, such state transitions are not known *a priori*, hence, β shall not be set externally and must be an internal parameter that is dependent of the current circuit state. For this, while there exist multiple implementation choices for β, the following choice is found to be effective:

$$\beta = 1 - e^{-k\gamma} \quad (26)$$

where $\gamma = \|x(t_0) - x(t_n)\|^2$ and k is a scalar to balance between the values of g_{11} and g_{12} as well as g_{21} and g_{22}. When the circuit is at steady state, $\beta = 1 - e^{-k\|x(t_0)-x(t_n)\|^2} = 0$. Therefore, g_1 and g_2 are the same as steady state phase conditions g_{12} and g_{22}, respectively. As more transient behavior
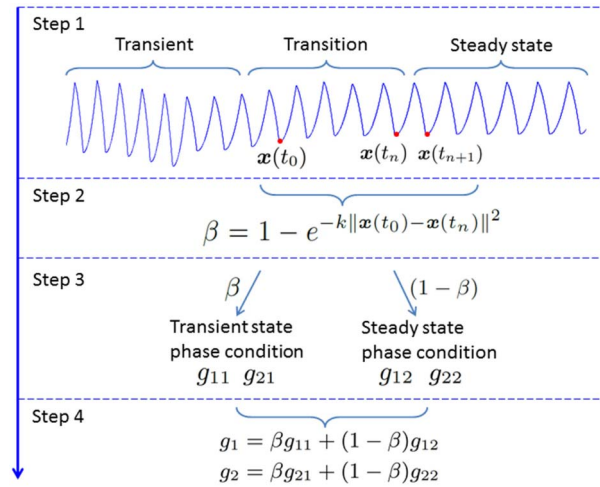

Fig. 6. Unifying phase condition. Steps 1 and 2 illustrate the dependency of the continuous mode tracking parameter β on current circuit state. Steps 3 and 4 weight phase conditions according to β to define the unifying phase conditions.

is excited in the circuit, the norm γ will gradually increase and β will increase accordingly, putting more weight on g_{11} and g_{21}. This mechanism has the desired properties to track the operation mode transition faithfully. For example, with $(\partial u(t)/\partial t) = 0$ and as the circuit transitions into steady state, β will not vanish immediately until it gets completely settled. It is also worth noticing that β is an unknown dependent on the unknown current state $x(t_n)$. The value of β can only become known after (25) is solved as a whole, providing generality and robustness for mode tracking.

V. FAST SIMULATION TECHNIQUES

In this section, three techniques are introduced to further improve the efficiency of the proposed EF algorithm. At the beginning of each EF step, a dynamic prediction scheme generates the best initial guess for $x(t_n)$ from three different initial solution predictors (ISPs). During each EF step, the simulator excludes certain digital nodes from convergence check, which reduces the number of iterations to reach convergence without degrading the accuracy of simulation results. At the end of each EF step, LTEs are estimated and the EF stepsize is changed using adaptive envelope step selection.

A. Dynamic Prediction Scheme

As shown in Fig. 7(a), a full cycle of transient simulation is performed for each Newton–Raphson iteration in one EF step. Since simulation of dc-dc converters is generally time-consuming, the full cycle transient analysis dominates the simulation time of EF in each step. To reduce the total simulation time and achieve higher speedups, the number of iterations in each step needs to be minimized. A good prediction on $x(t_n)$ can provide the simulator with a starting point that is close to the actual solution and need fewer iterations to reach convergence. However, no prediction methods can always generate the best initial guess due to the fact that dc-dc converters have different dynamic behaviors in different modes. Therefore, we
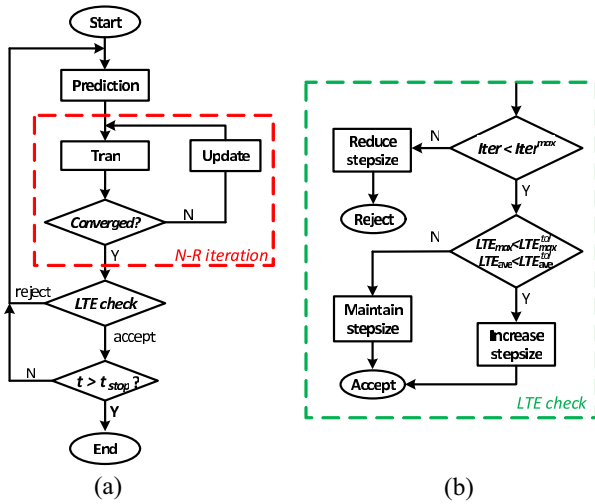
Fig. 7. (a) Simulation flow of proposed envelop following algorithm. (b) Flow of adaptive envelope step selection.
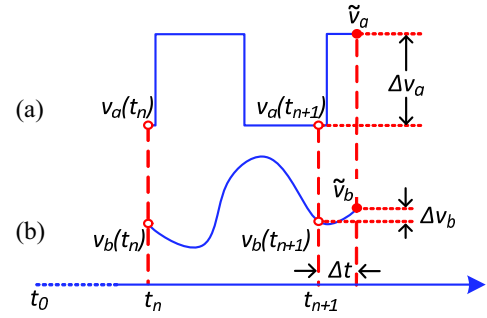

Fig. 8. Transient analysis waveforms of (a) an internal switching node and (b) the output node of the DC-DC converter in one iteration of an EF step.

proposed a prediction-selection scheme to provide the best initial guess for solution vector $x(t_n)$ from three different ISPs. The selections are made by comparing three perdition results and selecting the one with the least error.

The first predictor ISP_1 directly uses the solution from the last step as an initial guess for the current step, namely

$$x(t_n) = x(t_0). \tag{27}$$

The second predictor ISP_2 leverages the two solution vectors of the previous steps $x(t_0)$ and $x(t_1)$ and uses a linear extrapolation of the two as the initial guess for $x(t_0)$. Recall that in Fig. 4 we denote T_0 as the time period between t_0 and t_1, we have

$$x(t_n) = x(t_0) + \frac{T_{env}}{T_0}[x(t_1) - x(t_0)]. \tag{28}$$

The third predictor ISP_3 is first introduced in [13], which uses a linear extrapolation of the circuit transfer function ϕ to predict $x(t_0)$. To achieve this, we first observe that $\phi(x(t_0), t_0, T_0)$, which is the circuit transfer function from $x(t_0)$ to $x(t_1)$, is already available from the transient simulation of the last step. With this, we can approximate the circuit transfer function from $x(t_n)$ to $x(t_{n+1})$ using the first-order Tyler expansion

$$\phi(x(t_n), t_n, T_n) = \phi(x(t_0), t_0, T_0) + [x(t_n) - x(t_0)]\phi_x(x(t_0)) \tag{29}$$

where $\phi_x(x(t_0)) = (\partial\phi/\partial x)|_{x=x(t_0)}$. The left-hand-side of (29) is essentially equal to the solution vector $x(t_{n+1})$. Substituting (29) into the EF (2) results in:

$$x(t_n) = \left[\left(1 + \frac{T_n}{T_{env}}\right)I - \phi_x(x(t_0))\right]^{-1}$$
$$\left[\phi(x(t_0), t_0, T_0) - \phi_x(x(t_0))x(t_0) + \frac{T_n}{T_{env}}x(t_0)\right]. \tag{30}$$

Now, we have three different predictors and each of them generates accurate initial guesses for dc-dc converters operating in different modes. The first predictor (27) is essentially a zeroth order method, which generates accurate prediction when converters are near steady state. The second predictor method (28) is a first-order method and thus is effective for dc-dc converters with linearly changing load conditions. The third predictor (30) makes extrapolation of solution vectors based on circuit transfer functions. So it is most accurate when the circuit transfer function has almost linear changes between cycles and can be precisely calculated from the transient simulation.

To make the best uses of all three predictors, we design a selector that evaluates all three prediction results and chooses the one with the least error, which is measured by calculating distance from the given predicted solution to a valid circuit operating state. This can be done by setting the prediction result as the solution to the circuit and evaluate (1) with $u(t)$ moved to the left-hand-side. A non-zero residue vector on the right-hand-side can be acquired and the l_2 norm of such residue vector indicates how close the prediction is to the real circuit operating state. The predicted solution with the least l_2 error will be selected as the initial solution of the current step.

B. Automatic Node Selection for Convergence Check

DC-DC converters are mixed-signal circuits that include digital components with highly nonlinear behaviors. The outputs of those digital components have large swings and sharp transitions. As a result, the simulation is very challenging even for standard transient analysis with very small stepsizes. It is even more difficult for EF algorithm to efficiently reach convergence on these signals.

To illustrate this, the EF waveforms of two nodes in a PWM dc-dc converter are shown in Fig. 8, where the first node a is an internal node that drives the power switches and the second node b is the output node of the dc-dc converter. One Newton–Raphson iteration is shown where one cycle of transient simulation from t_n to t_{n+1} is performed for both nodes. At this iteration, the EF algorithm has found an accurate circuit state $v_a(t_n)$ and $v_b(t_n)$. Due to a small error Δt in cycle time T, the cycle starts from t_n and ends at $t_{n+1} + \Delta t$ instead of t_{n+1}. The corresponding end-of-cycle solution is $\tilde{v}_a$ and $\tilde{v}_b$, whereas the actual end-of-cycle solution is $v_a(t_{n+1})$ and $v_b(t_{n+1})$. For node b, if the error Δv_b and time difference Δt

are small enough, this solution will be accepted by the EF convergence check. However, the same conclusion cannot be drawn for node *a*, which shows a huge error in Δv_a due to the sudden change of voltage level within a short period Δt. As a result, this solution is not accepted by convergence check and the simulator has to keep iterating. However, even with more iterations, the Newton–Raphson method cannot efficiently converge to the actual solution, due to the fact that the waveform between t_{n+1} and $t_{n+1} + \Delta t$ of node *a* has discontinuous first order derivatives [14].

A simple way to fix this problem is to exclude node *a* and other nodes with sharp transitions from the convergence check. It is important to note that this does not affect the accuracy of the results since the solution of one EF step is $x(t_n)$, which is the circuit state at t_n rather than t_{n+1}. By avoiding choosing nodes excluded from convergence check as the phase monitoring nodes to calculate (20) and (22), we also make sure that the nodal voltage error of $x(t_{n+1})$ does not propagate to the evaluation of the phase conditions. To select the proper nodes for convergence check, a few cycles of transient simulation is conducted before the EF simulation is started. During the transient simulation, a node selector continuously monitors all node voltages and exclude any node that satisfies both of the following two criteria: 1) nodes with large swings that the nodal voltage reaches both 1% and 99% of the supply voltage V_{dd} within one cycle and 2) nodes with sharp slopes by checking if the maximum first order derivative of the nodal voltage exceeds certain threshold. In practice nodes that satisfy these two criterion are output nodes of the digital components of the internal control circuitry. After removing nodes that satisfy these two criteria, the EF simulation takes fewer iterations to reach convergence and the accuracy of the results are not compromised.

C. Adaptive Envelope Step Selection by LTE

To achieve good speedup factor while controlling accuracy, a backward-Euler-based LTE is utilized to predict the next envelope stepsize. The value of LTE is estimated during each step of EF [9]

$$\text{LTE} = \frac{T_{\text{env}}}{2}\left(\frac{x(t_{n+1}) - x(t_n)}{T_n} - \frac{x(t_1) - x(t_0)}{T_0}\right). \quad (31)$$

Note that the above LTE is a vector. We compute its l_2-norm LTE_{ave} and the l_∞-norm LTE_{max}. After solving each envelope step, LTE_{ave}, LTE_{max} and the number of Newton–Raphson iterations Iter are checked. Based on the LTE information, the current solution will be categorized into three different types, each leading to a specific action. If the number of iterations exceeds the maximum threshold Iter^{max} then the solution is rejected and a smaller stepsize is used to redo this EF step. If the iteration number is accepted, LTE_{ave} and LTE_{max} are compared with two prescribed tolerance values $\text{LTE}_{\text{ave}}^{\text{tol}}$ and $\text{LTE}_{\text{max}}^{\text{tol}}$. If both values are smaller than the tolerances, the stepsize is increased for the next EF step. Otherwise the same stepsize is maintained. Fig. 7(b) shows the detailed process of the adaptive envelope step selection.
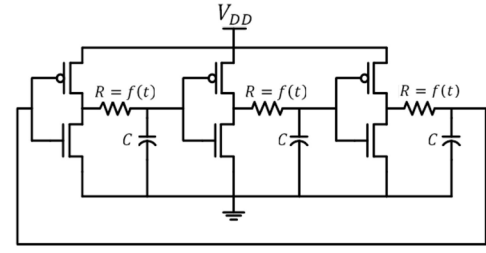

Fig. 9. Three-stage ring oscillator with the value of *R* controlled by a function of time $f(t)$.
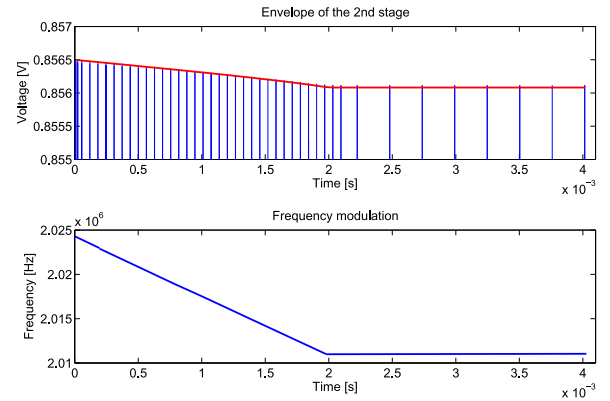

Fig. 10. Envelope of the second stage output voltage of the ring oscillator (top) and its frequency variation (bottom) simulated by the proposed EF method. In the top figure, the red line is the envelope while the blue lines are the transient responses obtained in each cycle of EF.

VI. SIMULATION RESULTS

The proposed EF technique with the unifying phase condition of (21) and fast simulation techniques has been implemented in a comprehensive in-house C++ based SPICE simulation environment with interfaces to industry standard BSIM4 transistor-level models. We first test the generality of the proposed unifying solution by applying the formulation in (22) to an oscillator. Then we move on to the circuits of our interest, PWM, PFM, and PSM dc-dc converters, and evaluate the efficiency and robustness of the proposed unifying method. We compare our method with the standard transient analysis in terms of speedups and accuracy and also comment on improvements over existing EF methods.

A. Three-Stage Ring Oscillator

The oscillator of Fig. 9 has three identical stages and the resistor of each stage is controlled by the same time varying function $f(t)$. To evaluate the performance of the proposed unifying EF method, $f(t)$ is designed in such a way that the oscillator transits between transient state and steady state. As shown in Fig. 10, the frequency of the ring oscillator first linearly decreases from 2.025 to 2.01 MHz in the first 2 ms and then remains at about 2.01 MHz for another 2 ms. Fig. 10 also shows in parallel the corresponding waveform of the second stage output nodal voltage simulated by the proposed EF method. From an initial value of $T_{\text{env}} = 32T_n$, the envelope step increases to $T_{\text{env}} = 128T_n$ during the
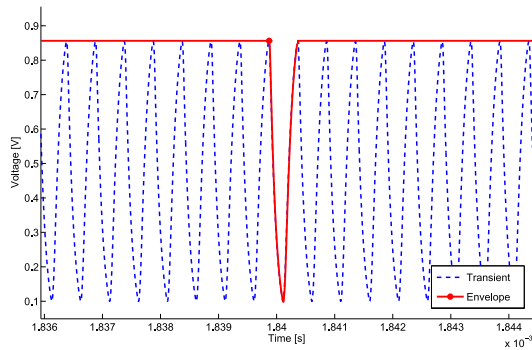
Fig. 11. Comparison between the proposed EF analysis (red solid line) and transient analysis (blue dashed line) of the ring oscillator.
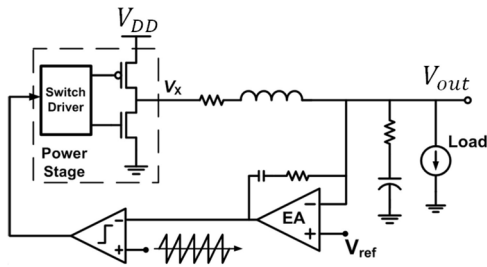

Fig. 12. PWM controlled dc-dc converter.

transient phase. As circuit enters to steady state and the estimated LTE decreases, the envelope step further increases to $T_{env} = 512T_n$ until the simulation ends. Fig. 11 compares the proposed EF method with the conventional transient analysis. The EF results match with those of the transient analysis with a high accuracy. An average speedup of $60\times$ is achieved with respect to the transient analysis. Among the existing methods, Mei and Roychowdhury [3] used similar circuits and obtains speedup factors of about $35\times$. Maffezzoni [9] and Mei and Roychowdhury [15] reported speedup factors higher than $60\times$ for oscillators. Though proven to be effective for ring oscillators, the proposed method may not be optimized for high-Q oscillators like crystal oscillators, due to the fact that the backward-Euler integration method, which we use for innerloop transient simulation, is a low-order method and has damping effects. In the next three examples we will simulate dc-dc converters with different modulation schemes, which are the main targeted circuits of our proposed methods.

B. PWM Controlled DC-DC Converter

Next, we focus on our targeted class of circuits, dc-dc converters that posses strong nonlinearities, hard switching activities, digital/memory and hysteretic effects, and strong feedback control. We first consider the startup transient of a standard dc-dc converter with PWM control that has all the essential real-life characteristics as shown in Fig. 12, where the switching frequency is determined by an external 10 MHz triangular signal applied to one of the comparator's inputs. The transistor-level schematics of the two key blocks, the error amplifier and comparator, are shown in Fig. 13. While operating with PWM control under a fixed switching frequency, testing our unifying EF technique without any
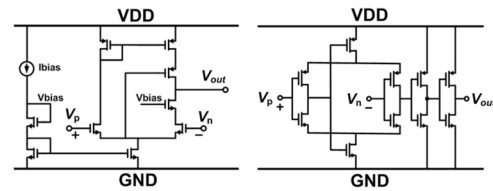

Fig. 13. Error amplifier (left) and comparator (right) of the PWM controlled dc-dc converter.
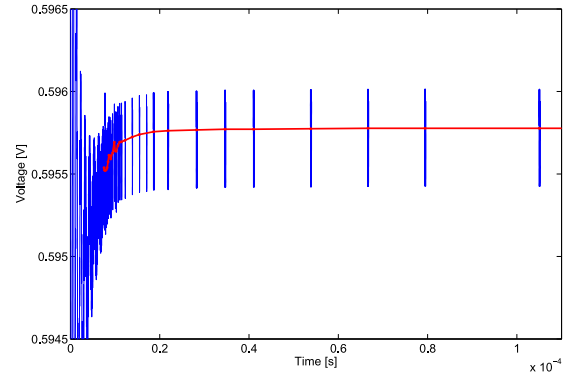

Fig. 14. Simulation of the PWM dc-dc converter using the proposed EF method. The red line is the envelope of the output voltage while the blue lines are the transient responses obtained in each cycle of EF.
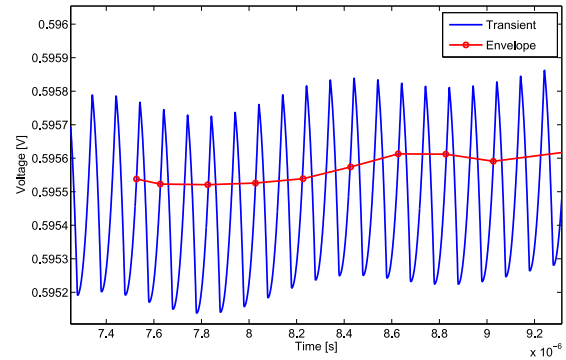

Fig. 15. Detailed comparison of EF results (red) and transient simulation results (blue) of the PWM dc-dc converter.

algorithmic-level change on this circuit would demonstrate its generality.

Fig. 14 shows the EF results of the PWM converter output response. The envelope step is gradually increased until steady state is reached. Fig. 15 compares our EF method with the transient analysis for the early startup phase, where the output node has the most dynamic response, showing the ability of our method in closely tracking the changing amplitude of output voltage.

Overall a speedup factor of $20\times$ is achieved in this example. In comparison, speedup factors in the range of $6\times$ are reported for PWM converters in [2]. The simulation speedup improvement of our proposed method over [2] is mainly due to the use of the fast simulation techniques. First of all, the dynamic prediction scheme selects a mix of ISP_2 and ISP_3 at the beginning of the startup simulation. Then it switches to ISP_1 to predict the initial solution using the solution from previous step as the output voltage of the converter reaches the peak and
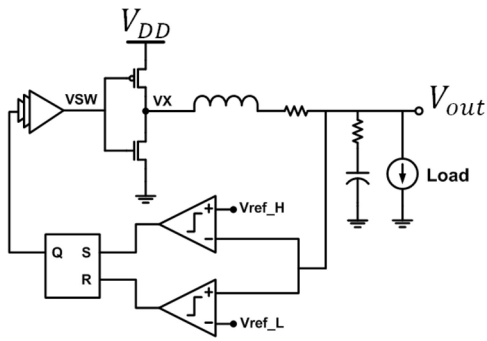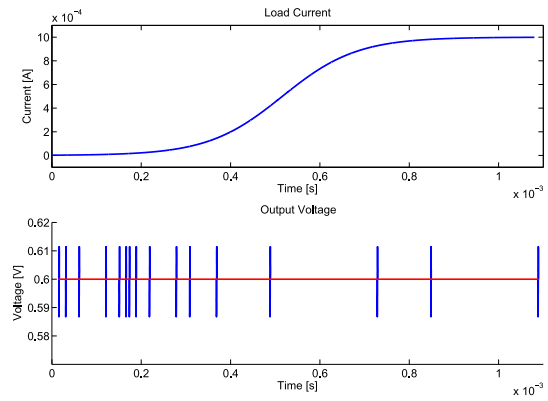
Fig. 16. Hysteretic/PFM dc-dc converter.

Fig. 17. Load current waveform (top) and the envelope of the hysteretic converter output node response simulated by our EF method (bottom). In the bottom figure the red line is the envelope while the blue lines are the transient responses obtained in each cycle of EF.

the dynamic behaviors of the converter gradually settle down. The second technique that bring the performance improvement is the adaptive envelope step selection scheme. As shown in Fig. 14, the envelope step selection scheme dynamically adjust the envelope step size T_{env} of the algorithm based on the LTE of each step, which make best use of the multirate characteristics of dc-dc converters. Finally, the automatic node selection excludes nodes with digital behavior and sharp transitions from the convergence check, resulting in a fast convergence without compromising the accuracy.

C. PFM DC-DC Converter

The next circuit we consider is a hysteretic/PFM dc-dc converter in Fig. 16. This circuit, along with other autonomous dc-dc converters, are the primary target of our proposed method. As shown in Fig. 16, a hysteretic comparator that consists of two separate high-gain comparators constantly compare the output voltage with a high (V_{ref_H}) and low (V_{ref_L}) threshold voltages. The outputs of the hysteretic comparator feed an SR-latch and then drive the two power switches. As such, the converter forces the output voltage to stay between V_{ref_L} and V_{ref_H} by dynamically adjusting the turn-on time of the pMOS power switch.

This is a challenging circuit for testing the robustness of the proposed EF technique due to its strong nonlinearity, high-gain blocks, hysteretic/memory effects, and feedback control. Even for the standard transient analysis, a source ramping scheme and/or tight stepsize control need to be in place to guarantee convergence and accuracy.

The load current of the converter increases from 0 to 1 mA following a sigmoid function, resulting in a switching frequency change from 1.06 to 1.11 MHz. The corresponding envelope of the output response is shown in Fig. 17. From a conservatively chosen envelope stepsize of $T_{env} = 16T_n$, the simulator gradually scales up the envelope stepsize according to the estimated LTE until the circuit enters into steady state. After that, the load current approximately linearly increases from 0.4 to 0.7 ms. As shown in Fig. 17, during this period of time, the envelope stepsize actually increases. This boost of performance comes from an internal scheme for guessing the new x_n value at the beginning of each envelope step that is based upon a linear extrapolation of x_0 and x_1, which are available before the Newton iteration starts. This prediction mechanism happens to provide fairly accurate initial
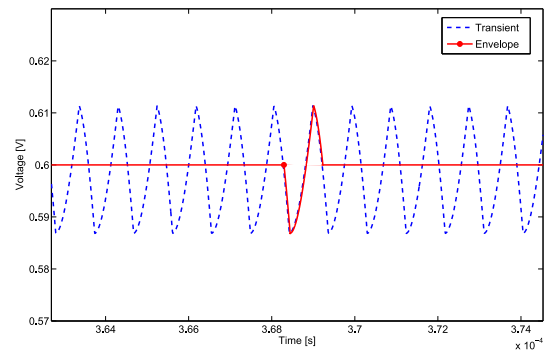

Fig. 18. Detailed comparison of the proposed EF method (red solid line) with the transient analysis (blue dashed line) for the PFM/hysteretic converter.

guesses while the load current approximately rises up linearly. In conjunction with the implemented LTE stepsize control, the scheme boosts the envelope stepsize allowed by the LTE tolerance around time 6 ms as shown in the bottom plot of Fig. 17. Fig. 18 compares the detailed EF results with the transient simulation results. The computed envelope accurately matches the transient simulation, demonstrating ability of our proposed method to closely track the envelope of highly dynamic and nonlinear converters with a varying switching frequency.

Our EF method achieves a speedup of 30× with respect to the transient analysis for this example. Very few reported works target autonomous dc-dc converters under varying load conditions. Kato *et al.* [7] demonstrated analysis of two autonomous converters using constant envelope steps of 3 and 5 without reporting any speedup factors. As discussed in Section I, a simplistic switched linear system model is adopted to model converters with an additional assumption on variation of cycle time that is not generally true in [7].

D. PSM DC-DC Converter

The last circuit we consider is a PSM dc-dc converter in Fig. 19, which represents one of the most popular dc-dc converter topologies in low-power design. This circuit is essentially an enhanced PWM dc-dc converter with the ability to
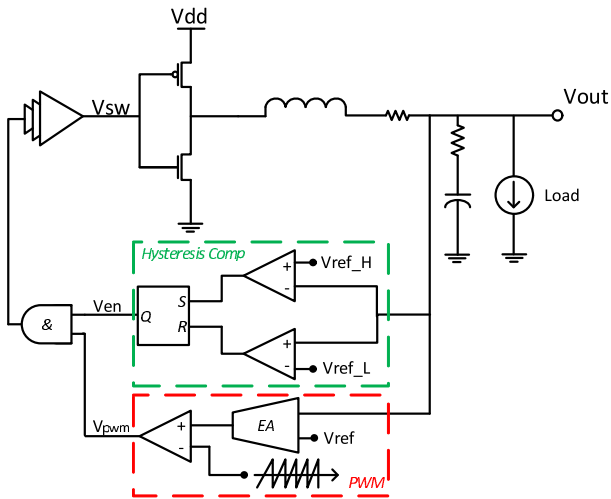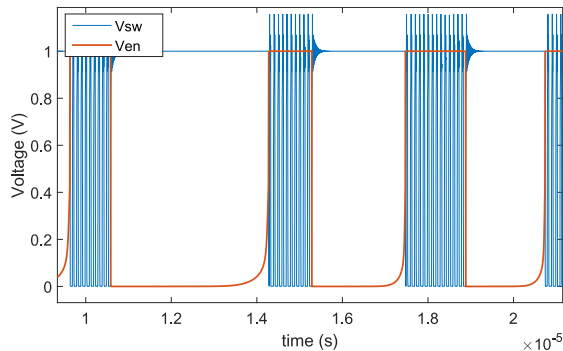
Fig. 19.   PSM dc-dc converter.

Fig. 20.   Switching signal V_{sw} and the enabling signal V_{en}.
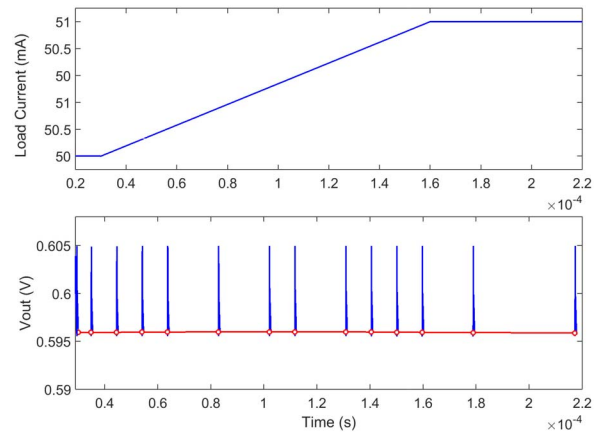

Fig. 21.   Linearly increasing load current (top) and the output node voltage response simulated by the proposed EF method (bottom). In the bottom figure the red line is the envelope while the blue lines are the transient responses obtained in each step of EF.

TABLE I
SIMULATION RESULTS FOR DC-DC CONVERTERS

		PWM	PFM	PSM
Number of nodes		22	31	41
Number of transient steps	TR	192,473	10,881,234	1,100,001
	EF	9,780	322,307	115,115
Total number of transient N-R iteration	TR	415,737	1,121,5154	1,374,336
	EF	20,737	365,974	132,590
Simulation time (sec)	TR	906	112,321	24,707
	EF	54	3,691	2,203
Speedup		20X	30X	11X

skip pulses when the output voltage is above certain threshold voltage. The hysteretic comparator compares V_{out} with two threshold voltages V_{ref_L} and V_{ref_H} and generates a binary enabling signal V_{en}. The PWM module compares the voltage difference between reference voltage V_{ref} and generates a series of pulses V_{pwm} to drive the power switches. When the output voltage is below V_{ref_L}, the enabling signal V_{en} is high and the power switches are directly driven by the PWM pulse signals, resulting in an increase of output voltage. By the time V_{out} reaches the upper threshold voltage V_{ref_H}, the enabling signal V_{en} becomes zero and the pulse signal generated by the PWM module is blocked by the AND gate. Thus the converter skips all PWM pulse signals until V_{out} drops below the lower threshold again.

Fig. 20 shows the waveforms of V_{en} and V_{sw}. When enabling signal $V_{en} = 1$, the PWM module generates multiple pulses to drive the power switches. The occurrence and number of PWM pulses depend on the load condition and are not known *a priori*. Thus EF simulation of this type of circuits is extremely challenging. In order to robustly apply the proposed EF algorithm to this type of circuits, we pick V_{out} and V_{en} as the phase monitoring nodes and define the cycle of the circuit by the periodic behavior of V_{en} rather than that of V_{sw}.

The results of EF simulation are shown in Fig. 21. The top waveform shows a linearly changing load current increased from 50 to 51 mA. The bottom waveform shows the voltage responses of the output voltage V_{out}. Starting from $T_{env} = 8\ T$, our proposed algorithm automatically adjusts stepsize based on the estimated LTE values. With the help of prediction, our proposed algorithm maintains a rather large stepsize during the period when the load current linearly increases. The circuit finally reaches the steady state at $t = 0.18$ ms and after that the stepsize quickly increases to $T_{env} = 64\ T$. Overall, a speedup of $10X$ is achieved with respect to transient analysis.

Table I summarizes the simulation results of PWM, PFM, and PSM dc-dc converters. The speedup of the proposed EF method with respect to the standard transient simulation are calculated based on the simulation time of both methods.

VII. CONCLUSION

A robust and efficient EF method is presented for circuits with constant or variable switching frequencies. At the core of our new EF algorithm are a novel time-delayed equal-phase condition and a mechanism that smoothly tracks the transitions of the circuit state. The implementation of fast simulation technique improves the efficiency of the algorithm while maintaining the same accuracy level. We verify the robustness, generality, and efficiency of the proposed technique using several test circuits for which our technique offers excellent simulation speedups and robustness.
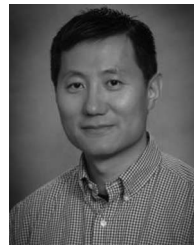
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Peng Li (S'02–M'04–SM'09–F'16) received the B.Eng. degree in information engineering and the M.Eng. degree in systems engineering from Xian Jiaotong University, Xian, China, in 1994 and 1997, respectively, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2003.

Since 2004, he has been with the Faculty of the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX, USA, where he is currently a Professor. His current research interests include very large scale integration systems, electronic design automation, and aspects of computational neuroscience.

Prof. Li was a recipient of various awards including the 2013–2014 William and Montine P. Head Fellow from the College of Engineering, Texas A&M University, the IEEE/ACM William J. McCalla ICCAD Best Paper Award in 2012, the 2011–2012 TEES Fellow Award from the College of Engineering, Texas A&M University, three IEEE/ACM Design Automation Conference Best Paper Awards in 2003, 2008, and 2011, the U.S. National Science Foundation CAREER Award in 2008, the ECE Outstanding Professor Award from Texas A&M University in 2008, two MARCO Inventor Recognition Awards in 2006 and 2007, and two SRC Inventor Recognition Awards in 2001 and 2004. He was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS from 2008 to 2016 and currently an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS.

Ya Wang received the B.S. degree in electrical engineering from Xian Jiaotong University, Xian, China, in 2012. He is currently pursuing the Ph.D. degree in electrical and computer engineering with Texas A&M University, College Station, TX, USA.
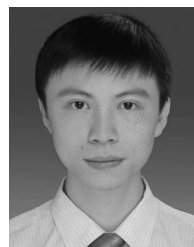
His current research interests include efficient simulation techniques of dc–dc converters as well as modeling of dc–dc converter in low power design.

Suming Lai received the B.S. degree in electronic science and technology and the M.Eng. degree in microelectronics and solid-state electronics from Xi'an Jiaotong University, Xi'an, China, in 2006 and 2009, respectively, and the Ph.D. degree in computer engineering from Texas A&M University, College Station, TX, USA, in 2014.

Since 2014, he has been with Maxim Integrated, San Diego, CA, USA, as a member of technical staff on IC design. His current research interests include analog and mixed-signal IC design, especially power/battery management IC design, and computer-aided design of IC power delivery networks.

Dr. Lai was a recipient of the William J. McCalla Best Paper Award at the IEEE/ACM International Conference on Computer-Aided Design, in 2012.