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Inversion Reduction Method for Real and Complex Distribution Feeder Models

Zachary K. Pecenak, Vahid R. Disfani, Matthew J. Reno, and Jan Kleissl

***Abstract*—The proliferation of distributed generation on distribution feeders triggers a large number of integration and planning studies. Further, the complexity of distribution feeder models, short simulation time steps, and long simulation horizons rapidly render studies computational burdensome. To mend this issue, we propose a methodology for reducing the number of nodes, loads, generators, line, and transformers of *p*-phase distribution feeders with unbalanced loads and generation, non-symmetric wire impedance, mutual coupling, shunt capacitance, and changes in voltage and phase. The methodology is derived on a constant power load assumption and employs a Gaussian elimination inversion technique to design the reduced feeder. Compared to previous work by the authors, the inversion reduction takes half the time and voltage errors after reduction are reduced by an order of magnitude. Using a snapshot simulation the reduction is tested on six additional publicly available feeders with a maximum voltage error 0.0075 p.u. regardless of feeder size or complexity, and typical errors on the order of 1×10^{-4} p.u. For a day long QSTS simulation on the UCSD A feeder, errors are shown to increase with changes in loading when a large number of buses removed, but shows less variation for less than 85% of buses removed.**

***Index Terms*—Distribution system, network reduction, mutual impedance, quasi static time-series simulations.**

NOMENCLATURE

$\mathbf{Z}$	Nodal Impedance Matrix
$\tilde{V}$	Nodal complex nominal voltages
I, J, K	Index of set of nodes of a bus
i, j, k	Index of bus
M	Set of nodes on the original feeder
m	Set of nodes on the reduced feeder
o	Subscript indicating original feeder
p	Number of phases
r	Subscript indicating reduced feeder
S	Complex power
X	Load/generation model
CB	Critical Bus, kept after reduction

I. INTRODUCTION

THE introduction of distributed energy resources (DER) into distribution networks en masse has transformed the study of power systems . Utility scale planning studies must consider the uncertainty in these resources and devise mitigation techniques under a plethora of operating conditions [1–3].

As more DERs are employed to meet the renewable generation goals being set globally [4], the complexity of these studies will compound. For a current example, the proposal of the Western Energy Imbalance Market will require voltage and phase information of the entire western interconnection simultaneously, which at roughly 80,000 nodes induces incredible computational expense. [5]. As a result, solutions to reduce the time required to carry out such studies are becoming increasingly important [6–9]. Network reduction provides a means for reducing the complexity and associated time of the systems being studied by removing buses and lines of a circuit to lessen the number of variables that must be solved. Thus, time savings are realized at the cost of ignoring state variables on certain buses.

In reference [10] four of the more popular network reduction techniques are discussed and compared for performance in static power flow simulations: i) Ward reduction [11], ii) Kron reduction [12], iii) Dimo's method [13], and iv) Zhukov's reduction [14]. For the two feeders investigated (IEEE 14 bus and IEEE 118 bus), all methods were shown to produce significant error in voltage due to reduction (> 0.01 pu), while the Ward reduction method produced the lowest error overall. However, the Ward reduction requires an initial solution to the power flow (which increases computational cost) and assumes fixed current loads. All of the methods are designed for transmission networks which tend to be balanced systems designed with symmetrical components. A body of research [15–17] has been performed for multiphase transmission systems for network equivalence from the electromagnetic transient perspective.

Recently, a body of work specifically tailored to distribution feeder simplification has emerged. The segmentation method in reference [18] introduces a constant power assumption to the literature on distribution network reduction. The methodology replaces model segments between two buses of interest with characteristic equations representing a simpler topology. The methodology is tested on Feeder J1 [19] and produces a small maximum voltage error of ($\mathcal{O}(10^{-3})$). However, an initial power flow is still needed as a system input and the authors retain capacitors, voltage regulators, PV systems, and the corresponding distribution transformers in the reduction, limiting the number of buses that can be removed.

A distribution feeder reduction technique for balanced distribution systems is proposed in [6] which does not require an initial power flow solution. Load and PV is aggregated recursively between a subset of buses until the entire network

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is reduced. When implemented in OpenDSS [20], the method produced negligible voltage error for the distribution feeder investigated. However, the feeder is modeled with no imbalance in generation or loading, symmetric impedance between buses without mutual coupling, and negligible shunt capacitance, and only a single voltage level, which is unrealistic. Further reduction across voltage levels is not considered, requiring transformer nodes to be kept in the reduced model, which increases computational cost.

In [21], the method proposed in [6] was enhanced to allow mutual coupling and imbalance in line impedance, and imbalance in loading. In addition, a weighting scheme preserved spatial and temporal variations in load and generation in the reduced feeder. Extensive validation on a 3-phase 621 bus feeder with unbalance in load, generation, and line loading was performed. Errors were ($\mathcal{O}(10^{-3})$) and the simulation time for a year long integration study was reduced by up to 96%.

Despite the improvements in applicability and accuracy in [21], it preserved a number of assumptions from previous methodologies: 1) While individual load models are preserved during the reduction process, the reduction methodology is formulated based on the assumption of fixed current loads which do not accurately represent common loads; 2) Shunt capacitance is ignored, which is a critical part of realistic distribution networks; 3) Reduction across voltage transformers is not possible, requiring the inclusion of extra buses in the reduced feeder; 4) The recursive nature of the algorithm causes the reduction times to scale with feeder size.

To overcome these limitations, a disparate and novel technique for reduction of multiphase unbalanced distribution feeders is presented here. The reduction methodology is a Gauss elimination matrix inversion technique which is derived using a more common fixed power model assumption for loads and generators.

The inversion reduction methodology is the first to demonstrate that the use of Guassian elimination techniques for reduction of feeders automatically considers complexities of multiphase unbalanced systems. In fact the methodology is shown to be a generalization of [21], with additional terms which facilitate the aggregation of load and generation across voltage transformers and the inclusion of shunt impedance in lines and buses.

The contributions of this paper to the literature on distribution network reductions are as follows:

1) Development of a methodology which can be applied with or without a power flow simulation or measured data
2) Improving on existing methods to account for complexities such as
   - shunt capacitance in distribution lines
   - feeders with multiple voltage levels
   - voltage-independent capacitor banks
   - reduction based on power (not current)
3) Reduction through a single calculation as opposed to a recursive formulation, rendering the method easier to implement and reducing computational cost
4) Algorithm for transforming admittance matrix to circuit elements as required by commercial power flow solvers

The rest of the paper is organized as follows. Section II briefly introduces the methodology in [21] to facilitate the comparison of the methods. In Section III, we derive the new inversion reduction methodology. Section IV demonstrates the inversion reduction on a simple 3 bus system and compares the proposed methodology with the method from [21]. The algorithm is given in Section V. Section VI discusses the error sources associated with the method and its assumptions. Section VII concludes the paper.

II. Review of Reference [21]

A. Introduction

The approach in [21] was a recursive method, which for a set of desired or critical buses (CB), looped through all the non-critical buses (NCB) and eliminated them by moving current injections to neighboring buses. For any set of neighboring buses i, j, k, where j is between buses i and k, we can write the p-phase voltage vector for buses j and k as follows:

$$V_j = V_i + \mathbf{Z_{ij}}(I_j + I_k) \tag{1}$$

$$V_k = V_j + \mathbf{Z_{jk}} I_k, \tag{2}$$

where $V \in \mathbb{C}^{p\times 1}$ and $I \in \mathbb{C}^{p\times 1}$ are the vectors of voltages and current injections of the p-phase bus, and $\mathbf{Z} \in \mathbb{C}^{p\times p}$ is the full impedance matrix of the line connecting the buses, where the diagonal elements denote self impedances and off-diagonal elements denote mutual impedances between different phases of the line.

B. End Bus Removal

An "end-bus" reduction of k onto j can be performed if there are no CB downstream of k. From equation (1), the voltage at bus j does not depend on V_k or Z_{jk}. Thus bus k and the line connecting j to k can be removed from the circuit, while I_k is moved onto bus j.

$$I_j^{\text{new}} = I_j + I_k \tag{3}$$

Note equation (1) is only a function of Z_{ij}, not Z_{jk}, indicating that the impedance between buses j and k is simply removed from the reduced circuit.

C. Middle Bus Removal

Removing the middle bus j from the circuit (dubbed "middle-bus" reduction) requires re-arranging equations 2 and 1 as follows:

$$V_k = V_i - \mathbf{Z_{ij}} \times (I_j + I_k) - \mathbf{Z_{jk}} \times I_k \tag{4}$$

$$V_k = V_i - (\mathbf{Z_{ij}} + \mathbf{Z_{jk}}) \times (I_k + (\mathbf{Z_{ij}} + \mathbf{Z_{jk}})^{-1} \times \mathbf{Z_{ij}} \times I_j) \tag{5}$$

We can restate equation (5) in the form given in equation (6)

$$V_k = V_i - \mathbf{Z}_{\text{eq}} \times I_k^{\text{new}} \tag{6}$$

where,

$$\mathbf{Z_{eq}} = \mathbf{Z_{ij}} + \mathbf{Z_{jk}} \tag{7}$$

$$I_k^{\text{new}} = I_k + (\mathbf{Z}_{\text{eq}})^{-1} \times \mathbf{Z_{ij}} \times I_j \tag{8}$$

As indicated in (6) to remove bus j, bus i is connected to bus k through an equivalent line with impedance equal to the summation of the two original lines. Further, a contribution of I_j is transferred to bus k according to the ratio of impedance between j and k to the equivalent impedance ($\mathbf{Z_{eq}}^{-1} \times \mathbf{Z_{ij}}$).

A similar relationship holds for the updated current on bus i, where $I_i^{\text{new}} = I_i + (\mathbf{Z}_{\text{eq}})^{-1} \times \mathbf{Z_{j,k}} \times I_j$.

D. Spatial and Temporal Variation in Load / Generation

The resulting reduced feeder is composed of loads and generation on the CBs, which are based on the aggregated current injections from the removed buses. However, the load and generation on the reduced feeder is only valid for the snapshot of loading conditions used during the reduction process. To remove the need for reduction after every change in load and generation, a weight matrix $\mathbf{W} \in \mathbb{C}^{M\times M}$, where M is the set of nodes in the original feeder, is introduced. Initially, $W_{ii} = 1$, while $W_{ij} = 0$, indicating that all loads are on their own node. As reduction progresses, $\mathbf{W}$ is updated by removing rows corresponding to nodes which are removed from the circuit and adding the values to the node that the load is being aggregated to. Any non-zero W_{ij} in the final $\mathbf{W} \in \mathbb{C}^{m\times M}$ indicates the ratio of current injection on node i which now resides on node j. Here m is the set of nodes in the reduced feeder.

III. Inversion Method Derivation

A. Circuit reduction

Here, a new approach to reducing a distribution feeder is proposed, which is formulated as a Gauss elimination inversion technique and is carried out in a single calculation, as opposed to looping through all CB in the circuit. A constant power load model is assumed, which is more representative of industrial and residential loads than the more common fixed current assumption, which is most applicable to special lighting load. The constant power load model assumption is solely used for derivation purposes, while individual load models are retained in the reduction.

The inversion reduction methodology is applicable to both radial and meshed feeders. The choice of reduced feeder network and the topology detection algorithms differ for meshed or radial system. This paper presents the reduction algorithms for radial feeders. The application to meshed feeders will be a topic of future work.

For the original or full feeder (subscript "o"), the vector of complex voltages of each node is given as $V_o \in \mathbb{C}^{M\times 1}$ and the vector of complex current injections at each node is $I_o \in \mathbb{C}^{M\times 1}$. The two variables are related through the nodal voltage equation by the system admittance matrix $\mathbf{Z_o} \in \mathbb{C}^{M\times M}$

$$V_o = \mathbf{Z_o} \times I_o. \tag{9}$$

The relations given in (9) represents just the system admittance and power injection. Traditionally, this relation uses a swing bus where the first element of I_o is a variable. In our formulation, the swing bus is not needed and if no load is present on the first node, that entry is zero. Similarly, we define a reduced feeder (subscript "r") with complex voltage vector of all m nodes of the reduced feeder $V_r \in \mathbb{C}^{m\times 1}$, complex current injection vector $I_r \in \mathbb{C}^{m\times 1}$, and impedance matrix $\mathbf{Z_r} \in \mathbb{C}^{m\times m}$. Akin to (9) we observe $V_r = \mathbf{Z_r} \times I_r$.

Requiring voltage equivalence before and after reduction at all buses in the reduced feeder (i.e. the CB of the full feeder) yields

$$V_{o,\text{CB}} = V_r, \tag{10}$$

where $V_{o,\text{CB}}$ is the subset of voltages in the full feeder corresponding to the CB. $V_{o,\text{CB}}$ is the product of the impedance matrix with NCB rows removed $\mathbf{Z}_{o,CB} \in \mathbb{C}^{m\times M}$ and the current injection vector I_o. Inserting (9) into (10) we obtain

$$\mathbf{Z}_{o,\text{CB}} \times I_o = \mathbf{Z}_r \times I_r. \tag{11}$$

To remove the dependence on current, we introduce the vectors of complex power for each node, $S_o \in \mathbb{C}^{M\times 1}$ and $S_r \in \mathbb{C}^{m\times 1}$ in the full and reduced feeders, respectively.

$$S_o = \tilde{V_o} \otimes I_o^* \tag{12}$$

$$S_r = \tilde{V_r} \otimes I_r^*, \tag{13}$$

where the superscript $*$ represents the conjugate operation and $\otimes$ is element-wise multiplication.

$\tilde{V_o}$ and $\tilde{V_r}$ are the complex voltage vectors representing the original and reduced feeders. The voltage vector definition is flexible, but the following scenarios may be most typical: (i) voltages from an initial power flow for a stationary point according to nominal loading; (ii) nominal voltages defined based on the nominal transformer ratios and phase shifts due to the type of transformers. To avoid an initial power flow, nominal voltages are used in the application of (12) and (13). The choice of voltage vector effect on reduction error is examined in section VI-E.

Solving for current

$$I_o = (\tilde{V_o}^{\text{inv}} \otimes S_o)^* \tag{14}$$

$$I_r = (\tilde{V_r}^{\text{inv}} \otimes S_r)^* \tag{15}$$

where $\tilde{V_o}^{\text{inv}}$ and $\tilde{V_r}^{\text{inv}}$ denote the element-wise inversion of the vectors $\tilde{V_o}$ and $\tilde{V_r}$ respectively. Substituting (14), (15) into (11) and solving for the vector of powers in the reduced system

$$S_r = \tilde{V_r} \otimes [(\mathbf{Z}_r^{-1} \times \mathbf{Z}_{o,CB})^* \times (\tilde{V_o}^{inv} \otimes S_o)]. \tag{16}$$

As for an arbitrary matrix A and two arbitrary vectors B and C, one can prove that $A \times (B \otimes C) = A \times diag(B) \times C$ and $B \otimes (A \times C) = diag(B) \times A \times C$, we rewrite (17) as

$$S_r = \mathbf{diag}(\tilde{V_r}) \times (\mathbf{Z}_r^{-1} \times \mathbf{Z}_{o,\text{CB}})^* \times \mathbf{diag}(\tilde{V_o}^{\text{inv}}) \times S_o, \tag{17}$$

indicating that for a chosen $\mathbf{Z}_r$ we can define a new set of equivalent loads and generation powers. Although the choice of $\mathbf{Z}_r$ is not unique, a logical choice is to simply remove the matrix rows and columns corresponding to the nodes that were removed from the system. That is, the admittance matrix

for the reduced feeder $\mathbf{Y}_r = \mathbf{Z}_r^{-1}$ is composed of equivalent impedances between the remaining buses and shunt elements such as capacitor banks. This is discussed in detail in section V.

B. Spatial and Temporal Variation in Load/Generation

Similar to [21], a weighting matrix $\mathbf{W} = S_r/S_o$ is adopted to aggregate original powers onto CB. From equation (17), $\mathbf{W} \in \mathbb{C}^{m \times M}$ is

$$\mathbf{W} = \mathbf{diag}(\tilde{V_r}) \times (\mathbf{Z}_r^{-1} \times \mathbf{Z}_{o,CB})^* \times \mathbf{diag}(\tilde{V_o}^{inv}) \quad (18)$$

Note that removing the nominal voltage matrices from $\mathbf{W}$ (i.e. assuming $\tilde{V_r} = \tilde{V_o}$), yields $\mathbf{W}_o = (\mathbf{Z}_r^{-1} \times \mathbf{Z}_{o,CB})^*$ which produces the same weighting matrix as in reference [21]. The addition of the nominal voltage matrices allows for the mapping of load and generation profiles across different voltage levels (i.e. across transformers).

C. Load / Generation Model Mapping

Generators and loads can be modeled in a variety of different ways. For example, OpenDSS has 7 options to model feeder loads and 7 options to model generators in addition to a model for PV. To retain these models through the reduction process, S_o can be defined as a matrix, where each column indicates a different load type (i.e. $\mathbf{S}_o \in \mathbb{C}^{M \times X}$ where X is the number of load types on the feeder). The proposed methodology which aggregates loads/generators into a single equivalent on retained buses is not suitable for reduction of Zip or multi-state load models [22] since individual load parameters would be lost. However, the method is expanded to reduce such loads models in reference [23].

IV. Example Reduction of 3 Bus System

A. Two lines

To illustrate a feeder reduction, a sample feeder is shown in Fig. 1. First, a single phase, three bus system connected by two lines is chosen to provide direct comparison to the methodology formulated in [21] and to provide intuition about the relationship between the original and reduced circuit. However, the methodology is applicable to any M bus, p-phase phase system. We define the system as follows:

$$\tilde{V_o} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, S_o = \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} \quad (19)$$

$$\mathbf{Z}_o = \begin{bmatrix} \frac{1}{z_{11}} + \frac{1}{z_{12}} & -\frac{1}{z_{12}} & 0 \\ -\frac{1}{z_{12}} & \frac{1}{z_{12}} + \frac{1}{z_{22}} + \frac{1}{z_{23}} & -\frac{1}{z_{23}} \\ 0 & -\frac{1}{z_{23}} & \frac{1}{z_{23}} + \frac{1}{z_{33}} \end{bmatrix}^{-1} \quad (20)$$

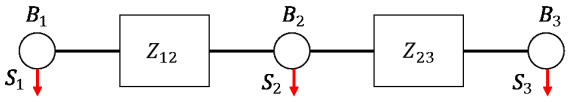

Fig. 1: Line model depicting a single phase 3 bus system connected by two lines. Each bus B injects power S_B. The impedance between a bus and its neighbor is denoted as Z_{ij}, while shunt impedance is denoted as Z_{ii}.

1) End bus reduction through removal of bus 3: To remove bus B_3, the rows and columns corresponding to B_3 in the admittance matrix can be removed to generate Z_r. Likewise, $\tilde{V_r}$ is equivalent to $\tilde{V_o}$ with the omission of the row and column corresponding to V_3. Solving (17) yields the power vector for loads and generators in the reduced feeder.

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_2^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 + S_3 \frac{1}{1+\frac{z_{23}}{z_{33}}} \frac{V_2}{V_3} \end{bmatrix} \quad (21)$$

The equation indicates that the power on B_1 remains the same ($S_1^{\text{new}} = S_1$). However, at B_2 a scaled power of B_3 with respect to both voltage and impedance is added. The scaling with respect to voltage accounts for change in phase and voltage magnitude, allowing loads to be aggregated across transformers, which can then be removed from system. The scaling due to impedance accounts for the shunt impedance on the bus, which was neglected in [12], and is a result of the full impedance matrix being used to calculate the updated loads.

For the special case of no shunt impedance ($z_{33} = \infty$) and no voltage change between B_2 and B_3, we recover

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_2^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 + S_3 \end{bmatrix} \quad (22)$$

Assuming $S_i = V_i I_i^*$, we in fact recover the form given in (3), indicating that the new methodology is a generalization of the methodologies proposed in [6, 21], but accounts for shunt impedance and changes in voltage phase and angle between nodes.

The impedance between B_1 and B_2 remains unchanged, while the impedance between B_2 and B_3 is removed from the circuit.

2) Middle bus reduction through removal of Bus 2: If it is desired to remove B_2 from the circuit and only keep B_1 and B_3, we formulate the new impedance matrix by removing the rows and columns of Z_o corresponding to B_2. Solving (17) with the given values for the updated power vector yields

$$S_r = \begin{bmatrix} S_1^{new} \\ S_3^{new} \end{bmatrix} = \begin{bmatrix} S_1 + S_2 \times \frac{z_{23}}{z_{12}+z_{23}+\frac{z_{12} \times z_{13}}{z_{22}}} \frac{V_1}{V_2} \\ S_3 + S_2 \times \frac{z_{12}}{z_{12}+z_{23}+\frac{z_{12} \times z_{13}}{z_{22}}} \frac{V_3}{V_2} \end{bmatrix}. \quad (23)$$

By removing the middle bus, the power of the loads on both remaining buses are modified due to the aggregation of the power from the removed bus. As observed in end bus reduction, the aggregated power is a function of both the shunt impedance of the removed bus, and the voltage ratio between the buses.

Here the impedance between B_1 and B_3 takes the form of an equivalent impedance

$$Z_{13_{eq}} = (z_{12} + \frac{z_{12} \times z_{23}}{z_{22}} + z_{23}). \quad (24)$$

For the special case when there is no shunt impedance ($z_{22} = \infty$) and the voltage level is the same, we recover

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_3^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 + S_2 \times \frac{z_{23}}{z_{12}+z_{23}} \\ S_3 + S_2 \times \frac{z_{12}}{z_{12}+z_{23}} \end{bmatrix} \quad (25)$$

and

$$Z_{13_{\text{eq}}} = (z_{12} + z_{23}) \tag{26}$$

Assuming $S_i = V_i I_i^*$, we recover the exact form of (7) and (8).

B. Line and transformer

To illustrate the ability to reduce across simple transformers, a two-winding transformer is introduced connecting B_2 and B_3 (Fig. 2).

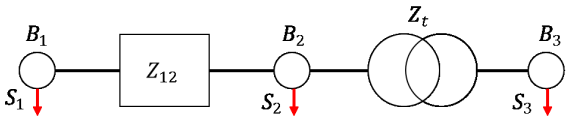

Fig. 2: Line model depicting a single phase 3 bus system connected by one line and one two-winding transformer with impedance Z_t.

The admittance matrix for the system with a transformer with voltage ratio $n = V_2/V_3$ is

$$\mathbf{Z}_o = \begin{bmatrix} \frac{1}{z_{11}} + \frac{1}{z_{12}} & -\frac{1}{z_{12}} & 0 \\ -\frac{1}{z_{12}} & \frac{1}{z_{12}} + \frac{1}{z_{22}} + \frac{1}{z_t} & -\frac{n}{z_t} \\ 0 & -\frac{n}{z_t} & \frac{n^2}{z_t} + \frac{1}{z_{33}} \end{bmatrix}^{-1}. \tag{27}$$

Removing the end bus removes the transformer from the circuit. The new power is

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_2^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 \\ S_2 + S_3 \frac{1}{1+\frac{z_t}{z_{33}}} \frac{1}{n} \frac{V_2}{V_3} \end{bmatrix}. \tag{28}$$

Removing the middle bus requires the line between B_1 and B_2 to be replaced with an equivalent transformer. The new powers are

$$S_r = \begin{bmatrix} S_1^{\text{new}} \\ S_3^{\text{new}} \end{bmatrix} = \begin{bmatrix} S_1 + S_2 \frac{z_{22} z_t}{z_{12} z_{22} + z_{12} z_t + z_{22} z_t} \frac{V_1}{V_2} \\ S_3 + S_2 \frac{n z_{12} z_{22}}{z_{12} z_{22} + z_{12} z_t + z_{22} z_t} \frac{V_3}{V_2} \end{bmatrix}. \tag{29}$$

The reduced admittance matrix becomes

$$\mathbf{Y}_r = \begin{bmatrix} z_{11_{eq}} + z_{t_{\text{eq}}} & -n z_{t_{\text{eq}}} \\ -n z_{t_{\text{eq}}} & z_{22_{\text{eq}}} + n^2 z_{t_{\text{eq}}} \end{bmatrix}, \tag{30}$$

where the subscript "eq" indicates an equivalent impedance composed of the original impedances. For this 3-bus system, the impedances are represented parametrically as:

$$Z_{11_{eq}} = \frac{z_{12} z_{22} + z_{11} z_t + z_{12} z_t + z_{22} z_t}{z_{11}(z_{12} z_{22} + z_{12} z_t + z_{22} * z_t)} \tag{31}$$

$$Z_{t_{\text{eq}}} = \frac{z_{22}}{z_{12} z_{22} + z_{12} z_t + z_{22} z_t} \tag{32}$$

$$Z_{22_{\text{eq}}} = \frac{n^2 z_{12} z_{33} + z_{12} z_{z22} + z_{12} z_t + z_{22} z_t}{z_{33}(z_{12} z_{22} + z_{12} z_t + z_{22} * z_t)} \tag{33}$$

The reduction logic is the same for more complex transformers (i.e. multiple winding, Δ-Y connections, split phase, etc...), however the form of $z_{t_{\text{eq}}}$ will differ.

V. Algorithm

A. Populate admittance, voltage, and power matrices

A circuit configuration is converted into an equivalent configuration for the reduced circuit as shown in Fig. 3. The feeder topology and CBs are determined as in [21].

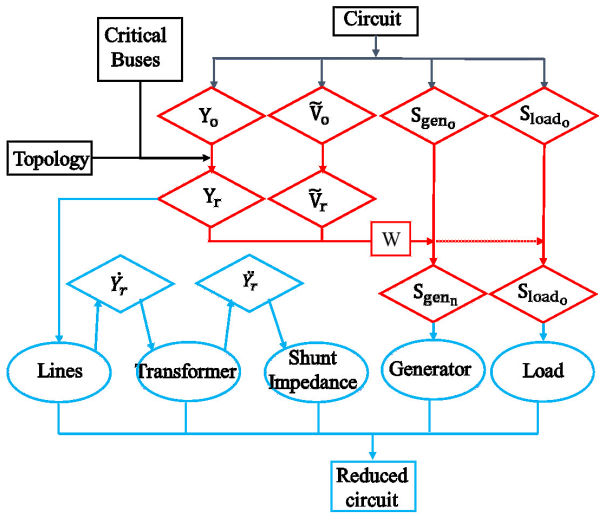

Fig. 3: Flowchart of the reduction algorithm. Colors show: (black) breakdown of the original model into its elementary parts; (red) Reduction of parts to equivalents; and (blue) building the reduced model from elementary parts.

An input file with feeder specifications is parsed and a circuit object is created that organizes the input data into the admittance matrix ($\mathbf{Y}_o \in \mathbb{C}^{M\times M}$), the complex base voltage vector ($\tilde{V}_o \in \mathbb{C}^{M\times 1}$), the load power ($\mathbf{S}_{o_{\text{load}}} \in \mathbb{C}^{M\times X}$), and the generation power ($\mathbf{S}_{o_{\text{gen}}} \in \mathbb{C}^{M\times X}$) matrices.

As described in Section III the matrix form of the powers are used to map different load model types. For a given load or generator on a bus i with model x, an entry in the power matrix for that element is given in S_o at row i, column x.

B. Reduce

First, the network is reduced by translating the nodal admittance matrix of the original feeder ($\mathbf{Y}_o \in \mathbb{C}^{M\times M}$) to an equivalent admittance matrix ($\mathbf{Y}_r \in \mathbb{C}^{m\times m}$) that describes the reduced circuit. This reduction is accomplished by calculating the impedance matrix for the full feeder ($\mathbf{Z}_o = \mathbf{Y}_o^{-1} \in \mathbb{C}^{M\times M}$) and removing all rows and columns not corresponding to CB to create the impedance matrix of the reduced feeder ($\mathbf{Z}_r \in \mathbb{C}^{m\times m}$). The reduced admittance matrix is then realized through inversion of the impedance matrix ($\mathbf{Y}_r = \mathbf{Z}_n^{-1} \in \mathbb{C}^{m\times m}$). The nominal voltages at the CB are equal to the voltages at the corresponding buses in the original feeder ($\tilde{V}_r = \tilde{V}_{o,\text{CB}}$). All other voltage entries are removed.

Second, incorporating the reduced network, the full network, and the voltage vectors, the weighting matrix $\mathbf{W}$ is found using (18). A matrix $\mathbf{S}_n \in \mathbb{C}^{m\times X}$ representing the load (or generation) powers on each node is found by multiplying $\mathbf{W}$ with the original power matrix $\mathbf{S}_o \in \mathbb{C}^{M\times X}$ (equation (17)).

C. Rebuild

In general, the power flow equations could be solved directly using the reduced admittance matrix and power vectors, and the rebuild step introduced below would be redundant. However, power flow solvers require specific input formats for the circuit. Thus translating the reduced matrices into a form that is representative of the new network, namely i) loads, ii) generators, iii) distribution lines, iv) transformers, and v) shunt impedance (including capacitors and reactors) improves the integration of the methodology with existing software.

Loads and generator power matrices, $\mathbf{S}$, are in order of the nodes, thus a load or generation object follows directly from the reduced power matrix. Rewriting the reduced network, on the other hand, is more challenging, as it requires analyzing the new feeder topology and nodal admittance matrix $\mathbf{Y}_r$. The admittance matrix is sparse and convoluted. For a bus i connected to a bus j, the terms $\mathbf{Y}_{ij}$ can represent the admittance between the two buses contributed from a distribution line or a transformer (or both) for different phases. The terms $\mathbf{Y}_{ii}$ represent both the shunt connected admittances as well as the impact of the connection between bus i and bus j; see (20) and (27). We follow the procedure below:

1) Distribution Lines: For a bus i, all connected downstream buses are identified. For the p-phase connection between bus i with nodes I and downstream bus j with nodes J, the impedance, $\mathbf{z} \in \mathbb{C}^{p\times p}$, between the buses is given by $\mathbf{z}_{IJ} = \mathbf{Y}_{IJ}^{-1}$. The corresponding resistance and reactance of the lines are then expressed as the real and imaginary parts of the matrix, respectively. The length of the line is calculated by the difference between the distances of bus i and j from the substation, as identified in the initial topology detection. The full network is developed by repeating the process above for each downstream bus and for each bus i. This process is summarized in **Algorithm 1**.

Algorithm 1 Retrieve lines from Y_r

```
Given Y_r
for bus i ∈ CB do
    Identify node set I that corresponds to bus i
    Identify any bus connected downstream to bus i to form
    the neighbor set N_i.
    for any bus j in N_i do
        Identify node set J that correspond to bus j
        if V_I=V_J then
            Find line impedance: z_line = Y_IJ^{-1}
            Find line length: L_ij = L_1i − L_1j
            Write line between bus i and bus j
        end if
    end for
end for
Calculate Y_L, admittance matrix of only line network
Subtract lines from Y_r: Ẏ_r = Y_r − Y_L
```

2) Transformers: In the new feeder, a transformer is needed to connect CB at different voltage levels, generally replicating reduced nearby transformers in the original circuit. For when both buses adjacent to a transformer are removed, the transformer is removed from the circuit, akin to the distribution lines. However, reduction then results in adjacent CB with different voltage bases (i.e. a CB on the primary side adjacent to one on the secondary side of the feeder). A new transformer composed of the aggregate impedance between the two buses must be created.

To isolate just the transformer, distribution lines are removed from $\mathbf{Y}_r$, resulting in a new matrix $\dot{\mathbf{Y}}_r$. The impedance of the transformer found in $\dot{\mathbf{Y}}_r$ depends on both the number of windings w, the phases p, and the connection type (i.e $\Delta-\Delta$, $\Delta-Y$, etc..). In general, however, a transformer connected between a bus i and j is comprised of the entries of $[\mathbf{Y}_{ii}, \mathbf{Y}_{ij}, \mathbf{Y}_{ji}, \mathbf{Y}_{jj}] \in \mathbb{C}^{p\times p}$. A connection detection algorithm is employed to determine the connection type of the transformer. The reconstruction of transformers is summarized in **Algorithm 2**.

3) Shunt Impedance: In the admittance matrix, the term $\mathbf{Y}_{ii} \in \mathbb{C}^{p\times p}$ of a bus i is composed of the shunt impedance on the bus as well as the contribution of connected buses

$$\mathbf{Y}_{ii} = 1/\mathbf{z}_{ii} + \Sigma_{j=1}^{J} 1/\mathbf{z}_{ij}, \tag{34}$$

where J is the number of buses connected to bus i. The connection admittance between each bus i and j (i.e. $Y_{ij} \in \mathbb{C}^{p\times p}$) is represented by,

$$\mathbf{Y}_{ij} = -1/\mathbf{z}_{ij} \tag{35}$$

Thus, the shunt impedance on bus i ($\mathbf{z}_{ii}$) can be calculated as,

$$\mathbf{z}_{ii} = \frac{1}{\mathbf{Y}_{ii} + \Sigma_{j=1}^{J} \mathbf{Y}_{ij}} \tag{36}$$

which is effectively accomplished through admittance matrix subtraction ($\ddot{\mathbf{Y}}_r$), leaving just the shunt terms. See **algorithm 3**.

Algorithm 2 Retrieve Transformers from Y_r

```
Given Ẏ_r
for bus i ∈ CB do
    Identify node set I that corresponds to bus i
    Identify any bus connected downstream to bus i in the
    neighbor set N_i.
    for any bus j in N_i do
        Identify node set J that correspond to bus j
        if V_I ≠ V_J then
            Find z_t = [ Y_II^{-1}   −Y_IJ^{-1} ]
                       [ −Y_JI^{-1}   Y_JJ^{-1} ]
            Identify connection type (i.e. Δ − Δ, etc...)
            Transform z_t to winding impedance (see [24])
            Write transformer between i and j
        end if
    end for
end for
Calculate Y_Tr, admittance matrix of only transformer net-
work:
Subtract transformers from Ẏ_r: Ÿ_r = Ẏ_r − Y_Tr
```

Algorithm 3 Retrieve shunt impedance from $\ddot{\mathbf{Y}}_r$

Given $\ddot{\mathbf{Y}}_r$
for bus $i \in$ CB **do**
  Identify node set I that correspond to bus i
  Find shunt impedance: $\mathbf{z}_{\text{shunt}} = \mathbf{Y}_{II}^{-1}$
  Write shunt component
end for

VI. VALIDATION

A. Strategy

The error due to reduction was detailed extensively for a single feeder in [21], where the error was most correlated with bus distance from substation, the number of buses removed, and net load on the bus. The new methodology shows the same trends for most feeders.

However, given the flexibility of the methodology proposed in this paper, the dependence of the error on feeder size, topology, and modeling complexity can also be assessed.

First, we validate the method by comparing results on the feeder examined in [21], referred to here as "UCSD A". Next, we examine the voltage error and savings in computing time on six disparate and publicly available feeder models: EPRI 5 and 7* [25], EPRI K1, J1, M1 [26], and IEEE 8500 [27]. The feeder models are summarized in Table I. In the EPRI 7* model load is aggregated at the feederhead as allocation factors were not considered in our algorithm.

Results are first shown for a snapshot simulation (not a time series). Loads and generators are assumed to operate at full capacity. The effect of error due to changing load conditions is considered further in sections VI-D and VI-E.

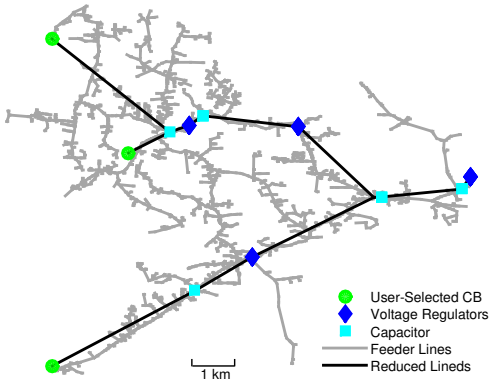

Fig. 4: IEEE 8500 test feeder (grey) and reduced equivalent (black) for three critical buses that were selected to be in areas where voltage extremes are expected.

As in [21], OpenDSS [20] is used to solve the power flow for both the original and reduced circuit. The error from reduction is defined as the difference in nodal voltage for the node in the power flow of the original circuit and in the reduced circuit. All simulations are run with a voltage convergence tolerance of 1×10^{-6} V pu, which is one order of magnitude lower than the voltage error for most simulations.

B. Comparison to reduction in [21] on feeder UCSD A

Comparing to the reduction maximum voltage error from reference [21] of $\mathcal{O}(10^{-3})$, the inversion reduction has

TABLE I: Characteristics of the 7 feeders investigated.

Feeder	Nodes	Length [km]	Model complexity
UCSD A	1302	4.3	Only one voltage level
K1	1751	7.1	Large distributed capacitor bank
EPRI 7*	2452	4.1	Aggregated load at feeder head
M1	3153	3.5	High shunt capacitance
EPRI 5	3437	5.2	Low complexity model
J1	4245	18.1	Large PV system at feeder end
IEEE 8500	8531	18.2	Extremely detailed transformers

$\mathcal{O}(10^{-5})$ error, which is negligible for practical applications (Fig. 5). As the UCSD A feeder does not include the secondary side (no transformers), the reduction in error can be attributed to the other improvements in the algorithm compared to [21] such as the inclusion of shunt capacitance in the reduction model, a more comprehensive circuit reconstruction which considers shunt impedances, the reduction of loads assuming fixed power models (versus fixed current in [6, 21]), and mapping of individual load models.

Counter-intuitively, when no buses are removed the error is non-zero. This is due to the implementation of the power flow solver, i.e. differences in how the feeder is originally modeled and how the algorithm represents it using simplified elements. If power flow was only based on the new admittance matrix and power vectors, the error should be zero.

The time required to reduce the circuit is also less for the inversion reduction (Fig. 6). This is expected, as the inversion reduction is based on Gaussian elimination, as opposed to a recursive method. In both methods the inclusion of more CB in the reduction increases the reduction time. In the inversion method, more CB increase the size of the system inversion during reduction (see (17)), whereas [21] loops through more buses.

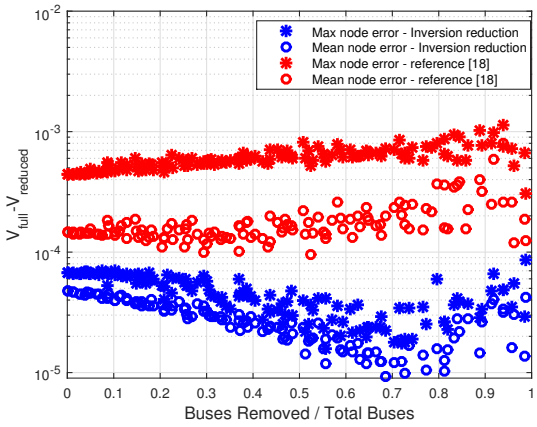

Fig. 5: Comparison of voltage error (maximum and average of all nodes) when reducing the UCSD A feeder with the recursive methodology proposed in reference [21] against the inversion reduction proposed in this work.

C. Snapshot validation on seven feeders

As observed in Fig. 7, the maximum errors for any feeder (the worst case) never exceed 0.008 pu. The greatest errors occur for the two largest feeders J1 [26] and IEEE 8500 [27]. The error is non-zero again for zero buses removed, for the reasons discussed previously. The lowest error occurs in the EPRI 7* feeder [25], where the maximum error actually decreases with increasing buses removed. The EPRI 7 error is smaller since all loads are at the feeder head, thus there is no movement of load from reduction. Since the reduction

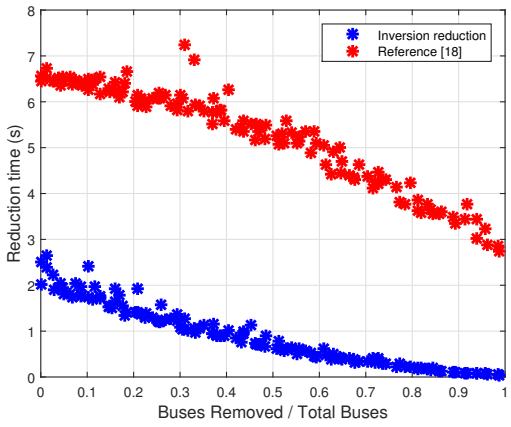

Fig. 6: Comparison of computational time for reducing the UCSD A feeder with the methodology proposed in reference [21] against the inversion reduction. Simulations are run on a desktop with Intel(R) Core(TM) i7-4770 processor with 32 GB RAM.

produces simplified representations of detailed models, the error due to mis-representation of elements is reduced as more buses are removed (i.e. translating back to commercial software). Although not shown here for brevity, the mean error for each feeder follows the same trend with number of buses removed but is generally one order of magnitude smaller, with the exception of EPRI 7 where the mean error is nearly identical to the maximum error. In general, longer feeders tend to have larger error, which is consistent with the findings in [21] where error increased with node distance from the substation.

Reduction time increases with the number of nodes in the original circuit (not shown), and decreases as more buses are removed (Fig. 8) consistent with [21] and the previous section.

Relative power flow time savings (Fig. 8) for the reduced feeder are independent of feeder model. Since power flow computational cost is proportional to feeder size, reducing a certain percentage of buses reduce simulation time by a similar amount. Specifically, decrease in simulation time is linear with number of buses removed, where n buses removed results in roughly $2n$ time savings. For a single user-selected CB, the power flow time savings for all feeders exceed 99%.

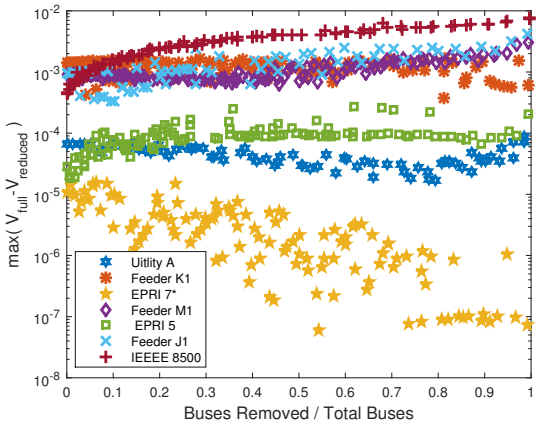

Fig. 7: Maximum error as a function of the number of buses removed for seven feeders. The y-axis is logarithmic and represents the maximum difference between all node voltages between the reduced and the full feeder.

D. Timeseries validation on the UCSD A feeder

To examine the effect of changing load and time dependent devices, a quasi-static time series (QSTS) simulation was

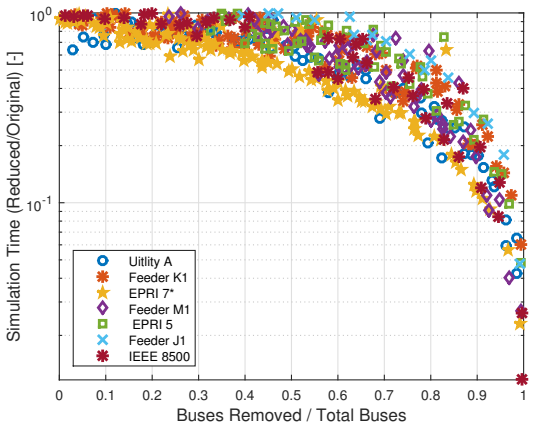

Fig. 8: The ratio of snapshot simulation time for the reduced circuit to the original circuit as a function of buses removed from the circuit for all feeders. Note, the trend would be linear if the Y axis was linear.

performed on the UCSD A feeder for 11/21/2016 at a time step of 30 s in OpenDSS. The day was chosen due to the large variation between maximum and minimum load as well as the variable solar irradiance due to partly cloud conditions. Similar to [21], each load operates under the same time-series shape scaled by its power rating, while each PV time-series is uniquely determined using a sky imager [28]. The aggregate demand, solar generation, and net demand profiles are given in Fig. 9.

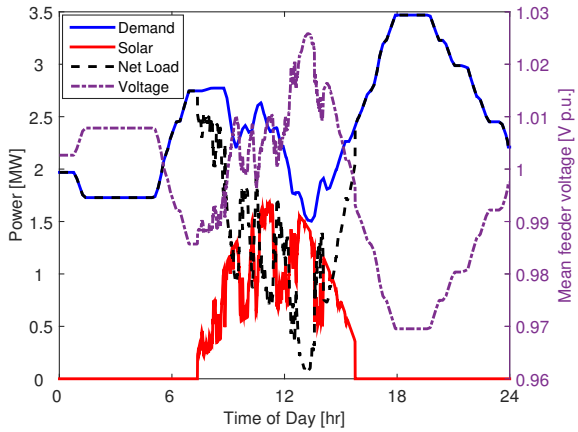

Fig. 9: (left) Time series for aggregate demand, generation, and substation net demand. (right) The mean feeder voltage over the day.

QSTS simulations were run for reduced feeders with varying number of critical buses (CBs) removed in increments of 5% To remove the dependence of error on CB location, five simulations were run for each CB ratio and the CB were selected at random. The time series of the maximum voltage difference between nodes in the reduced and original circuits are plotted as a function of the number of buses removed in Fig. 10. Error changes are small through out the day ($\mathcal{O}10^{-5}$) and follow the loading conditions (see Fig. 9). Larger variations ($\mathcal{O}10^{-4}$) occur with the number of buses removed from the circuit. For less than 85% of buses removed the error due to changing load is negligible, and error remains nearly constant throughout the QSTS. Given the low error, tap operations are identical between original and reduced QSTS for all reduction scenarios (not shown).

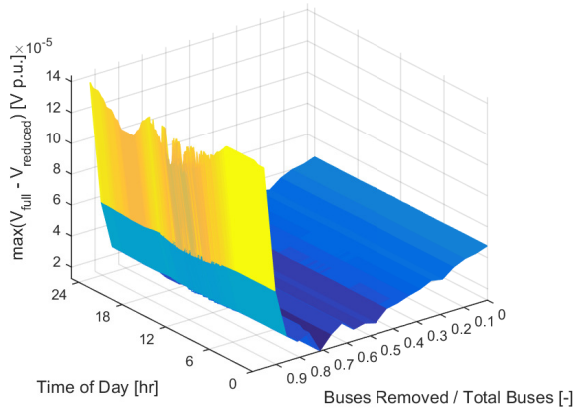

Fig. 10: Three dimensional representation of maximum voltage error due to reduction as a function of the time of day (loading condition) and number of buses removed.

Isolating the effect of changing load conditions (Fig. 11), it is observed that during periods of no solar generation (i.e. morning and evening) the maximum error varies little and monotonically decreases with increasing load. During periods of solar generation, the maximum error is variable, but generally is observed to decrease with increasing solar generation.

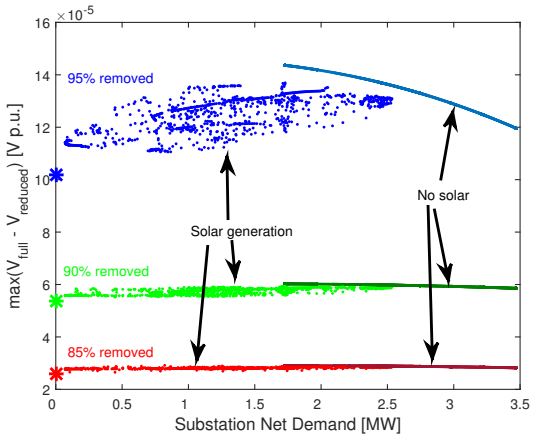

Fig. 11: Maximum voltage error due to reduction as a function of substation net load. Brighter colors indicate periods when solar generation is present, while matte colors indicate periods with zero solar generation. Errors are shown for three ratio of buses removed. The snapshot solution error is given on the left axis as stars for each ratio of buses removed for comparison.

E. Error due to choice of $\tilde{V}$

As discussed in section III, the reduction equation (Eq. (17)) can be run with either voltages obtained from a power flow solution or using the nominal nodal voltages. The validations presented thus far used nominal voltage vectors (to avoid the computational expense to run the powerflow). To examine the effect of using the power flow voltages voltage as input to the reduction, a fixed set of 5%, 10%, and 15% of CBs were simulated for the day using voltages from the snapshot solution (full loading and generation).

The choice of voltage vector has the greatest effect during the middle of the day when solar generators are producing (see Fig. 12), while for periods without solar generation there is no difference in error. The error only differ due to solar generation since the same load profile is used for each load, where a different profile is used for each solar generator. Given that an aggregate PV is created at each node, the combined solar profile is a mismatch representing the average of many geographical dispersed profiles. This error can be reduced by considering individual PV profiles at each node, as is proposed in [23]. For all scenarios of bus removal, the error increases with increasing PV generation when the powerflow voltage is used. Further, the reduction in error due to less buses being removed is more gradual for the powerflow solution. However as observed in Fig. 11, for 85% of buses removed, the error only weakly depends on changes in loading and generation.

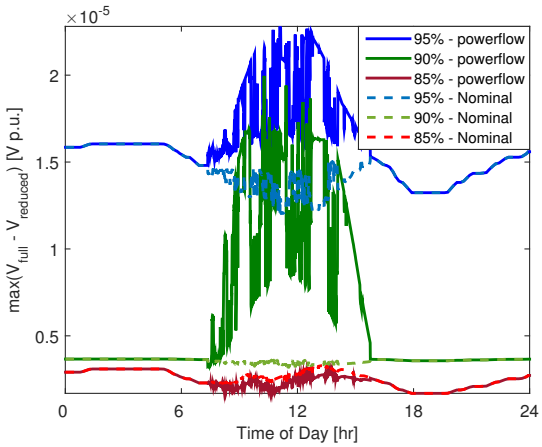

Fig. 12: Maximum voltage error for the time series for 85%, 90%, and 95% of the buses removed when the reduction is carried out using the (dashed lines) nominal nodal voltage and (solid lines) the powerflow solved voltage for the stationary point of full loading.

VII. Conclusions

A novel and general feeder reduction methodology based on Gaussian elimination, known as the inversion reduction method is proposed. The method is specifically designed to handle all of the complexities of distribution feeder models, including unbalance in loading, large shunt capacitance, and unique transformer configurations. The method is derived from first principles. A simple illustrative example demonstrates that the methodology is a generalization of the methodology proposed previously by the authors. Algorithmic details are provided.

The inversion reduction is compared against the previously proposed methodology on the same feeder and shown to be superior in both error and the speed of reduction. The methodology is then demonstrated on 6 additional feeders varying in topology, size, and modeling complexity. The maximum voltage error is small regardless of feeder size or complexity (< 0.008 p.u.). Finally, the methodology is tested on a single feeder using a day QSTS simulation, where it s shown that under changing load conditions the reduction produces least error near the linearization point, but error increases away from the linearization point. However, this effect is small for less than 85% of buses removed.

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