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Near surface defects: Cause of deficit between internal and external open-circuit voltage in solar cells

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Abstract

Interface recombination in a complex multilayered thin-film solar structure causes a disparity between the internal open-circuit voltage ($V_{OC,in}$), measured by photo-luminescence, and the external open-circuit voltage ($V_{OC,ex}$), that is, a V_{OC} deficit. Aspirations to reach higher $V_{OC,ex}$ values require a comprehensive knowledge of the connection between V_{OC} deficit and interface recombination. Here, a near-surface defect model is developed for copper indium di-selenide solar cells grown under Cu-excess conditions. These cell show the typical signatures of interface recombination: a strong disparity between $V_{OC,in}$ and $V_{OC,ex}$, and extrapolation of the temperature dependent $q \cdot V_{OC,ex}$ to a value below the bandgap energy. Yet, these cells do not suffer from reduced interface bandgap or from Fermi-level pinning. The model presented is based on experimental analysis of admittance and deep-level transient spectroscopy, which show the signature of an acceptor defect. Numerical simulations using the near-surface defects model show the signatures of interface recombination without the need for a reduced interface bandgap or Fermi-level pinning. These findings demonstrate that the $V_{OC,in}$ measurements alone can be inconclusive and might conceal the information on interface recombination pathways, establishing the need for complementary techniques like temperature dependent current–voltage measurements to identify the cause of interface recombination in the devices.

KEYWORDS
buffer layer, deep acceptor, defective layer, quasi-Fermi-level splitting, solar cell

1 | INTRODUCTION

Open-circuit voltage (V_{OC}), a key factor for the efficiency of a solar cell, is measured by either electrical or optical techniques. Electrical measurements, particularly current–voltage measurements give the measure of external open-circuit voltage ($V_{OC,ex}$) of a device, whereas optical measurements particularly calibrated photoluminescence

(PL) provide the measure of the internal open-circuit voltage ($V_{OC,in}$) or quasi-Fermi-level splitting (qFLs). The $V_{OC,in}$ (qFLs) is calculated from the ratio of total radiative recombination flux of the device to the flux of injected photons. It is generally measured via one sun calibrated PL measurement (in order to compare it to AM 1.5 G illuminated solar cell $V_{OC,ex}$) and translates to the energetic difference between the hole quasi-Fermi level (F_h) and electron quasi-Fermi level

(F_e) in the bulk.[1] Moreover, $V_{OC,in}$ provides a direct measure of the bulk quality of an absorber, while the $V_{OC,ex}$ measured in a current–voltage (I-V) measurement under one sun illumination is the energetic difference between the F_h at the hole contact and the F_e at the electron contact. The $V_{OC,ex}$ takes into account the interfaces and contacts as well and is a device related parameter. Hence, $V_{OC,ex}$ is a metric that represents the overall quality of the device. In order to translate optical quality of the absorber into electrical efficiency, that is, $V_{OC,ex}$, it is essential to have a uniform qFLs throughout the device structure.[2–4]

Thin films solar cells are complex multilayer structures consisting of many layers, namely, absorber, charge transport layer, etc., each of which individually affects the qFLs and could be a source of a gradient in qFLs. This often leads to a deficit between internal and external V_{OC}, that is, $V_{OC,in}–V_{OC,ex}$. The deficit can be observed in thin film solar cells such as Cu(In,Ga)(Se,S)$_2$,[5,6] CdTe,[7] and perovskite[4,8,9] and is associated to interface recombination in the device.[4,9–13] Identifying the source of interface recombination and the underlying qFLs gradient is crucial for achieving higher efficiency in these devices and enabling better understanding of device physics. The mismatch of the energy bands at interface between absorber and charge transport layer[4,14,15] and Fermi-level pinning are the two commonly evoked models to explain why and more so, in which case interface recombination dominates.[16–19]

Researchers employ qFLs measurements for quantifying interface recombination and determining the quality of surface passivation after charge transport layer deposition or post-deposition treatment (PDT).[4,20] Though qFLs measurements provide significant information regarding non-radiative recombination in the bulk, it fails to capture the details of interface processes especially in devices dominated by interface recombination.[21] The PL intensity increases exponentially with the qFLs. Thus, in the case of a qFLs gradient, PL will always detect the highest qFLs and will not indicate the gradient.[15] Therefore, temperature-dependent $V_{OC,ex}$ measurements are required to unravel the presence of interface recombination in the device and thus provide necessary information to understand the full extent of the non-radiative interface recombination losses in the device.[22]

Here, with the help of copper indium diselenide (CISe), a chalcogenide photovoltaic absorber material, we develop a comprehensive model for understanding the interface V_{OC} deficit by probing the effect of near-surface defects on $V_{OC,in}$ and $V_{OC,ex}$ of the CISe device. We choose CISe for studying the interface V_{OC} deficit, because CISe absorbers grown under Cu-excess conditions (addressed as Cu-rich throughout this work with as grown stoichiometry [Cu]/[In] > 1) and under In-excess (addressed as Cu-poor with as grown stoichiometry [Cu]/[In] < 1) growth conditions result in similar $V_{OC,in}$ with completely different $V_{OC,ex}$ and therefore different interface V_{OC} deficit.[10,23,24] Moreover, instead of the commonly used Cu(In,Ga)Se$_2$ compounds that have bandgap-graded absorber layers,[25] the ternary CISe compound allows to reduce the amount of free variables and redundant complexity in our model. This makes CISe an ideal case study to investigate the cause of the interface V_{OC} deficit in thin film solar cells.

We vary the interface defect density by treating Cu-rich absorbers with different solutions namely, aqueous KCN, aqueous bromine (Br$_{aq.}$), aqueous zinc (Zn$_{aq.}$), sulfur (S), and cadmium

(Cd) solution, as well as by depositing a Zn(O,S) buffer. With the help of admittance spectroscopy (AS), deep-level transient spectroscopy (DLTS), and temperature-dependent current–voltage (I-V-T) measurements, we probe the impact of these treatments. The study identifies the role of defects near (not at) the interface, which was hitherto not discussed. Furthermore, we scrutinize the limitations of $V_{OC,in}$ (qFLs) measurements alone in characterizing interface recombination and the necessity of temperature-dependent $V_{OC,ex}$ measurements. Using numerical modeling, we establish a model based on strong subsurface defects, which demonstrates an interface V_{OC} deficit for an interface with favorable band alignment and no Fermi-level pinning. The model is experimentally endorsed and provides insights on the origin and nature of these subsurface defects in CISe solar cells.

1.1 | Experimental observations of Cu-rich versus Cu-poor CISe solar cell

Before building a comprehensive model, it is necessary to look at the optical and electrical characteristics of CISe solar cells prepared using absorbers grown under Cu-rich and Cu-poor growth conditions. Throughout this work $V_{OC,in}$ will be used to define the qFLs, and the deficit between $V_{OC,in}$ and $V_{OC,ex}$ will be referred to as interface V_{OC} deficit, unless stated otherwise. Figure 1A shows typical I-V characteristics of Cu-rich and Cu-poor devices. Both devices are processed in a similar manner, that is, with same buffer (CdS) and window layer (i-ZnO + AZO), deposited with identical process parameters. The Cu-rich device exhibits a lower $V_{OC,ex}$ compared with Cu-poor device, even though absorbers have almost the same $V_{OC,in}$ (table in Figure 1B). The $V_{OC,in}$ is measured with the help of calibrated PL measurements that were performed using our own lab-built system with continuous wave 663-nm diode laser as an excitation source. For extracting $V_{OC,in}$, samples covered with buffer layer on top are illuminated with laser, and PL is measured. Intensity and spectral corrections are then applied to the raw data to determine $V_{OC,in}$; the entire procedure details can be found in reports.[23,26] An exemplary PL spectrum is presented in Figure S1A. As a consequence, Cu-rich devices suffer from a high interface V_{OC} deficit ($\sim$130 mV), similar to previous data on Cu(In,Ga)Se$_2$.[23] This is significantly higher than the one in Cu-poor device ($\sim$20 mV) or in fully optimized devices ($\sim$10 mV).[27] This interface V_{OC} deficit is clearly associated to interface recombination being the dominant recombination path in the device as revealed from $V_{OC,ex}$ measurements at different temperatures (Figure 1C). The activation energy (E_a) of the saturation current density is obtained from extrapolation of $V_{OC,ex}$ to 0 K.[19] For Cu-rich devices, E_a is always lower than the bulk bandgap (E_G) and is associated to the presence of deep interface defects[28,29] whereas, in Cu-poor devices E_a extrapolates to the E_G and hence, interface recombination does not limit $V_{OC,ex}$. Furthermore, an "S shape" in the first quadrant is observed at lower temperatures in Cu-rich devices, which is not present in Cu-poor device (Figure 1D). This roll-over in the first quadrant indicates a barrier for the forward current.[30] A problematic interface property often leads to an S shape in the fourth quadrant, which indicates an extraction barrier for the photocurrent.[31]
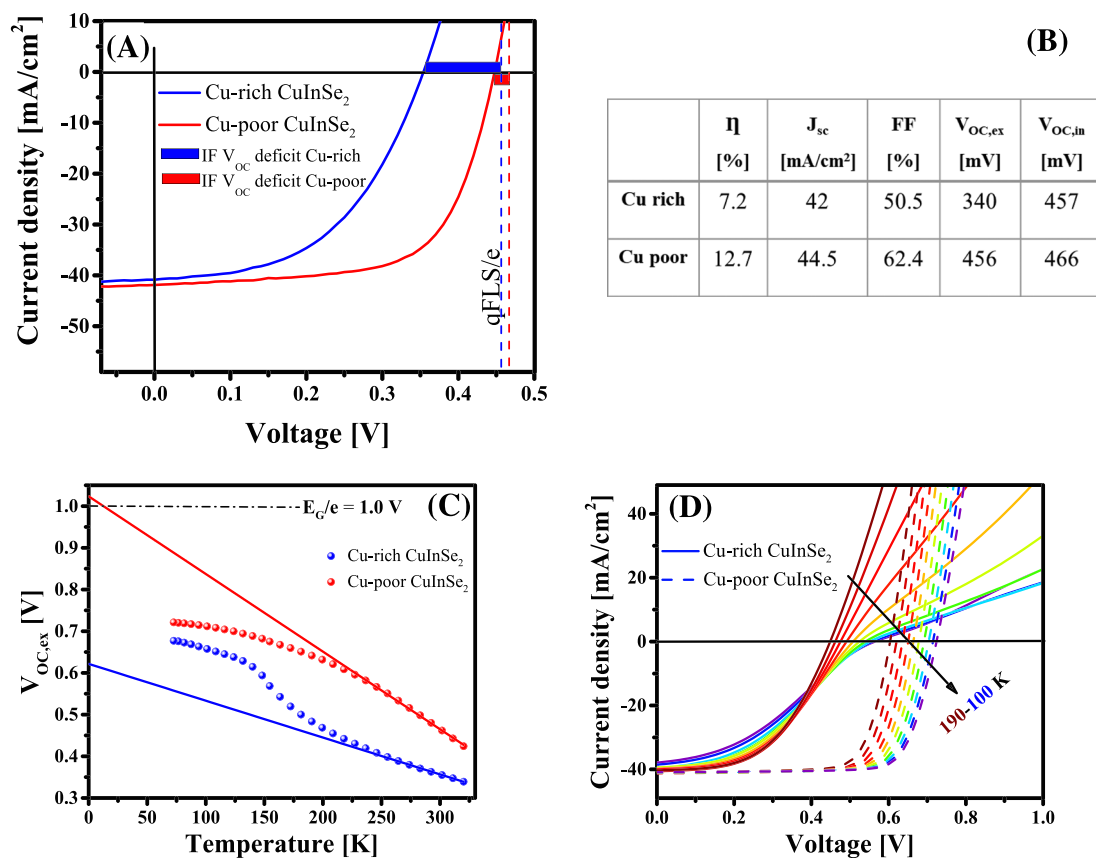
FIGURE 1 Comparison of Cu-rich versus Cu-poor copper indium diselenide (CISe) device (A) and (B) current–voltage (I-V) curve and characteristics. The comparison of $V_{OC,ex}$ and $V_{OC,in}$ shows a high interface V_{OC} deficit for Cu-rich devices. The blue and the red bar show the interface V_{OC} deficit for Cu-rich and Cu-poor device. (C) $V_{OC,ex}$ as a function of temperature, extrapolation to 0-K activation energy of saturation current density (D) I-V as a function of temperature, a "S shape" at lower temperatures is observed in Cu-rich devices [Colour figure can be viewed at wileyonlinelibrary.com]

In summary: the Cu-rich CuInSe$_2$ solar cells show the typical signatures of interface recombination: an extrapolation of $q \cdot V_{OC,ex}$ to 0 K that is smaller than the bandgap energy and a strong reduction of $V_{OC,ex}$ with respect to $V_{OC,in}$. However, the bandgap of Cu-rich and of Cu-poor material is essentially the same, and it has been shown many times that CdS forms a favorable band alignment with CuInSe$_2$.[32] On the other hand, if Fermi-level pinning was the dominant mechanism, a diode factor near 1 would be expected,[33] whereas, in general, we observe diode factors near 2 for Cu-rich CuInSe$_2$.[34] Thus, an alternative model is needed to explain the observed behavior. This model will be valid only if it can successfully reproduce the three observations made for Cu-rich devices: (i) a large interface V_{OC} deficit, (ii) an E_a of the saturation current smaller than the E_G, and (iii) a "S shape" in only the first quadrant. However, to build a reliable model, we will first probe the characteristics of the deep defect that has been speculated to be the cause of all these issues in Cu-rich CuInSe$_2$.[35]

1.2 | Origin and characteristics of the deep defects

Despite its superior morphological and optoelectronic properties, the device performance of CISe absorbers grown under Cu-rich conditions is inferior to its Cu-poor counterpart.[11] This is due to the necessary KCN etching step required to remove the secondary Cu$_{2-x}$Se phase. The etching results in high concentration $>10^{16}$ cm^{-3} of deep near-interface defects ($\sim$200 meV) in Cu-rich CISe absorbers.[35,36] The defects are termed as near-interface as AS performed at different DC applied voltage does not yield a voltage-dependent defect activation energy, which would be typical for interface defects (see Figure S1B,C). However, it is unknown whether the defect originates specifically from the KCN etching or from the etching process of secondary phase independent of the etchant used. To investigate this, Cu-rich CISe solar cells are prepared using two different etching solutions: 10% aqueous KCN solution (for reference) and 0.16% mM aqueous Br solution. The impact of etching on the defect structure is investigated by measuring AS. Figure 2A shows exemplary AS measurements for KCN etched Cu-rich CISe solar cell. The spectra exhibit a capacitance step in the temperature range of 190–100 K. The corresponding frequency derivatives of the AS spectra demonstrate broad asymmetric peaks (Figure 2B). These broad peaks are a peculiar feature always present in the AS spectra corresponding to the $\sim$200 meV defect.[35] In comparison, the AS of aqueous Br-etched Cu-rich CISe solar cell also exhibits a similar capacitance step (dotted lines in Figure 2A,B). More importantly, the inflection frequencies of
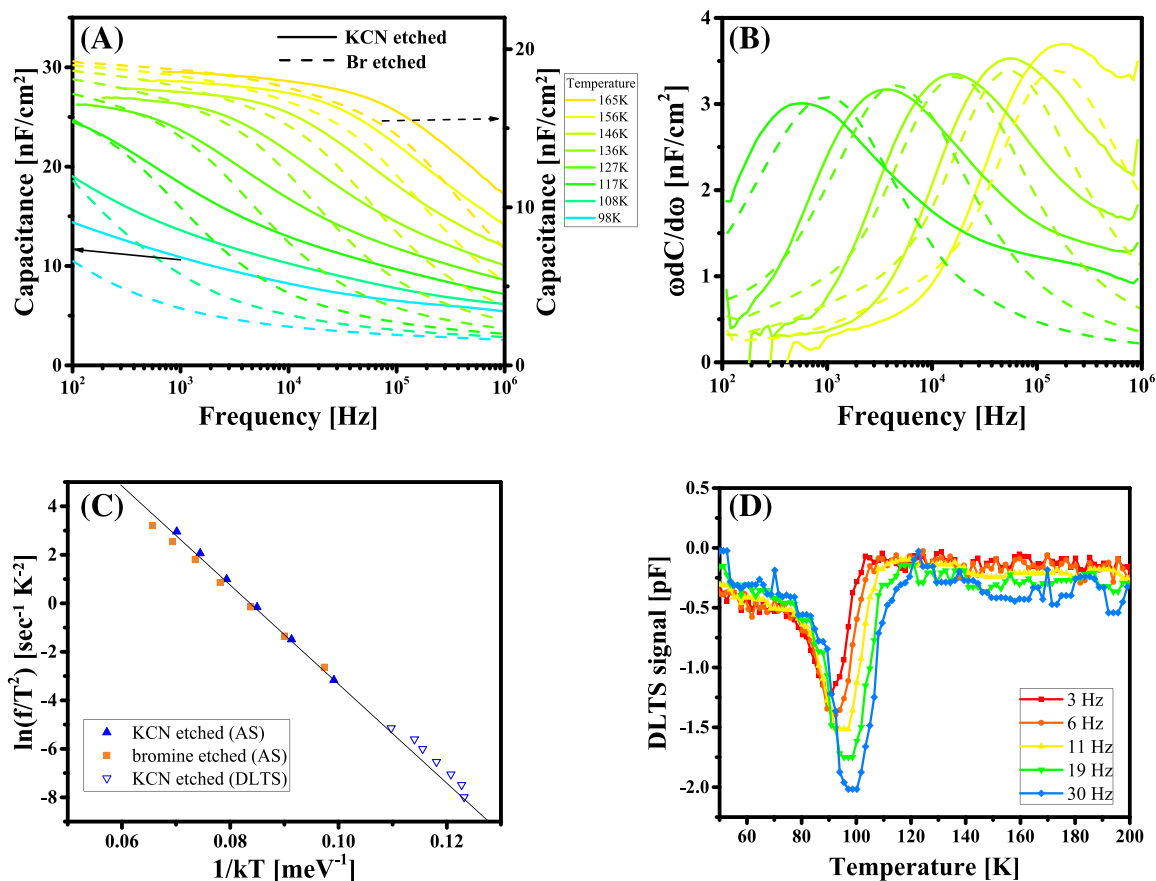
FIGURE 2 (A) Admittance spectra of Cu-rich copper indium diselenide (CISe) solar cell prepared from absorbers etched with KCN and bromine solution. Please note different *y*-axis for the KCN etched (right *y*-axis) and Br etched (left *y*-axis) devices. (B) $\omega dC/d\omega$ plot of corresponding admittance spectra, the peaks are broad and asymmetric. (C) Arrhenius plot of measured admittance (closed symbols) and deep-level transient spectroscopy (DLTS) (open symbols) measurements of CISe Schottky junction devices prepared with KCN etched and with bromine etched absorbers. (D) DLTS signals of the KCN etched CISe Schottky junction device [Colour figure can be viewed at wileyonlinelibrary.com]

AS of this device plotted together with that of the KCN-etched device in an Arrhenius plot lie very close to each other, with activation energies around 200 meV. This indicates presence of a similar capacitance response in both the devices. In supplement to these results, a device prepared from a Br-etched absorber also has the same E_a of the saturation current as the KCN etched device, significantly lower than E_G (Figure S2A), signifying the presence of prevailing interface recombination. Thus, both results, the presence of similar capacitance step with a similar activation energy and the presence of interface recombinations, confirm the existence of the deep defect independent of the etchant used to remove the $Cu_{2-x}Se$ phase. This suggests that the ~200-meV defect is an intrinsic defect originating from the removal of the secondary phase from Cu-rich CISe films, as suggested in the literature.[37]

Although AS provides the defect activation energy, it does not yield the defect nature. Therefore, to investigate whether the defect is acceptor or donor in nature, DLTS is measured on KCN etched CISe Schottky devices (Figure 2C). For the measurement, the device was kept at −1-V bias followed by a +1-V voltage pulse, and the

capacitance transient was measured. Figure 2D shows the DLTS results for a chosen rate window alongside with the corresponding Arrhenius plot in Figure 2C. The peak in the DLTS spectrum is negative, which is a fingerprint of emission of majority carriers from a trap. Further, the activation energy of the corresponding signal is similar to the one observed in AS. The DLTS data points in the Arrhenius plot continue the admittance data, suggesting that it is the same signal as the one observed in AS. These results are in accordance with our earlier observations, where a reduction in apparent doping was observed after passivation of the ~200-meV defect,[5,35] and confirm our speculation of the ~200-meV defect being acceptor in nature.

Earlier work has established the presence of deep defects in CISe solar cells,[35] be passivated with mild surface chalcogen treatments and buffer layers with high sulfur concentration in the deposition process.[28,35,38] Particularly interesting point is that these buffer layers, that is, CdS and Zn(O,S), are deposited via chemical bath at low temperature (<85°C), whereas the chalcogen treatment is done at higher temperatures (>300°C).[35] This suggests that the defect is present at or near the surface within few tens of nanometers. To explore this

possibility and rule out the properties of buffer layer as a viable cause for the disappearance of defect signature in AS, three PDTs are performed. For the PDTs, KCN-etched Cu-rich CISe absorbers were immersed into three separate solutions: ammoniac solution of $ZnSO_4$ (Zn-PDT), ammoniac solution of $CdSO_4$ (Cd-PDT), and ammoniac solution of CH_4N_2S (S-PDT), each at 80°C for 10 min. These absorbers were made into Schottky device, and then AS was performed.

Figure 3A gives the summary of the defect energies obtained after the three PDTs along with the values obtained after CdS and Zn(O,S) buffer deposition. For the PDT samples, a reduction in the defect activation energy is used as an indirect indicator for passivation the deep defect. This is because the samples that displayed a reduction in defect energy after different PDTs also display an improvement in $V_{OC,ex}$ (see Figure S2B) and consequently in the interface V_{OC} deficit, which signifies passivation of deep defects. Among the three PDTs, Zn-PDT leads to a complete passivation of the defect, confirmed by the significant reduction in the activation energy of the

capacitance step. The respective energies of 77 and 120 meV obtained after the Zn(O,S) buffer and Zn-PDT can be attributed to the A2 (60 meV) and A3 (135 meV) acceptor in $CuInSe_2$, respectively,[39,40] whereas S-PDT results in partial passivation, as it exhibits still the signature of a deep defect in the AS (Figure 3B) with activation energy ~170 meV. It has been speculated that the broadness of the 200-meV peak originates from contribution of two defects 200 ± 20-meV defect and 130 ± 10-meV defect.[35] And passivation of the 200-meV defect in the device leads to a decrease in activation energy of capacitance step in AS. In case of complete passivation, the defect with energy 130 meV remains; however, in case of partial passivation, an activation energy between 130 and 200 meV is obtained. For the S-PDT device particularly, the frequency derivative of AS (Figure 3C) displays broad peaks a feature similar to the un-passivated samples. Also, the main capacitance step in admittance spectra starts to bifurcate into two steps (response "a" and "b" in Figure 3B) at low temperatures (<130 K), which might be due to presence of two different
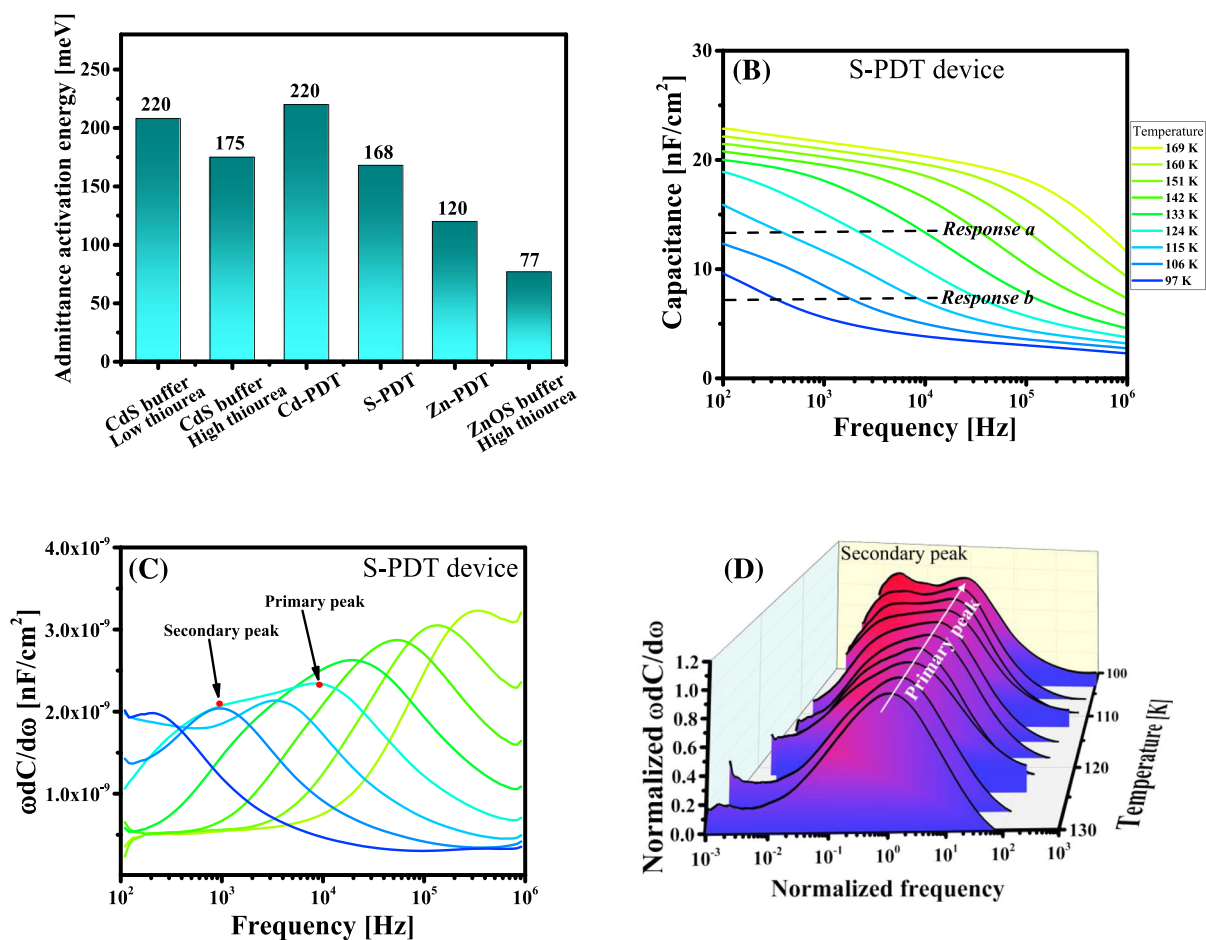
FIGURE 3 (A) Summary of activation energies obtained from Arrhenius plot of the main capacitance step for different post-deposition treatments (PDTs) and buffer layers. The bar chart shows the activation energy of the main capacitance step obtained for devices prepared after performing various PDT on the 10% KCN-etched absorbers. (B) Admittance spectra of S-PDT copper indium diselenide (CISe) absorber in a Schottky device (C) corresponding $\omega dC/d\omega$ plot, which at 124 K shows double peak structure, the high-frequency peak is arbitrarily named primary peak and the low-frequency peak as secondary peak. (D) the plot of normalized frequency versus normalized $\omega dC/d\omega$ with respect to frequency. The curve shows the appearance of a secondary peak particularly at low temperature [Colour figure can be viewed at wileyonlinelibrary.com]

defect signatures. For better visualization, the high-frequency peak of the curve at 124 K is arbitrarily assigned as primary peak and the other as secondary peak in Figure 3C. Figure 3D shows normalized amplitude of the primary peak plotted versus normalized inflection point (i.e., frequency at peak maxima) of the corresponding frequency derivative with the temperature as a parameter. Here, to better resolve the two peaks, the admittance spectra were measured in smaller temperature steps (∼3 K). A careful observation of the plot reveals the evolution of the second peak highlighted in red at low temperatures. This establishes the presence of two different defects, which constitute the main step in the admittance spectra of Cu-rich CISe devices. For the untreated absorbers, the presence of similar broad peaks in the ωdC/dω spectra (Figure 2B) indicates, even in that case, the capacitance step might be originating from contributions of two defects, one more prominent than the other. Lastly, the AS of Cd-PDT device does not show any reduction of the activation energy of the capacitance step (Figure 3A), confirming that neither Cd^{2+}, $(SO_4)^{2-}$, or OH^- results in passivation as they are contained in Cd-PDT solution. To summarize Zn treatment leads to a complete passivation of the defects, whereas S treatment leads to a partial passivation and Cd treatment alone leads to no passivation of the defect. In addition to these chemical treatments, ultrahigh vacuum (UHV) annealing, which is known to passivate near surface properties of $Cu(In,Ga)Se_2$, also results in passivation of the 200-meV defect (see discussion in Figures S3 and S4).[41–43] Thus, together with this and the PDT results, it can be concluded that the 200-meV defect is actually a defect at or near the surface. The defect is most probably the Cu—Se divacancy defect complex[44] as it is passivated by Zn PDT and S/Se PDT. This is because Zn cation can easily passivate the Cu vacancy due to its similar ionic radii, whereas the S/Se anion can directly passivate the Se vacancy. Besides this, the AS results suggest that the defect capacitance signal consists of two constituents, one of which (probably the Cu—Se divacancy defect signal) can be passivated with proper surface treatment.

To get an estimate of defect density, capacitance steps consisting of overlapping defect contributions (see for instance Figure 3D) were fitted as described in Weiss et al.[45] In particular, the defect response from a discrete defect level is extended to Gaussian defect distributions. Here, two Gaussian distributions are used and are fitted simultaneously to the complete temperature and frequency range. A fit describing the two and overlapping capacitance steps of the spectra shown in Figure 3D is shown Figure S5. For untreated sample, a defect density of $\sim 2 \times 10^{16}$ cm^{-3} and, for S-PDT sample, a defect density of $\sim 4 \times 10^{15}$ cm^{-3} were obtained.

To summarize, the experimental findings are as follows: The 200-meV defect is an acceptor defect, has a defect density of around $\sim 10^{16-17}$ cm^{-3},[35] and is present at or near the surface; that is, it is a subsurface defect. It is unclear how this defect can lead to the observed large interface V_{OC} loss and to a saturation current activation energy lower than the bandgap. In the next section, a numerical model is realized by introducing defects in CISe based on above discussed defect properties with the aim to describe the experimentally observed losses.

1.3 | Numerical simulation with subsurface defects

The results of the previous section indicate the near-surface and acceptor nature of the defect, that is, an acceptor defect present close to or at the absorber/buffer (A/B) interface. Therefore, the defect could represent either a defective layer within the absorber, just below the surface, or a defective interface (rather unlikely) between the absorber and the buffer. In this section, using numerical modeling, the impact of both a defective layer and a defective interface on the $V_{OC,in}$ and $V_{OC,ex}$ of the device will be investigated. The models will be assessed to reproduce the experimentally observed characteristics of Cu-rich CISe devices as discussed before: (i) >100-meV interface V_{OC} deficit, (ii) an E_a of the saturation current density lower than the E_G of CISe, and (iii) an "S shape" in the first quadrant at lower temperatures in the I-V curves.

A device model is designed in SCAPS-1D emulating the Cu-rich CISe devices (back contact/CISe/CdS/ZnO/Al:ZnO/front contact). Table S1 records the electrical and optical parameters used in the simulations, which were set constant, taking values from previous measurements,[46–48] and are the same as in our earlier simulations.[36] Further, no conduction band offset at the absorber/buffer (A/B) interface and flat band conditions at the absorber back contact were assumed to keep the model as simple as possible and to avoid convergence problems in SCAPS. Two models were developed. Both models involve deep acceptor defects, because the characteristic defect in Cu-rich CIS is a ∼200-meV deep acceptor state. The first model comprises a defective layer (often called p^+ layer in the literature,[49,50]) that is, a thin layer with high concentration of acceptor defects 220 meV away from the conduction band. There are no deep defects at the interface in this model (Figure 4A). Recently we have presented a similar model of a defective layer with an acceptor defect 220 meV away from the valence band.[36] All the features of the temperature dependence of the JV characteristics, as discussed in the following, are the same, independent of the energetic position of the defect (see also Figure S9). The second model comprises a defective interface, with a significant amount of deep interface acceptor defects above mid-gap at the A/B interface and large electron capture cross section, to ensure Fermi-level pinning (Figure 4B). The defect level is placed 0.65 eV above the valence band in this model. The defect energy value was chosen to allow for simulating an activation energy for recombination current as close as possible to the experimental values. The values of F_e and F_h give a measure of the density of thermal or photogenerated free carriers in the conduction and valence band, respectively. The high defect density (N_d) along with a large electron capture cross section (reported in Table S1) in both models results in strong reduction of electron quasi-Fermi level (F_e) and thus a reduction of the $V_{OC,in}$ near the surface due to Shockley–Read–Hall (SRH) recombination. Consequently, the $V_{OC,ex}$ of the device is reduced. Moreover, in both models, the $V_{OC,in}$ is reduced only in a very small region near the A/B interface: ∼100 nm for the defective layer and ∼50 nm for the defective interface, but is otherwise uniform throughout the absorber. This quasi-Fermi level gradient near the surface is observed independent of the carrier mobility. Even in high mobility
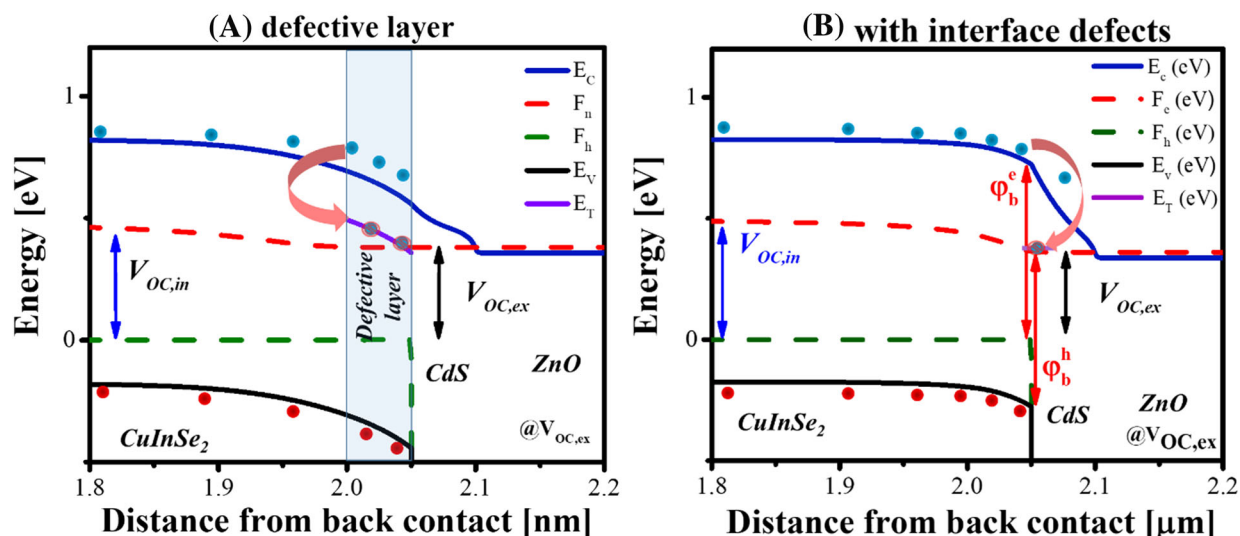
FIGURE 4 Simulated band diagram of the device at open-circuit ($V_{OC,ex}$) voltage with (A) defective layer and (B) interface defects. The maximum quasi-Fermi-level splitting in the device is labeled as $V_{OC,in}$, whereas the $V_{OC,ex}$ values are represented as the difference between the hole quasi-Fermi level at the back contact and electron Fermi level at front contact. The purple line shows the defect levels with high concentration in the device structure and φ_b is the hole barrier at the interface. The equilibrium band diagram is shown in Figure S6 [Colour figure can be viewed at wileyonlinelibrary.com]

limit (electron mobility values ~100 cm^2/V·s), the $V_{OC,in}$ is reduced near the surface in the CISe device. A $V_{OC,in}$ measurement by PL reflects the (nearly uniform) maximum $V_{OC,in}$ in the bulk of the absorber, as the PL intensity increases exponentially with the $V_{OC,in}$. The $V_{OC,ex}$ is the difference between the majority quasi-Fermi levels on either side. Because there is only a negligible gradient in the hole quasi-Fermi level, the $V_{OC,ex}$ is given by the $V_{OC,in}$ at the absorber buffer interface. Hence, it is established that both models result in deficit between the measured $V_{OC,in}$ and the $V_{OC,ex}$, as depicted in Figure 4.

As demonstrated in Figure 4, both models are capable of reproducing the experimentally observed $V_{OC,in}$ and $V_{OC,ex}$, and hence, the interface V_{OC} deficit. However, the validation of either model as the appropriate description for Cu-rich CISe devices requires also fulfillment of criteria (ii) and (iii). All Cu-rich chalcopyrite devices are characterized by a saturation current strongly dominated by interface recombination. This is indicated by E_a obtained from extrapolating $V_{OC,ex}$ versus temperature being always lower than the E_G.[10,19] As shown before, the Cu-rich CISe devices presented here also suffer from the same issue. Two possible explanations for an activation energy of the saturation current E_a lower than the bandgap are established in the literature: a cliff at the absorber buffer interface, that is, conduction band minimum of CdS lower than that of CISe, or Fermi-level pinning at this interface.[19,51] Thus, a straightforward origin of interface recombination could be an unfavorable band offset, that is, a cliff at the interface. However, CdS is a perfectly suited buffer for Cu-poor Cu(In,Ga)Se$_2$ absorbers, which have a higher conduction band minimum than pure CuInSe$_2$. There is no indication that the band edges of Cu-rich CuInSe$_2$ are different from those of Cu-poor material. Furthermore, the photoelectron study by Morkel et al.

reports a conduction band minimum of CdS aligned with the one of CISe, eliminating unfavorable band offset as the possible cause for interface recombination.[52] The other possible scenario could be the presence of a high concentration of defects (N_{IF}) at the CISe/CdS interface, which pins the electron Fermi level at the interface. In order to have a working solar cell like in Figure 1A, the pinning position must be above the middle of E_G to obtain a decent $V_{OC,ex}$. Thereby, the electron concentration at the interface remains significantly higher than the hole concentration. Thus, making the interface recombination dependent on the interface hole concentration (p_{IF}) and the hole surface recombination velocity (S_p), that is, R $\approx p_{IF} * S_p$.[19] The reverse saturation current density (J_0) then is given by[19]:

$$J_0 = qN_{v,a}S_p\exp\left\{-\frac{\varphi_b^h}{kT}\right\}, \qquad (1)$$

where $N_{v,\,a}$ is the effective valence band density of states in the absorber and q is the elementary charge, and φ_b^h is the equilibrium hole barrier at the interface and is equal to the energy difference between the position of electron Fermi level (F_e) and the valence band edge (E_v) under equilibrium, that is, $\varphi_b^h = F_e - E_{v.}$. We keep the nomenclature that is used in the literature,[33] although, out of equilibrium, for example, for a device under illumination like in Figure 4, φ_b^h does not represent the hole barrier. Equation 1 is true if the recombination current is dominated by interface recombination, that is, in the case of a significant S_p. This is more likely for a negatively charged interface, that is, with a high density of acceptor states. However, it is not necessarily the case that the pinning defect and the recombination defect are the same, although this is what we assume in our simulation. From Equation 1, it is evident that in case of Fermi-level pinning, the E_a of

the saturation current should be φ_b^h, which is lower than E_G. Consequently, the open-circuit voltage is given as follows[19,51]:

$$V_{OC,ex} = \frac{\varphi_b^h}{q} - \frac{kT}{q}\ln\left(\frac{qN_{v,a}S_{p0}}{J_{ph}}\right), \qquad (2)$$

where J_{ph} is the photogenerated current. Thus, $V_{OC,ex}$ is dominated by φ_b^h. One should note that for a good device that is not dominated by interface recombination, the $V_{OC,ex}$ at 0 K is equal to the bandgap of the absorber. It should be cautioned though that extrapolation of $V_{OC,ex}$ to the bandgap does not exclude interface recombination.[53] Thus, in case of Cu-rich CISe device with spike-type band alignment, Fermi-level pinning could explain an E_a value smaller than E_G, namely, φ_b^h obtained from $V_{OC,ex}$ versus temperature plot (assuming n, S_p, and J_{ph} are not or only weakly temperature dependent). We will therefore investigate further predictions from this model in the following.

For conceiving the appropriate defect model for CISe by numerical simulations, the device performance as displayed in Figure 1 will be simulated. Figure 5A shows the simulated $V_{OC,ex}$ values at different temperatures obtained from the two models with defects at or near the interface and for a reference model without any near interface defects. The simulations go down to 250 K; at lower temperatures, the numerical calculations would no longer converge. Remarkably, not only the model with electron Fermi-level pinning but also the model with a defective layer leads to an E_a of the saturation current less than the absorber E_G. It should be noted that the main recombination in the device with defective layer occurs in that defective layer and not at the interface (Figure S6D). The E_a values obtained with this model are slightly higher than experimental values. Even a considerable increase in defect concentration does not result in an E_a value below 0.78 eV (Figure S7A), but the activation energy depends on the exact energetic position of the defect.
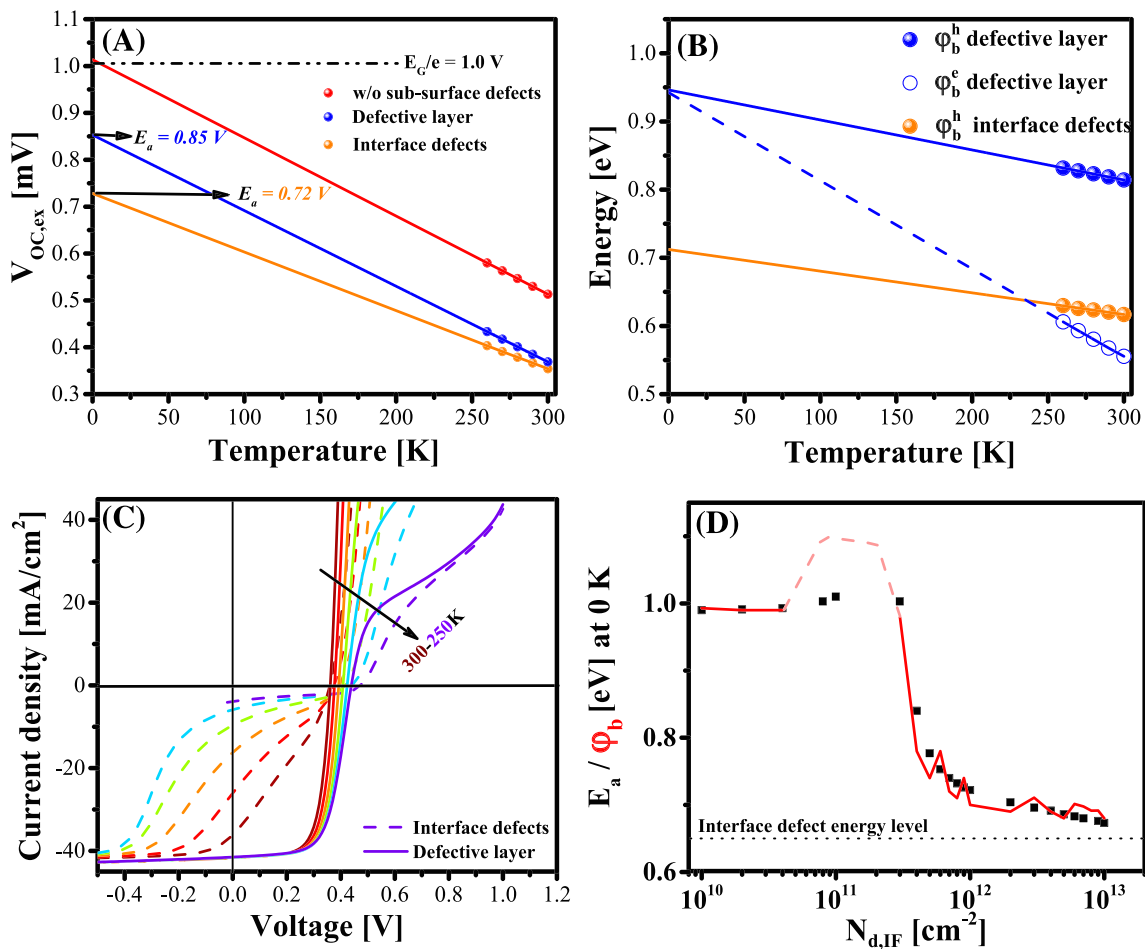

FIGURE 5 (A) Simulated external open-circuit voltage ($V_{OC,ex}$) values of the device with defective layer and of the device with interface defects. (B) the electron and hole barrier as the function of temperature and its extrapolation to 0 K. (C) Simulated current–voltage (I-V) curve at different temperatures of devices with defective layer and with defective interface. The former results in "S shape" in first quadrant (solid lines), whereas later results in "S shape" in third and fourth quadrant (dashed lines). (D) Activation energy (E_a) and the φ_b^h at 0 K for the device with interface defects as a function of interface defect density. The E_a is obtained from V_{OC} versus temperature curve and φ_b^h is obtained from extrapolation of hole barrier to 0 K. the graph clearly shows a direct correlation of the activation energy with hole barrier height. Both quantities approach the energy of the defect at high defect concentrations. We believe that the two points with φ_b larger than E_G are a numerical artifact [Colour figure can be viewed at wileyonlinelibrary.com]

Thus, both models are capable of introducing a recombination pathway with an E_a lower than the E_G. Another important observation comes from the hole barrier simulation at different temperatures (Figure 5B). Neither of the two models results in a temperature-independent hole barrier (φ_b^h). However, φ_b^h exhibits a only a weak temperature dependence in the device with interface defect, and the extrapolation of φ_b^h to 0 K equals the E_a obtained from $V_{OC,ex}$ measurements. This indicates that the simple model of Fermi-level pinning in Equation 1 is only an approximation, and E_a should be identified as φ_b^h at 0 K, as φ_b^h itself is weakly temperature dependent. It is noteworthy that the N_{IF} used here was 10^{12} cm^{-2} and even N_{IF} of 10^{14} cm^{-2} results in a weakly temperature dependent φ_b^h. Even in the latter case E_a is not equal to φ_b^h at 300 K.

It should be noted that we pin the Fermi level in our model by a high concentration of acceptor defects. It is possible that a more perfect pinning is obtained by a combination of acceptor and donor defects. Contrarily, in the device with the defective layer, both φ_b^h and $E_C - F_h$ (φ_b^e) are strongly temperature dependent and extrapolate to a value lower than the bandgap E_G, but higher than the activation energy E_a. This is to be expected, because the recombination takes places throughout the depth of the defective layer, where both values φ_b^h and φ_b^e change with position. The extrapolation of $V_{OC,ex}$ is given by the difference between the two Fermi levels as T approaches 0 K. This difference is constant along the depth of the defective layer. Thus, each φ_b taken individually is larger than E_a. There is a small difference between the extrapolated values of φ_b^h and φ_b^e on the one hand $V_{OC,ex}$ on the other, which can be explained by the rather long extrapolation. In summary, a strongly defective layer can lead to activation energies lower than E_G, without Fermi-level pinning and without a cliff in the conduction band alignment.

Finally, we test the model on criterion (iii), that is, the "S shape" in the first quadrant exhibited by Cu-rich CISe devices at lower temperatures. It has already been established it the literature that the "S shape" in the I-V curve originates from cliff at CdS/ZnO interface.[19] Therefore, in contrast to the above models where we had used only flat band conditions at the different interfaces, for the simulations in Figure 5C, we introduce a spike of 0.1 eV at the CISe/CdS interface and a 0.4-eV cliff at the CdS/ZnO interface. The particularly high cliff offset value was used to simulate the rollover in the first quadrant at higher temperature as SCAPS fails to converge at lower temperature. Figure 5C shows the I-V curves at low temperatures simulated for a device with a defective layer and a device with defective interface. For the first model, "S shape" in I-V at low temperatures in only the first quadrant is observed. On the contrary, the presence of Fermi-level pinning at interface leads to an "S shape" in the first and fourth quadrant. The rollover in the first quadrant in both models is due to the presence of a cliff at the CdS/ZnO interface (see Figure 6A). As a consequence, the electron density in the CdS layer is very low, which requires a significant gradient in the electron quasi Fermi level to drive the diode current. In contrast, in the case without cliff-like band alignment and thus higher electron concentration in the CdS layer, that drop of the electron quasi Fermi-level ΔF_n^{CdS} in the CdS buffer layer would otherwise contribute to the quasi Fermi-level splitting in the CuInSe$_2$ absorber and therefore yield a higher diode current, that is, no S shape in the first quadrant. As for the "S shape" in the fourth quadrant, the acceptor-type interface defects introduce negative charge at the interface that significantly reduces the band bending inside the absorber (see Figure 6B). This results in a higher concentration of holes near the interface as F_h is closer to the valence band maximum. Because holes are minority carriers near the interface, consequently, under illumination, there is higher recombination in the device leading to a lower photocurrent. The recombinations become even stronger as forward bias is applied; this is because the band bending decreases and F_h moves even closer to the valence band further reducing the photocurrent, and therefore to a "S shape" in fourth quadrant. In the model with defective layer on the contrary, the deep defects near the interface become charged as they cross the Fermi level. This charge is added to the total charge of the absorber; consequently, the band bending inside the absorber becomes steeper. As a result, the F_h is further away from the valence band maximum near
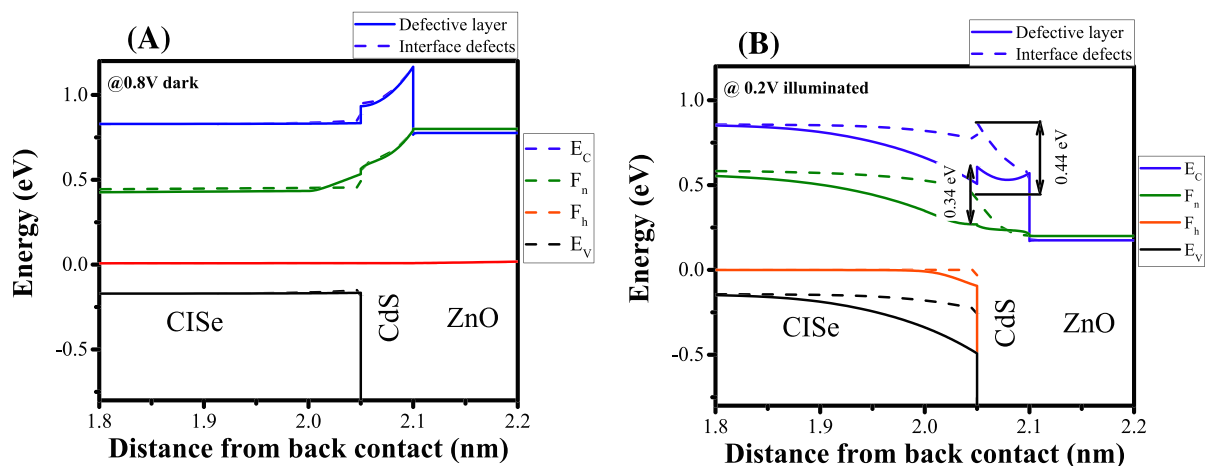
FIGURE 6 Simulated band diagram of copper indium diselenide (CISe) device with defective layer and interface defects (A) in the dark at 0.8 V at temperature 250 K (B) under illumination at 0.2 at 250 K [Colour figure can be viewed at wileyonlinelibrary.com]

the interface compared with the case of interface defects and therefore does not affect the photocurrent significantly. Additionally, the spike at the absorber–buffer interface can act as a barrier for the photocurrent. For the interface model, the "S shape" becomes stronger as the temperature decreases leading to a strong reduction in J_{sc} (Figure 5C). The simulation in Figure 6D indicates that the barrier is considerably higher in the case of the interface defect, because of the weaker band bending inside the absorber, thus acting as a barrier for the extraction of photogenerated carriers. Experimentally, such a reduction in J_{sc} is not observed; see Figure 1D. Thus, the I-V-T behavior of the device is best described by the model with a defective layer.

It is established that the model with a defective layer explains, to a good extent, the experimentally observed Cu-rich CISe device characteristics. Moreover, although the defects were placed 220 meV away from conduction band, the defects if placed 220 meV away from valence band also result in similar observations (see the Supporting Information). At this point, it is worth summarizing a few points regarding both models. Both models lead to a significant interface V_{OC} deficit in the device and an $E_a < E_G$. The exact values of both V_{OC} deficit and E_a depend on the defect properties such as defect energy, density, and capture cross section. However, the exact mechanism in the two cases is different: In the defective layer model, the main recombination is in the SCR close to the surface. On the contrary, the CISe/CdS interface is the location of the main recombination channel in the defective interface model and leads to a weak electron Fermi-level pinning as evident from Figure 5B where φ_b changes only weakly with temperature. The E_a is given by the value of φ_b^h at 0 K. Figure 5D shows simulated E_a and φ_b^h at 0 K (obtained by extrapolating simulated hole barrier values to 0 K), as in Figure 5A,B as a function of interface defect density ($N_{d,IF}$). It is clear that in a certain range by varying the defect density, one can have E_a anywhere between the E_G and the defect position in the interface E_G. Further, there is a one-to-one correlation between E_a and φ_b^h at 0 K.

Even though the models presented here might not be fully accurate, as they do not include many factors such as surface E_G widening or band offsets between absorber and buffer. Still, the models do a good job of reproducing the main experimental characteristics of Cu-rich CISe devices that indicate a problematic interface and provide a suitable explanation. Out of the two models, the defective p^+ layer explains better the observed I-V behavior at low temperatures. In addition, the simulations demonstrate that the commonly used model of Equation 1 is only an approximation, yet a useful one. Furthermore, we showed that the most critical parameters indicating interface recombination, that is, a significant difference between $V_{OC,in}$ and $V_{OC,ex}$, and an E_a of saturation current lower than E_G can be reproduced by a model that contains neither a reduced interface bandgap, nor Fermi-level pinning.

Moreover, these models, though applied and developed for Cu-rich CISe device, are equally applicable to any other device. Particularly, heterojunction devices that have optimum band offset with the hole and electron transport layer but are still dominated by interface recombination. Other than the conventional Fermi-level pinning due to the interface defects, interface recombination signature could

alternatively originate from the defective surface layer. The results of the simulations also demonstrate a way to differentiate between defective surface and defective interface. In both cases, the temperature dependent $V_{OC,ex}$ measurements will yield an E_a for saturation current lower than E_G. However, the two models can be distinguished looking at the I-V curves. Although a defective layer results in "S shape" in the first quadrant that is more similar to the experimental evidence, the defective interface results in "S shape" in both the first and fourth quadrant. Additionally, the defective interface results in a much reduced short-circuit current as the temperature is reduced, which is not observed experimentally. Thus again, the defective layer gives a more accurate description of the I-V-T behavior of the device. Once the root cause, that is, the presence of either defective interface or defective surface, is identified, a dedicated passivation strategy can be used to improve the device performance.

2 | CONCLUSIONS

In summary, CISe absorbers grown under Cu-excess and Cu-deficient conditions although possess similar $V_{OC,in}$ display different $V_{OC,ex}$ in the device due to presence of near surface defects. DLTS measurements revealed these defects are acceptor in nature. The presence of these acceptor defects in Cu-rich device lead to significant interface V_{OC} deficit leading to lower efficiency and electronic barriers in device structure, which is not observed in Cu-poor device. To elucidate the root origin of interface V_{OC} deficit, we have demonstrated two comprehensive models for Cu-rich CISe solar cells, which can be applied to other heterostructure solar cells as well. These models comprise either a near interface layer or the interface itself with a high concentration of deep acceptor defects. The drift and diffusion simulations have demonstrated that both models are capable of reproducing electrical characteristics of Cu-rich CISe devices, in particular reduced $V_{OC,ex}$ compared with $V_{OC,in}$. The reduction emanates due to deep traps at or near the surface, which lead to strong non-radiative recombinations in the region near the surface and dominate the $V_{OC,in}$ near the surface. As a consequence, the qFLs decreases rather abruptly near the surface resulting in a reduced $V_{OC,ex}$, thus resulting in an interface V_{OC} deficit in the device. In cases as such, the information regarding the gradient $V_{OC,in}$ is not accessible from PL measurements. However, we have demonstrated that the presence of both a defective surface and a defective interface could be confirmed by temperature-dependent $V_{OC,ex}$ measurements. In both cases, the activation energy of the saturation current density obtained by temperature-dependent $V_{OC,ex}$ measurements is lower than the bulk E_G of the absorber. Furthermore, we show that the presence of either defective layer or defective interface in a device predicts an activation energy of the saturation current lower than E_G and can be differentiated through I-V measurements particularly at temperatures below 300 K. Whereas the defective layer leads to a "S shape" in the first quadrant of the I-V curve as a signature of a barrier for injected carries, as observed experimentally, the defective interface leads to a "S shape" in the fourth as a signature of a barrier to photogenerated carriers.

Particularly for Cu-rich CISe solar cells together with AS and DLTS spectroscopy, a model is developed, which correlates the interface V_{OC} deficit to the presence of acceptor defect in Cu-rich CISe absorbers. A comparison of AS of absorbers etched with aqueous KCN and aqueous Bromine solutions revealed the defect to be an intrinsic part of Cu-rich devices originating from the etching of secondary phases, independent of the etchant. DLTS confirms that this defect is an acceptor defect. Analysis of several PDTs on the CISe absorbers demonstrated that the usual broad AS defect signature is produced by the response from two defect levels close to each other. The PDT results are in agreement with the Cu—Se divacancy as the cause of 200-meV defect signature.

As a general point of view, calibrated PL measurements provide information regarding the ratio of non-radiative to radiative recombination in the bulk of the absorber. However, in these measurements, near surface properties could be overlooked. To account for these, there is the need of complimentary techniques such as temperature dependent I-V measurements to characterize the device and assign recombination channels in the device. We have provided two universal models that can also be applied to others photovoltaic technologies to explain and understand the cause of interface V_{OC} deficit in the case where the band alignment does not impose a cliff situation.

2.1 | Device preparation and characterization methods

For the experiments, we used polycrystalline CISe thin films grown on molybdenum-coated soda lime glass in a one-stage process. Comprehensive details of the deposition process can be found in our previous report.[35] For investigating the impact of Zn, Cd, and S PDTs, the CISe absorbers were etched with 10% KCN solution for 5 min to remove the $Cu_{2-x}Se$ secondary phase. These were then immersed in three separate solutions; $3CdSO_4.8H_2O$ (0.1 M) in NH_4OH (2 M), $ZnSO_4.7H_2O$ (0.1 M) in NH_4OH (2 M), and CH_4N_2S (0.4 M) in NH_4OH (2 M) at 84°C for 15 min, all freshly prepared. For bromine treatment, the un-etched absorbers were immersed in aqueous Br_2 (0.01 M) plus potassium bromide (0.3 M) solution for 1 min. The treatment schematic can be seen in Figure S8.

The treated absorbers were further processed into two device configurations for characterization: "Schottky device" ($CuInSe_2$ with aluminum dots) and "Solar cell" ($CuInSe_2$ coated with CdS followed by zinc-oxide, aluminum doped zinc-oxide, and nickel aluminum grids). A standard Xenon short-arc lamp AAA solar simulator calibrated with a reference Si solar cell, with an IV source measure unit was used to measure the I-V of the devices. To perform low-temperature electrical characterization (AS, DLTS, and I-V-T), the devices were mounted inside a closed-cycle cryostat under vacuum below 4×10^{-3} mbar. A cold mirror halogen lamp adjusted to an intensity of ~100 mW/cm^2 was used to illuminate the device for I-V-T measurements. An inductance, capacitance, and resistance (LCR) meter was used to measure the admittance of the sample. In the setup, a controlled small-signal ac voltage pulse of 30 mV rms with frequency from $f = 20$ Hz to 2 MHz

was applied. In order to ensure accurate determination of device temperature during all the characterization, a Si-diode sensor glued onto an identical glass substrate was placed beside the solar cell. The numerical simulations were executed using SCAPS1-D software developed at the department of Electronics and Information Systems (ELIS) of the University of Gent, Belgium.[54]

CONFLICT OF INTEREST

The authors declare that they have no financial/commercial conflict of interest.

DATA AVAILABILITY STATEMENT

The data of Figures 1A,C, 2A, and 3B,D along with the SCAPS definition file are available at https://orcid.org/10.5281/zenodo.4643534.

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