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2-D Layered Materials for Next-Generation Electronics: Opportunities and Challenges

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(Invited Paper)

***Abstract*— Since the discovery of graphene in 2004, which proved the existence of 2-D crystals in nature, layered materials also known as van der Waals solids have received extensive reexamination, especially in the single-layer and multilayer forms because of their van der Waals type structure and unique properties that not only benefit many existing electronic components but also enable novel device concepts and design architectures. Numerous research efforts have been invested in these materials, and enormous quantities of results have been generated during the past 14 years. This paper provides an overview of the key physics and technology issues along with the most promising nanoelectronic applications of these materials and also identifies the challenges in this rapidly evolving field.**

***Index Terms*— 2-D layered materials, 3-D integration, black phosphorus (BP), field-effect transistor (FET), graphene, hexagonal boron nitride (h-BN), inductor, intercalation, interconnect, IoT, logic, low-frequency noise, memory, neuromorphic, scaling, sensor, synthesis, transition metal dichalcogenide (TMD), van der Waals heterostructures, very large scale integration (VLSI).**

I. Introduction

THE discovery of low-dimensional (with respect to the conventional 3-D or bulk materials) materials has triggered tremendous research surge, not only among material scientists and physicists but also in the electronic/optoelectronic device communities, because the unique physics and properties of these materials can enable novel and interesting nanoelectronic/optoelectronic applications. Before the 21st century, 0-D and 1-D materials, specifically fullerene (such as buckminsterfullerene and C_{60}) [1] in 1985 and carbon nanotube (CNT) [2] in 1991, respectively, had been successively discovered, while 2-D materials remained the only missing family in the low-dimensional material system. Theorists had arguably attributed the missing 2-D form to its thermodynamic instability in nature [3]. Although the electronic structure and properties of graphene [a single layer (1L) of carbon atoms and the earliest discovered member of the 2-D material family] were theoretically predicted by Wallace [4], and 1L carbon foils had been described by Boehm *et al.* [5], it was not until the beginning of the 21st century (in 2004/2005) when Novoselov *et al.* [6], [7] accidentally found that graphene and other 2-D crystals, such as 1L transition metal dichalcogenides (TMDs), can be stable at room temperature. This breakthrough triggered unprecedentedly broad and intensive research efforts across the world, not only because of the unexplored 2-D physics but also due to the significantly easier manufacturability of planar 2-D, compared to 0-D and 1-D materials. Benefiting from such a vigorous research environment, the theoretical infrastructure of 2-D physics was quickly established within the first several years [8], [9] following the discovery of graphene in 2004, and its swift recognition with the Nobel Prize in 2010. Subsequently, a number of exciting applications [10], [11] such as graphene-based molecular filter, graphene photon detector, graphene spintronics, atomically thin-body 2-D field-effect transistors (FETs), TMD valleytronics, and 2-D topological insulator were proposed. "All 2-D" circuits combining graphene interconnects with TMD transistors were also proposed [11]. During the past decade, researchers have been focused on improving and innovating these 2-D technologies. Some of the applications have achieved great progress toward large-scale production, while others still require more research efforts to prove their potential as well as practicality. Therefore, at this moment, a review of the motivation, progress, and remaining challenges of these 2-D technologies, as well as in-depth analysis for overcoming the challenges, is highly desirable for researchers in this field. This paper aims at providing such a review, exclusively focused on the 2-D nanoelectronics domain.

This paper is organized as follows. Section II provides a brief introduction to the fundamentals of 2-D materials. Section III reviews the core elements of 2-D electronics—2-D-FETs, as well as their derivatives including memory, sensors, and memristors, along with 2-D-tunnel-FETs (TFETs) for low-power (LP) electronics. 2-D interconnects that serve as the skeleton of 2-D electronic circuits are analyzed in Section IV. Passive devices, mainly inductors and capacitors, that uniquely exploit 2-D physics and properties are reviewed in Section V. Section VI discusses the ultimate scaling scenario—3-D integration of 2-D layered electronics.

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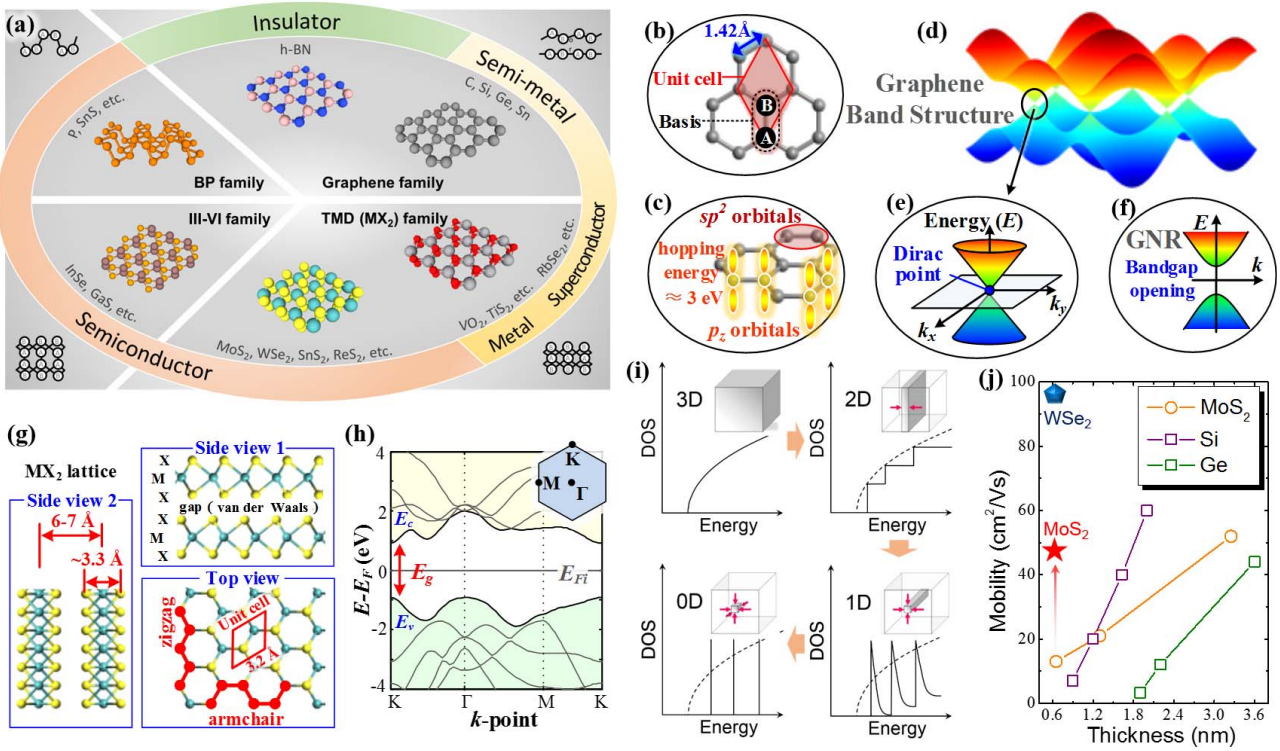

Fig. 1. (a) Broad 2-D material family [10]. (b) Unit cell, basis, and bond length of graphene. (c) Atomic orbitals of graphene. (d) Band structure of graphene, in which the energy dispersion (e) is linear for low energies near the six corners (Dirac points) of the 2-D hexagonal Brillouin zone. (f) Energy dispersion of a GNR, in which a bandgap can be engineered by varying the width, due to carrier confinement. (g) Lattice structure of TMDs from different views. (h) Band structure of typical TMDs such as MoS_2 and WSe_2. (i) DOS variation with reduced material dimension. (j) Mobility reduction with material thickness. Recently obtained electron mobility of 1L CVD MoS_2 and WSe_2, by improving material quality, are also shown, indicating that the improvement space of 2-D materials is large. Data for MoS_2, Si, Ge, and WSe_2 are obtained from [17]–[20], respectively.

Section VII briefly discusses 2-D material synthesis. Concluding remarks are provided in Section VIII.

II. Fundamentals of 2-D Layered Materials

In nature, more than 1800 types of layered materials among 108,423 experimentally known 3-D compounds have been found [12] through density functional theory calculations, to be "exfoliable" to 1L or multilayer (ML) (<10 nm) form, which are referred to as 2-D materials in this paper, if not specified otherwise. 2-D material family is so broad that almost all conduction mechanisms (metal, semimetal, semiconductor, insulator, superconductor, and topological insulator) can be found within the family, as shown in Fig. 1(a). This paper only covers those that are relevant to nanoelectronic devices, specifically, the semi-metallic graphene, insulating hexagonal boron nitride (h-BN), semiconducting/metallic TMDs, graphene nanoribbon (GNR), and black phosphorus (BP). Despite the diversity in the band structure, all 2-D materials share three common features. First, adjacent layers are held together by the relatively weak van der Waals bonds, while strong valence bonds firmly pack the in-plane (or in-layer) atoms together. The second feature is the atomic scale and uniform thickness (0.34–0.7 nm) of each layer that allows ultra-flexible and transparent electronics/optoelectronics. The third common feature is the pristine (or dangling bond free) surface. The combination of the first and the third features allow 2-D materials to be exfoliated akin to "peeling of onions," in contrast to the "potato slicing" manner of thinning the bulk materials (such as Si, Ge, and III–V compound semiconductors).

Graphene is formed by a 1L of carbon atoms (0.34 nm thick) arranged in a 2-D hexagonal (honeycomb) lattice. Fig. 1(b) schematically shows the basis (composed of two distinct types of carbon atoms, A and B), the parallelogram unit cell and the bond length (~1.42 Å) of graphene. As shown in Fig. 1(c), each carbon atom shares three electrons with three nearest neighbors in the form of sp^2 bonding, forming the in-plane σ band. The σ band determines graphene's structural and vibrational properties, such as its thermal conductivity and Young's modulus but does not contribute to its electrical properties. The strong coupling (hopping energy ~ 3 eV) between remaining p_z orbitals of carbon atoms form the π bands that impart graphene its exceptional electrical conductivity. These bands are featured with a peculiar linear E-k relation around the Dirac point and a zero bandgap, as shown in Fig. 1(d) and (e).

GNR is a narrow (<10 nm) strip of graphene with an intentionally designed spatial confinement along the width direction, thereby opening up a bandgap ($E_g = 1.4/w$ eV, w is in the unit of nanometers) [13], as shown in Fig. 1(f). GNRs have been extensively studied for many LP applications, such as logic FETs. The bandgap in GNR allows the ON/OFF current ratio of GNR FETs to be larger than four orders, which is beyond the capability of zero bandgap graphene.

1L h-BN [14] and BP [15] have similar lattice structure as graphene, the difference is that in h-BN, B and N atoms

TABLE I
BASIC PARAMETERS OF SEVERAL TYPICAL 2-D MATERIALS. E_g IS BANDGAP, $m_{e/h}$ IS ELECTRON/HOLE TRANSPORT EFFECTIVE MASS ALONG x/y-DIRECTION. T_{1L} REPRESENTS THE THICKNESS OF 1L 2-D MATERIAL

	Graphene	MoS_2	WSe_2	BP	h-BN
E_g (eV)	0	1.8	1.6	1.6	5.9
$m_{\_e,x/y}$ (m_0)	massless	0.57	0.36	0.12/1.3	0.26/2.21
$m_{\_h,x/y}$ (m_0)	massless	0.61	0.41	0.08/5.8	0.47/1.33
T_{1L} (nm)	0.3	0.65	0.65	0.65	0.3

replace carbon in the A and B positions in Fig. 1(b), while in BP, two P atoms at A and B positions are in different basal planes. Such breakup of lattice symmetry results in the asymmetric band structure with a bandgap of around 5 and 1.6 eV for h-BN and BP, respectively. Due to its large bandgap, h-BN is usually employed as an insulator in electron devices, such as the gate dielectric or substrate in FETs. BP is a highly anisotropic semiconductor (dissimilar effective mass along the x- and y-directions) and has been identified as a promising channel material (with mobility more than 1000 $cm^2/(V{\cdot}s)$) for high-performance (HP) FETs [15], [16].

TMDs have two types of atoms, M and X, which are arranged in a 2-D honeycomb array within the TMD plane, and in an X-M-X sandwich form normal to the TMD plane, as shown from different views in Fig. 1(g). M stands for the transition metal, such as Mo and W. X stands for chalcogen, such as O, S, Se, and Te. Each TMD layer has a fixed and a uniform thickness of ~0.65 nm. Fig. 1(h) shows the typical band structure of 1L TMD semiconductors, in which a parabolic conduction band minima and parabolic valence band maxima separate, and are both at the high-symmetry K point in the first Brillouin zone, i.e., typical 1L TMDs have direct bandgaps (obtained by the first-principle calculations), in contrast with corresponding bulk TMDs which have indirect bandgaps. The indirect-to-direct bandgap transition from bulk TMDs to 1L TMDs is due to the spatial confinement along the thickness direction.

In Table I, the basic parameters of several typical 2-D materials are summarized. As shown, typical semiconducting 2-D materials, MoS_2, and WSe_2 have relatively large effective masses, indicating that although the total density of states (DOS) is reduced due to the reduction of material dimension [Fig. 1(i)], these 2-D semiconductors can provide sufficiently large local DOS for electron devices, such as FETs that are made on material surfaces. On the other hand, it has been found that 2-D materials suffer less from mobility degradation, with respect to bulk materials such as Si [18] and Ge [19], when the material thickness is reduced [Fig. 1(j)]. Note that compared to the mature Si and Ge, the material quality of 2-D semiconductors still has plenty of room for mobility improvement, as reflected by the boosting of electron mobility in synthesized 1L WSe_2 [20]. These properties make 2-D materials promising for electron device applications.

III. 2-D-FET AND ITS APPLICATIONS

A. Logic Devices

The 2-D-FET is the most widely studied topic among all 2-D applications. For a typical FET, as schematically shown in Fig. 2(a), a term called natural length λ [21], which is essentially a feature length across which the majority of channel potential is dropped [Fig. 2(b)], can be employed to estimate the scalability of a specific FET structure. Obviously, a smaller λ promises better device scalability. According to the expression of λ [Fig. 2(c)], an ultrasmall channel thickness T_{ch} is desired, which explains the surge of the 2-D-FET research. However, such rough scalability estimation is not sufficient. Major metrics for FETs in digital applications [Fig. 2(d)] such as, ON/OFF currents (I_{ON}/I_{OFF}), and subthreshold swing (SS), have to be derived quantitatively, for both HP and LP applications. To determine the shortest channel lengths allowed by 2-D-FETs and TFETs, rigorous quantum transport simulations were carried out [16], [22], [23] to evaluate the performance of such FETs in sub-10-nm channel length scale. As shown in Fig. 2(e), for L_g of up to 5.9 nm, double gate (DG) structure can maintain an acceptable SS for MoS_2 FETs with a number of layers up to 3L, while single gate silicon-on-insulator (SOI) structure can only sustain 1L MoS_2. In contrast, the SS of Si DG MOSFET is much worse. It is found that 2L/1L MoS_2 provides the highest performance for HP and LP applications, respectively. For $L_g = 5.9$ nm, the optimal effective mass is around $0.3m_0$, below which the 2-D-FET suffers from source-to-drain tunneling leakage and above which the carrier velocity decreases. It is also found that the ultrathin body of 2-D enables a novel gated Esaki diode (GED) structure for TFETs, which makes the device scalable to 3 nm. The switching energy and delay of various sub-10-nm 2-D-FETs are benchmarked in Fig. 2(f) confirming their potential for ultra LP computing.

On the experimental front, Radisavljevic *et al.* [24] implemented the first top-gated 2-D-FET with 1L MoS_2, in which ON/OFF current ratio and SS were reported to be 10^8 and 74 mV/dec, respectively. Although the mobility of their 1L MoS_2 was subsequently corrected to be ~10 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [25], it has been effectively enhanced by improving material quality, and/or engineering the dielectric environment [26], [27]. Fig. 2(g) summarizes the highest mobility data from experiments for various 2-D materials [17]–[20], [26]–[30] along with their bandgaps. Graphene, BP, and tellurene show high mobilities but with zero or low bandgaps, which limits their application in LP electronics. The mobilities of other 2-D semiconductors are generally lower than that of bulk semiconductors. However, the latter decreases rapidly with film thickness, as reflected by the Si data. 2-D semiconductors become very competitive at 1L and 2L cases. Note that since the channel width is much larger than the 2D channel thickness, its effect on mobility is generally negligible compared to the effect of channel thickness.

Contact plays an important role, especially in short-channel FETs. The extreme thinness and relatively large bandgap of 2-D TMDs inevitably bring challenges to low-resistance ohmic contact formation. Most demonstrated 2-D-FETs in the early

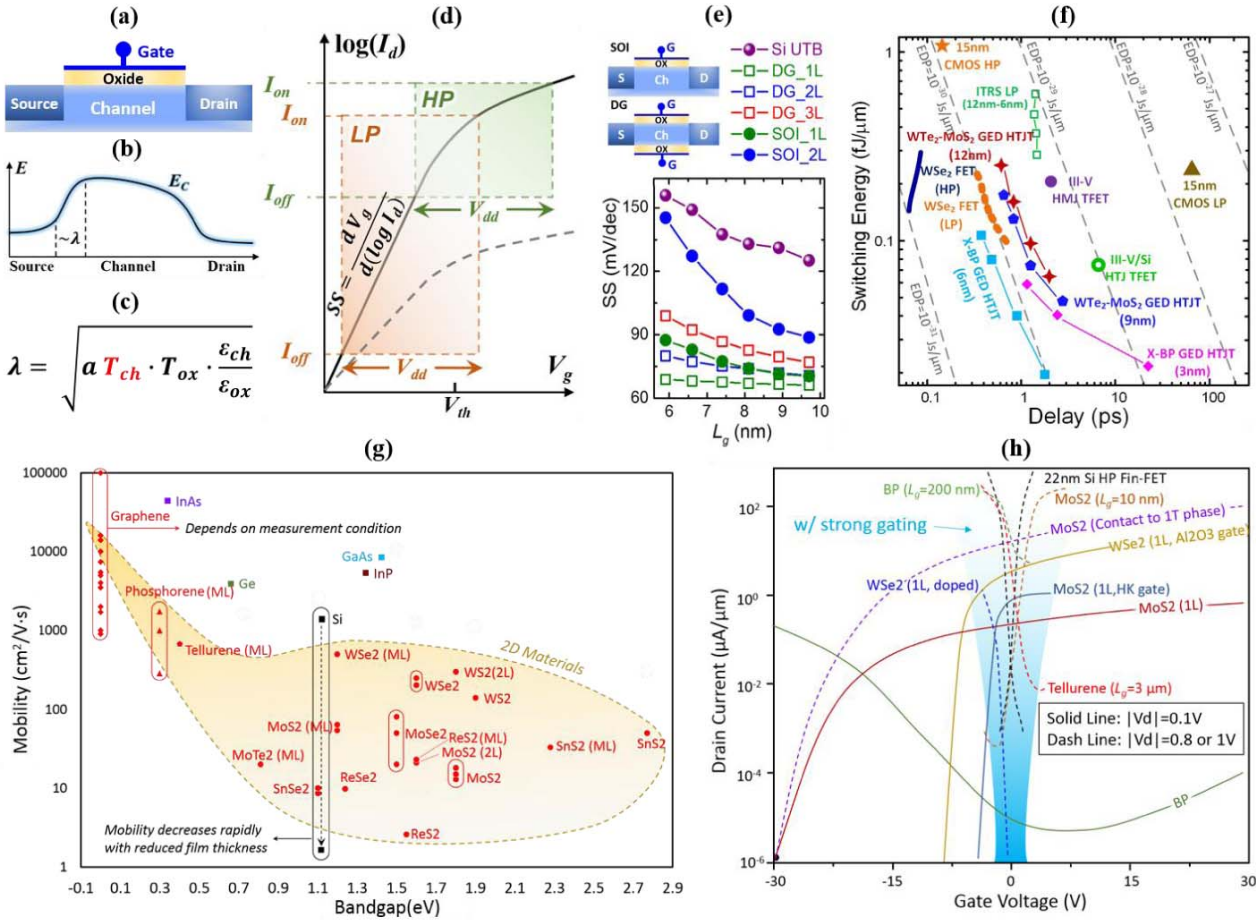

Fig. 2. (a) Typical FET structure. (b) Conduction band profile across source-channel-drain. (c) Formula of natural length λ. T_{ch} and T_{ox} are the thickness of channel and gate dielectric, respectively. $\varepsilon_{ox/ch}$ represent the respective permittivity values and α captures the gate topology (single/double/gate-all-around). (d) Transfer characteristics of FETs, and operation regions for HP and LP application. (e) Simulated SS versus L_g for MoS_2 FETs with different number of layers and device structures (SOI and DG). (f) Energy-delay benchmarking of 2-D-FETs and 2-D TFETs. GED represents gated Esaki diode. The detailed information about the devices included in this plot can be found in [22], [23]. (g) Collected mobility data from experiments for various 2-D materials as well as several typical bulk semiconductors [17]–[20], [26]–[30]. Those without "(ML)" mark represent their 1L forms. (h) Transfer characteristics of the state-of-the-art 2-D-FETs demonstrated so far. The 2-D materials not marked as "(1L)" represent ML forms. Curves in the shaded region are for devices with strong gating (equivalent oxide thickness, EOT $<$ 5 nm) [26], [30], [41], [51], [58], [59].

days were limited by large contact resistance [26], [31]–[33]. Extensive theoretical studies [34]–[38] were performed to demystify the nature of contacts between various metals and 2-D semiconductors, and valuable knowledge was derived to bring forward the role of van der Waals gap, d-orbitals in contact metals, and Fermi level pinning [34] due to interfacial alloy formation, based on which optimal metals could be identified for corresponding 2-D materials [37]. The obtained results are generally consistent with experimental results [26], [30], [39]. However, contacts to some specific 2-D materials, such as MoS_2, that suffer from the Fermi level pinning effect, cannot be fully optimized by selecting the proper contact metal only. To address this problem, "seamless contacts" were proposed [40] and implemented via phase engineering [41], in which the semiconducting 2H-MoS_2 was converted into metallic 1T-MoS_2, thereby lowering the contact resistance to 0.24 k$\Omega\cdot\mu$m, which is comparable with that of the state-of-the-art Si MOSFETs. However, more research efforts, such as using advanced passivation technique, are needed to stabilize the 1T-MoS_2 [42].

While the phase engineering on 2-D relies on converting a portion of the semiconducting channel into metallic, the junction between semiconducting and metallic part is still a Schottky junction, which will lead to ambipolar leakage current, and degraded SS. Therefore, suitable doping technique is still necessary to convert a Schottky barrier contact into a transparent ohmic contact, and lower sheet resistance in the S/D extension regions, thereby making a MOSFET, instead of a Schottky barrier FET [42]. There have been some efforts in this direction. For example, researchers introduced surface adsorbates, such as NO_2 [43] and metal particles [44]–[46] that can transfer charge to the 2-D layers, and achieved a degenerate doping level. However, due to the pristine surface of 2-D materials, surface adsorbates are usually unstable. Compared to the surface adsorbate approach, recently developed intercalation doping [47] is much more stable. The main limitations of this technique are the relatively long intercalation time

and irrelevance to 1L 2-D materials. Therefore, nontraditional approaches should be innovated for doping van der Waals materials.

Ultrascaled FETs need high-quality thin high-k (HK) dielectric to improve gate control [48]. The pristine surface of 2-D materials, although beneficial for carrier transport and gate control efficiency, makes the direct growth of high-quality thin gate dielectric on top of a 2-D channel challenging. The effective wetting layer has to be identified for corresponding 2-D materials. In fact, the best scenario is to develop 2-D layered HK dielectrics. The emerging perovskites have been found able to generate high capacitance in a capacitor structure, and thereby were proposed to serve as a gate dielectric for 2-D-FETs [49]. However, it remains unclear if thin perovskites in FET environment can provide the same capacitance, without introducing any hysteresis (memory effect of perovskites) into current–voltage curves. Recently, Chamlagain *et al.* [50] reported that 2-D insulating Ta_2O_5 thermally oxidized from TaS_2 has a dielectric constant of ∼15.5, and could serve as an effective gate dielectric on MoS_2, which is a positive step toward achieving 2-D dielectric with competitive dielectric constant with respect to HfO_2, although more efforts are needed to realize a transfer-free process for high-volume manufacturing.

There have been a few attempts to fabricate ultrashort channel (10-nm scale) 2-D-FETs [51], [52]. However, they either employed bottom gate structure or used electron-beam lithography (EBL) technique to define channel lengths. As well known, the bottom gate structure and/or EBL lead to low flexibility/yield, which limits their current use to prototyping and research. Recently, the first top-gated chemical vapor deposition (CVD) MoS_2 short-channel FET was demonstrated [53], [54] by employing Al_2O_3 wrapped metallic nanowire (NW) as a gate. This approach not only avoids EBL but also enables a gate-first self-aligned process for S/D formation. Further improvement efforts on this approach include advanced large-scale deterministic placement processes for NWs [55], [56]. It is interesting to note that almost at the same time, Desai *et al.* [57] claimed to have demonstrated a 1-nm gate-length MoS_2 FET back-gated with a single-wall nanotube (SWNT). While this paper demonstrated that channel charges in a FET can indeed be controlled with a gate electrode of 1-nm physical length, the demonstrated transistor is not a self-aligned structure (gate length and channel length are uncorrelated), which limits its utility in terms of addressing the transistor scaling problem. Moreover, the low DOS of SWNT is not ideal to drive high-DOS MoS_2 channel, and hence limits the device ON-current.

Fig. 2(h) shows transfer characteristics of the state-of-the-art 2-D-FETs made on various 2-D materials, as well as 22-nm Si HP Fin-FET [26], [30], [41], [51], [58], [59]. In general, there is still a long way to go before 2-D-FETs can compete with Si devices. Strong gate (shaded region) and short channel are required for 2-D-FETs to achieve good performance. Although BP and tellurene have high mobilities that translate to high ON currents, they suffer from low bandgaps (in ML forms) that limits the ON/OFF current ratio. WSe_2 appears to be a promising 2-D material for both n- and p-type device applications but needs more experimental exploration.

In order to enable 2-D-FETs for large-scale circuit exploration, a comprehensive compact model has been established [60], specifically for 2-D-FETs. This model (available on *nanoHUB*[1]) takes into account several practical issues in most experimentally demonstrated 2-D-FETs, including defects, mobility degradation, and insufficient doping density.

Although 2-D material channel can help to improve the FET electrostatics, SS is still limited by the thermionic lower bound of 60 mV/dec at room temperature. The pursuit of ultralow voltage operation without compromising performance [Fig. 2(d)] requires the involvement of subthermionic devices such as negative capacitance (NC) FET [61], electrostrictive FETs [62], and TFETs. Si *et al.,* recently integrated an NC layer into 2-D-FETs, and observed low SS [61]. In principle, a 2-D channel cannot provide sufficient charge density in the subthreshold regime to induce polarization charge in the NC layer, and hence gate voltage amplification, thus SS of a 2-D NC-FET cannot be low. Hence, the observed low SS cannot be attributed to NC effect. The 2-D electrostrictive FETs still require experimental justification. TFET performance has been below expectation for a long time, probably limited by the intrinsic properties of conventional bulk semiconductors. Detailed theoretical studies established the benefits of 2-D channel materials for designing TFETs [23], [40], [63]. Aided by these theoretical works, as well as understanding of interfaces to metal contacts [37]–[39], optimization of number of layers for improving ON current [30] and gate dielectrics [48] for 2-D semiconductors, we demonstrated the first 2-D-channel TFET that innovatively combined the mature doping process of bulk germanium as the source and the thin body/pristine interface of a 2-D material as the channel [64]. This vertical 3-D/2-D (Ge-MoS_2) heterojunction TFET exhibited an unprecedentedly low minimum SS of 3.9 mV/decade and average SS of ∼30 mV/decade over four orders of the drain current. These SS values have been confirmed to be achievable via rigorous band-tail analysis of 2-D semiconductors and various 2-D–2-D and 3-D–2-D heterostructures [65]. Although the first prototype 2-D-TFET exhibits low ON current, the steep SS can be effectively utilized in LP sensing applications [66], [10]. ON current can be improved via better heterojunction design and interface quality control.

Device reliability plays an important role in determining the aging profile of IC products. The reliability physics of 2-D-FETs has received some preliminary attention [67]–[70]. It was shown that imperfect dielectric environment (e.g., SiO_2) of 2-D channel introduced plenty of remote charge trap density, and resulted in large transfer characteristics hysteresis, low frequency noise [70], and bias temperature instability. The 2-D insulator, h-BN was identified [67] as an excellent dielectric, in terms of charge trap density, but the high temperature could lead to rapid charge trap generation in h-BN. More research is needed to understand the 2-D-FET reliability physics and suppress potential device performance degradation.

[1]https://nanohub.org/publications/51/1

B. Memory Devices

In addition to switching devices in logic circuits, FETs also serve as an access device for various memory elements, such as dynamic random-access memory (DRAM). Currently, the gate-induced-drain-leakage (GIDL) issue in Si-based DRAM technology sets a lower bound for the refreshing frequency, which translates to minimum unavoidable energy dissipation. Recently, the potential of using 2-D-FETs for access transistors of DRAM [71] was explored. It was shown that the relatively large bandgaps and suitable effective mass of several 2-D semiconductors such as MoS_2 and WSe_2 can effectively suppress GIDL while maintaining good current drivability. In the rapidly growing nonvolatile memory area, the floating gate transistor (FGT) still remains the main technology driver [72]. It is essentially a FET but with thicker gate stack and a floating conductor inserted inside the dielectric. The first 2-D FGT was demonstrated using MoS_2 channel and graphene floating gate [73]. Good retention and endurance were achieved. Subsequently, it was uncovered that WSe_2 channel aided by judicious design of HfO_2 gate stack and GNR floating gate not only effectively suppressed cell-to-cell interference thereby improving scalability but also greatly prolonged the state retention time [74].

Beside the FET structure, the memory cell can be as simple as a metal–insulator–metal (MIM) resistive RAM (RRAM) structure. Pan *et al.* [75] recently demonstrated an h-BN-based MIM RRAM cell. Although the mechanism of this device is not well articulated, such work reflects the possibility of more exotic 2-D memory innovations.

C. Radio Frequency and TeraHertz Application

As shown in Fig. 2(g), although the zero or small bandgaps of graphene, BP (ML), and tellurene (ML) prevent them from LP logic application, their high mobilities are highly desirable for radio frequency (RF) FETs [76], [77]. Graphene RF FETs were found able to operate at a frequency of several hundred gigahertz, and potentially up into the TeraHertz range [78], [79]. However, zero bandgap graphene channel introduces anomalous current saturation that affects the voltage gain, and also results in large leakage power, which could be a serious problem. In contrast, the semiconducting BP [80] and tellurene [29] RF FETs have the opportunity to achieve a balance between high-frequency operation and reasonable leakage power. More research efforts are needed in terms of reducing the contact resistance and other parasitic effects, which are equally important for RF devices.

D. Sensing Application

FET-based sensing devices are of high interest to the Internet-of-Things community, due to the LP operation and low cost enabled by the mature very large scale integration technology. Sensitivity is obviously the most important metric for sensors. It has been found that the sensitivity of a FET biosensor exponentially depends on its SS [66]. This inspired the demonstration of a MoS_2-based pH sensor achieving sensitivity as high as 713 for a pH change by 1 unit along with efficient operation over a wide pH range (3–9) [81]. Ultrasensitive and specific protein sensing was also achieved with a sensitivity of 196 even at 100 femtomolar concentration. What is more important is that FET-based sensors can benefit from the high scalability of 2-D-FETs. In other words, the 2-D-FET-based sensor can be scaled without compromising its sensitivity, which is highly desirable for single molecular detection. The sensitivity can be further improved by employing 2-D-TFETs, thanks to their subthermionic SS [10].

E. Memristors and Neuromorphic Computing

Neuromorphic application-specific-integrated-circuits (ASICs) are being developed by many industrial entities to fit the forthcoming artificial intelligence (AI) era and provide better performance with lower power consumption [82], [83]. However, the fundamental progress relies on the innovation of materials and device technology that enables complicated computing performed with a smaller footprint and lesser power. Memristive devices are promising artificial neuron devices for neuromorphic computing and machine learning applications [84]. The largest applications of neuromorphic computing are image processing and recognition, i.e., the "eyes" of AI. For human eyes, the neurons are not only light sensing devices but also include an image processor [85], [86]. A light-sensitive memristor is crucial to mimic the functionality of eyes. On the other hand, a light-sensitive memristor can be used as the synapses to receive an optical light pulse for the electrical neural network [87]. 2-D materials, due to their atomically thin body, can be used to fabricate ultrafine structure for precise functionality. Recently, it has been demonstrated that it is possible to create large arrays of quantum dot superlattices on 2-D semiconductor materials by patterning with electron-beam irradiation [88]. 2-D materials are extremely sensitive to any change of charges due to the ultrathin body, thus the charge stored in the quantum dots can be sensed even at room temperature and thereby recreate the mechanism of neuron membrane. It has been shown that FETs made with precisely designed quantum dot superlattice on single-crystal 1L MoS_2 can function as synapses that work at room temperature and exhibit a memristive short-term plasticity to light stimulation [89].

IV. 2-D Interconnects

Interconnects are essential components in circuits and systems for signal routing and power delivery. In this section, interconnect scaling challenges and recent progress [Fig. 3(a)] in emerging graphene-based interconnects are discussed.

A. Interconnect Scaling

The scaling down of transistors increases the circuit integration density and performance. The interconnects, especially local interconnects, are also required to scale down for connecting the transistors. As the interconnect dimension scales down, the resistivity of Cu interconnects, with cross-sectional dimensions of the order of the mean free path of electrons in current and imminent technologies [90], is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering, and the presence of a highly resistive diffusion barrier layer [91], [92]. The steep rise in

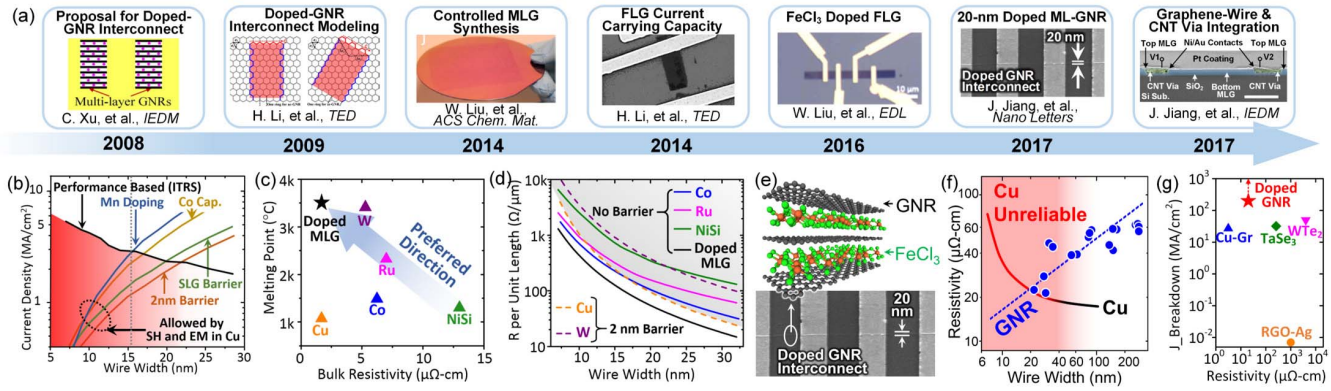

Fig. 3. (a) Progress in graphene interconnects research summarized in chronological order. GNR, MLG, FLG, ML-GNR, and CNT represent graphene nanoribbon, multilayer graphene, few-layer graphene, multilayer-GNR, and carbon nanotube, respectively. (b) Circuit-performance driven current density and maximum allowed current density for Cu interconnects with 2-nm TaN barrier, 1L graphene barrier, Co capping, and Mn doping. The red region indicates that the required current density exceeds the maximum allowed current density as interconnect scales down. (c) Material melting point versus bulk resistivity for bulk materials including nickel silicide (NiSi), Cu, Co, Ru, W, and doped MLG. (d) Estimated resistance per unit length versus wire width for Cu and W (with 2-nm barrier) and Co, Ru, NiSi, and doped MLG (without a barrier). (e) Schematic of $FeCl_3$ intercalation doped ML-GNR and SEM image of a 20-nm wide doped ML-GNR interconnects. (f) Measured doped ML-GNR resistivity and estimated Cu resistivity for similar dimensions. Red region indicates that the Cu wires suffer from severe self-heating (SH) and EM. The doped ML-GNR resistivity decreases with width because the narrower ML-GNRs are doped more efficiently (due to easier diffusion of the intercalates for narrower widths) so that the conductivity degradations from edge scatterings and bandgap opening are compensated [107]. (g) Reported wire resistivity versus breakdown current density of reduced-graphene-oxide-Ag composite (RGO-Ag), MLG-capped Cu (Cu-Gr), semi-metallic ML-WTe_2 (with line widths $\geq 2\mu m$), metallic $TaSe_3$ (100 nm), and doped ML-GNR (20 nm).

resistivity of Cu interconnects increases interconnect delay at both the global level and the local level [93]. More importantly, the rising Cu resistivity also poses a reliability concern due to Joule heating or self-heating (SH) induced significant metal temperature rise [91]. The large metal temperature rise, which exponentially degrades interconnect electromigration (EM) lifetime, severely limits the maximum current-carrying capacity of scaled Cu interconnects [90], [91], [93] [Fig. 3(b)]. In addition, it is becoming increasingly difficult to avoid the formation of voids in Cu interconnects during Damascene process beyond 14-nm node with TaN Cu-diffusion barrier. These voids can further increase the Cu interconnect resistance and aggravate the EM effects [93]. Other materials, including Co [94], [95], Ru [96], and NiSi, have been identified as possible candidates for replacing Cu. However, they either cannot meet the current-carrying capacity requirements at scaled dimensions or have significantly higher resistivity with respect to Cu. [Fig. 3(c) and (d)]. Hence, there is a critical need to identify a new interconnect material.

In the nanocarbon family (including CNTs and graphene), graphene in addition to its fascinating electrical, mechanical, and thermal properties (including high melting point), also has planar structure that allows easy patternability instead of using the complex Damascene process necessary due to the difficulty to etch Cu, and does not require any barrier layer that is necessary for Cu, which makes it very attractive for next-generation interconnects and passives [97], [98].

B. Graphene Nanoribbon Interconnects

For interconnect application, multilayer graphene (MLG), as opposed to 1L graphene, is preferred to lower its resistance [97]. It has been established that MLG exhibits high current-carrying capacity (>100 MA/cm^2) [99], due to its strong sp^2 covalent bonding, compared with metallic bonding in Cu. By patterning MLG into ribbons of less than 100 nm widths, one can obtain ML-GNRs that exhibit similar dimensions as back-end-of-line (BEOL) Cu wires in the state-of-the-art CMOS technology and high current-carrying capacity [100]–[104]. GNR-based interconnects are also promising to serve as the skeleton of the future "all 2-D" circuits [11].

Although the ML-GNRs have also been shown to exhibit high breakdown current density and high resistance to electromigration, the electrical conductivity of these ML-GNRs is about one to two orders of magnitude lower than that of BEOL Cu wires, due to low electron/hole concentration and edge scattering. Xu *et al.* [105] first proposed the use of intercalation doping to increase ML-GNR electrical conductivity, and theoretically proved that doped ML-GNRs can outperform Cu wires [106]. The intercalation doping increases carrier concentration in MLG/ML-GNR by charge transfer between the intercalation dopant and graphene/GNR and thereby boosts its electrical conductivity [106]–[108]. Follow-up experiments demonstrated $FeCl_3$ intercalation doped GNR interconnects [Fig. 3(e)] with comparable resistivity with respect to Cu [Fig. 3(f)] while providing $>20\%$ circuit performance improvement along with $>70\%$ energy savings for global wires due to the significantly lower parasitics of doped GNR due to their thinness [107] and >40-folds reliability improvement [109]. Note that other emerging interconnect materials, including graphene-Cu composite, $TaSe_3$, and WTe_2, have been reported. However, their electrical conductivity and current-carrying capacity cannot beat those of doped graphene/GNRs [Fig. 3(g)].

Unlike metals, which can be deposited by electroplating at around room temperature, high-quality MLG growth requires high-temperature (>850 °C) CVD process [110], which violates BEOL thermal budget, and also requires use of metal catalyst substrate. Attempts toward low-temperature direct graphene growth on dielectrics have been reported by plasma-enhanced CVD [111] and remote catalyzation [112],

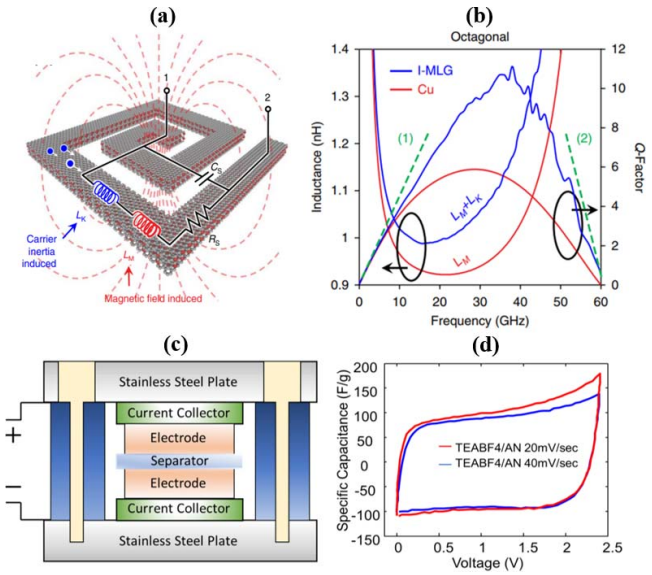

Fig. 4. 2-D passive devices. (a) Schematic of an inductor showing kinetic and magnetic inductance. (b) Inductance and *Q*-factor comparison of intercalated-MLG (I-MLG) and Cu inductors with octagonal geometry. Green dashed lines represent (1) upper limit of Q-factor and (2) substrate loss, self-resonance and skin effects at high frequencies. (c) Schematic of a supercapacitor [116] fabricated with chemically modified graphene (CMG) for electrodes. The separator is an electrolyte. (d) *CV* plot of CMG material with tetraethylammonium BF4 electrolyte in acetonitrile. The figure shows two plots, each obtained for different scan rates of 20 and 40 mV/sec. Images in (a), (b) and (c), (d) are adapted from [114] and [116], respectively.

but they cannot satisfy the BEOL thermal budget. Moreover, although contacts to doped ML-GNR with low contact resistance [107] and high current-carrying capacity [109] has been demonstrated, the process integration of multi-level ML-GNR interconnects is challenging. Inspired by the idea of seamless contacts between graphene interconnects and GNR-FETs [40], Jiang *et al.* [113] recently demonstrated a graphene wire and CNT via integration scheme employing a nickel–carbon alloy contact [Fig. 3(a), right-most panel].

V. 2-D Passive Devices

Compared to active devices, passive devices (inductors and capacitors) in ICs have not scaled proportionately with scaling of the technology node. This is because of the requirement of large surface areas in these devices, which dictate and finally limit the maximum value of attainable inductance/capacitance. A recent breakthrough in the form of the first kinetic inductor [114] [Fig. 4(a)] has tremendous potential in alleviating the scaling issue of inductors, by exploiting a unique 2-D materials design, thereby making it possible to demonstrate a substantial value of kinetic inductance at room temperature and overcome a 200 years old limitation of the original design of inductor (by Michael Faraday) that relied on the magnetic inductance alone [115]. This large kinetic inductance essentially increases the overall inductance because it acts in series with the magnetic inductance. The invention involves MLG intercalated with bromine, which promotes weak interlayer interactions, thereby decreasing the momentum scattering rate leading to a high value of kinetic inductance at room temperature. This allows achieving a material with the highest inductance-density ever made or in other words, achieving the same inductance density as a conventional inductor at only one-third of the total area. The high value of inductance in conjunction with the reduced resistance in intercalation doped MLGs compared to conventional metallic interconnects yield high values of the *Q*-factor [Fig. 4(b)]. This invention has far-reaching implications in shifting the entire paradigm of how conventional RF circuits are designed today. In addition to this, as demonstrated in [107], MLG possesses high electrical conductivity, thermal conductivity, current tolerance, and mechanical strength, which enable it in being very reliable while handling high current density. Immediate practical use of the kinetic inductors includes applications in astronomy (as kinetic inductance detectors), integrated voltage regulators in advanced microprocessors, and radio-frequency identification (RFID), to applications in the emerging Internet of Things (IoT) paradigm such as, wireless sensors for vapor, humidity, heat, and water quality detection, wireless bacteria detection in the human body including tooth enamel and skin - as transmitter/receiver components such as voltage controlled oscillators and low-noise amplifiers. The main challenge of using graphene as on-chip inductors is the synthesis compatibility of MLG with current IC process technology, as already discussed in the previous section.

In addition to inductor scaling, scaling of the capacitor is also a prerequisite as transistor pitches scale down. This is because a smaller capacitor would help in reducing the footprint of the entire circuit. This capacitance scaling is enabled by finding solutions to increasing the obtained capacitance per unit area. Recently, there has been much interest in the use of supercapacitors, which not only typically offer 10–100 folds more energy per unit volume than electrolytic capacitors but also can accept and deliver charge faster than batteries and tolerate many more charging and discharging cycles. These supercapacitors generally use carbon and its derivatives as electrodes [116], and this could be particularly useful in DRAM circuits where it could help in reducing the footprint while simultaneously increasing the total capacitance, thereby increasing the charge retention capacity and decreasing the refresh rate. Supercapacitors can be generally classified into two main categories based on the mechanism of the energy storage—electrical double layer capacitors (EDLCs) and pseudocapacitors [117]. In EDLCs [Fig. 4(c)], since the capacitance is realized by the accumulation of charges at the electrode–electrolyte interface; electrodes with the high surface area, pore size, and good electrical conductivity are suitable choices. Capacitance in pseudocapacitors is realized by transferring faradic charges between electrodes and electrolytes by reversible multielectron faradic reactions.

The requirement of a porous electrode with the high surface area to volume ratio and low equivalent series resistance make graphene the most attractive choice for use in supercapacitors among all available materials to date [Fig. 4(d)] [118]. Graphene has the highest surface-volume ratio among all carbon allotropes. The normalized surface area of a single graphene sheet is 2675 $m^2 \cdot g^{-1}$ [117], essentially setting the upper limit for all carbon materials. Yang *et al.* [118] recently reported graphene supercapacitors with high power and energy densities, a Coulombic efficiency of 97.5% and

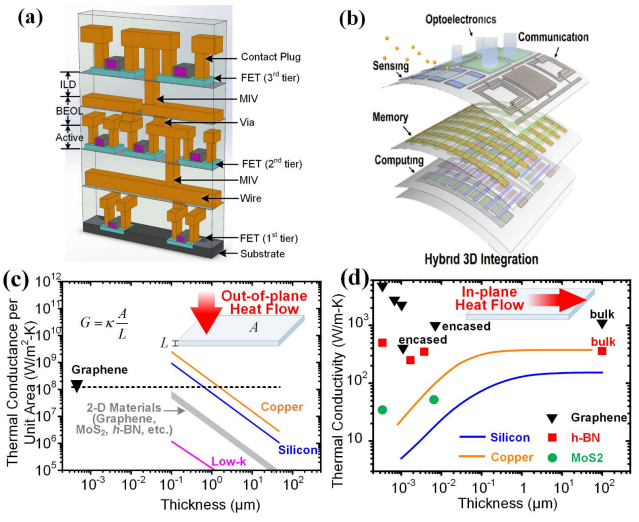

Fig. 5. (a) Schematic of M3D integration. Each tier consists of the inter-layer dielectric layer, BEOL layer, and active device layers. (b) Schematic of M3D integration of 2-D logic computing circuits, memories, sensing circuits, and optoelectronics and communication circuits. (c) Out-of-plane thermal conductance per unit area for 1L graphene and bulk materials. In the inset equation, G, k, A and L are the actual thermal conductance, thermal conductivity, area, and length along the heat transport direction, respectively. Ideal interfaces between silicon/copper and surrounding dielectric are assumed in the simulations. The out-of-plane thermal conductance for bulk materials with $<$ 100 nm thickness is not plotted because of the lack of rigorous heat transport theory at those dimensions. (d) In-plane thermal conductivity versus film thickness for bulk materials (silicon and copper) and 2-D materials. In (c), the thermal conductance of 2-D material (graphene) is dominated by the interfaces, whereas that of bulk materials (copper, silicon, and low-k) consists mainly of bulk thermal conductance. In (d), 2-D materials are suspended samples by default unless marked as "encased" (by SiO_2).

large charge and discharge cycles (7000 while still retaining 100% capacitance), which makes these devices attractive in the foreseeable future. Although there are significant benefits of using supercapacitors, their inability to withstand high voltages, higher production cost, and limited scalability (due to requirements of liquid electrolytes and large electrode surface area) remain as challenges for their application options.

VI. Monolithic 3-D Integration With 2-D

3-D integration stacks devices and circuits vertically and has been studied as a solution for increasing integration density, reducing power and signal path latency, and achieving heterogeneous integration [119]. Through-silicon-via (TSV) based 3-D integration fabricates all tiers in parallel and then stacks them by a bonding process. TSVs connect adjacent Si layers and possess large dimensions [120], [121], compared with standard BEOL vias in the planar technology, thereby creating large parasitic capacitance and thermal/mechanical stress in the Si layers. Monolithic 3-D (M3D) integration fabricates multiple stacked tiers sequentially on the same wafer [Fig. 5(a)]. Monolithic inter-tier vias (MIVs) connecting adjacent tiers are much smaller than TSVs or even Through-oxide-vias (TOVs) [122], and allow higher MIV placement density, thus offering more design flexibility.

The most critical challenge of M3D integration is low-process thermal budget [123], in which the process temperature of the upper layers should not exceed a critical temperature (~500 °C). Unfortunately, the fabrication of the upper layers usually has to consist of high-temperature processes such as silicon crystallization and dopant activation. The other critical challenge is thermal/self-heating issue [124]. Although M3D integration mitigates the overheating problem by employing thinner tiers that provide smaller thermal resistances, it also creates strong tier-to-tier thermal coupling, which exacerbates the thermal problem [124]. Furthermore, in scaled technology nodes, where subthreshold leakage results in a significant amount of a chip's total power consumption [125], the stronger thermal coupling in M3D aggravates the subthreshold leakage problem, which can further aggravate the thermal problem [126], [127].

The low SS of 2-D-FETs enables a weak dependence of leakage current on temperature rise due to self-heating [128] thus making it an ideal candidate for M3D integration. The out-of-plane thermal conductance of 2-D layered materials is small w.r.t conventional bulk materials (e.g., Si and Cu) due to the presence of vdW gaps in the out-of-plane direction. Moreover, for 1L or FL/ML 2-D materials, the out-of-plane thermal conduction will be dominated by their interfaces to the surrounding materials because of their atomically thin bodies. However, the vertical thermal resistance in M3D is dominated by dielectrics, which exhibit lower out-of-plane thermal conductance w.r.t 2-D materials because of their larger thickness [Fig. 5(c)]. 2-D devices significantly reduce M3D stack thickness, thus minimizing the effective thermal resistance and self-heating of the upper tiers. On the other hand, 2-D materials exhibit excellent in-plane thermal conductivity [Fig. 5(d)]. The thermal conductivities of bulk materials decrease as the thickness decreases due to phonon (or electron in metals) boundary scatterings caused by surface roughness and interface defects [129]. The thermal conductivity degradation also occurs in copper thin films, where heat transport is mainly contributed by electrons [130]. In 2-D materials, such thermal conductivity degradation is not severe, and high in-plane thermal conductivity helps lateral heat spreading and removing hotspots in M3D ICs.

The M3D integration of 2-D layered materials and devices was first proposed by Banerjee *et al.*, [131] and analyzed by Jiang *et al.* [132]. Recent progress on integrating ML (3–7 nm thickness), 2-D devices has been reported by using exfoliated ML MoS_2 and WSe_2 [133]. For practical M3D integration, a wafer-scale transfer of synthesized 2-D materials or a low-temperature direct growth of 2-D materials on dielectric substrate is preferred. Although large area synthesis of 2-D materials on dielectrics has been achieved by CVD at 550 °C [20] and by atomic layer deposition at 300 °C, low-temperature wafer-scale high-quality 2-D material growth remains a challenge. Given the wide variety of 2-D devices, including logic devices [26], nonvolatile memories [73], sensors [81], [46], and passive devices [114], a hybrid M3D integration of logic computing, memory, sensing, optoelectronics, and communication circuits [Fig. 5(b)] can be envisioned [131].

VII. 2-D Material Synthesis

The capability of synthesizing high-quality and large-scale 2-D material is a prerequisite for commercializing 2-D elec-

TABLE II
SUMMARY OF THE PROS AND CONS OF EXISTING SYNTHESIS APPROACHES FOR 2-D MATERIALS

	Synthesis Method	Pros	Cons
Top-down	Mechanical Exfoliation	• High crystallinity and high mobility • Low defect density • Low cost • Applicable for various 2-D layered materials	• Not scalable (~ μm scale) • Non uniform area • No thickness control • Poor yield • Limited to lab-scale usage
	Liquid Exfoliation	• Large-scale production of nanosheets • High-yield • Inexpensive process	• Difficult to produce thin layers • Low crystallinity • Limited applications (e.g., catalysis and electro-chemical storage) • Extrinsic defect formation during the exfoliation process • No thickness control • Solution based process
Bottom-up	CVD (Chemical Vapor Deposition)	• Large size of single crystal growth on catalytic/dielectric/plastic substrates • Large-scale growth • Versatile growth process (Heterostructure & Superlattice growth) • Easy doping process	• Inhomogeneous grain sizes and crystal quality • No defect control • No controllability of precursors • Non-uniform layer thickness • Relatively high-temperatures (~700-1100 ^{0}C)
	MOCVD (Metal Organic-CVD)	• Large-scale and uniform growth • Easy control of precursor delivery • Stoichiometric control	• Complex design of precursors • Toxic environment • High-cost process • Carbon impurities from the metal organic precursors • Slow growth rate • Limited grain size (5-8 μm)
	ALD (Atomic Layer Deposition)	• Self-limiting process - Ideal for monolayer • Lowest temperature growth process • Wafer scale growth • Precise thickness control	• Poor crystallinity (post-annealing process required) • Small grain size (sub-10 nm range) • Non- precise control of precursors due to dangling bond free surface of 2-D TMDs
	MBE (Molecular Beam Epitaxy)	• High purity • High crystallinity • In-situ growth process	• Small domain size • Limited coverage • Non-controllable thickness or number of layers • Slow and expensive process

tronics in the future. So far, great progress has been achieved in terms of realizing layer controllable wafer-scale synthesis [110], [134], as well as various heterojunctions [135] for novel functionalities achievable beyond those with homogeneous materials. Extensive efforts are still in demand, such as increasing the single-crystal size and lowering synthesis temperature to make it CMOS compatible. Table II summarizes the pros and cons of existing synthesis approaches for 2-D materials. Due to the space limitation of this paper, readers are referred to recent review articles reporting the status of 2-D material synthesis [135], [136].

VIII. CONCLUSION

This paper provided a comprehensive overview of the most exciting accomplishments in 2-D nanoelectronics to date and identified the remaining challenges that need to be overcome for employing 2-D van der Waals materials in next-generation nanoelectronics. More specifically, we highlighted the prospects of 2-D materials for a number of applications uniquely enabled by them—from active nanodevices in the form of FETs and their derivatives (memory, sensor, and memristor), to passive elements—interconnects, inductors, and capacitors, as well as innovative chip architecture in the form of monolithic-3D integration with 2-D layered materials, which can serve as a unique platform to incorporate emerging 2-D materials in next-generation electronics.

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