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# High Performance Pulse Ring Voltage Controlled Oscillator for Internet of Things

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**Abstract**—This paper presents a low phase noise, low power, wide tuning range, small area pulse ring oscillator fabricated in inexpensive 130nm CMOS technology, suitable for the widescale internet of things market. The ring uses very non-linear Pulse gates instead of conventional inverters as buffers substantially reducing the impulse sensitivity function (ISF) and thus the phase noise. The timing signal is rising-edge and ground referenced, allowing the supply to be used as control voltage. Common mode supply noise is rejected by double inversion in every stage of of the pulse gate as well as insensitivity to pulse amplitude and width. Fabricated ring oscillators show a phase noise of  $-98.41$  dBc/Hz at 1MHz offset for 1.872GHz oscillator at 2.94mW power consumption and  $-95.14$ dBc/Hz at 1MHz offset for 388MHz oscillator at 216uW power consumption. The oscillators have a tuning range of 388MHz to 2.455GHz.

## I. INTRODUCTION

Distribution of high frequency, low jitter, timing over long distances is costly, motivating small localized synchronizing oscillators that maintain some global coherence relation. Internet of things needs a huge number of low phase noise, cheap (low area and cheap technology), voltage controlled oscillators to synchronize the behavior of intermittently connected elements.

This oscillator is based on pulse-gates which have high timing repeatability and have been used in high performance serial links [1]. The design of the circuit results in sensitivity only to the rising edge rate (not the amplitude or pulse width once the trigger threshold is reached). Further, the output pulse width is not sensitive to the input width. These properties act to reduce the root mean square value of Impulse Sensitivity Function [2], resulting in substantial phase noise improvement over inverter and linear amplifier based delay elements. Further, the signals are buffered (double inversion) [3] leading to better high frequency supply noise rejection. Pulse-gates have asymmetric ISF and thus exhibit slightly higher flicker phase noise sensitivity. Conventionally, VCO's are phase locked to mitigate such low-frequency noise. Integrated charge based input threshold control [4] rejects random small charge spurs from ground.

## II. CONCEPTS AND CIRCUITS

Pulse gates have the circuit design shown in Figure 1. The gates are connected as shown in Figure 2 making a simple ring oscillator. An 'OR' pulse-gate has 2 pull down NMOS instead of a single one and the extra input is used to start the pulse in the ring.

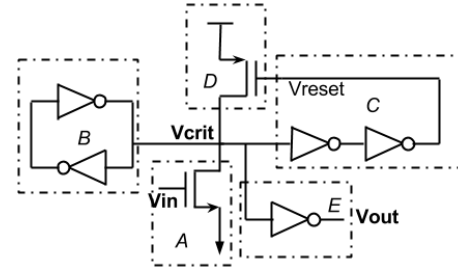


Fig. 1: Pulse-gate Topology: (A: Vin : Input Pull-Down Vcrit; B: Threshold Control : Schmidt trigger; C: Reset Loop : Sets Pulse Width; D: Pull Up : Restores Vcrit on Reset; E: Vout : Output Buffer)

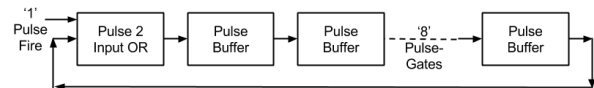


Fig. 2: Pulse Ring Oscillator with a ring of '8' Gates

## III. RESULTS

In the fabricated oscillator shown in Figure 3, a ring of 8 gates is started with an external pulse. The oscillator frequency shows a linear behavior with supply as control voltage as shown in Figure 5.

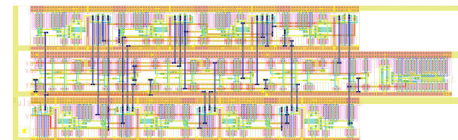


Fig. 3: Layout of Fabricated Oscillator (60umX20um)

The measured phase noise performance for the oscillator is shown in Figure 6. Phase noise is better than  $-95$ dBc/Hz @ 1MHz offset across the operating range of 388MHz to 2.455GHz. It deteriorates below 0.6V in the current design. Two figures of merit have been used for oscillator comparison with the other (free-running) ring oscillators.  $FOM_1$  compares the phase noise and power consumption of the oscillators and is defined in Equation 1 ( $\Delta f$  refers to the phase noise measurement offset,  $f_o$  refers to the measurement frequency and  $P_o$  refers to the DC power

TABLE I: Fabricated Ring Oscillator Performance Comparison

Ref	Technology	Phase Noise	Power	Measurement Frequency	Tuning Range	$FOM_1$	$FOM_2$	Status
This Work	130nm	-98.41dBc/Hz @ 1MHz	2.94mW	1.872GHz	0.388-2.455GHz	159.16dB	178.38dB	Tested
[5]	350nm	-126dBc/Hz @ 10MHz	7.48mW	866.521MHz	0.381-1.15GHz	156.0dB	170.9dB	Simulated
[6]	350nm	-116dBc/Hz @ 10MHz	42.9mW	-	0.92-0.925GHz	138.9dB	110.0dB	Tested
[7]	180nm	-105dBc/Hz @ 1MHz	-	1.81GHz	1.1-1.86GHz	-	166.9dB	Tested
[8]	180nm	-106.1dBc/Hz @ 0.6MHz	65.5mW	900MHz	0.73-1.43GHz	151.5dB	169.3dB	Tested
[9]	180nm	-89.79dBc/Hz @ 0.6MHz	16mW	850MHz	0.394-1.14GHz	140.8dB	158.4dB	Simulated
[10]	130nm	-91.5dBc/Hz @ 1MHz	0.44mW	-	0.4-0.433GHz	147.1dB	121.9dB	Tested
[11]	90nm	-90 dBc/Hz @ 0.6MHz	16.8mW	1.74GHz	1.57-3.57GHz	147.0dB	161.4dB	Simulated

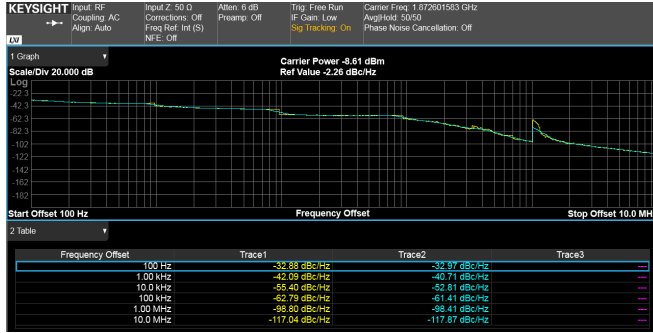


Fig. 4: Measured Phase Noise@1MHz for freq.=1.872GHz at 1.2V Supply

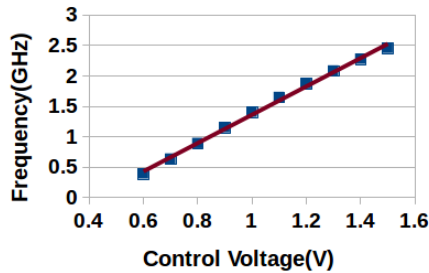


Fig. 5: Control Voltage-vs-Operating Freq.: Linear Behavior

consumption).  $FOM_2$  (defined in Equation 2, where  $f_{max}$  and  $f_{min}$  refer to the maximum and minimum frequency in the tuning range respectively) accounts for tuning range along with phase noise. It can be seen in Table I that this work outperforms all the tested and simulated related VCOs in both figure of merits.

$$FOM_1 = 20\log\left(\frac{f_o}{\Delta f}\right) - PN - 10\log\left(\frac{P_o}{1mW}\right) \quad (1)$$

$$FOM_2 = 20\log\left(\frac{f_o}{\Delta f}\right) - PN + 20\log\left(\frac{f_{max} - f_{min}}{f_{min}}\right) \quad (2)$$

#### IV. CONCLUSION

The oscillator design presented in this paper achieve very low phase noise characteristics by exploiting the non-linear switching behavior of pulse-gates. The designs are inherently less sensitive to power and thermal noise sources than conventional designs allowing for low-power, inexpensive

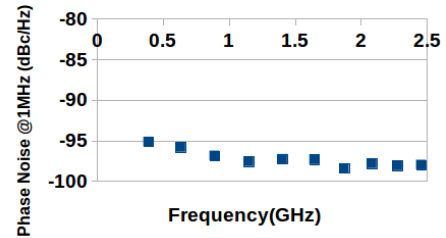


Fig. 6: Phase Noise@10MHz-vs-Operating Frequency

integration in battery and intermittently powered and synchronized IOT applications.

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