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Nanopillar Emitters: Photonic Crystals, Heterostructures, and Waveguides

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Nanopillar Emitters: Photonic Crystals, Heterostructures, and Waveguides

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requirements for the degree Doctor of Philosophy

in Electrical Engineering

By

Adam Christopher Scofield

2015

ABSTRACT OF THE DISSERTATION

Nanopillar Emitters: Photonic Crystals, Heterostructures, and Waveguides

by

Adam Christopher Scofield

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2015

Professor Diana L. Huffaker, Chair

Compound semiconductors, which consist mostly of column III and column V elements, are widely used in opto-electronic devices such as light-emitting diodes, lasers, and solar cells. Thin-film, one-dimensional III-V devices are a mature technology used in industrial and commercial applications. Because of this, there is little left to explore in one-dimensional structures to improve device performance significantly, with advances usually attributed to improvements in fabrication and production volume.

In order to further explore the possibilities of compound semiconductors, research has to led to the development of nanowires and nanopillars. These nanostructures, with diameters ranging from 10 - 100 nm and lengths of several micrometers, are synthesized in a bottom-up approach, rather than being etched with standard nanofabrication techniques. This approach allows researchers to develop unique three-dimensional structures with differing III-V

compositions in order to make transformational, rather than incremental improvements in device performance. The ability to control III-V synthesis in three-dimensions has led to numerous demonstrations of opto-electronic devices with broad applications in solid-state lighting, medical sensing, spectroscopy, and telecommunications.

In this dissertation, nanopillar-based emitters, particularly in the near-infrared, are explored. The fundamental motivation behind this work is the ability to directly grow GaAs and InGaAs nanopillars on Si (111) substrates without dislocation defects, making them promising for applications such as low-power lasers for optical interconnects. We begin with an analysis for the needs of a laser design to reach power levels necessary for chip-scale optical interconnects. This sets the direction for research on nanopillar-based emitters. First, the photonics of nanopillar arrays are explored, which led to the demonstration of photonic crystal cavities and photonic crystal lasers. Then, the fabrication of electrically-driven nanopillar emitters is demonstrated and used to develop advanced heterostructures for current injection and carrier confinement. Finally, we show the monolithic waveguide integration of nanopillar devices and effective coupling between a single-mode optical fiber and nanopillar device, paving the way for future development of nanopillar lasers for optical interconnects.

The dissertation of Adam Christopher Scofield is approved.

Robert N. Candler

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University of California, Los Angeles

2015

This thesis is dedicated to my friends and family.

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- **A.C. Scofield**, J.N. Shapiro, A. Lin, A.D. Williams, P.S. Wong, B. Liang, D.L. Huffaker "Bottom-up photonic crystal cavities formed by patterned III-V nanopillars", *Nano Letters*, 11(6), 2242-2246
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- **A.C. Scofield**, D.L. Huffaker, "Monolithic waveguide integration of nanopillar photonic devices", *Semiconductor and Integrated Optoelectronics*, 2014 **(Invited)**
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- **A.C. Scofield**, S-H Kim, J.N. Shapiro, A. Lin, B. Liang, A. Scherer, D.L. Huffaker, "Room-temperature continuous-wave lasing in nanopillar photonic crystal cavities", *Conference for Lasers and Electro-Optics*, 2012
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Patents and Intellectual Property

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- **A.C. Scofield**, D.L. Huffaker, "Axial GaAs/GaAsP nanopillar heterostructures grown by selective-area MOCVD", U.S. Provision Patent No. 62/019,231
- **A.C. Scofield**, A. Lin, D.L. Huffaker, " Hybrid Si/III-V nanopillar optoelectronic devices", U.S. Provision Patent No. 62/019,234

Chapter 1

1.1 Overview

For more than a decade, researchers across the field of photonics have strived to achieve optical interconnects within and between silicon chips[1]. While forming an effective detector based on epitaxial Germanium was developed early on[2–5], there is still a strong need for a light-emitting device on Silicon. The advent of high-efficiency vertical cavity surface emitting lasers (VCSELs) and flip-chip bonded InGaAsP lasers on silicon-on-insulator (SOI) substrates[6,7] has enabled high-speed active optical cables to increase bandwidth and reduce power consumption in computer clusters. However, as scaling in electronics increases, the demand for higher bandwidth between processors and lower power consumption per bit is also increasing[8,9]. To address this problem, many companies and researchers have been working towards pushing optoelectronic transceivers on chip.

While the power requirements in terms of femto-joules-per-bit have been well established for optical interconnects for intra- and inter-chip communications[9], there is a void in literature as to the actual requirements these numbers place on the design of lasers that can operate at this extremely low power level. For optical interconnects to be viable for inter- and intra-chip communications, it is well known that the system power dissipation needs to be on the order of 10 fJ/bit or less. Even though a large body of research exists for micro/nano lasers aimed at this application, an analysis of the actual laser device requirements that are necessary to make these systems practical is absent from literature. In this chapter, we analyze a basic optical interconnect based on the state-of-the-art reported values for the various components, and determine the laser design requirements in terms of cavity Q, active area, carrier lifetime, and thermal dissipation.

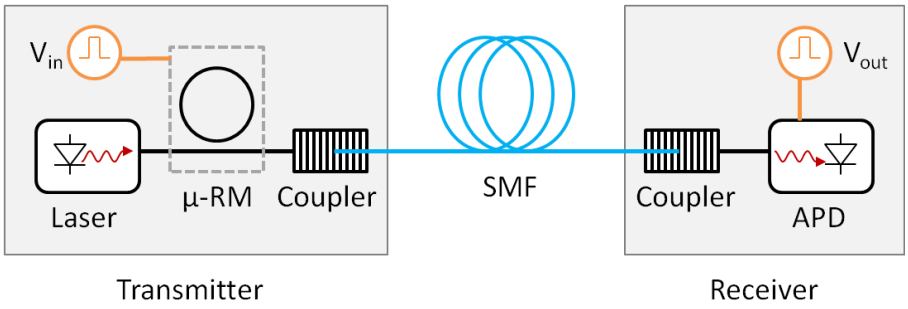

Fig. 1. Schematic of the optical system for a single channel. Whether the complete system uses multiple fibers or wavelength division multiplexing, each laser will have to power the photodetectors through these same basic components.

1.2 System Analysis of Optical Interconnects

In order to make a realistic set of input and output power requirements for the next generation lasers, a basic system analysis of the optical interconnect is necessary. While the driver electronics for the lasers are quite complicated, the actual optical system is relatively simple. Figure 1 shows a schematic diagram of the system for a single transmission channel. The systems consists of five components: (i) laser, (ii) modulator, (iii) waveguide-to-fiber couplers, (iv) optical fiber, and (v) photodetector. The input power of the laser is the target energy per bit minus the energy per bit consumed by the modulator. The output power of the laser is set by the photodetector sensitivity plus the optical loss of each of the components between the laser and detector.

A. Silicon Micro-ring Modulators

The most compact and lowest energy consumption modulators on the silicon platform are microring modulators[10–12]. The fundamental operating principle of these devices is plasma dispersion due to excess carriers in silicon. The silicon microring is incorporated with a lateral p-i-n junction. Injection of carriers into the ring causes a change in the refractive index of silicon, and shifts the resonant frequency of the microring. This

shift in resonant frequency changes the coupling of light from the adjacent bus waveguide into the ring. This results in modulation of the light passing through the bus waveguide. The fundamental limitations on this design have been explored in detail to achieve the highest level of performance. The end result is a modulation rate of 25 Gb/s at a cost of 7 fJ/bit. Additionally, the inherent waveguide coupling results in an insertion loss of 2 dB.

B. WAVEGUIDE-TO-FIBER COUPLERS

A critical function and challenge in optical interconnects is coupling of light from on-chip waveguides to optical fibers. Two approaches are taken in the design of fiber couplers: vertical couplers and edge couplers[13,14]. The vertical couplers shown have the advantage of easier alignment. Large holes can be etched into the silicon substrate which serves as a plug for a multi-fiber connector[15]. The drawback to this approach is that multimode fibers are necessary for low loss coupling. Alternatively, edge couplers using a gradient index waveguide or inverse tapered waveguide can couple to single mode fibers at the cost of precision alignment. In either case, over a 50 nm wavelength range necessary for wavelength division multiplexing, approximately 1 dB of low can be expected.

C. OPTICAL FIBERS

The loss mechanisms in optical fibers are well established. As the total loss is dependent on the length of the fiber between the two chips, the fiber length must be set to some reasonable value. Both for high performance computer clusters and data centers, it can be expected that 1 km of fiber will fit most applications. Whether the 1310 nm or 1550 nm center wavelength is used is yet to be determined since at both of these wavelengths, the

optical loss is less than 1 dB/km. The worst case scenario using a 1310 nm center wavelength will have a loss of 0.5 dB/km.

D. Ge-on-Si Avalanche Photodetectors

Currently, the standard detectors used in silicon optoelectronic transceivers are Ge p-i-n photodetectors grown on silicon waveguides[16]. The material quality has been dramatically improved in order to achieve responsivities greater than 0.9 A/W. However, since there is no gain in the detector, a substantial optical power is necessary for a reasonable bit-error-rate. Ge-on-Si avalanche photodetectors have recently been demonstrated with a gain-bandwidth product of 340 GHz[4]. The end result is that a bit-error-rate of 10^{-9} gives a receiver sensitivity of -29 dBm. This value sets the absolute minimum power to 1.3 μW average incident on the detector.

E. Input and Output Power Requirements for Lasers

With a brief analysis of the optical system from laser to photodetector, a reasonable estimate of the output power of the laser can be made. This is done using the following equation,

$$P_o = 2\alpha_{coupler} + \alpha_{modulator} + \alpha_{fiber} + P_{receiver} \quad (1)$$

where P_o is the output power of the laser in units of dBm. From the previously established values for optical losses and receiver sensitivity, the resulting output power of the laser is then -24.5 dBm or 3.6 μW continuous power in the waveguide. A reasonable buffer to ensure low bit-error-rate is at least 2 dB, so that the target power should be closer to 6 μW.

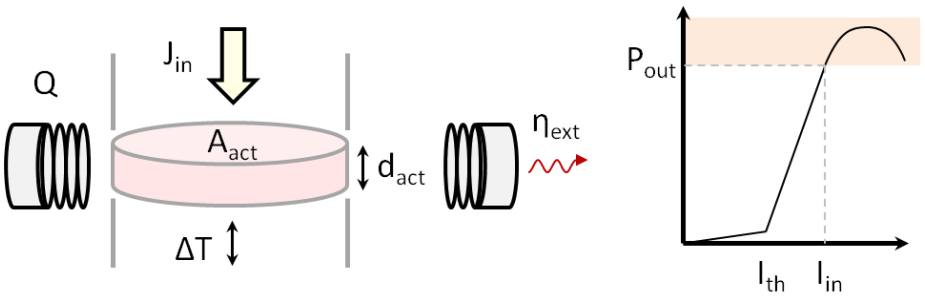

Fig. 2. The general design or "black box" laser. The important parameters are only the active area, cavity Q, confinement factor, and waveguide coupling efficiency. Relationships between these values are found by assuming a maximum input power and minimum output power.

The input power can be determined entirely by the target energy consumption of the system and the fraction required by the modulator. The continuous input power can be determined by using the following equation,

$$P_{in} = \left(E_{target} - E_{modulator}\right) \times B_{modulator} \quad (2)$$

where Emodulator and Bmodulator are the energy consumption (fJ/bit) and bit rate (Gb/s) of the modulator. Using the values for the state-of-the-art silicon microring modulators described above, the input power of the laser is 75 μW.

1.3 General Design Requirements of the Laser

With the input and output power requirements established, it is important to then find the required properties of a laser of arbitrary geometry in order to evaluate the different candidate designs. Most generally, the output power can be related to the input power by a number of measures: (i) current area A_{act}, (ii) cavity Q, (iii) confinement factor Γ, and (iv) waveguide coupling efficiency η. These parameters for a “black box” laser are shown in Figure 2.

A. Input Current and Waveguide Coupling

The first task is to find the maximum input current Iin from the input power. This is most simply done by using the Shockley equation for a diode to find the current for a given input power,

$$P_{in} = I_{in}\frac{nkT}{q} ln\left(\frac{I_{in}}{A_{act}J_0} + 1\right) \quad (3)$$

where n is the ideality factor and I_0 is the saturation current. While the range of materials used in near-infrared extends from GaAs to InP, an ideality factor of n = 1.5 and saturation current of $J_0 = 2.2 \times 10^{-9}$ A/cm2 can be expected. The resulting maximum input current is then ~60 µA.

With the maximum input current clearly defined, the threshold current and external coupling efficiency of the laser can be related by assuming the laser will operate well above threshold. In this case, the output power of the laser is given by

$$P_o = \eta_{ext}(I_{in} - I_{th})\frac{hv}{q} \quad (4)$$

where η_{ext} and I_{th} are the external coupling efficiency and threshold current. The coupling efficiency η_{ext} is the product of internal quantum efficiency ηint and waveguide coupling efficiency η_{wg}, denoted as

$$\eta_{ext} = \eta_{int} \times \eta_{WG} \quad (5)$$

The waveguide coupling efficiency affects the total cavity Q by

$$Q_{tot} = \left(\frac{\eta_{WG}}{1+\eta_{WG}}\right) Q_{WG} \quad (6)$$

where Q_{wg} is the fraction of the cavity Q coupled to the waveguide. The actual values of Q_{wg} and η_{wg} will need to be determined for each candidate design.

B. Cavity Q, Active Area, and Modal Confinement Factor

The cavity Q, active area Aact, and confinement factor Γ will be the three most important parameters in the laser design, as they are related to the threshold gain by

$$g_{th} = \frac{2\pi n_{g,a}}{\lambda} \cdot \frac{1}{Q \cdot \Gamma} \tag{7}$$

where ng,a is the group refractive index of the gain material and λ is the lasing wavelength[17]. The current density can also be related to the gain in the active material by

$$g = g_0 \ln\left(\frac{N + N_s}{N_{tr} + N_s}\right) \tag{8}$$

where N_s and N_{tr} are the saturation current density and transparency current density. For InGaAs compounds emitting in the wavelength range of interest, $N_s = 5\times10^{18}$ cm^{-3} and $N_{tr} = 1.1\times10^{18}$ cm^{-3}, while $g_0 = 3000$ cm^{-1}. Combining these equations then leads to an expression for the threshold current

$$I_{th} = A_{act} \frac{d_{act}}{\tau_{eff}} \left[(N_{tr} + N_s) exp\left(\frac{2\pi n_{g,a}}{\lambda} \cdot \frac{1}{g_0 \cdot Q \cdot \Gamma}\right) - N_s\right] \tag{9}$$

This equation can then be combined with the power output of the laser in order to show the relationship between Q, Γ, and Aact to achieve the desired output power given a maximum input current. This expression is given by

$$A_{act} = \frac{I_{in} - \frac{q}{h\nu} \cdot \frac{P_o}{\eta_{ext}}}{(N_{tr} + N_s) exp\left(\frac{2\pi n_{g,a}}{\lambda} \cdot \frac{1}{g_0 \cdot Q \cdot \Gamma}\right) - N_s} \tag{10}$$

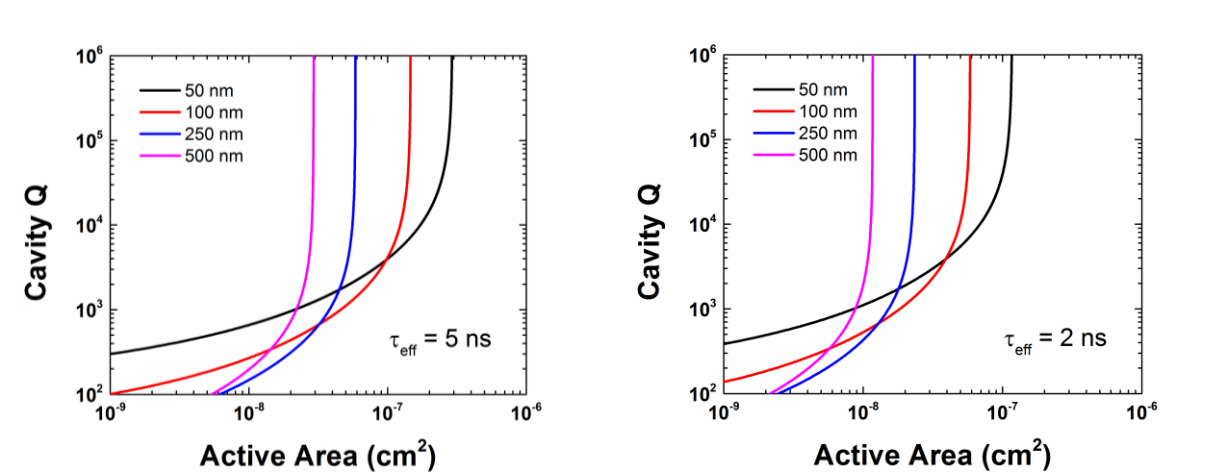

Fig. 3. Plot of active area vs. cavity Q for several confinement factors. Reducing the active area for the fixed input current value produces a higher gain coefficient and results in a lower Q value necessary for the required threshold. Thermal issues will arise at smaller active areas due to the extremely high current density.

From this equation we can find the necessary Q value for a given active area A_{act} and confinement factor Γ.

Figure 3 shows a plot of multiple $Q(A_{act})$ curves for different values of d_{act}. This shows a distinct relationship between the cavity Q and active area to reach 6 µW output with only 60 µA input. For smaller active areas, a lower Q value is necessary to reduce the threshold current while for larger areas a higher Q is necessary due to the low material gain. Without any other considerations, this would indicate that an extremely small active area device can still function even with a very low Q value. However, the current density through such a small active area would be unreasonably high, likely causing the device to fail. In order to place a lower limit on the active area, the thermal impedance of the device must be considered.

C. Thermal Impedance and Efficiency Restrictions

The low Q value as a result of the previous calculation seems unreasonable at first. However, when dealing with a small current aperture such as this, the overall wall plug

efficiency must be taken into consideration. The curve in Figure 3 represents the minimum Q and A_{act} to get 6 μW output for 75 μW input. This means the ~69 μW of the input power is dissipated as heat. If the active area is represented as a disk, the radius would be 0.9 μm with a power density of 2.7 kW/cm^2. To estimate the temperature change due to power dissipation, we can use the equation

$$\Delta T = P_D Z_T \tag{11}$$

where P_D is the dissipated power and Z_T is the thermal impedance. The expression for thermal impedance of a disk source on a large substrate is given by

$$Z_T = \frac{1}{2\varepsilon r} \tag{12}$$

where ε is the thermal conductivity of the substrate and r is the radius of the disk. For the thermal conductivity of the substrate, we must use the value for SiO2 of 0.014 Wcm^{-1}K^{-1}, since the laser will be on a silicon-on-insulator substrate. The resulting increase in temperature for this example is then ΔT = 13°C. While seemingly small, this rise in temperature will greatly reduce the output power much below the required output. For consistent performance, the laser should have a temperature rise of less than 1°C due to dissipated power.

Setting a constant temperature difference places further restriction on the relationship between input and output power. For the case of the disk source on a large substrate, he expression for thermally dissipated power as a function of active area is

$$P_D = P_{in} - P_o = 4\varepsilon \Delta T \sqrt{\frac{A_{act}}{\pi}} \tag{13}$$

The consequence of this expression can be viewed in two ways: either the input power has to be significantly reduced but still achieve the same output, or the output power has to be significantly increased for the given input. Figure 4 shows a comparison of restricting the input and the output power for different allowed temperature differences. In Figure 4(a), the input power is held constant. As the active area decreases, the laser output must be increased in order to maintain the same temperature difference. In Figure 4(b), the output power is held constant, and as the active area is decreased the input power must also be decreased in order to maintain the same temperature difference.

The result of this is that the active area can only be made smaller if the efficiency of the laser is improved. Depending on the temperature restriction, the necessary cavity Q to reduce threshold will increase asymptotically as either the input power approaches the theoretical minimum or the output power approaches the theoretical maximum. A revised

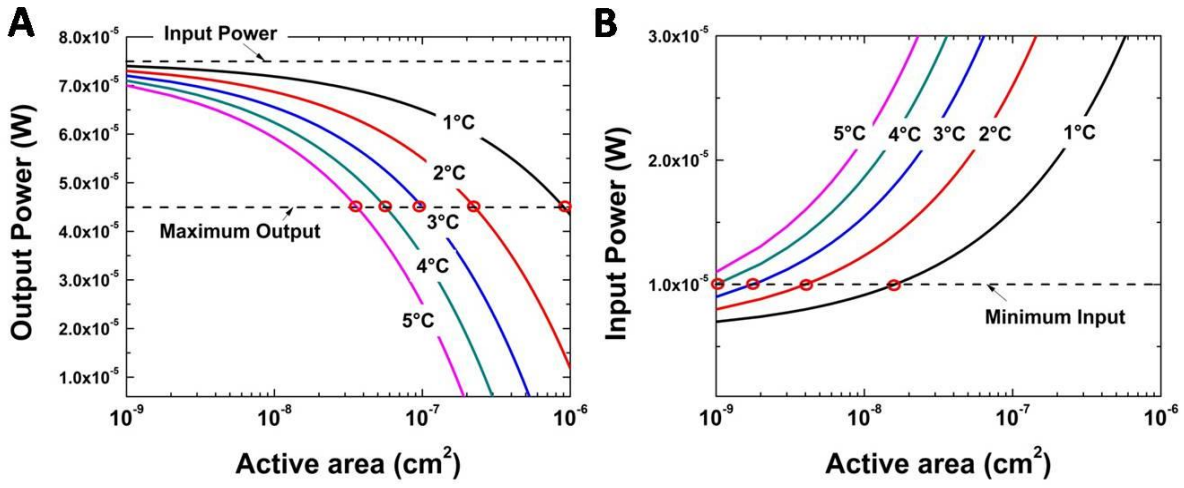

Fig. 4. Comparison of thermal limitations on the laser design. (A) The case where the input power is constant and the laser efficiency is improved to reduce temperature increase. The theoretical maximum output power is shown for the laser, where the intersections (red circles) show the minimum area that can be used. (B) The case where the output power is constant while the efficiency is increased to reduce the necessary input power. The theoretical minimum input power is shown where the allowed area is significantly smaller than in (A).

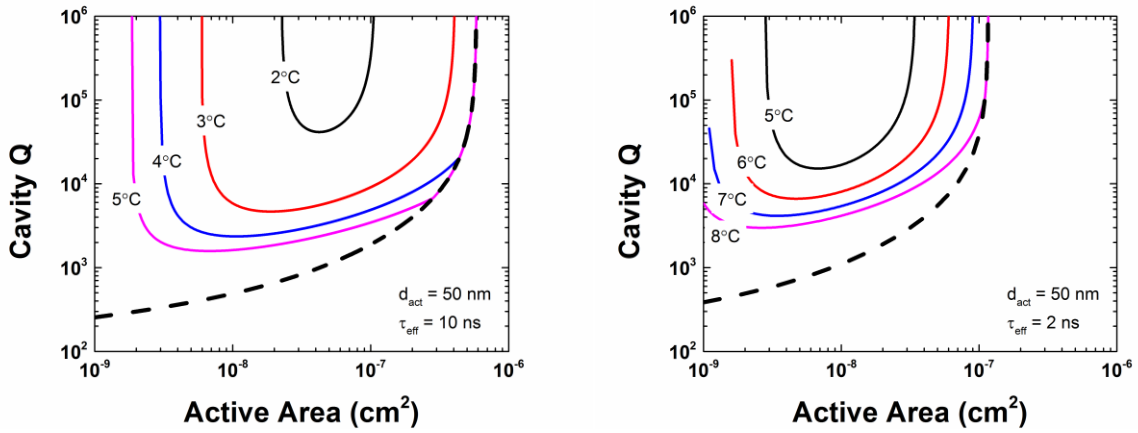

Fig. 5. Plot of cavity Q vs. active area with the thermal budget taken into consideration. In order to maintain a certain temperature, the cavity Q rises asymptotically below a particular active area to compensate with increased efficiency. For a given temperature value, there is a minimum active area where even a threshold-less laser does not have the required efficiency.

plot of Q vs. A_{act} for various temperatures is shown in Figure 5 to illustrate this behavior. Realistically, the target temperature increase should be in the 1-2°C range. For any given thermal budget, a minimum cavity Q can be found as a function of area. As high-Q cavities are difficult to fabricate repeatedly in many designs, this value for A_{act} should be used.

Several additional facts must be considered in a more thorough analysis than what is presented here. The optical system analysis used to determine the minimum output power in the previous section will need to be extended for specifics of the actual optoelectronic transceiver such as waveguide losses on chip and additional components (optical isolators, multiplexors, demultiplexors, etc.). Raising the minimum output of the laser will shift the optimal active area to larger values accordingly. Finally, this analysis assumes a waveguide coupling efficiency of 90%. This means that the minimum Q value for the laser design must be the total Q with at least 90% coupling efficiency. In other words, the uncoupled cavity Q must be at least 10× larger.

1.4 Micro-ring and Photonic Crystal Resonators

Currently, the best performing lasers on silicon are microdisk[18] and microring[19] resonators. This laser design is used for many of the reasons established above: high-Q, small footprint, and high waveguide coupling efficiency. However, the circular design is limited by bend losses in the ring waveguide, and as a result the maximum Q value of the resonator is scaled down with the active area. Even at the lower limit for waveguide width of 0.5 μm, the microring cavity does not have a sufficient Q value to operate. Overcoming the thermal limitation to the device design could push microring lasers closer to the target region. This has motivated development in silicon-on-diamond wafers, but this work is still in the early stages and may prove too costly for manufacture.

1.5 Conclusions

With a relatively simple analysis, general requirements for lasers to be used in next generation optical interconnects have been established in terms of basic laser cavity properties. It is found that in order to reach the famed 10 fJ/bit mark, the power dissipation is the key limitation in lasers on this size scale. Therefore, lasers meeting these design requirements must have a sufficiently small area and high cavity Q. The current state-of-the-art microring lasers do not appear to meet these requirements due to fundamental limitation on cavity Q vs. active area for microrings. Since the requirements are so stringent for lasers operating at these power levels, it is evident that a new type of photodetector will be needed to continue scaling past the 10 fJ/bit mark. In any case, it is likely that in 20 years, optical interconnects will face a crisis similar to the scaling of silicon CMOS transistors in that lasers will not be able to be made smaller and still function.

An additional aspect that should be considered is illustrated in Figure 6. For the silicon photonics platform, much of the restriction on the laser design is due to the thermally insulating buried oxide layer. In this case, we can take the same parameters used in Figure 5(a) and change the thermal conductivity of the substrate while considering a junction temperature rise of 1°C. The most important outcome of this calculation is that for a substrate thermal conductivity of 0.68 $Wcm^{-1}K^{-1}$(equivalent to bulk InP), the necessary cavity Q is nearly identical to the case of Figure 3, where power dissipation was neglected. This can be interpreted in two ways: either fJ/bit transceivers should be made on InP rather than SOI, or a highly effective metal heat sink process must be developed for silicon photonics so that the power can be directed to the silicon substrate underneath the buried oxide layer.

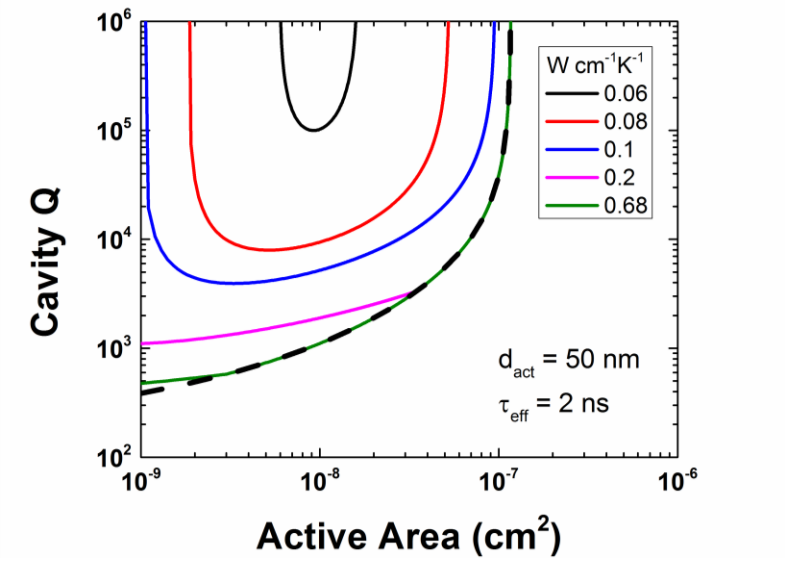

Fig. 6. Comparison of different substrate thermal conductivities shows that the SiO_2 layer in the SOI substrate is the main limitation of the laser design. Improved thermal conductivity greatly reduces the necessary cavity Q to reach the required output power. In the case of an InP substrate, the cavity Q is nearly equivalent to the model with no thermal restrictions.

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Chapter 2

2.1 Selective-Area Growth of III-V Nanopillars

The selective-area growth of III-V nanopillars has been studied by several groups around the world over the last decade[1,2]. It is notably different than other forms of III-V nanowire synthesis in that there is no metal catalyst to assist in the growth. Instead, the growth is confined to nanoscale openings patterned in a dielectric mask which prevents growth elsewhere on the substrate surface. This approach has unique advantages and challenges: (1) The nanopillars are grown without a catalyst, and therefore cannot suffer from metal contamination, (2) The nanopillar position and diameter is well defined by the lithography used to pattern the nanoholes, (3) Control over axial and radial crystal growth can be accomplished, but only for certain materials and specific growth conditions.

The fact that the nanopillar position and diameter can be accurately controlled by the lithography process is the key enabler of much of the work in this thesis. The impact of the nanopillars' periodic structure on optical properties will be explored in later chapters. However, the most important aspect of the selective-area growth is the greatly relaxed lattice matching requirements of different materials used to form heterostructures[3,4]. The use of selective-area growth at nanoscale dimensions (<100 nm) avoids defect formation due to lattice mismatch by allowing strain relief in the lateral direction. By this method, highly uniform arrays of III-V nanopillars can be successfully grown on Si (111) substrates[5–8]. An example of this growth is shown in Figure 1.

Initially, development of III-V NPs grown on Si focused on the nanoscale lithographic patterning of nanohole arrays to serve as a growth template. For this purpose, LPCVD silicon nitride films 20 nm in thickness were used as the growth mask in order to

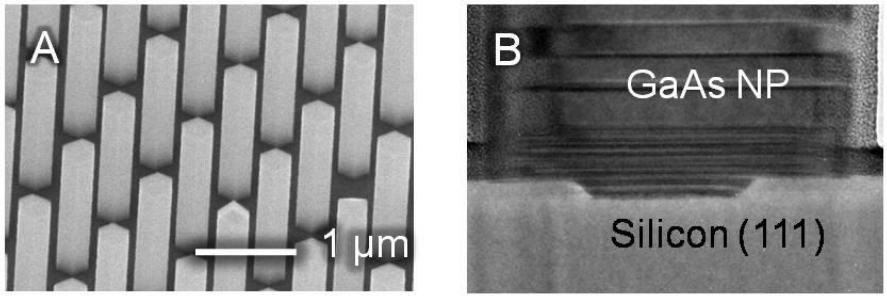

Figure 1. (a) Tilted SEM of GaAs NP array grown on Si. (b) Cross-section TEM of the GaAs/Si interface showing dislocation-free growth.

provide a high etch selectivity over silicon dioxide during the native oxide removal prior to growth. The nanohole arrays were patterned by electron-beam lithography and reactive-ion etching as shown in Figure 2.

The growth of GaAs was demonstrated by using a two-temperature growth process. The initial GaAs layer was grown at a low temperature of 400°C in order to form a stable GaAs (111)B surface. This low temperature growth was chosen both to prevent anti-phase domain formation at the interface, but also in order to facilitate development of nanopillar growth and devices by creating an identical growth surface to GaAs (111)B substrates. Following the formation of the low temperature GaAs seeding layer, the nanopillar growth

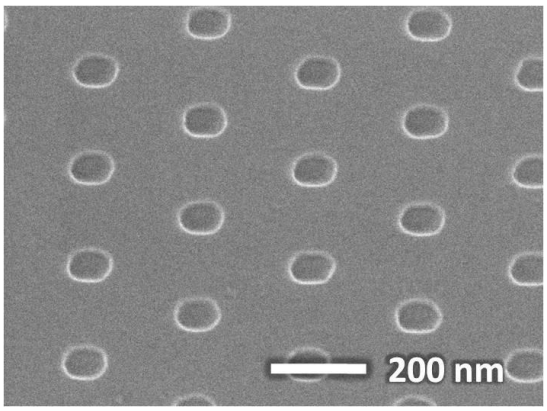

Figure 2. Nanohole array etched into the silicon nitride growth mask on Si(111).

is carried out at 700°C, identical to the growth conditions on GaAs substrates. This resulted in the growth of highly uniform GaAs nanopillar arrays on Si (111) substrates.

The ability to grow nanopillar arrays under nearly identical conditions on both Si(111) and GaAs (111)B substrates is the primary motivation for the development of nanopillar based emitters as the nanopillar growth could be studied more rapidly by growth on GaAs substrates, followed by porting of the growth conditions to the Si substrates.

2.2 In-Situ Passivation of Nanopillars

While nanopillars are a promising route to achieving high-efficiency emitters on Si, the current limitation of all nanopillar opto-electronic devices is the quality, or effectiveness, of the surface passivation. Previous studies of surface passivation of III-V materials are almost entirely limited to chemical passivation by Ammonium Sulfide or similar Sulfur containing compounds[9,10]. The majority of the work in this thesis is based on InGaP shells lattice matched to GaAs for *in-situ* surface passivation[11–13]. However, small changes in interrupt time between switching of As and P precursors produced considerable variation in device performance. This observation indicates that the primary limitation of the InGaP passivation is the interface between Ga(In)As and InGaP, as luminescence intensity and diode characteristics are nearly independent of the InGaP shell thickness.

A possible reason for the interface sensitivity to the As and P precursor switching is the fact that InGaAsP compounds formed between GaAs and InGaP can potentially lead to non-radiative recombination. This effect has been documented widely in studies of crystal growth related to Heterojunction Bipolar Transistors (HBTs) based on InGaP/GaAs. Since the necessary thickness of the passivation shell is on the order of 5 - 10 nm, the lattice

matching of the shell material to the core is not highly restricted as it is for planar devices. Therefore, the InGaP shell can be replaced with a GaP shell that is only slightly tensile strained. The advantage of the GaP shell compared to the InGaP shell is that all compositions of GaAsP have a higher band-gap than GaAs, potentially reducing the sensitivity to the As and P precursor switching.

Initial studies of GaP shells have shown that an optimized growth condition of GaP is able to produce a 15x improvement in PL intentsity relative to the best known InGaP passivation. Even with this marked improvement in luminescence intensity, the GaP passivated NPs still show signs of interface limitation. Most notable, is the degradation of luminescence intensity over several hours of excitation at medium pump powers, and rapid degradation at high pump powers.

In order to better understand these limitations, knowledge of the carrier lifetime is necessary. To accomplish this, a customized time-resolved micro-photoluminescence setup was constructed based on time-correlated single photon counting (TCSPC) module with a Si avalanche photodiode (APD) and photomultiplier tube (PMT) for sub-nanosecond time resolution from 350 - 1700 nm. Initial TRPL measurements of InGaP and GaP passivated NPs fell below the system resolution of ~100 ps. Changes in interrupt time shown in Figure 3 showed that intermixing between As and P at the interface between GaAs and GaP could dramatically improve the lifetime up to ~0.5 ns.

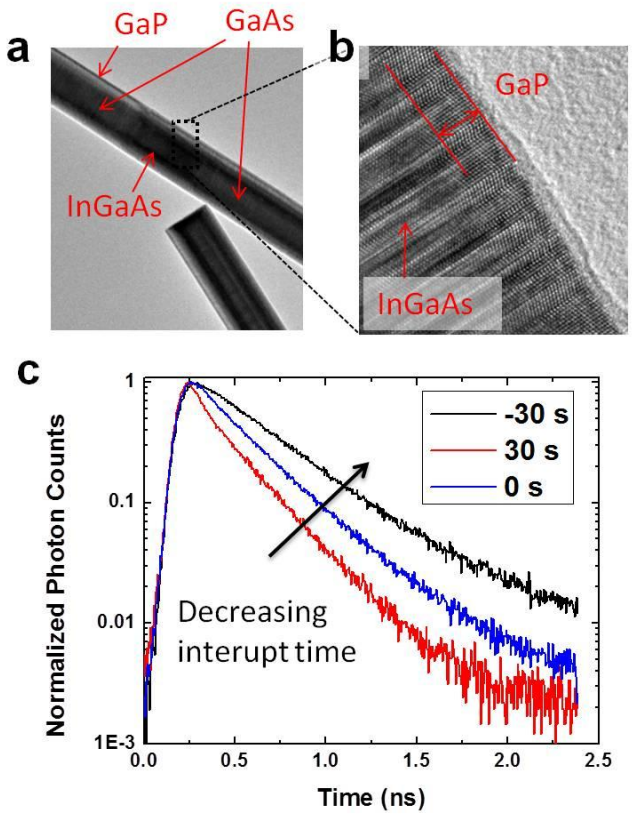

Figure 3. (a) TEM image showing the Ga(In)As NPs with GaP shells. (b) Magnified TEM image of the InGaAs/GaP interface. (c) TRPL measurements of the carrier lifetime with varying interrupt times between As and P precursor flows.

While the changes in interrupt time yielded a substantial improvement in lifetime, the measured lifetimes are still below values typical of planar films by up to an order of magnitude. Therefore, a study of the possible mechanisms of the non-radiative recombination limiting the lifetime has revealed that one of the major limitations of the carrier lifetime is the substrate, as shown in Figure 4. Here, TRPL measurements compared the carrier lifetime under different conditions: on-substrate, in PDMS, in PDMS under back illumination, and in PDMS under back illumination and with Ammonium Sulfide passivation of the exposed GaAs surface from the PDMS peel-off process. The fact that the lifetime is highest in the case of the PDMS back-side illumination with sulfide passivation indicates that the substrate quality is one of the major limitations in carrier lifetime.

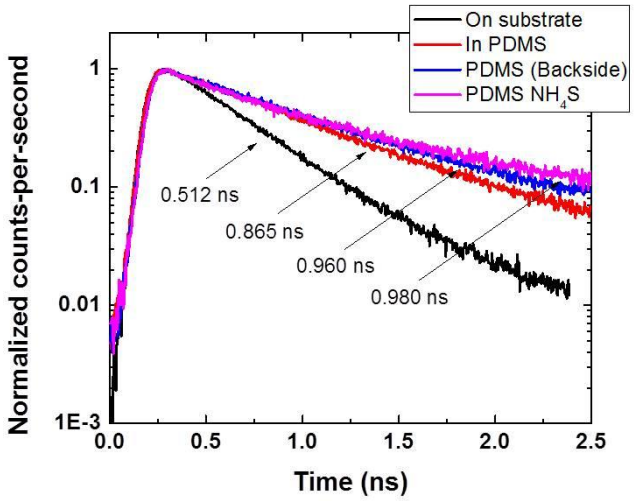

Figure 4. TRPL measurements of GaP passivated GaAs NPs under different conditions: on-substrate, in PDMS, in PDMS under back illumination, and in PDMS under back illumination and with Ammonium Sulfide passivation of the exposed GaAs surface from the PDMS peel-off process.

However, even under these ideal conditions, the carrier lifetime is still substantially lower than bulk GaAs and InGaAs.

As an alternative to III-P passivation, purely III-As passivation was explored to

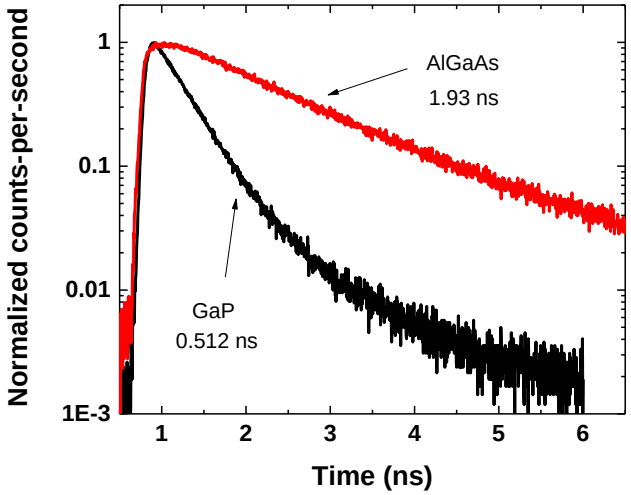

Figure 5. TRPL measurements of the optimized GaP passivation in comparison to the optimized AlGaAs passivation.

potentially reduce interfacial recombination. For this purpose, alloys of AlGaAs are ideal, as they have a significantly wider bandgap than GaAs and are lattice matched for any Al composition. Similar to the development of InGaP and GaP passivation, the AlGaAs passivation was studied initially by PL intensity measurements in order to establish the optimum growth temperature and Al/Ga ratio. This concluded with the ideal growth temperature being between 580 - 600°C and an Al/Ga ratio of 1:1.

A comparison between the optimized GaP passivation and AlGaAs passivation is shown in Figure 5. While the longest carrier lifetime of the GaP passivation was only ~0.5 ns, the optimum AlGaAs passivation has a lifetime of ~2 ns. With a lifetime of ~2 ns, the NPs can be considered a suitable material for lasers in the fJ/bit regime as shown in Chapter 1.

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Chapter 3

3.1 Optical Resonators for Nanowires

NW based lasers pose a unique challenge over other optoelectronic components because they require a carefully designed and fabricated resonant optical cavity. Several different approaches have been taken to form cavities for NW lasers, including plasmonic waveguides[1], Fabry-Perot resonators[2], microring racetrack resonators[3], and top-down etched photonic crystal cavities[4,5]. However, these devices were fabricated by mechanical removal of the NWs from the growth substrate and random placement on a host substrate[5,6]. Alignment of subsequent process steps was done to each NW individually. Currently there is no feasible manufacturing method to place the NWs on the host substrate with the necessary precision to fabricate these devices at the wafer scale.

An alternative approach to integration of NWs and NPs with PICs is lithographic control of the growth position and diameter. This allows for photonic crystal (PC) waveguides, resonant cavities, and active gain regions to be formed entirely by NPs grown simultaneously. These PC devices correspond to the dielectric rods in air structure, which differs from the more conventional air holes in a dielectric slab structure in that the photonic band gap occurs for TM polarization rather than TE polarization. PC waveguides of this type with no active gain have been reported previously using vapor-liquid-solid (VLS) grown NWs patterned by nanoimprint lithography[7]. However, this method suffers from limited variability in the NW diameter due to the Au catalyst particle size, the tapered profile of the NWs, and defect growth between the NWs that will result in optical losses. These problems can be avoided by growth of NPs via catalyst-free selective-area epitaxy (SAE). Furthermore, the SAE patterns include optical alignment marks for device integration.

3.2 BOTTOM-UP PHOTONIC CRYSTALS

In this work, we exploit the ability to design device parameters with SAE to enable 2-D photonic crystal devices. Control of both NP pitch and diameter allow for the photonic band-gap (PBG) region and defect cavity active region to be comprised entirely of III-V NPs grown simultaneously. The SAE grown NPs offer a unique advantage due to their hexagonal cross-sections with side-wall facets consisting of the {1-10} family of crystal planes[8]. These side-walls are completely vertical and have atomic scale roughness[9–11], avoiding two of the largest contributors to cavity losses in top-down fabricated photonic crystals[12,13]. The growth of pure axial GaAs/InGaAs/GaAs heterostructures allows for the appropriate placement of gain material within the cavities at the anti-nodes of the electric field[14,15]. Furthermore, the ability to grow lattice matched InGaP shells over the NPs provides effective *in-situ* surface passivation to prevent non-radiative recombination and surface pinning that is detrimental to device performance[16,17].

These PC cavities consist of a PBG region and an active gain region. Figure 1(a) shows a scanning electron microscope (SEM) image of the etched growth mask for a single defect cavity to illustrate the NP arrangement. The growth mask consists of a 20 nm thick SiN_x film formed by plasma-enhanced chemical vapor deposition that is subsequently patterned by electron-beam lithography (EBL) and reactive ion etching (RIE). Line edge roughness typical of EBL and RIE patterns is visible in the SEM, however, this roughness does not translate into the NP sidewall. For the PBG region, the NPs are arranged in a triangular lattice with a constant radius to pitch ratio (r/a) of 0.2. This ratio is chosen to ensure a wide TM like band-gap exhibited by the dielectric rods in air structure. For all of the active regions, NPs with a 65 nm diameter and 175 nm pitch are arranged in a square lattice fill the defect cavities. This particular arrangement of

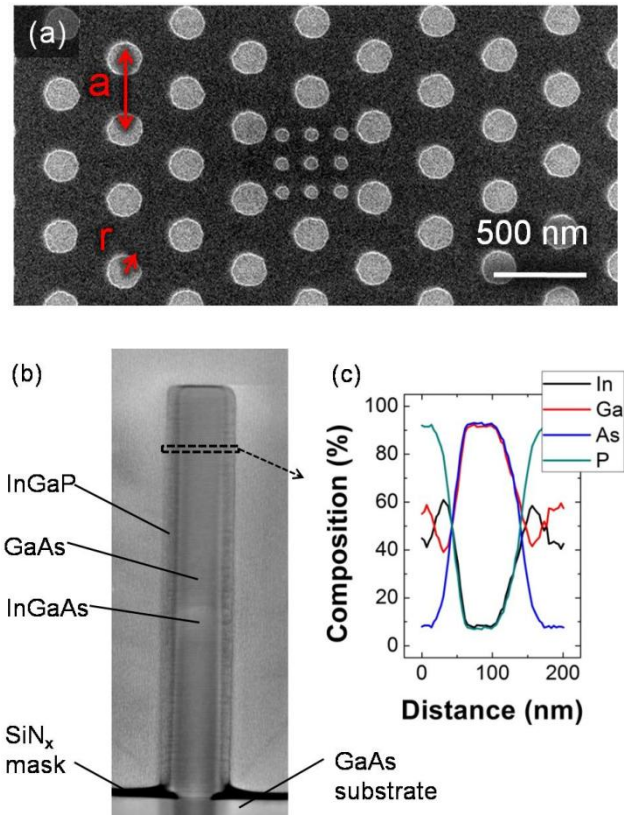

Figure 1. (a) Top-down SEM of the etched growth mask of an L1 cavity. (b) Cross-section HRTEM of a NP showing the GaAs/InGaAs axial core structure and InGaP shell. (c) Radial EDS scan with composition of In, Ga, As, and P.

NPs in the active regions is chosen due to its high concentration factor for TM polarization at the peak emission wavelength. The resulting fill factor (FF) of this configuration is 0.433, while that of the PBG region is 0.145.

To study the effects of the PBG on the emission spectrum, an array of devices is formed with varying pitch ranging from 264 - 534 nm in increments of 12 nm for a total of 20 columns. The first row in each column is a device with no defect cavity for reference. The second and third rows of each column are devices with single (L1) or triple defect (L3) cavities in the center. Each device is referred as *x*-*y* , where *x* is the column number in order of smallest to largest pitch and *y* is the row number. Based on the standard 2-D model of infinitely tall dielectric rods in a triangular lattice, the PBGs of the devices should range from 0.8 to 1.6 μm. To reduce the

perturbation to the 2-D approximation used to estimate the band-gap wavelength ranges, the pillars were grown at least 800 nm tall to be sufficiently greater than the half-wavelength of the emission peak.

The NPs used to form the PC cavities are grown with axial InGaAs heterostructures followed by *in-situ* passivation with InGaP shells to prevent non-radiative surface recombination. Figure 1(b) shows a high-resolution transmission electron microscopy (HRTEM) image of the NP cross-section where the contrast between the GaAs, InGaAs, and InGaP portions can be seen. These NPs are grown by low-pressure vertical flow metal-organic chemical vapor deposition on patterned GaAs (111)B substrates. The NP growth is separated into two steps. First, the axial GaAs/InGaAs/GaAs double heterostructure is grown at a temperature of 735°C under an ambient hydrogen pressure of 60 Torr using trimethyl-gallium (TMGa), trimethyl-indium (TMIn), and tertiary-butyl-arsine (TBA) as precursors. The InGaAs section is grown at approximately the mid-length of the NP with a calculated gas phase concentration of 30% Indium. A more detailed description of the growth and masking is reported elsewhere[12]. The resulting Indium concentration in the solid is calculated to be 14.5% from the peak emission wavelength of 970 nm. Once the axial core structure is grown, the temperature is reduced to 575°C under an arsenic overpressure. Following a hydrogen purge and tertiary-butyl-phosphorous (TBP) preflow optimized to reduce As/P intermixing, an ~8-10 nm thick InGaP shell lattice matched to GaAs is grown. Figure 1(c) shows an energy dispersive x-ray spectroscopy (EDS) scan in the radial direction of the NP used to verify the composition of the GaAs core and InGaP shell.

Figure 2(a) shows an SEM image of a full device after growth demonstrating the high uniformity of the NP arrays. While these PC cavities provide in-plane optical confinement, the lower effective index of refraction in the active region (n_{eff} ~ 2.0) results in optical loss into the

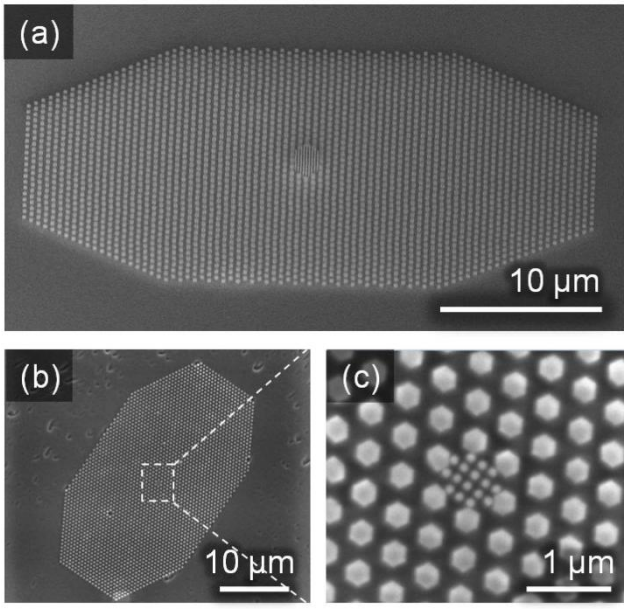

Figure 2. (a) 45° tilted SEM of a NP photonic crystal cavity. (b) Low vacuum SEM of NP PC cavity embedded in PDMS. (c) High magnification image of the single-defect cavity from the device in (b).

substrate (n_{GaAs} = 3.3). Due to the reduced pitch and diameter, the NPs within the cavity are as much as 20% taller than those forming the PBG. To form cavities with out-of-plane optical confinement, the NP PCs are encapsulated in polydimethylsiloxane (PDMS) and removed from the patterned substrate mechanically by shearing at the NP/substrate interface. Figure 2(b) shows a top-down image of a PC embedded in PDMS after lift-off taken by a low-vacuum SEM. In Figure 2(c), a high-magnification SEM shows the L1 defect cavity region of the device in 2(b). By performing a lift-off of the NPs in PDMS, the refractive index above the cavity is then n = 1.0 for air and n = 1.47 below the cavity for PDMS.

3.3 Optical Characterization of Nanopillar PhCs

Prior to the PDMS lift-off, the PC cavities are characterized on the substrate. The samples are characterized at both 300K (data not shown) and 77K using a liquid-nitrogen cooled InGaAs focal plane array with a 50x objective lens oriented normal to the substrate. A 659 nm continuous wave diode laser operating at 2 mW output power is used as the excitation source

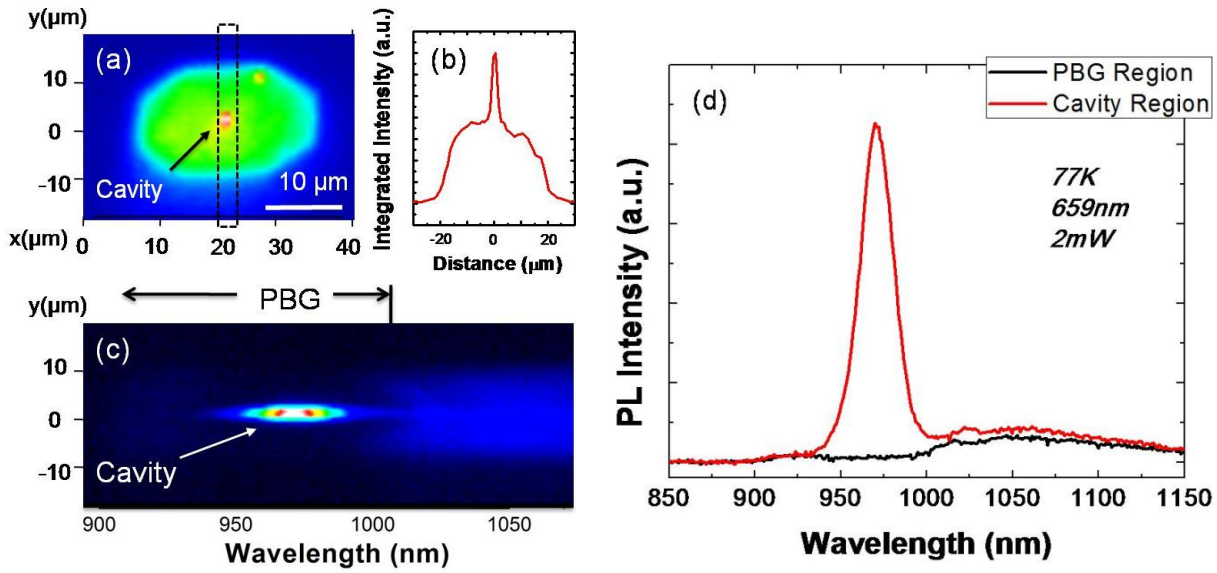

Figure 3. (a) Spectrally integrated image of a PC where the PBG exists in the emission range of the device. (b) Line scan of integrated intensity along the center axis of the device shown in (a). (c) Spectrally resolved image of the PC in (a) taken along the center axis of the device as illustrated by the outlined box in (a). (d) Comparison of PL spectra taken on the cavity region and on the PBG region of the device.

with a 75° angle of incidence to the substrate normal and a spot size of ~100 μm in diameter. At 300K, the full-width half-maximum (FWHM) of the cavity emission is greater than 50 nm and not well separated from the emission outside the PBG. Figure 3(a) shows a spectrally integrated image of device *17-3* at 77K, which exhibits a PBG from 800 to 1000 nm spanning the range of emission. In Figure 3(b) a line-scan of the integrated image shows that the PL intensity of the cavity region located in the center of the device is increased by a factor of 2 relative to the PBG region. Figure 3(c) shows the spectrally resolved PL taken along the center axis of the device. At the edge of the device (y = 10 μm), the cut-off wavelength of the PBG appears to be at 1 μm, where only the "tail" of the InGaAs emission can be observed. Closer to the center of the device (y = 0 μm), the PBG cut-off shifts to 1025 nm due to the increase in NP height. Only at the center of the device, where the cavity is located, can the InGaAs emission peak (λ~970 nm) be observed. To exemplify this, Figure 3(d) shows a comparison of the spectra taken on the cavity

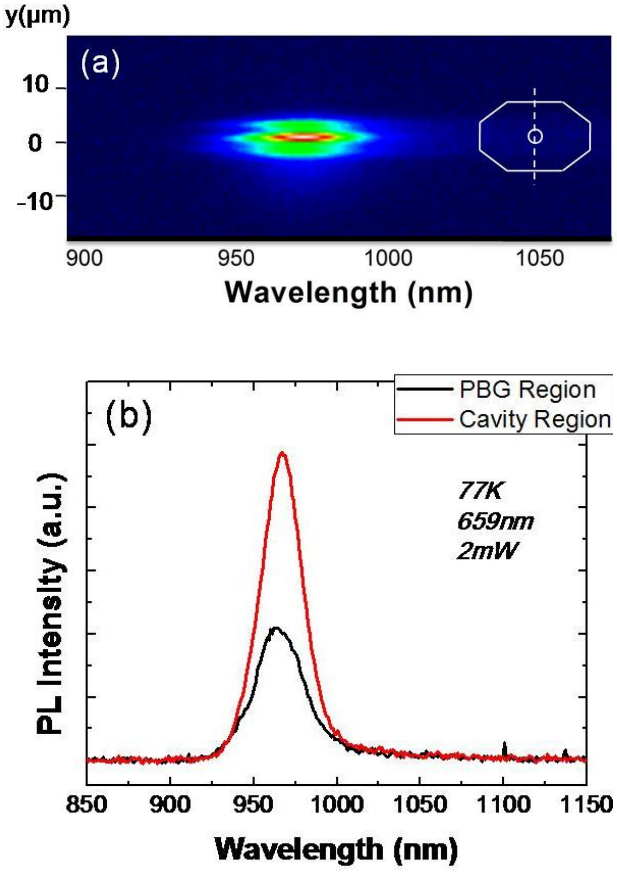

Figure 4. (a) Spectrally resolved image along the center axis of a PC where the PBG in not in the emission range. The inset diagram shows the orientation of the device with the dotted line showing the axis along which the emission is resolved. (b) PL spectra of the PC in (a) comparing the cavity and PBG regions of the device.

region and at the midpoint between the cavity and the edge of the device. The spectrum taken at the midpoint does not exhibit the emission peak at 970 nm above the noise floor of the detector. This provides clear evidence of a PBG inhibiting the InGaAs band-edge transition in agreement with previous optical characterization of top-down PC cavities[18].

To further demonstrate that the suppression of the 970 nm emission is due to a PBG and not the NP growth itself, a device on the same sample with identical configuration but different lattice constant in the PBG region is characterized for comparison. Figure 4(a) shows the spectrally resolved PL along the center axis of device *5-3*. In this case, the 970 nm emission peak

is observable across the entire device. This is exemplified in Figure 4(b), where spectra taken on the cavity region and at the midpoint between the cavity and edge are compared. Only an increase in intensity is observed from the cavity region relative to the PBG region. Since this is observed in both devices, it is most likely due to the increased FF of the NPs in the cavity region compared to the PBG region. This results in a larger volume of InGaAs per unit area within the cavity.

Although the PC cavities characterized on the substrate are expected to have a significant optical loss in the out-of-plane direction, the effect of the optical confinement due to the PBG is readily observable. In devices where the PBG does not overlap the range of emission, the FWHM is measured to be 33 nm. In the devices where the PBG spans the range of emission, the FWHM is measured to be 23 nm. This reduction in line-width corresponds to a cavity quality factor *Q* of 42. In addition to the optical power loss into the substrate, the precise arrangement of NPs forming the cavity will also have a strong effect on the *Q* factor. For top-down PC cavities, it has been shown through simulation and experiment that displacement of the etched holes adjacent to the cavity can result in greater than an order of magnitude difference in *Q* factor[19,20]. These displacements modify the *k*-space distribution of the electric field to reduce the out-of-plane optical loss. Since this technique has not yet been applied to the devices presented in this paper, it is expected that a similar performance increase can be attained by more detailed modeling of the cavity design.

To form a PC cavity with out-of-plane optical confinement, the index of refraction both above and below the cavity must be less than the effective index of the cavity. Using the same characterization method as described above, the samples are cooled to 77K and the PL spectrum is measured along the center axis of the devices. Figure 5(a) shows device *16-3* with a PBG

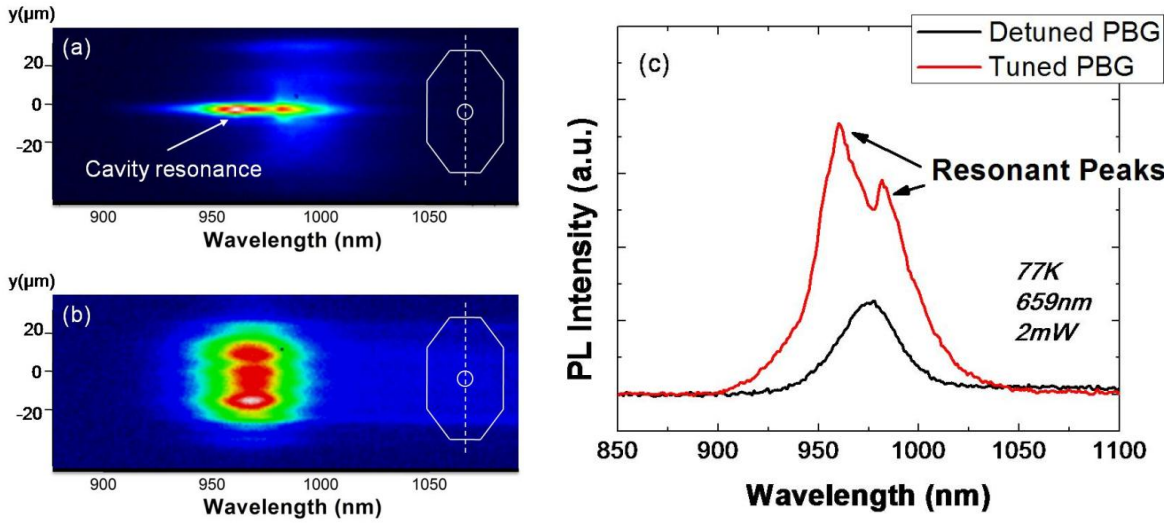

Figure 5. (a) Spectrum of a PC embedded in PDMS with a PBG in the emission range. (b) Spectrum of device where no PBG is present in the emission range. (c) PL spectra comparing the two devices in (a) and (b) taken on the cavity region.

overlapping the emission range while Figure 5(b) shows device *5-3* with a PBG outside the emission range. Similar to the devices on the growth substrate, a clear suppression of the InGaAs band-edge emission is observed where the emission is within the range of the PBG. More importantly, though, is the observation of resonant peaks in the PL spectrum of the cavity in 5(a). As a comparison, Figure 5(c) shows the spectra of the two devices taken on the cavity region. For the device with the PBG covering the emission range, two resonant peaks are observed at 960 nm and 980 nm. The FWHM of each of the resonant peak is estimated to be 10 nm, corresponding to a cavity *Q* of ~96. While an improvement over the *Q* factor measured for the devices on the substrate, this value is still considerably low.

Examination of the devices in PDMS by low-vacuum SEM did not reveal any damage or defects surrounding the cavity. Because of this, the low cavity *Q* indicates that the specific arrangement of NPs in the cavity is most likely to be the limiting factor. This arrangement not only influences the spatial distribution of the cavity mode but also variation in NP height due to

the difference in pitch and diameter, both of which will affect the cavity *Q*. More specifically, the reduced diameter and pitch in the cavity region results in taller NPs. Future improvements will require finite-difference time-domain (FDTD) simulations to determine the optimum placement of NPs within and adjacent to the cavity. The primary goal will be to minimize the variation in pitch and diameter while simultaneously maximizing the cavity *Q*.

3.4 CONCLUSIONS

In summary, we report the ability to form bottom-up PC cavities with SAE of III-V NPs. By exploiting the flexibility provided by the SAE growth technique, both PBG structures and active gain regions are formed simultaneously during growth. Careful control of the V-III ratio and growth rates results in highly uniform PC devices with L1 and L3 defect cavities. An axial GaAs/InGaAs heterostructure with an InGaP shell shows strong emission at a peak wavelength of 970 nm. Inhibition of the band-edge transition in devices where the PBG overlaps the emission range is observed. Out-of-plane optical confinement is achieved by embedding the PC devices in PDMS followed by mechanical separation from the original substrate. The PC cavities in PDMS exhibit cavity resonances at 960 nm and 980 nm. Future work will include FDTD simulations to optimize the cavity design to achieve higher *Q* factors. Applications to optofluidics and reuse of patterns after PDMS lift-off will also be explored.

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Chapter 4

4.1 Background and Challenges of Nanowire Lasers

In the past decade, intense research has been performed in the area of nanowires (NWs) and nanopillars (NPs). These semiconductor nanostructures can be synthesized with specific material compositions[1], axial and radial heterostructures[2,3], and on large lattice mismatched substrates including silicon[4,5]. Such attributes, combined with their small cross sections, promise new device architectures and pathways to on-chip photonic integration[6]. An essential component for a viable photonic circuit is a high-performance NW-based laser. Researchers have sought to make efficient NW-based lasers by a number of methods, including top-down photonic crystal (PhC) cavities[7], micro-stadium resonators[8], plasmonic waveguides[9], and NWs that support whispering gallery modes[10,11]. So far, these demonstrations have largely been limited to single NWs due to lack of control over position and diameter, thus inhibiting low-loss optical cavity design with sufficient material gain[12,13], while avoiding highly detrimental surface recombination[14]. In some cases, the resonant cavity and the NW active region require separate lithography and processing steps[7,8]. In other cases the cavity is simply limited by optical losses at the facets[9–11]. As a result, NW-laser demonstrations to date have large threshold power densities and awkward external coupling schemes making them impractical for large-scale integration. Typical reported values of threshold power density range from ~100 kW/cm^2 to >1 MW/cm^2 and require femto-second pulses. Furthermore, most reported NW-based lasers are multimode, which can limit their utility for communications and multiplexing applications.

In order to overcome these problems and realize a practical NW-based laser solution, a high-*Q* cavity with effective surface passivation is necessary. Of the different possible candidates for high-*Q* optical cavities, PhC nano-cavity resonators[15] are an attractive choice due to small

mode volume[16], high spontaneous emission coupling factor[16,17], and low threshold power. In this work, we implement a "bottom-up" technique where the PhC cavity is formed entirely by III-V NPs using catalyst-free selective-area metal-organic chemical vapor deposition[18]. The resulting device is fundamentally different in that it uses a NP ensemble rather than a single NW to form both active region and cavity. This approach is enabled by accurate control of position and diameter of the NPs, whereby the photonic band-gap and active gain region are grown simultaneously from a masked substrate. By carefully engineering the geometry and heterostructures of the NPs forming the cavity, we achieve low-threshold single mode lasing at room-temperature.

4.2 NANOPILLAR PHC LASER STRUCTURE

The NPs forming the PhC lasers implement a GaAs/InGaAs/GaAs axial heterostructure for accurate placement of gain within the cavity[19], while radial growth of InGaP shells provides *in-situ* passivation. The selective-area grown NPs take the equilibrium shape determined by environmental growth conditions with the resulting side-wall facets consisting of the {1-10} family of crystal planes[20]. The resulting pillar side-walls are perfectly vertical and have atomic scale roughness[21,22], which inherently avoids two major contributions to loss in top-down PhC cavities[23,24]. Both pillar placement and diameter, which fix cavity resonance wavelength and *Q*, are determined lithographically. Thus, the cavity resonant wavelength can be designed arbitrarily. Furthermore, the same patterns used to define the position and diameter of the NPs also include optical alignment marks for device integration.

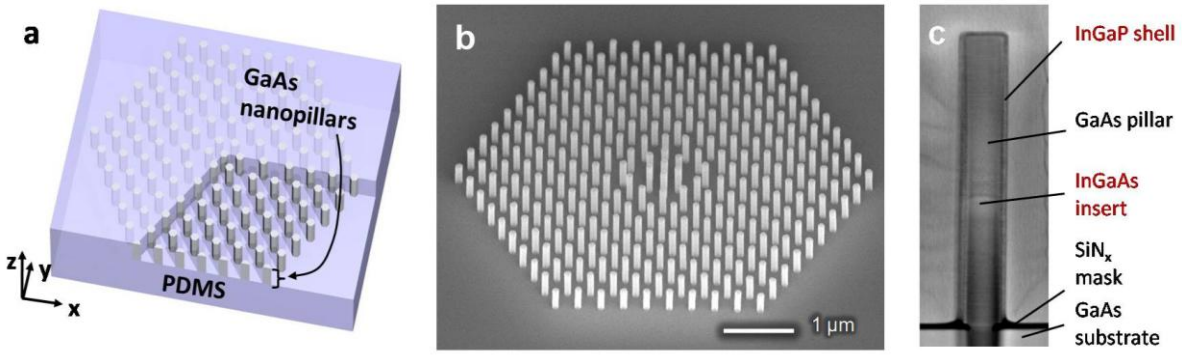

Figure 1. (a) Schematic diagram of the NP PhC lasers in PDMS. (b) 45° tilted SEM of a NP PhC as grown on the substrate. (c) Cross-section STEM of a NP showing the InGaAs insert located at the center of the pillar and InGaP shell.

The bottom-up PhC lasers consist of NPs embedded in polydimethylsiloxane (PDMS) as shown in Figure 1(a). The NPs are first grown on a SiN_x masked GaAs (111)B substrate. Following growth, PDMS is drop cast to a thickness of ~1 mm and cured in atmosphere. The PDMS film is then removed mechanically from the growth substrate. During the PDMS lift-off, the NPs are broken at the base making the patterned substrate reusable for additional growths. The resulting structure forms the complete laser cavity, where the NPs are surrounded by PDMS on all but the top side where they are exposed to air.

Figure 1(b) shows an SEM image of a typical NP PhC laser as grown on the substrate. Each device is a 5 µm × 5 µm array of hexagonally-packed pillars which comprise the resonant cavity, surrounding seven central pillars which form the laser active region. The cavity *Q* and resonant wavelength are lithographically-defined by NP diameter and pitch, respectively. A 4 × 6 matrix of cavity arrays is patterned across the growth substrate for controlled variation in both pillar diameter (100 - 130 nm) and inter-pillar pitch (324 - 342 nm). A microscope image of the device array matrix embedded in PDMS is shown in Appendix A.

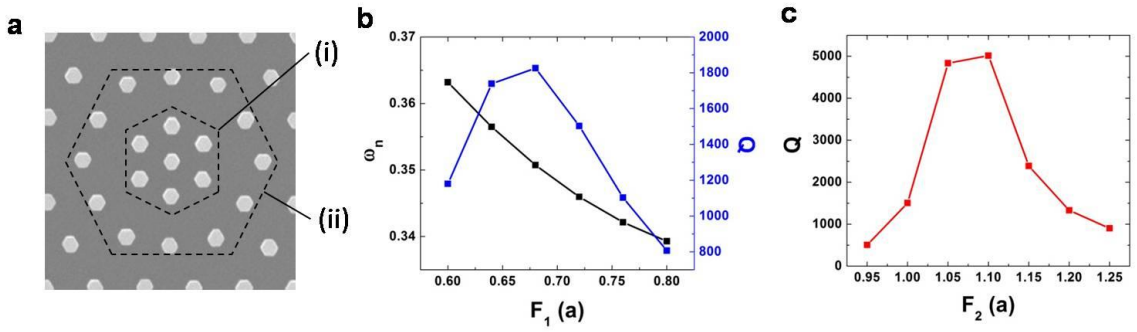

Figure 2. (a) Top-down SEM image of the NPs forming the high-*Q* cavity. The two hexagonal contours labeled (i) and (ii) show the regions where the NP positions were optimized. (b) The *Q* and frequency dependence on the NP spacing in region (i). (c) The *Q* dependence on the NP spacing in region (ii).

A cross-section scanning transmission electron microscope (STEM) image of a single representative NP from one of the cavities is shown in Figure 1(c). The pillars are ~730 nm tall and 120 nm in diameter with about 5-10% height variation from center to edge of a cavity and are comprised of both an axial and a radial heterostructure. The axial double-heterostructure is formed by a well-placed 130 nm $In_xGa_{1-x}As$ insert, where x is measured to be ~15% from both the spontaneous emission peak wavelength and energy dispersive x-ray spectroscopy scan. The lateral heterostructure is formed by a 5 nm lattice-matched InGaP shell to reduce surface recombination. The details of the patterning process and growth conditions are described in more detail in Chapter 3.

4.3 FDTD Simulation and Cavity Optimization

3-D finite-difference time-domain (FDTD) simulations are employed to optimize structural parameters such as the height, radius, and the locations of the NPs. The cavity is formed by modifying the original lattice points of the triangular photonic-crystal as shown in Figure 2(a). The cavity consists of two separate sub-regions defined by the two hexagonal contours labeled (i) and (ii). For the inner region (i), the six pillars are rotated by 90° with respect

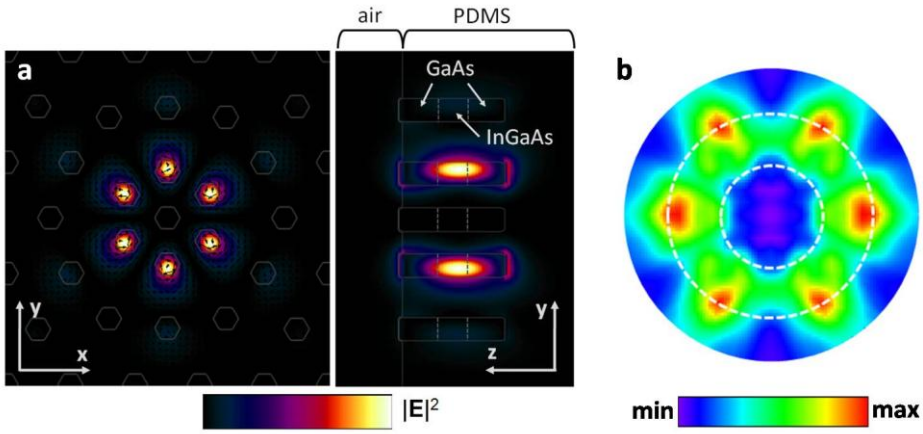

Figure 3. (a) Top-down view of the vector field pattern of the magnetic-field (H_x, H_y) overlaid upon the electric-field intensity ($|\mathbf{E}|^2$) distribution within the cavity showing the hexapole mode overlapping six center NPs and cross-section view of $|\mathbf{E}|^2$ within the cavity showing the overlap with the InGaAs inserts. (b) Far-field radiation pattern of the cavity hexapole mode. The far-field data over the upper hemispherical points (θ,ϕ) is represented in (x,y) by the mapping defined by $x=\theta\cos\phi$ and $y=\theta\sin\phi$.

to the center pillar position. The distance is then scaled down from the center by a factor of F_1. Figure 2(b) shows the change in cavity Q and normalized resonant frequency ω_n as a function of F_1. It should be noted that Q and the frequency of the mode are critically dependent on F_1, since the majority of the mode energy is concentrated within these six pillars. For the outer region (ii), the twelve pillar positions are arranged in a circle and fine tuned by the scaling factor F_2 to optimize Q as shown in Figure 2(c).

A top-down and cross-sectional view of the electric-field intensity distribution ($|\mathbf{E}|^2$) in the cavity is shown in Figure 3(a). The final arrangement of the NPs in the center of the cavity forms a non-degenerate hexapole mode[25]. The positions of the neighboring pillars are modified to maximize the cavity Q while keeping the resonant frequency close to the center of the PBG in order to maintain a large spontaneous emission factor β. The final result of this design optimization yields a simulated cavity Q of 4,600 with an effective mode volume V_{eff} of 0.137 $(\lambda/n)^3$. In the cross-sectional view of Figure 3(a), the location of the InGaAs inserts is highlighted

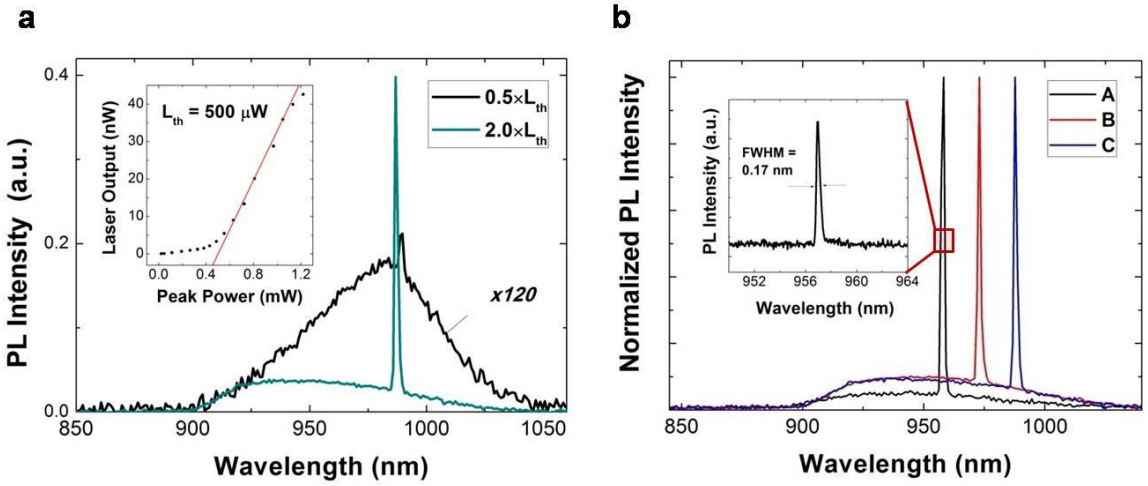

Figure 4. (a) Emission spectra of a NP-PC laser emitting at 989 nm both at $0.5\times L_{th}$ and $2\times L_{th}$. Inset shows *L-L* curve of the same device with a threshold of 500 μW peak pulse power. (b) Comparison of devices A, B, and C with different pitch and diameter NPs that emit at wavelengths between 960 and 990 nm. Inset shows high-resolution laser spectrum of device A with a FWHM of 0.17 nm.

to show the confinement of carriers to the field anti-node. Based on the insert length as a fraction of the total pillar, the energy confinement factor Γ and threshold gain g_{th} are calculated with group index and material dispersion of bulk InGaAs[26]. With an insert length that is 18% of the total height as measured by STEM, this method yields $\Gamma = 0.185$ and $g_{th} = 197$ cm^{-1}.

4.4 NANOPILLAR PHC LASER CHARACTERIZATION

The devices are optically pumped using a pulsed semiconductor laser with a 660 nm peak wavelength, 10 μm diameter spot size, and 16 ns excitation pulse at a 1 MHz repetition rate. A 50× microscope objective oriented at 45° to the surface normal is used to both excite the NPs and collect emission. Simulated far-field radiation patterns[27,28] of the cavity resonant mode (Fig. 2B) show that the laser emission should be directed 50° - 70° from normal. Figure 4(a) shows emission spectra from one array both below and above threshold at pump powers of $0.5\times L_{th}$ and $2\times L_{th}$. Below threshold, the spectrum is the integrated emission from all NPs within the array including cavity and active region. The spontaneous spectrum is peaked near 975 nm with

FWHM of 65 nm. Even at this very low pump power, the resonant cavity mode can be detected. The characteristics of the sub-threshold cavity emission has not yet been analyzed as stimulated or spontaneous. The FWHM of the modal peak is approximated to be 0.45 nm, which corresponds to an experimental cavity Q of ~2000. At $2\times L_{th}$, the spectrum is dominated by a single peak at 989 nm. The corresponding L-L curve for this device, shown as the inset, indicates a lasing threshold of 500 μW peak pulse power or 625 W/cm^2 peak power density. The output power increases linearly until above $2\times L_{th}$ where the device emission begins to saturate, reaching an estimated peak output power of 42.5 nW at the InGaAs detector.

The model used to predict the ideal Q required threshold gain gives g_{th} = 197 cm^{-1}. However, with the measured cavity Q of ~2000, an actual threshold gain of g_{th} ~ 500 cm^{-1} is predicted. Since InGaAs bulk gain can be expected to reach >1000 cm^{-1} at room temperature with moderate carrier densities, the measured L-L curve and consequent lasing threshold appear to be in reasonable agreement with the predictions of the model. This combined with the measured data provide strong evidence that the devices achieve single mode lasing at low threshold power density. Additionally, the fact that these estimates are based on gain in bulk InGaAs indicates the effectiveness of the InGaP shells used for surface passivation since the threshold for unpassivated InGaAs with the given surface to volume ratio would not be achievable at room temperature.

Figure 4(b) shows a comparison of three devices at ~$2\times L_{th}$ which demonstrates the ability to control lasing wavelength lithographically. The devices A, B, and C are designed to have the cavity resonance at 950, 970, and 990 nm, which correspond to pillar pitch a of 324 nm, 331 nm, and 338 nm, respectively. This allows control of the wavelength with pitch by $d\lambda/da$ = 2.1. However, the final height of the grown pillars does not match the target height from the

optimized design due to both inaccuracy of the growth time of the pillars, as well as the difference in growth rate between devices due to difference in diameter. The resulting peak wavelengths are 960 nm, 974 nm, and 989 nm. A high resolution scan of the laser spectrum of device A, in the inset, shows a FWHM of 0.17 nm.

4.5 CONCLUSIONS

The bottom-up approach to NP-PhC lasers introduces many design possibilities, which cannot be realized with the top-down PhC devices. Based on the measured threshold power density, we expect that further design optimization of the NP PhC cavities and increased InGaAs insert thickness will reduce the threshold gain by a factor of 4 or 5 to achieve continuous wave, room temperature operation. Additional modification of NP position and diameter within the cavity will enable engineering of the far-field emission pattern[29,30]. The current design featuring NPs embedded in PDMS can be useful as internal light sources for spectroscopy in microfluidic and biosensing systems, especially since the patterned growth substrate can be reused after PDMS lift-off. In parallel, we are exploring on-chip integration utilizing a dielectric core-cladding stack to achieve out-of-plane optical confinement while the NPs remain on the growth substrate. Finally, with the narrow linewidth and lithographic control of wavelength, these devices are promising for on-chip wavelength division multiplexing applications.

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Chapter 5

5.1 Background of Nanowire-Based Light-Emitting Diodes

Semiconductor nanowires (NWs) and nanopillars (NPs) have drawn increased interest in recent years due to several advantages over planar epitaxial methods. The ability to form defect free interfaces between highly lattice mismatched materials[1,2], as well as the ability to control axial and core-shell growth with specific composition[3–5] offers flexibility not achievable with planar growth. This has led to a number of optoelectronic device demonstrations, including photodetectors[6–8], light-emitting diodes (LEDs)[9–13], and lasers[14–18]. However, a common criticism of these devices is that they exhibit significantly higher leakage current densities and forward operating voltages than their planar counterparts. This discrepancy is due to surface state and contact effects that are highly dependent on the heterostructure and geometry used in the device.

So far, NW-based devices either implement an axial or a core-shell heterostructure in the form of a *p-n* or *p-i-n* diode. Each approach is limited by either mid-gap surface states or the metal-semiconductor interface. Axial heterostructures have the advantage of the lower band-gap radiative region centered along the length of the NW so that it is well separated from the contacts. However, the large surface-to-volume ratio results in several detrimental effects due to mid-gap surface states: (i) non-radiative recombination which can severely limit the material gain, carrier lifetime, and diffusion length[19], (ii) generation of carriers in reverse bias leading to high leakage current, and (iii) depletion of the nanowire core leading to space-charge limited transport and high series resistance[20]. Core-shell heterostructures may have a larger band-gap material for the shell to reduce surface recombination, but do not have good separation between the active region and the metal contact. Any band bending at the metal-semiconductor interface

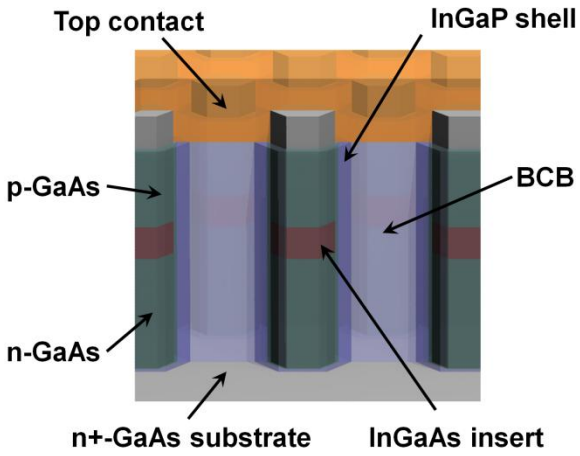

Figure 1. Schematic of the NP-LED device structure depicting the axial *n*-GaAs/*i*-InGaAs/*p*-GaAs heterostructure and InGaP shell.

due to trap states or a Schottky barrier in core-shell heterostructures can deplete a significant portion of the junction given the small cross section of the NWs[21,22]. In addition to diminished device performance, these effects also compromise electronic characterization such as capacitance-voltage measurements.

5.2 NANOPILLAR LED DEVICE DESIGN AND STRUCTURE

In this work, we demonstrate a method of maintaining contact separation from the active region while simultaneously having surface passivation by implementing a composite axial/core-shell heterostructure. The formation of the axial/core-shell heterostructure is enabled by catalyst-free selective-area epitaxy of III-V NPs. In this case, the active region is placed arbitrarily along the length of the NP by using an axial n-GaAs/i-InGaAs/p-GaAs heterostructure, while an i-InGaP shell is used to prevent non-radiative recombination and surface depletion. The narrow pillar diameter allows for a larger than normal In composition resulting in 1.3 μm emission, while surface passivation *in-situ* results in low reverse bias leakage and ideality factor comparable to planar devices.

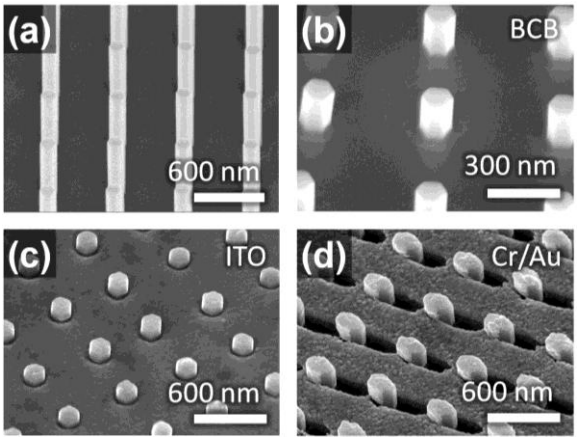

Figure 2. (a) SEM images of NPs as grown on the GaAs substrate. (b) Exposed NP tips after planarization/etch-back of BCB and selective InGaP chemical etch. (c) NP tips coated with ITO contact. (d) NP tips coated with Cr/Au contact layer.

The device structure used for the NP-LEDs is shown in Figure 1. The III-V NPs are grown by selective-area metal organic chemical vapor deposition on masked n+ doped GaAs (111)B substrates. The growth sequence is divided into two major segments. First, an axial n-GaAs/i-InGaAs/p-GaAs heterostructure is grown at 730°C, followed by i-InGaP shell growth at 600°C. The masking process and growth conditions are reported in more detail elsewhere[23]. The n-dopant used was tetraethyltin (TESn) and the p-dopant was dimethylzinc (DMZn). Doping calibration was performed with planar GaAs films to determine the Ga/Sn and Ga/Zn ratios, with both n and p doping levels in the NP estimated to be ~3×10^{17} cm^{-3}. The InGaP shell is undoped in order to ensure no parasitic junctions are formed between the shell and axial segments. For comparison, an additional sample was grown with only the axial heterostructure. The resulting NPs are 150 nm in diameter and 1.2 μm in height. Cross-sectional transmission electron microscopy of samples grown under the same conditions shows the length of the InGaAs segment to be 100 - 115 nm with an InGaP shell thickness of 5 nm.

A scanning electron microscope (SEM) image of the as-grown NPs is shown in Figure 2(a). Following growth, the NPs are planarized using bisbenzocyclobutene (BCB) and hard-

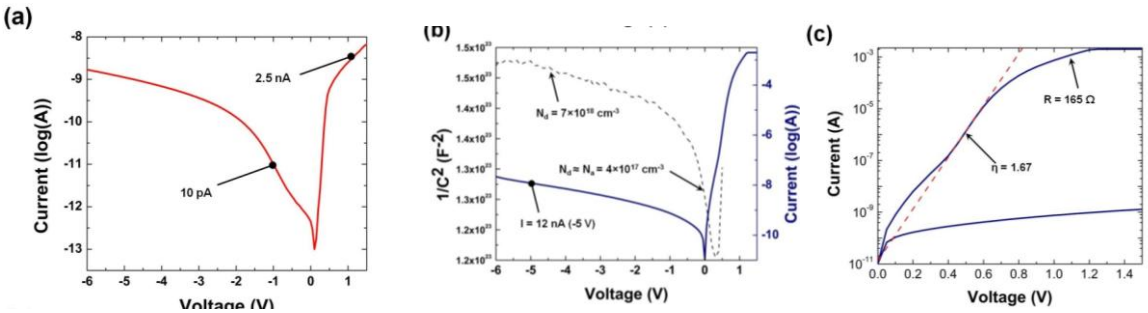

Figure 3. (a) Semi-log plot of the axial-only diode I-V characteristic. (b) Semi-log plot of axial/core-shell diode I-V characteristic (solid line) and C^{-2}-V characteristic (dashed line) with extracted NP doping level of ~4×10^{17} cm^{-3} and substrate doping of 7×10^{18} cm^{-3}. (c) Detailed I-|V| characteristic showing ideal diode fit (dashed line) with an ideality factor of $\eta = 1.67$ and series resistance $R_s = 165$ Ω.

cured at 250°C. A AuGe/Ni/Au film is deposited on the backside of the n+ GaAs substrate and annealed at 400°C for 30s to form an ohmic contact. The BCB film is then etched back using a reactive ion etch plasma to expose ~100 nm of the NPs, followed by a selective H_3PO_4:HCl (7:1) chemical etch of the InGaP shell to expose the p-GaAs core as shown in Figure 2(b).

Each 1 cm^2 sample contains four 500 µm × 500 µm arrays of NPs. The devices were fabricated so that two of the arrays have 25 nm indium tin oxide (ITO) top contacts and two of the arrays have 20 nm/100 nm Cr/Au top contacts using RF plasma sputtering and tilted electron-beam evaporation, respectively. Close-up SEM images of the ITO and Cr/Au contacts are shown in Figures 2(c) and 2(d). The purpose of the different contacting methods is to achieve good light extraction from the ITO coated NPs, while the Cr/Au provides an ohmic contact in order to ascertain the true *p-i-n* junction characteristics without obstruction from any Schottky barrier formed between ITO and GaAs.

5.3 NANOPILLAR LED OPTICAL AND ELECTRICAL CHARACTERIZATION

The I-V and C^{-2}-V characteristics of the Cr/Au contacted NP arrays are shown in Figures 3(a) and 3(b). Measurements were performed using an Agilent 4156C semiconductor parameter

analyzer and E4981A capacitance meter. The I-V measurements extend from -6 V to 2 V. First, the NP array with only the axial heterostructure is shown in Figure 3(a). As expected, the device has a high series resistance of > 1 MΩ, and a low rectification ratio of 2.5×10^{2} at +/- 1 V. The composite axial/core-shell NP array is shown in Figure 3(b). The rectification ratio at +/- 1 V is 10^{6}, while the leakage current at -5 V is 12 nA. Since a phase angle of close to 90° is needed for impedance measurements, only in the axial/core-shell sample were reliable C^{-2}-V characteristics able to be acquired. The C^{-2}-V characteristic shows two distinct carrier densities. At large reverse bias voltages, the C^{-2} slope results in a calculated carrier density of 7×10^{18} cm^{-3}, while at small reverse bias voltages, the C^{-2} slope results in a carrier density of 4×10^{17}. Here the cumulative *p-i-n* junction area is taken to be 3.1×10^{-5} cm^{2} from the area of all the NPs in the array. This measurement is within reasonable agreement with the doping concentration of $>10^{18}$ cm^{-3} in the n+ GaAs substrate and target doping concentration in the NP to be 3×10^{17} cm^{-3}. Additionally, the capacitance at zero-bias indicates a junction width of 122 nm, which meets the expected width of the intrinsic region.

A detailed semi-logarithmic plot of the I-|V| characteristic for the axial/core-shell NP array is shown in Figure 3(c). The forward bias curve shows a typical transition from recombination current to diffusion current, followed by high-level injection and series resistance. An ideal diode curve is fit to the diffusion current region with a resulting ideality factor of $\eta = 1.67$. The series resistance is then calculated to be $R_s = 165\ \Omega$ using the equation $R_s = \Delta V/I$. In comparison to other reports of NP-LEDs in this materials system[12], the ideality factor and reverse bias leakage current are significantly lower for a similar number of NPs. Since the NPs do not use a Au catalyst, we expect that generation and recombination currents will primarily deviate from planar devices due to surface states which have a density of $\sim10^{14}$ $cm^{-2}eV^{-1}$ in

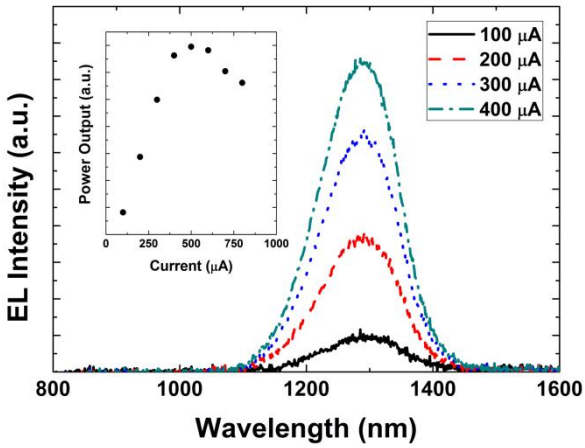

Figure 4. Current dependent EL spectra with emission peak at 1290 nm. Inset shows power output vs. input current with linear behavior at low current densities followed by saturation under high-level injection.

GaAs[24]. Any depletion region at the surface can also give rise to leakage current and high series resistance. For GaAs NWs in particular, both AlGaAs and InGaP shells have been demonstrated to remove this effect[25,26]. Furthermore, the low ideality factor is close to planar GaAs diodes which typically have factors ranging from 1.1 to 1.5.

The current-dependent electroluminescence spectra from one of the ITO contacted NP axial/core-shell arrays is shown in Figure 4. The NP-LEDs were electrically driven with a constant current source ranging from 100 - 800 μA at room temperature. A 50× long focal length microscope objective is used to collect emission from the sample which is imaged and spectrally resolved using a liquid nitrogen cooled InGaAs focal plane array. The measured emission was integrated over a 20 μm × 20 μm area containing ~10^3 NPs. The resulting emission peak is measured to be 1290 nm with a full width half maximum of 145 nm. The integrated output power is shown to increase linearly up until 400 μA (59 A/cm^2), above which the emission saturates and then decreases slightly and at 1 mA (148 A/cm^2) the ITO contact breaks down.

Since there was no observed shift the EL peak wavelength, this is likely due to joule heating in the ITO film, which had a measured sheet resistivity of 634 Ω/□.

5.4 CONCLUSIONS

In summary, we have demonstrated NP-LEDs utilizing a composite axial/core-shell heterostructure with peak emission wavelength at 1.3 μm. The combination of axial current injection as well as *in situ* passivation leads to device performance close to that of planar grown GaAs emitters. The electroluminescence intensity increases linearly until 59 A/cm^2, where the emission saturates. In terms of material gain, this current density should result in a gain coefficient of ~800 cm^{-1} for InGaAs. If placed in an optical cavity with a *Q* of 3000 or greater, this may be sufficient for room temperature lasing. Since the NPs reported here rely solely on the band offset between the undoped InGaAs region and doped GaAs regions for carrier confinement, future improvements can be made by incorporating Al or P to form diffusion barriers on either side of the active region. In all, we believe the device performance of the composite axial/core-shell NP-LEDs makes it a promising a approach to future NP or NW based emitters.

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Chapter 6

6.1 Nanowire-Based Light-Emitting Diode Heterostructures

Semiconductor nanowires (NWs) and nanopillars (NPs) have been the subject of intense research because of their promise in new nanoscale electronic and optoelectronic devices. Much of their potential is derived from the ability to form complex axial and radial heterostructures that are either impossible or not easily attained using planar epitaxy. Different combinations of axial and radial heterostructures have been implemented in light-emitting diodes[1–3], lasers[4,5], photodetectors[6,7], and solar cells[8]. In terms of light-emitting devices, the predominant application of NWs has been in the visible wavelength range for future solid-state lighting, with only a few examples of devices operating in the near-infrared[9,10]. Being less developed, the near-infrared devices are missing one of the key components to making a high internal efficiency emitter: an axial high band-gap barrier to limit diffusion of carriers past the active region.

In planar GaAs-based emitters, the typical choice for the diffusion barrier layer is $Al_xGa_{1-x}As$, as it is lattice-matched for any composition *x*. For GaAs NW- or NP-based emitters the use of AlGaAs as a barrier has been demonstrated, but the propensity of Al to adhere to the surrounding substrate and NP sidewalls limits the use of AlGaAs to core-shell-type heterostructures[11]. These core-shell-type emitters require a radial current injection scheme, placing the active region in close proximity to the metal contact, which can be highly detrimental to device performance because of band-bending and recombination at the semiconductor/metal interface. For many applications, an axial current injection scheme is necessary in order to maintain separation between the active region and contacts[12,13]. If an axial current injection scheme is used, then axial heterostructures must also be used to form the diffusion barriers.

6.2 Forming Axial Diffusion Barriers with GaAsP Inserts

In this work, we demonstrate the growth and application of axial GaAsP diffusion barriers in GaAs NPs. The lattice mismatch between GaAs and GaAsP limits the critical thickness of the barriers in planar devices to avoid dislocation defects. In NP devices, however, the greatly reduced lattice matching requirements of axial heterostructures alleviates this problem to a large extent[14,15], making GaAsP a strong alternative choice for the barrier material instead of AlGaAs. Furthermore, the switching of column-V precursors during growth is shown to produce more abrupt interfaces than column-III switching, and GaAsP alloys with 10-20% Phosphorus have reduced non-radiative recombination from surfaces, defects, and interfaces compared to GaAs and InGaAs[16].

In order to properly implement the axial GaAsP heterostructures in any device, a detailed study of the material growth and electronic properties is necessary. With planar structures this characterization would normally be accomplished with a combination of photoluminescence and capacitance-voltage measurements. In NPs, however, the impact of the three-dimensional geometry makes it either difficult or impossible to deconvolve the non-ideal effects of the surfaces and interfaces on these measurements. Therefore, an alternate set of measurements and characterization is needed to circumvent these effects. In this case, we use energy-dispersive x-ray (EDS) measurements and temperature-dependent current-voltage characteristics to determine the compositional dependence on growth conditions and the electronic band-offsets, respectively.

The NP arrays and devices used in this study were grown by selective-area metal-organic chemical vapor deposition with nanopatterned SiO_2 on GaAs (111)B substrates. The details of the growth and selective-area mask patterning process are described in more detail elsewhere[17]. In order to accurately characterize and apply the GaAsP axial barriers using the aforementioned

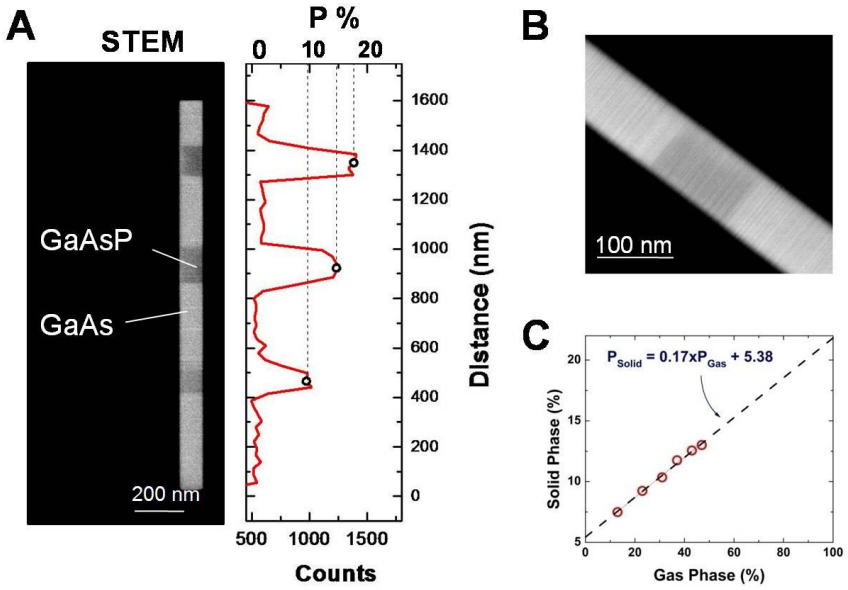

Figure 1. (a) STEM image of a GaAs NP with multiple GaAsP inserts with EDS data of Phosphorus composition as a function of distance along the length of the NP. (b) Magnified STEM image of one of the GaAsP inserts showing the abrupt transition between materials. (c) Plot of Solid Phase vs. Gas Phase composition of GaAsP extracted from EDS data from the axial GaAsP inserts.

techniques, three different types of NP structures were grown: (i) NPs with multiple i-GaAsP inserts in i-GaAs with varied Phosphorus composition, (ii) NP arrays with single n-GaAsP inserts in n-GaAs with InGaP passivation, and (iii) axial n-GaAs/i-InGaAs/p-GaAs NP light-emitting diodes with and without GaAsP barriers.

6.3 TEM AND EDS ANALYSIS OF GAASP INSERTS

The first type of NP structure, GaAs NPs with multiple GaAsP inserts, is used to characterize the growth of the axial GaAsP segments by scanning transmission electron microscopy (STEM) and EDS. An example NP and data from these measurements is shown in Figure 1. Three samples, each with three GaAsP inserts of varying composition, were used to relate the gas phase composition of Arsenic and Phosphorus with the solid phase composition and observe any relevant structural changes or defects. In order to maintain simplicity in the growth, the GaAsP inserts were formed only by the addition of tertiary-butyl-phosphine to the

gas mixture while the temperature, tri-methyl-gallium, and tertiary-butyl-arsenic flow rates were all held constant.

Following growth, the NPs were scraped and deposited on TEM grids for measurement. An STEM image of a NP from the first of the three samples is shown in Fig 1(A), where the image contrast shows the GaAsP segments as darker regions along the length of the NP. A close-up image of one of the inserts is in Fig. 1(B), showing the abrupt transition from GaAs/GaAsP. In all three growths, a 10 min GaAs segment is grown followed by alternating 2 min GaAsP and 2 min GaAs segments. For the growth represented in Fig. 1(A), the Phosphorus gas phase composition used in the GaAsP segments was varied from 7% to 16% as calculated from the gas flow rates into the chamber. By using the *P/(As+P)* method, the Phosphorus composition as a function of position along the NP was extracted from an EDS scan as shown plotted adjacent to the STEM image in 1(A), and the overall composition of each segment was taken to be the average of the EDS data points.

The imaging and composition measurements were repeated for the second and third growths, with the collective data of gas phase vs. solid phase composition shown in Fig. 1(C). For the range of gas phase compositions between 7% and 50%, the incorporation of phosphorus into the solid is linear, as shown by the fitting in 1(C). At higher gas phase compositions from 60% to 80%, the GaAsP segments transition from an axial to a core-shell heterostructure. In this composition range, the strain fields are noticeable in TEM images and the uniformity of the NP arrays decreases, as the NPs have different oblong cross-sections rather than hexagonal cross-sections. Further details of these effects are shown in Appendix B.

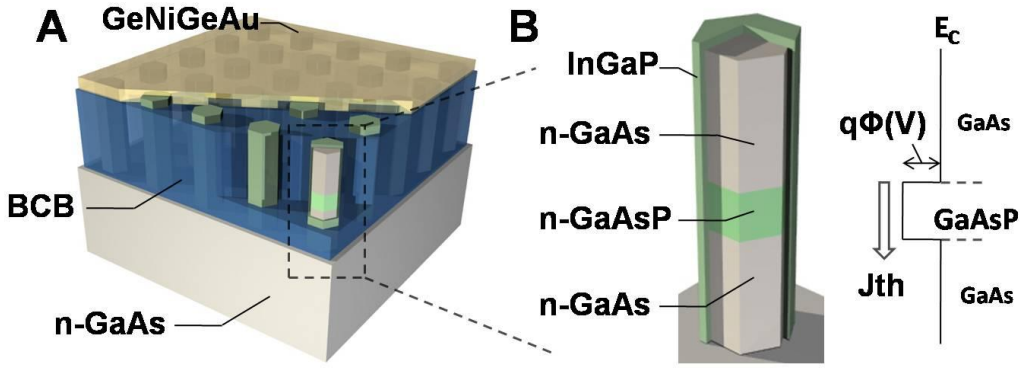

Figure 2. (a) Schematic of the device structure used to measure the conduction band offset of the GaAsP inserts. (b) Detailed view of the NP heterostructure and (c) conduction band-edge diagram illustrating the thermionic emission limited current flow through the device.

While different temperature and gas flow ratios may impact the phosphorus incorporation rate into the solid, we limit the present work to a fixed set of growth conditions for both GaAs and GaAsP to make device applications of the GaAsP barriers more practical. In this case, the presented data shows an upper limit of about 14% phosphorus in the solid phase while maintaining an axial heterostructure with high-uniformity NP arrays. This composition corresponds to a band-gap of 1.58 eV. This energy is 165 meV greater than the band-gap of GaAs, which is sufficient for significant blockage of carrier diffusion at room temperature, given an appropriate conduction and valence band offset of the two materials.

6.4 Single GaAsP Insert Devices and Band-Offset Measurements

In order to determine the relative band-offset between the axial GaAsP and GaAs, a series of temperature-dependent current-voltage measurements must be performed to extract the barrier height from thermionic emission. To accomplish this task, NP devices with the second type of structure described above were grown and fabricated as illustrated in Figure 2(A). In this case, arrays of ~50,000 NPs are used so that a sufficiently large current is measurable over a wide range of temperature and bias. The NP heterostructure shown in 2(B) consists of an n-

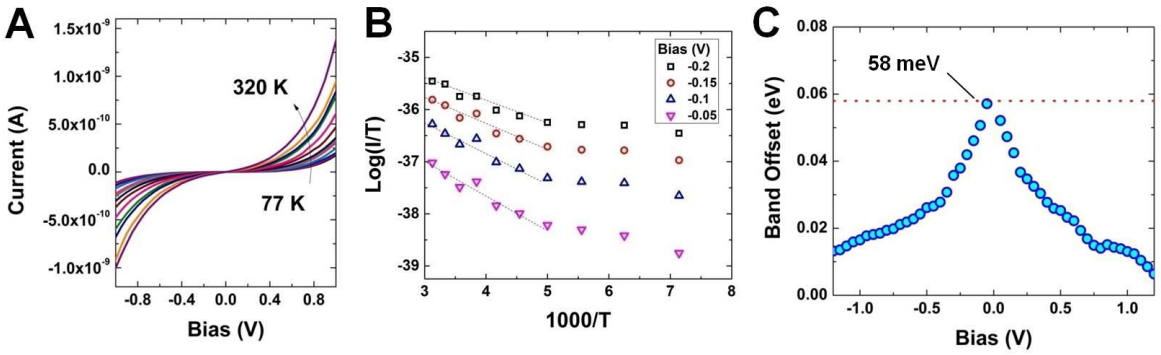

Figure 3. (a) Temperature dependent I-V curves ranging from 77 to 320K. (b) Arrhenius plot of the current as a function of temperature for several bias points and linear fitting used to calculate band offset. (c) Extracted band offset as a function of bias voltage and extrapolated zero-bias band offset of GaAsP with 10.5% Phosphorus.

GaAs/n-GaAsP/n-GaAs axial structure with InGaP shells for surface passivation. Here, the contacts to the n-GaAs substrate and n-GaAs top segment of the NP are ohmic Ge/Ni/Ge/Au, so that the band structure of the device is simply the GaAsP barrier with a height equal to the conduction band offset as shown in Figure 2(C).

In unipolar devices such as these with a single barrier, the current is limited by thermionic emission of electrons according to $I \propto T^2 exp\{-q\varphi(V)/kT\}$, with the barrier height $q\varphi(V)$ being a function of voltage. To extract the zero-bias barrier height corresponding to the conduction band offset, the current-voltage characteristic must be acquired over a range of temperatures as shown in Fig. 3(A). This allows the barrier height to be extracted at each bias point via Arrhenius plot. Fig 3(B) shows this method for several bias points where the barrier height is extracted for temperatures between 225-320K, below which the thermionic emission is shows little change with temperature.

The barrier height in eV as a function of bias is shown in Fig. 3(C) over a range of -1 to 1V. The bias dependent height shows a typical inverse u-shape characteristic, where the effective height increases with decreasing bias. From this curve, the zero-bias barrier height corresponding

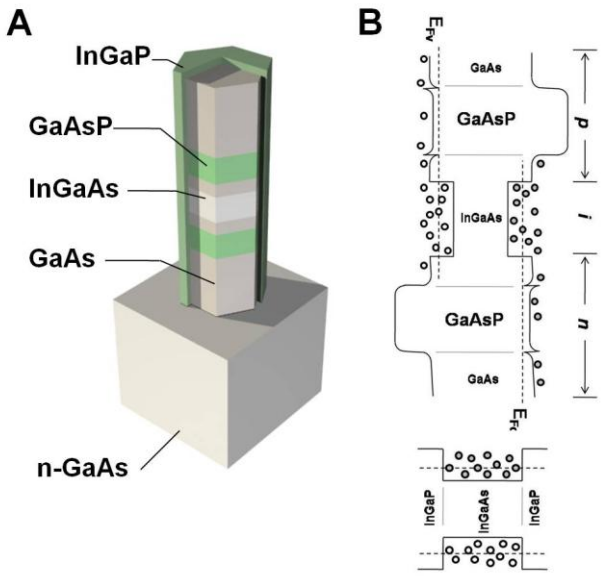

Figure 4. (a) Schematic of the device structure used in the NP-LEDs to demonstrate the application of GaAsP inserts as diffusion current barriers, and (b) electronic band-edge diagrams of the NP in the axial and radial directions.

to the conduction band offset can be extracted. In this case the conduction band offset of the single GaAsP insert is shown to be approximately 58 meV. Given the 10.5% Phosphorus composition of the insert as determined from prior EDS measurements, this corresponds to a band-offset ratio dEc/dEv of 0.8, making the axial GaAs/GaAsP a type-I heterostructure.

6.5 Implementing GaAsP Barriers in Nanopillar LEDs

Having performed characterization of the material composition and electronic band offset of the GaAsP inserts, they can be properly implemented in light-emitting diodes to demonstrate their functionality as diffusion barriers. The device design used to test this effect is shown in Figure 4. The basic NP-LED design is a composite axial/core-shell NP heterostructure consisting of n-GaAs/i-InGaAs/p-GaAs segments for current injection with an InGaP shell for surface passivation. The NP arrays are planarized with bisbenzocyclobutene and contacted with indium-

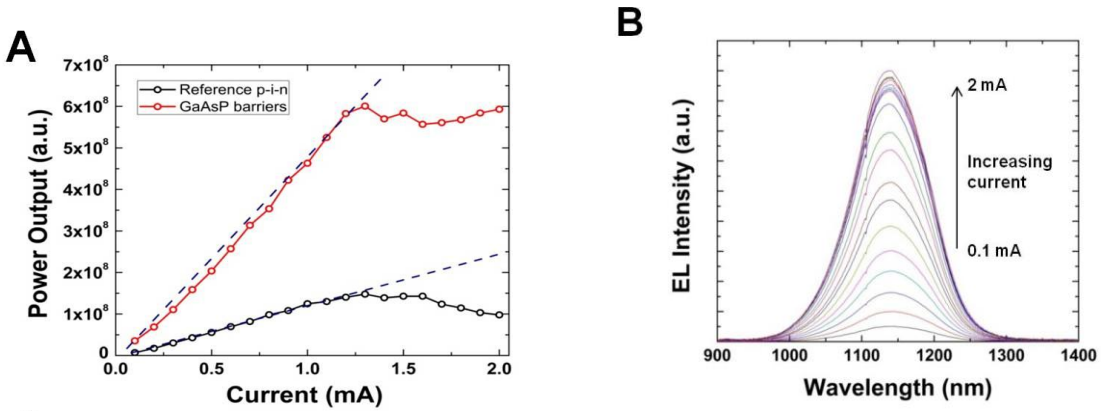

Figure 5. (a) Comparison of the L-I characteristics of the NP-LEDs with and without the GaAsP diffusion barriers, and (b) electroluminescence spectra of the NP-LEDs with GaAsP barriers as a function of input current.

tin-oxide, allowing electroluminescence to be collected vertically from the samples. Further details of the device fabrication and design are reported elsewhere[18].

In order to quantify the impact of the GaAsP barriers on device performance, NP-LEDs were grown and fabricated with and without the GaAsP barriers. The LEDs with GaAsP were grown with the addition of Phosphorus to the n-GaAs and p-GaAs segments with a short 30s break in Phosphorus flow both before and after the i-InGaAs emission region, making the complete axial heterostructure n-GaAs/n-GaAsP/n-GaAs/i-InGaAs/p-GaAs/p-GaAsP/p-GaAs. For consistency with the band offset measurements, the same Phosphorus flow rate corresponding to a composition of 10.5% was used for both GaAsP segments. During the GaAsP growth, the dopant flow rates for both Sn and Zn were increased by a factor of two in order to shift the barrier to predominantly block minority carriers on either side of the junction as illustrated in Fig. 4(B). This combination of axial diffusion barriers with InGaP shells provides a complete three-dimensional confinement of carriers to the InGaAs emission region as shown in 4(B).

The NP-LEDs with and without GaAsP barriers were measured at room temperature using a 50x magnification long focal length objective lens with a monochromator and liquid-nitrogen cooled InGaAs detector. Electroluminescence was produced from the devices by using a source-meter operating in constant current mode. The results of these measurements are shown in Figure 5. At each current point, the total electroluminescence intensity and spectra were collected as shown in 5(A) and 5(B), respectively. The LEDs with GaAsP inserts exhibit a significant increase in output intensity at each drive current compared to those without the inserts, indicating the effectiveness of the diffusion barriers. The increase in quantum efficiency of the NP-LEDs with the diffusion barriers is nearly five-fold over the normal LEDs as extracted from the linear fitting of the *L-I* curves.

Comparison of the electroluminescence spectra of the two devices as a function of current reveals an additional difference in performance. While the LED without barriers maintains the same peak emission wavelength as a function of current, the LED with barriers shows a blue-shift of the peak emission wavelength by ~50 nm. Though the actual electronic density of states in highly twinned NWs or NPs such as these are uncertain, we can estimate based on bulk InGaAs properties that the carrier density increases up to $2x10^{18}$ cm^{-3} before the thermal rollover occurs at high current densities. This value could potentially produce optical gain under current injection, and further improvements in material quality and device design may yield carrier densities sufficient for electrically injected lasers.

6.6 CONCLUSIONS

The characterization and application of axial GaAsP diffusion barriers in NPs enables many design possibilities beyond the enhancement of electroluminescence in NP-LEDs. With the introduction of an axial barrier, other devices such as detectors and photovoltaics can also

benefit. For example, the simple introduction of a diffusion barrier can reduce dark current in photodetectors or serve as a second band-gap material for tandem solar cells. Furthermore, the switching of the column V precursor yields highly abrupt interfaces between GaAs and GaAsP. This fact could be exploited to circumvent issues in producing quantum heterostructures with mixed column III elements, which in prior reports have been shown to suffer from compositionally graded interfaces.

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Chapter 7

7.1 Integration of NPs with Passive Optical Waveguides

Nanowire-based devices have many advantages over their thin-film counterparts because of their complex three-dimensional structures, their integration in larger systems is substantially more difficult and has generally been ignored by the research community. This is primarily due to two reasons: (1) most nanowires or NPs are grown randomly with little control over position and diameter[1–3], and (2) their high aspect-ratios limit the use of standard device fabrication techniques which typically require planar surfaces. In recent years, a few research groups have addressed the problem by implementing modern lithographic techniques including nanoimprint lithography[4] and electron-beam lithography[5–9] to control position and diameter of nanowire growth. The second problem has only been addressed to a small extent, where simple, non-integrated devices such as photodetectors[10–12] and solar cells[13–16] have been demonstrated.

The absence of integrated systems containing multiple nanowire-based devices is due to the fact that passive optical waveguides could not be fabricated around the nanowires as-grown on the original substrate. So far, only a few scarce demonstrations of nanowires integrated

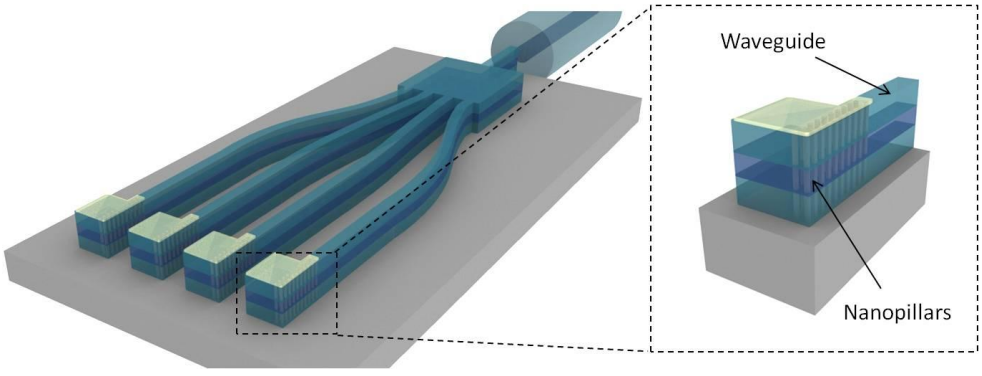

Figure 1. The overall vision of integrating NP optoelectronic devices with planar passive optical waveguides and components, making it possible to link NP devices to fiber.

with waveguides have been shown[17–19]. However, these techniques rely on removing the nanowires from their original substrate and randomly dispersing them on a host substrate. This has only enabled devices to be fabricated on an individual basis, where the waveguide, metal contacts, etc., are aligned to each nanowire or pair of nanowires. In order to overcome these limitations, a technique to fabricate optical waveguides around the nanowires as-grown is necessary to form systems at the chip-scale.

In Fig. 1, We present an approach for monolithic integration of III-V NP devices with passive optical waveguides at the chip-scale. The NPs are distinct from typical nanowires because they are grown by selective-area epitaxy, which allows for accurate control of position and diameter by patterns generated by electron-beam lithography[20,21]. The controlled growth of NPs is done relative to lithographic alignment marks, in order for standard semiconductor process techniques to be used. Passive optical waveguides can then

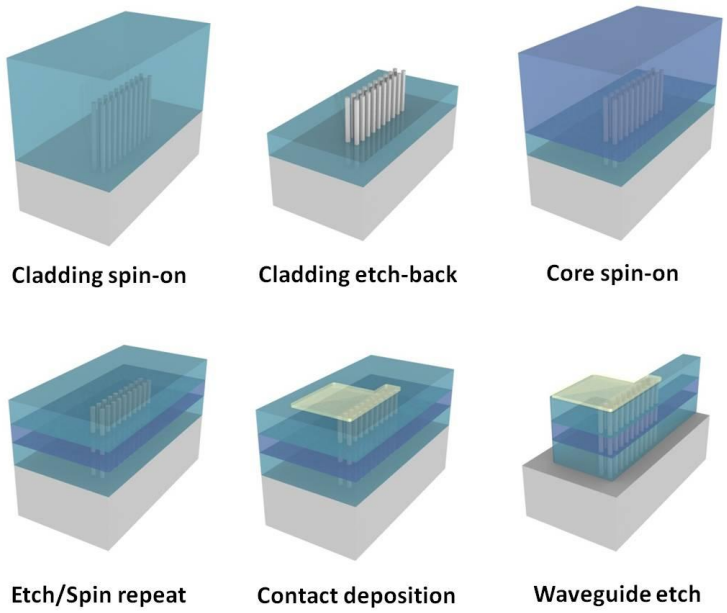

Figure 2. Illustration of the waveguide fabrication process.

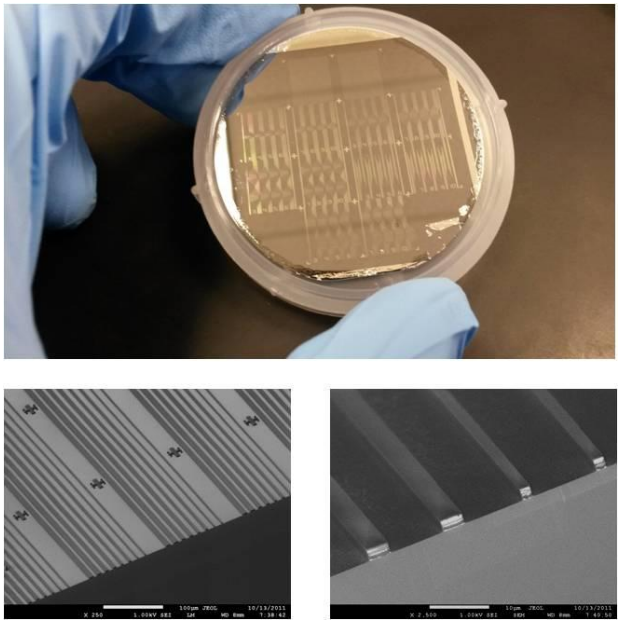

Figure 3. Wafer-scale testing of the polymer waveguides. Photograph shows a 2" Si wafer with waveguides of different lengths and curvature for loss measurements. SEM images show the waveguide ends at the cleaved edge of the substrate.

be fabricated around the NPs by a repetitive planarization and etch-back process with polymers of different refractive indices, forming a planar waveguide layer that is subsequently patterned with photolithography. This enables passive optical waveguides integrated with up to thousands of NP devices at the chip-scale.

7.2 Process Development and Testing of Waveguide Coupling to NPs

An illustration of the waveguide fabrication process is shown in Fig. 2. In this process, the passive waveguide layers are formed by two polymers of different refractive indices. The cladding layer is comprised of CYTOP, with a refractive index of 1.34, and the core layer is comprised of polyimide with a refractive index of 1.7. This refractive index difference is sufficient to provide strong optical confinement perpendicular to the substrate.

Because of the high aspect ratio of the NPs, a multiple coating and etch-back process is used. In each step, the NP arrays are completely planarized by spin-coating the polymer film to a thickness significantly larger than the height of the NPs. Once embedded in the polymer, the uniformity of the planarization can be measured by a surface profilometer. Following planarization, the polymer layer is isotropically etched in an O_2/CF_4 plasma to reduce the polymer thickness to the necessary height of the cladding layer, leaving the NP arrays exposed. This process is repeated for the polyimide core layer and CYTOP top cladding layer. The final structure after the three polymer coating/etch-back is a planar waveguide that covers the entire substrate. This planar waveguide is subsequently patterned using standard optical lithography and dry etching. In the case of electronic devices, the metal contacts are formed by a lift-off process prior to patterning the waveguide layer. A more detailed description of this process is included in Appendix C.

The polymer waveguide process was first tested on Si substrates as shown in Fig. 3. The core-cladding process was on a 2" Si wafer, and the waveguides were patterned using plasma etching and a metal hard mask. After cleaving, the waveguide ends have flat surfaces which light from a microscope objective or lensed fiber can be coupled into the waveguides. The waveguides were successful in propagating light at near-infrared wavelengths and are currently being used for loss measurements to characterize the effectiveness of the waveguide process.

Following the waveguide process testing, the waveguides were tested with NP arrays in order to demonstrate coupling of light both to and from the NPs. For this experiment, NPs with axial InGaAs segments emitting in the 900-1000 nm range were grown in small arrays that can fit within a single waveguide. Samples with ~150 NP arrays were produced on

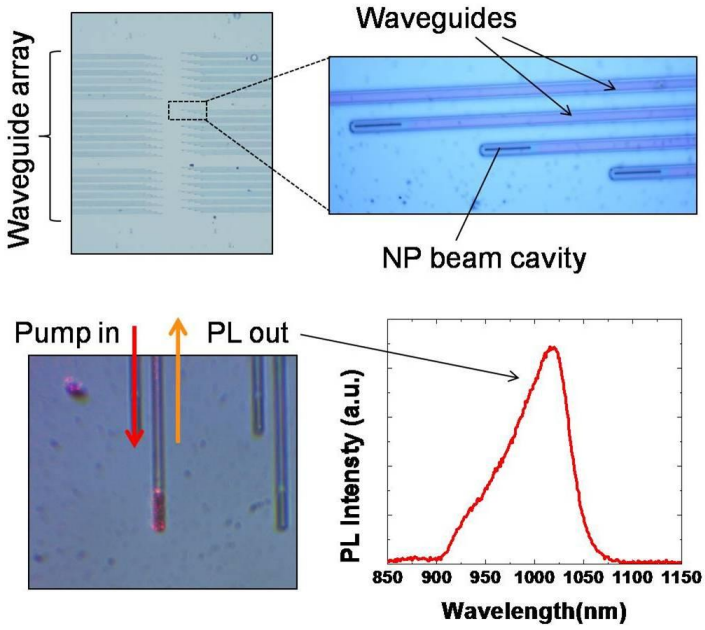

Figure 4. Optical testing of NP arrays in polymer waveguides. Upper left: microscope image of the fabricated die, and close-up view of several waveguides with NP arrays at right. Bottom left: photopumping of a NP array from the edge of the chip with HeNe laser, and collected photoluminescence spectrum from the NP array at the waveguide end.

undoped GaAs substrates and the waveguide fabrication was performed on each 1 cm^2 sample and diced to 2 mm^2 pieces.

After fabricating waveguides around the NP arrays, the devices were tested optically as shown in Fig. 4. The finished dies are 1 x 2 mm and have ~150 NP arrays, each having a separate waveguide between the array and the edge of the die. In order to test the coupling of light to and from the NP arrays, a 50x long focal length objective lens is used to couple light from a HeNe laser into the waveguide at the edge of the chip. Using a vertical microscope, the photopumping of the NP array can be observed in a CCD camera. Under illumination from the HeNe laser, the NP arrays emit light from the InGaAs segments. Part of the photoluminescence is coupled to the waveguide, and the same objective lens used to

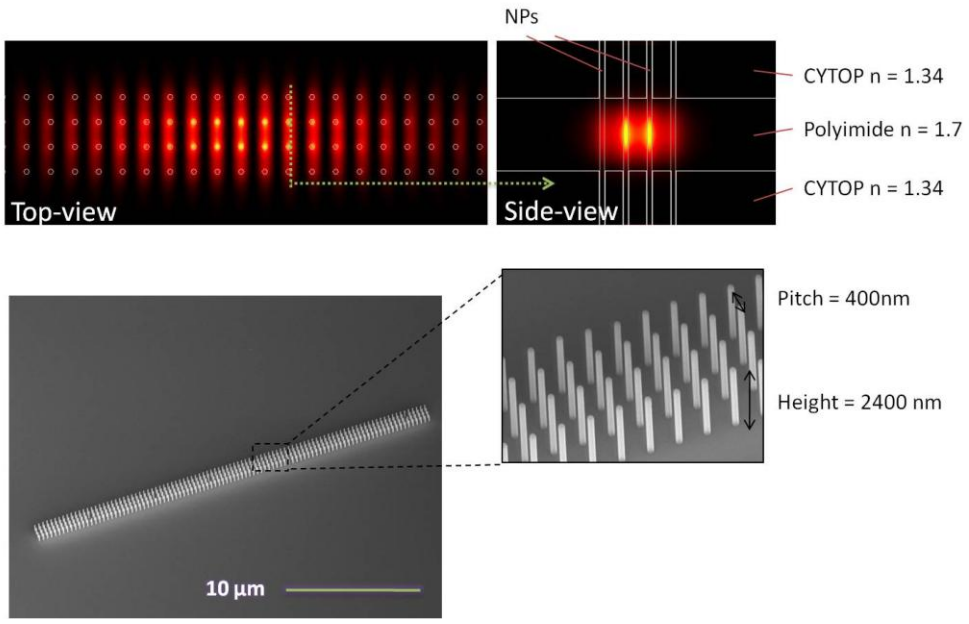

Figure 5. Electromagnetic simulation of the NP photonic crystal cavity embedded in the polymer waveguide, and SEM image of one of the NP arrays before the waveguide fabrication.

couple light into the waveguide is used to collect the emission. The emission is then directed to a spectrometer, where the spectrum is resolved to show that the signal is from the InGaAs band-edge at ~1 µm.

7.3 Photonic Crystal Cavities in Waveguides

After the demonstration of NP array emission coupling to the polymer waveguides, the project diverged into two separate tracks to expedite development. The first track was the testing of NP photonic crystal cavities in the polymer core/cladding structure, and the second was the testing of electrical devices coupled to the polymer waveguides.

In order to form photonic crystal cavities with NPs in the polymer core/cladding structure extensive simulation of the optical properties of NP arrays in the polymers was conducted. This study found that with appropriate pitch and diameter of the arrays, an optical mode

could be produced that was partially overlapping the NPs, but extended far enough into the surrounding polymer layers such that the index contrast between the core and cladding layers could provide vertical confinement of the optical mode. Using a one dimensional photonic crystal cavity design, a high quality factor optical mode could be obtained by modulating the pitch of the NPs in the array with a Gaussian envelope. By tuning the depth and width of the Gaussian envelope, the cavity Q was optimized to high values of greater than 100,000, which is significantly higher than can be realistically achieved with fabrication imperfections.

The end result of the cavity design study is shown in Fig. 5. The finite-difference time-domain (FDTD) simulations in the upper portion of the figure show the top-view and side-view of the final optimized cavity mode. In the top-view, the decay in the optical field intensity due to the Gaussian profile of the NP array is seen. In the side-view, the optical field clearly overlaps the NPs at their center. The optical field is seen to extend into the polymer core, but the index contrast between the core and cladding layers prevents the field from extending far into the cladding layer and substrate.

In the lower portion of Fig. 5 are SEM images of a NP array used in testing the growth of this particular design. Later versions of the design include rows of additional NPs which are used to increase uniformity of the NP growth by preventing edge-effects in the arrays. The additional NPs act as a buffer to maintain uniformity of material during growth, while at the same time the diameters of the "buffer" arrays can be made significantly larger so as to prevent accidentally contacting the buffer NPs in electrically driven devices.

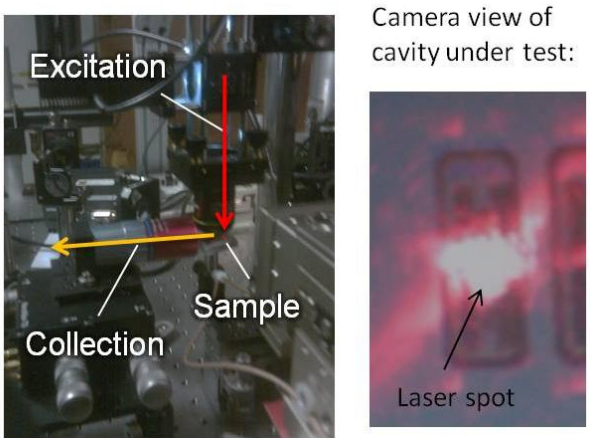

Figure 6. Testing of the NP photonic crystal cavities in the polymer core/cladding structure. Left image shows the experimental setup for optical excitation. Right image shows the microscope view of a device under excitation.

The experimental testing of the fabricated NP photonic crystal cavities is shown in Fig. 6. The setup used for testing was custom built for this particular type of photonic crystal cavity. Because the cavity incorporates the waveguide structure, the emission will be predominantly in-plane. However, the devices must be photopumped out-of-plane, perpendicular to the substrate. For this purpose, an open microscope was built with a 660 nm diode laser attached. The microscope is held above the sample and the laser is projected through the objective lens to the sample. The same objective is used for imaging the sample and positioning the laser on the cavity. A camera image of a cavity being photopumped is shown in Fig. 6.

Using the setup for vertical photopumping of the cavity, the emission from the cavity must be collected from the waveguide edge. This is accomplished by positioning the sample at a slight tilt, and focusing on the cavity edge with a 50x long focal length objective lens. The light collected from the objective is then directed to a 300 mm length spectrometer, and projected on a liquid nitrogen cooled InGaAs CCD camera. Using the InGaAs CCD, the

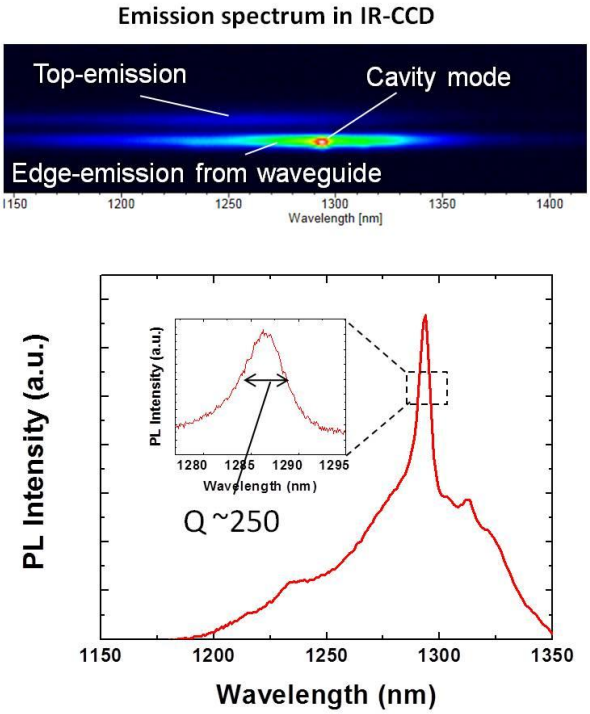

Figure 7. Experimental data from the NP photonic crystal cavities. Top image shows the emission spectrum captured by the CCD. Bottom image shows a detail of the spectrum and inset shows high resolution spectrum of the cavity mode.

objective can be precisely position to the cavity edge to resolve the emission coming from the cavity mode.

The experimental data from one of the NP photonic crystal cavities in the waveguide structure is shown in Fig. 7. The NPs in these samples are grown with an InGaAs axial segment emitting at ~1.3 μm. Because of the tilted angle at which the long focal length objective collects light from the sample, the emission from the top of the waveguide structure can be distinguished from the emission at the edge of the waveguide structure. As shown in Fig. 7, the emission from the top shows a typical spontaneous emission spectrum while the emission from the edge exhibits characteristics of the photonic crystal cavity. A detailed image of the spectrum from the edge shows additional peaks from the photonic band edges at 1230 nm and 1310 nm. In between the photonic band edges the cavity mode

can seen at 1286 nm and is significantly higher intensity as expected. A high resolution image of the cavity spectrum shows the mode has a full-with half-maximum (FWHM) of 5 nm. From the FWHM of 5 nm, the cavity Q is calculated to be ~ 250.

At present, the maximum cavity Q of ~ 250 is insufficient for lasing at room temperature with this experimental setup. Based on other reports, this could potentially produce lasing either at liquid nitrogen temperatures, or by using a high-power pulsed laser as a pump source. However, this cavity Q is two orders of magnitude lower than the simulated cavity Q for this design, indicating that a significant loss mechanism exists in the structure. FDTD simulations have shown that this is most likely due to absorption in the core polymer layer, since geometric imperfections cannot account for the two order of magnitude reduction in cavity Q. To address this issue, new polymers such as bisbencyclotene are being tested to replace the polyimide core layer that was used in these cavities.

7.4 FIBER-COUPLED NP PHOTODETECTORS

The development of waveguide coupled NP optoelectronic devices was done in parallel with the NP photonic crystal cavities described above. The goal of this work was to show the feasibility of coupling light from a single mode fiber to a NP device through a waveguide and vice versa. So far, the former of these has been accomplished.

The complete waveguide fabrication process described in section B was performed for the devices. This includes the final steps of depositing electrical contacts and etching the planar waveguide layer into discrete ridge waveguides. This is shown in Fig. 8. In these samples, each chip is designed to have ~150 devices, each with their own electrical contact and ridge waveguide. The waveguides connect the NP devices at the center of the chip to the cleaved

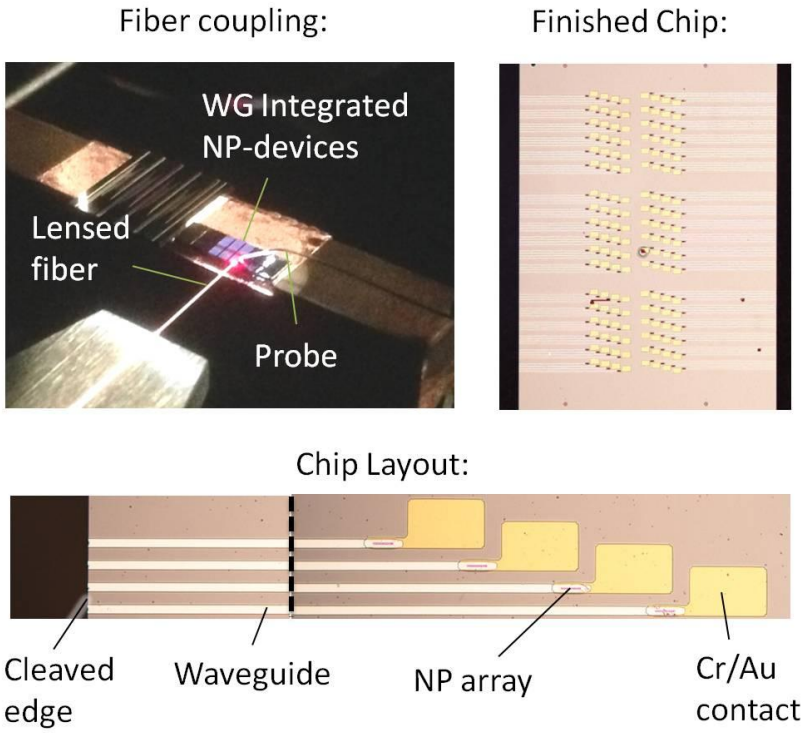

Figure 8. Experimental testing of NP optoelectronic devices coupled to passive optical waveguide. Upper left image shows experimental setup, where a lensed fiber is used to couple light into the waveguide at the chip edge, while the NP device is being electrically probed. Upper right shows a die photograph of the fabricated chip. Lower image shows a magnified view of the chip layout.

edge of the chip. A single mode optical fiber is coupled to a waveguide at the cleaved edge by a lensed fiber tip, where different light sources can be used for testing by coupling to the fiber at the opposite end. Under this configuration, each device can be tested for photoresponse and spectral response with different light sources.

The experimental data from the waveguide integrated NP photodetectors is shown in Fig. 9. In order to characterize the detector performance, two different types of light sources were used. The first was a 660 nm diode laser. The diode laser emission was lens coupled into the single mode fiber, which was then coupled into the polymer waveguide and measured by the NP detector. Under dark conditions, the NP detector exhibits an excellent diode characteristic, with a rectification ratio of $> 10^8$ and a dark current of only 100 pA at -20 V.

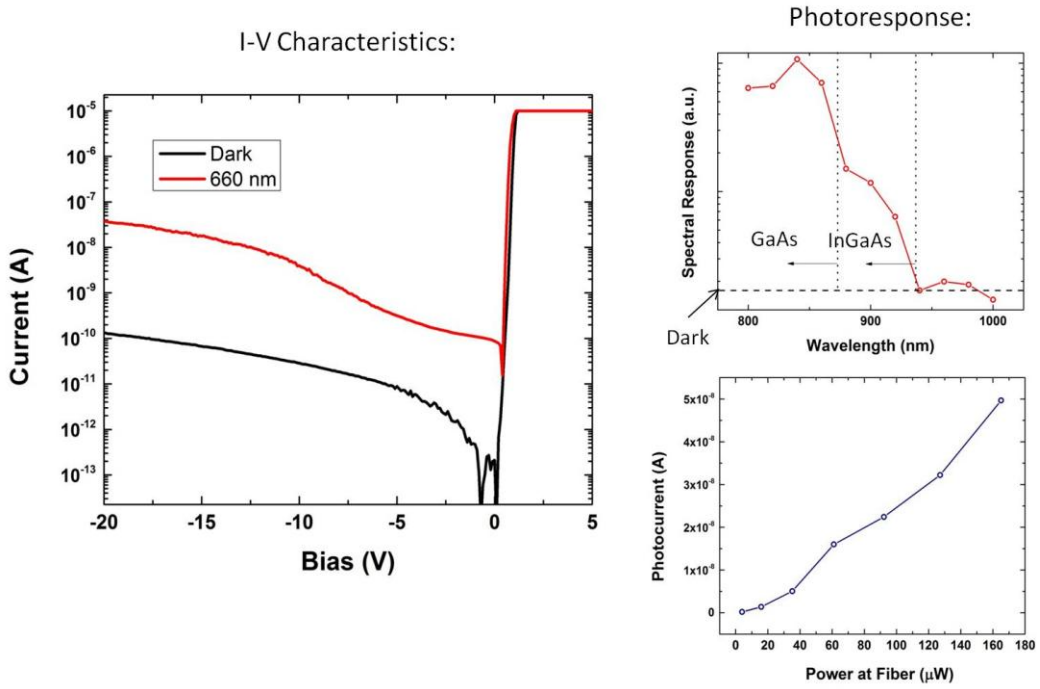

Figure 9. Characteristics of the waveguide coupled NP photodetector. Left image shows the light and dark I-V curves. Top right shows spectral response from the device with GaAs and InGaAs band edge absorption. Bottom right shows the photoresponse of the device under illumination at 925 nm.

Under excitation from the diode laser, the detector exhibits a photocurrent that is 10^2 greater than the dark current across a wide range of bias voltages.

The second type of light source used to characterize the devices was a supercontinuum laser with a tunable wavelength filter, so that the spectral response and power dependent photoresponse could be measured. For the spectral response, the NP detector was reverse-biased at -10 V while the output of the supercontinuum laser was swept from 800 nm to 1000 nm. The photocurrent was then normalized to the measured power output from the end of the lensed fiber tip. The spectral response clearly shows three distinct regions. The first region is the wavelength range between 800 nm and 875 nm, where the light is absorbed by both the GaAs and InGaAs components of the device. The second region is in the range of 875 nm to 950 nm, where the light can only be absorbed by the axial InGaAs segment in the

NPs. The third region is the cutoff beyond the InGaAs band-edge. The three distinct regions of the spectral responses clearly demonstrate that the InGaAs axial segments in the NPs are absorbing the laser light, and that the axial *p-i-n* diode is effectively extracting the photo-generated carriers and producing the photocurrent. This is verified by power dependent photoresponse which shows a linear dependence of photocurrent vs. input power to the waveguide.

7.5 CONCLUSIONS AND OUTLOOK

Successful development and testing of the fabrication of passive optical waveguides around NP array devices in a monolithic approach is achieved. The demonstration of waveguiding, coupling light to and from NPs, photonic crystal cavities, and waveguide integrated NP detectors were demonstrated. This result is the first known instance of coupling light from a single mode fiber to a nanowire optoelectronic device via waveguide. At present, there are numerous improvements that can be made to the next generation of devices. First, alternative polymer core layers are being explored to achieve low-loss transmission. This will serve both performance of waveguide integrated detectors and photonic crystal cavities. With sufficient improvement in cavity Q, the NP arrays should be capable of lasing at room temperature. Furthermore, the devices presented in this work have not yet fully employed all of the advanced heterostructures that were developed under the first year of the project, leaving room for significant improvement.

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Chapter 8

The work in this thesis has shown the development of Nanopillar-based emitting devices in the near-infrared, ranging from photonic crystal lasers to light-emitting diodes and waveguide integration. However, significant work remains to push the development of nanopillars to realize the original goal of demonstrating an electrically injected laser capable of fJ/bit energy levels as described in Chapter 1.

This design concept has been extended to address the problem of electrical injection, growth on SOI substrates, and waveguide coupling. The result of this is the beam-type photonic crystal cavity shown in Figure 1. Finite-difference time-domain simulations have been used to model the cavity Q, confinement factor Γ, and waveguide coupling efficiency. The details of the process of this design are similar to those employed in Chapter 7, and we can summarize the end result of

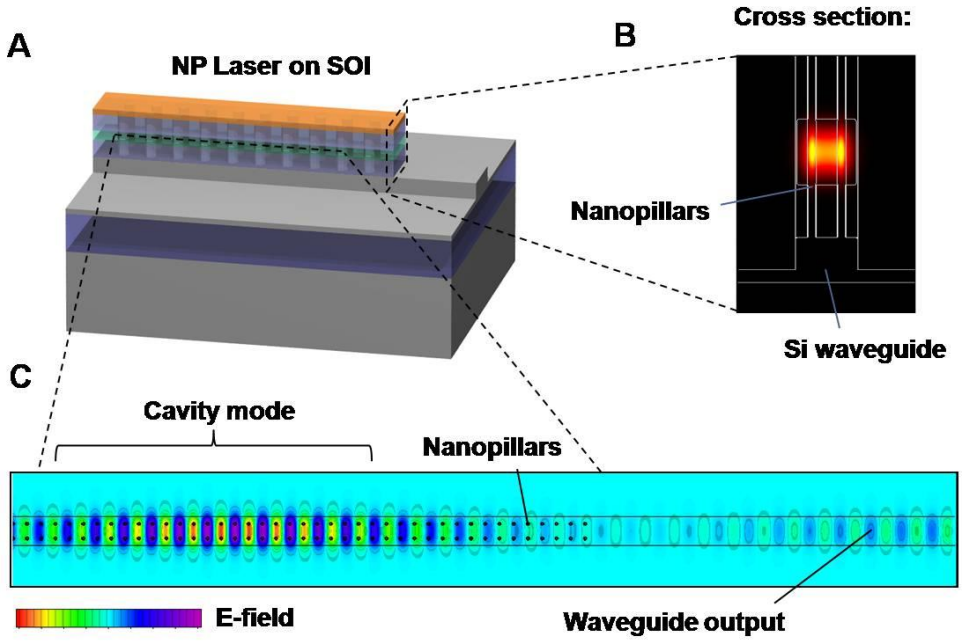


Figure 1. (a) Design of the NP photonic crystal laser coupled to a SOI waveguide. (b) Cross-section of the E-field intensity. (c) Top-view of E-field showing the cavity mode and waveguide coupling.

the similation as follows:

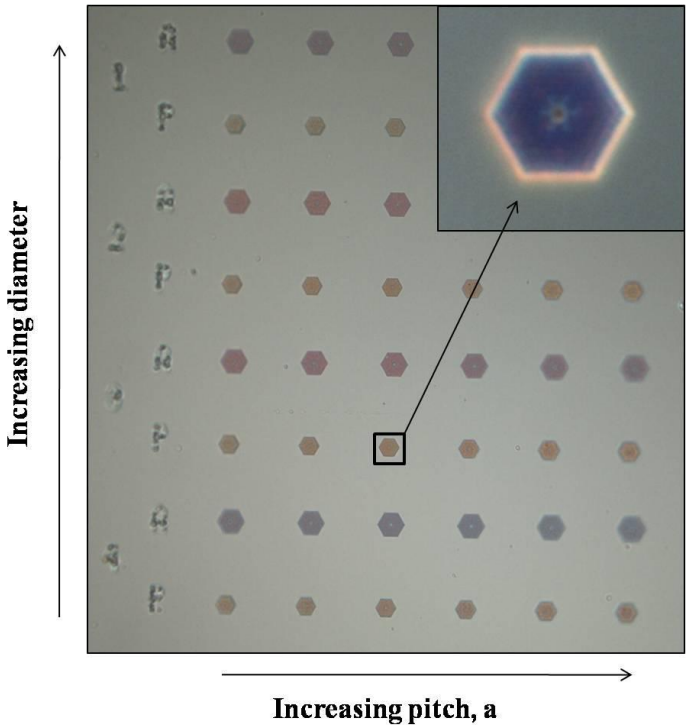
Cavity Q	Γ	η_{wg}	A_{act}
9,162	**0.213**	**0.9**	**2.2×10^{-8} cm^2**

Compared with the original analysis in Chapter 1, these values are enough to surpass even the 1°C temperature requirement given an appropriate heat sink, such as a thick electroplated contact.

Appendix A

Photonic-Crystal Cavity Arrays in PDMS:

The nanopillar photonic-crystal cavities are arranged in arrays with varying pitch and diameter in order to fine tune the resonant wavelength and *Q* factor. Each array contains 4 rows and 6 columns of devices. In each row, the radius is varied between $0.15 \cdot a$ and $0.2 \cdot a$ (where a is the inter-pillar pitch). In each column, the inter-pillar pitch is varied between 324 nm and 342 nm. This variation in pitch corresponds to resonant wavelengths between 950 nm and 1000 nm according to the normalized frequency calculated from FDTD simulations ($\lambda = a/\omega_n$, where $\omega_n = 0.342$). Fig. S2 shows a dark-field optical microscope image at 50× magnification of an array in PDMS with the inset showing a single device at 150× magnification. Additional rows for other experiments (labeled A) are visible but not reported on in this paper.



Appendix B

High Phosphorus Composition GaAsP Inserts:

Nanopillars with multiple GaAsP axial inserts in GaAs were imaged by both scanning transmission electron microscopy (STEM) and high-resolution transmission electron microscopy (HRTEM). Under HRTEM, samples with high concentrations of Phosphorus (greater than 20%) exhibit noticeable strain fields at the GaAs/GaAsP interfaces. The strain fields are ovular in shape, as shown in Figure S1, and are remarkably similar to the simulated strain in nanowire heterointerfaces in Reference 16. As predicted by other theoretical work, the strain is relaxed within 10 - 20 nm of the interface without the formation of dislocation defects. This indicates the possibility of the absence of a critical thickness (or infinite critical thickness) for GaAsP axial inserts within the range of 20% Phosphorus composition and nanopillar diameter less than 100 nm.

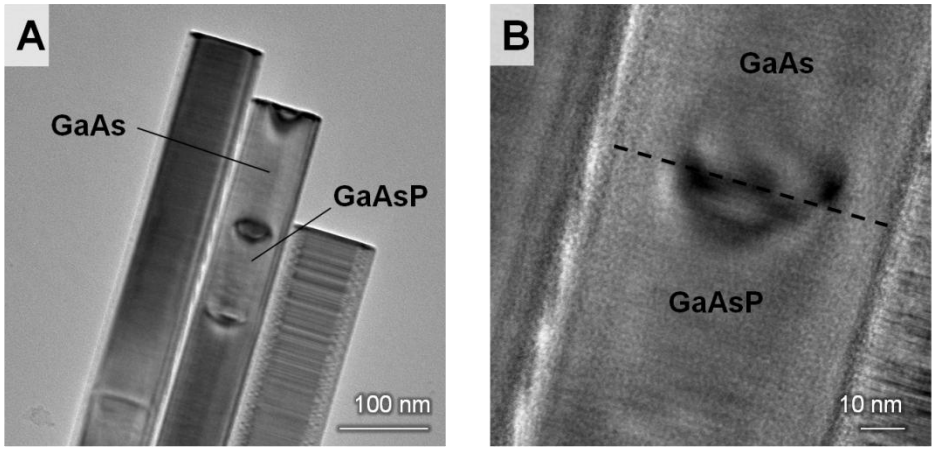


Figure S1. (A) HRTEM image of a GaAsP insert in a GaAs nanopillar, and (B) close-up view of the GaAs/GaAsP interface.

Uniformity Degradation at High Phosphorus Composition:

While characterization of single nanopillars by TEM showed axial GaAs/GaAsP inserts that were strain-relaxed, an important observation from the growth of these samples was a degradation of nanopillar uniformity with higher Phosphorus compositions. In order to explore this in a controlled manner, samples with single GaAsP inserts in GaAs nanopillars were grown. As shown in Figure S2, it can be seen from optical microscope images at 100× magnification, that beyond 10% Phosphorus in the solid phase (~30% in gas phase), the number of defective nanopillars increases with increasing Phosphorus composition. Therefore, in order to maintain high-uniformity in devices, the solid phase Phosphorus composition is limited to approximately 10%.

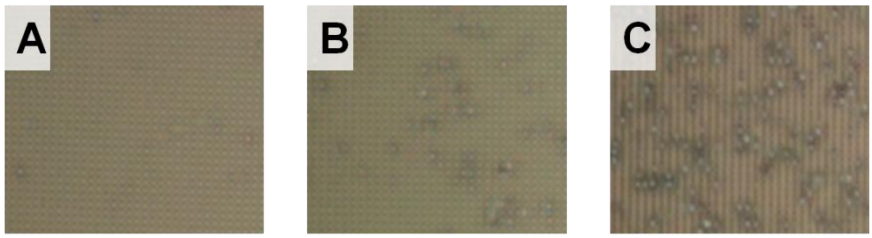


Figure S2. Optical microscope images of GaAs nanopillar arrays with single GaAsP inserts with (A) 10% P, (B) 13% P, and (C) 21% P.

Appendix C

Polymer Waveguide Process Steps:

1. **Growth mask removal:** The growth mask is removed using the Oxford RIE in order to prevent problems in measuring the CYTOP lower cladding thickness using the Nanospec. The CYTOP lower cladding layer also adheres to the substrate better than the growth mask. The following recipes and times can be used:

    a. SiO_2 mask: Oxide-slow, 70s.

    b. SiN_x mask: Nitride-slow, 70s.

2. **CYTOP lower cladding coat:** The lower cladding layer is CYTOP, using a double spin-coat process. This layer should be ~ 4µm in thickness in order to fully planarize the Nanopillars in and around the cavity regions. An HMDS prime of at least 5 mins is used to promote adhesion to the substrate. Between each coating, the solvent is baked at 70°C for 15-30 mins in order to prevent stretching and non-uniformity in film thickness prior to curing. The complete coating process is as follows:

    a. Dehydration bake, 180°C, 5 mins.

    b. HMDS prime, 5 mins.

    c. Spin-coat first layer, 800 rpm, 100 rpm/s, 180 s.

    d. First solvent bake, 70°C, 15 mins.

    e. Spin-coat second layer.

    f. Second solvent bake.

3. **CYTOP curing:** The CYTOP lower cladding is cured in the Carbolite Oven at 280°C for one hour. The samples are placed on top of Aluminum foil in a petri dish in order to prevent sticking to the glass surface. The ramp rates are not to exceed 1°C/min, in order to prevent delamination of the film. An excess flow of Nitrogen of 25 L/min is used to better remove solvent from the oven.

4. **Backside metal contact (n-GaAs):** The standard backside metal for n-GaAs substrates is a multilayer Ge/Ni/Ge/Au contact. The layer thicknesses and deposition rates for the materials are 50A/100A/150A/1.5kA and 0.4As/0.6As/0.8As/3As. The contact is then annealed in the RTP at 380C for 30s.

5. **CYTOP lower cladding etch:** The CYTOP is isotropically etched using the Oxford RIE with a custom recipe, AS-POLY-1. The typical etch rate is ~20A/s. Generally, the most accurate cladding thickness is obtained by dividing the etch into three or four parts, where 50% of the etch is done with the first part, 40% of the etch is done with the second parts, and the remaining 10% is done with the third and/or fourth parts. The recipe uses a low power of 50W in order to prevent increased etch rates due to heating in the polymer film. The AS-POLY-1 settings are as follows:

    a. Power: 50W

    b. Pressure: 150 mTorr

    c. CF_4: 20 sccm

    d. O_2: 100 sccm

6. **Polyimide core coating:** The Polyimide core layer uses the chemical PI-2611 from Dow Chemicals. The PI-2611 bottle is stored in the refrigerator and needs to be brought to ambient temperature before spin coating. The drop casting of the PI-2611 is done prior to spinning. The film needs ~5 mins to set so that the polymer infiltrates the nanopillars without leaving air bubbles. Then the spinning process is as follows:

    a. 500 rpm, 30s

    b. 1000 rpm, 30s

    c. 5000 rpm, 120s

    The film is then baked for solvent removal in the same conditions as the CYTOP film: 70C for 15 mins.

7. **Polyimide curing:** The Polyimide films are cured in the Carbolite oven at 220C for 1 hour. Higher temperatures may be used to better drive off the solvent and promote cross-linking, but increased temperatures have a risk of film shrinkage, potentially causing large bubbles to form between the Polyimide and CYTOP layers.

8. **Polyimide edge-bead removal:** The edge-bead of the Polyimide and CYTOP films is removed by hand with a razor blade. Due to the edge-bead thickness, use of a photomask layer to remove the edge-bead is generally impractical. The edge-bead removal is primarily necessary in order to use the Dektak to measure the film thickness during the etching process.

9. **Polyimide core etch:** The Polyimide core etch follows the same process and conditions as the lower cladding etch.

10. **CYTOP top cladding:** The CYTOP top cladding layer uses the same spin-on process as the lower cladding. However, only a single coating is necessary for the top cladding as only a small fraction of the nanopillar are exposed at this point. The CYTOP is then cured at only 200C in order to prevent any changes to the Polyimide core layer during the top cladding

11. **Contact metal lift-off:** The contact metal used for p-GaAs is Cr/Au (5 nm/200 nm). The lift-off is performed using the standard image reversal process with AZ5214.

12. **Waveguide photoresist process:** The waveguide patterning can be performed in one of two ways: (1) AZ5214 is double coated onto the sample to produce a 2x thick resist layer and a non-reversal process is used, or (2) the standard AZ5214 image reversal process is used and Al lift-off is performed. In many cases, the Al lift-off yields better results, since the Al hard mask has effectively infinite etch selectivity, and issues with patterning a thicker photoresist are avoided.

13. **Waveguide etch:** The waveguides can be etched using the same recipe as the core and cladding layer etch-back steps.