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A 48-to-12 V Cascaded Resonant Switched-Capacitor Converter Achieving 4068 W/in^3 Power Density and 99.0% Peak Efficiency

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***Abstract*—A 4-to-1 cascaded resonant switched-capacitor (ReSC) converter, comprising two cascaded 2-to-1 ReSC converters, has been demonstrated to have high efficiency and high power density in previous literature. This work explores the approaches to further improve the performance of the cascaded ReSC converter, including merging two phases of the first stage into one phase and reducing the intermediate decoupling capacitor. The impact of the intermediate capacitor on the interaction between two stages is studied. With the optimization of circuit structure, active and passive component selection, layout, etc., this converter achieves a power density of 4068 W/in^3 under 48 V input and 60 A output. The converter also has high efficiency for the entire load range, achieving 99.0% peak efficiency and 97.9% full-load efficiency with gate drive loss included. Both power density and efficiency are superior to the state-of-the-art.**

***Keywords*—hybrid converter, switched capacitor, cascaded resonant converter**

I. Introduction

As the demand of internet and computing resources is growing fast in recent years, the power consumption of servers and data centers keeps increasing [1]. To address the issue of high distribution loss on the bus bar of server racks, the 48 V bus architecture has been proposed and will be widely used for the next-generation data centers [2]. One important research topic regarding this architecture is stepping down from 48 V to the Point-of-Load (PoL) voltage, which is usually implemented by an intermediate bus converter followed by a voltage regulator (VR), with the benefits of high efficiency and reutilization of the 12 V legacy system.

Many topologies have been explored for the 48-to-12 V intermediate bus applications. The inductor-based converters, like the buck converter, have limited power density since the inductors dominate the size of the overall solution [3]. The efficiency would be sacrificed if the switching frequency is pushed too high to shrink the inductor size. The LLC converter is another mature magnetic-based topology and has good performance in both efficiency and power density, but has the drawbacks of complicated transformer design, limited scalability, and high cost [4].

Since capacitors have higher energy densities compared with inductors, switched-capacitor (SC) based converters have the potential to achieve higher power density and have gained more and more attention in performance-driven applications [5]–[8]. The 2-to-1 SC converter reported in [9] achieves 2000 W/in^3 power density and 99% efficiency for 48-to-24 V power conversion. Multiple 2-to-1 SC converters can be cascaded to realize higher-ratio conversion [10]. The cascaded SC converter reported in [11] has outstanding performance through the introduction of resonant inductors, and is thus called cascaded resonant switched-capacitor converter. The flying capacitors are soft charged so the capacitor charge redistribution loss is eliminated [12]–[14]. The resonance between flying capacitors and inductors enables soft switching for all MOSFETs, so the switching loss can be reduced. Both the soft charging and soft switching are beneficial for efficiency. Another advantage of the cascaded resonant converter is the effective utilization of passive components, which leads to a high power density.

Two phases of the cascaded resonant converter can be paralleled to offer higher current, and the second stages are interleaved to reduce the mid-point capacitance, as illustrated in Fig. 1(a). Based on this structure, key topology and design modifications are performed in this work to improve efficiency and power density. The first stage is merged into one phase to reduce the amount of active components, which has considerable practical advantages in terms of reduction in PCB layout area, and number of level shifters and gate drivers. The magnetic volume is also reduced since the merged first stage uses only one ferrite gapped inductor. Compared to two-phase inductors, the single-phase inductor can be designed with the same energy, while using a smaller core size. A key contribution of this work is also a design approach to significantly reduce the size of the intermediate capacitor, C_{mid}. Instead of using sufficiently large C_{mid} to completely decouple the first stage and second stage, a small C_{mid} is carefully chosen in this work to reduce the passive volume while maintaining circuit performance through investigations of the resulting multi-resonant circuit topology. By using the technologies of reducing active and passive components mentioned above, the new converter achieves extremely high power density (4068 W/in^3) and efficiency (99.0% peak efficiency and 97.9% heavy-load efficiency with drive loss included).

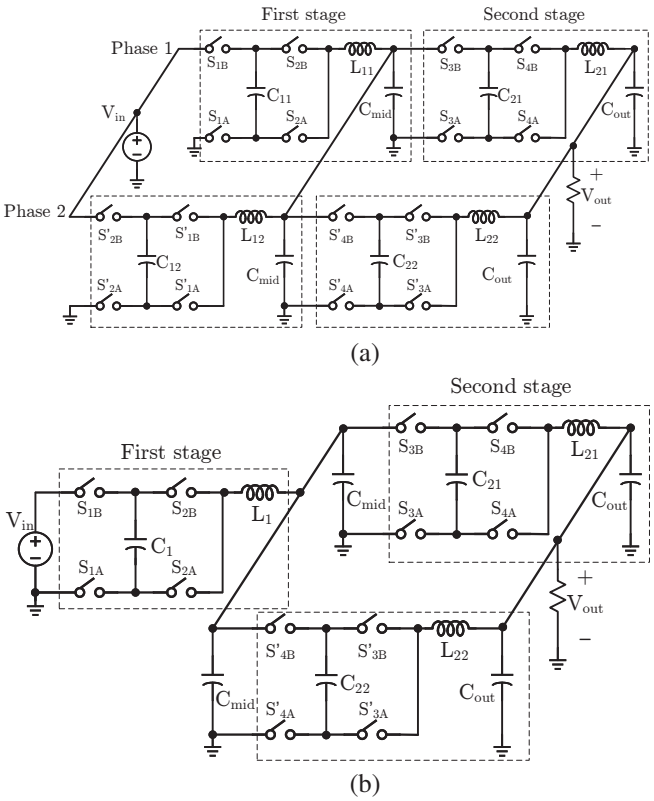


Fig. 1: (a) Two-phase cascaded resonant converter introduced in [11]. (b) The first stage is merged into one phase.

II. Operation Principle

A. Analysis of Cascaded Resonance

The operation principle of the proposed cascaded resonant converter is similar to that of the conventional resonant 2-to-1 SC converter. In order to achieve ultra-efficient and fixed-ratio power conversion, all MOSFETs in this converter operate with the same switching frequency and 50% duty cycle. In one half cycle of the period, the LC tank of the first stage is in series with the resonant tank of C_{21} and L_{21}, as shown in Fig. 2(a). Notice that the current through L_1 matches that through L_{21}, so little current goes through C_{mid}. In the other half cycle of the period, the operation modes of the second-stage resonant tanks are swapped. The branch of C_{22} and L_{22} is in series with C_1 and L_1, and the other branch, C_{21} and L_{21}, is charging V_{out}. The operation principle analyzed above indicates that the first stage is synchronized with the interleaved second stages.

The PWM signal of switch S_{1A} in Fig. 1(b) and the currents of resonant components in the scenario of sufficiently large C_{mid} are shown in Fig. 2(b). The two stages have the same resonant frequency, and all MOSFETs realize zero current switching (ZCS) when the switching frequency equals the resonant frequency. The capacitor C_{mid} is sufficiently large and will not participate in the resonance of other passive components. Thus, zero current goes through C_{mid}, and the inductor current i_{L1} matches the capacitor currents i_{C21} and $-i_{C22}$.

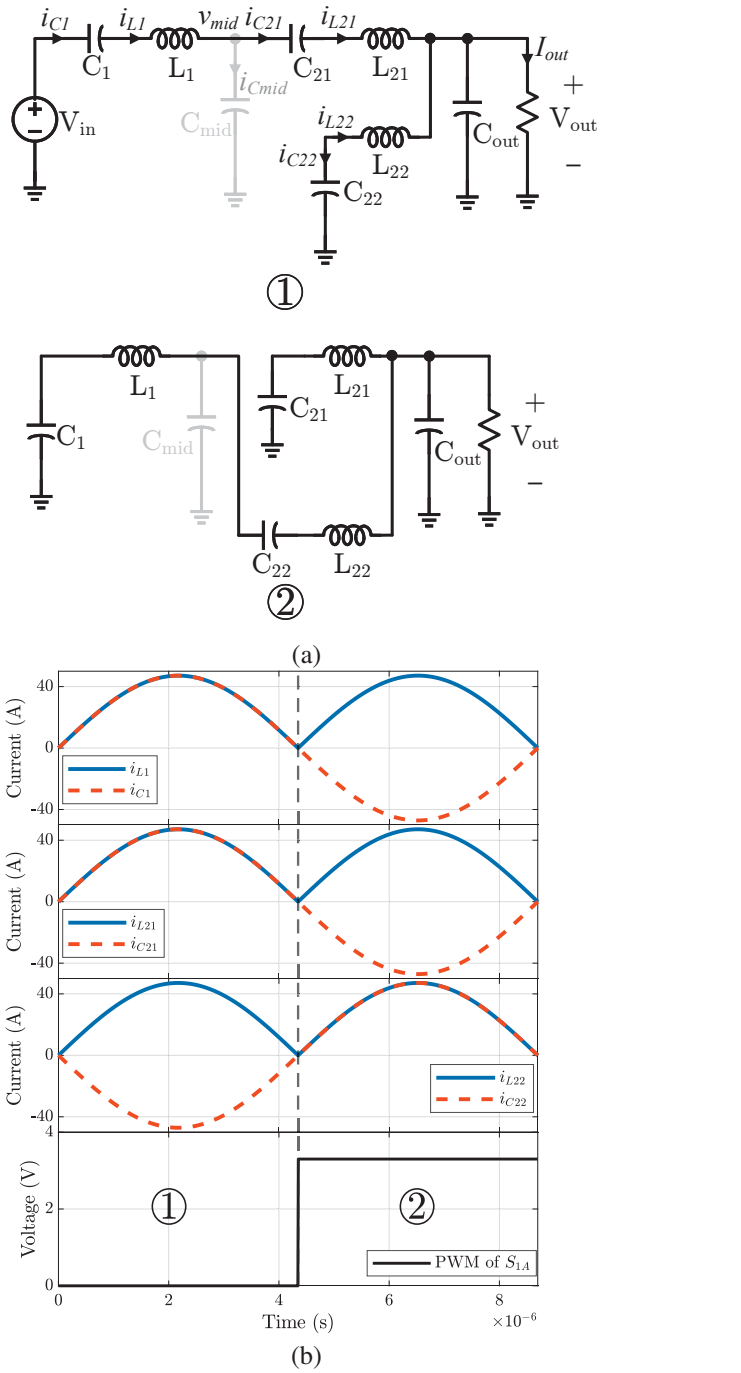


Fig. 2: (a) Equivalent circuits and (b) inductor/capacitor currents of the converter in Fig. 1(b) with sufficiently large C_{mid}.

B. ZVS Implementation

In practical implementations, the switching frequency can be chosen to be slightly higher than the resonance to guarantee complete soft-switching and low conduction loss, which has been discussed in [15]. One advantage of this converter is that the switching frequency is not required to be strictly matched with the resonant frequency, and the passive components are allowed to have a relatively large tolerance, e.g., ±20%. Another desirable feature is that zero voltage switching (ZVS) is

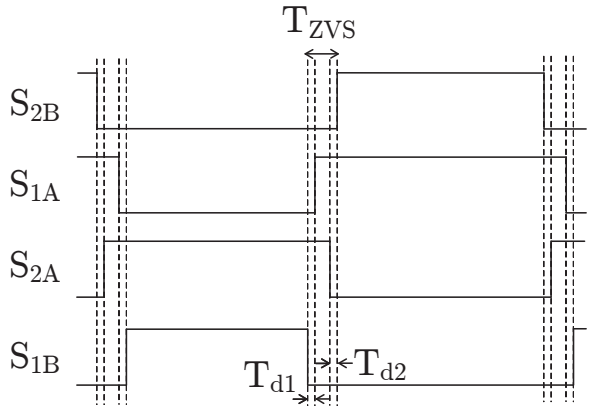


Fig. 3: PWM driving scheme of ZVS mode for a general 2-to-1 hybrid converter exemplified by the first stage of cascaded resonant converter in Fig. 1(b). The PWM signals of low-side switches S_{1A} and S_{2A} are overlapped for reducing the body diode conduction.

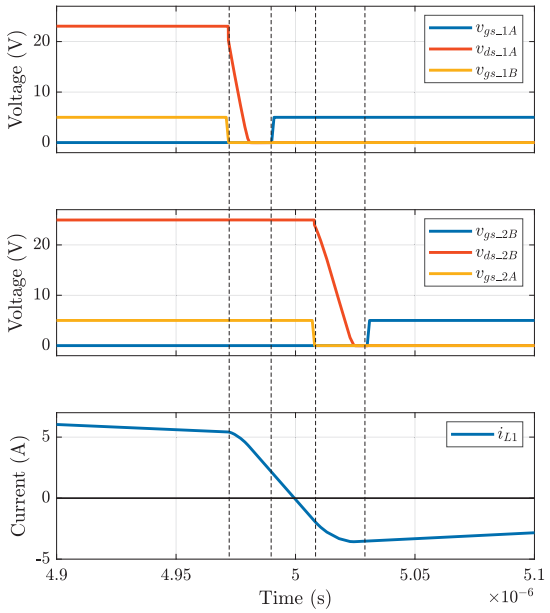


Fig. 4: Simulated gate signals, drain-to-source voltages, and inductor current to demonstrate ZVS turn on of S_{1A} and S_{2B} by using the PWM scheme in Fig. 3.

available for all MOSFETs. Compared with the PWM scheme in [15], an additional degree of freedom is added in this work to minimize the body diode conduction. As seen from the proposed PWM scheme in Fig. 3, the deadtimes of low-side PWM and high-side PWM are controlled independently. The deadtime T_{ZVS} is used to control the demagnetization time of the resonant inductor so that the negative inductor current is of sufficient magnitude for S_{2B} to achieve ZVS, as illustrated in Fig. 4. The deadtimes T_{d1} and T_{d2} are reserved to discharge the C_{oss} capacitances of S_{1A} and S_{2B}, respectively. For the cascaded resonant converter operating at 48 V input and 100 – 200 kHz switching frequency, the deadtimes T_{d1} and T_{d2} usually range from 15 ns to 30 ns, and the T_{ZVS} ranges from 40 ns to 100 ns. This ZVS method is also applicable to other ReSC topologies such as the resonant Dickson converter.

C. Design of Intermediate Capacitor

For the conventional single-phase cascaded resonant converter, a sufficiently large intermediate capacitor C_{mid} is needed to decouple the first stage and second stage. For example, a large C_{mid} (19 × 1206 ceramic capacitors) has been used in [11] and takes ∼20% of the total footprint on the back side of the board. Consequently, reducing the C_{mid} size is an effective way to improve power density. One advantage of the interleaving structure of the second stage is the cancelled current ripple at the V_{mid} node, which allows a small C_{mid} to be used. It should be noted that only the second stages need to be interleaved; the first stage is not required to be interleaved to have this cancelling effect.

The selection of C_{mid} depends on the allowed voltage ripple on the intermediate node V_{mid}, the allowed mismatched current of the two stages, and the parameters of the main resonant tanks. Although the interleaving cancelling effect on the intermediate node greatly reduces the current ripple of i_{Cmid}, the capacitor C_{mid} cannot be omitted since two stages always have a certain mismatch in reality, and their mismatched current needs to flow through C_{mid}. It is also necessary to have a certain C_{mid} as the decoupling capacitor for the second-stage MOSFETs S_{3B}, S_{3A}, S'_{4B}, and S'_{4A} shown in Fig. 1(b). The decoupling capacitor needs to have a low impedance to reduce the voltage overshoot and high-frequency switching noise. Even though the resonant frequencies are perfectly matched for two stages ($f_r = \frac{1}{2\pi\sqrt{L_1C_1}} = \frac{1}{2\pi\sqrt{L_2C_2}}$, where $L_2 = L_{21} = L_{22}$ and $C_2 = C_{21} = C_{22}$), the resonance of C_{mid} and other passive components such as C_1, L_1, C_{21}, and L_{21}, may cause high current through C_{mid}, as shown in Fig. 5(a), which plots the RMS current and peak-to-peak voltage of C_{mid}, as a function of capacitor size. The corresponding current waveforms of i_{L1}, i_{L21}, and i_{Cmid} at the designed point and the resonant point are shown in Fig. 5(b) and (c), respectively. As seen from the waveforms, a capacitor value of C_{mid_crit} results in large undesirable circulating resonant currents in the LC tanks, so operating at this point should be avoided.

To better understand the multi-resonance mechanism, the equivalent circuit of Fig. 2(a) is redrawn in Fig. 6 by considering only the ac component. By analyzing this circuit, the resonant frequency including C_{mid} can be found to be

$$f_{mid} = \frac{1}{2\pi\sqrt{\frac{L_1L_2}{L_1+L_2}\frac{C_{mid}(C_1+C_2)}{C_{mid}+C_1+C_2}}} \tag{1}$$

Since the resonant tanks C_1L_1 and $C_{21}L_{21}$ have the same resonant frequency f_r, the resonance when paralleling them is also f_r, which leads to

$$f_r = \frac{1}{2\pi\sqrt{\frac{L_1L_2}{L_1+L_2}(C_1+C_2)}} \tag{2}$$

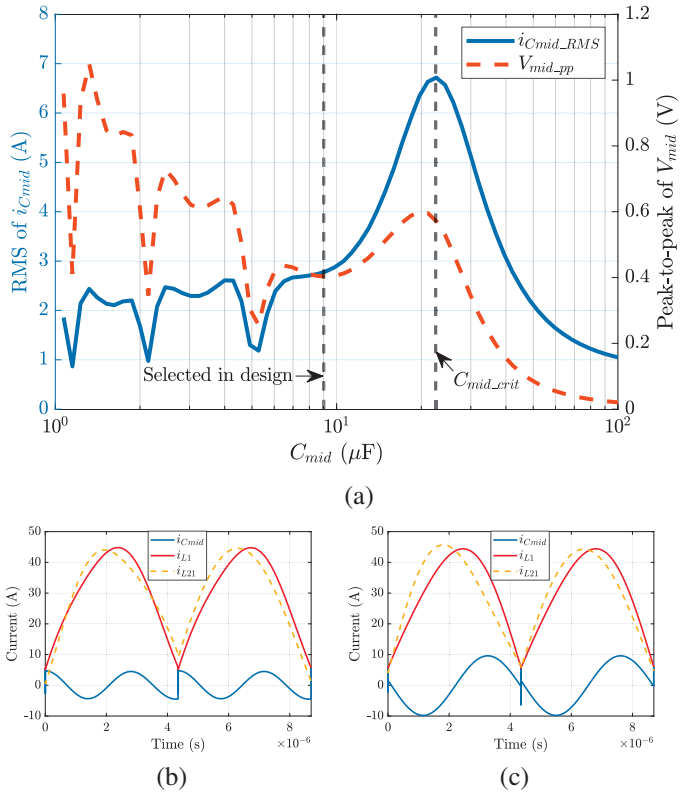


Fig. 5: (a) Simulated RMS current of C_{mid} and the peak-to-peak voltage of V_{mid}. Simulated inductor currents and i_{Cmid} at (b) the selected capacitance in this design and (c) resonant point C_{mid_crit}, demonstrating large resonant current through C_{mid} at the undesirable operating point.

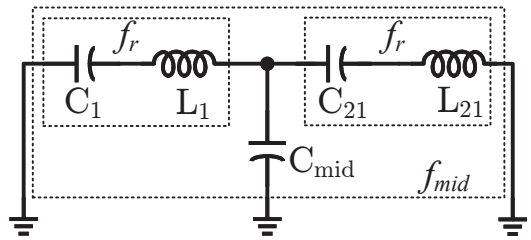


Fig. 6: Equivalent circuit of phase 1 in Fig. 2(a) considering only ac path.

By comparing (1) and (2), the ratio $\frac{f_{mid}}{f_r}$ is calculated by

$$\frac{f_{mid}}{f_r} = \sqrt{1 + \frac{C_1 + C_2}{C_{mid}}} \tag{3}$$

The resonant point C_{mid_crit} in Fig. 5(a) corresponds to $\frac{f_{mid}}{f_{sw}} = 2$. To avoid high voltage and current ripples of C_{mid}, the ratio $\frac{f_{mid}}{f_{sw}}$ is recommended to be designed in the range of $2.5 < \frac{f_{mid}}{f_{sw}} < 4$. The corresponding C_{mid} range is then solved from

$$6.25(\frac{f_{sw}}{f_r})^2 - 1 < \frac{C_1 + C_2}{C_{mid}} < 16(\frac{f_{sw}}{f_r})^2 - 1 \tag{4}$$

As the switching frequency is slightly higher than f_r for ZVS, for example $f_{sw} = 1.1\ f_r$, the C_{mid} range in (4) is approximated by $0.06(C_1 + C_2) < C_{mid} < 0.15(C_1 + C_2)$. In this design, $C_{mid} = 9\ \mu\text{F} = 0.1(C_1 + C_2)$ is selected to achieve small capacitor volume (6×0805 ceramic capacitors), low voltage ripple on V_{mid} (< 500 mV), and low RMS current through C_{mid} (< 3 A), while also being relatively insensitive to component variations.

III. Hardware Implementation and Experimental Results

A prototype is fabricated to verify the performance of the proposed resonant converter. The first-stage switches are implemented by the Infineon 40 V MOSFET, IQE013N04LM6ATMA. The second-stage switches are implemented by the Infineon 25 V MOSFET, IQE006NE2LM5CG. The flying capacitors and resonant inductors are selected carefully to meet the requirement of resonant frequency (105 kHz in this design). The intermediate capacitor C_{mid} is selected based on Fig. 5(a). The resonant inductors are implemented by Coilcraft SLC7530S-500ML for both stages. In order to reduce the trace resistance, 6-layer PCB with heavy copper (4 oz. for outer layers and 2 oz. for inner layers) is used in the design. The detailed component parameters are listed in Table I. Compared with the cascaded resonant converter in [11], this work uses lower-$R_{ds(on)}$ MOSFETs and a lower-DCR inductor for improving heavy-load efficiency.

An annotated photograph of the hardware prototype is shown in Fig. 7. The MOSFETs, resonant inductors, and partial flying capacitors are tightly placed inside a rectangular box on the top side. The remaining flying capacitors and gate drive circuitry are placed directly underneath on the back side of the board. High-side gate drivers with internal level-shifter are used to drive the floating switches. The gate drive power is provided by a cascaded bootstrap method introduced in [16], [17].

The prototype has been tested up to 60 A output current. The corresponding power density is 4068 W/in^3 at 48 V input. The efficiencies with 40 – 60 V input were measured with Yokogawa WT3000 precision power meters. Very high efficiency has been achieved across the entire load range, as shown in Fig. 8. The peak efficiency is 99.0%, and full-load efficiency is 97.92% at 48 V input, with drive loss included. Considering only the power-stage efficiency with drive loss excluded, the peak efficiency is 99.2%, and full-load efficiency is 97.97%. For high input voltages such as 54 V and 60 V, the switching frequency is slightly increased to optimize the efficiency. Notice that the resonant current in Fig. 2(b) mainly depends on the load current and is almost independent of the input voltage, which indicates that conduction loss is independent of V_{in}. At heavy load, higher V_{in} has higher input power but similar loss, and thus shows higher efficiency.

High-efficiency operation greatly reduces the complexity of thermal design. As shown in Fig. 9, the maximum temperature is 68^{o}C at full load with fan cooling only. So far, the maximum output current of this converter is limited by the inductor

TABLE I: Main component listing of the cascaded resonant converter

Component	Manufacture and Part number	Parameters
1st stage MOSFET	Infineon, IQE013N04LM6ATMA	40 V, 1.1 mΩ
1st stage flying capacitor C_1	TDK, C3216X5R1H106K160AB TDK, C2012X5R1V226M125AC	10 × 10 μF*±20%, 50 V, X5R, 1206 12 × 22 μF*±20%, 35 V, X5R, 0805
Intermediate capacitor C_{mid}	TDK, C2012X5R1V226M125AC	6 × 22 μF*±20%, 35 V, X5R, 0805
2nd stage MOSFET	Infineon, IQE006NE2LM5CG	25 V, 0.65 mΩ
2nd stage flying capacitor C_{21}	Murata, GRM21BR61E226ME44L	12 × 22 μF*±20%, 25 V, X5R, 0805
Resonant inductors L_1, L_{21}, and L_{22}	Coilcraft, SLC7530S-500ML	50 nH, 50 A I_{sat}
Gate driver	Analog Devices, LTC4440-5	80 V, high-side
Bootstrap diode	Infineon, BAT6402VH6327XTSA1	40 V, Schottky

* The capacitance listed here is the nominal value before dc derating.

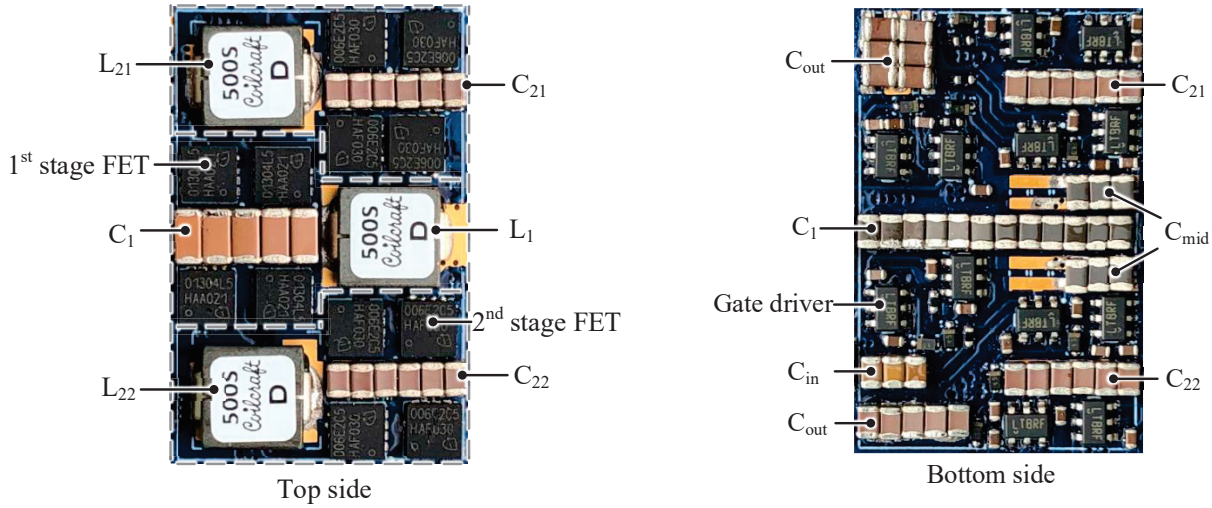


Fig. 7: Annotated photograph of the converter with the dimensions of 0.68 × 1.06 × 0.24 in (17.3 × 27 × 6.2 mm).

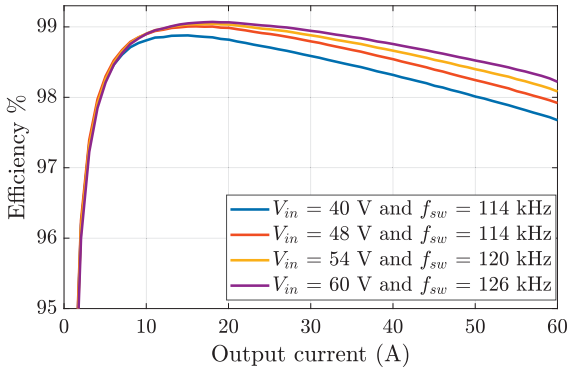


Fig. 8: Measured efficiencies at 40 – 60 V input including gate drive loss.

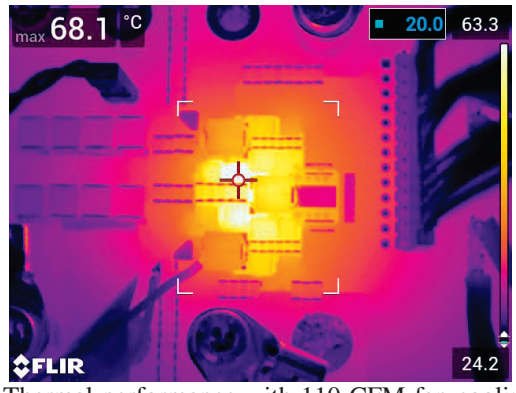
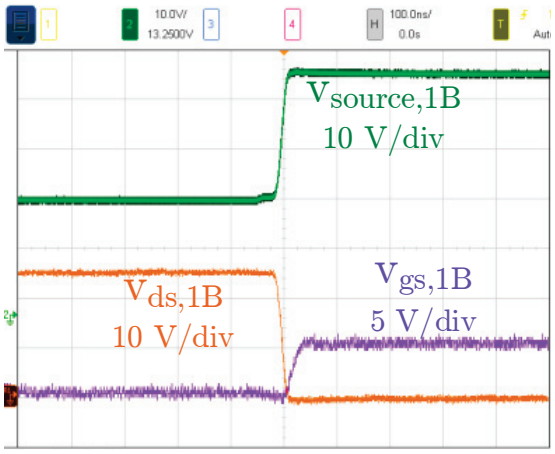


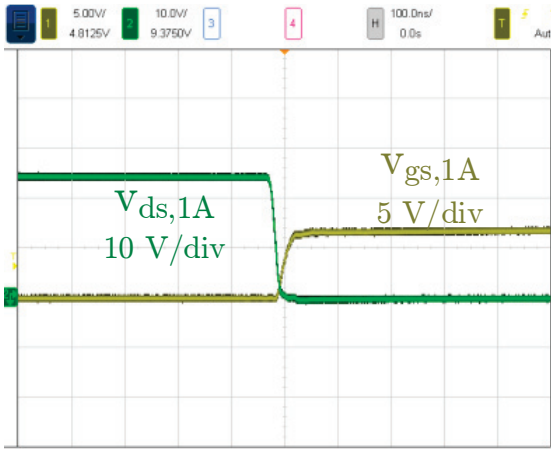
Fig. 9: Thermal performance with 110 CFM fan cooling only (V_{in} = 48 V, I_{out} = 60 A).

saturation current. Based on present thermal measurement result, the MOSFETs and capacitors have sufficient margin to handle higher current stress, and the inductors with higher saturation current can be used in the future to improve the power level.

By applying the PWM driving scheme in Fig. 3, this converter achieves ZVS for all MOSFETs, as demonstrated in Fig. 10, which shows the gate signals and drain-to-source



(a)



(b)

Fig. 10: Measured drain-to-source and gate voltages to demonstrate ZVS turn-on of (a) S_{1B} and (b) S_{1A} in Fig. 1(b) at V_{in} = 48 V and I_{out} = 20 A.

voltages of S_{1B} and S_{1A}. Both switches are turned on after the drain-to-source voltages drop to zero. Also, the voltage waveforms are clean and have no significant switching noise thanks to ZVS operation. Notice that fixed deadtime is used in this work, and the deadtime may not be enough to realize ZVS at heavy load. Nonetheless, it is unnecessary to realize ZVS in full-range load since the conduction loss is dominant at heavy load, and ZVS operation may cause higher RMS current.

This converter also has a tight load regulation, as illustrated by Fig. 11. The output voltage drops only 250 mV (2% V_{out}) at full load, corresponding to an equivalent output resistance of 4.1 mΩ. The transient response is also tested when load current steps from 10 A to 30 A. As seen from Fig. 12, the output voltage reaches steady state within ∼6 switching cycles and does not show significant undershoot.

The efficiency and power density of this work and the state-of-the-art 48-to-12 V intermediate bus converters are listed in Table II. Compared with the conventional cascaded resonant converter, this converter achieves 60% higher power density while having the best efficiency performance. Also,

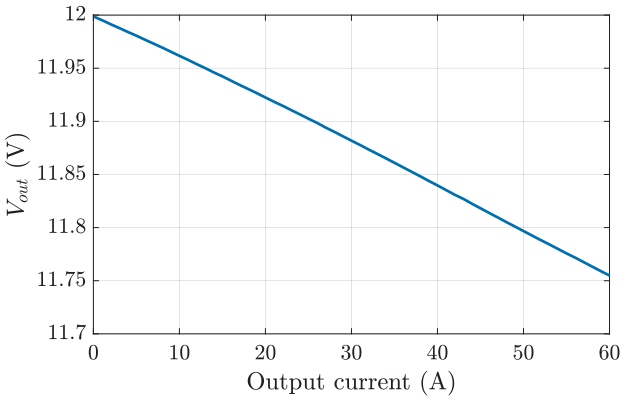


Fig. 11: Measured load regulation at V_{in} = 48 V.

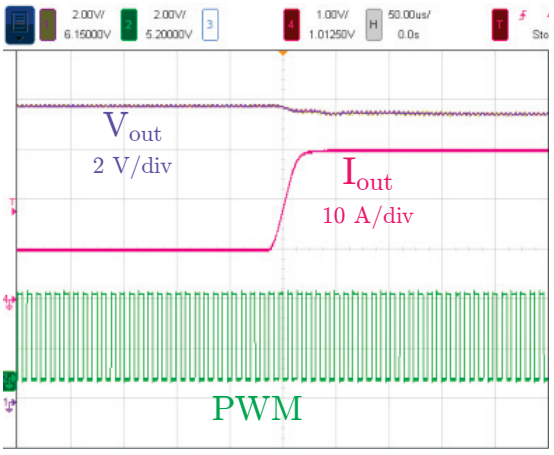


Fig. 12: Measured transient response of 10-to-30 A load step at V_{in} = 48 V.

both the power density and efficiency are higher than the highly integrated and highly optimized Vicor design. As the best ReSC demonstration to date, this converter can be fabricated using inexpensive and common components, e.g., Silicon MOSFETs, off-the-shelf inductors, and 6-layer PCBs. Furthermore, this converter does not reach thermal limitation at its full power and therefore still has the potential to increase power density by optimizing the inductors.

IV. Conclusions

A cascaded resonant converter with a merged first stage is proposed in this work. The PCB layout area and gate driver circuits are reduced significantly. Most of the current ripples are cancelled in the intermediate capacitor C_{mid} because of interleaving operation of the second stage. The multi-resonant mechanism of C_{mid} and other LC tanks is analyzed, and a general guideline to select the capacitance of C_{mid} is provided. A hardware prototype is built and tested with input voltage ranging from 40 – 60 V and output current up to 60 A. Both steady-state and transient performances are verified experimentally. The 4068 W/in^3 power density, 99.0% peak efficiency, and 97.9% full-load efficiency at the nominal

TABLE II: Comparison of this work with state-of-the-art 48-to-12 V intermediate bus converters

Reference	Topology	Max. I_{out} at 12 V output	Power density at 12 V output	Efficiency	Conversion ratio
This work	12-switch cascaded resonant	60 A	4068 W/in^3	Full load: 97.92% Peak: 99.0%	48-to-12 V
				Full load: 98.08% Peak: 99.0%	54-to-13.5 V
Cascaded resonant [11]	16-switch cascaded resonant	60 A	2500 W/in^3	Full load: 97.23% Peak: 99.0%	48-to-12 V
Vicor NBM2317 [18]	Sine amplitude converter (SAC)	60 A	4022 W/in^3	Full load: 97.3% Peak: 98.0%	54-to-13.5 V
Zero-inductor voltage (ZIV) [19]	2-phase hybrid SC	70 A	2500 W/in^3	Full load: 97.2% Peak: 99.1%	48-to-12 V
Google STC [20]	4-to-1 resonant Dickson	50 A	1040 W/in^3 (estimate)	Full load: 97.41% Peak: 98.61%	54-to-13.5 V
LLC with matrix transformer [4]	LLC	75 A	1600 W/in^3	Full load: 98.0% Peak: 98.4%	54-to-13.5 V

voltage 48 V reflect a dramatic improvement over the state-of-the-art converters from industry and academia.

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