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Democratizing Digital Microfluidics by a Cloud-based Design and Manufacturing Platform

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Resembling the impact of digital microelectronics on electronic devices for information technology, digital microfluidics (DMF) was anticipated to transform fluidic devices for lab-on-a-chip (LoC) applications. However, despite a wealth of research and publications, electrowetting-on-dielectric (EWOD) DMF has not seen the anticipated wide adoption, and commercialization has been painfully slow. Identifying technological and resource hurdles of developing own DMF chip and control system as the culprit, we envision to democratize DMF by building a standardized design and manufacturing platform. Toward this vision, we introduce a proof-of-concept cloud platform that empowers any users to design, obtain, and operate DMF chips (https://edroplets.org). For chip design, we establish a web-based EWOD chip design platform with layout rules and automated wire routing. For chip manufacturing, we build a web-based EWOD chip manufacturing platform and fabricate four types of EWOD chips (i.e., glass, paper, PCB, and TFT) to exercise the foundry service workflow. For chip control, we introduce a compact EWOD control system along with a web-based operating software. Although industrial fabrication services are beyond the current scope, we hope this Perspective will inspire academic and commercial stakeholders to join the initiative toward a DMF ecosystem for the masses.

1. Introduction

Digital microfluidics (DMF)[1-3] emerged as a revolutionary advancement in microfluidics, enabling independent control over individual droplets with electric signals alone.[3-5] Distinct from continuous flow (i.e., analog) microfluidics[6-8] and flow-carried droplet microfluidics[9-11], DMF manipulates discrete droplets with an array of planar electrodes, where four basic droplet operations (i.e., creating, transporting, merging, and cutting) can be performed.[12] Resembling a digital integrated circuit (IC) chip with numerous transistors processing digits for logic functions, a DMF chip with numerous electrodes can manipulate droplets for fluidic functions. As processing electric signals in bits made digital microelectronics compact and highly reconfigurable, handling liquids in droplets makes DMF systems uniquely simple and reconfigurable (i.e., no hardwired fluid pathways). This distinctive feature positions DMF as a platform technology capable of programming complex fluidic protocols on a given chip[13-16], paving the way for standardized design and manufacturing of lab-on-a-chip (LoC) devices and systems. Despite the name, most microfluidics chips are the size of a small plate (i.e., in centimeters) rather than a chip (i.e., in millimeters), which originated from IC chip.

Enabling electric control over various types of liquid on a hydrophobic surface, electrowetting-on-dielectric (EWOD)[17-20] has started the concept of DMF and become the most popular driving mechanism for DMF.[5,21-23] Like digital IC which revolutionized electronics and ushered in the era of information technology (IT), DMF holds a potential to transform fluidics (i.e.,

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liquid handling) and empower LoC. However, despite a wealth of research and publications on EWOD DMF, its commercialization has been painfully slow.[24] A few companies started exploring library preparation for DNA sequencing – a typical DMF application today – since the mid-2000s. For example, NuGEN Technologies (acquired by Tecan) worked with Advanced Liquid Logic (acquired by Illumina) to develop a DMF system called Mondrian SP Workstation[25], which was on the market only briefly around 2010. Next, Illumina launched NeoPrep in 2015 but also discontinued it soon for undisclosed reasons.[26] In 2016, Miroculus (acquired by Integra) started developing a DMF based system for library preparation called Miro Canvas after acquiring Kapplex[27], and launched their product in 2022.[28] In 2018, Volta Lab was formed to utilize DMF with open-configuration for sequencing library preparation, and released their product in 2024.[29] Additionally, MGI (a subsidiary of BGI) launched their library preparation product (DNBeLab Series D) in China in 2022.[30] Typically, it took over five years for a company to develop an EWOD-based DMF product.

Difficulties in optimizing a variety of chip parameters and overcoming reliability issues of EWOD DMF chips are generally considered to be the main bottleneck that slows product development. Without standard chip fabrication processes, each company or research lab has to reinvent the wheel by developing own fabrication processes and operation techniques. Furthermore, adoption of EWOD DMF remains limited to only a few specific applications. For example, despite the versatility for numerous molecular diagnostic applications, currently only three products are on the market: ePlex by GenMark[31] for respiratory pathogen detection, SEEKER and FINDER by Baebies[32] for lysosomal storage disorders (LSD) detection and glucose-6-phosphate dehydrogenase (G6PD) deficiency, respectively. The limited applications of EWOD DMF, despite its inherent versatility, is also associated with the technical and cost barriers of chip fabrication. Additionally, design of chip and development of control system pose a practical challenge, discouraging students, resource-limited research labs, and startups from exploring EWOD DMF for own ideas or applications when quick proof-of-concept verifications are highly desired.

Drawing a comparison to digital IC, Fig. 1 illustrates the obstacles encountered by EWOD DMF today. The remarkable success of the IC industry can be attributed to the standardized infrastructure that makes chip design and manufacturing accessible for a vast user base, as visualized in Fig. 1(a). This standardization enables high-volume production, which, in turn, lowers technological hurdles and reduces manufacturing cost, creating a positive feedback loop that fosters industry growth. In contrast, without standardized infrastructure for EWOD DMF, users have to build everything by themselves – from design and fabrication of DMF chip to development of DMF control system – before they can test their ideas and applications, as visualized in Fig. 1(b). Two decades of anecdotal experiences and numerous observations have led us to identify that the lack of standardized design and manufacturing is the main obstacle that has been hindering the wide adoption and commercialization of EWOD DMF. The challenges are categorized and discussed below:

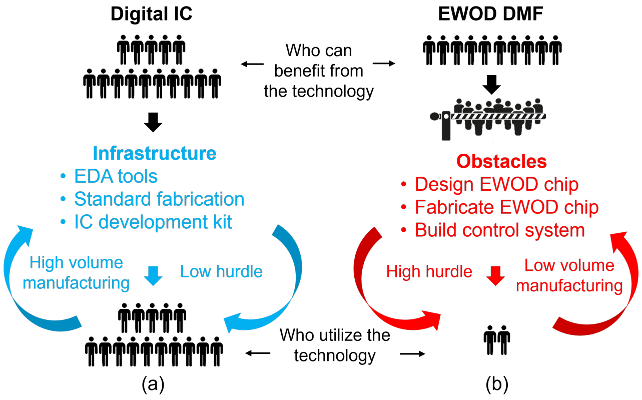


Fig. 1 The current ecosystems of (a) digital IC vs. (b) EWOD DMF

Chip design: Designing a manufacturable EWOD chip requires following foundry's design rules akin to the design rules of IC. However, most potential users of EWOD DMF, often with backgrounds in molecular biology and chemistry, are not familiar with the photolithographic fabrication of IC or micro electro mechanical systems (MEMS). Consequently, it takes a long time for them to acquire the fabrication knowledge and understand the design rules. Furthermore, the lack of specialized electronic design automation (EDA) tools for EWOD DMF forces designers to create chip layouts with conventional software and perform wire routing manually. This practice is time-consuming and error-prone, necessitating iterations of costly fabrication and testing.

Chip fabrication: The fabrication of functional and reliable EWOD chips presents a significant challenge. Various parameters, including those atypical for IC fabrication (e.g., material, thickness, deposition condition, hydrophobic layer) must be properly selected, depending on many factors such as sample liquid properties, operation condition (e.g., temperature), chip configuration (i.e., parallel plates or coplanar configuration), and actuation parameters (e.g., voltage, frequency). For prototyping, if an academic lab or startup opts to develop its own fabrication process, it typically takes several months for a student or technician to obtain basic training and longer to fabricate simple EWOD chips. For commercialization, where reliability is crucial, even after successful prototyping, three well-known EWOD chip failure mechanisms loom to undermine its reliability: current leakage (a short-term failure)[33-35], electric charging (a long-term degradation)[36,37], and biofouling[38,39]. While these fundamental problems have not been fully resolved, certain techniques can help alleviate the problems to achieve an acceptable product life cycle.[38-41] However, learning and applying these techniques further complicate the development of EWOD DMF, resulting in slow commercialization and limited applications.

Chip control: Operating an EWOD chip requires a relatively high voltage (i.e., rarely below 40 V and commonly over 100 V) to power many electrodes independently, often involving multiple electronic instruments including a high-voltage source. The absence of a user-friendly control system is frequently a practical deterrence, especially for biology and chemistry researchers without engineering background. While open-source hardware such as OpenDrop[42] and Dropbot[43] exists, they have a limited number of independent control channels (e.g., less than 128). Moreover, in practice these devices only work with their own EWOD chips, lacking the versatility to serve a diverse user base with widely different needs.

Consequently, the lack of standardized design, convenient manufacturing, and versatile control system renders EWOD DMF inaccessible to a wide range of users. At the same time, the technological hurdles in chip manufacturing prevent readily available fabrication services, leading to high chip costs. This, in turn, discourages potential foundries and other entities from investing in manufacturing infrastructure, creating a chicken-and-egg dilemma that prevents the industry growth and hinders the full potential of DMF from being reached, as summarized in Fig. 1(b).

2. Framework and Workflow of the Platform

To overcome the above obstacles and democratize DMF, a cloud-based cybermanufacturing ecosystem for EWOD DMF has been envisioned.[44,45] Here we report the first proof-of-concept design and manufacturing platform for EWOD DMF, laying the groundwork for the envisioned DMF ecosystem. The platform consists of four main components: (i) EWOD chip design platform, (ii) EWOD chip manufacturing platform, (iii) marketplace for EWOD control systems and ancillary modules, and (iv) DMF online community. The workflow of the platform is schematically described in Fig. 2. To design an EWOD chip, a user can visit the design platform and create a layout file by drawing desired patterns of EWOD electrodes on a virtual canvas and letting the imbedded software generate the wire routing, completing a design file. To have EWOD chips fabricated, a user can upload the design file to the manufacturing platform and select desired specifications (e.g., chip type and quantity), based on which the platform will suggest chip foundries. Once the user selects a foundry and places an order, the foundry manufactures, packages, and ships the chips to the user. To utilize EWOD chips, a user can order an electronic control system and ancillary modules (e.g., an overhang camera, temperature controller, and magnetic actuator) through the online marketplace. To perform own experiments on the EWOD chip, a user can program desired droplet operation protocols using a web-based graphic user interface (GUI) available on the platform and execute these protocols on the chip via the control system. Through an online community, users are encouraged to share their chip designs, droplet protocols, and experiences with fellow users and providers.

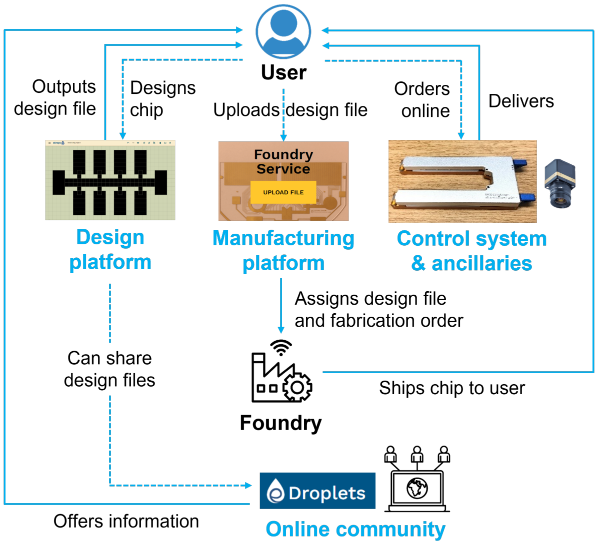
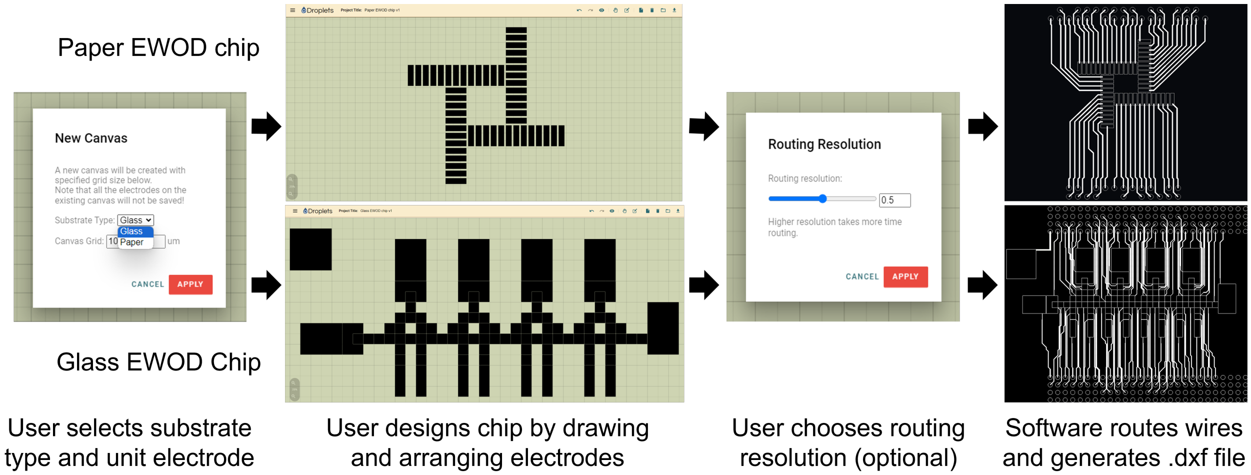


Fig. 2 Workflow of the cloud-based design and manufacturing platform for EWOD DMF. Broken lines and arrows indicate user operations while solid lines indicate platform operations.

The ultimate vision of this initiative is to establish a publicly accessible platform, allowing anyone to utilize EWOD DMF at an affordable cost, without the need to develop any infrastructure themselves. For one, the platform would support design and manufacturing for common types of EWOD chips, whose fast growth to a large volume is likely to attract commercial foundries. It would also provide a platform for users to obtain control systems, software, and ancillary modules for different experiment protocols offered by various hardware and software developers. Since achieving the full vision is beyond the scope of this paper, instead here we will demonstrate a proof-of-concept platform with a basic workflow and outline the current development status of the platform in the following sections. The goal is to inspire and attract both academic and commercial entities to participate in the development of the cloud platform and overcome the technological obstacles of EWOD DMF in a collective and synergistic manner.

3. EWOD Chip Design Platform

Since its layout essentially comprises a large number of similar electrodes, EWOD DMF presents a unique opportunity to build on standard unit cells predefined to meet the design rules for manufacturing, lowering the barrier of EWOD chip design and ensuring manufacturability. Inspired by EDA tools for IC, which incorporate IC design rules, we have developed an EWOD chip design platform (http://cad.edroplets.org/) that incorporates EWOD design rules. Currently, the design platform offers two exemplary chip types fabricated in two labs acting as foundries for this report: single-layer glass-based chip by the Nanolab at UCLA and single-layer paper-based chip by the Biological Interface lab at Sogang University. Here, single layer means all EWOD electrodes are fabricated on one conductive layer.



New Canvas

A new canvas will be created with specified grid size below.
Note that all the electrodes on the existing canvas will not be saved!

Substrate Type: Glass (Glass / Paper)

Canvas Grid: 10 um

Routing Resolution

Routing resolution: 0.5

Higher resolution takes more time routing.

Fig. 3 Workflow of the EWOD DMF design platform for single-layer EWOD chip (http://cad.edroplets.org)

For EWOD DMF, a unit cell (referred to as "unit electrode" hereinafter) can be defined by (i) electrode pitch (i.e., size + gap), (ii) shape (e.g., square, hexagon), and (iii) gap between adjacent electrodes. As illustrated in Fig. 3, the design workflow allows users to draw desired layouts of unit electrodes on a canvas using a "painting pen" function. We selected the common square shape with a few different pitches (i.e., 500 µm, 1000 µm, 1500 µm, 2000 µm, and 3000 µm) as a set of unit electrodes. Based on the fabrication capabilities of the two acting foundries, 5 µm and 30 µm were selected as electrode gaps for glass-based and paper-based EWOD chips, respectively. These conservative design rules would ensure any allowed design will lead to a working chip despite the uncertainties in current fabrication and assembly, which will improve over time. A virtual canvas with variable grid size was implemented in the design platform to define the available sizes and positions of unit electrodes. By arranging and merging multiple unit electrodes on the canvas, one can create electrodes with various shapes and sizes for complex layouts while following the design rules. As an example of standardization that dramatically simplifies the overall experience of users, we assume all the EWDO chips will have contact pads that match the pogo pins in the electronic control system detailed in section 6.

For a single-layer EWOD chip, drawing routing wires to connect many EWOD electrodes with as many contact pads can be time-consuming and error-prone, especially daunting if the number of electrodes is large, e.g., over 100. To address this issue, an automated wire routing algorithm has been developed[46,47], implemented in the design platform, and utilized here for the glass-based and paper-based chips with various electrode sizes and shapes. The wire routing algorithm consists of three primary steps: (1) routing graph generation, which creates a graph with meshes to define available wire paths between the EWOD electrodes and contact pads based on design rules, (2) path selection and routing, which determine optimal wire connecting point and shortest wire path for each electrode and generates wires to connect electrodes with contact pads, and (3) chip design file generation, which produces a .dxf file that foundries can use for chip fabrication. The user may ask the software to create either all the 256 contact pads to match the 256 pogo pins of the electronic control system described in section 6 or create only those wired to EWOD electrodes among the 256 contact pads. The former is useful for glass chip with a transparent indium tin oxide (ITO) layer, for which the full array of 256 contact pads helps user align the chip to the control system (detailed in section 6), while the latter is useful for paper chip with a printed conductive layer, for which a small number of silver contact pads helps save ink consumption.

Equipped with a drawing canvas, which features embedded design rules and automatic wire routing, and a user-friendly workflow, the platform offers an accessible design tool that helps lower technological barriers and expedite the EWOD chip design process. Importantly, the design algorithm includes design rules as variable parameters, which can be easily modified to satisfy different design rules from different foundries. Currently, the platform supports the design of single-layer EWOD chips and has demonstrated its utility via glass-based and paper-based chips. Single-layer EWOD chips are suitable for relatively simple on-chip protocols since they can accommodate only a limited number of electrodes due to wire-routing constraints[48]. For applications requiring a dense array of electrodes, multi-layer (e.g., PCB) or active matrix (e.g., TFT) EWOD chips provide more practical solutions. To design multi-layer and active matrix EWOD chip, which the design platform is expected to serve in the future, open-sources (e.g., KiCAD) or commercial software (e.g., Altium Designer and Cadence Virtuoso) can be used.

4. EWOD Chip Fabrication

Learning from the IC industry, which significantly benefited from standardization and modularity, we advocate to establish standardized fabrication processes for EWOD chips, which will free users from the need to develop their own fabrication processes and learn the intricacies of addressing reliability issues. To start, Table 1 categorises currently prevalent types of

Table 1 Comparison of four main substrate types for EWOD chips

Chip Type	Glass	Paper	PCB	TFT
# of electrodes	~100	~50	~500	10000
Electrode size	~1 mm	~3 mm	~2 mm	0.1–1 mm
Surface roughness	Low	High	High	Low
Cost	High	Low	Medium	High
Key feature	Transparent	Fast process	Multi-layer	Active matrix

EWOD chip and compares their key characteristics, such as common number and size of electrodes, surface roughness, fabrication cost, and unique features.

Glass-based single-layer EWOD chips are a popular choice for academic research[1,18,22,49] due to several advantages. Glass is available as circular wafer and compatible with IC clean room processes like silicon, allowing small size of and gap between EWOD electrodes. It is also transparent and smooth, offering additional freedom for sample observation and lowering required voltage for droplet manipulation (e.g., below 100 V)[50], respectively. Paper-based single-layer EWOD chip can be fabricated using an inkjet printer without requiring a photomask or cleanroom facilities. Featuring fast, simple, and low-cost manufacturing, the paper-based EWOD chip is particularly suitable for rapid prototyping and even considered favorable for environmental sustainability.[51] However, it is limited by surface roughness and low printing resolution, necessitating higher voltages and larger electrode sizes for droplet actuation.[52,53] Practically all single-layer EWOD chips share the inherent drawback of limited number of electrodes due to wire-routing constraints[48]. Developed to overcome the routing issue on a single-metal-layer substrate, PCB-based EWOD chips allow plenty of electrodes on a given substrate.[54-58] They have become the choice for most commercial EWOD products today, in part benefiting from the large price drop in PCB industry in the 2000s. However, PCB EWOD chips are restricted by the high surface roughness and pattern steps, necessitating a filler fluid or higher voltage (e.g., more than 120 V) for droplet manipulation unless the PCB surface is polished.[54,55] More recently, thin-film-transistor (TFT)-based active matrix (AM) EWOD chip has emerged as a promising technology for DMF.[59-62] Leveraging the infrastructure of the display industry, tens of thousands of electrodes with ~100 µm in size and each powered by a set of transistors can be fabricated on a glass substrate, opening a door for high-throughput, high-resolution applications (e.g., single-cell based assay).[63-65] Although the TFT-based EWOD chip was considered to be prohibitively expensive, some companies in the display industry have begun to explore AM EWOD, utilizing their existing TFT manufacturing facilities[66,67] and leading to more affordable fabrication.

To accommodate various application requirements (e.g., number of electrodes, cost, and driving voltage), we envision to establish standard fabrication processes for four types of EWOD chips: (i) glass-based single-layer EWOD chip, (ii) paper-based single-layer EWOD chip, (iii) PCB-based multi-layer EWOD chip, and (iv) TFT-based AM EWOD chip. If the fabrication is standardized, users can focus on their applications without the burden of developing own fabrication processes, accelerating technology adoption. Although single-layer glass EWOD chips have been the most popular choice in the past two decades especially for academic research, we anticipate some of them will be replaced by TFT-based EWOD chip in coming years, especially for commercial applications.

Establishing standard fabrication for all the above EWOD chip types will require extensive process development and involve commercial foundries, which is beyond the scope of this paper. To get started, in this report we utilized commonly used fabrication processes to fabricate the aforementioned four types of EWOD chips with distinct configurations, as summarized in Fig. 4. Shown in Fig. 4(a), single-layer glass-based EWOD chip was designed by using the EWOD design platform described in section 3. The chip was completed in parallel-plate configuration (i.e., closed device with top and bottom plates) to enable droplet creation. The substrate (i.e., bottom plate) of the chip was fabricated on a 4-inch glass wafer covered with a 180 nm-thick ITO layer. ITO was patterned using photolithography and wet etching to form EWOD electrodes. A 2 µm-thick silicon nitride layer was deposited using plasma-enhanced vapor deposition (PECVD). The hydrophobic topcoat was made by spin-coating 70 nm Cytop. The contact pads were protected by a Kapton tape as a shadow mask while the dielectric and hydrophobic layers are coated and subsequently exposed for electrical connection. To make the cover (i.e., top) plate, ITO glass was purchased (University Wafer) and coated with Cytop. Two layers of copper tape were used to create a 200 µm gap

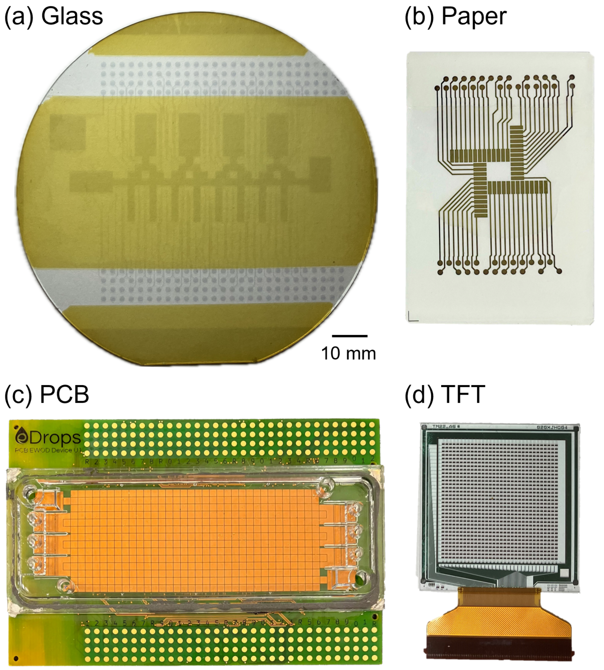

(a) Glass
(b) Paper
(c) PCB
(d) TFT

Fig. 4 Pictures of four different types of EWOD DMF chips fabricated to support the platform. (a) Glass-based chip, (b) Paper-based chip, (c) PCB-based chip, and (d) TFT-based chip. The scale bar applies to all pictures.

between the top and bottom plate and also electrically connect them.

Shown in Fig. 4(b), single-layer paper-based EWOD chip was designed by using the EWOD design platform described in section 3. The chip was completed in one-plate configuration (i.e., open device with no top plate) to enhance the featured simplicity, low cost, and fast turn-around. The electrode patterns were printed using a Fujifilm Dimatix printer equipped with silver nanoparticle (AgNP) conductive ink. The printed conductive ink electrode was sintered at 170°C for 15 minutes, resulting in low resistance. Subsequently, a dielectric layer of polysulfone and a hydrophobic layer of Teflon were deposited by spin coating. The spin-coated films were annealed at 100°C for 15 minutes after each coating process to relieve internal stresses. Finally, the chip was immersed in silicone oil (5 cSt) for 12 hours, resulting in an oil-impregnating surface that facilitates liquid movement.

Shown in Fig. 4(c), the multi-layer PCB-based EWOD chip was designed by using an open-source software, i.e., KiCAD. The chip was completed in parallel plate configuration (i.e., closed device with top and bottom plates) with filler oil to facilitate droplet operations. More than 500 electrodes were implemented on a single chip to accommodate various complex protocols. The bottom plate including dielectric layer was fabricated by a PCB manufacturer and covered with hydrophobic layer by spin-coating Cytop at UCLA. The top plate was ordered from a plastic injection molding company and coated with a conductive polymer and a hydrophobic layer at UCLA. Developed as the first standard and universal EWOD chips for the proposed platform, the PCB-based EWOD chip will be reported in detail as a separate publication.

Shown in Fig. 4(d), TFT-based EWOD chip with a square array of 32 x 32 electrodes each of 1 mm in size was ordered from TIANMA Microelectronics Corp. The chip was completed in parallel-plate configuration with air environment (i.e., no filler oil used) at UCLA to showcase the advantage of its smooth surface and low topography. The bottom plate was hydrophobized by spin-coating Cytop, and the top plate was fabricated and assembled with the bottom plate using the process described for the glass-based EWOD chip above.

We have verified the above four types of EWOD DMF chip for basic droplet operations and had some of them tested by a small number of collaborating labs (see Acknowledgements). Most of the fabrication services will be open in near future for select groups of users to further improve and validate the fabrication processes. After a few additional phases of progress for quality control, we aim to open the fabrication platform for the public, thereby enabling boarder participation from academic labs, startups, and foundries.

5. EWOD Chip Manufacturing Platform

Once fabrication processes are standardized and foundry processes ready for service in the future, we envision a fully functional manufacturing platform. When matured, the platform will allow users to access the fabrication capabilities and pricing information from various foundries so that users can select a suitable foundry for their applications. The standardized fabrication processes will define critical fabrication parameters, such as (i) type and size of chip, (ii) thickness and deposition method of dielectric and hydrophobic layers, and (iii) gap between top and bottom plates for parallel-plate devices. Consequently, foundries would only require two pieces of information from the user: a chip design file made on the design platform and the quantity of chips being ordered. This streamlined approach will simplify the foundry service workflow, making the chip ordering easy even to users with little background in EWOD technology.

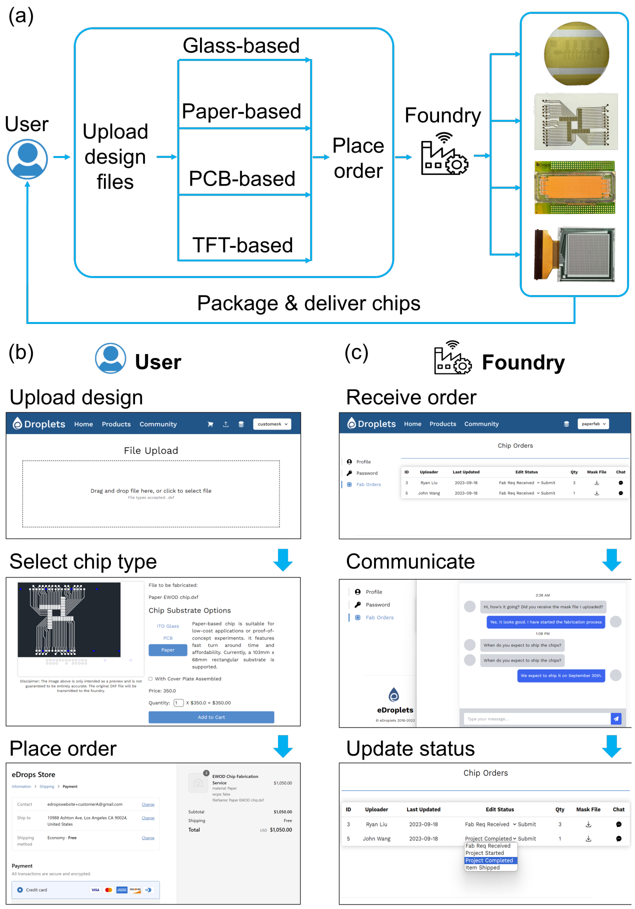


Fig. 5 Workflow of the EWOD DMF manufacturing platform. (a) Overview of the foundry service workflow. (b) Web interfaces of the platform for users, and (c) Web interfaces of the platform for foundries.

In the current stage, we have prototyped a manufacturing platform that demonstrates a foundry service workflow, as schematically illustrated in Fig. 5(a). As shown in Fig. 5(b), users can upload chip design files, select chip types and quantities, and place an order. Upon confirmation and payment, the platform assigns the order to a designated foundry for manufacturing. As shown in Fig. 5(c), foundries can log into the platform with own accounts and accept the assigned order, update the project status, and ship the fabricated chips to users. Until commercial foundries are established, which will take some time, the Biological Interface Lab at Sogang University and the Micro and Nano Manufacturing Lab at UCLA may act as

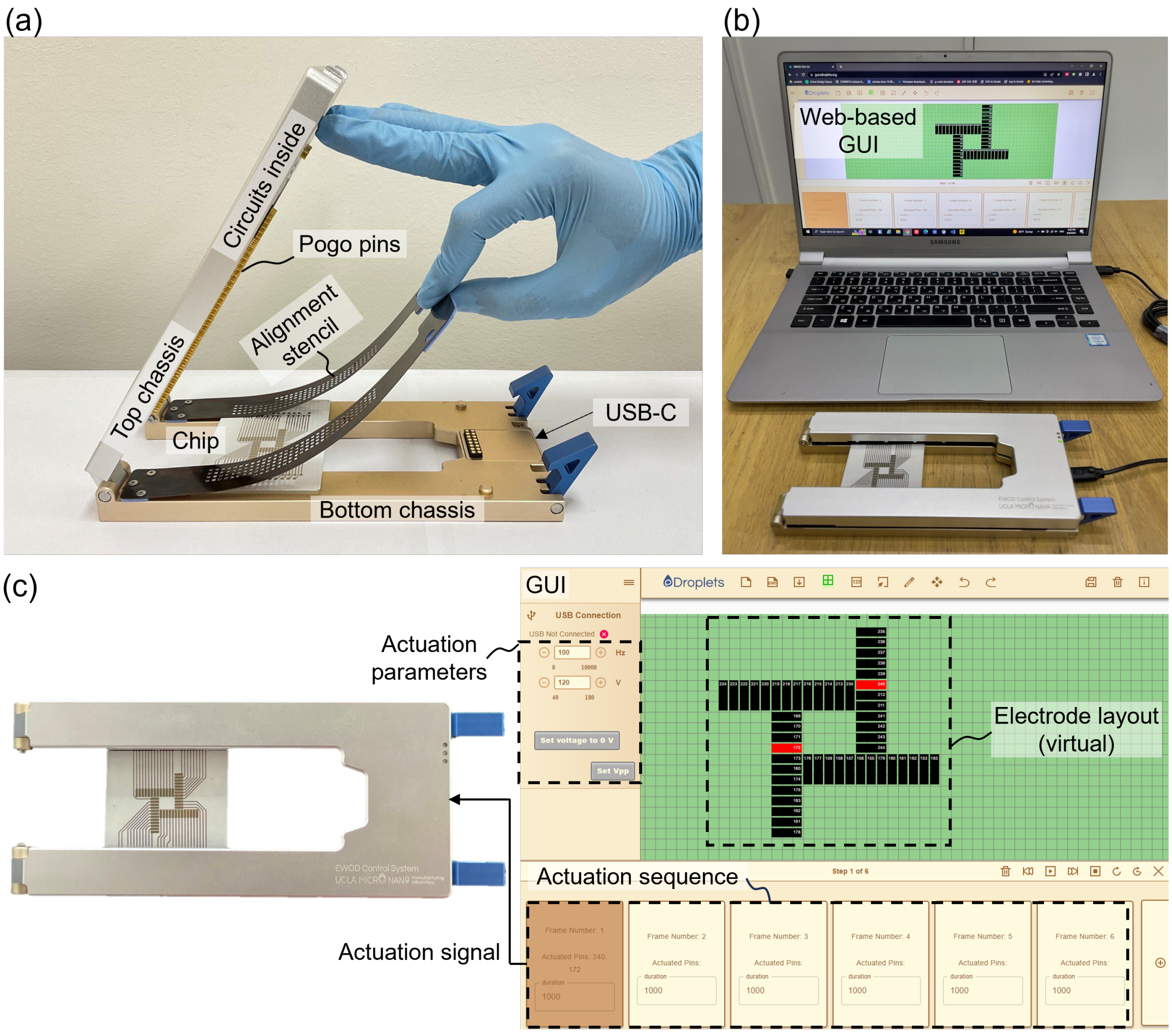


Fig. 6 An electronic control system developed for passive EWOD chips (shown with a paper-based chip). (a) A picture of the system when opened, (b) A picture of the system USB-connected to a computer, which provides power and software, and (c) Web-based GUI in actuation sequence programming mode using the electrode layout imported from the design file.

provisional foundries to fabricate the paper-based and glass- or PCB-based EWOD chips, respectively. For TFT-based EWOD chips, currently TIANMA Microelectronic Corp. has been identified as a potential foundry. Although not all the fabrication services outlined here will be available to the public soon, most of them will be open for a limited number of requesting users while improving the utility and reliability of the cloud-based manufacturing platform. As the standardization matures and user base grows, we anticipate that commercial foundries will join the platform to provide industrial fabrication services, helping the platform grow toward a self-sustaining ecosystem for DMF.

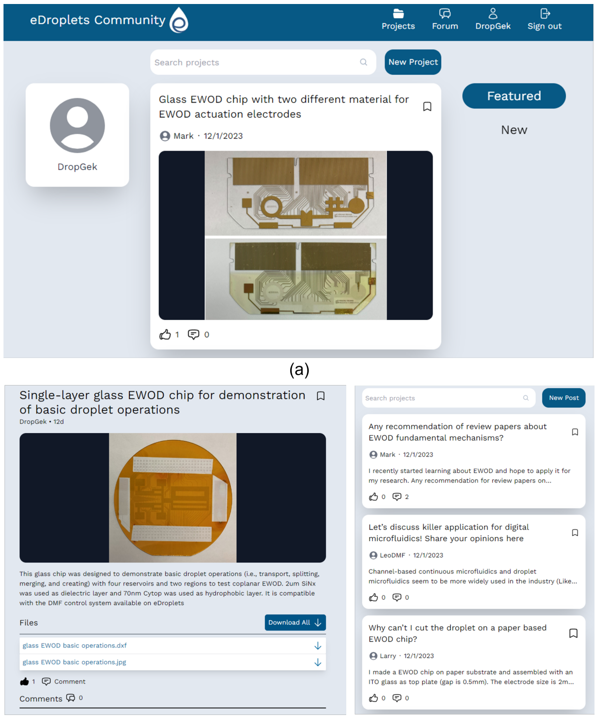
6. Marketplace for EWOD Control Systems and Ancillary Modules

Once receiving EWOD chips from a foundry, a user will need an electronic control system and perhaps ancillary modules (e.g., overhang camera, temperature control module, magnetic actuator) as well to operate the chip for their experiments. We envision an online marketplace for users to order various open-source or commercial control systems as well as ancillary modules provided by hardware developers and companies. The format of the chip-system interface (e.g., a contact pad array with fixed pitch for passive EWOD chips; a flexible printed circuit (FPC) with fixed number of pins for AM EWOD chips) will be standardized and released to the hardware developers and other users via the platform. The standardized format of chip-system interface is also implemented in the chip design platform so that all the chips designed and fabricated through the platform can be operated by any control system and ancillary as far as they follow the standard.

In the present study, we have developed a compact electronic control system compatible with all passive EWOD chip types (e.g., glass, PCB, silicon, and paper) of diverse shapes, sizes, and thicknesses,[68] as shown in Fig. 6(a), to complete demonstrating the workflow from chip design and fabrication to chip control. As shown in Fig. 6(b), the control system is powered and operated by a computer through a USB cable. A web-based GUI (https://gui.edroplets.org/) was developed for the operation and is accessible on the platform. As shown in Fig. 6(c), a user can create the virtual electrode layout on the GUI canvas after simply converting the design file to an operation file (named .ewds for EWOD sequence) on the platform. By assigning actuation parameters (i.e., voltage and frequency) and selecting virtual electrodes for on or off, a user creates one actuation step (referred to as “frame” in the GUI). Multiple frames define an actuation sequence, and a user can run the sequence on the computer, which transfers electric signals to the control system via USB. Actuation sequence files can be saved in a standardized format named as .ewds, facilitating the sharing of experiment protocols.

As shown in Fig. 6(a) and (b), the EWOD control system includes four main components: (1) system hardware (chassis), (2) electronic circuits, (3) chip-system interface, and (4) web-based GUI. The system hardware, which consists of two aluminium chassis (plates), arrays of pogo pins, and an alignment stencil, ensures quick and easy loading and unloading of EWOD chip. Housed in the aluminum chassis, the control circuits utilized HV3418, a serial-to-parallel high-voltage converter, to provide voltages in the range of 40–180 V DC or 80–360 V_{pp} AC at frequency up to 10 kHz through 256 output channels. The chip-system interface utilizes a 256 spring-loaded pogo-pin array that aligns with and presses on the 256 contact pads on an EWOD chip to provide electric signals. A unique chip-system alignment mechanism was designed by using a polyimide stencil with 256 through-holes. After placing an EWOD chip on the bottom stage (chassis) and letting the stencil rest on the chip, the user can nudge the chip until all the contact pads on the chip are clearly seen through the holes, which indicates successful alignment. Then, the system can be swing closed until the latches lock and secure the chip. With all the pogo pins passing through the holes and landing on the contact pads, electric connection between the system and the chip is established and ready for operation. The U-shape chassis design accommodates integration of ancillary modules, such as heaters or sensors, by leaving sufficient space below the installed chip.

For most simple biological and chemical protocols, 256 independent control channels should be sufficient to control passive EWOD chips for on-chip experiments. However, more complex protocols or highly multiplexed assays may require an AM EWOD chip to independently control a large number of electrodes. In this study, we used a prototype electronic control system for AM EWOD chip provided by TIANMA Microelectronics for testing. Companies such as ACXEL have also developed own AM EWOD control systems for various applications. Developing a universal AM EWOD control system will require more complicated driving circuits and control algorithm to manage a large number of electrodes (i.e., more than 100,000). Developers and companies with expertise in display module design may develop a universal AM EWOD control system and make it available via the marketplace platform in the future.



Glass EWOD chip with two different material for EWOD actuation electrodes

Mark · 12/1/2023

1 0

(a)

Single-layer glass EWOD chip for demonstration of basic droplet operations

DropGek • 12d

This glass chip was designed to demonstrate basic droplet operations (i.e., transport, splitting, merging, and creating) with four reservoirs and two regions to test coplanar EWOD. 2um SiNx was used as dielectric layer and 70nm Cytop was used as hydrophobic layer. It is compatible with the DMF control system available on eDroplets

Files

glass EWOD basic operations.dxf

glass EWOD basic operations.jpg

1 Comment

Comments 0

(b)

Any recommendation of review papers about EWOD fundamental mechanisms?

Mark · 12/1/2023

I recently started learning about EWOD and hope to apply it for my research. Any recommendation for review papers on...

0 2

Let’s discuss killer application for digital microfluidics! Share your opinions here

LeoDMF · 12/1/2023

Channel-based continuous microfluidics and droplet microfluidics seem to be more widely used in the industry (Like...

0 0

Why can’t I cut the droplet on a paper based EWOD chip?

Larry · 12/1/2023

I made a EWOD chip on paper substrate and assembled with an ITO glass as top plate (gap is 0.5mm). The electrode size is 2m...

0 0

(c)

Fig. 7 EWOD DMF online community (https://community.edroplets.org). (a) Home page of the project gallery, (b) Web page of a shared project, and (c) Web page of questions on the user forum.

7. DMF online community

We have developed an online community, which currently includes a project gallery and a user forum. Drawing inspiration from open-source project repositories in the software industry (e.g., GitHub), a DMF project gallery allows users to share their chip designs and experiment protocols in a standardized format, as shown in Fig. 7(a). This enables other users to download, modify, and create derivative designs and protocols. Currently, the project gallery allows users to share their EWOD chip designs by uploading files in .dxf and write a description of key features for their chips. It also allows other community users to comment on the project for questions and discussions. Fig. 7(b) shows the web page of an example project. Additionally, an online forum offers a place where users can ask questions, provide answers, share practical experiences, and offer feedback on tools and services. Fig. 7(c) shows a list of example questions on the user forum web page. By fostering sharing, the online community will help create additional knowledge, generate new data, and expand the user pool to facilitate synergistic growth of the DMF ecosystem.

8. Conclusion and Outlook

Identifying technological and resource hurdles as the main culprit for the slower-than-expected adoption of EWOD DMF, we have proposed a standardized design and manufacturing platform for EWOD DMF to catalyse an easy and widespread adoption of the technology for education, research, and commercialization. In line with this vision and to kickstart, we have developed a proof-of-concept cloud-based design and manufacturing platform for EWOD DMF composed of four components: (i) chip design platform with automatic wire routing, (ii) chip manufacturing platform with the foundry service workflow, (iii) marketplace for control systems and ancillary modules, and (iv) community to share information. Four substrate types (i.e., glass, paper, PCB, and TFT) of EWOD chips have been fabricated and tested for common droplet operations, setting the direction toward a fully functional platform with a set of standardised fabrication processes for various applications in the future. By demonstrating the workflow of the platform that lowers engineering and cost burdens for prospective users, we anticipate growing acceptance of EWOD DMF. As the technology becomes more accessible, we envision the user base to reach a critical mass so that an increased production volume lowers the manufacturing cost, which in turn would further expand the user base. The resulting positive feedback loop akin to the IC industry would allow EWOD DMF to achieve the much-anticipated revolution for LoC applications.

Author Contributions

Conceptualization: C.-J. K., J. L., and Q. L. W. Investigation: Q. L. W., E. H. C., J. L., H.-C. H., S. K., Y. P., and L. X. Methodology: Q. L. W., E. H. C., J. L., H.-C. H., S. K., L. X., K. S., T.-Y. H., and C.-J. K. Project administration: C.-J. K. and Q. L. W. Resources: C.-J. K., T.-Y. H., and K. S. Funding acquisition: C.-J. K., T.-Y. H., K. S. Software: Q. L. W., H.-C. H., K. T., S. K., Z. H., B. C., D. Y., C.-C. W, and C. C. Supervision: C.-J. K., T.-Y. H., and K. S. Writing – original draft: Q. L. W. and C.-J. K. Writing – review & editing: Q. L. W., H.-C. H., S. K., K. S., T.-Y. H., and C.-J. K.

Conflicts of interest

There are no conflicts to declare.

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