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A Silicon-Based 0.3 THz Frequency Synthesizer With Wide Locking Range

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Abstract—A 300 GHz frequency synthesizer incorporating a triple-push VCO with Colpitts-based active varactor (CAV) and a divider with three-phase injection is introduced. The CAV provides frequency tunability, enhances harmonic power, and buffers/injects the VCO fundamental signal from/to the divider. The locking range of the divider is vastly improved due to the fact that the three-phase injection introduces larger allowable phase change and injection power into the divider loop. Implemented in 90 nm SiGe BiCMOS, the synthesizer achieves a phase-noise of −77.8 dBc/Hz (−82.5 dBc/Hz) at 100 kHz (1 MHz) offset with a crystal reference, and an overall locking range of 280.32–303.36 GHz (7.9%).

Index Terms—Active varactor, Colpitts, frequency generation, frequency synthesizer, injection-locked divider, multi-phase injection, phase-locked loop (PLL), terahertz, ring oscillator, triple-push VCO.

I. INTRODUCTION

THz BAND (0.3–3 THz), extending from the highest millimeter-wave (mm-wave) frequency range to the lowest infrared frequency, has drawn great attention. Recent research in the THz region is expanding to wide range of applications such as spectroscopy, imaging, and ultrahigh-data-rate wireless communications [1]–[6]. For imaging applications, due to the short wavelength and non-ionized characteristic of the THz wave, it provides a non-invasive and high spatial resolution image detection, which fits the requirement of security surveillance including stand-off imaging for detection of hidden objects [7], [8]. The SNR and the resolution can be improved by utilizing a synchronized carrier for time integration. For wireless communication applications, the availability of very wide unused bandwidth in the THz spectrum makes it possible to build up a wireless data-link with data rates in excess of tens of gigabits-per-second by using modulation scheme such as amplitude-shift keying (ASK) or on-off keying (OOK) [9]–[13]. Due to large atmospheric attenuation of THz waves, one promising application of this spectrum is in the area of scientific satellite communication [14], [15].

An accurate and stable THz source proves to be essential for coherent data link, active sensing, and frequency metrology. Recently, silicon-based signal sources at low-THz range (e.g., 200 and 300 GHz) using coupled VCOs and harmonic generation have been reported [16]–[18]. [19] proposes a push-push VCO in which the frequency variation is achieved using inductive tuning. The lower loss of inductive tuning mechanism compared to traditional varactor tuning makes this design amenable to THz frequency range. [20] presents a SiGe 530 GHz array-based radiator comprising 16 radiating elements each with its own ring-antenna and balanced triple-push oscillator with no tuning capability. Free-running signal sources exhibit severe frequency fluctuation and are vulnerable to temperature and process variations. Moreover, the VCOs reported in prior work exhibit limited tuning range, not often sufficient to tackle these variations and meet bandwidth requirements of the systems they are designed for. For example, in a radar system, both bandwidth and frequency of operation contribute to the resolution, in that, the former affects the cross-range resolution while the latter contributes to the range resolution [21]. Consequently, the need for precise oscillation frequency with wide tuning range and low close-in phase-noise calls for closed-loop source topologies. Millimeter-wave phase-locked loops (PLLs) incorporating push-push VCOs have been demonstrated up to 164 GHz [22] in silicon technologies. M. Seo *et al.* presented a 300 GHz PLL with 0.12% locking range and divider ratio of 10 in a III-IV technology [23]. Due to the low divider ratio, the PLL in this work demands a high-frequency input reference signal which could be generated from another PLL, resulting in a high phase-noise and system complexity.

In this paper, we present a 300 GHz frequency synthesizer incorporating a triple-push VCO with Colpitts-based active varactor (CAV) and a frequency divider with three-phase injection. The synthesizer, implemented in 90 nm SiGe BiCMOS with f_T/f_{MAX} of 240/315 GHz, achieves 7.9% of locking range (280.32–303.36 GHz) and generates −14 dBm of output power at 290 GHz. Based on the measurement result, the frequency scaled phase-noise of the 294.9 GHz signal is −77.8 dBc/Hz (−82.5 dBc/Hz) at 100 kHz (1 MHz) offset. The remainder of the paper is organized as follows. Section II discusses the synthesizer architecture and system-level consideration for THz frequency applications. Section III focuses on the analysis of the proposed VCO and divider. The measurement setup and measurement results are shown in Section IV with prior work comparison.
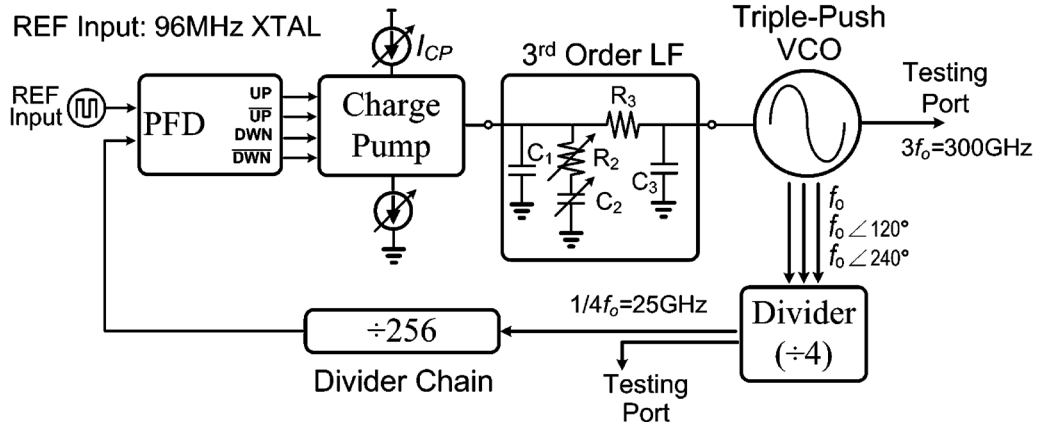
Fig. 1. The proposed architecture of the 300 GHz frequency synthesizer.

II. ARCHITECTURE OF THE THz FREQUENCY SYNTHESIZER

In a THz frequency synthesizer, the VCO and the first stage of the divider chain following the VCO are two of the most important building blocks which dominate the PLL performance including locking range, phase-noise, and output power. As the operation frequency approaches the device f_{MAX}, transistors barely provide sufficient power gain or negative resistance even with a proper feedback loop. The transistor's gain limitations along with severe loss of passive components such as capacitors, varactors and inductors make it difficult to design frequency dividers or fundamental oscillators at THz frequencies. A PLL operating at lower frequency followed by a frequency tripler (e.g., harmonic-based or injection locked tripler) alleviates some of the challenges, as was extensively discussed in [24]. While the harmonic-based tripler (HBT) is amenable to high frequencies close to f_{MAX} it consumes additional DC power and degrades the overall PLL phase-noise. The total phase-noise, $S_{\text{Total}}(\Delta\omega)$, of a lower-frequency PLL followed by the HBT is expressed as [24]:

$$S_{\text{Total}}(\Delta\omega) = 3^2 S_{\text{Fund}}(\Delta\omega) + S_{HT}(\Delta\omega) + S_{MN}(\Delta\omega) \quad (1)$$

where $S_{HT}(\Delta\omega)$ is the phase-noise of the low-frequency PLL, $S_{HT}(\Delta\omega)$ and $S_{MN}(\Delta\omega)$ represent the phase-noise contributions from the harmonic transistors (the transistors generating 3rd-harmonic signals) and the output matching network of the HBT, respectively. The tripler's noise contributions, $S_{HT}(\Delta\omega)$ and $S_{MN}(\Delta\omega)$, cause a deviation from the ideal value, that is, the HBT's input phase-noise $S_{\text{Fund}}(\Delta\omega)|_{\text{dB}}$ plus $20\log_{10}(3)$.

Fig. 1 shows the architecture of the proposed 300 GHz frequency synthesizer composed of a triple-push VCO, a three-phase injection locked divider ($\div 4$) followed by a $\div 256$ divider chain, a phase frequency detector/charge pump (PFD/CP) with a tunable current (I_{CP}: 150–300 μA), and a 2-bit programmable 3rd-order loop filter [25]. The input reference is fed by a 96 MHz crystal oscillator. The VCO's 3rd-harmonic signal will be the synthesizer's output ($3f_o = 300$ GHz) and its three-phase fundamental signals (f_o) are fed to the divider. The use of the triple-push VCO results in the injection of lower frequency signal f_o to the divider chain, thereby relaxing the divider design requirement and lowering its DC power consumption. Although one can clearly implement a higher harmonic

VCO and further decrease the fundamental frequency, but it is noteworthy that the VCO's harmonic output power will be limited by the transistor nonlinearity. Since no additional frequency multiplier follows the synthesizer in this design, the noise contribution of the harmonic generation transistors, $S_{HT}(\Delta\omega)$, in (1) will no longer exist, resulting in lower phase-noise.

Using the triple-push VCO, the first-stage divider within the synthesizer operates at around 100 GHz. An injection-locked frequency divider (ILFD) is commonly used at mm-wave frequencies [26]. Nonetheless, an ILFD exhibits small locking range, which limits the frequency range of the synthesizer. One of the solutions to improve the locking range is to use multi-phase injection [27]. The availability of three-phase fundamental frequency signals in the triple-push VCO allows us to consider an ILFD with three-phase injection. The proposed three-phase injection locked divider exhibits a wide locking range, which encompasses the VCO's tuning range. The synthesizer locking range, therefore, follows the VCO's frequency tuning range. The $\div 256$ divider chain uses ECL- and CML-type topologies for their wide bandwidth characteristic. The PFD is implemented based on a conventional structure similar to the one presented in [28]. By sending an "up" and a "down" current pulses to the CP during each reference cycle, the PFD dead zone is eliminated and the loop gain for small phase error is improved.

An on-chip third-order loop filter is utilized, in which C_2 produces the first pole and together with R_2 is used to generate a zero for the loop stability. C_1 is used to smoothen the control voltage ripples. R_3 and C_3 are used to further suppress reference spurs and high frequency noise. The loop filter's component values are $C_1 = 800$ fF, $R_2 = 13$ kΩ, $C_2 = 22$ pF, $R_3 = 21$ kΩ, and $C_3 = 300$ fF.

III. SYNTHESIZER BUILDING BLOCKS

A. Triple-Push VCO With CAV

An alternative way of producing a high frequency signal, especially when it is close to the transistor's f_{MAX}, is to make use of the oscillator's harmonics. To retain the output power, minimizing the resonator's loss at both the harmonic and fundamental frequencies is essential. For example, if the resonator's loss is minimized only at the oscillator's fundamental frequency
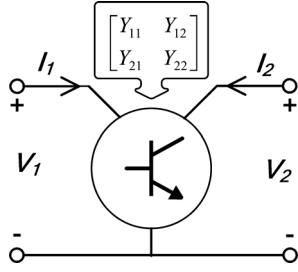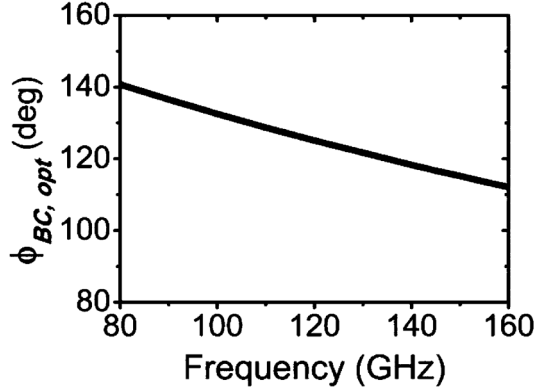
Fig. 2. A two-port Y-parameter representation of a single transistor.

Fig. 4. (a) A two-stage ring oscillator with a phase-shift of $65°$ between stages. (b) A three-stage ring oscillator with phase-shift of $10°$.

Fig. 3. The simulated $\phi_{BC,opt}$ versus frequency for a transistor with aspect ratio of $L_E/L_B = 4\,\mu m/0.09\,\mu m$ and biased at its maximum f_{MAX}.

Fig. 5. A conventional three-stage ring VCO employing a varactor in parallel with a buffer at the base terminals of the transistors.

and increased at its harmonics, the fundamental signal swing will be improved and the transistors will thus generate higher intrinsic harmonic power. This harmonic power, once passing through the resonator, will be degraded significantly. In addition, the frequency-tuning mechanism, introduced at the fundamental frequency, exhibits ever-increasing loss at the harmonic frequency, thereby further degrading the harmonic power. Besides, the relative input-output phase difference ϕ and gain A of single transistor, defined in Fig. 2, affects the output power that this transistor can generate [29]. If a transistor operates in its optimum condition, expressed by (4), it generates the maximum output power, as will be described later. In our VCO design, all these considerations are taken into account in order to improve the output power and subsequently, a better phase-noise if the VCO operates in the current-limited region [30], which is usually the case for THz VCOs.

Starting from the transistor's input-output phase and gain conditions, shown in Fig. 2 is a two-port Y-parameter representation of the transistor. The power generated from the transistor (P_G) is defined as [31]:

$$P_G = -A\,|V_1|^2\,|Y_{12} + Y_{21}^*|\cos\left(\angle\,(Y_{12} + Y_{21}^*) + \phi_{BC}\right) \quad (2)$$

where

$$A = \frac{|V_2|}{|V_1|}, \quad \phi_{BC} = \angle\,\frac{|V_2|}{|V_1|}. \quad (3)$$

In (2), P_G reaches its maximum absolute value if

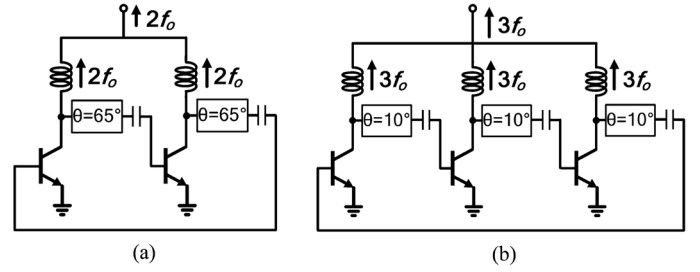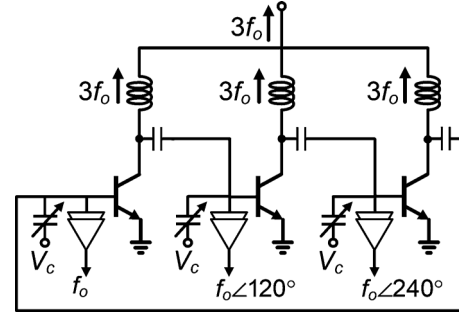$$\phi_{BC} = \phi_{BC,opt} = (2k+1) - \angle\,(Y_{12} + Y_{21}^*) \quad (4)$$

where k is an integer. Under a given bias condition, there exists an optimum phase difference between the base and the collector, $\phi_{BC,opt}$ that a transistor generates the maximum power. Fig. 3 shows the simulated $\phi_{BC,opt}$ versus frequency for a transistor with aspect ratio of $L_E/L_B = 4\,\mu m/0.09\,\mu m$ and biased at its maximum f_{MAX}. The optimum phase condition varies from $140°$–$110°$ across the frequency range from 80–160 GHz. In the proposed VCO design, the transistors are designed to satisfy this phase condition so as to achieve substantially better VCO performance.

Based on the net power analysis of the single transistor, a systematic approach of designing a 300 GHz oscillator is now described. A harmonic ring oscillator offers the ability to achieve $\phi_{BC,opt}$ by adding extra phase shift between stages. Fig. 4(a) shows an example of a two-stage ring (i.e., cross-coupled) oscillator, where the second harmonic signal $2f_o$ is retrieved from common output terminal. Referring to Fig. 3, $\phi_{BC,opt}$ at fundamental oscillation frequency of 150 GHz is $115°$. Because of the $180°$ constant phase difference between two stages, an extra phase shift of $65°$, realized using a t-line, is required to achieve $\phi_{BC} = \phi_{BC,opt}$. A larger phase shift requires a longer t-line with inevitably larger in-series loss in the signal path. This loss degrades the fundamental voltage swing inside the ring which, in turn, degrades the second harmonic power. Consequently, ring oscillators requiring larger extra phase shifts to achieve $\phi_{BC,opt}$ will produce smaller harmonic power. Shown in Fig. 4(b) is another example using three-stage ring. By virtue of its design, the three-stage ring oscillator requires a small phase shift of $10°$ to satisfy the optimum phase condition. In addition, compared to the two-stage counterpart, more branches participate in the harmonic power
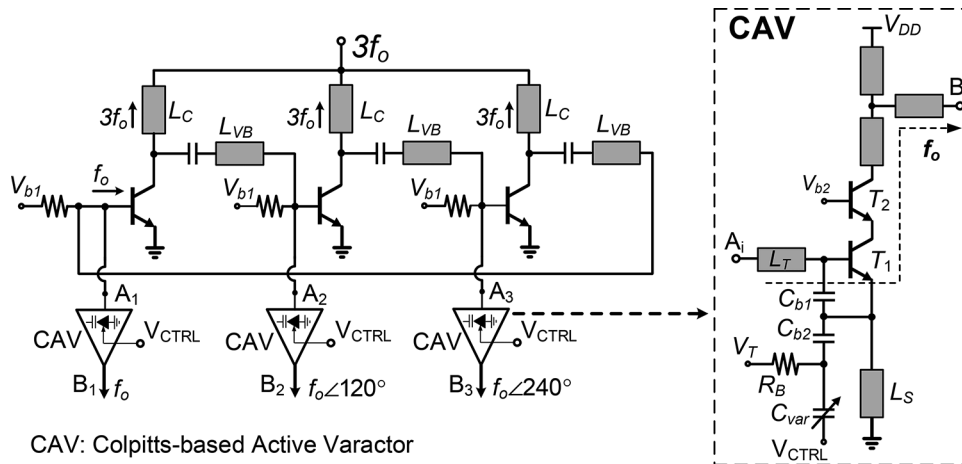
Fig. 6. The schematic of the proposed triple-push VCO with CAV.

generation, resulting in a higher output power. The three-stage ring oscillator is thus chosen as the VCO core.

The conventional approach for frequency tuning in a three-stage ring VCO, shown in Fig. 5, employs a varactor in parallel with a buffer at the base of each ring transistor. The input parasitic capacitor of the buffer, however, decreases the oscillation frequency. Decreasing the loading inductor, L_C, boosts up the oscillation frequency at the expense of lowering the gain of each stage. Both the loss of the buffer and the varactor degrades the base voltage swing of the ring transistor, especially the severe varactor loss at high frequency becomes a bottleneck. Therefore, a new frequency tuning circuitry called Colpitts-based active varactor (CAV) is introduced. The schematic of the VCO with CAV is shown in Fig. 6. The VCO's f_o is traveling along the VCO three-stage ring with 120° phase difference between stages. Its 3rd-harmonic signals generated from the transistors nonlinearity will be in-phase and collected at the common-mode output $3f_o$. The t-line L_{VB} is used to introduce 10° phase shift for transistor's optimum phase condition. When considering the phase shift of the L_{VB} across the VCO tuning range, the maximum phase deviation from $\phi_{BC,opt}$ is only 1.8°. The transistors still operates near optimum phase condition. In a conventional Colpitts oscillator, the Colpitts cell is an essential part of the oscillator that enables sustainable oscillation by providing loss compensation mechanism for the resonator. On the other hand, the CAV in this design merely realizes extremely low-loss tunable capacitance and isolates the varactor loss from the VCO ring. In addition, it buffers the VCO's f_o to the divider, and thus, avoids loading the VCO ring. In the CAV schematic, node A_i ($1 \leq i \leq 3$) is connected to each stage of the VCO ring and output node B_i ($1 \leq i \leq 3$) is connected to the divider. Inside the CAV, the cascode stage T_1-T_2 with its T-junction matching network buffers the VCO's f_o and feeds the signal to the divider. The bypass capacitor C_{b2}, the large resistor R_B, and bias voltage V_T are used to level-shift V_{CTRL} within the voltage range required by the charge pump. The t-line L_T models the short interconnect between the CAV and the VCO ring in the actual layout. The three CAVs are placed in close proximity of the VCO ring so that the L_T effect on the oscillation frequency and tuning range becomes negligible.
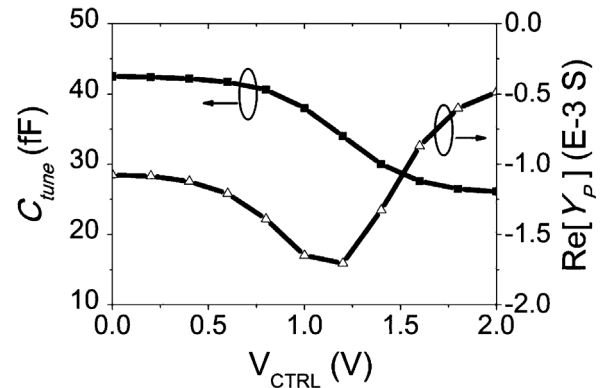

Fig. 7. The simulated tunable capacitor C_{tune} and the parallel conductance $\text{Re}[Y_P]$ of the CAV (seen from node A_i of Fig. 6).

Shown in Fig. 7 are the simulation results of the CAV including the tunable capacitor C_{tune} and the parallel conductance $\text{Re}[Y_P]$ seen form node A_i ($1 \leq i \leq 3$). C_{tune} monotonically decreases from 42–26 fF with V_{CTRL} varying from 0–2 V for frequency tuning. The negative conductance $\text{Re}[Y_P]$ across the tuning range compensates for the large varactor loss and also helps the VCO start-up condition. Shown in Figs. 8(a) and (b) are the simulated fundamental voltage swings of the conventional and the CAV-tuning VCOs, respectively, with the same tuning range and oscillation frequency. The proposed VCO achieves more than three times higher base voltage swing than the conventional counterpart. Fig. 8(c) shows the simulated phase noise, where the proposed VCO achieves 2.3 dB better than the conventional one. Fig. 8(d) shows the phase noise simulation of the proposed VCO over process and temperature variation.

In addition to providing 10° phase shift, the L_{VB} also enhances the $3f_o$ power collection by blocking the $3f_o$ from flowing to the next stage as shown in Fig. 9(a). The current source I_{3f_o} represents the 3rd-harmonic current generated from a transistor and C_p is the input parasitic capacitor of the next stage. At the 3rd-harmonic frequency, the series L_{VB} and C_P exhibits higher inductive impedance. Therefore, the large portion of the 3rd-harmonic current will flow into the load,
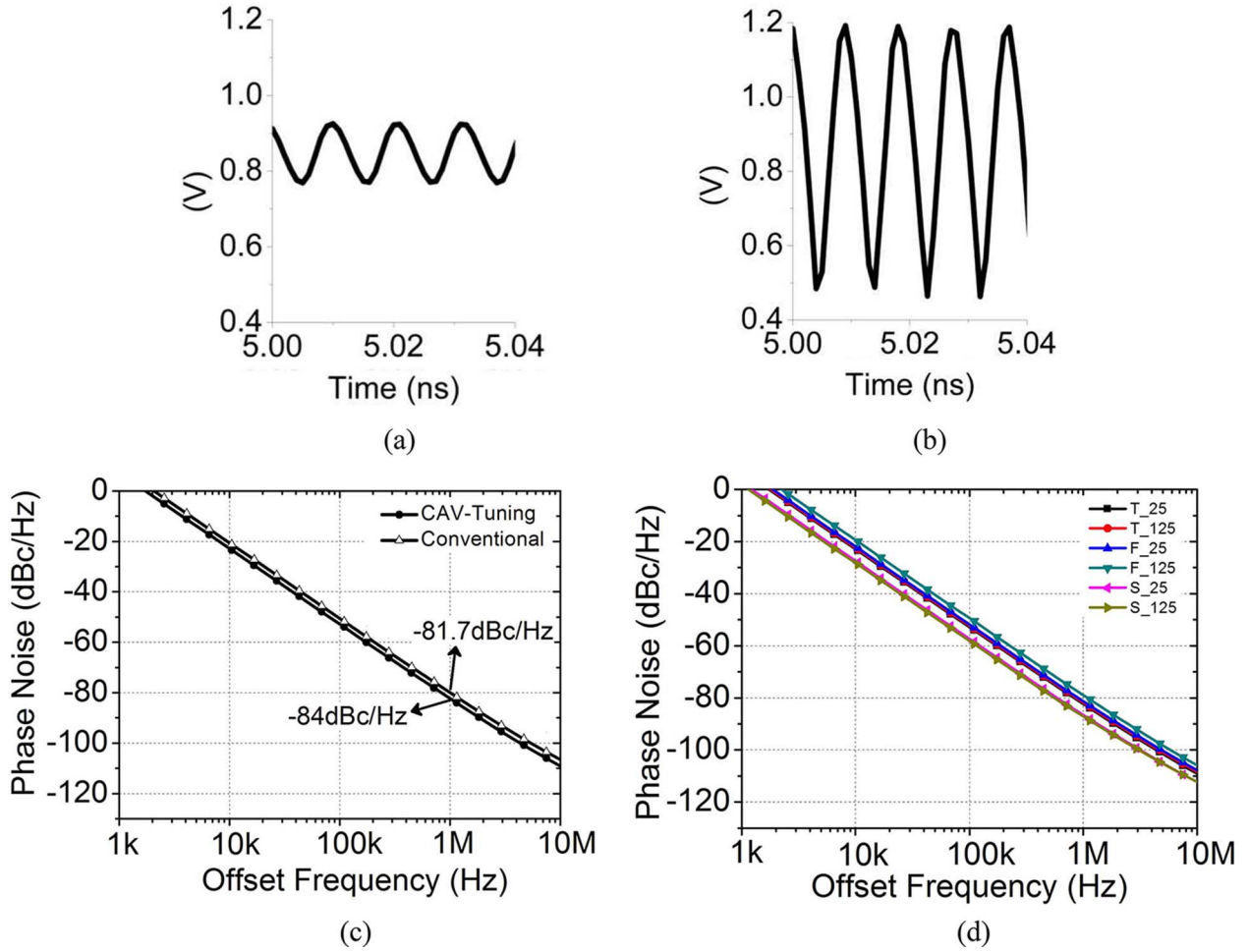
Fig. 8. The simulated fundamental voltage swings for (a) a three-stage ring VCO with a conventional varactor tuning as shown in Fig. 5, (b) a three-stage ring VCO with CAV-tuning, (c) their simulated phase noise, and (d) the phase noise simulation of the proposed VCO over process and temperature variation.
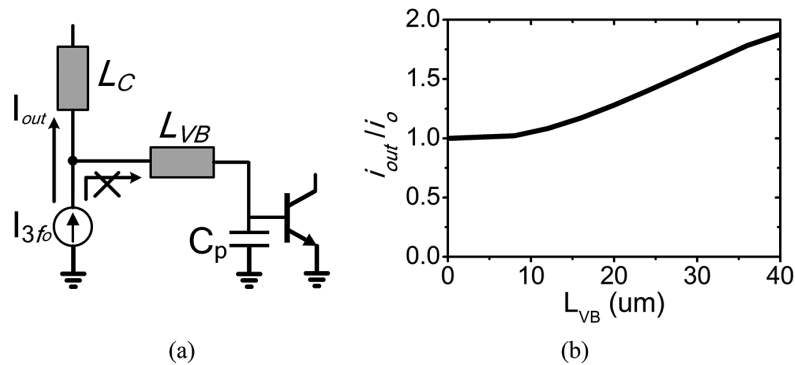

Fig. 9. (a) The 3rd-harmonic power enhancement by using L_{VB} to partially resonate with C_p. (b) The simulation of the normalized 3rd-harmonic current flowing to the load versus the length of the t-line L_{VB}.

I_{out}. The plot shown in Fig. 9(b) is the current I_{out} normalized to I_o (the current flowing to the load without L_{VB}). As L_{VB} increases to 40 μm, I_{out} is improved by as much as 1.9 times.

B. Three-Phase Injection Locked Divider ($\div 4$)

Shown in Fig. 10 is the conceptual loop of the proposed injection locked divider. Each stage is composed of an amplifier, a mixer, and a low-pass filter (LPF). The free-running frequency of the loop is designed close to $1/4 f_o$, and each stage contributes

120° phase-difference between its input and output. The three 3rd-harmonic signals ($3/4 f_o$) generated from the amplifiers are all naturally in-phase. The input three-phase signals coming from the VCO's three-phase output are mixed with $3/4 f_o$ signals. The mixers' outputs ($1/4 f_0, 1/4 f_0 \angle 120°, 1/4 f_0 \angle 240°$) are injected back to the loop and are added constructively with the loop's signal. In the steady-state, the loop is locked to the injected signals and divide-by-4 operation is performed. The same conceptual loop can readily perform divide-by-5
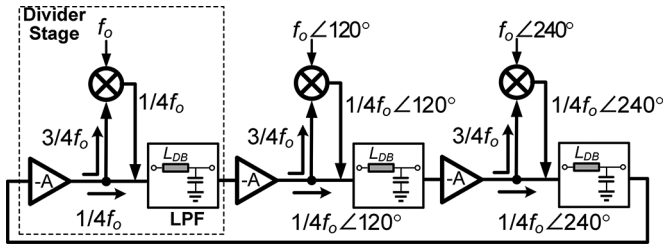
Fig. 10. The conceptual loop of the proposed three-phase injection locked divider (divide-by-4).
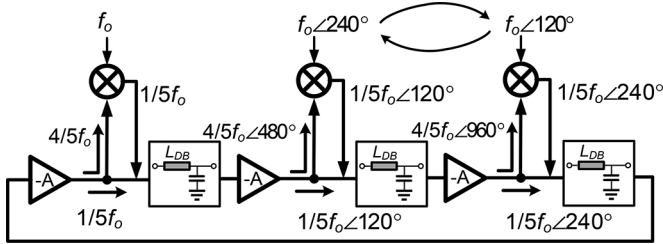

Fig. 11. By swapping the last input signals, the same conceptual loop performs divide-by-5.

by simply swapping the last two input signals, as depicted in Fig. 11. Assuming the free-running frequency of the loop is close to $1/5 f_o$, the three-phase input signals are mixed with the loop's 4th harmonic $(4/5 f_o)$. The loop will be locked to the mixer's output signals $(1/5 f_o, 1/5 f_0 \angle 120°, 1/5 f_0 \angle 240°)$.

Compared with the single injection, the multi-phase injection achieves wider locking range and requires lower input power. For a general case of N-stage divider with M-phase injection, in the phasor domain, each injection current, I_{in}, introduces a phase change ϕ to the loop signal (I_{osc}), and each LPF needs to compensate for a phase change θ in order to satisfy Barkhausen criteria. The phase change θ of each LPF is expressed as

$$\theta = \frac{M}{N}\phi. \tag{5}$$

If I_{in} is much smaller than I_{osc}, the normalized single-side locking range is then expressed as [32]:

$$\frac{\Delta f}{f_a} \leq \frac{M}{N} \cdot \frac{1 + \tan^2 \frac{\pi}{N}}{\tan \frac{\pi}{N}} \cdot \left| \frac{I_{in}}{I_{osc}} \right| \tag{6}$$

where f_a is the free-running frequency of the N-stage divider. From (6), it is seen that (a) the locking range is proportional to the number of injected phases (M); (b) under the same locking range, the injection current I_{in} is lowered by M times; (c) with higher mixer's efficiency, the injection current is increased, resulting in wider locking range. Fig. 12 demonstrates the special case when $N = M = 3$. With three-phase injections, the phase change (θ) of each LPF is equal to the phase change (ϕ) introduced by the injection current. The overall phase shift of each LPF thus becomes $-\pi/3 + \phi$.

Fig. 13 shows the circuit implementation of the proposed divider. The amplifying stages $(T_{a2} \sim T_{c2})$ with the t-lines of L_{DM} and L_{DB} form the divider's three-stage ring and transistors $T_{a1} \sim T_{c1}$ act as the three mixing cells. The three-phase input signals are fed to the base terminals of the mixing cells, and mixed with the loop's 3rd-harmonic signals. The mixer's
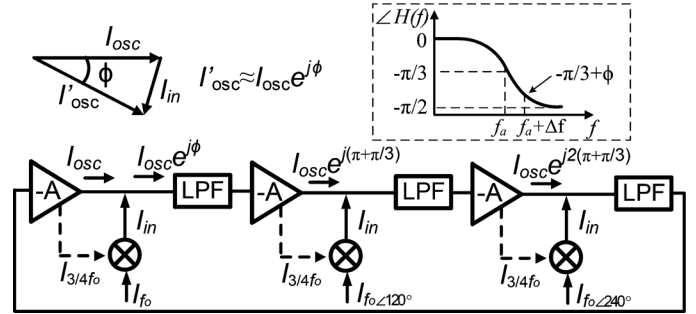

Fig. 12. The three-stage divider with three-phase injection $(N = M = 3)$, where the phase change of each LPF is equal to the phase change ϕ introduced by the injection current I_{in}.
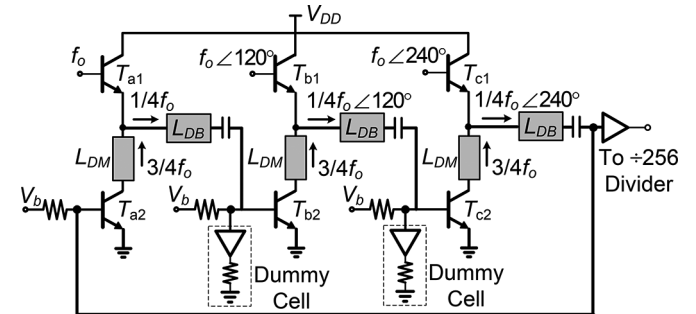

Fig. 13. The schematic of the proposed three-phase injection locked divider $(\div 4)$.

outputs $(1/4 f_0, 1/4 f_0 \angle 120°, 1/4 f_0 \angle 240°)$ flow back to the loop at three injection points. Similar to the VCO in Fig. 6, with the aid of the L_{DB} to block the loop's 3rd-harmonics $(3/4 f_o)$ from flowing to the next stage, the mixing efficiency is improved and thus further increases the locking range. A buffer is used to feed the divider's output $1/4 f_o$ to the rest of the divider chain $(\div 256)$ and two dummy buffers are added to provide symmetric parasitic loading to other stages

C. Integration and Layout of VCO and Divider

At high frequencies, any interconnect or cross-over introduces parasitics that cause severe signal distortion. This distortion will adversely affect the performance of the synthesizer's VCO and divider such as phase-noise, output power, and input sensitivity. The structural similarity of the proposed VCO and the three-phase injection divider helps us co-design/co-optimize these blocks and develop a compact layout. Shown in Fig. 14 is the integration of the VCO and the divider within the synthesizer, where the inner blue circle indicates the VCO ring. The VCO's f_o travels along the inner blue ring and its 3rd-harmonic signals are collected coherently at the center's $3f_o$ pad. The t-line's length realizing L_C determines the perimeter of the VCO ring and the length of L_{VB}. The t-line L_{VB}, used to introduce 10° phase shift for transistor optimum condition, forms the ring's perimeter. By narrowing L_C and widening L_{VB} to proper values, the L_{VB}'s t-line is fitted into the VCO ring. Three CAVs are placed in the layout with respect to divider's three-phase inputs such that no extra t-line or signal cross-over is required. The outer rectangle realizes the divider's loop, which is locked to the VCO ring and performs divide-by-4. The divider's output
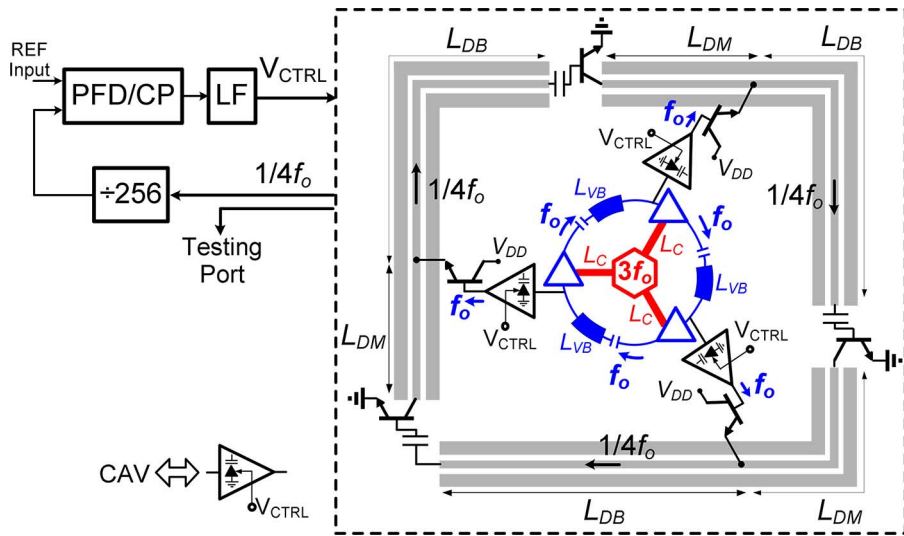
Fig. 14. The integration of the proposed VCO and divider within the synthesizer where the inner blue circle and outer rectangle indicate the VCO's and the divider's three-stage rings, respectively.
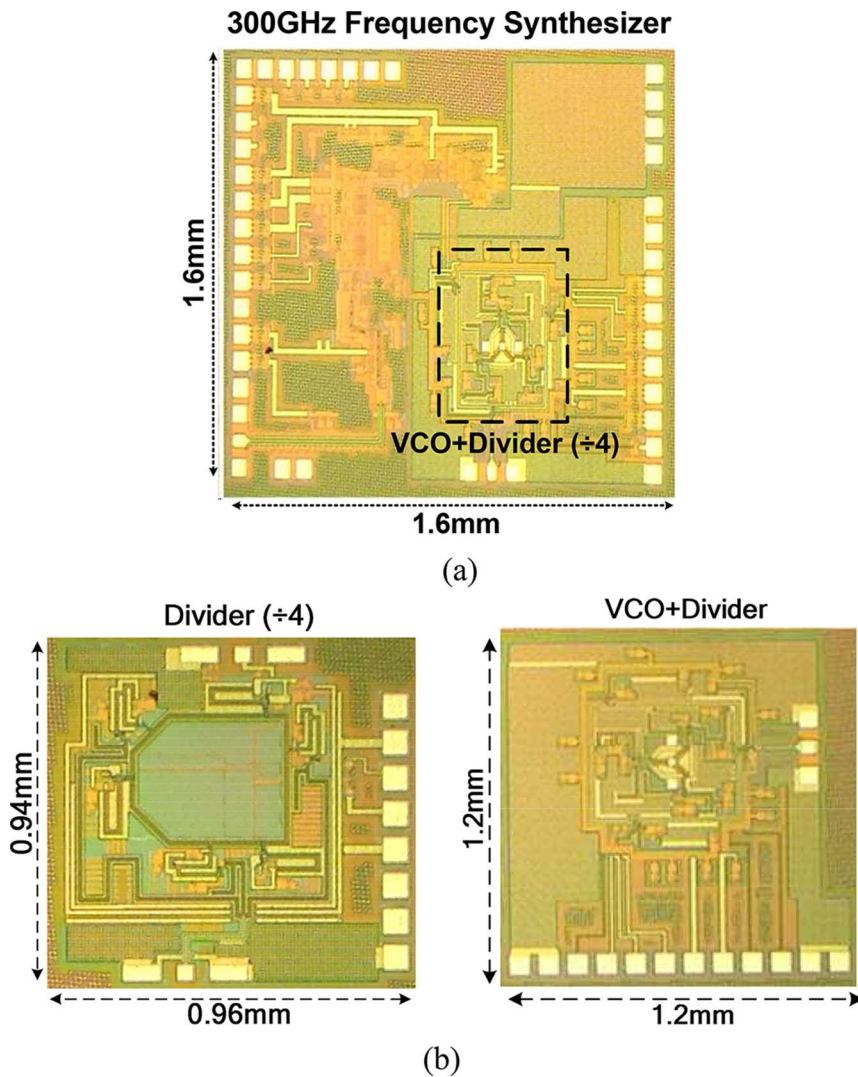

Fig. 15. The die micrographs of (a) the proposed 300 GHz frequency synthesizer, and (b) the stand-alone divider ($\div 4$) and the VCO+divider.
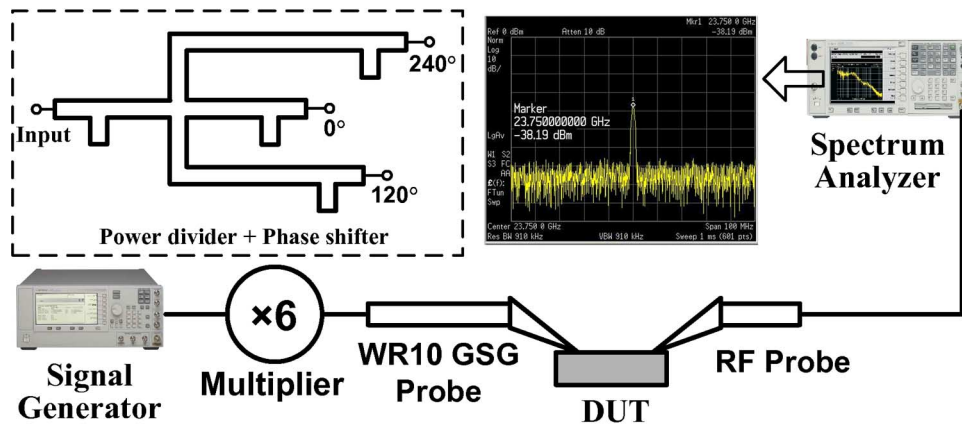
Fig. 16.   The stand-alone divider measurement setup.

$1/4f_o$ is then fed to the synthesizer divide-by-256 and forms a closed-loop through PFD/CP and LF. Two testing ports ($3f_o$ and $1/4f_o$) are used to measure the synthesizer's output spectra and its locking behavior. From a practical perspective, since the 300 GHz output pad is located at the center of the VCO ring, magnetic radiation can be used to radiate out the synthesizer's 300 GHz output signal.

IV. MEASUREMENT RESULTS

Three individual circuits including a divider, a VCO+divider and a 300 GHz frequency synthesizer were fabricated in 90 nm SiGe BiCMOS with six metal layers and f_T/f_{MAX} of 260 GHz/315 GHz. Their die micrographs are shown in Fig. 15(a) and (b). The synthesizer chip area is 1.6×1.6 mm^2 including DC and RF pads. All the t-lines were implemented using coplanar waveguides (CPWs) with a 2.8 μm thick-top-metal (M6) as the signal line and M3 as the shielding ground. With such the design, M1 and M2 can be used as DC power connection under the t-lines. The CPWs and the interconnection lines were carefully characterized using planar 3-D electromagnetic simulations.

In order to generate a three-phase signal for measuring the divider's input sensitivity, an on-chip three-way power divider and two on-chip phase shifters were used to provide input to the stand-alone divider. In the divider measurement setup shown in Fig. 16, an external W-band signal from a multiplier ($\times 6$) was applied to the divider input using a WR-10 GSG waveguide probe, and the divider output was connected to the spectrum analyzer (SA). With the measured divider's output spectrum and the input frequency, the divider's locking to the input signal was verified. By sweeping the input frequency and power, the divider's input sensitivity was measured. Fig. 17 shows the plot of the input sensitivity versus input frequency for two bias settings (Vb = 1.35 V and Vb = 1.48 V). With the two bias settings, the measured overall locking range is 91.9–101.8 GHz and the divider's average DC power consumption is 48.4 mW. At Vb = 1.35 V, the divider's free-running frequency is 99.5 GHz. At the higher bias voltage (i.e., Vb = 1.48 V), the free-running frequency decreases to 95.5 GHz due to the larger C_π's of the divider's amplifying transistors. Moreover, under this bias condition the amplifying transistors generate smaller 3rd-harmonic signals, results in locking-range degradation.
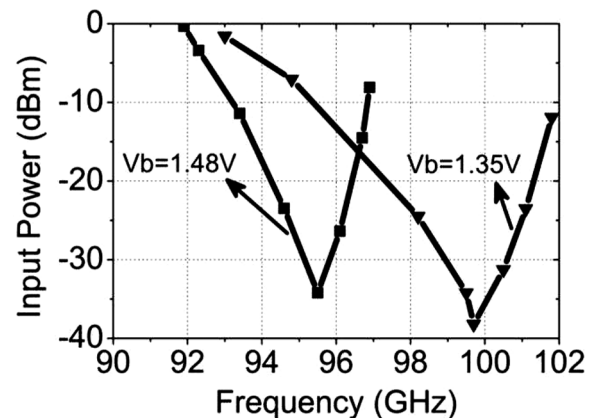

Fig. 17.   The measured divider's input sensitivity with two bias settings.

The VCO+divider chip was used to measure the VCO free-running performance and verify the divider's functionality with its input fed by the VCO. Fig. 18 shows the measurement setup. For the VCO's output power measurement, the VCO output was connected to a WR-3 waveguide GSG probe followed by the calorimetry power sensor. The waveguide taper was used to transform waveguide interface from WR-3 to WR-10. The measured power was calibrated by the loss of the signal path including the probe and the taper. For the VCO's oscillation frequency and tuning range measurement, the VCO's output signal was down-converted to the SA by using the harmonic mixer. Meanwhile with the divider's measured output spectrum, the divider locking characteristic was validated over the whole VCO tuning range. Since the divider is locked to the VCO and the conversion loss of the harmonic mixer is high (>70 dB), the VCO phase-noise is measured at the divider output. This phase-noise measurement is close to the direct measurement of the VCO's output. This is because the output phase-noise profile of an injection locked divider is similar to a first-order PLL, where the input noise is low-pass-filtered while the divider noise is high-pass-filtered and is thus negligible [33].

Shown in Fig. 19 is the VCO's oscillation frequency and output power where the solid and hollow symbols represent the measurement and simulation results, respectively. The measured oscillation frequency varies from 280 to 303.36 GHz (i.e.,
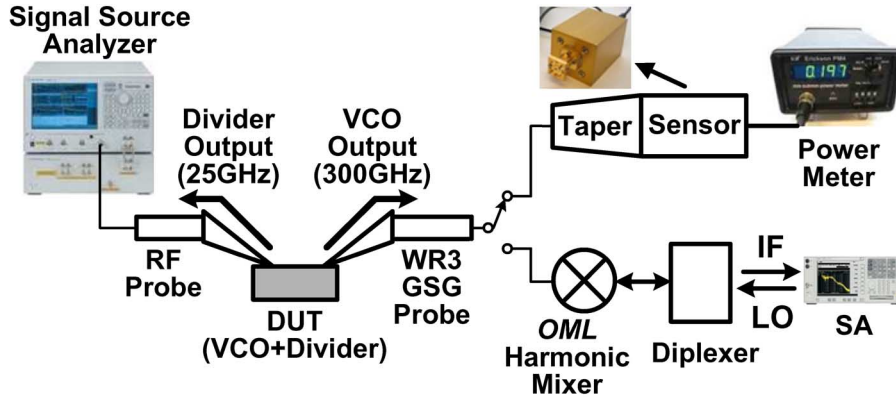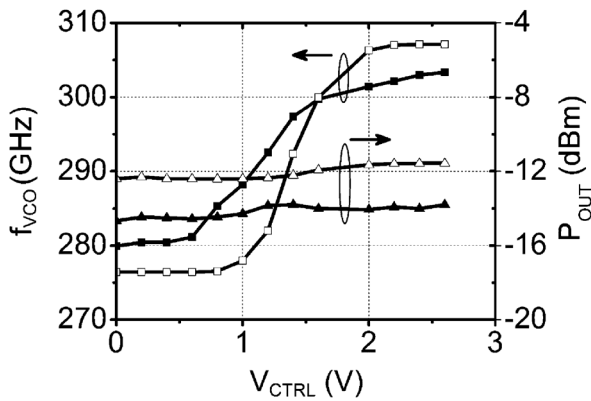
Fig. 18. The VCO+divider measurement setup.

Fig. 19. The VCO's oscillation frequency and output power versus V_{CTRL}, where the solid and hollow symbols represent the measurement and simulation results, respectively.
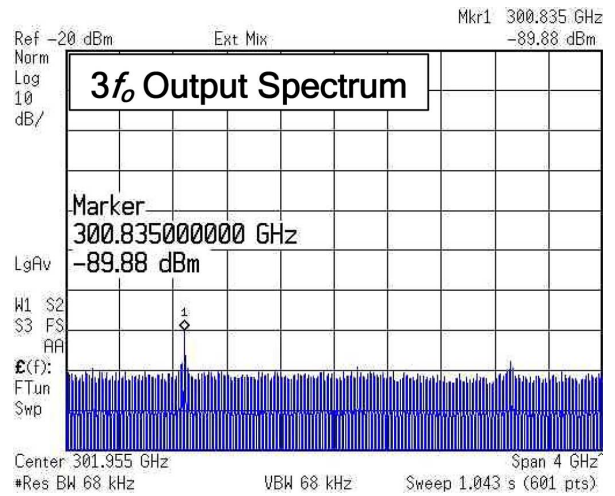

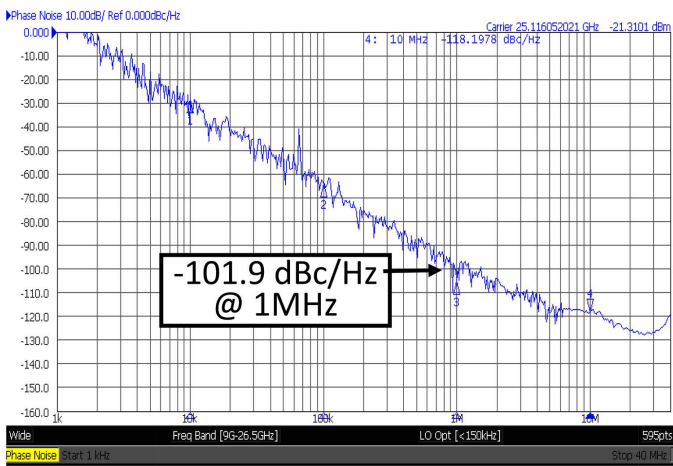Fig. 21. The measured synthesizer's output spectrum.

Fig. 20. The measured phase-noise profile at the divider's output where the input VCO frequency is 100.4 GHz.

8% of tuning range) with V_{CTRL} varying from 0 to 2.6 V. The measured output power is -14 dBm with less than 0.5 dB variation. Fig. 20 shows the measured phase-noise profile at the divider's output where the input VCO frequency is 100.4 GHz.

The phase-noise at 1 MHz offset is -101.9 dBc/Hz, and the corresponding VCO phase-noise is -80.3 dBc/Hz (with a factor of $20 \log_{10} 12$). The VCO's DC power consumption is 105.6 mW.

The synthesizer measurement setup is similar to that of the VCO where the synthesizer's $3f_o$ output was down-converted to the SA and its $1/4f_o$ was connected to the signal source analyzer. The synthesizer input was fed using a crystal oscillator or a signal generator (SG) for measuring the synthesizer's locking range. The measured synthesizer's output spectrum was shown in Fig. 21 when the synthesizer was locked at 300.8 GHz. Fig. 22 shows the measured phase-noise profile at the $1/4f_o$ output port when the synthesizer was locked to a 95 MHz reference feeding by the SG. The profile depicts a closed-loop locking behavior, in which the frequency response for input noise is low-pass filtered and VCO noise is high-pass filtered. The synthesizer's locking range was measured by sweeping the input frequency from the SG and measuring the output spectra. Shown in Fig. 23 is the measurement of the synthesizer's scale-up phase-noise versus its output frequency. The locking range varies from 280 to 303 GHz which closely follows the VCO's tuning range. The minimum phase-noise at 1 MHz offset is -75.4 dBc/Hz when the synthesizer's output frequency is 296 GHz. With the input signal

TABLE I
PERFORMANCE SUMMARY

| Three-Phase Injection-Locked Divider		Triple-Push VCO		300GHz Frequency Synthesizer	
Frequency (GHz)	93 ~ 101.8	Frequency (GHz)	280 ~ 303.36	Frequency (GHz)	280.32 ~ 303.36
Divider Ratio	4	Tuning Range	8%	Divider ratio	1024
Locking Range	10.2%	Output Power	−14 dBm	Locking Range	7.9%
Input Power	< 0 dBm	PN @ 1MHz offset (dBc/Hz)	−80.28*	PN @ 100kHz offset (dBc/Hz)	−77.8 @ 294.9GHz*
Supply (V)	2	Supply (V)	1.8	PN @ 1MHz offset (dBc/Hz)	−82.5 @ 294.9GHz
DC Power	48.4 mW	DC Power	105.6 mW	DC Power	376 mW

*Scaled-up phase noise at 300 GHz
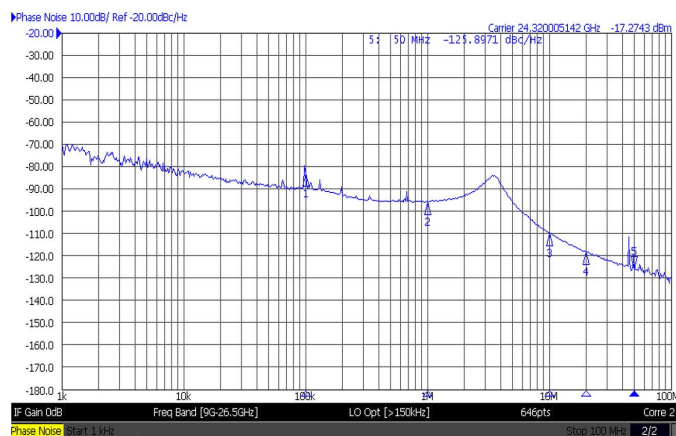
Fig. 22. The measured phase noise profile at the synthesizer's $1/4f_o$ output when the synthesizer was locked to a 95 MHz reference feeding by the SG.

Fig. 23. The measurement of the synthesizer's scale-up phase-noise versus its output frequency with the synthesizer's input reference from a SG and a crystal oscillator.
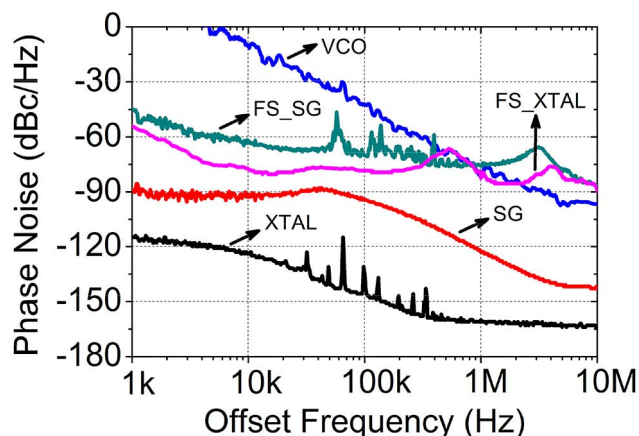
Fig. 24. The measured phase noise profiles of the synthesizer, the VCO and the input reference.

fed from a 96 MHz crystal oscillator (i.e., the synthesizer's output frequency is 294.9 GHz), the measured phase-noise is −82.5 dBc/Hz (−89.6 dBc/Hz) at 1 MHz (10 MHz) offset. Fig. 24 shows the measured phase-noise profiles at 294.9 GHz for the free-running VCO, the synthesizer with its input from the SG (labeled as FS_SG) and from the crystal oscillator (labeled as FS_XTAL), input signal from the SG (labeled as SG) and from the crystal oscillator (labeled as XTAL). In a comparison between the two plots of FS_SG and FS_XTAL the in-band phase-noise follows the input noise, and thus a better input signal results in a lower phase-noise. Note that one of the important advantages using a synthesizer over a VCO is that, because of the closed-loop locking behavior, the phase-noise within the synthesizer's loop bandwidth is significantly reduced (e.g., −45 dBc/Hz and −77.8 dBc/Hz at 100 kHz offset for the VCO and the synthesizer, respectively). Table I shows the measured performance summaries of the proposed divider, VCO, and synthesizer.

Tables II and III provide the performance comparison with the prior work for the VCO and the 300 GHz synthesizer, respectively. In the VCO's comparison table, the proposed VCO
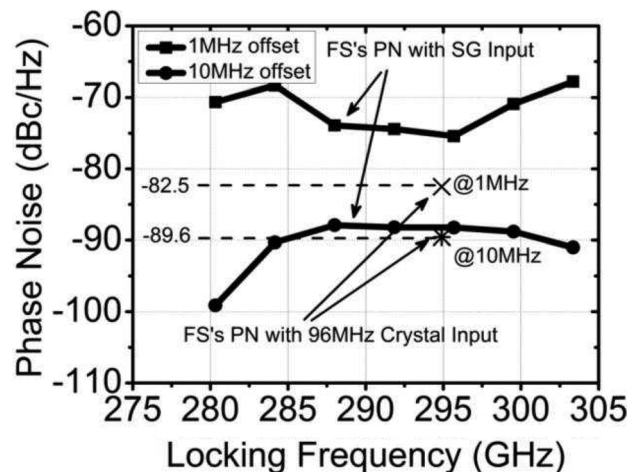
demonstrates the widest tuning range with similar FOM_T to [17] and [34] (42 dB better than [18]). Note that for the oscillators reported in [34], the frequency tuning is achieved by

TABLE II
VCO COMPARISON

	This work	[17]	[18]	[34]
Frequency (GHz)	290	290	324	288
Tuning Range (%)	8	4.5	1.2	1.4*
PN @ 1MHz offset (dBc/Hz)	−80.28	−78	−78	−87
Output Power (dBm)	−14	−1.2	−46	−1.5
DC Power (mW)	105.6	325	12	275
FOM$_T$	−153.4	−154	−111.4	−153.2
Technology	90nm SiGe BiCMOS	65nm CMOS	90nm CMOS	65nm CMOS

*Tuning by changing supply voltage.

$$**FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{FTR}{10}\right) + 10\log\left(\frac{P_{DISS}}{1mW}\right) - P_{out}$$

TABLE III
SYNTHESIZER COMPARISON

	This work	[23]	[22]
Frequency (GHz)	280.32 ~ 303.36 (3rd)	300.76 ~ 301.12 (fund.)	160 ~ 169 (2nd)
Divider ratio	1024	10	128
Locking Range	7.9%	0.12%	5.5%
PN @ 100kHz/1MHz offset (dBc/Hz)	−77.8 / −82.5	−78 / −85	−75 / −78
DC Power (P$_D$)	376 mW	301.6 mW	1250 mW
FOM$_T$* @ 100kHz/1MHz offset	−179.4 / −163.9 dBc/Hz	−144.4 / −131.4 dBc/Hz	−163.1 / −146.1 dBc/Hz
Technology (f$_{max}$)	90nm SiGe BiCMOS (315 GHz)	InP HBT (800 GHz)	130nm SiGe BiCMOS (280 GHz)

$$*FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{Locking\ Range}{10}\right) + 10\log\left(\frac{P_D}{1mW}\right)$$

changing the supply voltage, and thus suffer from considerable output power variation.

In the synthesizer comparison table, [23] reports the highest synthesizer in III-IV technology with an f_{MAX} of 800 GHz, and [22] presents the highest in silicon using a similar technology to our work. Our synthesizer demonstrates higher operation frequency and divider ratio, wider locking range (60 times wider than that in [23]), and comparable phase-noise. The use of a crystal oscillator instead of an SG makes our synthesizer a practical and complete system. The proposed synthesizer achieves a 20 dB better figure-of-merit (FOM$_T$) among the other work.

V. CONCLUSION

A fully integrated THz frequency synthesizer including a triple-push VCO with Colpitts-based active varactor (CAV) and a three-phase injection locked divider was implemented in 90 nm SiGe BiCMOS. By using the VCO's 3rd-order harmonic as the output signal and injecting its fundamental to the divider chain, the synthesizer's operation frequency was designed to become close to the transistor f_{MAX} while relaxing the divider's operation frequency. Meanwhile, the three-phase injection improved the divider's locking range to cover the VCO's tuning range. The proposed synthesizer thus achieved a wide locking range which follows the VCO's tuning range. The proposed CAV provided frequency tunability and varactor isolation to the VCO, and acted as a buffer between the VCO and the divider. In addition to the similar structure of the VCO and the divider, an efficient circuit co-design and compact layout was achieved. To the best of our knowledge, this work reports the highest frequency synthesizer in silicon and is capable of using a crystal oscillator as the input.

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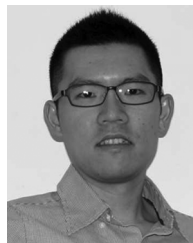
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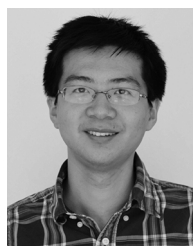
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