

# UCLA

## UCLA Previously Published Works

### Title

Can RF help CMOS processors?

### Permalink

<https://escholarship.org/uc/item/4rv764dv>

### Journal

IEEE Communications Magazine, 45(8)

### ISSN

0163-6804

### Authors

Socher, Eran  
Chang, Mau-Chung Frank

### Publication Date

2007-08-01

Peer reviewed

# Can RF Help CMOS Processors?

*Eran Socher and Mau-Chung Frank Chang, University of California, Los Angeles*

## ABSTRACT

Digital circuits implemented in CMOS technology have been the workhorses of high performance computer processors for more than a decade, following Moore's law with exponentially increasing integration and performance. Driven by lower cost, increasing performance, and mixed-signal benefits, CMOS technology also has found increasing use in analog, and more recently, RF applications. Now, with transistor performance still improving, wires are becoming the limiting factor for speed and performance by imposing limits on communication bandwidth and latency between processing cores and memories, both off- and on-chip. Communication and circuit techniques, developed mainly for narrow band-wireless RF communication can help increase the wired communication speed in digital systems. This approach, dubbed RF Interconnect (RF-I), picks up speed for on-board and on-chip applications, changing the communication paradigm from the old parallel unidirectional time-shared bus to new transmission lines enabling reconfigurable communication using both frequency and code division multiple access techniques.

## ADVANTAGES OF CMOS FOR DIGITAL CIRCUITS

Complementary metal-oxide semiconductor (CMOS) technology has reigned as the leading fabrication technology for very-large-scale integration (VLSI) digital circuits and systems for the last 20 years [1]. The main advantage of this technology for digital circuits compared with n-type metal-oxide-semiconductor (NMOS) and bipolar technologies is the dramatic reduction of static power consumption. The ability to use NMOS and positive channel metal oxide semiconductor (PMOS) transistors in the same integrated circuit enables basic digital circuits to either charge or discharge the capacitive output load using the same input signals, consuming energy only when changing the output value. Using the transistor gate as circuit input makes the input impedance predominately capacitive, thus making the problem of cascading circuits simple and increasing the available fan-out.

Use of both types of transistors (NMOS and PMOS) in conjunction makes the logic-voltage levels independent of transistor size, and control of the PMOS-to-NMOS size ratio enables construction of symmetrical logic gates in terms of transition from low to high and back. These traits make

even complicated digital circuits easier to design in CMOS technology through the use of hierarchy and simplified circuit modeling. Digital circuits and systems are thus designed using high-level languages to describe the logic and automated tools to synthesize the resulting circuits and layout using standard building blocks [1]. The relative ease with which CMOS circuits can be interfaced enables modular design, where the digital system is divided into functional blocks that can be designed separately using relatively simple input/output constraints. Using this "divide and conquer" approach, VLSI digital designs with hundreds of millions of transistors have been implemented [1].

## SCALING AND MOORE'S LAW

CMOS digital circuits can benefit tremendously by scaling down transistor dimensions. The delay of a logic gate is proportional to its load capacitance and inversely proportional to the charge/discharge transistor current. A major contribution to the load capacitance is the gate capacitance of the following stage, which is proportional to the transistor channel length  $L$ . Using simplified transistor models, transistor current can be shown to be inversely proportional to  $L$ . Reducing  $L$  can therefore decrease the delay of CMOS digital circuits [1]. Defined in 1965, Moore's law set a course for the VLSI industry of exponential improvement in performance. Much of that performance improvement was achieved through scaling laws [2] that set a relation between transistor parameters while shrinking their dimensions.

The relation between shrinking transistor dimensions and logic gate delay has an enormous effect on overall processing performance. Reducing the size of transistors enables the integration of more circuits on the same chip area, which increases the number of operations done each clock cycle within that chip area. The reduction in gate delay enables an increase in clock frequency, which further increases the number of operations completed per second. In addition, even with increasing total fabrication costs, scaling the dimensions of transistors decreases the cost per transistor and the cost of computing, making the trend worthwhile.

## THE BOTTLENECKS OF SCALING

Scaling laws generally apply to transistors and the basic logic circuits in which they are used. The overall digital system constitutes more phys-

ical elements, mainly interconnects, as well as different technologies. As a result, while CMOS transistors continue to shrink in size and improve their performance in terms of speed, the system performance is limited by other (primarily external) circuit components, the connectivity between circuits, and other figures of merit such as power consumption.

One bottleneck is the available data rate of off-chip printed circuit board (PCB) lines. At low frequencies, both the inductance and resistance of the wire can be neglected, and only its capacitance must be considered. If the output buffer is large enough, it has enough current to charge and discharge the wire-load capacitance in the allotted symbol time. As frequencies (data rates) increase, the symbol time decreases, and the wire resistance makes it difficult to charge and discharge the whole wire within the symbol time, resulting in reduced voltage swing or signal loss. As frequencies further increase, inductance becomes significant, making the wire a lossy transmission line requiring termination to avoid reflections that further degrade the signal. These practical considerations limit the achievable data rates on the PCB to approximately 1 Gb/s per line, unless sophisticated equalization techniques are used [3]. Hence, although processor cores can work at clock frequencies as high as 4 GHz, the data rate with which they can send and receive data on board is much lower.

The bottleneck becomes even narrower when a shared bus is considered. Traditionally, processor cores communicate with the dynamic random access memory (DRAM) through an on-board bus, which is also called the front side bus (FSB). Due to reflections and losses on the bus line, the achievable data rate does not exceed 1 Gb/s for each bus line, which is less than the achievable clock rates of processor cores (currently 2–4GHz). The effectiveness of processor to memory communication is even more limited due to the fact that only one of the cores can communicate with the DRAM at the same time. As a result, the latency of data transmission can be high and is expected to increase as the number of processor cores increases [4].

Since scaling decreased the delay of basic digital circuits in CMOS, it enabled the increase of processor frequency and the integration of more transistors on the same die area. However, dynamic power consumption of digital circuits is proportional to their switching frequency, so power and its density per unit area also increased to the point where a further increase in frequency would be detrimental due to thermal effects adversely affecting performance and reliability. Power is also proportional to the square of the supply voltage that has been decreasing with scaling, but not fast enough. Power also may increase due to its proportionality to the total load capacitance of digital circuits, which also tends to increase with scaling due to the higher level of integration achieved on the chip area. Thus, power consumption is also a bottleneck in processor performance under scaling.

Although scaling benefits the speed of the CMOS transistor itself, it does not have the same effect on the wires connecting the transistors together. Hence, the wires connecting the

transistors become more important in determining the delay of circuits [5]. Wires add to the total delay due to their non-negligible resistance and capacitance. The resistance of wires increases with scaling mainly because the width of the wires decreases. The capacitance of the wires does not change much with scaling because the reduction in width is somewhat compensated by the reduction in wire spacing. As a result, the resistive capacitive (RC) delay of wires is actually increasing with scaling, making it more dominant from one technology node to the next. Process improvements such as using copper instead of aluminum and low-K dielectrics help reduce wire delay but do not stop the continuing trend.

When discussing wire delay, a distinction should be made between local wires and global wires. Since the die size does not change much between technology nodes, global wires have similar length and therefore increase their delay with scaling. Local wires, however, reduce their length with scaling and therefore scale their delay as well. As a result, scaling down the dimension of the same circuit along with its local wires would scale its delay, but global communication across the chip would have increased delay with scaling and would serve as a bottleneck to overall speed.

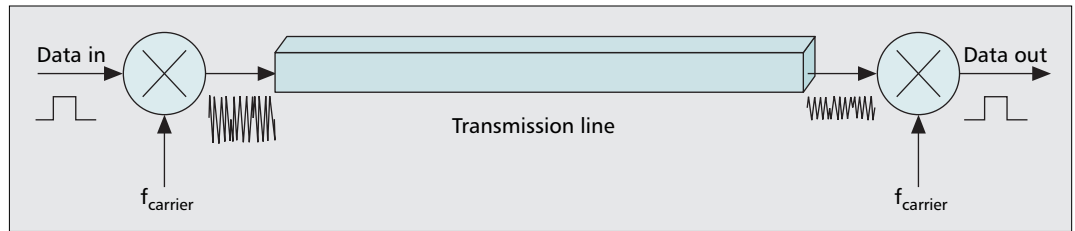
Since achieving better performance by increasing clock frequency is no longer a viable option primarily due to constraints in power consumption, the current trend in microprocessor architecture design is to achieve better performance using parallelism [6]. Instead of using one processing core with higher frequency, more cores can be integrated on the same chip (or the same package) with the same total area (thanks to scaling down transistor dimensions), each operating at a reasonable frequency in terms of power consumption. If each core is scaled down in dimensions, the area it consumes also is scaled down, and its local wires are not a bottleneck to its performance. However, communication between distant cores on chip and to peripheral components, such as the memory, is limited in bandwidth and latency due to on-chip and off-chip interconnect limitations. As a result, interconnects become the bottleneck for performance in current and future microprocessors. To further enable performance increase, the communication latency and data rate must be improved for both on-chip and off-chip links.

## RF INTERCONNECT CONCEPT

An alternative to voltage or current signaling is signaling using modulation of electromagnetic waves. The wave, typically at radio or millimeter-wave frequency can be transmitted along a transmission line at the effective speed of light. Then, digital data can be used to modulate the amplitude and the phase of the carrier wave, similar to the way it is done in wireless communication. At the receiver end, demodulation is used to retrieve the digital information that was sent. The concept is illustrated in Fig. 1, where mixers are used to modulate the carrier with the digital data using binary phase shift keying (BPSK).

*Since achieving better performance by increasing clock frequency is no longer a viable option primarily due to constraints in power consumption, the current trend in microprocessor architecture design is to achieve better performance using parallelism.*

Transmission across longer links does not necessarily mean more power consumption, as long as the signal at the receiving end is large enough compared with noise and interference; energy-wise this also makes it an effective method of data transmission for longer distances and higher data rates.



■ **Figure 1.** RF interconnect concept.

Sending information by modulating a carrier at higher frequency has an advantage due to the non-ideal nature of the wire. Random un-modulated digital signals have most of their energy in frequencies from DC up to twice the maximum data rate. Since wires are dominated by RC behavior at low frequencies, the response of the wire to each frequency is different, generally with increasing attenuation and phase lag for higher frequencies. This means that the voltage swing and delay are different for slow and fast changing signals. As a result, the output signals suffer more from inter-symbol interference (ISI) as data rates increase.

In contrast, when a high frequency carrier is used, the wire inductance dominates over the resistance that allows propagation of waves in the transmission line. For the wave propagation characteristics to be controlled, the current return path must be well defined using common transmission line structures such as a microstrip or a coplanar waveguide. Close to the carrier frequency, signal loss does not change much with frequency, and wave velocity hardly changes at all. Thus, using modulation of a high frequency carrier wave makes the frequency dispersion less influential to signal integrity, even at high data rates, because the bandwidth-to-center frequency ratio is relatively small. As a result, the probability of ISI is greatly reduced even at high data rates.

Another advantage of modulation is the reduced latency. When using voltage signaling without modulation, the latency or delay is dominated by the RC constant of the wire, because the full capacitance of the wire must be charged and discharged through the wire resistance or the data would be distorted. Even though the output signal would start changing at light speed, a time on the order of RC is required to make a significant voltage change compared with the input voltage swing. This RC latency grows approximately quadratically with the wire length [1], making it significant for off-chip wires. Inserting repeaters optimally along on-chip wires can make the latency linear with the total length but still results in a large delay. Using repeaters with off-chip wires usually is not practical. Using transmission lines to send information modulated on high frequency carrier waves enables smaller latencies because the velocity at which the wave propagates is the effective speed of light in the material. This velocity is typically two to three times smaller than the free-space speed of light, depending on the dielectric constant around the transmission line. The attenuation of the signal increases with the resistance of the wire, but the speed at which it propagates hardly changes.

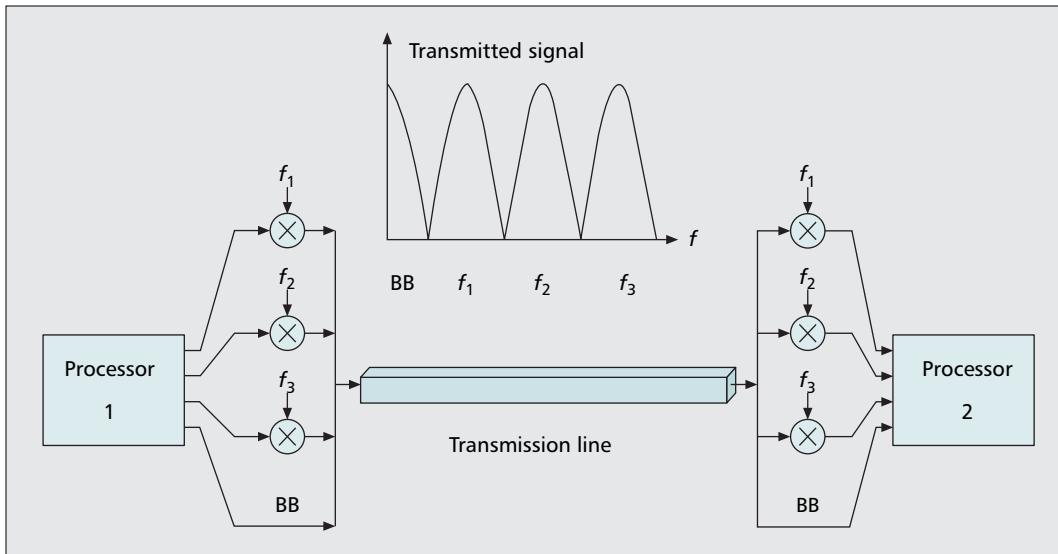
It also is important to look at the energy and power consumed using RF-I compared with traditional voltage signaling because increased power consumption in CMOS processors was one of the primary drivers for its consideration in the first place. In voltage signaling, energy is consumed when charging and discharging the wire capacitance. As a result, the energy consumption increases with wire length and spacing scaling, and the power increases with the data rate. Using electromagnetic (EM) waves to carry information requires power to drive the transmission line, but the effective energy consumption per bit would actually decrease with the data rate as more information is being sent for the same amount of transmission power. Transmission across longer links does not necessarily mean more power consumption, as long as the signal at the receiving end is large enough compared with noise and interference; energy-wise this also makes it an effective method of data transmission for longer distances and higher data rates.

## ENHANCING PERFORMANCE WITH FDMA

The modulation frequency of the carrier is limited by both the signal bandwidth-to-carrier frequency ratio and by the speed of the mixer. However, higher data rates can be achieved by using multiple carrier frequencies. In this approach, different carrier frequencies are modulated using different data streams, but all transmissions share the same transmission line. Using multiple carriers can increase the total data rate between two users or enable multiple users to use the same transmission line at the same time with wide bandwidth and very small interference. The approach is similar to frequency division multiple access (FDMA), which is widely used in wireless communication and benefits from the fact that in wired communication, there are no FCC limitations on the frequencies used (provided the radiation power leaking out does not exceed regulatory limits), so the total available bandwidth is very high.

The principle of operation is illustrated in Fig. 2 for data transmission between two processors. The frequency spectrum is divided into different bands, including the low frequency baseband (BB). In this example, four data streams are transmitted on the same transmission line using up-conversion to higher frequencies. This frequency multiplexing effectively increases the total data rate between two processors by a factor of four, using only one connecting wire.

Using more than two carrier frequencies enables multiple-user communication sharing the same transmission line, at the cost of more elaborate filtering and mixing. This enables the reduction of the number of wires on board and on chip.



■ **Figure 2.** Data rate enhancement using FDMA RF interconnect.

FDMA can offer simultaneous communication between more users using the same transmission line. Figure 3 shows an implemented system [7] that demonstrates that concept. In this system, four CMOS chips in a 0.18  $\mu\text{m}$  technology are connected to the same transmission line on a PCB using wire bonding of the chip pads. The transmission line is terminated on both ends to minimize reflections. All the chips are identical and contain a transmitter and a receiver for both baseband signals and for data up-converted to an RF frequency of 7.4 GHz. Selectivity between bands is achieved using bandpass or lowpass filtering. The RF carrier was modulated using BPSK. Using this scheme, simultaneous data rates of 2 Gb/s were achieved in both the baseband and the RF band.

One of the advantages, as can be seen in Fig. 3, of using FDMA is the ability to communicate bi-directionally on the same wire. Due to the separation of signals in frequency, there is no interference between signal waves traveling in opposite directions at the same time. Using more than two carrier frequencies enables multiple-user communication sharing the same transmission line, at the cost of more elaborate filtering and mixing. This enables the reduction of the number of wires on board and on chip.

Using more frequency bands on the same shared transmission line offers interesting opportunities in terms of re-configuration of the system as well. Traditional interconnects are fixed. They connect fixed points at a fixed available data rate. If a bus is used, only one transmission is possible at a time, again using the same available data rate. Realizing transceivers that can communicate at different carrier frequencies on the same transmission line enables control of the ports that are communicating and at what data rate. Assigning more frequency bands to one transmitter and one receiver would increase the aggregate data rate between the two. When the number of bands is smaller than the number of units, not every unit can send information simultaneously. However, if frequency bands can be assigned dynamically to different transmitters

and receivers, communication can be adjusted according to the current requirements of the system. Moreover, the same band that is assigned to one of the transmitters can be assigned to several receivers, thus distributing data in parallel to several (but not necessarily all) units, while other units are free to communicate using other frequency bands.

## EXPANDING OPTIONS USING CDMA

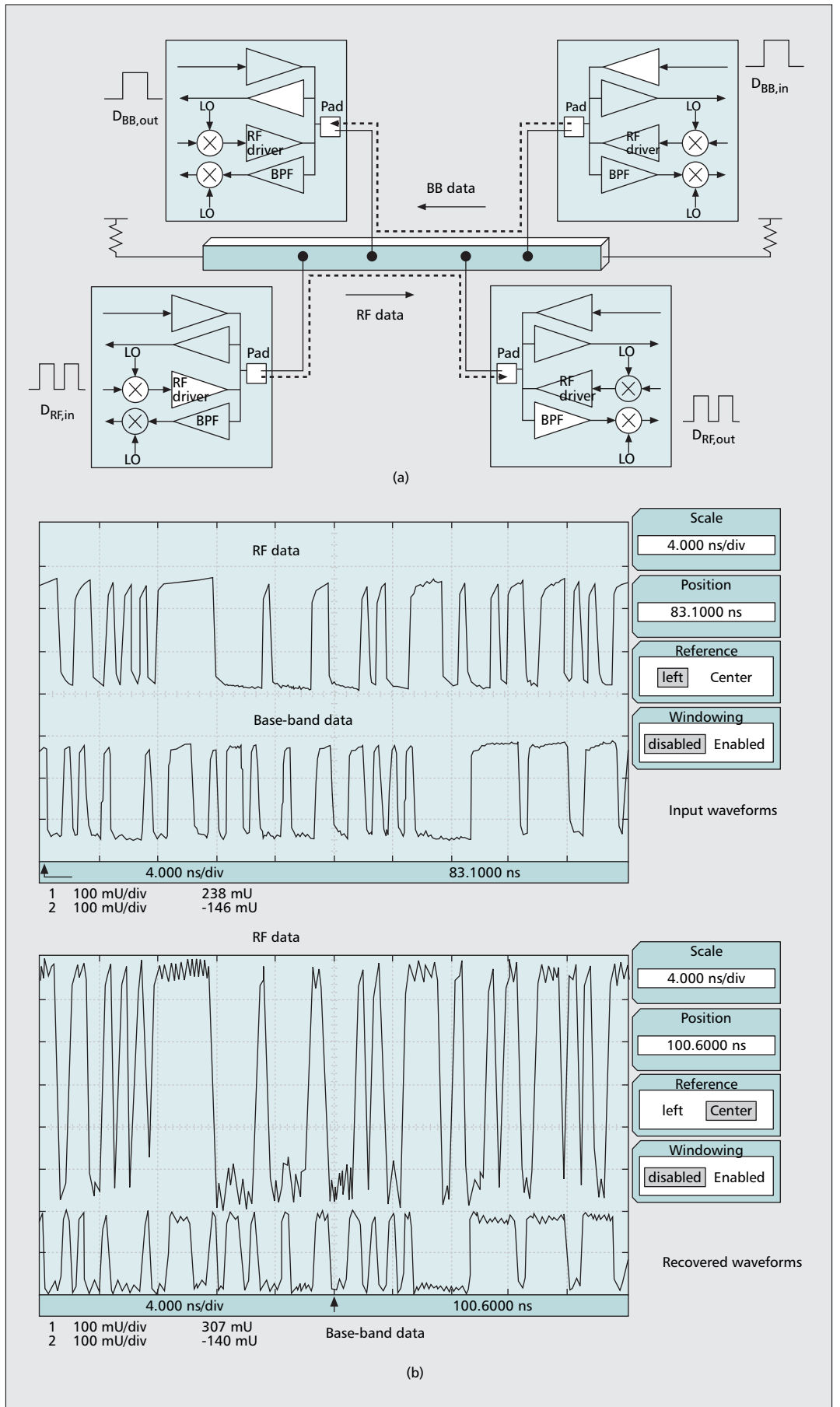
Another approach that increases versatility and concurrency is code division multiple access (CDMA) [8]. In this widely-used approach, multiple users use the same bandwidth at the same time, but their data is code-modulated using orthogonal codes so that each of them can be identified and its individual data extracted. Orthogonal codes can be obtained using either Walsh or pseudo noise (PN) codes.

Multiplexing information on a shared medium using Walsh codes is achieved on a transmission line in a similar way it is achieved in free space [8, 9]. As an example, if only two codes are used, two orthogonal Walsh codes are required to code two different bit streams by simple multiplication. The resulting coded streams are summed on the shared medium (e.g., a transmission line) creating a multilevel bit stream. The multilevel bit stream is then decoded at the receiver end into the original two streams using the same two codes for multiplication and summation. Because the codes are orthogonal, ideally there is no interference between the data streams.

The obvious advantage of using CDMA signaling compared with the traditional bus approach is latency. A traditional bus actually is based on time division multiple access (TDMA) interconnect, which means that the time the different units use the bus is divided between them. While one unit is sending information to another unit, no other transmission is possible, which results in long latencies for the other units that wait. Even more time is lost in the transition between transmissions. In CDMA, however,

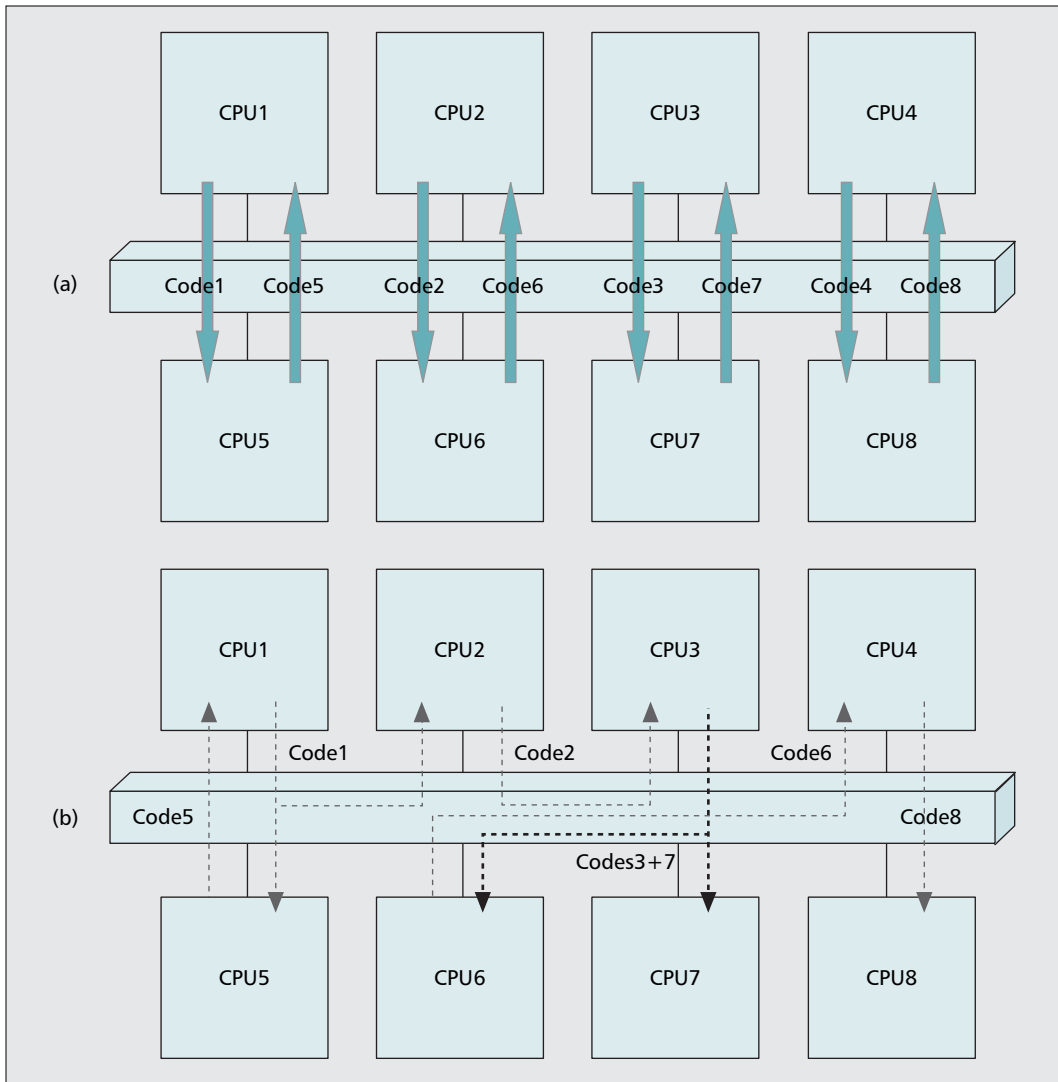


The obvious advantage of using CDMA signaling compared with the traditional bus approach is latency. A traditional bus actually is based on TDMA interconnect, which means that the time the different units use the bus is divided between them.



■ **Figure 3.** Four-chip implementation of FDMA interconnect onboard showing a) system schematics; b) measurement of 2 Gb/s bidirectional data transmission.

*In contrast to FDMA, where changing the carrier frequency of a transceiver requires more complicated and more challenging circuit design due to the high bandwidth involved, re-configuration of the codes used by CDMA transceivers is relatively easy and can be done in real-time operation.*



**Figure 4.** Reconfiguration of CDMA bus communication pattern from a) uniform to b) variable data rate.

transmissions are simultaneous so that there is no added latency due to *busy line* wait periods.

A CDMA bus also offers bi-directional communication at the same time, using the same wire. The use of two orthogonal codes enables transmission and reception using different codes, thus reducing the probability of interference between transmissions. Using more codes allows the connection of more than two transceivers using the same transmission line. Thus, concurrent communication between different processing units can exist without delays and dead time.

In contrast to FDMA, where changing the carrier frequency of a transceiver requires more complicated and more challenging circuit design due to the high bandwidth involved, re-configuration of the codes used by CDMA transceivers is relatively easy and can be done in real-time operation. Controlling the pattern of communication dynamically offers great advantages to a CDMA-based bus or network, because it can accommodate the changing requirements of communication in terms of allocating more or less bandwidth to communicating units. Hence, it may be possible to relieve congestion prob-

lems in the system, decrease latencies of transmissions, and improve overall system performance; especially when the system is communication-limited. Figure 4 illustrates an example where communication patterns can be re-configured dramatically. In this example, eight processing cores share a CDMA bus. A basic configuration (a), setting bi-directional communication between pairs of cores, is achieved by assigning different codes to each transmitter/receiver pair. Option (b) shows a more complicated pattern, where the transmitter of core 3 is assigned two codes for increased bandwidth, and the same codes are used in the receivers of cores 6 and 7 to enable both of them to receive this high bandwidth data. Other codes are assigned to enable communication between other pairs or trios of cores. Physical implementation of this type of information broadcasting requires careful design of the transmission line topology. This includes its termination and especially, the coupling elements connecting it to the different transceivers to accommodate power division between receivers and minimizing reflections that could contribute

to inter-symbol and inter-channel interference. CDMA can be used as a multiple access scheme at baseband (without modulating an RF carrier), achieving simultaneous communication between multiple units. Figure 5 shows a chip that uses CDMA modulation on a carrier frequency of 5 GHz [9]. One advantage of this approach is the smaller signal propagation latency (speed of light limited instead of RC). Another advantage is in the data rate. Because a

carrier frequency is used, frequency dispersion is less significant and higher modulation frequency can be used. Moreover, if more carrier frequencies are implemented, the aggregate data rate can be further increased using FDMA.

### 3D CHIPS OPEN NEW POSSIBILITIES

One of the current technological trends in CMOS processes is 3D stacking. In this trend, several thin tiers of transistors and wires are stacked vertically to achieve a higher level of integration. Due to vertical integration, the same functionality can be implemented in a smaller chip area, reducing both cost and the distance signals required to travel across the chip. Reduced distance decreases both transmission latency and the consumed energy. However, 3D stacking requires vertical connection between transistor and metal tiers, usually implemented using metal studs that cut through layers of silicon and insulators. Alignment of such direct connections is difficult on a large scale and therefore requires a relatively large connection area.

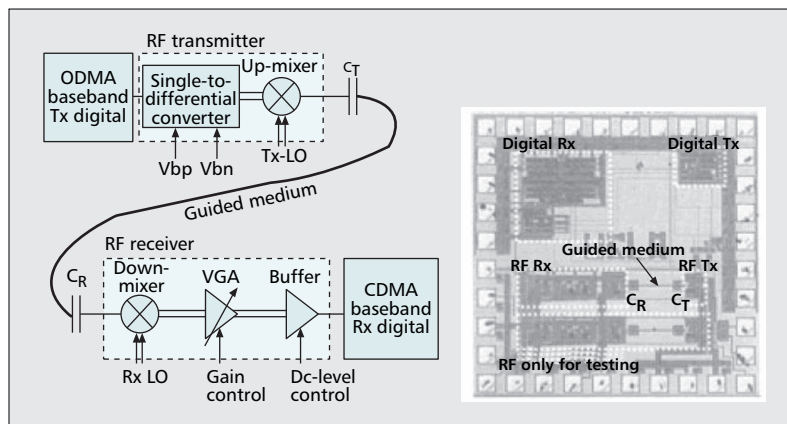
The use of RF signaling has an advantage over standard voltage signaling for inter-layer communication. Because the signal is modulated on a high-frequency carrier, it does not require a direct connection, and capacitive or inductive coupling is enough for transmission. Figure 6a shows a schematic view of a fabricated 3D integrated circuit demonstrating an RF interconnect using capacitive coupling, with the photograph of the actual die shown in Fig. 6b. In this circuit [10], an amplitude shift keying (ASK) modulation of a 25GHz carrier is used so that recovery of the data requires only an envelope detector. Metal layers in each of the tiers are used to form capacitors with values of tens of femtofarads that are sufficient for effective coupling. This realized RF interconnect achieves a maximum data rate of 11 Gb/s per wire and a very low bit error rate (BER) of  $10^{-14}$  measured at about 8 Gb/s. The use of small capacitors for coupling has an advantage over on-chip inductors or antennas due to the better field confinement that reduces cross-talk and interference between different links. Using a high frequency carrier wave would reduce interference with other baseband circuits or logic operating at much lower frequency. If interconnect density is high, more shielded types of transmission lines, such as striplines, should be considered.

### FUTURE PROSPECTS

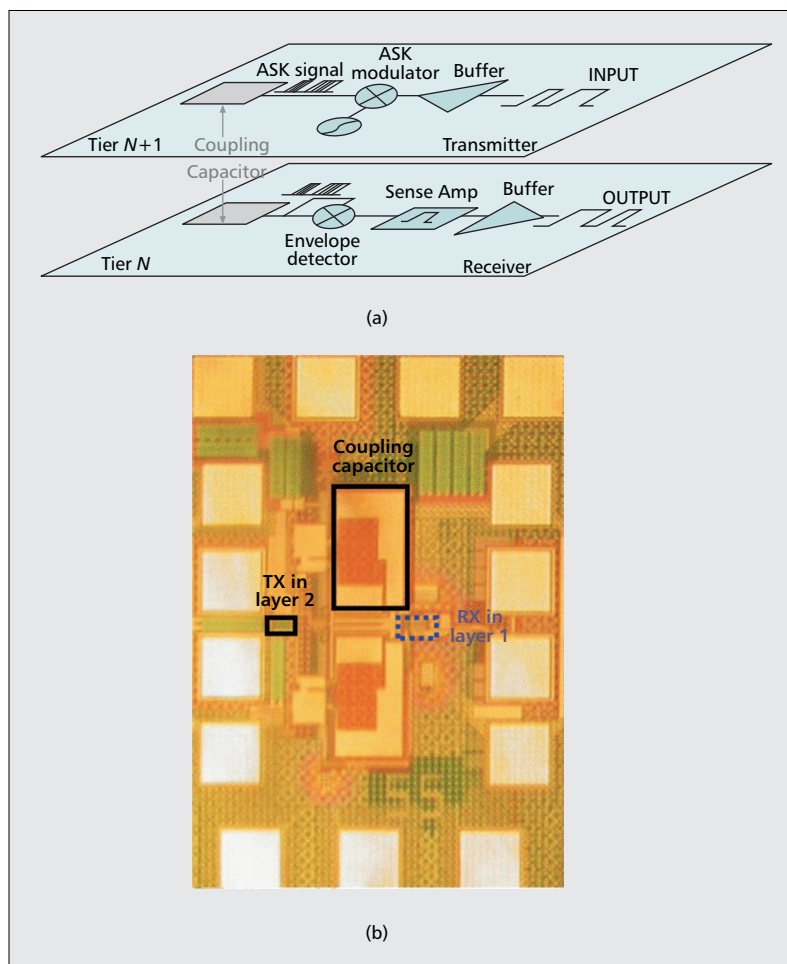
What does the future hold for RF circuits and techniques in the digital CMOS world?

One possible direction is the integration of FDMA and CDMA advantages into transceivers, creating multi-carrier CDMA (MC-CDMA). In these on-board or on-chip networks, data will be both coded and up-converted to higher carrier frequencies to enjoy both ultra-high aggregate data rates (reaching hundreds of Gb/s per wire) and a high level of re-configurability.

Another direction that awaits implementation is the application of RF interconnects to on-chip networks. With the number of on-chip cores and memory caches increasing, the communication between them will be a bottleneck. Using a



■ **Figure 5.** Schematic view (left) and chip photograph (right) of on-chip CDMA RF interconnect demonstrator.



■ **Figure 6.** RF interconnect prototype implemented in a 3D 0.18  $\mu\text{m}$  CMOS process: a) schematic view; b) chip photograph.



shared transmission line and transmission using RF frequencies would enable high bandwidth and low latency communication that would “cut through the traffic” of the conventional network on chip (NoC) architectures and enable further improvement of many-core microprocessors.

The use of RF interconnects for NoC may be further advanced by implementing the processor in a 3D fabrication process. 3D technology enables multi-tier implementation of CMOS circuits. In such a process, one of the tiers can be used for high-data-rate and low-latency RF communication links between the many cores on other tiers.

#### ACKNOWLEDGMENTS

The authors would like to thank the current and past members and collaborators of the UCLA High Speed Electronics Laboratory, including Prof. I. Verbauwhede, J. Kim, J. Ko, Q. Gu, Z. Xu, L. Zhang, Y. Qian, C. Chien, and H. Shin, for fruitful discussions and circuit design contributions.

#### REFERENCES

- [1] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd ed., Prentice Hall, 2003.
- [2] R. Dennard *et al.*, “Design of Ion-implanted MOSFETs with Very Small Physical Dimensions,” *IEEE J. Solid State Circuits*, vol. SC-9, no. 5, Oct. 1974, pp. 256–68.
- [3] T. Granberg, *Digital Techniques for High Speed Design*, Prentice Hall, 2004.
- [4] J. Kim *et al.*, “A Cost-Effective Latency-Aware Memory Bus for Shared-Memory Multi-Core Systems,” *IEEE Trans. Comp.*, to be published.
- [5] R. Ho, K. W. Mai, and M. A. Horowitz, “The Future of Wires,” *Proc. IEEE*, vol. 89, no. 4, 2001, pp. 490–504.
- [6] J. Held, J. Bautista, and S. Koehl, “From a Few Cores to Many: A Tera-scale Computing Research Overview,” [http://download.intel.com/research/platform/terascale/terascale\\_overview\\_paper.pdf](http://download.intel.com/research/platform/terascale/terascale_overview_paper.pdf)
- [7] J. Ko *et al.*, “An RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access Chip-to-Chip Communication,” *ISSCC Dig. Tech. Pap.*, Feb. 2005, pp. 338–39.
- [8] A. J. Viterbi, *CDMA Principles of Spread Spectrum Communication*, Communication Series, Addison-Wesley, June 1995.

- [9] M. F. Chang *et al.*, “RF/wireless Interconnect for Inter- and Intra-Chip Communications,” *Proc. IEEE*, vol. 89, no. 4, Apr. 2001, pp. 456–66.
- [10] Q. Gu *et al.*, “Two Gb/s/pin Low-Power Interconnect Methods for 3D ICs,” *ISSCC Dig. Tech. Pap.*, Feb. 2007, pp. 448–49.

#### BIOGRAPHIES

ERAN SOCHER (socher@ee.ucla.edu) earned a B.A. in physics, and B.Sc., M.Sc., and Ph.D. degrees in electrical engineering, all from the Technion — Israel Institute of Technology, where he worked on CMOS-compatible MEMS sensors and actuators and their readout electronics, especially for uncooled thermal imaging. He is a visiting researcher at the High Speed Electronics Laboratory and a visiting assistant professor in the Department of Electrical Engineering at the University of California at Los Angeles (UCLA). His current research interests are RF and millimeter-wave CMOS circuits for on-chip and wireless high data rate communication. Before joining UCLA in 2006 he was a research engineer in the Israel Defense Forces (IDF) and an adjunct lecturer at the Technion and Bar-Ilan University. He has authored over 30 journal and conference papers, and is the recipient of several teaching and research awards and scholarships.

MAU-CHUNG FRANK CHANG [F] received his B.S. in physics from National Taiwan University in 1972 and his Ph.D. in electrical engineering from National Chiao-Tung University, Taiwan, in 1979. He is currently a full professor in the Electrical Engineering Department and director of the High Speed Electronics Laboratory at UCLA. He is a co-editor of the IEEE Transactions on Electron Devices. Before joining UCLA, he was ssistant firector of the High Speed Electronics Laboratory at the Rockwell Science Center, where he developed and transferred the AlGaAs/GaAs HBT technology from the research laboratory to the production line (Conexant Systems). His research work has been mostly in the development of high-speed semiconductor devices and integrated circuits for mixed signal communication and sensor system applications. He is the inventor of the multi-I/O reconfigurable RF/wireless interconnects based on FDMA/CDMA multiple access algorithms for inter- and intra-ULSI communications. His research group has demonstrated the world’s first source-synchronous CDMA bus interface with reconfigurable multichip access capability and the first 324-GHz CMOS VCO. He has authored over 200 technical papers and 10 book chapters, edited one book, and holds 17 U.S. patents. He was honored with Rockwell’s Leonardo Da Vinci award in 1992, the National Chiao-Tung University’s Distinguished Alumni Award in 1997, and National Tsing-Hua University’s Distinguished Alumni Award in 2002.

Using a shared transmission line and transmission using RF frequencies would enable high bandwidth and low latency communication that would “cut through the traffic” of the conventional network on chip (NoC) architectures.