2025 IEEE Applied Power Electronics Conference and Exposition (APEC), Atlanta, GA, USA

Analysis and Implementation of Minimum-Sensor Capacitor Voltage Estimators for Flying Capacitor Multilevel Converters

S. T. Mahbub
R. K. Iyer
I. Z. Petric
R. C. N. Pilawa-Podgurski

Analysis and Implementation of Minimum-Sensor Capacitor Voltage Estimators for Flying Capacitor Multilevel Converters

S. Tahmid Mahbub, Rahul K. Iyer, Ivan Z. Petric, Robert C. N. Pilawa-Podgurski

Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA
Email: {tahmid, rkiyer, pilawa}@berkeley.edu, ivan5ric@ieee.org

***Abstract*—This work studies the estimation of capacitor voltages in the Flying Capacitor Multilevel (FCML) converter via direct measurements of only the input voltage, switched node voltage, and a minimum number of additional voltage sensors. Prior work developing capacitor voltage estimators for FCML converters has demonstrated that capacitor voltages are unobservable over specific ranges of duty ratios that depend on the converter level count. This work derives the minimum number of differential capacitor voltage sensors required to ensure capacitor voltage observability over the entire conversion ratio range and discusses where these sensors must be placed. Experimental results employing industry-standard digital signal processor hardware verify capacitor voltage observability with the proposed approach and demonstrate improved converter performance compared to the dithering solution previously proposed for retaining observability.**

I. Introduction

The Flying Capacitor Multilevel (FCML) [1] converter enables simultaneous use of smaller magnetic components and high-figure-of-merit low-voltage devices in designs, and has been recently explored in applications demanding highly efficient and compact power conversion solutions [2]–[6].

A generalized N-level FCML converter, shown in Fig. 1, is made up of $n_c = N-1$ series-connected complementary switch pairs and $M = N-2$ flying capacitors. In steady-state operation, the converter's switching signals are generated with symmetric Phase-Shifted Pulse-Width Modulation (PS-PWM) shown in Fig. 2, yielding a switched node voltage with effective frequency $f_{\text{eff}} = (N-1)f_{\text{s}}$ as shown in Fig. 3a. The reduced instantaneous switched node voltage and its higher fundamental frequency enable the use of an $(N-1)^2$ lower filter inductance L, compared to a 2-level converter, to meet a current ripple specification. Furthermore, the nominal balanced flying capacitor voltages are given by $v_{c,k} = \frac{k}{n_c}V_{\text{in}}$ where $k = \{0, ..., n_c - 1\}$ is an integer. This corresponds to an equal nominal blocking voltage of $\frac{1}{n_c}V_{\text{in}}$ across each switch in the converter, enabling the use of low-voltage switches with high figure-of-merit in place of high-voltage switches rated for the full supply voltage [7], [8].

In a FCML converter operated with PS-PWM, the capacitor voltages reach their nominal steady-state values via a "natural balancing" phenomenon characterized in [9]–[11]. Imbalance in capacitor voltages results in the inductor current ripple

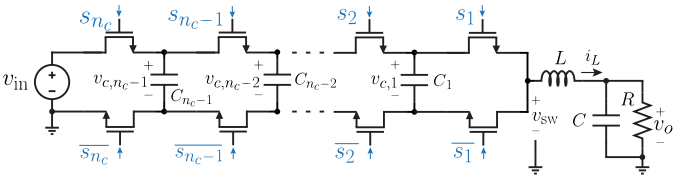


Fig. 1: Schematic of an N-level FCML converter showing $n_c = N-1$ complementary switch pairs and $M = N-2$ flying capacitors.

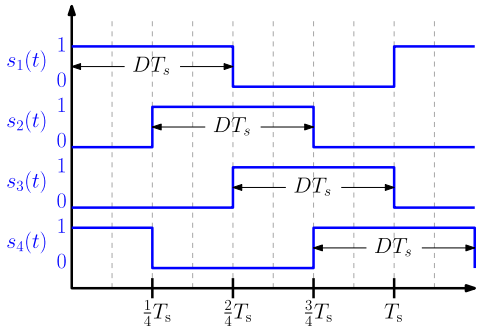
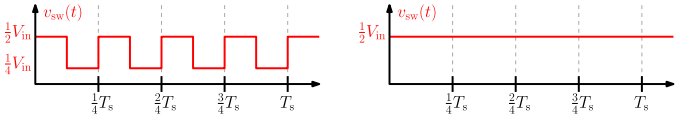


Fig. 2: Switching signals for a 5-level FCML converter generated with duty ratio $D = 0.5$ under PS-PWM.



(a) v_{sw} for $0.25 < D < 0.5$. (b) v_{sw} for $D = 0.5$.

Fig. 3: Switched node voltage v_{sw} under PS-PWM at different duty ratios D with balanced flying capacitor voltages for a 5-level FCML converter.

deviating from its nominal symmetric triangular shape, which drives nonzero average capacitor currents that serve to re-balance the system. The natural balancing dynamics are typically slow and underdamped. In converter start-up and shut-down scenarios, the oscillatory line transient response results in unequal voltage stresses across the power devices in the converter, and may cause switch blocking voltages to surpass the device ratings.

Recent work has investigated closed-loop "active balancing" control to regulate the flying capacitor voltages to their balanced fractions of the supply voltage [12]–[19]. However, most active balancing requires measurement of the capacitor voltages, which is typically accomplished with differential

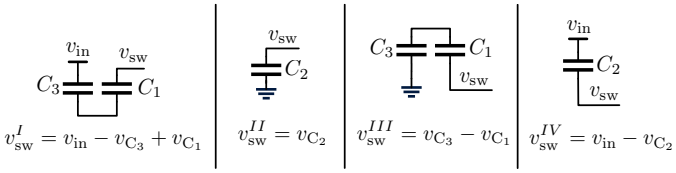


Fig. 4: Flying capacitor connections with $D = 0.5$ for the 5-level FCML converter. Each phase corresponds to a quarter of the switching period T_s.

voltage measurement circuits. As the required hardware in such schemes scales linearly with the converter level count N, this approach is cost-prohibitive for higher level-count designs and can significantly increase the overall system volume. Thus, recent research [12], [20]–[22] has investigated estimation of capacitor voltages with a reduced number of sensors by using only ground-referenced measurements of the supply input and the switched node voltage v_{sw}.

This work presents a systematic framework for: 1) identifying which capacitor voltages cannot be estimated solely with input and switched node measurements, and 2) subsequently identifying where additional sensor(s) must be placed to recover observability of all capacitor voltages, under the PS-PWM scheme. The proposed approach addresses cost-effective sensing for reliable control of flying capacitor voltages—a key obstacle to industry adoption of FCML converters. The results of this work are especially applicable to high level-count multilevel inverters in which the conversion ratio crosses several regions where capacitor voltages are unobservable in each line cycle.

Section II discusses the capacitor estimation problem, considering the relationship between the switched node voltage, the input voltage and the flying capacitor voltages. Section III analyzes the positioning of the minimum number of additional differential voltage sensors that must be placed to observe all capacitor voltages. Section IV compares the performance of the proposed minimum-sensor design with previously reported schemes for both a 5-level and a 7-level FCML converter.

II. The Capacitor Voltage Estimation Problem

The switched node voltage can be written as a combination of the M flying capacitor voltages and the input voltage in each switching phase. Under the assumption that the capacitor voltage dynamics are slow compared to the switching period, this relationship is described [22] in the form shown in (1). In this representation, $[v_{\text{sw}}]$ and $[v_{\text{in}}]$ are column vectors describing the values of the switched node and input voltages for each switching phase, $[v_{\text{c}}]$ is a column vector describing each flying capacitor's voltage, $[C]$ is a matrix that captures the polarity of capacitor connections to the switched node in each switching phase, and $[W]$ is a diagonal matrix describing whether the input voltage is connected to the switched node in a particular switching phase.

$$\underset{n_{\text{ph}}\times 1}{[v_{\text{sw}}]} = \underset{n_{\text{ph}}\times M}{[C]} \cdot \underset{M\times 1}{[v_{\text{c}}]} + \underset{n_{\text{ph}}\times n_{\text{ph}}}{[W]} \cdot \underset{n_{\text{ph}}\times 1}{[v_{\text{in}}]} \tag{1}$$

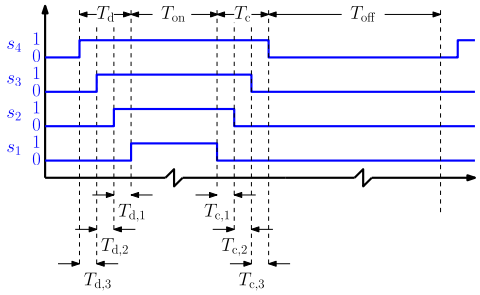


Fig. 5: Switching signals for a 5-level FCML converter generated with Quasi-Two-Level (Q2L) Modulation when inductor current has a negative valley and a positive peak. The capacitors are individually discharged during the $T_{\text{d},1}$, $T_{\text{d},2}$ and $T_{\text{d},3}$ intervals through the negative inductor current. The capacitors are individually charged during the $T_{\text{c},1}$, $T_{\text{c},2}$ and $T_{\text{c},3}$ intervals through the positive inductor current.

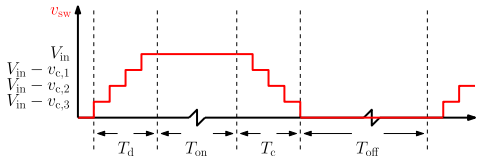


Fig. 6: Example waveform for the switched node voltage v_{sw} with Q2L switching. $T_{\text{on}} \gg T_{\text{d}}$, $T_{\text{on}} \gg T_{\text{c}}$.

A. Modulation Scheme

The relationship described in (1) depends on the modulation scheme being used. Fig. 2 and 4 show the switching signals and corresponding flying capacitor connections respectively for a 5-level FCML converter operating under PS-PWM with a 50% duty ratio. At this operating point, (1) is expanded as

$$\underset{[v_{\text{sw}}]}{\begin{bmatrix} v^I_{\text{sw}} \\ v^{II}_{\text{sw}} \\ v^{III}_{\text{sw}} \\ v^{IV}_{\text{sw}} \end{bmatrix}} = \underset{[C]}{\begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \end{bmatrix}} \underset{[v_{\text{c}}]}{\begin{bmatrix} v_{C_1} \\ v_{C_2} \\ v_{C_3} \end{bmatrix}} + \underset{[W]}{\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}} \underset{[v_{\text{in}}]}{\begin{bmatrix} v^I_{\text{in}} \\ v^{II}_{\text{in}} \\ v^{III}_{\text{in}} \\ v^{IV}_{\text{in}} \end{bmatrix}}. \tag{2}$$

If the matrix $[C]$ has full-column-rank, the unique minimum-norm solution for the flying capacitor voltages can either be determined exactly via the pseudoinverse [23] $[v_{\text{c}}] = [C]^{\dagger}\left([v_{\text{sw}}] - [W]\,[v_{\text{in}}]\right)$ or approximately via iterative methods such as that detailed in [22], [24]. The issue of capacitor voltage observability—whether capacitor voltages can be measured using only the switched node and input voltage measurements—therefore arises when $[C]$ is not full-column-rank, as detailed in [20]–[22].

When using an alternate modulation scheme, (2) is rewritten with different values of $[C]$ and $[W]$ depending on the sequence of switching states that appears over the switching period. For example, with the quasi-2-level (Q2L) modulation scheme [15]–[18], at most one capacitor is connected to the switched node in any switching phase, which guarantees observability of all capacitor voltages. To ensure the switched node voltage measurements are sufficiently far from switching transitions, the durations of the states when capacitors are connected must be sufficiently long.

Switching signals and an example switched node voltage waveform under the Q2L scheme are shown in Fig. 5 and

Fig. 6 respectively. For the rising edge of the switched node voltage under the Q2L scheme (during the T_{d} interval in Fig. 6), the system is described by

$$\underbrace{\begin{bmatrix} v_{\mathrm{sw}}^{I} \\ v_{\mathrm{sw}}^{II} \\ v_{\mathrm{sw}}^{III} \end{bmatrix}}_{[v_{\mathrm{sw}}]} = \underbrace{\begin{bmatrix} 0 & 0 & -1 \\ 0 & -1 & 0 \\ -1 & 0 & 0 \end{bmatrix}}_{[C]} \underbrace{\begin{bmatrix} v_{\mathrm{C}_1} \\ v_{\mathrm{C}_2} \\ v_{\mathrm{C}_3} \end{bmatrix}}_{[v_{\mathrm{c}}]} + \underbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{[W]} \underbrace{\begin{bmatrix} v_{\mathrm{in}}^{I} \\ v_{\mathrm{in}}^{II} \\ v_{\mathrm{in}}^{III} \end{bmatrix}}_{[v_{\mathrm{in}}]}. \tag{3}$$

$[C]$ is full-column-rank, implying observable capacitor voltages. Despite the observability advantage, the Q2L scheme relinquishes the $(N-1)^2$ reduction of filter inductance as compared to PS-PWM, which remains the most commonly used modulation scheme for the FCML converter. This work focuses on minimum-sensor estimation specifically under the PS-PWM scheme.

B. System Observability and Unobservable States

Under the PS-PWM scheme, matrix $[C]$ is rank-deficient when the duty ratio can be expressed as $D = \frac{m}{n_c}$, where $m \in \mathbb{N}$ and m and n_c are not co-prime [20], [21]. In practical implementations, the unobservable region is a range of duty ratios around these points as short-duration switching phases cannot be reliably sampled without coupling noise from the switching transitions into the switched node voltage measurements. At these conversion ratios, the total number of switching phases in a period is n_c. Therefore the rank deficiency, defined as $\rho_{\mathrm{d}} := n_c - 1 - \mathrm{rank}\left([C]\right)$, indicates the number of unobservable capacitor voltages. To recover observability at non-co-prime duty ratios, the number of differential capacitor voltage sensors required, N_{s}, is also given by the rank deficiency

$$N_{\mathrm{s}} = \rho_{\mathrm{d}} = n_c - 1 - \mathrm{rank}\left([C]\right) \tag{4}$$

The unobservable capacitor voltages can be identified from non-zero entries in the basis vectors spanning the null space of $[C]$. From the rank-nullity theorem, the number of basis vectors spanning the null space is equal to ρ_{d}. As an example, the null-space of $[C]$ from the 5-level converter example of (2) is spanned by

$$\{[n_1]\} = \left\{ \begin{bmatrix} 1 & 0 & 1 \end{bmatrix}^{\mathrm{T}} \right\}. \tag{5}$$

v_{C_1} and v_{C_3} can be expressed in terms of a common-mode and differential-mode value. The common-mode value is defined as $\left(v_{\mathrm{C}_1} + v_{\mathrm{C}_3}\right)/2$ and the differential mode value is defined as $v_{\mathrm{C}_3} - v_{\mathrm{C}_1}$. The nullspace basis vector $[n_1]$, in (5), indicates that a common offset applied to v_{C_1} and v_{C_3} is indeterminate from the switched node voltage measurements and only the differential mode value can be determined. This is readily verified from the switched node equations in Fig. 4. Thus, these two capacitor voltages cannot be uniquely estimated without additional information.

For a 7-level FCML ($n_c = 6$), duty ratios corresponding to $2/6$ ($m = 2$), $3/6$ ($m = 3$) and $4/6$ ($m = 4$) yield switched node voltage equations where certain capacitor voltages are unobservable. When operating at $D = 3/6$, the null-space basis vectors of the corresponding $[C]$ matrix are

$$\{[n_1], [n_2]\} = \left\{ \begin{bmatrix} 1 & 0 & 0 & 1 & 0 \end{bmatrix}^{\mathrm{T}}, \begin{bmatrix} 0 & 1 & 0 & 0 & 1 \end{bmatrix}^{\mathrm{T}} \right\}. \tag{6}$$

When operating at $D = 2/6$ and $D = 4/6$, the null-space basis vector is

$$\{[n_1]\} = \left\{ \begin{bmatrix} 1 & 0 & 1 & 0 & 1 \end{bmatrix}^{\mathrm{T}} \right\}. \tag{7}$$

Following the arguments made for the 5-level converter, the capacitor voltages cannot be uniquely estimated without additional sensors. Notably, the null-space basis vectors in (6) are shifted versions of each other due to the circulant nature of the capacitor connections under PS-PWM.

TABLE I
MINIMUM ADDITIONAL SENSOR COUNT

m \ n_{c}	2	3	4	5	6	7	8	9	10	11	12
1	0	0	0	0	0	0	0	0	0	0	0
2		0	1	0	1	0	1	0	1	0	1
3			0	0	2	0	0	2	0	0	2
4				0	1	0	3	0	1	0	3
5					0	0	0	0	4	0	0
6						0	1	2	1	0	5
7							0	0	0	0	0
8								0	1	0	3
9									0	0	2
10										0	1
11											0

III. Sensor Placement Strategy

The rank deficiency of the system's $[C]$ matrix, ρ_{d}, dictates the number of additional sensors needed to uniquely estimate all flying capacitor voltages at the corresponding duty ratio. Table I specifies the minimum number of flying capacitor voltage sensors to enable estimation across operating duty ratios for FCML converters under PS-PWM, up to 13 levels ($n_{\mathrm{c}} = 12$). The duty ratio is given by m/n_{c}.

As described in Section II-B, the unobservable capacitor voltages are identified by non-zero entries in the null-space basis vectors. In the 5-level case, adding a sensor to either v_{C_1} or v_{C_3} enables estimation of all flying capacitor voltages uniquely. In this approach, only 3 sensors are needed for the switched node voltage, the input voltage and either flying capacitor, with only the flying capacitor voltage requiring a differential sensor. This is two fewer than the total number of sensors required when measuring all flying capacitor voltages directly. For higher level count converters, the difference between the minimum-sensor design and a design sensing all capacitors is more significant.

In the case of measuring v_{C_1} directly, the additional measurement information can be captured by the augmented system described in (8), where $v_{C_1,\mathrm{meas}}$ indicates the directly measured capacitor voltage. Note that appending the elemen-

tary row vector $[1\ \ 0\ \ 0]$ to the $[C]$ matrix results in the full-column-rank *augmented* matrix $[C_{\rm aug}]$.

$$\underbrace{\begin{bmatrix} v_{\rm sw}^{I} \\ v_{\rm sw}^{II} \\ v_{\rm sw}^{III} \\ v_{\rm sw}^{IV} \\ \hline v_{C_1,\rm meas} \end{bmatrix}}_{[v_{\rm sw}]} = \underbrace{\begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 0 \\ \hline 1 & 0 & 0 \end{bmatrix}}_{[C_{\rm aug}]} \underbrace{\begin{bmatrix} v_{\rm C_1} \\ v_{\rm C_2} \\ v_{\rm C_3} \end{bmatrix}}_{[v_{\rm c}]} + \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ \hline 0 & 0 & 0 & 0 \end{bmatrix}}_{[W_{\rm aug}]} \underbrace{\begin{bmatrix} v_{\rm in}^{I} \\ v_{\rm in}^{II} \\ v_{\rm in}^{III} \\ v_{\rm in}^{IV} \end{bmatrix}}_{[v_{\rm in}]}. \tag{8}$$

For the 7-level converter, the null-space basis vectors corresponding to operation at $D = 3/6$, given in (6), indicate that one sensor must measure either v_{C_1} or v_{C_4} and a second sensor must measure v_{C_2} or v_{C_5}. The null-space basis vector corresponding to operation at $D = 2/6$ and $D = 4/6$, given in (7), indicates that one sensor must measure either v_{C_1}, v_{C_3}, or v_{C_5}. To preserve observability across all duty ratios, the 7-level converter has several possible combinations of additional sensors. Of particular interest is the addition of sensors for $v_{\rm C_1}$ and $v_{\rm C_2}$. This minimum-sensor addition places the sensors at the lowest voltage capacitors and ensures capacitor voltage observability over the entire conversion ratio range.

Elementary row vectors corresponding to the measurement of $v_{\rm C_1}$ and $v_{\rm C_2}$—$[1\ \ 0\ \ 0\ \ 0\ \ 0]$ and $[0\ \ 1\ \ 0\ \ 0\ \ 0]$— can be appended to the $[C]$ matrix corresponding to the 7-level FCML converter to obtain the corresponding full column-rank *augmented* matrix $[C_{\rm aug}]$ similar to the 5-level case in (8).

In the general case, the minimum number of sensors can be placed sequentially from C_1, C_2 and onwards, or from $C_{\rm M}$, $C_{\rm M-1}$ and so on. Placing sensors at the lowest voltage capacitors is advantageous as lower common-mode voltages require less attenuation on resistive dividers, which is helpful for reducing measurement noise, and allows for smaller routing clearances in the sensing circuits.

As a further example, an 11-level FCML ($n_c = 10$) converter may be considered. Table I indicates that 4 flying capacitor voltage sensors are needed. Adding sensors from either end—$\{v_{\rm C_1}, v_{\rm C_2}, v_{\rm C_3}, v_{\rm C_4}\}$ or $\{v_{\rm C_9}, v_{\rm C_8}, v_{\rm C_7}, v_{\rm C_6}\}$—will enable recovering observability across all duty ratios.

IV. Experimental Characterization

The proposed estimator is implemented on a Texas Instruments TMS320F28379D DSP. Assuming that the dynamics of capacitor voltages are slow compared to the rate at which they appear in the estimator equations, they are estimated using Richardson's iterative method [24]. This work extends the estimator design of [22] by incorporating information from the additional minimum sensors. The outputs of the iterative solver corresponding to the estimated capacitor voltages are augmented by the measured differential capacitor voltage readings as in (8) for the 5-level case. This can be implemented by skipping the iterative computation for each capacitor that has an attached sensor and using the capacitor voltage directly.

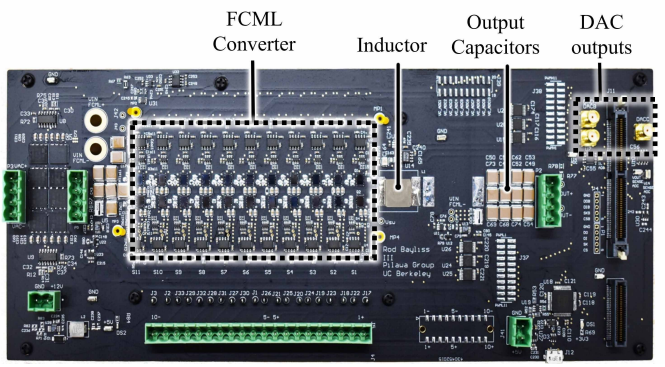


Fig. 7: FCML converter prototype used in this work. $L = 4.7\,\mu$H, $C_{\rm fly} = 8.8\,\mu$F, $f_{\rm sw,eff} = 200\,$kHz.

TABLE II
CONVERTER SPECIFICATIONS

Converter Parameter	Value
Effective Switching Frequency	200 kHz
Inductance	4.7 μH
Flying Capacitance	4x 2.2 μF
Switches	EPC2302
Gate Driver	LM5114
Isolator	ADUM5240
Cap. Voltage Sensor	AD8429ARZ-R7

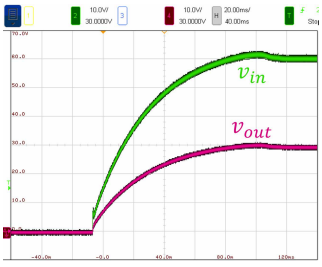
The estimator is verified on the prototype shown in Fig. 7. The hardware is a 12-level converter with key parameters given in Table II, with the ability to configure to a lower level count by shorting consecutive switching cells. To verify minimum-sensor operation, the estimator is verified on both a 5-level and a 7-level converter. To maintain similar harmonic content in the inductor current without changing the inductance, the effective switching frequency, $f_{\rm eff}$, was kept constant between the 5-level and 7-level tests.

The digital-to-analog converters (DACs) on the DSP were used to output the estimated capacitor voltages so that they may be measured on an oscilloscope along with the real measured flying capacitor voltages. The signals are scaled on the oscilloscope for direct comparison with measured capacitor voltages. Experiments were carried out with natural balancing under the PS-PWM scheme.

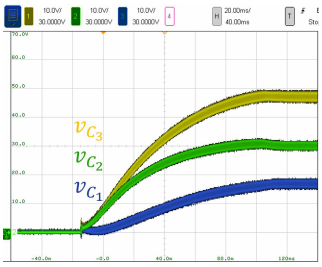
A. Estimation for a 5-Level Converter

The 12-level converter is reconfigured as a 5-level FCML converter by shorting seven switching cells. The converter is operated at the unobservable nominal duty ratio $D = 0.5$.

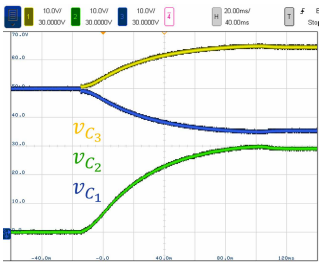
Results are first shown in Fig. 8 for the converter operating under an input voltage transient typical of a startup scenario highlighting the inability to correctly estimate v_{C_1} and v_{C_3} without the additional voltage sensor on C_1. Fig. 9 illustrates the erroneous estimation in steady-state without additional sensor information for C_1. The estimated voltages snap to the correct values once the sensor information is used for capacitor C_1. In these tests, v_{C_2} is unaffected by the use of the sensor since its voltage is an observable state. In contrast, Fig. 10



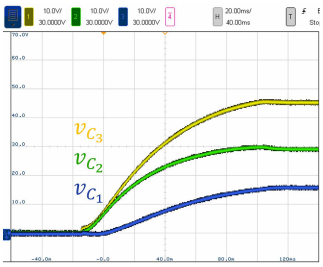
(a) Input and output voltages during startup from 0 V to 60 V with $D = 0.5$.



(b) Measured flying capacitor voltages during startup.

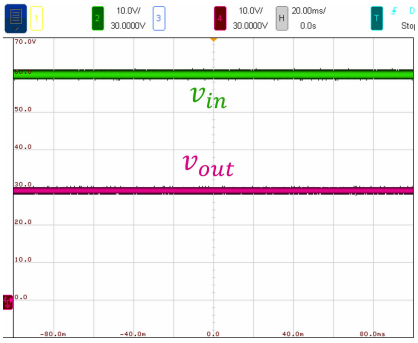


(c) Estimated capacitor voltages with no additional capacitor voltage sensors.

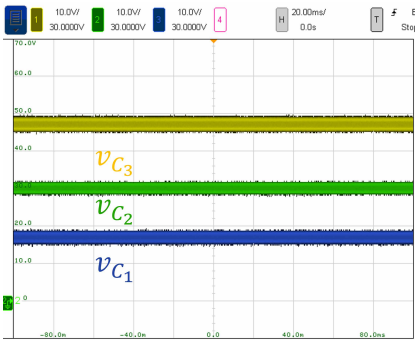


(d) Estimated capacitor voltages with additional sensor for C_1.

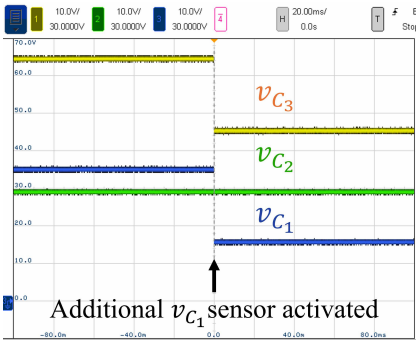
Fig. 8: Supply startup test 0 V to 60 V with $D = 0.5$ for the 5-level FCML converter. At this operating point, v_{C_1} and v_{C_3} cannot be correctly estimated from just the input and switched node measurement. The addition of a sensor for C_1 enables correct estimation of all flying capacitor voltages.



(a) Steady state input (60 V) and output (30 V) voltages with $D = 0.5$.

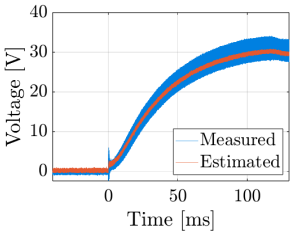


(b) Measured flying capacitor voltages in steady state operation.

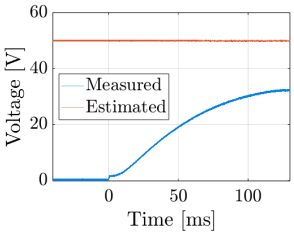


(c) Estimated capacitor voltages before and after additional sensor for C_1 is used.

Fig. 9: Steady-state estimation test for the 5-level FCML converter. Before the v_{C_1} sensor is used, only v_{C_2} is correctly estimated. Once the sensor is used, v_{C_1} and v_{C_3} snap to the correct estimates that match measurements. v_{C_2} is unaffected by the use of the sensor.



(a) Differential mode voltage.



(b) Common mode voltage.

Fig. 10: Cap voltages v_{C_1} and v_{C_3}, during input startup from 0 V to 60 V, for the 5-level FCML converter in Section IV-A. The differential mode voltage is defined as $v_{C_3} - v_{C_1}$.The common mode voltage is defined as $\left(v_{C_3} + v_{C_1}\right)/2$. The estimated differential voltages match the measured values. The common mode voltage cannot be correctly estimated without additional sensors.

depicts the incorrect common-mode voltage estimation for v_{C_1} and v_{C_3} without the use of the additional sensor.

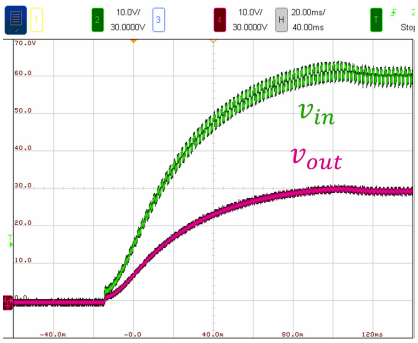
Prior work [22] has demonstrated the use of a dithering scheme, operating at observable duty ratios $D = 0.485$ and 0.515 for an effective conversion ratio of 50%. Fig. 11 illustrates the result of a similar dithering implementation and highlights the increased ripple on the flying capacitor voltages as well as on the supply line voltage. The estimator proposed in this work does not suffer from the increased ripple observed with dithering.

B. Estimation for a 7-Level Converter

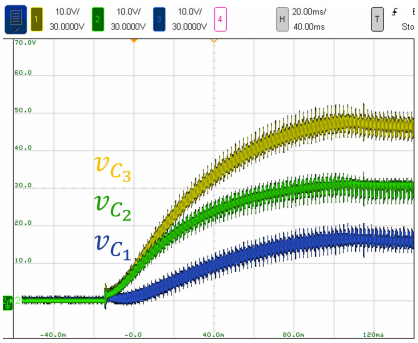
The 12-level converter is reconfigured as a 7-level FCML converter by shorting five switching cells. For clarity of the presented experimental data, the measured and estimated capacitor voltages from multiple oscilloscopes are combined and plotted on a single set of axes via post-processing in MATLAB.

Results are shown in Fig. 12 for the converter operating under an input voltage transient typical of a startup scenario. The converter is operating at an unobservable duty ratio of $D = 0.5$. This experiment illustrates the inability to correctly estimate v_{C_1}, v_{C_2}, v_{C_4} and v_{C_5} without the additional voltage sensors on C_1 and C_2.

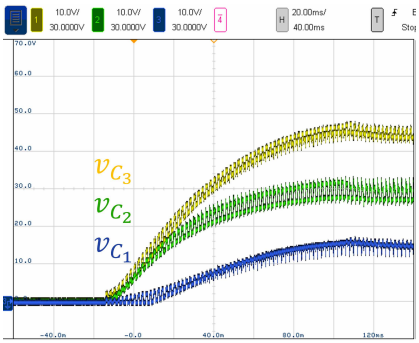
As indicated from (6), only the difference between v_{C_1} and v_{C_4} can be computed uniquely but not their common mode voltage. Similarly, only the difference between v_{C_2} and v_{C_5} can be computed uniquely but not their common mode voltage. This is observed in Fig. 12b. As illustrated in Fig. 10, the startup transient is coupled into both the common mode and differential mode voltages. Since the estimated values in Fig. 12b do not capture the correct common mode voltage as described above, they arrive at incorrect steady-state values before the measured capacitor voltages have reached steady-state. The parameter v_{C_3} is correctly estimated without the need for additional sensors. The addition of sensors for C_1 and C_2 enables correct estimation of all flying capacitor voltages.



(a) Input and output voltages during startup to 60 V with $D = 0.5 \pm 0.015$ dithering.

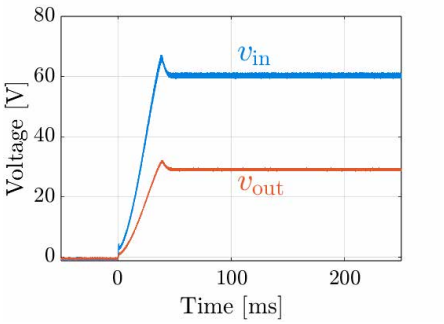


(b) Measured flying capacitor voltages during startup with dithering.

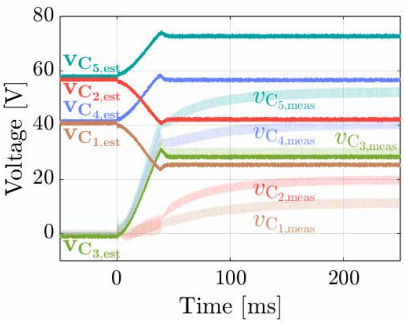


(c) Estimated capacitor voltages during startup with dithering.

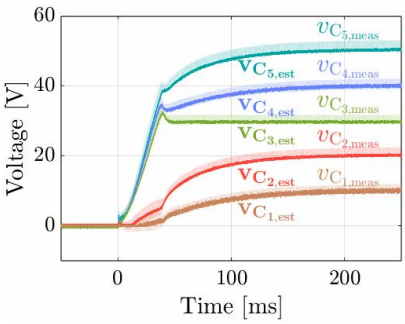
Fig. 11: Dithering test for the 5-level FCML converter without using sensor for C_1. Dithering around $D = 0.5$ enables estimating v_{C_1} and v_{C_3} at an otherwise unobservable operating point. However, the impact of dithering propagates to all flying capacitor voltages and the input voltage.



(a) Input and output voltages during startup from 0 V to 60 V with D = 0.5.



(b) Capacitor voltages with no additional capacitor voltage sensors.



(c) Capacitor voltages with additional sensor for C_1 and C_2.

Fig. 12: Supply startup test 0 V to 60 V with $D = 0.5$ for the 7-level FCML converter. Lighter shaded colors—annotated as $v_{C_{x,meas}}$—represent measured capacitor voltages; darker shaded colors—annotated as $v_{C_{x,est}}$—represent voltages estimated by the DSP. At this operating point, v_{C_1}, v_{C_2}, v_{C_4} and v_{C_5} cannot be correctly estimated from just the input and switched node measurements. The addition of sensors for C_1 for C_2 enables correct estimation of all flying capacitor voltages.

V. Conclusions

This work analyzes and demonstrates an implementation of minimum-sensor capacitor voltage estimation for FCML converters over the entire conversion ratio range. The presented framework for a general N-level converter demonstrates the ability to place sensors at the lowest capacitor voltages under PS-PWM. The estimator is implemented on a commercial digital signal processor and demonstrates excellent tracking of the capacitor voltages for practical 5-level and 7-level converters. Future work will investigate implementation of the estimator alongside closed-loop active balancing control in FCML converters with a small number of sensors, enabling reduction in converter volume and cost.

Acknowledgment

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0001609 in the OPEN 2021 program monitored by Dr. Olga Blum Spahn. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

References

[1] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403 vol.1.

[2] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[3] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a gan-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 153–12 165, 2020.

[4] L. Horowitz and R. C. Pilawa-Podgurski, "A 14-level fcml inverter for electric vehicles with optimal capacitors achieving 175 kw/kg and 380 kw/l power density," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 1009–1013.

[5] O. Lorenz and J. Sanchez, "Ultra low-profile flying capacitor 7-level 3kw pfc with optimized high frequency layout and active balancing using 100v gan," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 22–28.

[6] Q. Huang, Q. Ma, P. Liu, A. Q. Huang, and M. A. de Rooij, "99% efficient 2.5-kw four-level flying capacitor multilevel gan totem-pole pfc," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 5795–5806, 2021.

[7] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020.

[8] J. Azurza Anderson, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, and J. W. Kolar, "Three levels are not enough: Scaling laws for multilevel converters in ac/dc applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3967–3986, 2021.

[9] T. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, pp. 356–364, 1997.

[10] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The general case," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1658–1666, 2006.

[11] Z. Xia, B. L. Dobbins, and J. T. Stauth, "Natural balancing of flying capacitor multilevel converters at nominal conversion ratios," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[12] G. Farivar, A. M. Y. M. Ghias, B. Hredzak, J. Pou, and V. G. Agelidis, "Capacitor voltages measurement and balancing in flying capacitor multilevel converters utilizing a single voltage sensor," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 8115–8123, 2017.

[13] C.-Y. Lu, D.-H. Lin, and H.-C. Chen, "Decoupled design of voltage regulating and balancing controls for four-level flying capacitor converter," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 12 152–12 161, 2021.

[14] R. K. Iyer, I. Z. Petric, R. S. Bayliss, N. C. Brooks, and R. C. N. Pilawa-Podgurski, "A high-bandwidth parallel active balancing controller for current-controlled flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, pp. 1–15, 2024.

[15] R. K. Iyer, S. T. Mahbub, and R. C. N. Pilawa-Podgurski, "Dynamical modeling and control of the flying capacitor multilevel converter under quasi-two-level switching for active balancing in light-load conditions," in *2024 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2024, pp. 1–7.

[16] R. K. Iyer, S. T. Mahbub, and R. C. Pilawa-Podgurski, "Quasi- two-level switching for active balancing of flying capacitor multilevel converters under light-load conditions," in *2024 IEEE International Communications Energy Conference (INTELEC)*, 2024, pp. 1–7.

[17] P. Czyz, P. Papamanolis, F. Trunas Bruguera, T. Guillod, F. Krismer, V. Lazarevic, J. Huber, and J. W. Kolar, "Load-independent voltage balancing of multi-level flying capacitor converters in quasi-2-level operation," *Electronics*, vol. 10, no. 19, 2021. [Online]. Available: https://www.mdpi.com/2079-9292/10/19/2414

[18] S. Mersche, D. Bernet, and M. Hiller, "Quasi-two-level flying-capacitor-converter for medium voltage grid applications," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 3666–3673.

[19] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 769–778, 2012.

[20] Z. Xia, B. L. Dobbins, J. S. Rentmeister, and J. T. Stauth, "State space analysis of flying capacitor multilevel dc-dc converters for capacitor voltage estimation," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 50–57.

[21] Z. Xia, K. Datta, and J. T. Stauth, "State-space modeling and control of flying-capacitor multilevel dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 38, no. 10, pp. 12 288–12 303, 2023.

[22] I. Z. Petric, R. K. Iyer, N. C. Brooks, and R. C. N. Pilawa-Podgurski, "A real-time estimator for capacitor voltages in the flying capacitor multilevel converter," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–8.

[23] A. Ben-Israel and T. N. E. Greville, *Generalized Inverses: Theory and Applications*. New York, NY: Springer, 2003.

[24] L. F. Richardson, "The approximate arithmetical solution by finite differences of physical problems involving differential equations, with an application to the stresses in a masonry dam," *Philosophical Transactions of the Royal Society of London. Series A, Containing Papers of a Mathematical or Physical Character*, vol. 210, pp. 307–357, 1911. [Online]. Available: http://www.jstor.org/stable/90994