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Whole-Chip ESD CAD Tools and Scalable ESD Device Modeling Methodology

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Li Wang

June 2015

Dissertation Committee:
Dr. Albert Wang, Chairperson
Dr. Jianlin Liu
Dr. Sheldon Tan

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The Dissertation of Li Wang is approved:

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Committee Chairperson

University of California, Riverside

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To my family for all the supports.

ABSTRACT OF THE DISSERTATION

Whole-Chip ESD CAD Tools and Scalable ESD Device Modeling Methodology

by

Li Wang

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, June 2015
Dr. Albert Wang, Chairperson

Electrostatic discharge (ESD) failure is a major reliability problem to integrated circuits (IC). On-chip ESD protection is mandatory for all IC chips to protect against any possible ESD damages. Therefore, Whole-chip ESD protection circuit simulation is essential to chip-level ESD protection design synthesis, optimization, verification and prediction. Today, trial-and-error approaches still dominate in practical ESD circuit designs due to lack of full-chip ESD simulation tools and accurate ESD device modeling technique.

This thesis reports a new chip-level ESD CAD tool, which can accurately extract ESD devices from layout files, generate an ESD netlist, simulate ESD discharge function at chip level and conduct full-chip ESD zapping test simulation. This CAD tool is designed with several unique algorithms and a smart ESD parametric checking mechanism, which takes full consideration of ESD protection operation principles. Therefore, this new CAD tool is different from existing simple ESD spacing and bus resistance checking approaches, and can achieve whole-chip ESD protection verification and prediction. The CAD tool consists of three modules: an ESD device extraction

module, an ESD design inspection module and an ESD zapping test module. The ESD extraction module can accurately extract arbitrary ESD protection structures at full chip level. Decomposed-based subgraph isomorphism algorithm is used for ESD device extraction to improve time efficiency. The ESD design inspection module serves to remove non-critical ESD devices extracted based upon a novel smart parametric checking mechanism. The ESD zapping test module is developed to perform complex ESD protection zapping test simulation using Dijkstra's algorithm to resolve the problem of finding the critical ESD discharging path at chip level. The new ESD CAD tool was verified at full chip level using ESD protection designs implemented in 0.35 μm BiCMOS technology.

ESD device models were reported for traditional diode and MOSFET type ESD structures. However, due to complex ESD behaviors, particularly the electro-thermal-process-device-circuit-layout coupling effects, the existing ESD models have limited accuracy in describing complex ESD physics and coupling effects, such as thermal boundary condition and snapback I-V behavior.

This thesis presents a new scalable ESD behavioral modeling technique, which uses Verilog-A to develop accurate ESD behavior models for various ESD protection structures, such as novel nano crossbar ESD protection structures, novel 3D field-programmable ESD protection structures using SONOS and NCD ESD devices, silicon controlled rectifier (SCR) based ESD protection structures, HV diode and SCR ESD protection structures, 28nm CMOS gated diode and DTSCR ESD protection structures. The new scalable ESD behavior modeling technique was fully verified by SPICE circuit

simulation and transmission line pulse (TLP) ESD testing, which will enable whole-chip ESD circuit design optimization and verification.

Flip chip technique using ball grid array (BGA) pad-ring arrays is a popular technology for small footprint chips used in size-sensitive electronics. However, ESD protection design for ICs using large BGA pad-ring array is an emerging challenge since where to place an ESD structure becomes a real layout design problem.

This thesis reports design of a BGA pad-ring array with different ESD metal routing for a visible light communication (VLC) transceiver implemented in 180nm BCD technology at whole-chip level. The ESD structures and their ESD-critical parameters, and the ESD metal bus resistance were extracted by our ESD Extractor CAD tool. The new ESD behavior modeling technique was used to model the ESD structures. The extraction and modeling was validated by SPICE simulation and TLP testing for different ESD metal routing.

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Chapter 1 Introduction

1.1 Background

ESD (electrostatic discharge) phenomenon originates from transfer of static electric charges between two objects with different electrostatic potentials as they are brought into contact [1]. Figure 1.1 shows one of the most-widely ESD scenario, where the human body discharging current to IC parts. This process usually lasts several hundred nanoseconds and the peak current could reach to several amperes. The heat produced by the human body discharging current will cause thermal breakdown damage in the IC parts if there're no proper on-chip ESD protection structures [48].

Figure 1.1 ESD damage to IC chips

In the past few years, up to billions of dollars loss is caused by ESD damage in IC (integrated circuit) industry every year, since the ESD resulting large voltage and current surges may cause severe damages to IC parts. Therefore, ESD failure is becoming a major reliability problem to IC chips, which have gained wide research interests from both academic and industry.

There're two types of ESD induced damages: thermal breakdown due to high current, and MOSFET gate dielectric rupture due to excess electric field, both of which are the catastrophic failures. Figure 1.2 shows two kinds of ESD induced damages, including thermal breakdown which often happens on the output IO, and gate breakdown which often happens at the input IO since the gate is directly faced to the ESD pulse. Hence, on-chip ESD protection is mandatory for all IC chips to protect against any possible ESD damages [2]. In principle, on-chip ESD protection is implemented in the way that an ESD protection unit is connected between a pair of IC pins such as I/O to ground (GND). The ESD protection structure remains off in normal IC operation. When an ESD transient appears at the I/O pin, it will trigger the ESD protection circuit and form a low-impedance shunting path to discharge the high ESD current efficiently. ESD protection is provided since not too much heat is generated and I/O voltage is clamped to a sufficiently low level to avoid any dielectric rupture.

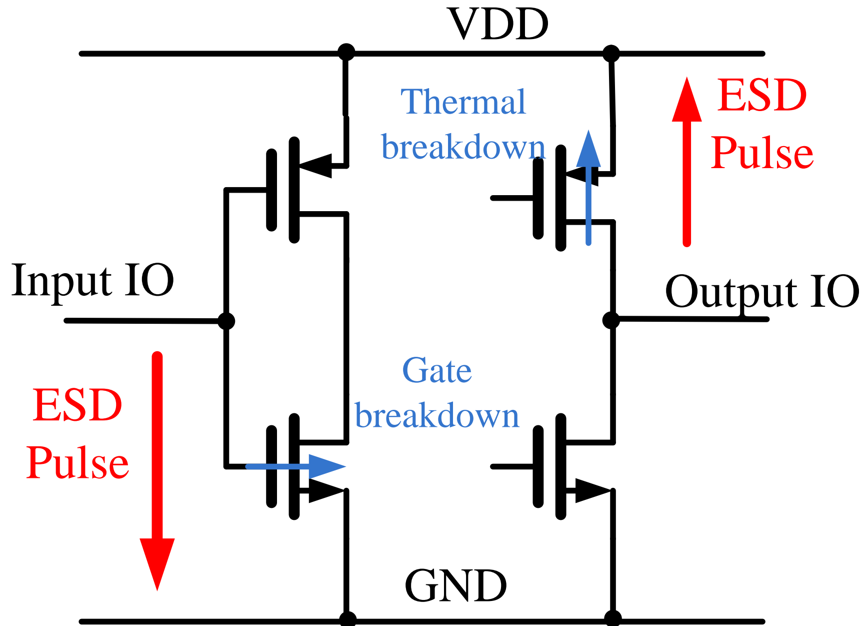


Figure 1.2 ESD induced damages: thermal breakdown and gate breakdown

As IC technologies continue advance into very-deep-sub-micron (VDSM) domain as shown in Figure 1.3 , on-chip ESD protection circuit design becomes increasingly more challenging particularly for parasitic sensitive analog, mixed-signal (AMS) and multi-GHz RF ICs [3, 4]. There are many challenges remain to be addressed in ESD protection designs, including CAD based ESD protection design methodology for design prediction and optimization, ESD-RFIC co-design, accurate high current ESD device modeling, low-parasitic ESD protection for RF/AMS ICs, accurate RF ESD design characterization, and ESD protection for nano systems, and so on [52]. However, whole-chip ESD protection design verification CAD tools and accurate high-current ESD device modeling are in urgent demand because the experience-based trial-and-error ESD protection design approaches, which are both time-consuming and exceedingly expensive, are becoming intolerable to today's design of complex chips with large number of I/O

pins and strong influences between ESD protection and the core IC protected [3]. A working stand-alone ESD protection unit does not warrant chip level ESD operation because parasitic devices inside the core circuit has the potential of becoming an unexpected shunting path, which will cause ESD failure. It usually takes average two or three times for an experienced circuit designer to complete a successful ESD protection design. The demand for 1st–Si success to meet the critical time-to-market requirement in industrial designs will not be possible without CAD-based whole-chip ESD protection design verification and accurate high-current ESD device modeling. In all, novel whole-chip ESD verification CAD tool and accurate high-current ESD device modeling are the biggest challenges in on-chip ESD protection designs.

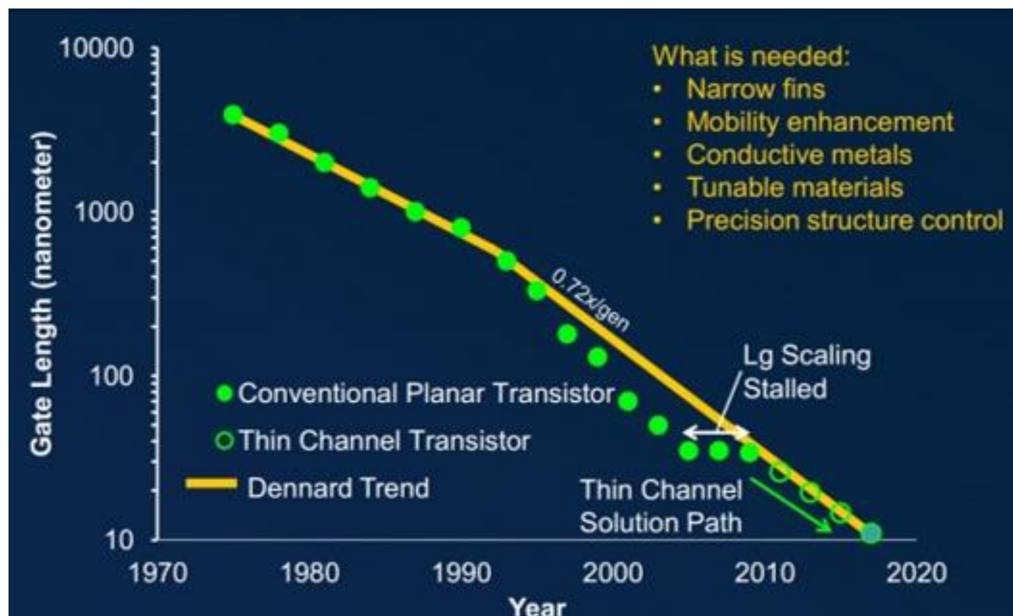


Figure 1.3 IC Technology Roadmap (from internet)

1.2 Whole-chip ESD Protection Design Principle

The principle of ESD protection is two ways: one is to discharge high ESD current through a low impedance path, and the other is to clamp voltage to a low level.

The typical discharging I-V curves of ESD protection structures are shown in Figure 1.4 (a) simply turn-on type (b) snapback type.

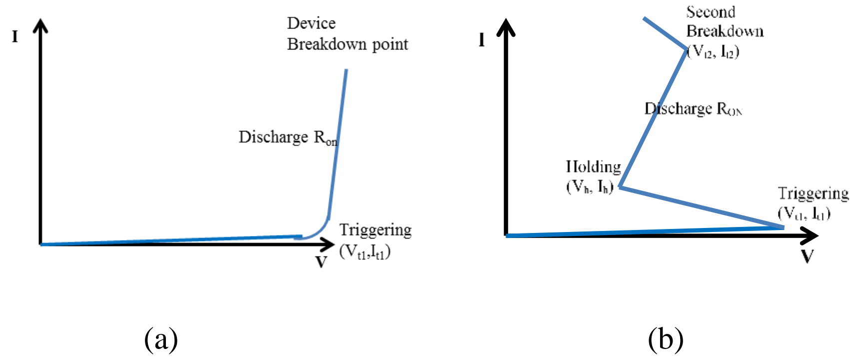


Figure 1.4 Typical discharging I-V curves for ESD protection structures (a) simply turn-on (b) snapback

The simply turn-on type ESD protection structure will be triggered to discharge ESD current after the device voltage reaches its turn-on voltage (V_{t1}) as depicted in Figure 1.4 (a). "On-resistance" (R_{on}) indicates the discharging resistance of the I-V curve. The ESD protection structure could provide lower clamping voltage when the R_{on} is lower. The ESD protection structure will breakdown, when the ESD current exceeds its ESD current protection ability.

The second solution is based on the snapback I-V curve shown in shown in Figure 1.4 (b). When the ESD voltage stress on this type of ESD protection structure reaches its triggering voltage (V_{t1}), it will firstly go into a state of negative resistance, which is called snapback, until the device voltage reduces to the holding voltage (V_h). The holding voltage V_h will clamp the ESD voltage on device to a sufficiently low level and hence protect the inner circuits from dielectric breakdown. The ESD protection structure begins

to discharge ESD current in a low-R_{on} state until it reaches the second breakdown (V_{t2}, I_{t2}) after the holding voltage.

The triggering voltage, current and time (V_{t1}, I_{t1} and t_1), holding voltage and current (V_h and I_h), discharging on-resistance (R_{on}), second breakdown voltage and current (V_{t2}, I_{t2}), are all critical parameters for ESD protection structures. Proper ESD protection requires comprehensive design consideration for these ESD critical parameters in practices.

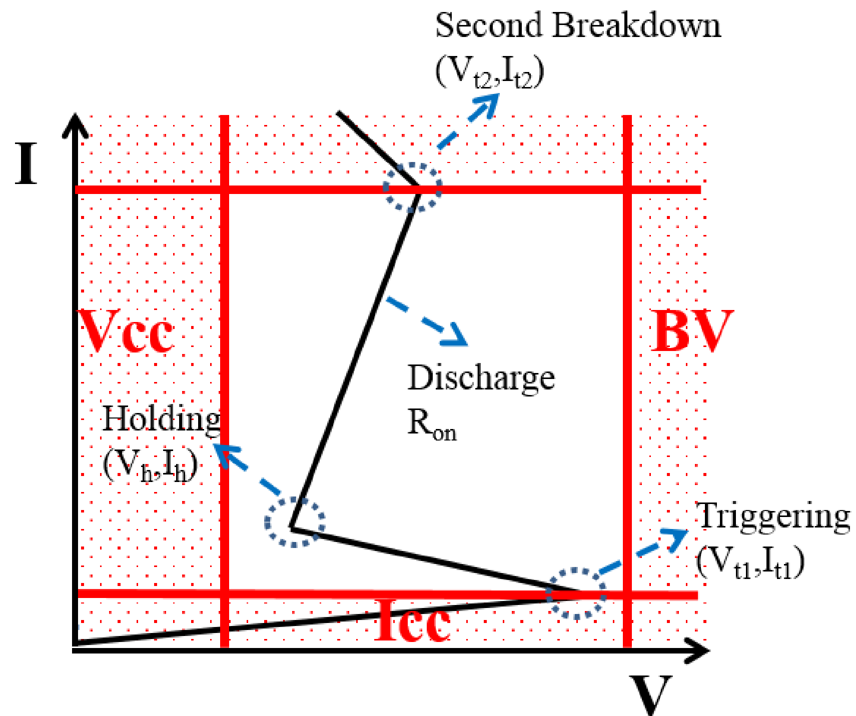


Figure 1.5 ESD Protection Design Window

The region between inner circuit breakdown voltage (BV) and power supply voltage (V_{CC}) , with current bounded by the total on-chip supply current (I_{CC}), is called ESD Design Window as shown in Figure 1.5. Firstly, the V_{t1} of ESD protection structure

must be lower than the breakdown voltage of the protection node by a safety margin (at least 10%). V_{t1} also needs to be higher than V_{CC} since the ESD protection structure should be kept off during inner circuit normal operation. Secondly, V_h should be higher than the supply voltage (V_{CC}) by a safety margin and I_h should be higher than the supply current (I_{CC}) to avoid possible latch-up effect. The emerging challenge is that, this ESD design window becomes narrower when using traditional ESD protection structures as IC technologies continue to advance into sub-100nm domains [39]. Therefore, it is imperative to develop novel non-traditional ESD protection structures and triggering-assisting circuitry to satisfy the narrower ESD design window, which makes today's ESD protection design more complicated [43, 47]. As a result, whole-chip ESD protection design verification CAD tools and accurate high-current ESD device modeling are strongly needed to simulate the complicated ESD protection design and modeling the novel ESD protection structure.

Moreover, ESD protection design is a whole-chip design task as opposed to designing stand-alone ESD protection devices. Ideally, a complete full-direction ESD protection solution is necessary for the whole IC chip as illustrated in Figure 1.6 for a mixed-signal chip, which consists of I/O ESD protection for each I/O pad, as well as a power clamp. The ESD protection in the circuit should provide ESD protections in the directions as follows to protect against all possible ESD pulse modes: positive ESD from I/O to VSS (PS), negative ESD from I/O to VSS (NS), positive ESD from I/O to VDD (PD), negative ESD from I/O to VDD (ND), positive ESD from VDD to VSS (DS) and positive ESD from VSS to VDD (SD). As a result, there is a low-impedance conducting

path from each pad to any other pads on the chip. However, full-chip complete ESD protection scheme may resulted in significant ESD-induced parasitic effects and large layout area used if traditional one-directional ESD protection devices are used. Hence, novel multi-directional ESD protection structures are desired [3] and so accurate high-current ESD device modeling are necessary for the novel multi-directional ESD protection structure.

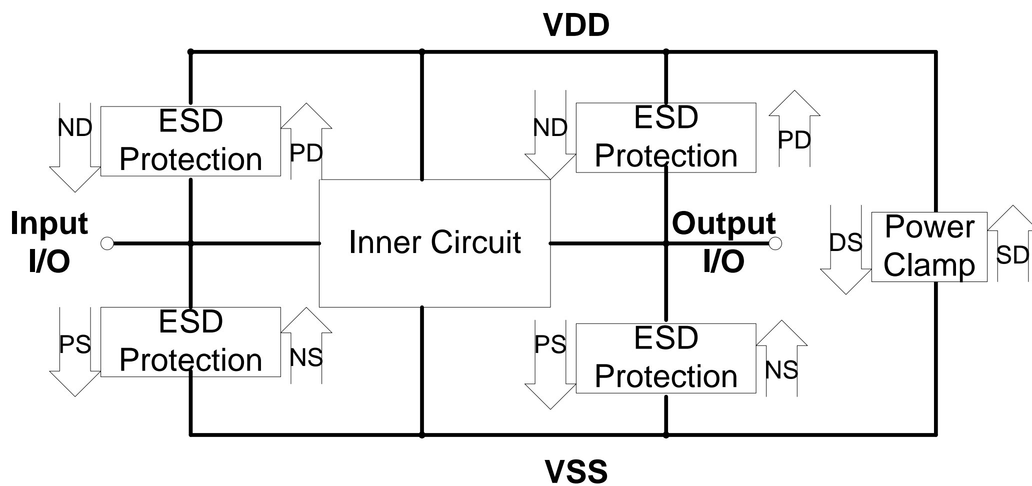


Figure 1.6 Full-chip ESD protection scheme

1.3 ESD Protection Structure

Various ESD protection structures have been developed and applied in different circuits and designs of IC technology. Commonly used ESD protection structures includes the simply turn-on type ESD protection structure in section 1.2, including STI diode, gated diode, and diode string, and snapback type ESD protection structure, including GGMOS (ground-gated MOS), SCR (silicon controlled rectifier), LVSCR (low voltage triggered SCR), DTSCR (diode triggered SCR) and so on.

1.3.1 Diode

There're two types of diode: STI diode and gated diode. As shown in Figure 1.7, STI diode contains a PN junction, which is formed by N+/P-Well in CMOS IC process. The forward PN junction has low on resistance and so very high current handle ability. And its triggering voltage V_{t1} is as low as ~0.7V.

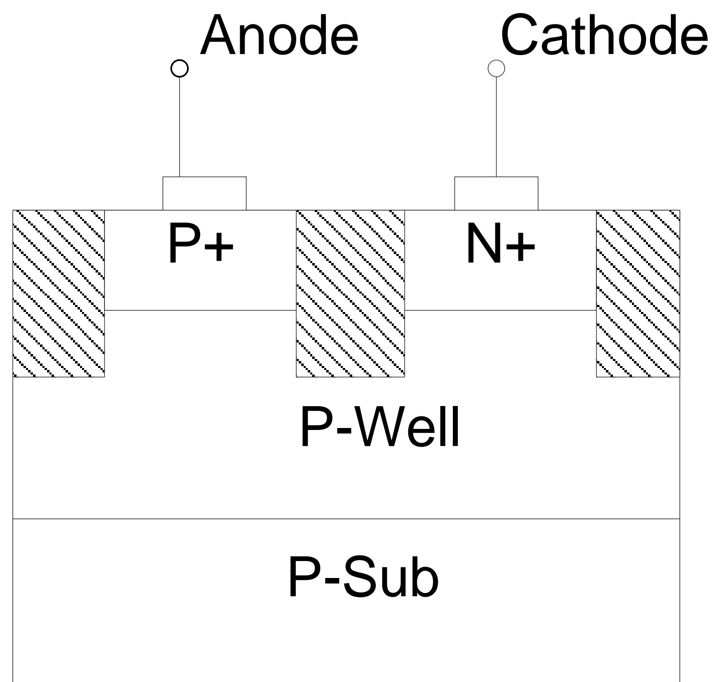


Figure 1.7 STI Diode N+PW cross-section

Figure 1.8 indicates the gated N+PW diode x-section. Gated diode also contains a PN junction, which is formed by N+/P-Well in CMOS IC process as STI diode. But gated diode has larger ESD current conduction ability since the current can go straightly through the channel between the N+ and P+ without any sharp turning and current crowding as seen in Figure 1.9.

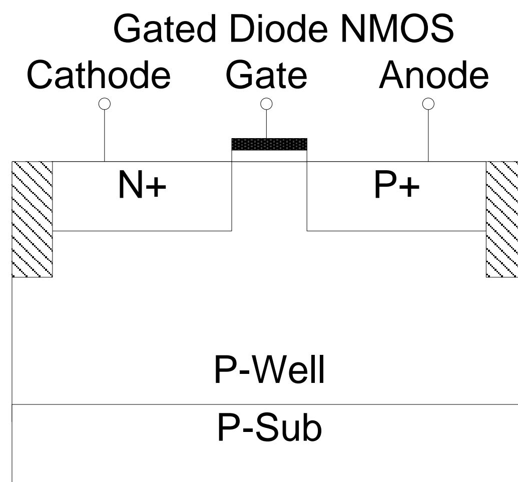


Figure 1.8 Gated Diode N+PW cross-section

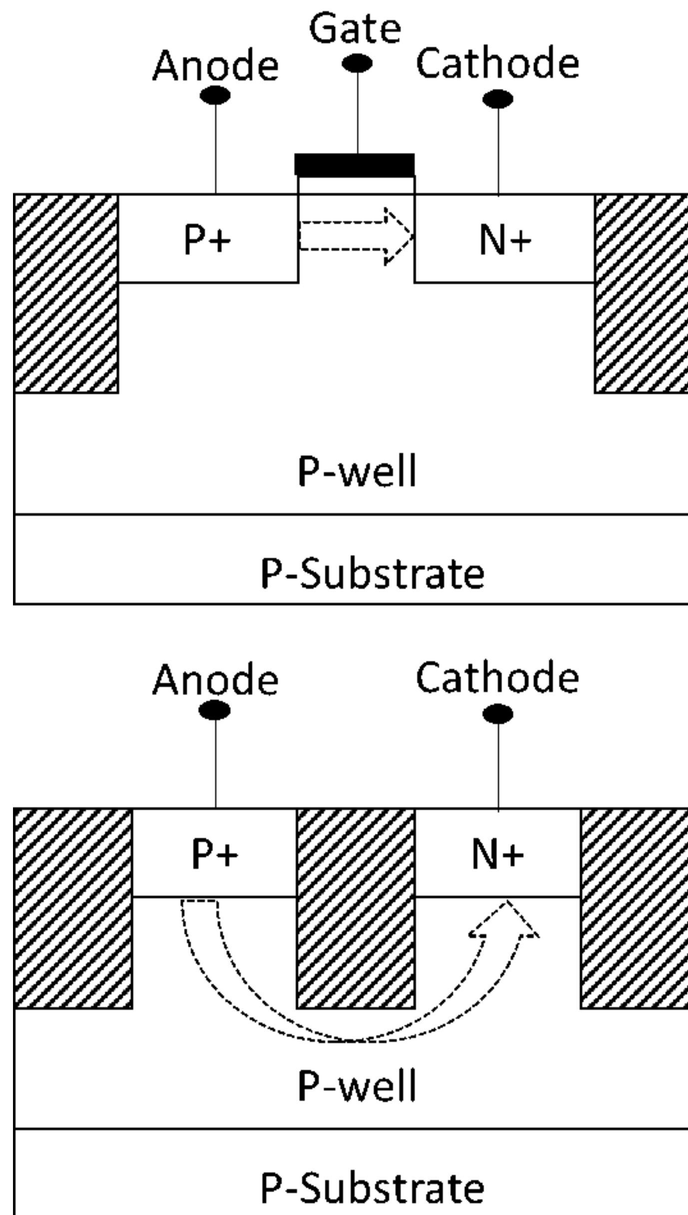


Figure 1.9 ESD discharge path for N+/P-well STI (upper) and poly-gated (lower) diode

1.3.2 Diode String

Figure 1.10 shows a diode string ESD protection structure, which has N (N=2) diodes isolated by deep N-well connected in series. The trigger voltage V_{t1} will be N multiplying single diode triggering voltage, and the diode string total parasitic

capacitance will be 1/N of the single diode. However, the total ESD discharging Ron of the diode string will be N multiplying the single diode Ron. In ESD protection circuit schematic, diode string could be placed at I/O ports to provide low parasitic ESD protection, and it could also be used as a power clamp, whose number of diodes should be decided by the power supply voltage.

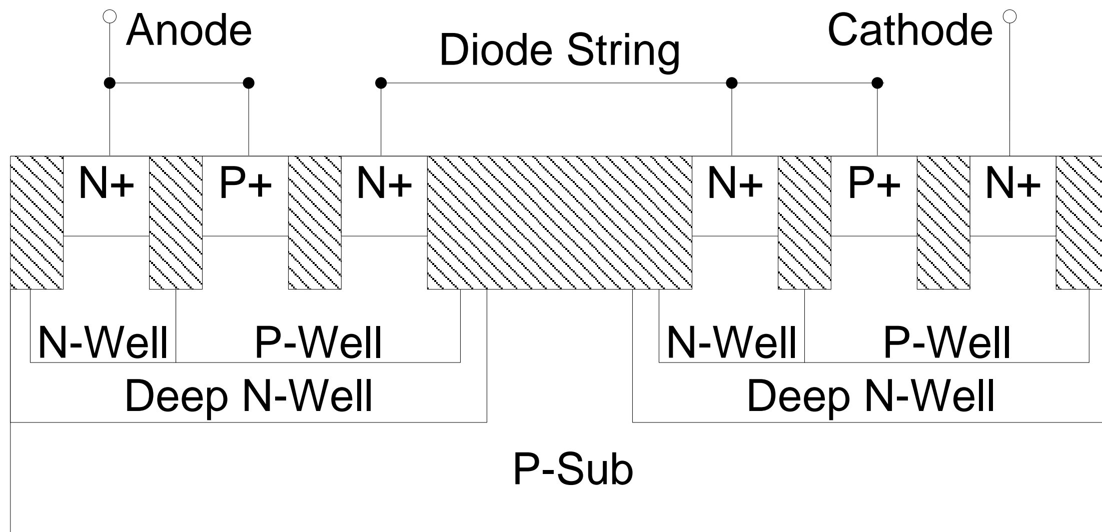


Figure 1.10 Diode string (N=2) cross-section

1.3.3 GGMOS

Gate-grounded NMOS transistor (GGNMOS) could be used as an ESD protection device. Figure 1.11 shows the cross-section and equivalent circuit of a GGNMOS. The drain is connected to anode, and the gate, source and bulk nodes are connected together to cathode.

The principle of a GGNMOS in ESD protection operation is as below. When a positive ESD transient pulse appears at the anode with respect to the cathode, the drain-bulk junction is reverse-biased all the way to its breakdown. Avalanche breakdown takes place and generates lots of electron-hole pairs. The hole current flows into the cathode

via the bulk-region and build up a potential, across the lateral parasitic resistance R. As the potential increases, the bulk-source junction turns on, eventually triggers the parasitic lateral NPN transistor. The parasitic bipolar is triggered into snapback region and the following active region, to shunt ESD current and clamp voltage at anode.

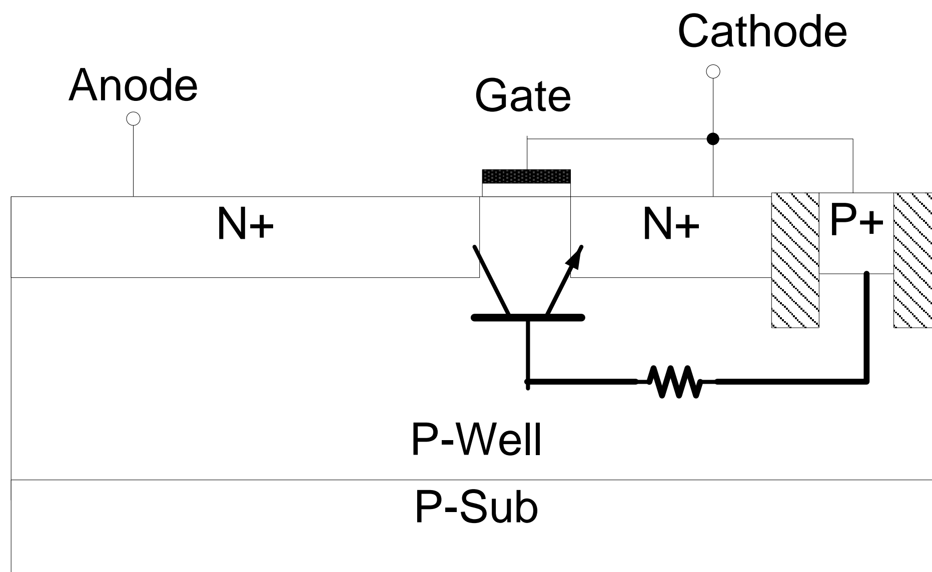


Figure 1.11 GGNMOS cross-section

PMOS could also be connected as GGPMOS for ESD protection. However, the parasitic PNP bipolar will be the discharging device in the GGPMOS. Another difference is the GGPMOS cathode will be tied to the power supply when it is placed in the circuits.

1.3.4 SCR

The silicon-controlled rectifier (SCR) ESD structure is attractive because it has high ESD protection efficiency. Figure 1.12 shown the cross-section and equivalent circuit of a SCR. The N+ and P+ in N-Well are connected to anode, and the N+ and P+ in P-Well are connected to cathode. There're two parasitic bipolar, Q1 and Q2, and two parasitic well resistors, $R_{N\text{-}Well}$ and $R_{P\text{-}Well}$ for the equivalent circuit of SCR. Q1 is a PNP

bipolar, which is formed by the P+ in N-Well, N-Well and P-Well, and Q2 is an NPN bipolar, which is composed of N-Well, P-Well and the N+ in P-Well.

When a positive ESD transient pulse appears from anode to cathode, the current from the N-Well/P-Well junction avalanche breakdown will generate a voltage drop on $R_{N\text{-}Well}$. With the increasing of the avalanche current, the voltage drop will be high enough to turn on Q1. The current from the collector of Q1 will go to the base of the Q2, and finally will turn on the Q2. Then, both of the bipolar will feed current from their own collector for the other one's base, thus the voltage on the anode will drop rapidly to the holding voltage V_h. The two bipolar will be in active region and start to discharge ESD current in a low-Resistance and clamp the voltage at the anode.

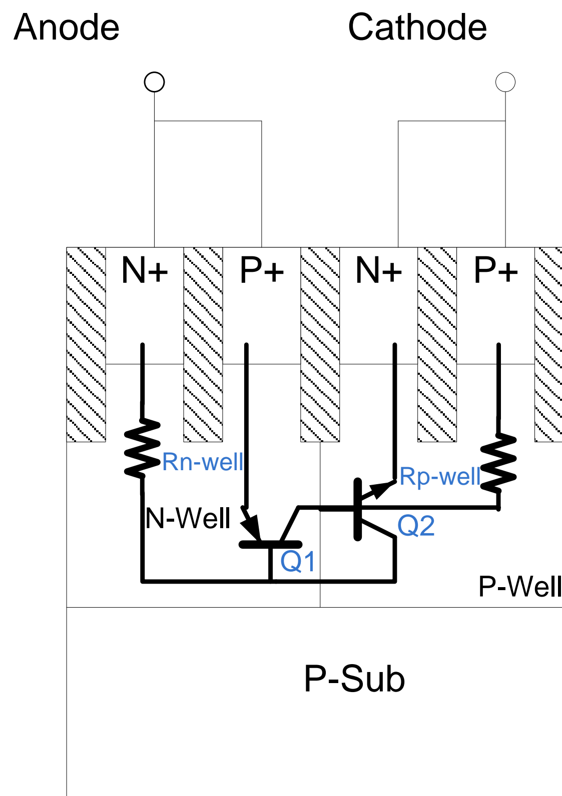


Figure 1.12 SCR cross-section

The drawback of SCR is that it has a high V_{t1} than those of other devices introduced above, due to the high avalanche breakdown voltage between N-Well and P-Well. Thus it will not meet the ESD design window. However, V_{t1} of SCR ESD structures may be reduced by different low-triggering mechanism.

The LVSCR ESD structure is a type of improvement for the low-triggering mechanism. Figure 1.13 depicts the LVSCR cross-section. The LVSCR structure is a normal SCR device with embedded short-channel NMOS to enhance ESD triggering. Since the NMOS drain breakdown voltage occurs first at a much lower voltage level than the normal N-well/P-well breakdown in a regular SCR structure, a LVSCR can be triggered at a much lower ESD V_{t1}. ESD triggering for a LVSCR can be reduced to V_{t1}=6~10V, suitable for advanced ICs.

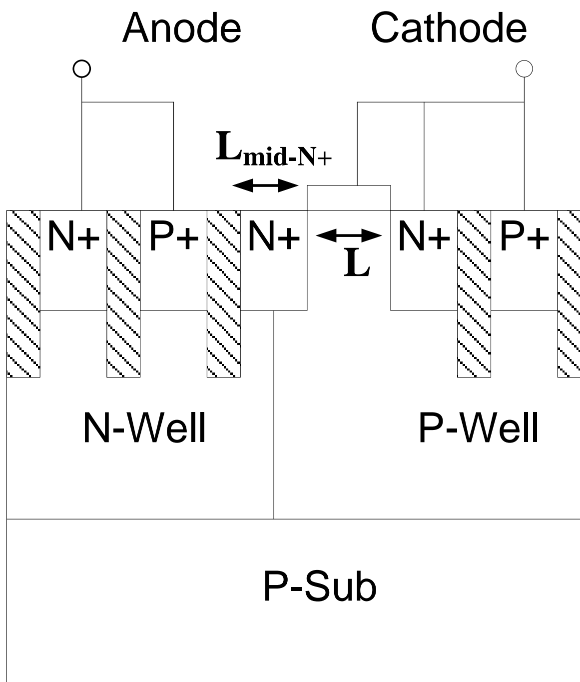


Figure 1.13 LVSCR cross-section

Diode triggered silicon controlled rectifiers (DTSCR) is another type of improvement for the low-triggering mechanism. It has become an attractive ESD protection device in advanced CMOS technologies due to their low capacitive loading and high failure current compared to diode based or NMOS based devices [31]. The DTSCR's tunable trigger/holding voltages offer design flexibility for a range of different I/O voltage requirements.

The DTSCR employs an external trigger diode chain to latch the device during ESD stress conditions as soon as the diode string injects enough current into the SCR gates G2, as shown in Figure 1.14. The triggering voltage V_{t1} of the DTSCR depends on the number of trigger diodes.

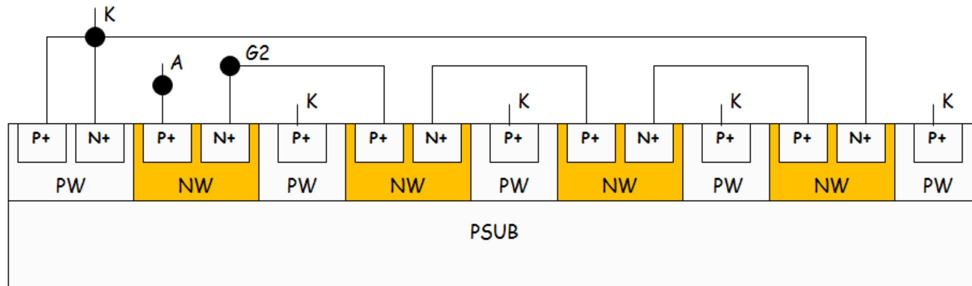


Figure 1.14 DTSCR cross-section with 3 trigger diodes.

1.4 Design Overview of Whole-chip ESD Protection CAD and Modeling

On-chip ESD protection solution development has drawn more and more attentions both in academic and industry, especially in developing ESD CAD tools and accurate ESD device models for practical ESD protection design verification.

Recent R&D efforts in ESD CAD may be classified in two types: Technology Computer-Aid Design (TCAD)-based [5-7] and ECAD-centric [8-10]. Physics-based numerical TCAD simulation has proven to be very useful in practical ESD protection

design at I/O cell scale. However, TCAD-based ESD protection design requires comprehensive and in-depth knowledge in device physics and process technology since TCAD simulator is a device-level simulation tool, which is often beyond the capabilities of IC designers. In addition, TCAD-based ESD protection design is very time consuming, computing expensive and not quite suitable for large-scale chip level simulation. On the other hand, ECAD-based ESD protection design verification has been limited to checking of ESD layout spacing, bus resistance checking, and so on, which cannot address ESD protection operation details quantitatively that is essential to achieving full-chip level ESD protection design verification and prediction as desired for RF/AMS IC designs.

Regarding to all these issues, we proposed the whole-chip ESD CAD tool as illustrated in Figure 1.15. This CAD tool is designed with several unique algorithms and a smart ESD parametric checking mechanism, which takes full consideration of ESD protection operation principles. It consists of three modules: ESD Extractor, ESD Inspector and ESD Zapper. ESD Extractor is a new function to extract arbitrary ESD structures at full chip level. Decomposed-based subgraph isomorphism algorithm is invented for ESD devices extraction to improve time efficiency. ESD Inspector is to remove non-critical ESD devices extracted based upon a novel smart parametric checking mechanism. In addition, ESD Zapper is developed to perform ESD protection zapping test simulation by implementing Dijkstra's algorithm to resolve the problem of finding the critical ESD discharging path.

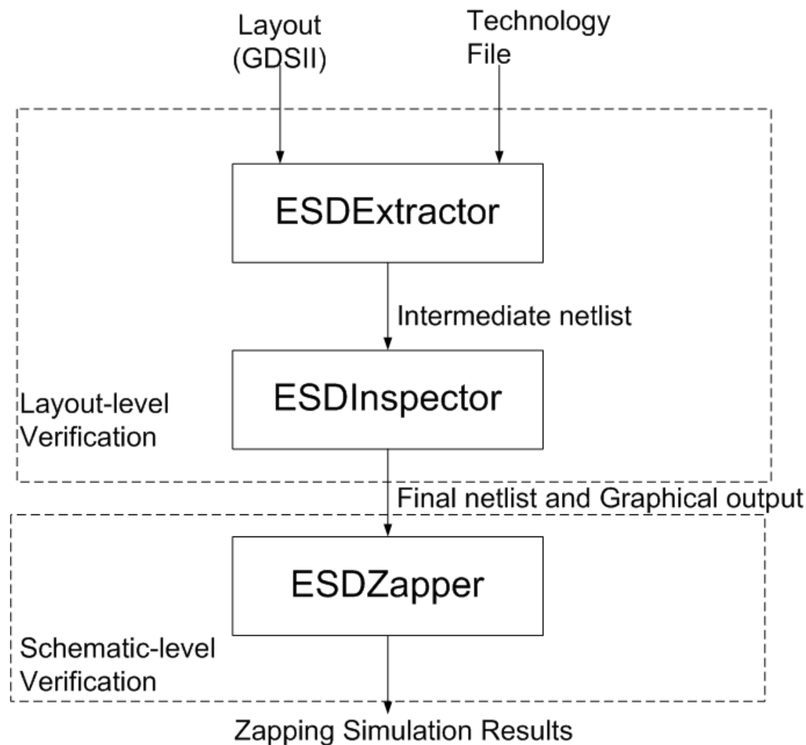


Figure 1.15 Illustration of the Whole-chip ESD CAD Tool

From the circuit design perspective, ESD Extractor and ESD Inspector realize layout-level verification, which provide IC designers a quick feedback after the physical layout design is completed and also provide the netlist for the schematic-level verification. ESD Zapper provides circuit designers complete simulation of the behavior of the whole chip circuit under ESD zapping of human body model (HBM).

HBM is one of the most-widely adopted ESD stress models in both academic and industry. HBM represents the process that the electrostatic charges storing in human body discharge to ground through IC parts when human body make a contact with the pins of the IC parts. This human body discharging process usually lasts several hundred nanoseconds and the peak current could reach to several amperes. The heat produced by

the human body discharging current will cause thermal breakdown damage in the IC parts if proper on-chip ESD protection structures are not available.

Typical HBM discharging current waveform has the main features as below: pulse rise time (t_r) is about 2 ~ 10nS; pulse duration time (t_d) is around 150nS, as shown in Figure 1.16 as defined in ESDA/JEDEC HBM standard [32]. Commercial HBM ESD testers must follow these rules of waveform, and waveform verification has to be done before the HBM test begins every day.

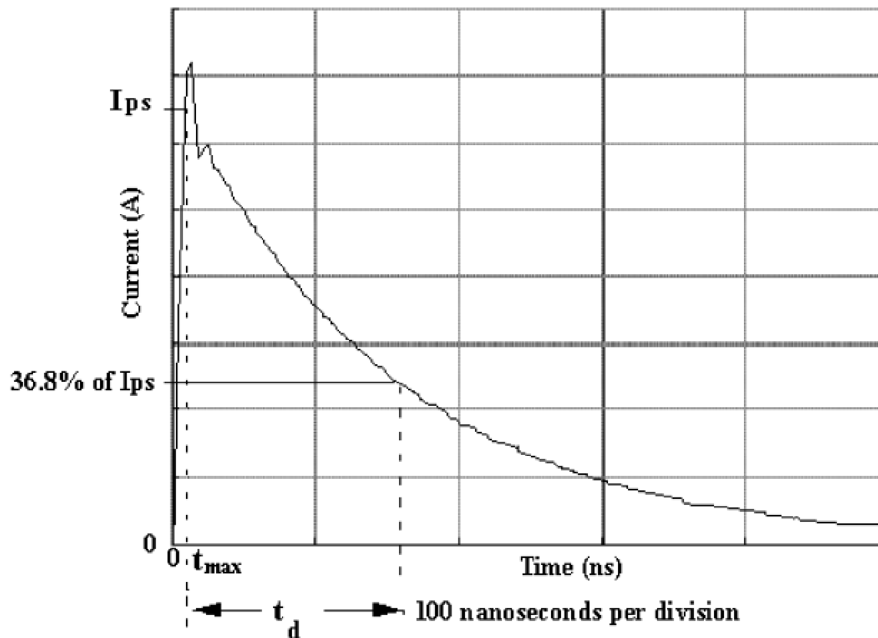


Figure 1.16 HBM current waveform

On the other hand, several ESD device modeling methods were reported for normal diode and MOSFET type of ESD protection devices based on the high current physical mechanisms [11-13]. However, due to the complexity of ESD discharging behaviors, i.e., the electro-thermal-process-device-circuit-layout coupling effects, existing ESD modeling approaches have limited accuracy in modeling complicated ESD

physical behaviors, such as thermal boundary conditions and snapback I-V behavior [1-3]. It is particularly challenging to develop physics-based ESD models for emerging nano ESD protection structures where the ESD protection mechanisms are still being investigated [14-17].

Regarding to all these modeling challenges, we proposed a new scalable ESD behavioral modeling technique as illustrated in Figure 1.17. The new ESD behavior modeling technique utilizes Verilog-A to describe complicated ESD discharging behavior, which enables accurate description of ESD device behaviors without being limited by the complex, and often unknown, ESD device physics. Firstly, the relationship between ESD-critical parameters and design splits must be established. After extracting ESD-critical parameters from TLP testing results and analysis, a scalability model per device dimensions can be set up. Next, the TLP curves are divided into several section-wise segments. Each segment of the TLP testing curve can be modeled by a formula to describe the corresponding ESD function in Verilog-A and the fitting parameters can be extracted from the TLP curve directly correlated with device dimensions. An accurate scalable ESD behavior model is then obtained, which must be verified by comparing SPICE circuit simulation with TLP testing.

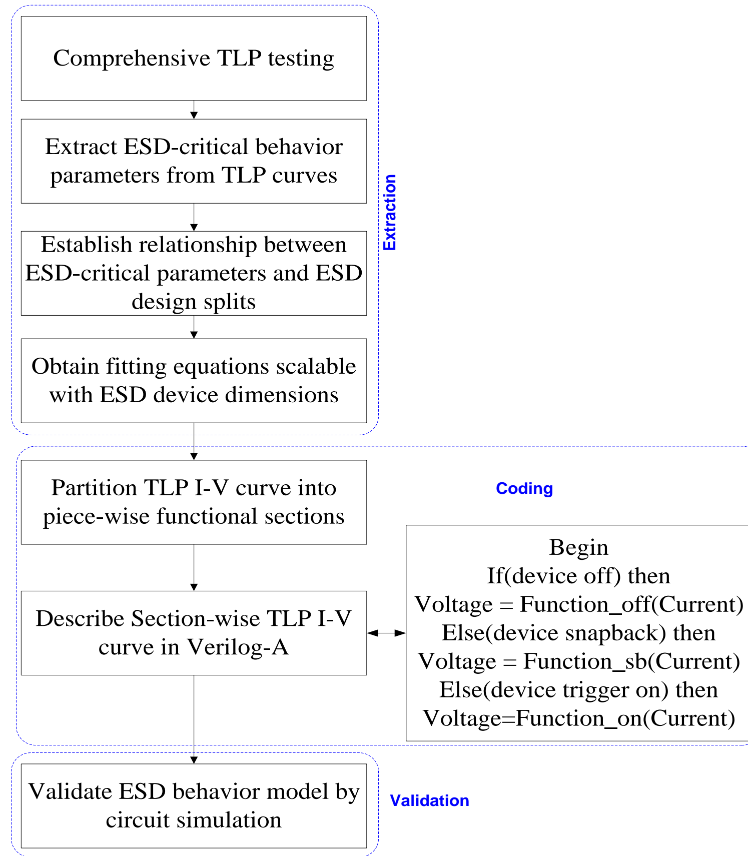


Figure 1.17 A flow chart of ESD behavior modeling.

From the device modeling perspective, behavioral ESD device modeling enables accurate description of ESD device behaviors without being limited by the complex, and often unknown, ESD device physics. It overcomes the difficulties to extract complicated parameters based on high current and thermal physics. It is relatively easy to achieve a semi-physical model to describe high current ESD device behaviors using behavior language Verilog-A. It is empirical since scalability with device dimensions for key ESD-critical parameters (V_{t1}, V_h) can be established by matching TLP testing with design splits. In addition, behavioral ESD modeling also contribute to ease the convergence problem often caused by avalanche breakdown.

Besides, flip chip technique using ball grid array (BGA) pad-ring arrays is a popular technology for small footprint chips used in size-sensitive electronics. However, ESD protection design for ICs using large BGA pad-ring array is an emerging challenge due to several reasons. First, unlike chips using wire bonding, ICs using BGA pad-ring arrays have constraints in on-chip ESD protection design where I/O pads, supply and ground (GND) pads are fixed in a given BGA pad-ring array determined by the chip performance. Hence, where to place an ESD structure becomes a real layout design headache. Second, with no layout flexibility for placing ESD structures in a BGA pad-ring array, ESD metal routing is very challenging that will seriously affect ESD protection performance at chip level. Between any given IO pad with an ESD protection structure underneath and a supply/GND pad with a fixed location, there will be many possible ESD metal routes. For a large chip using BGA pad-ring array, different ESD metal routing may significantly take effect on-chip ESD protection design due to the substantially different bus resistance associated with ESD metal routes even using the same ESD device for a given pad.

Regarding to all these BGA pad-ring array ESD protection challenges, we proposed a full-chip level verification using the new ESD Extractor CAD tool and new scalable ESD behavioral modeling technique. A BGA pad-ring array with different ESD metal routing for a VLC transceiver implemented in 180nm BCD technology was verified at whole-chip level. Two types of ESD were designed, one for the digital & analog domain (up to 5V) and the other for the power domain (up to 30V). The ESD structures and their ESD-critical parameters from full-chip layout design (GDSII data

file), were extracted by our ESD Extractor CAD tool. For accurate chip-level ESD protection circuit simulation, the ESD metal bus resistance was extracted by ESD Extractor tool. The geometrical dimension width and length of ESD metal interconnects are extracted from the layout file and the bus resistance can be calculated according to related metal sheet resistivity and layout data. The new ESD behavior modeling technique was used to model the GCNMOS ESD structures fabricated in this work to enable whole-chip ESD circuit design simulation and verification. It utilizes Verilog-A language to describe ESD-critical parameters extracted from ESD Extractor CAD tool. The extraction and modeling was validated by SPICE simulation and TLP testing for different ESD metal routing.

1.5 Thesis Organization

This thesis consists of 5 chapters.

Chapter 2 will treat the implementation of whole-chip ESD CAD tool. First, challenges for ESD device extraction will be studied. Then novel algorithms and the implementation methods for ESD Extractor are presented. The necessity of developing ESD Inspector is discussed and then a novel concept of smart parametric checking is proposed along with a set of reduction criteria. ESD zapper is designed according to ESD protection design critical task of simulating the complex, time-consuming ESD zapping test at whole-chip level. The algorithm and implementation for ESD zapper is also provided. To the end, full chip ESD protection application example was designed and verified the CAD tool implemented in 0.35 μm BiCMOS technology.

Chapter 3 focuses on new accurate and scalable behavioral modeling method. The modeling method is explored on novel ESD protection structures, such as nano crossbar, novel 3D field-programmable ESD protection structures including SONOS and NCD ESD devices firstly. Then it's applied to traditional ESD protection structures, for example SCR, HV diode, gated diode and DTSCR. For each kind of ESD protection structure, the ESD behavior models were developed from ESD testing results and verified in SPICE circuit simulation.

Chapter 4 will be dedicated to a BGA pad-ring array with different ESD metal routing for a VLC transceiver implemented in 180nm BCD technology full-chip verification. The ESD structures and their ESD-critical parameters, and the ESD metal bus resistance were extracted by our new ESD Extractor CAD tool. The new ESD behavior modeling technique was used to model the ESD structures. The extraction and modeling was validated by SPICE simulation and TLP testing for different ESD metal routing.

Chapter 5 will conclude with the main contributions and achievements of the presented work, and some suggestions for future research.

Chapter 2 Whole-chip ESD CAD Tool

2.1 Introduction

In this chapter, we proposed the whole-chip ESD CAD tool as illustrated in Figure 1.15. This CAD tool is designed with several unique algorithms and a smart ESD parametric checking mechanism, which takes full consideration of ESD protection operation principles. It consists of three modules: ESD Extractor, ESD Inspector and ESD Zapper. ESD Extractor is a new function to extract arbitrary ESD structures at full chip level. Decomposed-based subgraph isomorphism algorithm is invented for ESD devices extraction to improve time efficiency. ESD Inspector is to remove non-critical ESD devices extracted based upon a novel smart parametric checking mechanism. In addition, ESD Zapper is developed to perform ESD protection zapping test simulation by implementing Dijkstra's algorithm to resolve the problem of finding the critical ESD discharging path.

2.2 ESD Extractor

To enable ESD-function-based whole-chip ESD protection design verification at layout level, ESD Extractor CAD module is critical since it’s the very first step in any design verification. Several challenges exist for ESD protection device extraction tool as follow [51]. Firstly, extraction of ESD protection device is different from that regular IC devices since ESD protection circuits often use unconventional devices. Conventional IC devices, such as MOSFET and BJT, can be extracted using basic Boolean operation of layout features, while ESD protection devices usually have very complicated and

irregular layout patterns [24]. Secondly, to fully address the complicated parasitic ESD failure problem, good ESD device extraction method must be able to extract all possible parasitic ESD-like devices within the whole chip, since ESD transient current often causes the turn-on of parasitic ESD-like devices before the desired intentional ESD devices may be triggered and results in pre-mature ESD failure at chip level. The ESD netlist generated by the ESD Extractor should contain all ESD-type devices possibly being turned on under an ESD pulse, whether it is an intentionally designed ESD protection device or a parasitic ESD-like device. Therefore, the ESD Extractor is designed to have the capability of extracting any possible ESD-type structures and their ESD-critical parameters from full-chip layout design.

2.2.1 Design Overview of ESD Extractor

Figure 2.1 shows the flow chart for ESD Extractor, a new CAD tool that is capable of extracting arbitrary ESD-like devices of any structure and takes full consideration of both intentional and parasitic ESD-type device, which consists of three execution steps: (1) to read the device definition in the technology file and save it in the model database; (2) to save the layout data into the layout database after necessary prepossessing; (3) to identify all possible ESD-type devices with their ESD-critical parameters, intentional or parasitic, in the extraction engine. The output data is sent to the next module, ESD Inspector, to remove non-critical ESD devices extracted.

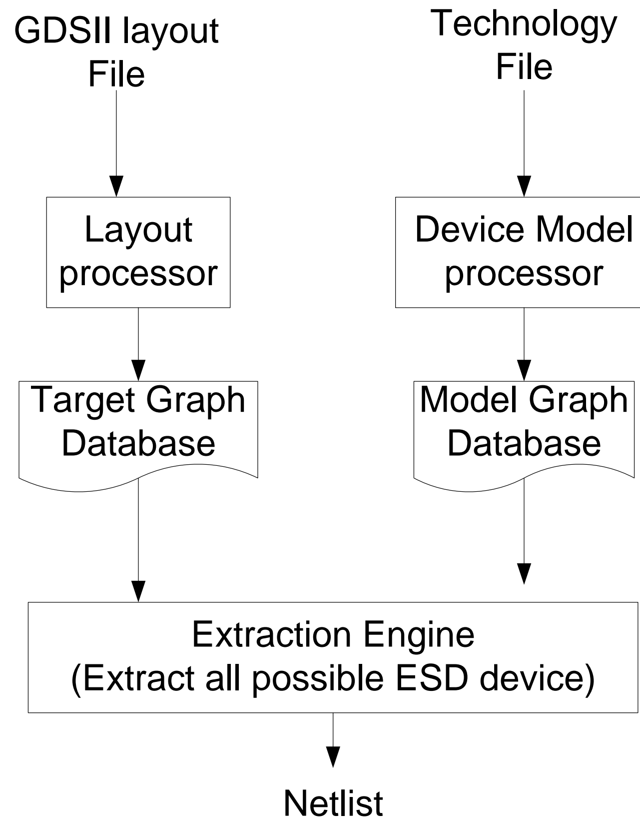


Figure 2.1 Flow chart for ESD Extractor

2.2.2 Layout Processor

IC layout is a geometrical description of masks in GDSII format, so it's necessary to have a layout processor to transform the input GDSII layout file into graph data structures and save them in the target graph (TG) database as shown in Figure 2.1.

GDSII layout file contains a set of graphical geometries situated on separate mask layers as illustrated in Figure 2.2 (a), which includes two partly overlapping polygons situated in two separate mask layer Poly and P-plus. To avoid using more computationally expensive geometrical operations (such as include, intersect, surround, divide), all the input geometries in all mask layers are first merged together and then

partitioned into non-overlapping regions, as shown in Figure 2.2 (b) the layout is partitioned into 6 non-overlapping regions [49].

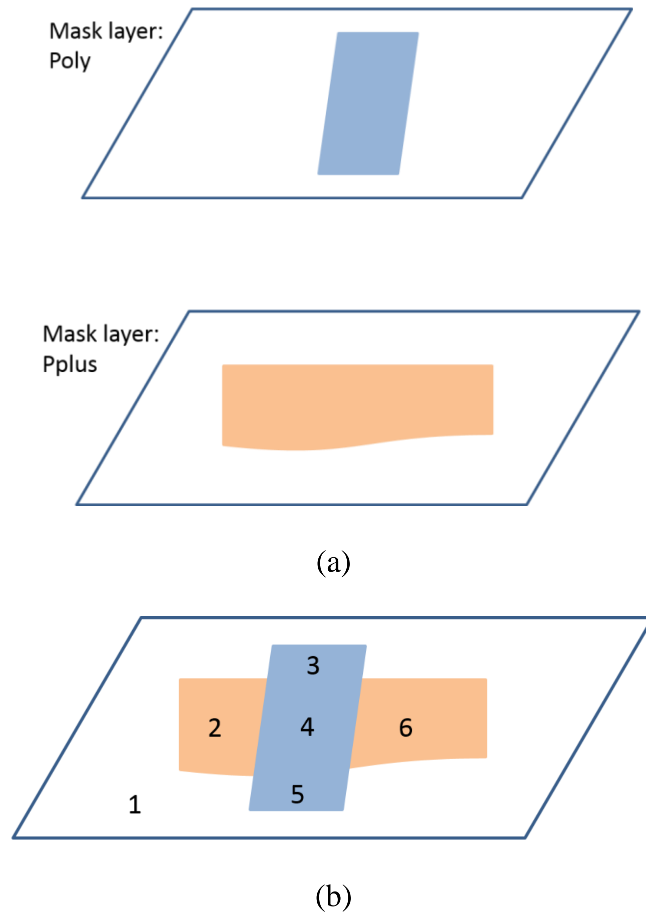


Figure 2.2 Layout processing example

In our design, each region is a simple polygon consisting of a set of stacked mask layers, where the presence and absence of mask layers are described in the program as mask values, which use a bit mask code word, with “1” representing the presence of that layer and “0” indicating the absence of the mask layer. Therefore, a mask value code of all “0’s” represents the bare wafer substrate without any other IC physical layers.

For the inner geometrical presentation, the target layout graph (TG) data structure are used to indicate the GDSII layout file. A TG consists of a finite set of vertices, where

each vertex corresponds to a non-overlapping region and a set of edges joining the vertices with each edge representing an adjacency relationship existing between a pair of the vertices. The TG for the layout design in Figure 2.2 is shown in Figure 2.3, where each circle represents a vertex for TG and the solid lines represent the edges for TG.

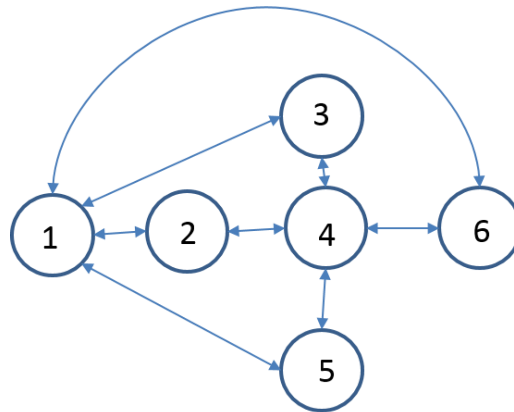


Figure 2.3 TG for the layout design example in Figure 2.2

2.2.3 Device Model Processor

There're many ESD device types including the classic GGNMOS, GCNMOS, BJT, diode and SCR, as well as any novel ESD protection structures. Hence, each device type is described by a unique device model graph (MG). An adjacent list graph structure is adopted for device model graph definition. The structure of a MG is defined as MG (V, E). The attribute V is a set of vertices with each vertex corresponding to a non-overlapping region with a specific mask value. The attribute E is a set of relationships between two different vertices of the device model, which includes geometrical adjacency relationship and electrical connectivity relationship for ESD protection. Hence, a complete set of vertices form a device model, MG. The part in dashed box shown in Figure 2.4(a) is the cross-section for GGNMOS without guard-ring and pick-ups, with its

layout indicated in Figure 2.4(b). A MG for it is shown in Figure 2.4(c), where each circle represents a vertex of the MG, the solid lines represent geometrical adjacency relationship R1 and the dashed lines represent electrical connectivity R2.

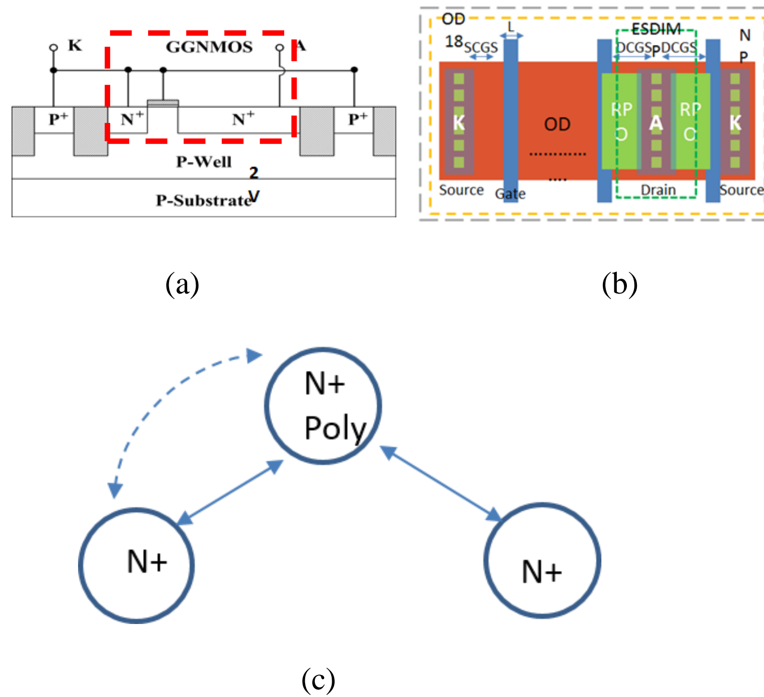
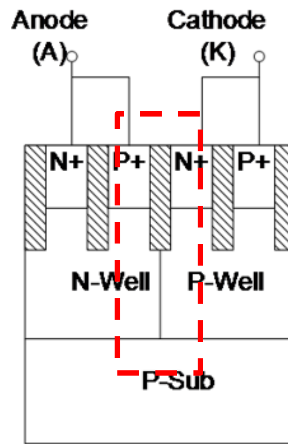
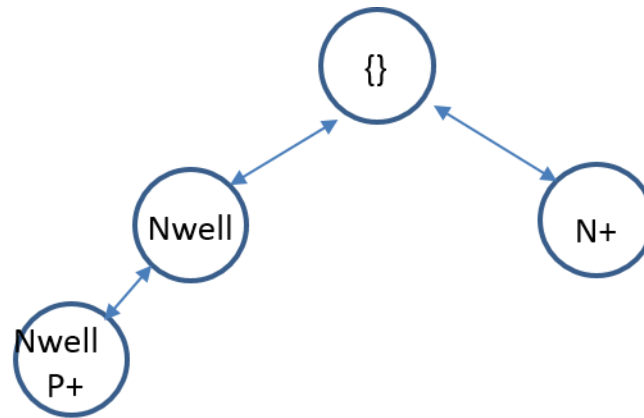


Figure 2.4 GGNMOS (a) cross-section (b) layout (c) MG definition

Figure 2.5 illustrates an SCR ESD device with pick-ups. So the part in dashed box without pickups is selected as MG for SCR ESD device. This SCR MG definition ensures that each parasitic ESD-type SCR device will be extracted.



(a)



(b)

Figure 2.5 SCR (a) cross-section (b) MG definition

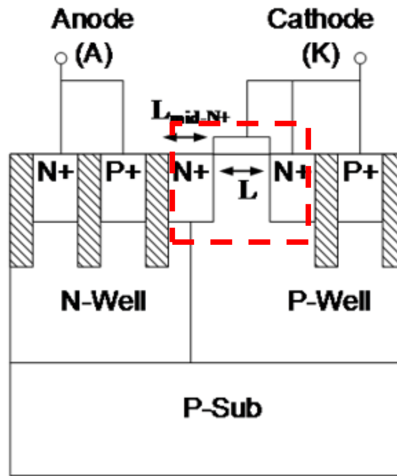
2.2.4 Device Recognition Algorithm

Since the whole IC layout data is presented as a target graph and each device type is described by a unique device model graph, a device is identified by matching one section of the target graph with one of the model graphs. So we propose a decomposition-based subgraph isomorphism technique to recognize arbitrary ESD protection structures.

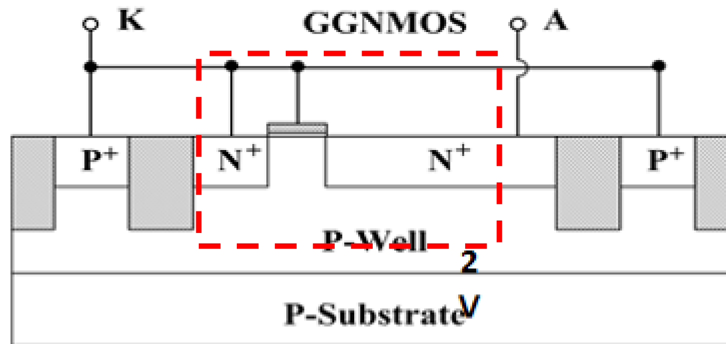
We want to find all subgraph isomorphism from any of the models to the input graph. Under a naive strategy, some reported device extractors [26, 27] use a top-down

approach, which would match the input graph sequentially to each model using. The main disadvantage of this approach is that it is linearly dependent on the number of model graphs [25].

However, an ESD protection device extractor has its own special requirement. Firstly, there're many ESD device types including the classic GGNMOS, BJT, diode and SCR, as well as any novel ESD protection structures, e.g., a dual-direction SCR ESD protection device [21]. Besides, another unique feature of ESD protection devices is that different ESD protection structures may share common layer elements. For example, LVSCR and GGNMOS share common elements shown in Figure 2.6 .



(a)



(b)

Figure 2.6 (a) LVSCR cross-section, (b) GGNMOS cross-section

According to the unique features of ESD protection devices, we propose a new device recognition algorithm based on a decomposition approach to improve ESD device recognition efficiency. Unlike the top-down approach [26, 27] that handles each MG individually, our algorithm first explores the relationship between the device MGs by a decomposition procedure. The main advantage of this scheme is that the common part of any two or more MGs will only be matched for once, which makes the device recognition

procedure not heavily dependent upon the number of device MGs as does the top-down approach. Meanwhile, in our new approach, model containment relationship can be explicitly expressed. Hence, any redundant device, i.e., the small device like GGNMOS contained in a larger device LVSCR, can be easily removed from the final result, thus eliminates the necessity of developing an individual redundant device processor and improves the computing time efficiency in ESD protection device recognition.

The device recognition algorithm consists of two steps: model decomposition and device recognition. Firstly, different device MGs are recursively decomposed and the decomposition results, D (M), are saved by a special inner data structure. Secondly, the TG is matched with D (M).

The decomposition result of MG, D(M), is a set of tuple data structure as T(G, lG, rG, E, ifModel, ifCheck), where G, lG, rG are graphs; lG is left subgraph of G; rG is right subgraph of G; E is a set of edges between lG and rG to construct G. ifModel is a Boolean variable. If ifModel = true, G is corresponding to a device model. IfCheck is a Boolean variable. If ifCheck = true, G may contain another MG, directly or indirectly. Decomposition procedure is shown in Figure 2.7.

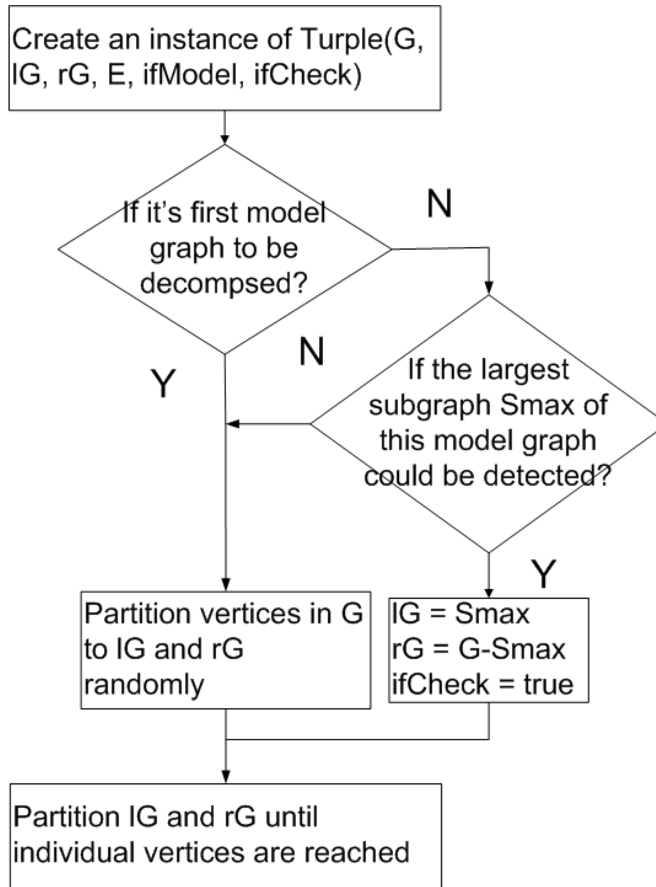
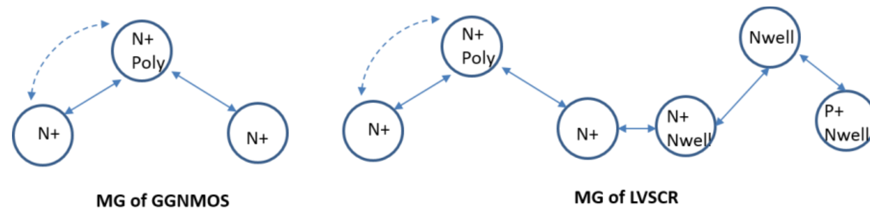


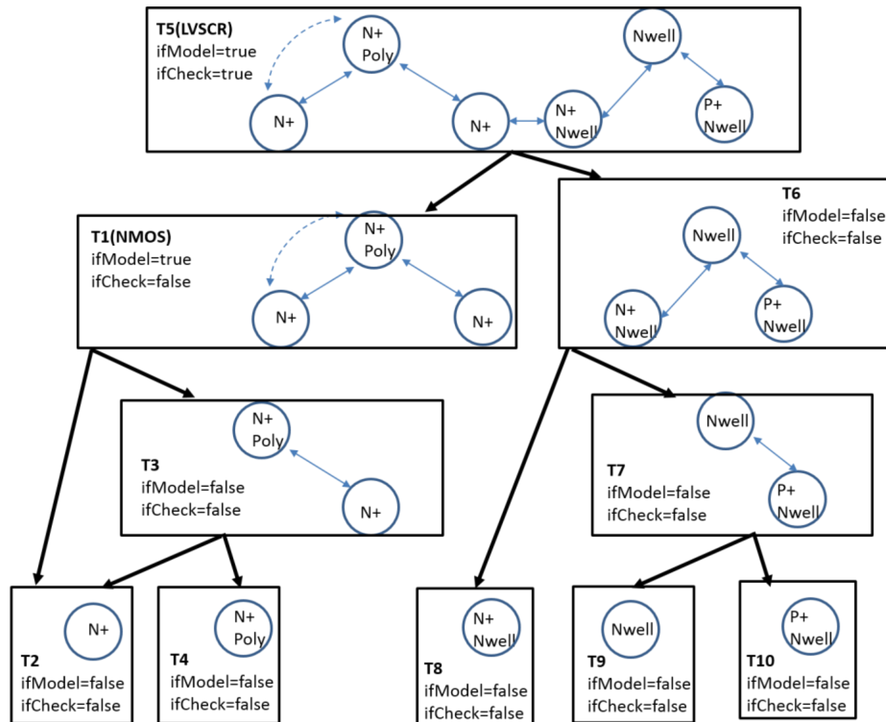
Figure 2.7 Flow chart of decomposition procedure

Figure 2.8 illustrates the MGs for a GGNMOS and LVSCR ESD protection device. Let MG1 = GGNMOS and MG2 = LVSCR, the decomposition result, T1~T10 in D (M), is shown in Figure 2.8 (b). From the decomposition procedure, the GGNMOS is first decomposed into two parts, with the left subgraph, lG, being T2 and the right subgraph, rG, being T3. Because the lG contains only one vertex, it will not be decomposed any more. The rG will be further decomposed into two parts. The decomposition results of the GGNMOS are saved in D (M) as T1~T4. Now the LVSCR is decomposed. Firstly, the largest subgraph in D (M), Smax, is first searched in D (M) whose contents are now T1~T4, and the result is T1 (GGNMOS). Then the LVSCR will

be decomposed into two parts, with lG to be T1 (GGNMOS) and the leftover parts as rG to be T6. Next, the algorithm further decomposes the right subgraph of LVSCR as T6, with results of T7~T10. The common subgraph of GGNMOS and LVSCR, GGNMOS as T1, is saved only once in D (M). In addition, for the LVSCR (T5), ifCheck = true makes sure that redundant device is removed in the device recognition stage.



(a)



(b)

Figure 2.8 Model Decomposition Procedure for GGNMOS and LVSCR

Instead of matching each MG individually to a TG, the device recognition procedure is shown in Figure 2.9. Firstly, it finds all individual vertices of the D (M) within the TG and then gradually combine them into larger subgraph isomorphism. In order to keep track of the components that have been matched already with the TG, each member in D (M) can be marked with one of three different tags. In the beginning, all members in D (M) are marked unsolved. As soon as a member has been tested for subgraph isomorphism with the TG, it is either marked alive or dead. If the search for subgraph isomorphism was successful, then the member is marked alive and all detected subgraph isomorphism are associated with it using hash map. Otherwise, the subgraph is marked dead and no subgraph isomorphism are associated with it. This process continues until either all members in D (M) have been tested or no member can be found for which both subgraphs are marked alive.

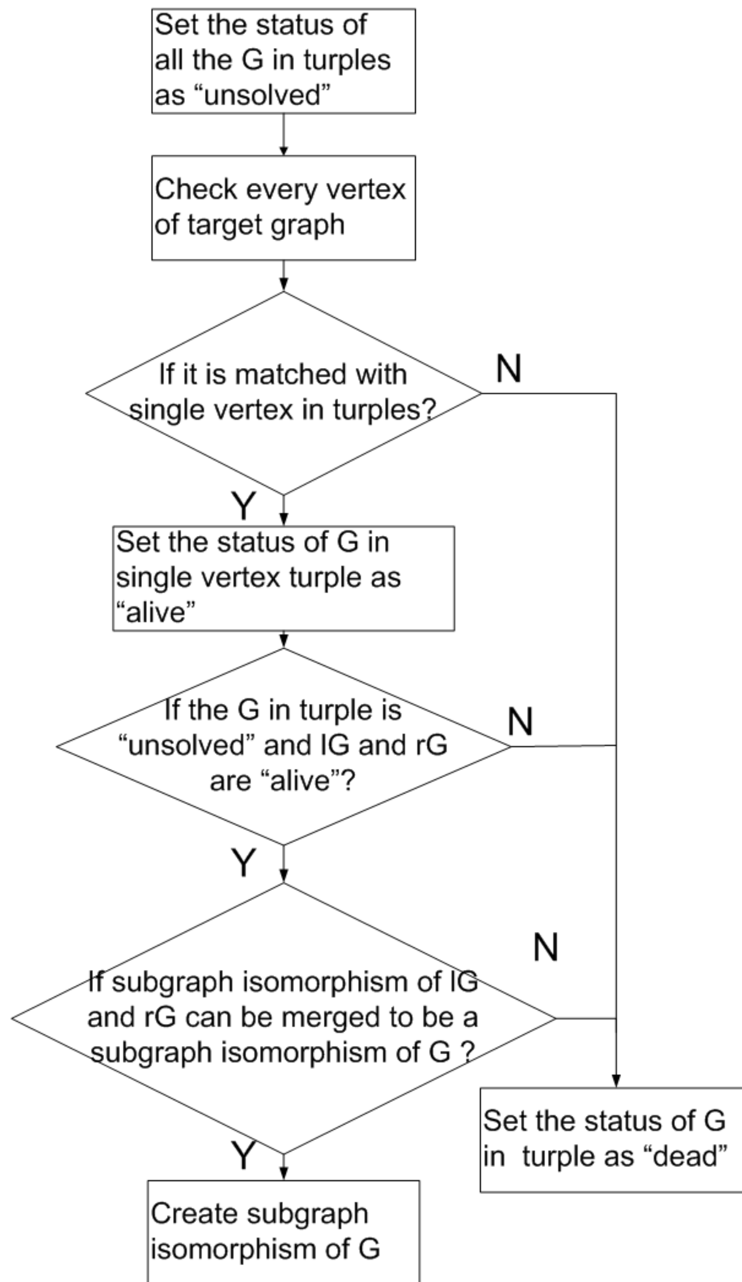


Figure 2.9 Flow chart of Device Recognition procedure

For the time complexity, the top-down approach is O (NIM), in which N is the number of the model graphs, I is the number of vertices in the target graph, and M is the total number of vertices of model graphs. Compared to that, if all model graphs are

identical for the extremely situation, the decomposition-based subgraph isomorphism approach has the time complexity of O(IM), which heavily improves the time efficiency by N times than the top-down approach.

2.3 ESD Inspector

The ESD extractor extracts all intentional and parasitic ESD devices from a layout file, however, the number of the ESD devices are so large that it will take effect to the time efficiency for the schematic level simulation. Therefore, it is critical to identify those life-threatening ESD-type parasitic devices that designers should really concern. Therefore, a new CAD tool module of ESD Inspector is developed to remove non-critical ESD devices extracted based upon a novel smart parametric checking mechanism.

2.3.1 Design Overview of ESD Inspector

The goal of ESD Inspector is to remove non-critical ESD devices extracted and to generate an input deck for schematic-level simulation. Different from other ESD physical design checking tools reported, ESD Inspector use a new smart ESD parametric checking mechanism [28]. İt is observed that the behavior of all kinds of ESD devices, including intentional or parasitic can be described by some important quantitative parameters. Such ESD-critical parameters include triggering (V_{t1}, I_{t1}), holding (V_h, I_h), discharging (R_{ON}) and thermal breakdown (V_{t2}, I_{t2}), etc., which is introduced in Section 1.2. Figure 2.10 illustrates the combined functional flow chart for the ESD Extractor and ESD Inspector.

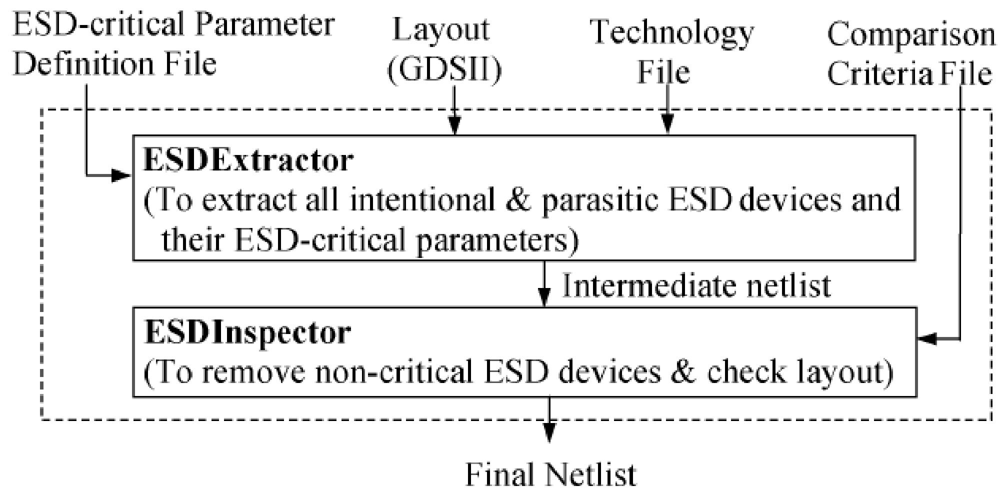


Figure 2.10 Flow chart for ESD Extractor and ESD Inspector.

2.3.2 Smart Parametric Checking Mechanism

Considering all possibilities in the ESD protection combination, the new smart parametric checking mechanism defines a group of ESD-critical parameter checking criteria [33].

Assuming a case of two ESD devices, A and B, in series. Then the total series triggering voltage, V_{t1}, will be estimated first, by $V_{t1}A+V_{t1}B$.

Assuming a case of two ESD devices, A and B, in parallel. Several criteria is described as below. (1) Triggering criteria: If ESD devices A and B are in parallel and V_{t1} of A is much higher than V_{t1} of B, then device A is a non-critical ESD device and could be removed. (2) Holding criteria: If ESD devices A and B are connected in parallel and A has a higher V_h than B does, then A is a non-critical ESD device and will be removed. (3) R_{ON} criteria: If ESD devices A and B are in parallel and have comparable V_{t1}, but R_{ON} of A is much larger than that of B, then device-A may not discharge the ESD current and could be removed.

As more about the ESD protection behavior is understood and any novel ESD protection mechanisms are discovered, more ESD-critical parameter based smart parametric checking criteria can be added in practical ESD layout design verification. However, the fundamental smart parametric checking mechanism remains the same as we discussed as above.

The smart parametric checking mechanism is used to remove non-critical ESD devices and to generate critical ESD devices netlist using ESD Inspector after extraction of ESD devices and ESD-critical parameters, which take effect to the time efficiency for the schematic level simulation.

2.4 ESD Zapper

Successful on-chip ESD protection design must use the whole-chip ESD protection design approach because of complex ESD circuit has interaction effects with core circuit, compared to traditional design practices that often treat ESD protection design as stand-alone ESD protection structure. Figure 2.11 shows an example for a whole chip ESD stress scenario. While an ESD discharging path between the PADs is designed (solid line), parasitic conducting paths may conduct the current (dash line) and result in early ESD failure.

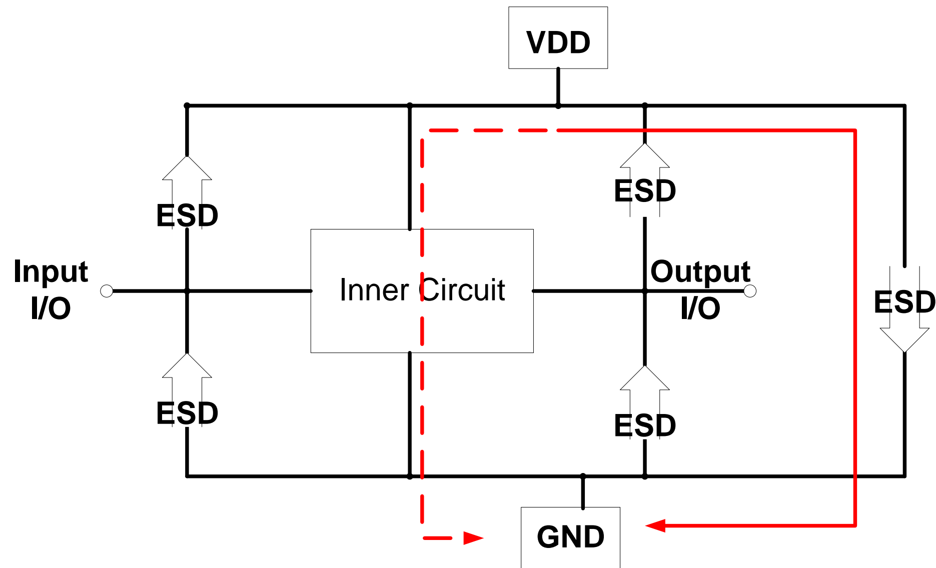


Figure 2.11 whole chip ESD stress scenario

Therefore, one important problem to resolve for whole-chip ESD protection circuit design verification is to identify the critical ESD discharging paths on a chip, which considers all possible ESD-type devices including designed ESD structures and parasitic ESD type devices. Hence, ESD zapper is designed to achieve whole-chip ESD protection design verification and prediction, since this module is developed to perform whole-chip checking to identify critical ESD discharging paths.

2.4.1 Design Overview of ESD Zapper

Figure 2.12 shows the flow chart of ESD Zapper. As described in section 2.2 and 2.3, after complete ESD extraction operation by ESD extractor and device reduction by ESD Inspector, the output ESD netlist is the input to the ESD Zapper. Also zapping condition including the pad combination is the input for the ESD Zapper. The ESD netlist is transformed to a novel weighted graph, where the ESD protection circuit is described as a weighted graph with each electrical node corresponding to a vertex and each ESD

device being an edge of the graph. Then critical ESD discharging paths between pads are found using Dijkstra's algorithm, which finds the shortest paths between nodes in a graph [50].

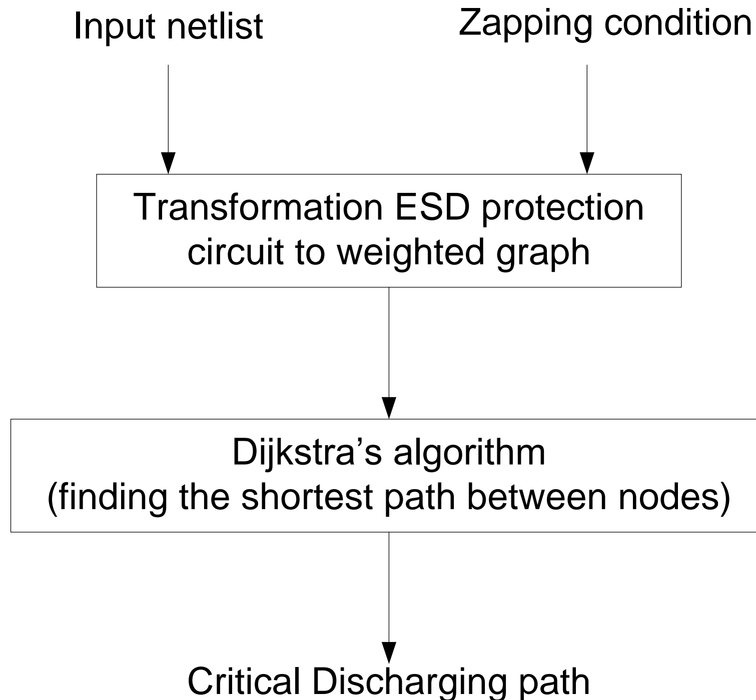
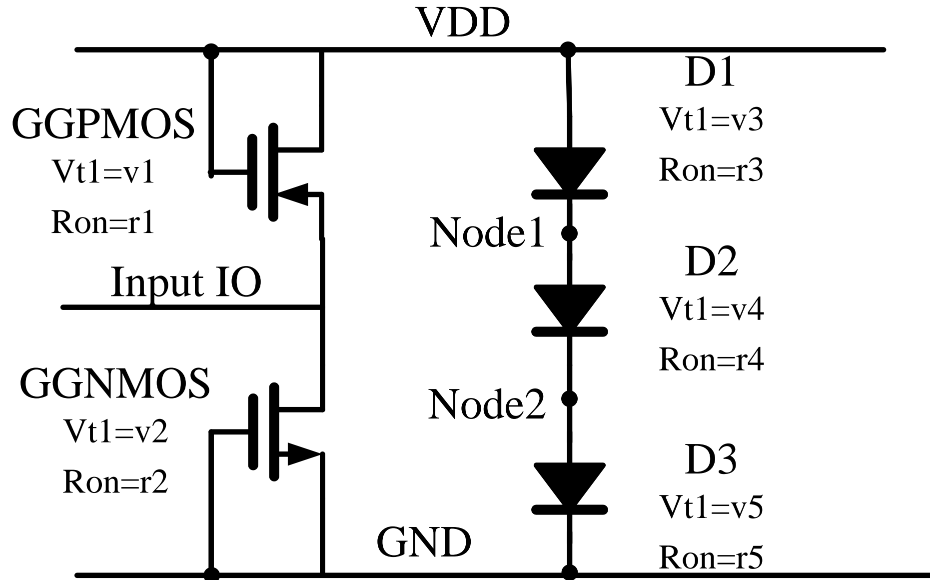


Figure 2.12 Flow chart for ESD zapper

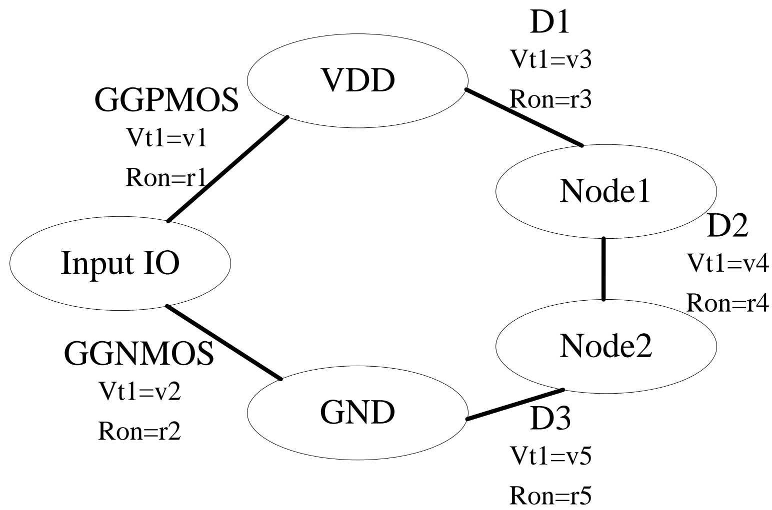
2.4.2 Critical Discharging Path Algorithm

The ESD protection circuit is described as a weighted graph with each electrical node corresponding to a vertex and each ESD device being an edge of the graph. The ESD-critical parameters of each device are assigned to the corresponding edge as its weight. Figure 2.13 illustrates an example circuit with ESD protection (a), consisting of GGNMOS and GGPMOS as the input IO ESD protection, and diode string as power clamp, and its corresponding weighted graph (b). Then the critical discharging path can

be found by finding the path with the smallest weight between two given vertices, for example VDD and GND.



(a)



(b)

Figure 2.13 Example for (a) ESD protection circuit (b) transformed weighted graph

There are many developed algorithms we can choose to find the shortest path in the graph, such as Dijkstra's algorithm, the Bellman–Ford algorithm, and Prim's algorithm. Considering the feature of weighted graph in this problem, which does not include negative edge weights and is concerned with only two nodes, Dijkstra's algorithm is selected to find the shortest path.

Figure 2.14 shows the flow chart of Dijkstra's algorithm. Let the node at which we are starting be called the initial node. Let the distance of node Y be the distance from the initial node to Y. Dijkstra's algorithm will assign some initial distance values and will try to improve them step by step. Firstly, assign to every node a tentative distance value: set it to zero for our initial node and to infinity for all other nodes. Secondly, set the initial node as current. Mark all other nodes unvisited. Create a set of all the unvisited nodes called the unvisited set. Thirdly, for the current node, consider all of its unvisited neighbors and calculate their tentative distances. Compare the newly calculated tentative distance to the current assigned value and assign the smaller one. For example, if the current node A is marked with a distance of 6, and the edge connecting it with a neighbor B has length 2, then the distance to B (through A) will be 6 + 2 = 8. If B was previously marked with a distance greater than 8 then change it to 8. Otherwise, keep the current value. Fourthly, when we are done considering all of the neighbors of the current node, mark the current node as visited and remove it from the unvisited set. A visited node will never be checked again. Fifthly, if the destination node has been marked visited (when planning a route between two specific nodes) or if the smallest tentative distance among the nodes in the unvisited set is infinity (when planning a complete traversal; occurs

when there is no connection between the initial node and remaining unvisited nodes), then stop. The algorithm has finished. Finally, select the unvisited node that is marked with the smallest tentative distance, and set it as the new "current node" then go back to step 3. Time complexity of Dijkstra's algorithm is O (n^2), where n is the number of the vertices.

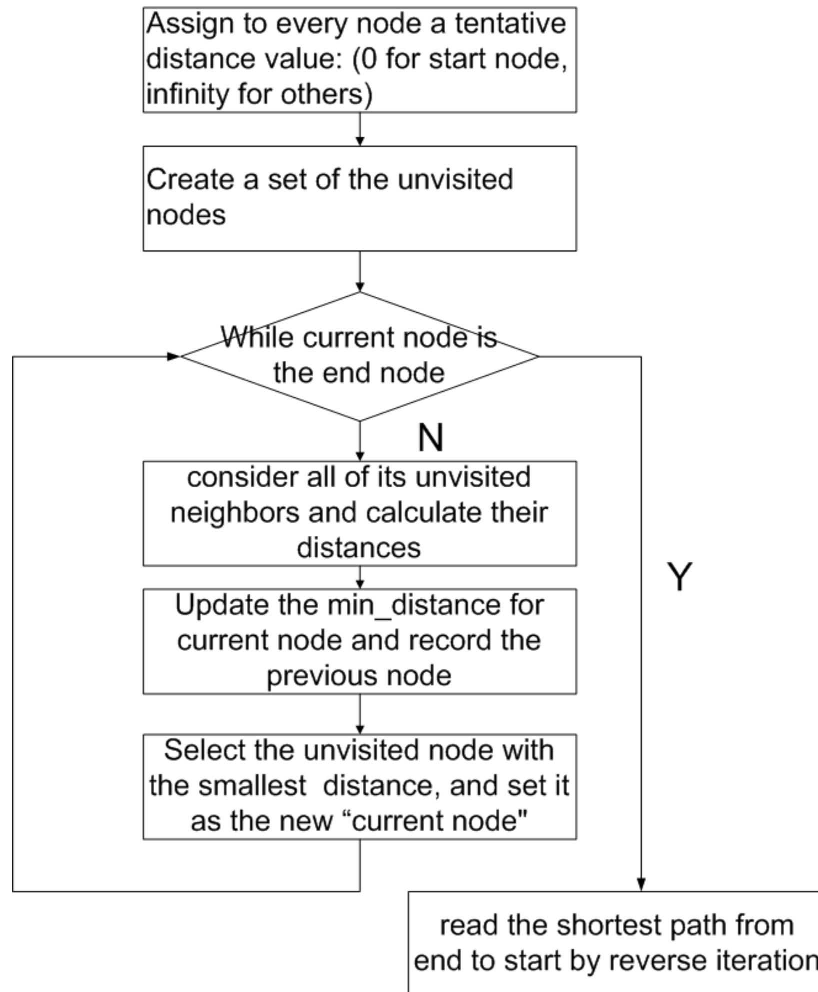


Figure 2.14 Flow chart of Dijkstra's algorithm

2.5 ESD CAD Tool Application Example

ESD CAD tool is implemented with C++ for Microsoft Windows platforms, since C++ is an object-oriented programming language and has the features of abstraction, encapsulation, inheritance, and polymorphism. The development environment is Visual C++ and debug method is embedded debug tools of Visual C++, such as break points. In addition, it has a user-friendly GUI Interface.

As an input file of ESD CAD tool, the technology file includes the device model graph definition, as shown in Figure 2.15 for the definition of LVSCR model graph.

```
#LVSCR
#
setdevice        {LVSCR}
device_vertex    1 2
device_vertex    2 6
device_vertex    3 2
device_vertex    4 3
device_vertex    5 1
device_vertex    6 9
device_edge      1 2
device_edge      2 3
device_edge      3 4
device_edge      4 5
device_edge      5 6
device_terminal  {K} 1  29
device_terminal  {A} 6  30
```

Figure 2.15 Model Graph Definition for LVSCR

Figure 2.16 shows the layout of an ESD protection circuit example. It consists of several ESD protection structures, including two SCRs as ESD protection for input IO, GGNMOS and GGPMOS (2xfingers) as ESD protection for output IO, and a LVSCR as power clamp. It was fabricated in a commercial 0.35 um BiCMOS technology and tested for full function.

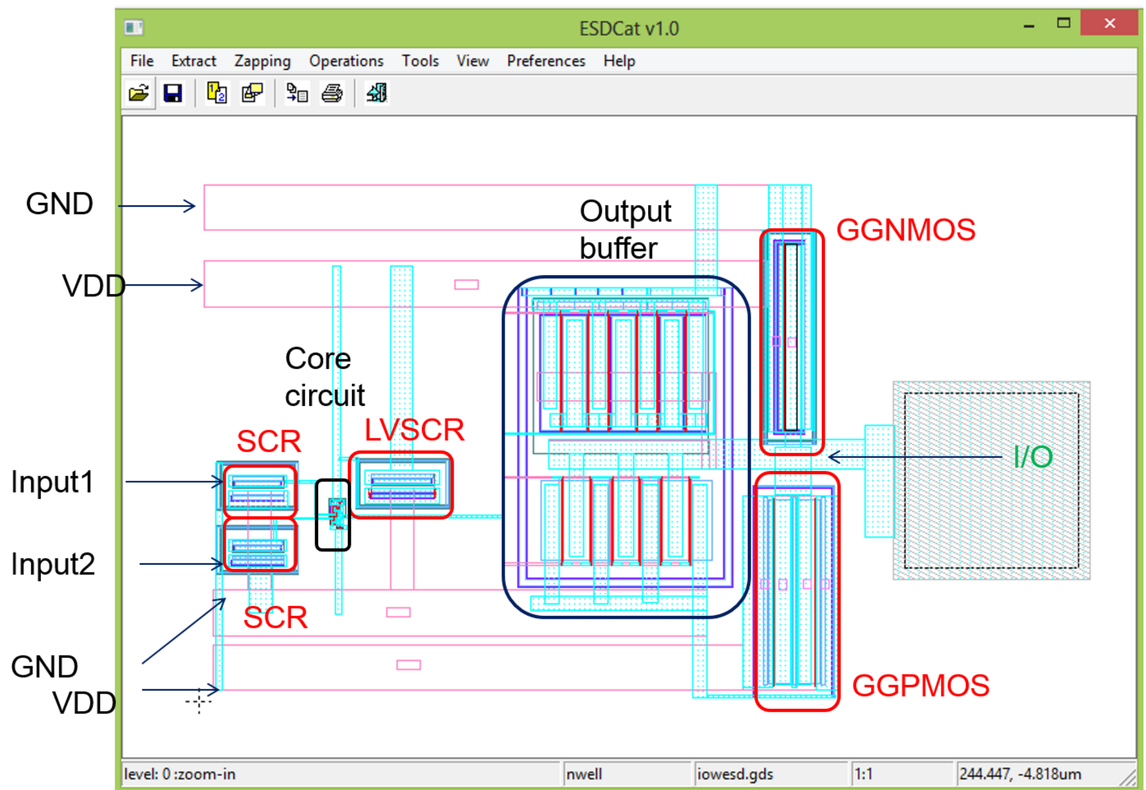


Figure 2.16 layout of an ESD protection circuit example

ESD Extractor are used to extract all possible ESD-type structures and their ESD-critical parameters. The extraction results are shown both in the graphical format as Figure 2.17, and in the text format as Figure 2.18 , where each extracted ESD device is presented by its name, terminal nodes and ESD-critical parameter. Therefore, after extraction, intentional ESD devices including GGNMOS, GGPMOS, SCR52, SCR55,

and LVSCR are extracted, and parasitic ESD devices including SCR51, MVSCR1 are also extracted.

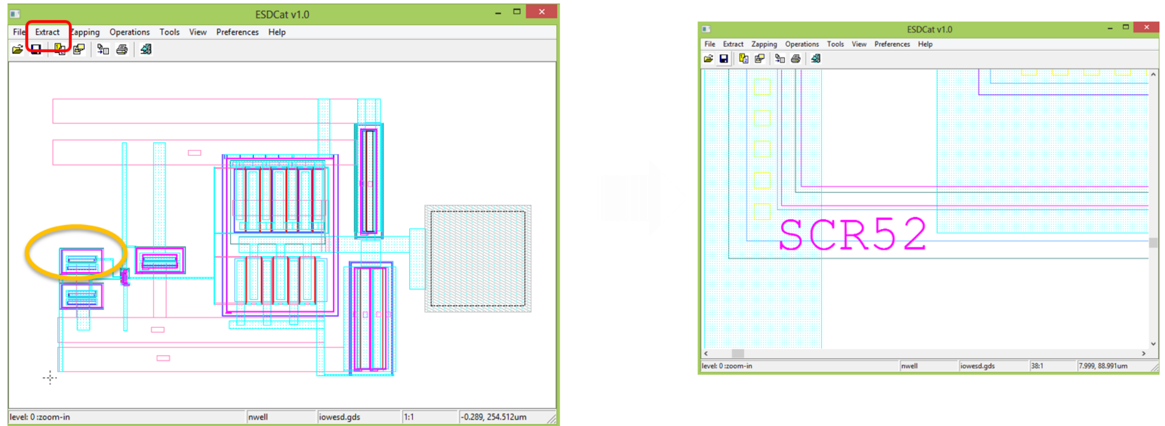


Figure 2.17 Extraction results in the graphical format

GGNMOS1 I/O GND GND Vt1=8.91125 It1=0.0297619 Vh=3.61722 Ih=0.327223 Ron=9.66
GGPMOS7 Vdd Vdd I/O Vt1=8.70509 It1=0.00892004 Vh=0.923127 Ih=0.0292166 Ron=14.375
GGPMOS8 Vdd Vdd I/O Vt1=9.78873 It1=0.0958904 Vh=15.825 Ih=1.05429 Ron=14.375
SCR51 VDD GND Vt1=19.7109 It1=0.0322163 Vh=3.621 Ih=0.190816 Ron=13.2117
SCR52 Input1 GND Vt1=19.5228 It1=0.0263374 Vh=3.59333 Ih=0.155833 Ron=16
SCR55 Input2 GND Vt1=19.5228 It1=0.0263374 Vh=3.59333 Ih=0.155833 Ron=16
MVSCR1 VDD GND Vt1=9.71092 It1=0.0322163 Vh=3.621 Ih=0.190816 Ron=13.2117
LVSCR1 VDD GND Vt1=0.7 Vt1b=18 It1=0.0271825 Vh=4.35829 Ih=0.409904 Ron=7.94891

Figure 2.18 Extraction results in the text format

The intermediate ESD netlist was examined using the smart ESD parametric checking mechanism to remove all redundant ESD devices extracted, resulting in a final ESD netlist. Figure 2.19 (a) shows the intermedia netlist, where the SCR51 and MVSCR1 has been removed since the V_{t1} is much higher than LVSCR1 that they'll not be turned on, resulting in the final netlist shown in Figure 2.19 (b).

```
GGNMOS1 I/O GND GND   Vt1=8.91125   It1=0.0297619   Vh=3.61722   Ih=0.327223   Ron=9.66
GGPMOS7 Vdd Vdd I/O   Vt1=8.70509   It1=0.00892004   Vh=0.923127   Ih=0.0292166   Ron=14.375
GGPMOS8 Vdd Vdd I/O   Vt1=9.78873   It1=0.0958904   Vh=15.825   Ih=1.05429   Ron=14.375
SCR51 VDD GND   Vt1=19.7109   It1=0.0322163   Vh=3.621   Ih=0.190816   Ron=13.2117
SCR52 Input1 GND   Vt1=19.5228   It1=0.0263374   Vh=3.59333   Ih=0.155833   Ron=16
SCR55 Input2 GND   Vt1=19.5228   It1=0.0263374   Vh=3.59333   Ih=0.155833   Ron=16
MVSCR1 VDD GND   Vt1=9.71092   It1=0.0322163   Vh=3.621   Ih=0.190816   Ron=13.2117
LVSCR1 VDD GND   Vt1=0.7   Vt1b=18   It1=0.0271825   Vh=4.35829   Ih=0.409904   Ron=7.94891
```

(a)

```
SCR52 Input1 GND   Vt1=19.5228   It1=0.0263374   Vh=3.59333   Ih=0.155833   Ron=16
SCR55 Input2 GND   Vt1=19.5228   It1=0.0263374   Vh=3.59333   Ih=0.155833   Ron=16
LVSCR1 VDD GND   Vt1=0.7   Vt1b=18   It1=0.0271825   Vh=4.35829   Ih=0.409904   Ron=7.94891
GGNMOS1 I/O GND GND   Vt1=8.91125   It1=0.0297619   Vh=3.61722   Ih=0.327223   Ron=9.66
GGPMOS7 Vdd Vdd I/O   Vt1=8.70509   It1=0.00892004   Vh=0.923127   Ih=0.0292166   Ron=14.375
GGPMOS8 Vdd Vdd I/O   Vt1=9.78873   It1=0.0958904   Vh=15.825   Ih=1.05429   Ron=14.375
```

(b)

Figure 2.19 (a) Intermedia netlist (b) Final netlist

From the final netlist, two possible discharge path between VDD and GND is shown in Figure 2.20. Therefore, ESD Zapper is applied to identify the critical ESD discharging paths on the chip, which considers all possible ESD-type devices including designed ESD structures and parasitic ESD type devices. Figure 2.21 (a) shows the graphical output, with the critical discharging path between VDD and GND marked using a solid line. Figure 2.21 (b) shows the text output.

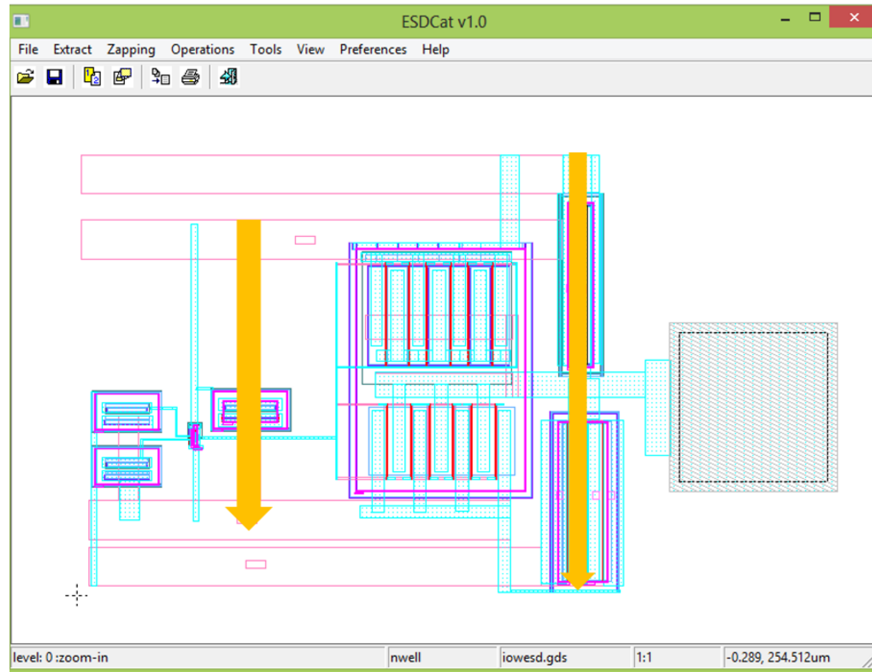
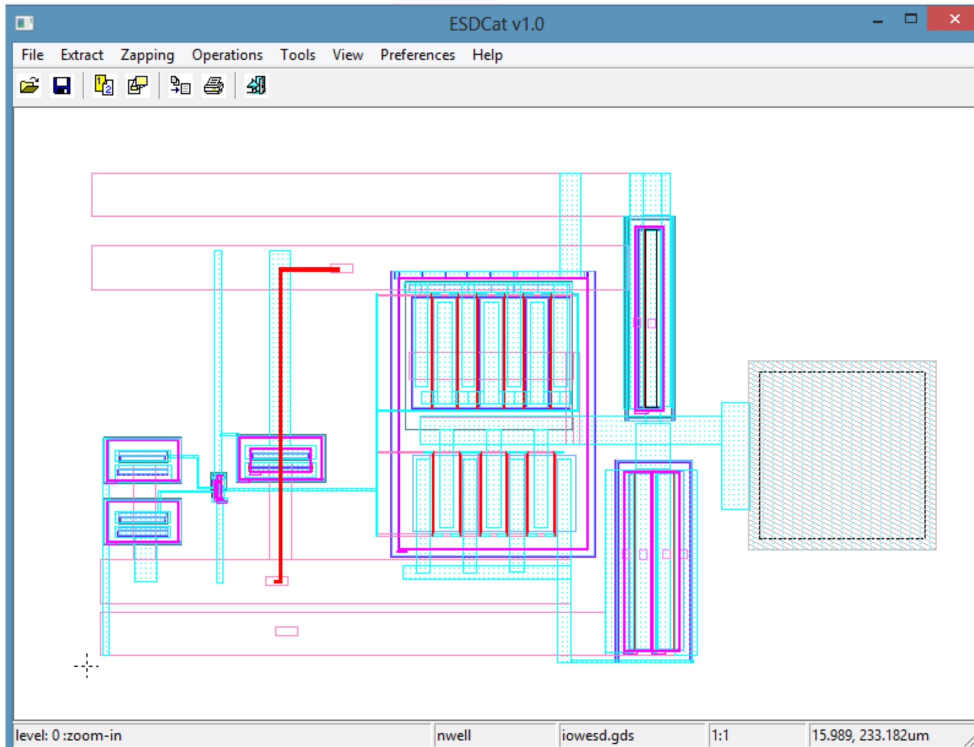


Figure 2.20 two possible discharge path from VDD to GND



(a)

```
Discharging path found from  VDD  to  GND, total Vt1= 0.7
LVSCR1 VDD GND    Vt1=0.7   Vt1b=18  It1=0.0271825  Vh=4.35829  Ih=0.409904
```

(b)

Figure 2.21 Critical discharge path between VDD and GND (a) graphical output (b) text output

Chapter 3 Scalable ESD Protection Structure Behavior Modeling

3.1 New Scalable ESD Behavior Modeling

To fully understand ESD protection mechanisms and further to enable whole-chip ESD circuit design simulation and verification, accurate ESD device modeling is required, which is very challenging due to the extremely complex ESD discharging behaviors. This is particularly true to model any non-traditional ESD structures, such as new SONOS and NCD ESD structures. The first step for ESD modeling is to understand basic ESD discharging functions, such as snapback ESD I-V curve shown in Figure 1.4 (b), which depicts the ESD-critical parameters include triggering (V_{t1}, I_{t1}), holding (V_h, I_h), ESD discharging resistance (R_{ON}) and ESD thermal failure threshold (V_{t2}, I_{t2}) [1]. Behavioral ESD device modeling enables accurate description of ESD device behaviors without being limited by the complex, and often unknown, ESD device physics. It overcomes the difficulties to extract complicated parameters based on high current and thermal physics. It is relatively easy to achieve a semi-physical model to describe high current ESD device behaviors using behavior language Verilog-A. It is empirical since scalability with device dimensions for key ESD-critical parameters (V_{t1}, V_h) can be established by matching TLP testing with design splits. In addition, behavioral ESD modeling also contribute to ease the convergence problem often caused by avalanche breakdown.

A new ESD behavior modeling technique is developed, which can accurately describe ESD discharging I-V behaviors piece-wisely and delivers reliable behavior ESD device models. The new ESD behavior modeling technique utilizes Verilog-A to describe

complicated ESD discharging behavior by ESD-critical parameters extracted from ESD I-V curves by TLP testing, which is then verified in SPICE circuit simulation. Figure 3.1 shows a flow chart to develop scalable behavior ESD device models for ESD devices. Firstly, the relationship between ESD-critical parameters and design splits must be established. Comprehensive TLP testing, featuring ESD pulse rise time t_1~10ns and duration t_d~100ns, plays a key role in this step. After extracting ESD-critical parameters from TLP testing results and analysis, a scalability model per device dimensions can be set up. Next, the TLP curves are divided into several section-wise segments according to ESD functions including: device off, device triggering, device snapback and ESD discharging, which may be repeating depending upon the complexity of measured ESD discharging curve for a given ESD device as shown in Figure 3.2. Each segment of the TLP testing curve can be modeled by a formula to describe the corresponding ESD function in Verilog-A and the fitting parameters can be extracted from the TLP curve directly correlated with device dimensions. For example, as shown in Figure 3.2, Function_off describes the device-off region of a TLP curve. An accurate scalable ESD behavior model is then obtained, which must be verified by comparing SPICE circuit simulation with TLP testing. Figure 3.3 shows a schematic for circuit level ESD simulation of the ESD structures using the ESD behavior models developed in this work. The circuit level ESD simulation was conducted using HBM ESD standard.

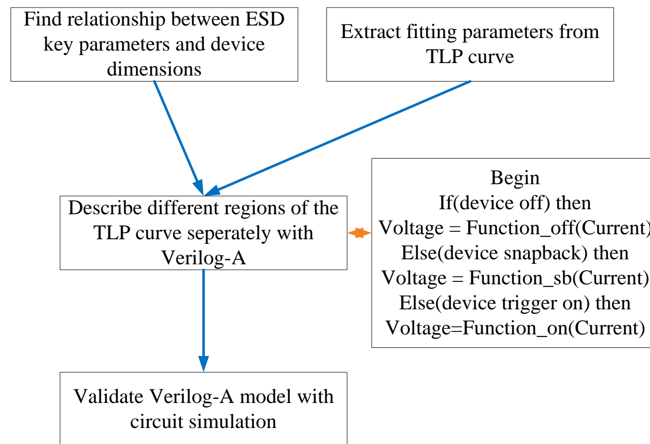


Figure 3.1 Flow chart for developing behavior models by Verilog-A.

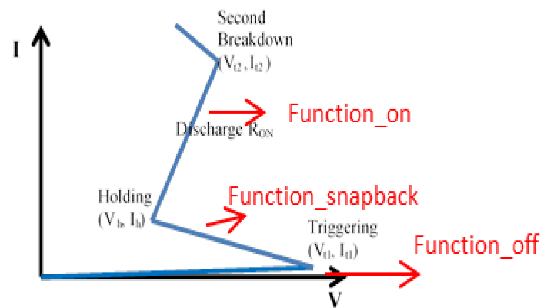


Figure 3.2 Partition TLP curve into sections per ESD discharging functions.

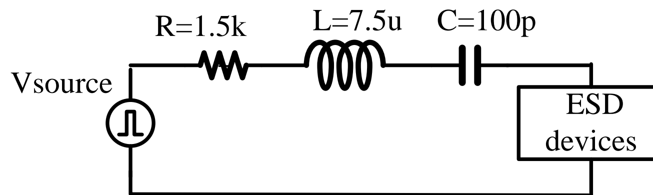


Figure 3.3 The circuit level ESD simulation schematic used to verify the new ESD behavior models

3.2 Novel Nano Crossbar ESD Device Model Method and Verification

3.2.1 Novel Nano Crossbar ESD Protection

Traditional ESD protection utilizes PN-junction-based active devices, such as, diodes, BJTs, FETs and SCRs, which have inherent disadvantages including ESD-induced leakage, parasitic capacitance and noise, etc. Revolutionary ESD protection

mechanisms are in demand for next-generation ICs in nano scales. Recently, we reported a novel non-traditional nano phase switching ESD protection concept. Prototype nano crossbar ESD protection structures and array circuits were demonstrated [14, 15]. Figure 3.4 depicts the new nano crossbar ESD protection structures, including a single-node nano crossbar. ESD device cross section (a), a 3X3 nano crossbar array ESD structure (b), and its typical on-chip ESD protection scheme (c). Conceptually, it is a sandwich structure consists of a thin SiON dielectric layer between two Cu/W metal electrodes [38]. The anode (A) and cathode (K) electrodes are connected to an I/O pad and VDD or ground (GND) of an IC.

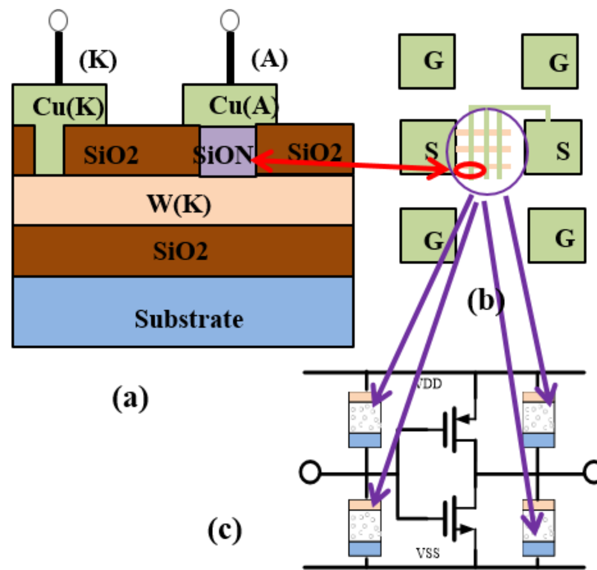


Figure 3.4 New nano crossbar ESD protection structure and circuit scheme: (a) Cross-section, (b) 3X3 ESD array, (c) on-chip ESD protection scheme

Figure 3.5 illustrates the proposed new dispersed local tunneling model to describe the new nano phase switch ESD protection mechanism. In principle, the nano switch ESD structure remains off in normal IC operations and the dielectric layer ensures extremely very low leakage, which is a major advantage over traditional PN-type ESD

devices. The porous SiON dielectric, made of nano particles and prepared by a new low-temperature process, allows Cu atoms pre-diffuse into the dielectric media, which are trapped by local O/N atoms and enable extremely fast local tunneling under strong electrical field. As an ESD surge appears to an I/O pad, a strong transient ESD-induced electrical field will ignite the dispersed local ESD tunneling effect, which turns on the nano ESD switch swiftly [46]. ESD discharging will take off immediately to provide ESD protection on a chip. After the ESD pulse passes over, the nano switch will return to its off state quickly without affecting normal IC operations. In prototype designs, the nano switch ESD structures were designed as nano crossbar single-node devices and array circuits with different design splits, including varying crossbar node area (1µmX1µm to 80µmX80µm), array size (1X1 to 20X20) and SiON compositions in order to understand the new ESD discharging mechanism.

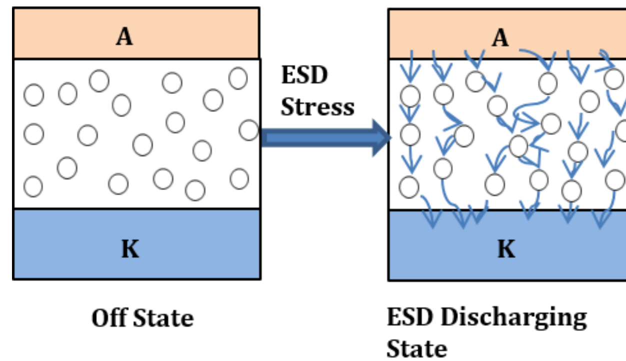


Figure 3.5 New nano crossbar ESD dispersed local tunneling model

The new nano crossbar ESD protection structures were fully verified in experiments. Figure 3.6 gives a measured ESD I-V curve for a sample single-node nano crossbar switch of 5µmX5µm by special transmission line pulsing (TLP) ESD testing, which clearly shows the desired snapback I-V curve in ESD discharging operation

according to Figure 1.4 (b). The measured ESD-critical parameters for the prototype device are: triggering voltage of V_{t1}~12.5V and holding voltage of V_h~7.4V [14].

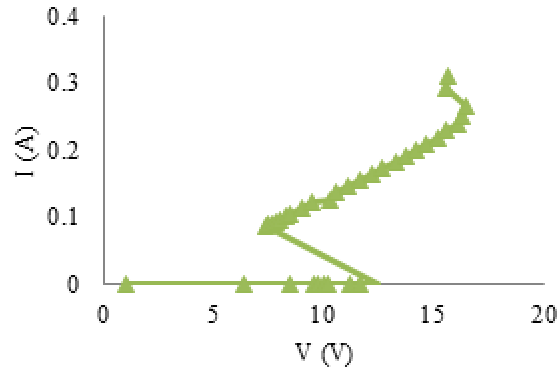


Figure 3.6 Measured snapback I-V curve for a nano crossbar single-node ESD device with node area of 5μmX5μm by TLP testing.

3.2.2 Nano Crossbar ESD Device Model Method

In order to thoroughly understand the new nano phase switching ESD protection mechanism and enable circuit level ESD protection design simulation, it is critical to develop accurate and scalable ESD device models for the new nano ESD protection structures. Since it takes more research to understand the true physics of the new nano crossbar ESD protection structures, we chose to develop behavior models for the new nano crossbar ESD structures by using Verilog-A description based on the measured ESD functions. The thorough TLP measurement and simulation results allow us to develop the Verilog-A behavior ESD device models in this work, as shown in Figure 3.1.

Comprehensive TLP testing was conducted according to human body model (HBM) ESD standard where the pulse rise time is t_1~10ns and its pulse duration is t_d~100ns. Developing accurate and scalable ESD device models requires carefully

correlating the measured ESD-critical parameters with ESD design dimensions, including nano crossbar node areas, crossbar array sizes and layout parameters. Table 3.1 compares measured ESD-critical parameters for a few sample nano crossbar single node structures with different sizes. Figure 3.7 describes the measured relationship between ESD triggering voltage V_{t1} and crossbar node area for the nano switch ESD devices. Figure 3.8 depicts measured ESD discharging resistance R_{ON} related the crossbar node area of the nano switch ESD devices.

Table 3.1 TLP Results for Different Nano ESD Devices

Device Size (μmXμm)	**TLP Testing Results**	
	V_{t1}(V)	***R_{ON}(Ω)***
5X5	12.5	55
10X10	12.2	44
20X20	11.5	19

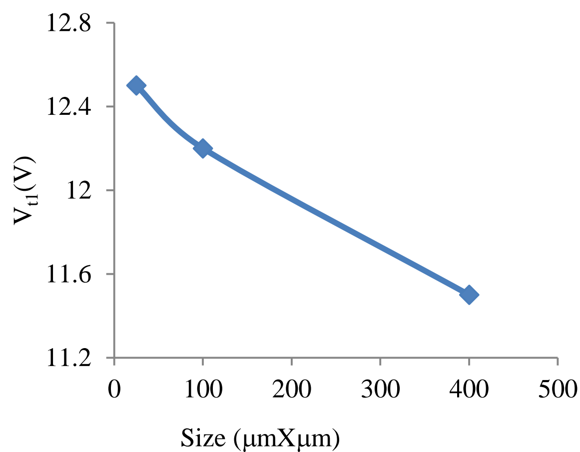


Figure 3.7 Measured Vt1 v.s. device size for nano crossbar ESD structures

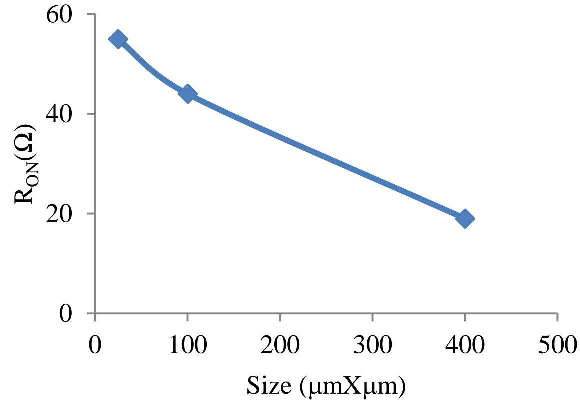


Figure 3.8 Measured ESD RON v.s. size for nano ESD devices

ESD measurements show clear monotonic relationship for the fabricated nano crossbar ESD switches, which can be described mathematically by Equations (3.1) and (3.2) below that are used in Verilog-A for behavioral description of the new ESD protection device models.

$$v_{t1} = -0.004 \times Size + 12.6 \tag{3.1}$$

$$R_{ON} = -0.147 \times Size + 58.667 \tag{3.2}$$

Similarly, all other ESD-critical parameters, including I_{t1}, V_h, I_h, R_{ON}, V_{t2}, I_{t2}, can be extracted from TLP testing and described in Verilog-A. These ESD-critical parameters are extracted for different prototype nano ESD switch structures of varying design dimensions in this work, which leads to the scalable behavior ESD models for the new nano crossbar ESD protection structures.

3.2.3 ESD Device Model Verification for Nano Crossbar

The newly developed scalable ESD behavior models were fully verified by circuit simulation using SPICE simulator and TLP testing.

Figure 3.9 compares TLP testing curve with SPICE circuit simulation result using the new behavior model developed for a prototype nano crossbar ESD switch with the crossbar node area of 5μmX5μm. Figure 3.10 gives the similar comparison for a sample nano crossbar ESD switch device with node area of 10μmX10μm. Figure 3.11 depicts the I-V curves from TLP testing and SPICE circuit simulation for another prototype nano crossbar ESD device with node area of 20μmX20μm. Figure 3.12 describes the I-V characteristics for a sample nano crossbar array ESD circuit, with the crossbar node area of 10μmX10μm and the array circuit size of 3X3, from both TLP testing and SPICE circuit simulation. The comparisons in Figs. 3.9 - 3.12 readily show that the ESD I-V characteristics from circuit level simulation using the new scalable behavior ESD models developed agree well with those from TLP testing for all new nano crossbar ESD protection devices and array circuits of different design splits. It strongly suggests that the new scalable ESD behavioral modeling technique and the extracted ESD behavior models are accurate and scalable for the new nano ESD switch structures fabricated in this work. Hence, the new scalable behavior models for the new nano crossbar ESD devices and its array structures developed using Verilog-A can be used for full-chip ESD protection circuit simulation and verification using standard SPICE tool.

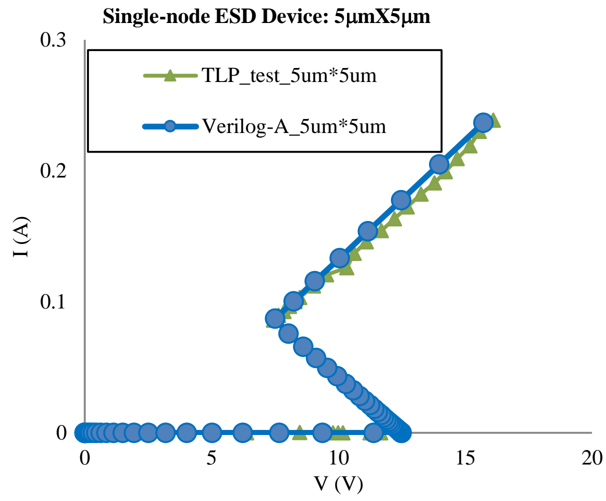


Figure 3.9 SPICE simulation for a single-node nano crossbar ESD device (area size 5µmX5µm) using the new ESD behavior model matches the TLP testing result well.

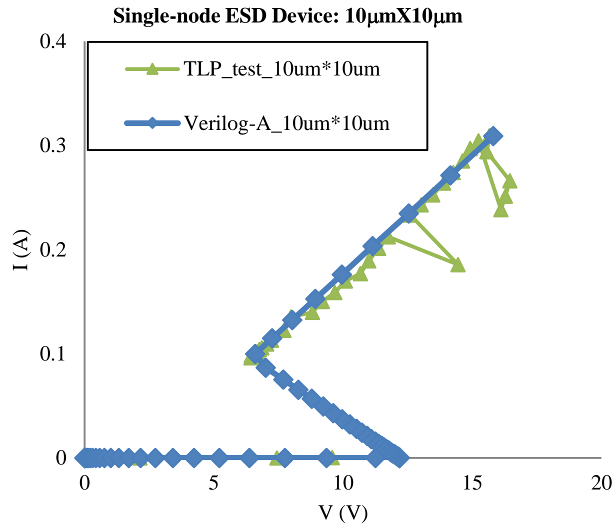


Figure 3.10 SPICE simulation for a single-node nano crossbar ESD device (area size 10µmX10µm) using the new ESD behavior model matches the TLP testing result well

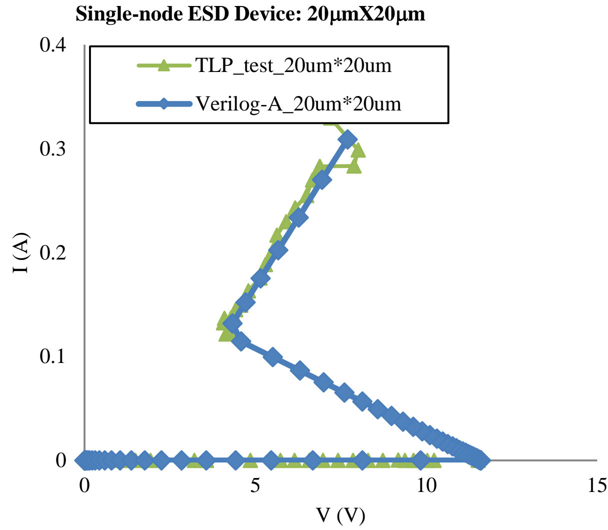


Figure 3.11 SPICE simulation for a single-node nano crossbar ESD device (area size 20µmX20µm) using the new ESD behavior model matches the TLP testing result well

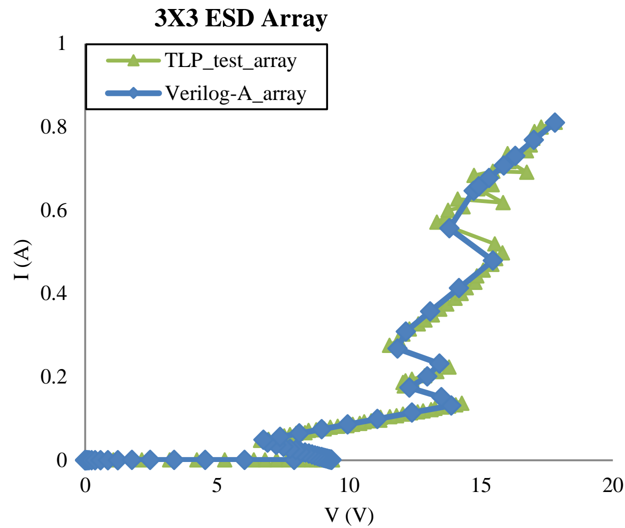


Figure 3.12 SPICE simulation for an nano crossbar array ESD protection circuit (node area: 10µmX10µm, array size: 3X3) using the new ESD behavior model matches the TLP testing result well

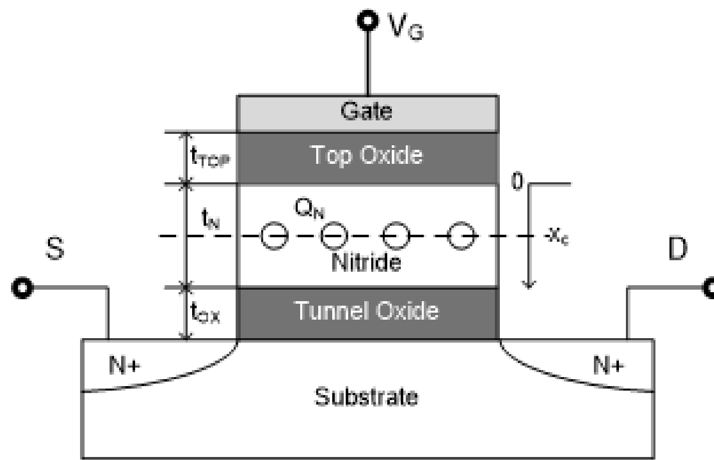
3.3 SONOS ESD Protection Model Method and Verification

All traditional ESD structures have fixed ESD-critical parameters [3], including ESD triggering voltage (V_{t1}), after Si design and fabrication are done. However, the measured ESD-critical parameters may be different from simulation design due to inevitable process, voltage and temperature (PVT) variations in fabrication. In addition,

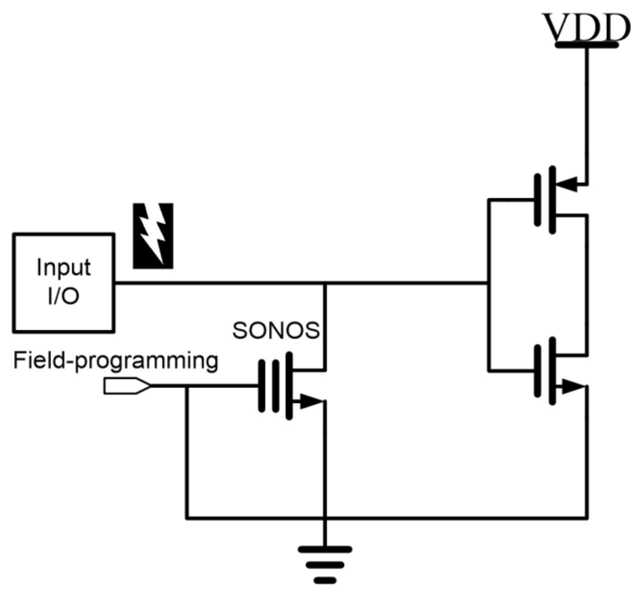
IC scaling down leads to ESD Design Window shrinking, new programmable ESD protection mechanisms hence become essential to accurate ESD protection designs [2]. Overall, field-programmable ESD protection mechanisms and structures are needed to fine-tune key ESD-critical parameters in post-Si field designs [16-18]. We devised a novel 3D field-programmable ESD protection solutions using silicon-oxide-nitride-oxide-silicon (SONOS) and report accurate Verilog-A ESD behavior models for the new non-traditional ESD protection structures.

3.3.1 SONOS ESD Protection

Figure 3.13 shows new 3D SONOS ESD structure (a) and a typical ESD protection circuit scheme (b). The novel ESD protection mechanism follows: with an embedded floating SONOS gate, extra charges are stored in SONOS where the charge density can be controlled by gate programming [35-37]. This modifies threshold voltage (V_{th}) of a MOEFET, hence resulting in change of ESD triggering voltage (ΔV_{t1}). As showed in Figure 3.13 (b), SONOS ESD structure is connected as a GGNMOS ESD device with a field-programming control to its gate. Figure 3.14 shows measured ESD I-V curves for a SONOS ESD device with W10µm/L0.15µm by transmission line pulsing (TLP) ESD testing [18]. The desired snapback ESD I-V curves are readily observed. It also clearly shows that erasing operation reduces the ESD V_{t1}, while programming increases the ESD V_{t1}.



(a)



(b)

Figure 3.13 SONOS (a) field-programmable ESD protection structure concepts, and ESD protection circuit scheme (b).

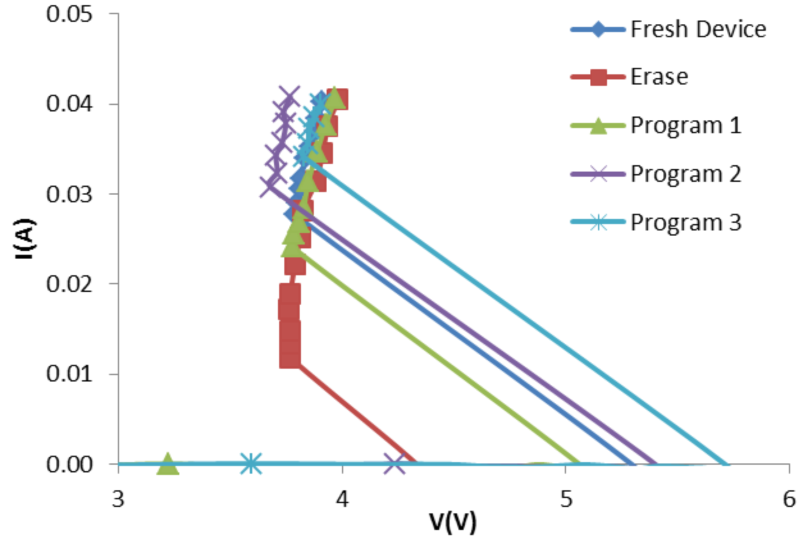


Figure 3.14 Measured ESD I-V curves by TLP for SONOS

3.3.2 SONOS ESD Device Model Method

Developing accurate and scalable ESD device models requires carefully correlating the measured results with ESD design features, including field-programmable ESD device sizes, layout patterns, SONOS material properties. Table 3.2 compares measured V_{t1} for sample SONOS ESD devices. Figure 3.15 depicts the measured V_{t1} versus SONOS ESD channel length (L) relationship, showing desired programmable ESD ΔV_{t1} by designs. Equations (3.3) is extracted to fit into measured ESD behaviors for Verilog-A modeling. Similarly, all other ESD-critical parameters (I_{t1}, V_h, I_h, R_{ON}, V_{t2}, I_{t2}) can be extracted from TLP testing and described in Verilog-A. ESD models were extracted for the field-programmable ESD structures with varying design dimensions in this work, which leads to scalable behavior ESD models.

$$V_{t1} = 4.53(L - 0.18) + 4 \quad (3.3)$$

Table 3.2 Measured ΔVt1 for sample SONOS ESD devices

ESD L (μm)	V_{t1} (V)
0.18	4
0.35	4.77
0.5	5.16

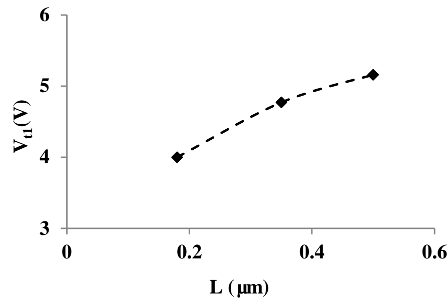


Figure 3.15 Measured Vt1 versus device size for sample SONOS ESD structures

A W10/L0.5μm SONOS ESD device is selected as an example to describe how the behavior model is generated. Figure 3.16 shows that the measured TLP curve is divided into multiple sections according to its complex ESD discharging behaviors, with its fitting formulas for different I-V sections listed below.

If ($V<V_{t1}$)

V <+ A*I; (Function_off)

Else if ($V<V_{h1}$)

V <+ B+C*I; (Function_snapback_1)

Else if ($V<V_{t_2}$)

V <+ D+E*I; (Function_on_1)

Else if ($V<V_{h2}$)

V <+ F+G*I; (Function_snapback_2)

Else if ($V<V_{t_3}$)

V <+ H+I*I;   (Function_on_2)

Else if ($V<V_{h3}$)

V <+ J+K*I;   (Function_snapback_3)

Else if ($V<V_{t2}$)

V <+ L+M*I;   (Function_on_3)

Parameter A is achieved from I_{t1}, which could be extracted from measured TLP curve and V_{t1}, which could be obtained from formula 3.3, correlated with device channel length. Similarly, fitting parameters B~M can be obtained either from correlated with device dimension or extracted from TLP curve.

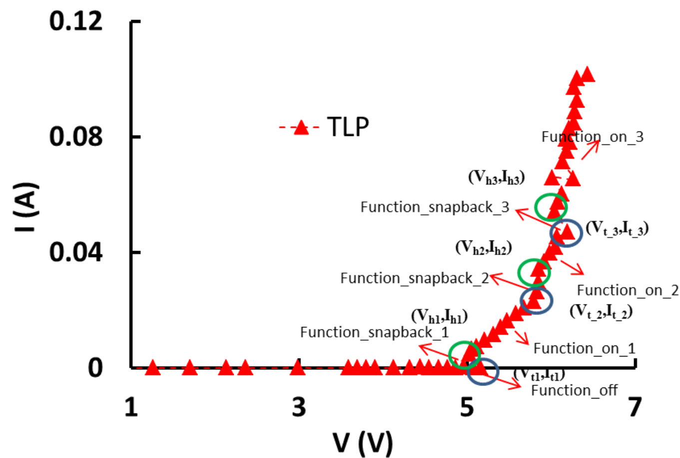


Figure 3.16 TLP curve partition for a W10/L0.5μm SONOS ESD device

3.3.3 SONOS ESD Device Model Verification

Many new SONOS ESD devices with varying layout dimensions were used for behavior model extraction and verification. Figure 3.17- 18 show ESD I-V curves from TLP testing and SPICE circuit simulation using the new ESD behavior models developed for two sample ESD devices (W/L=10/0.18μm, 10/0.5μm). Clearly, simulated ESD

circuit function using the new behavior models matches TLP testing curve very well. Further, good agreement between TLP testing and SPICE simulation holds for SONOS ESD devices with varying dimensions, confirming that the new ESD behavior modeling technique developed is not only accurate, but also scalable to layout variation, which is very important for practical on-chip ESD protection circuit designs because the actual ESD design dimensions may vary to meet specific circuit requirements including programmable ESD ΔV_{t1} and ESD protection level, etc.

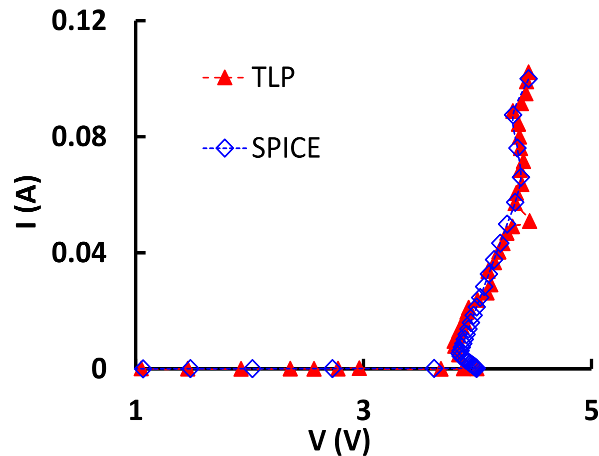


Figure 3.17 SPICE circuit simulation for a W10/L0.18µm SONOS ESD device using ESD behavior model matches TLP testing curve well

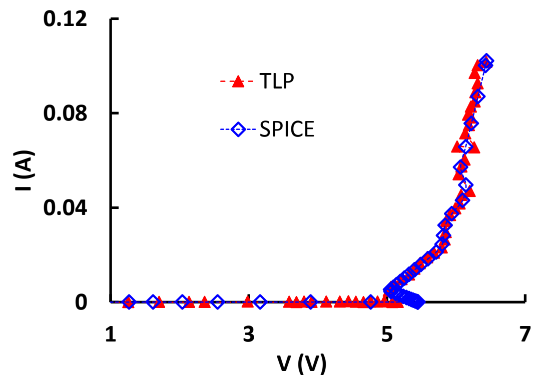


Figure 3.18 SPICE circuit simulation for a W10/L0.5µm SONOS ESD device using ESD behavior model matches TLP testing curve well

3.4 NCD ESD Protection Model Method and Verification

We devised another novel 3D field-programmable ESD protection solutions using nano crystal dots (NCD) structures in CMOS-compatible processes, and report accurate Verilog-A ESD behavior models for the new non-traditional ESD protection structures.

3.4.1 NCD ESD Protection

Figure 3.19 depicts the new 3D NCD ESD structure and its ESD protection circuit scheme [16]. In principle, an NCD ESD structure is an MOSFET containing a layer of nano crystal dots, which is connected as a GGNMOS ESD structure. The ESD V_{t1} programmability for NCD ESD devices is realized by charging/de-charging the NCD layer with free carriers through gate control. Figure 3.20 shows measured I-V curves for a sample NCD ESD device (W100/L2μm) before and after programming by TLP testing. It clearly shows that the desired snapback ESD I-V behavior that delivers a wide $\Delta V_{t1} \sim 2V$ by programming the embedded nano crystal dots.

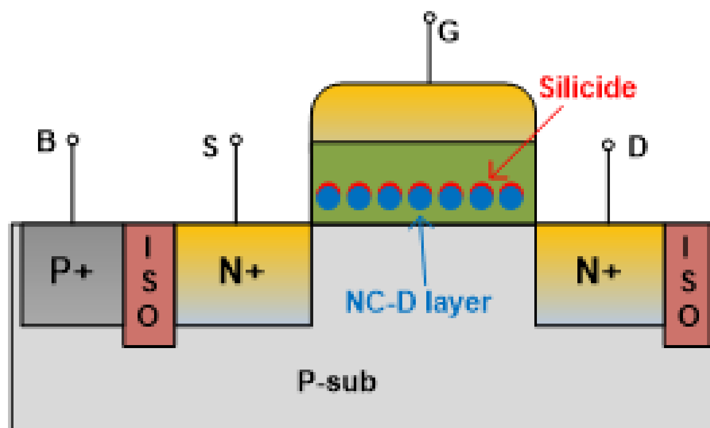


Figure 3.19 NCD field-programmable ESD protection structure concepts

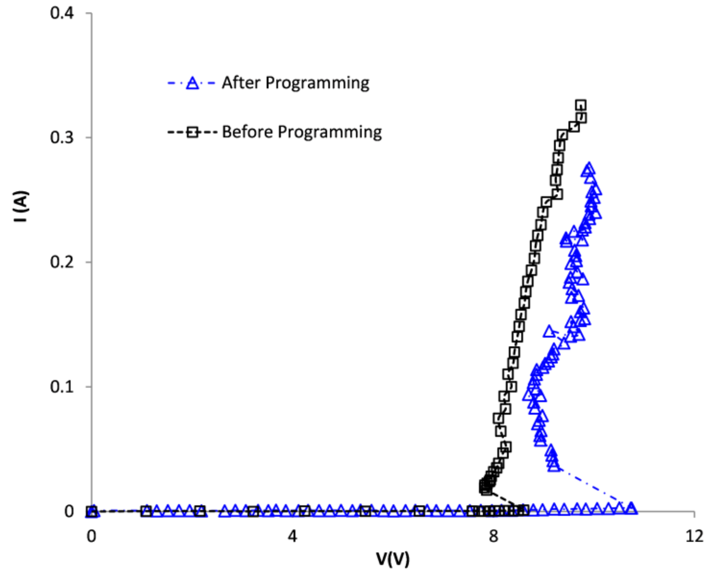


Figure 3.20 Measured ESD I-V curves by TLP for NCD

3.4.2 NCD ESD Device Model Method

NCD ESD device behavior models are generated similarly. Table 3.3 compares measured V_{t1} for sample NCD ESD devices. Figure 3.21 depicts the measured relationship between ESD V_{t1} and L of NCD ESD devices, which shows desired programmable ESD ΔV_{t1} by design variation. Equations 3.4 is obtained to fit into measured ESD behavior model parameters using Verilog-A.

$$V_{t1} = 0.7(L-1)+7.9 \tag{3.4}$$

Table 3.3 Measured ΔV_{t1} for sample NCD ESD device

ESD L (μm)	V_{t1} (V)
1	7.9
2	8.6
3	8.95

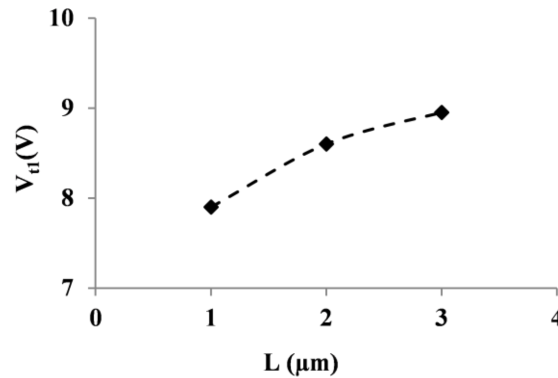


Figure 3.21 Measured Vt1 versus device size for sample NCD ESD structures

A W/L=100/1μm NCD ESD device is used to show ESD behavior modeling procedures. Figure 3.22 shows its TLP curve that can be divided into three ESD functional sections with the fitting formulas given below for model parameter extraction.

If (V<Vt1)

V <+ A*I; (Function_off)

Else if (V<Vh)

V <+ B+C*I; (Function_snapback)

Else if (V<Vt2)

V <+ D+E*I; (Function_on)

Parameter A was achieved from I_{t1}, extracted from measured TLP curve and V_{t1}, which was obtained from equation 3.4, correlated with device channel length. Similarly, fitting parameters B~E were generated either by correlating with device dimension or extraction from TLP curve.

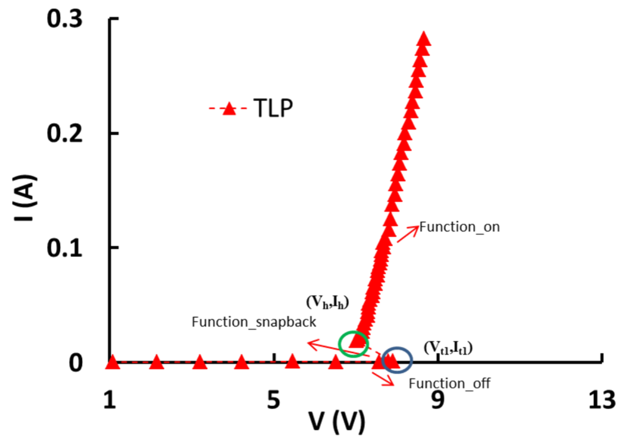


Figure 3.22 TLP curve partition for a W100/L1μm NCD ESD device

3.4.3 NCD ESD Device Model Verification

New NCD ESD device of different design splits was studied for modeling verification. Figs. 3.23- 3.24 compare ESD I-V curves from TLP testing with SPICE circuit simulation using new ESD behavior model for two sample NCD devices (W/L=100/1μm, 100/2μm), which again show excellent agreement and accuracy, as well as scalability of the new ESD behavior models. Further, to enable field design variations, behavior models for ESD devices under different programming conditions are developed. Figure 3.25 compares TLP and SPICE simulation curves for a sample NCD device after programming, which shows good agreement (the same device in Figure 3.24 tested before-programming). It clearly shows that the new scalable ESD behavior modeling technique allows to develop accurate ESD device models for the novel field-programmable ESD structures, which enables whole-chip ESD circuit simulation, synthesis, optimization, verification and prediction in designs.

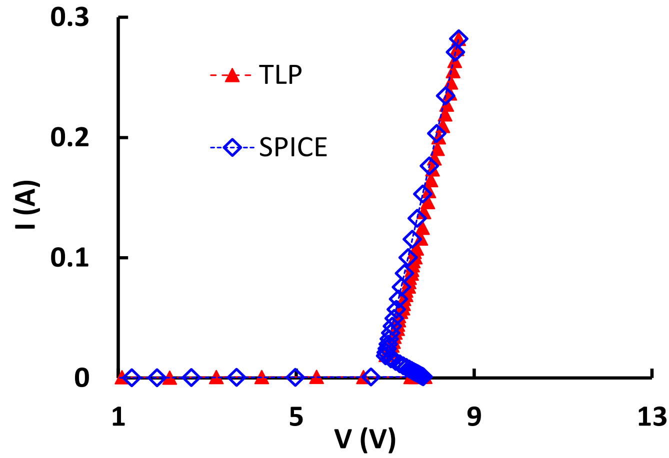


Figure 3.23 SPICE circuit simulation for a W100/L1µm NCD ESD device using ESD behavior model matches TLP testing curve well (Fresh)

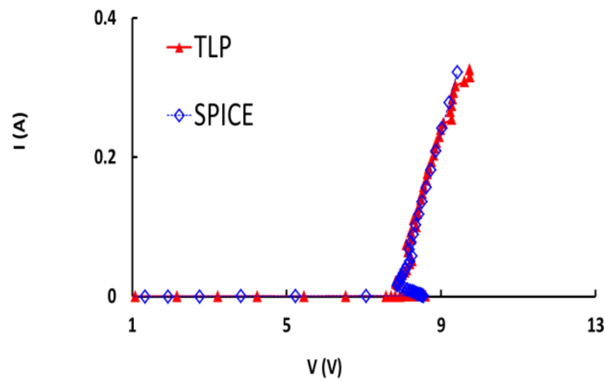


Figure 3.24 SPICE circuit simulation for a W100/L2µm NCD ESD device using ESD behavior model matches TLP testing curve well (before programming)

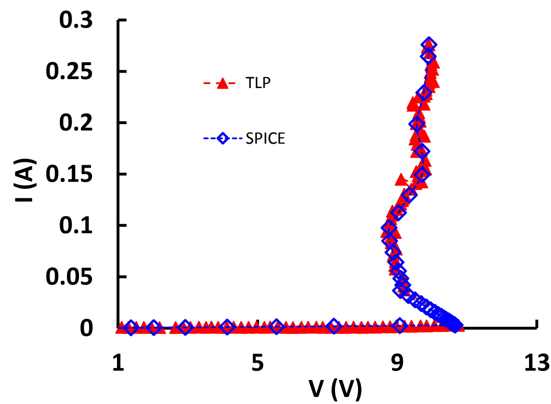


Figure 3.25 SPICE simulation for a W100/L2µm NCD ESD device (Fig. 3.24) using behavior model matches TLP testing curve well (after programming)

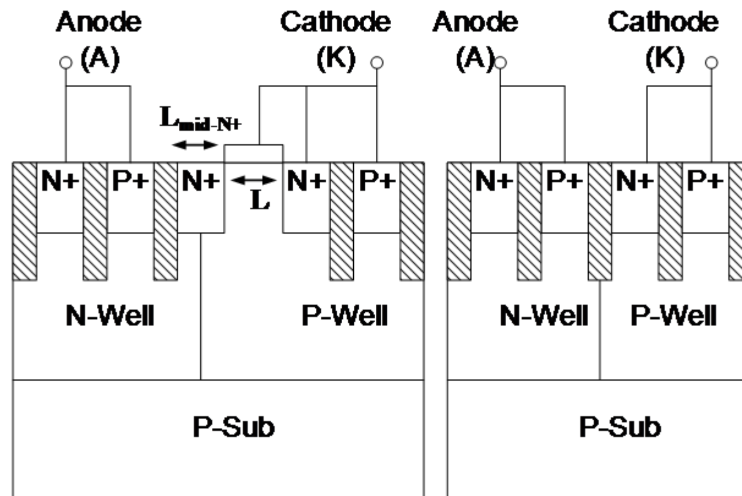
3.5 SCR based ESD Protection Model Method and Verification

SCR based ESD protection structures have the advantages of handling higher ESD surges and having lower parasitic effects, hence become attractive to RF and mixed-signal ICs at advanced technology nodes [19-21]. We describe a new scalable behavioral modeling technique for SCR based ESD protection structures to enable full-chip ESD protection circuit simulation.

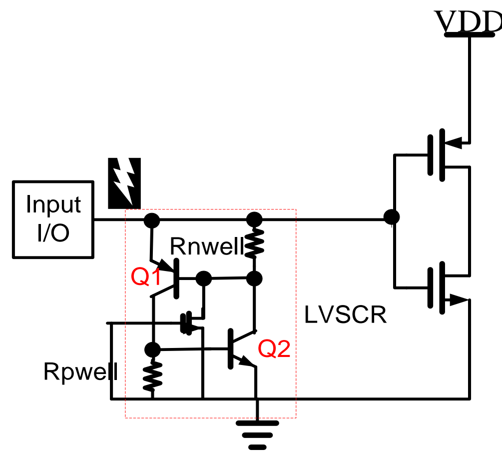
3.5.1 LVSCR ESD Protection Structure

The LVSCR ESD structure is attractive because it has reduced ESD triggering voltage (V_{t1}), while features high ESD protection level, good ICs at advanced nodes. V_{t1} of SCR ESD structures may be reduced by different low-triggering mechanism. Figure 3.26 depicts a new gate-coupled LVSCR ESD structure designed in this work including its cross-section and on-chip ESD protection circuit scheme. The LVSCR structure is a normal SCR device with embedded short-channel NMOS to enhance ESD triggering. Since the NMOS drain breakdown voltage occurs first at a much lower voltage level than the normal N-well/P-well breakdown in a regular SCR structure, a LVSCR can be triggered at a much lower ESD V_{t1}. As shown in Figure 3.26 , a normal SCR consists of a vertical PNP (Q1) and a lateral NPN (Q2) transistors, hence V_{t1} is fairly high, typically 15~25V in a 180nm Bi/CMOS technology. For LVSCR structure, when ESD surge occurs, increase in V_{AK} turns on the NMOS device, which initiates a seeding current to trigger current regeneration in LVSCR as following: Collector current in Q1 supplies base current for Q2 and pushes it into active mode; in turn, collector current of Q2 sources base current for Q1. As long as the current gain product is greater than one, the

current regeneration sustains in a LVSCR structure, pushing it into a negative resistance region with very low ESD discharging resistance (R_{ON}). ESD triggering for a LVSCR can be reduced to V_{t1}=6~10V, suitable for advanced ICs [40].



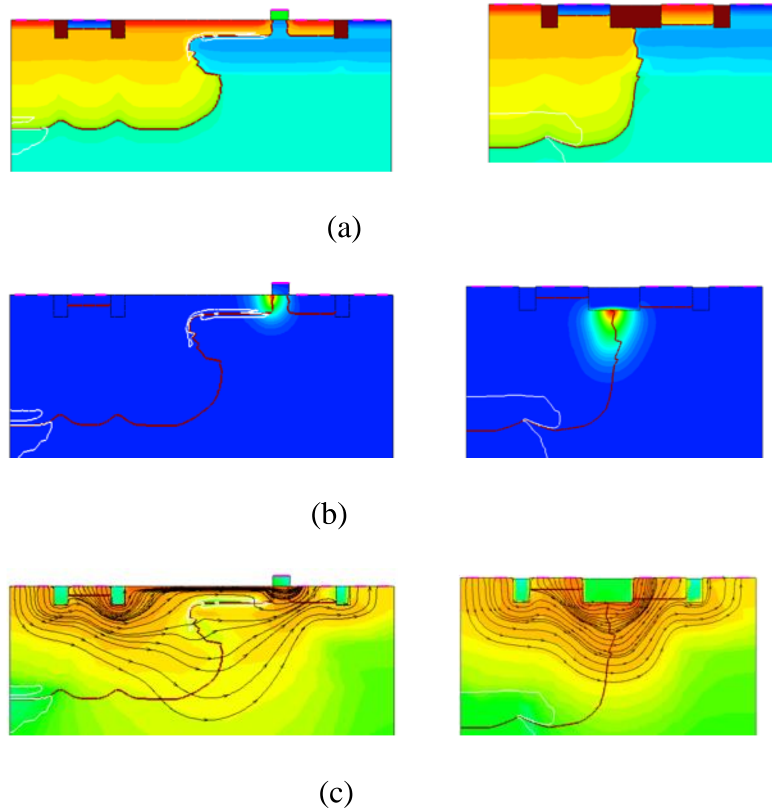
(a) (b)



(c)

Figure 3.26 LVSCR (a) versus SCR (b) ESD structure (L is NMOS channel length and $L_{mid\text{-}N+}$ is length for N+ across P-well/N-well), and equivalent circuit model and on-chip ESD protection circuit scheme for LVSCR structure (c)

In this work, comprehensive mixed-mode ESD simulation was conducted for ESD design optimization [22]. Figure 3.27 depicts simulated cross-section, heating effect and temperature contours, and transient ESD discharging behaviors for the NMOS-triggered LVSCR compared with an SCR structure under the same ESD stresses. It is clearly observed that the ESD discharging current tends to crowded around the drain of the embedded NMOS inside the LVSCR structure, resulting in an ESD-induced hot spot at the NMOS D/G corner, while a hot spot appears at the N-well/P-well junction inside a SCR. The simulated transient ESD discharging current conduction path and distribution reveal details of ESD discharging operation, critical to ESD design optimization and prediction.



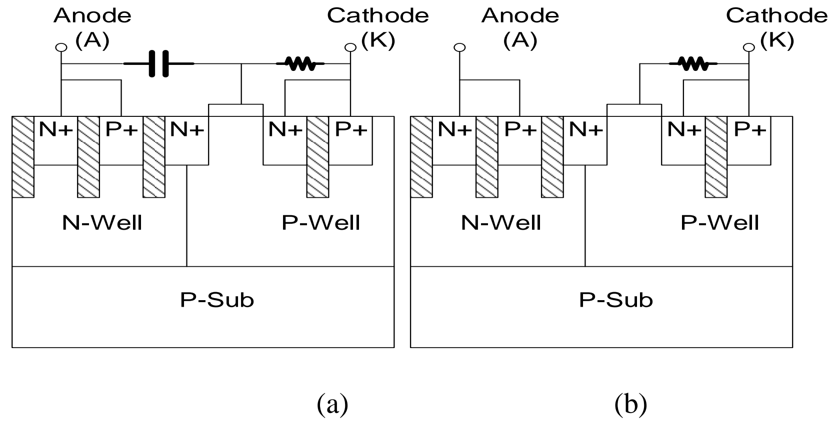
(a)

(b)

(c)

Figure 3.27 Simulated (a) cross-section, (b) temperature contours and heating effect, and (c) ESD discharging current flows for NMOS-LVSCR (Left) and SCR (Right) ESD protection structures under the same ESD stressing

To further reduce V_{t1}, gate-coupled techniques were applied to LVSCR without an involving avalanche breakdown mechanism. Figure 3.28 shows two types of such ultra-low triggering LVSCR structures, including an RC-coupled LVSCR (a) and a gate-resistor LVSCR (b), both served to further reduce ESD V_{t1}. Figure 3.29 shows simulated transient ESD I-V curves for sample structures including a normal SCR, an NMOS-LVSCR (L0.35μm/$L_{mid\text{-}N+}$3μm), a RC-coupled LVSCR (L0.35μm/$L_{mid\text{-}N+}$3μm) and a gate-resistor LVSCR (L0.35μm/$L_{mid\text{-}N+}$1μm) under 2kV ESD stressing. It is clearly observed that an NMOS-LVSCR has reduced V_{t1} over a normal SCR, while the RC-coupled LVSCR and gate-resistor LVSCR achieved ultra-low V_{t1}.



(a) (b)

Figure 3.28 (a) Schematic for RC-coupled LVSCR, (b) gate-resistor LVSCR

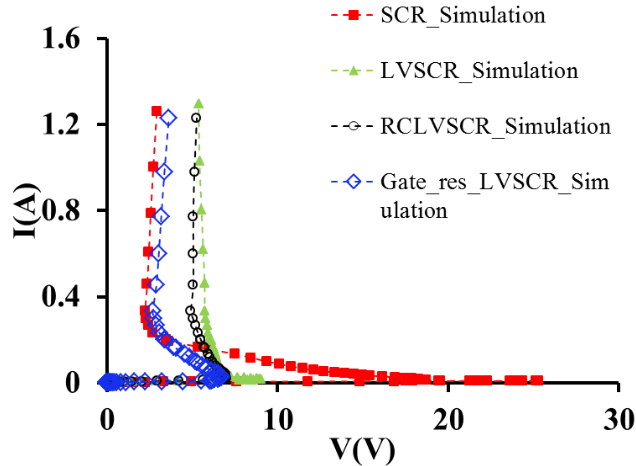


Figure 3.29 Simulated transient ESD discharging I-V curves for SCR, NMOS-LVSCR (L0.35µm/$L_{mid\text{-}N+}$3µm), RC-coupled LVSCR (L0.35µm/$L_{mid\text{-}N+}$3µm) and gate-resistor LVSCR (L0.35µm/$L_{mid\text{-}N+}$1µm)

A large set of various LVSCR ESD structures were fabricated in an 180nm RF BiCMOS. Comprehensive ESD characterization was conducted using transmission line pulse (TLP) tester (Barth 4002+). Figure 3.30 shows measured ESD I-V curve for one sample NMOS-LVSCR device with channel width, channel length and middle N+ length ($L_{mid\text{-}N+}$) of W30µm/L0.45µm/Lmid-N+1µm. It clearly shows the desired snapback I-V curve in ESD discharging operation. The measured ESD-critical parameters are V_{t1}~9.2V and holding voltage of V_h~3V for this sample LVSCR ESD device.

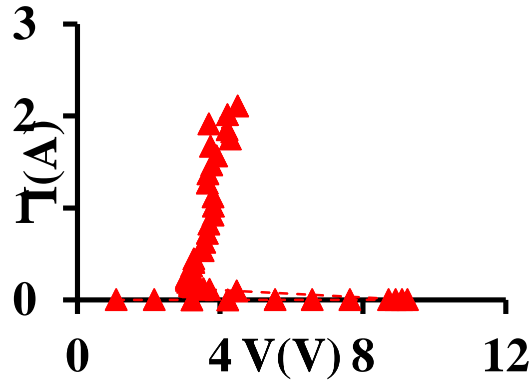


Figure 3.30 Measured snapback I-V curve for a sample NMOS-LVSCR ESD device featuring $W/L/L_{mid-N+}$=30/0.45/1μm by TLP testing

3.5.2 LVSCR ESD Device Model Method

Comprehensive TLP testing was conducted according to human body model (HBM) ESD standard where ESD pulse rise time and duration are t_1~10ns and t_d~100ns, respectively. The accuracy of scalable ESD device models depends upon the correlation between the ESD measurement results and ESD physical design parameters, which were selected carefully via mixed-mode ESD simulation to achieve desired ESD-critical parameters. For example, the gate length (L) of the embedded NMOS plays a key role in determining V_{t1} of LVSCR. Figure 3.31 gives the measured V_{t1} versus L for sample LVSCR device splits, showing that a shorter NMOS channel reduces V_{t1} for LVSCR. On the other hand, the ESD holding voltage V_h, critical to avoiding latch-up in IC designs, is controlled by the N-well overlap of the P+ anode, which is revealed by the measured V_h ~ mid-N+ length relation shown in Figure 3.32.

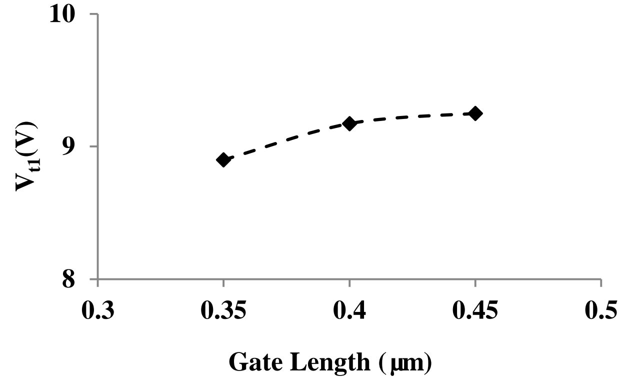


Figure 3.31 Measured V_{t1} versus L for sample LVSCR ESD structures

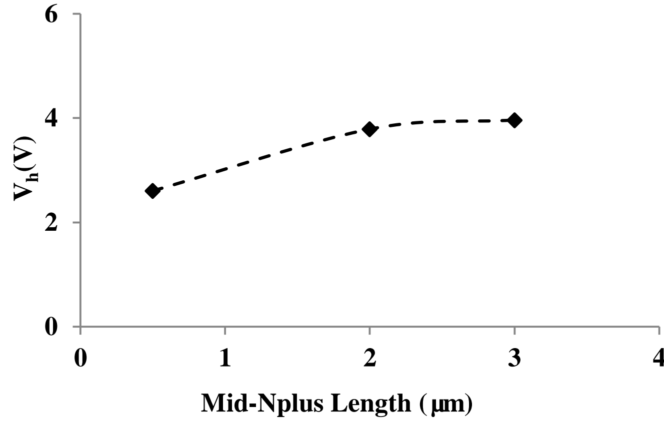


Figure 3.32 Measured V_h versus mid-N+ length for sample LVSCR ESD devices

The fitting equations 3.5 and 3.6, obtained from Figs. 3.31 and 3.32, are used to extract the ESD behavior model parameters using Verilog-A. Similarly, all other ESD-critical parameters (I_{t1}, V_h, I_h, R_{ON}, V_{t2}, I_{t2}) can be extracted from TLP testing and described in Verilog-A. ESD models were extracted for a large group of LVSCR ESD structures with varying design dimensions in this work, which resulted in a set of scalable behavior ESD models for LVSCR structures.

$$V_{t1} = 5.48(L - 0.35) + 8.898 \tag{3.5}$$

$$V_h = 0.786(L_{mid-N+} - 0.5) + 2.607 \tag{3.6}$$

3.5.3 LVSCR ESD Device Model Verification

Figs. 3.33 - 3.35 show ESD I-V curves from TLP testing and SPICE circuit simulation using the new ESD behavior models developed for three sample LVSCR ESD devices with different L, i.e., $W/L/L_{mid\text{-}N+}$ = 30/0.35/1μm, 30/0.4/1μm and 30/0.45/1μm, respectively. Clearly, the simulation using the new ESD models matches TLP testing very well. It confirms that the new ESD behavior modeling technique developed for SCR type ESD structures is not only accurate for ESD circuit simulation, but also scalable to physical layout (L), which is very important for practical on-chip ESD protection circuit designs because the actual ESD design dimensions may vary to meet specific circuit requirements including ESD protection level, etc.

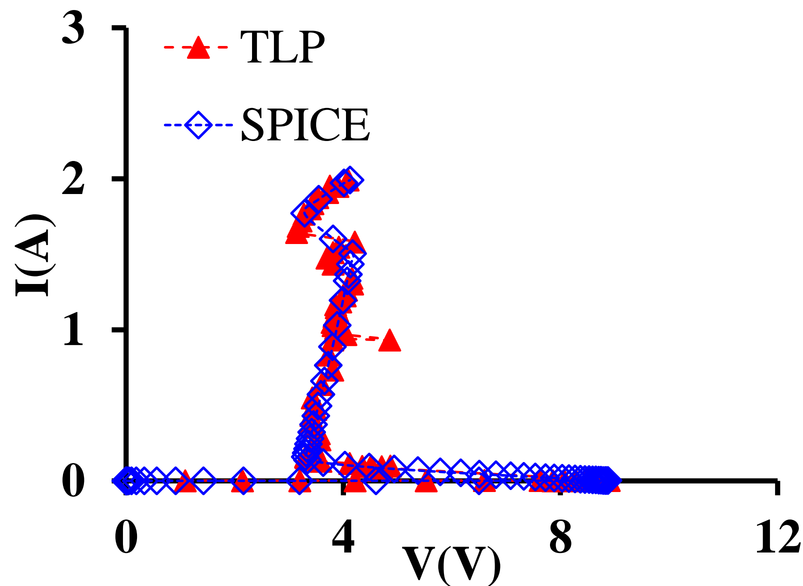


Figure 3.33 SPICE circuit simulation using behavior model matches TLP testing well for a sample LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=30/0.35/1μm

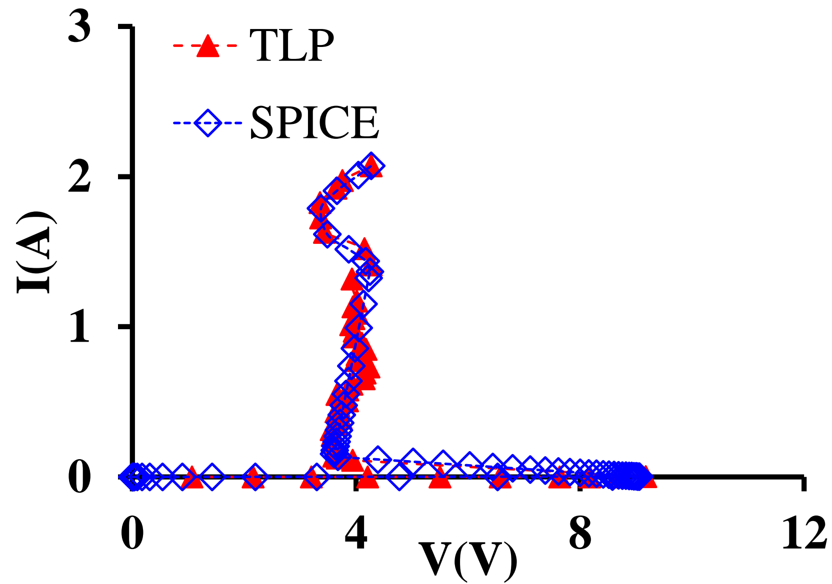


Figure 3.34 SPICE circuit simulation using behavior model matches TLP testing well for a sample LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=30/0.4/1µm

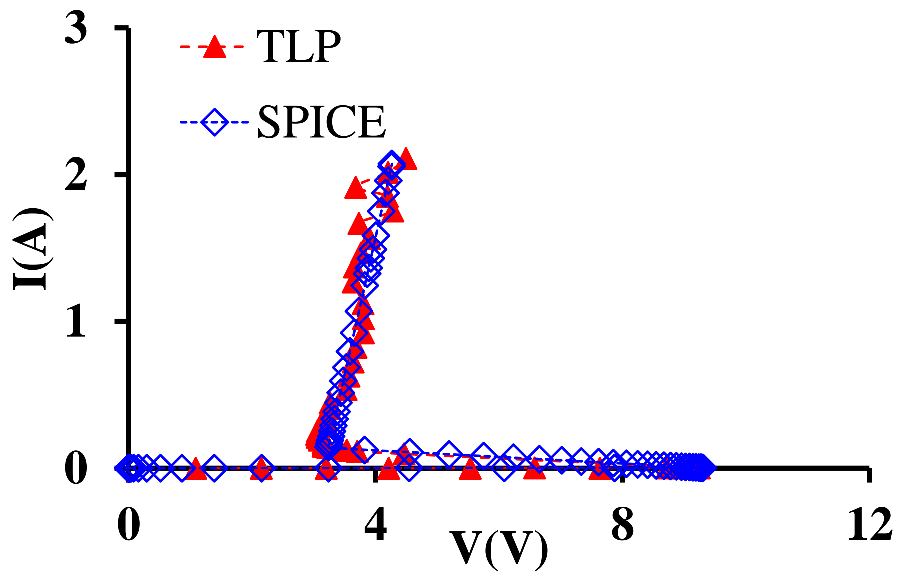


Figure 3.35 SPICE circuit simulation using behavior model matches TLP testing well for a sample LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=30/0.45/1µm

Figs. 3.36 -3.38 compare ESD I-V curves from TLP testing and ESD circuit simulation using new behavior models for three sample ESD devices with varying mid-

N+ length, i.e., $W/L/L_{mid\text{-}N+}$ =30/0.35/0.5µm, 30/0.35/2µm, 30/0.35/3µm, respectively, which again show excellent agreement and accuracy and scalable to $L_{mid\text{-}N+}$.

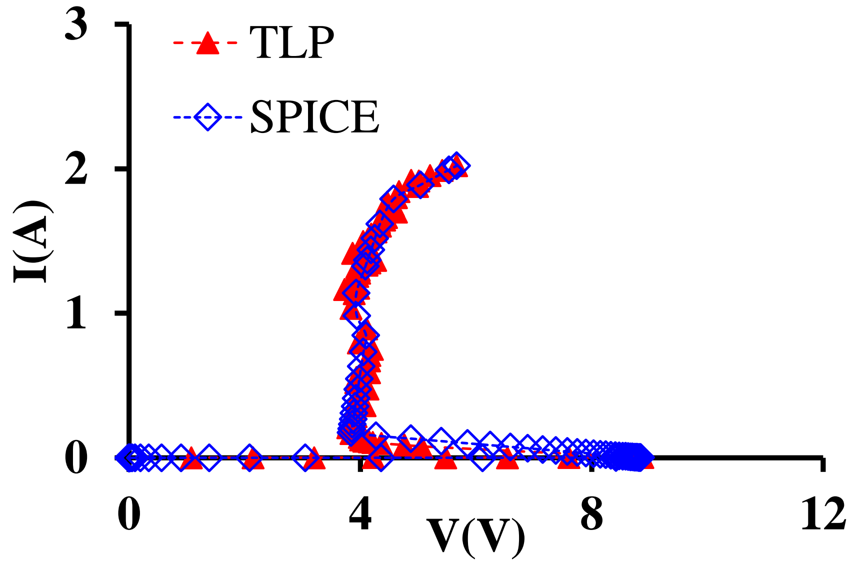


Figure 3.36 SPICE circuit simulation using behavior model matches TLP testing well for a sample LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=30/0.35/0.5µm

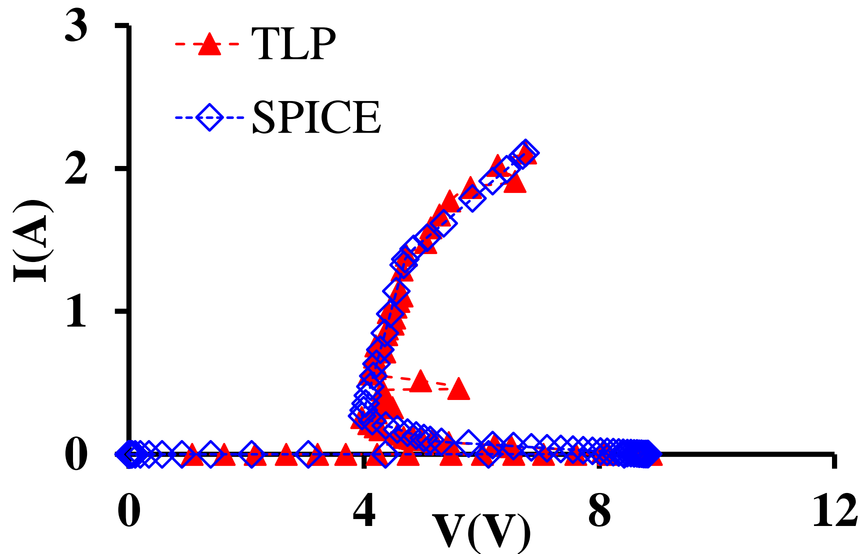


Figure 3.37 SPICE circuit simulation using behavior model matches TLP testing well for a sample LVSCR structure featuring $W/L/L_{mid\text{-}N+}$= 30/0.35/2µm

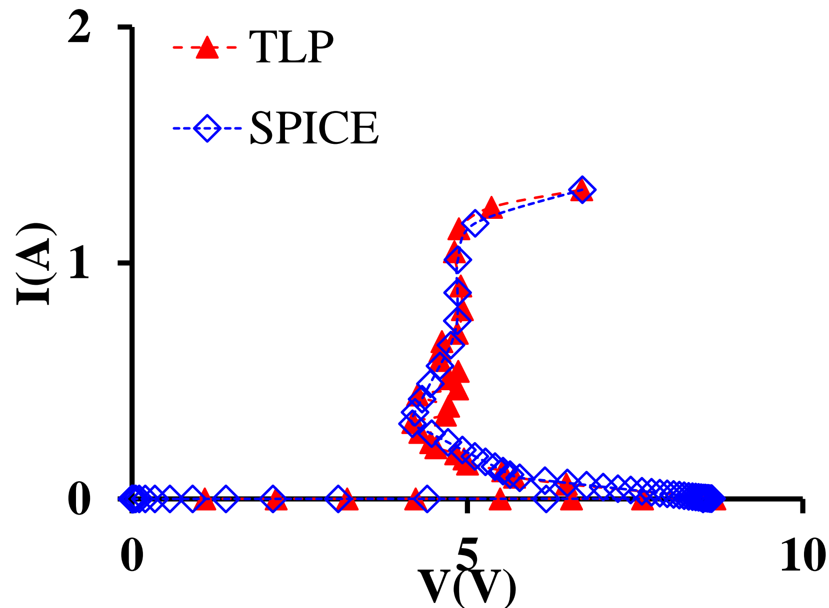


Figure 3.38 SPICE circuit simulation using behavior model matches TLP testing well for a sample LVSCR structure featuring $W/L/L_{mid\text{-}N+}$= 30/0.35/3μm

ESD behavior models for a group of gate-coupled LVSCR ESD devices with varying layout dimensions were also extracted and verified by SPICE circuit simulation. Figure 3.39 shows ESD I-V curves comparison between TLP testing and ESD circuit simulation using new ESD behavior models for a sample RC-coupled LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=90/0.35/3μm, C=1pF and R=10KΩ. Figure 3.40 offers similar comparison between TLP testing and SPICE simulation for a sample gate-resistor LVSCR structure of R= 100KΩ and $W/L/L_{mid\text{-}N+}$=30/0.35/1μm. Excellent agreement was obtained in both cases.

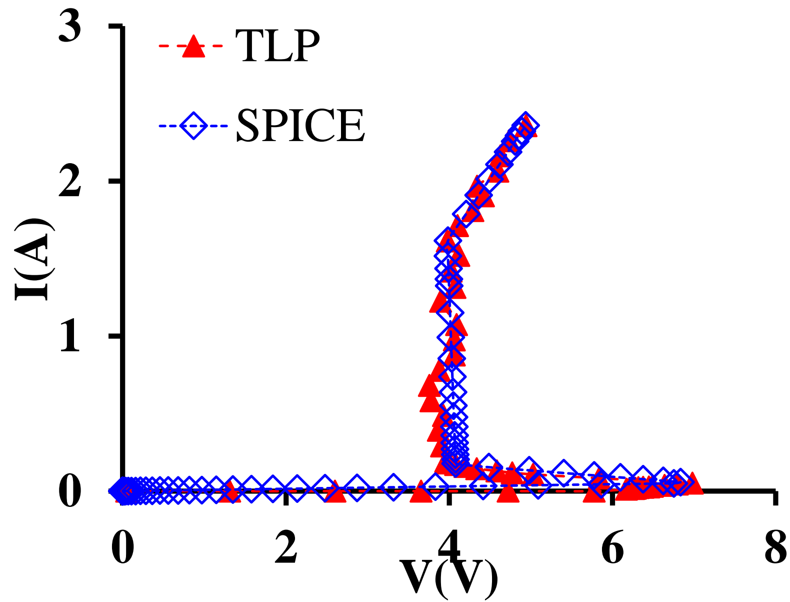


Figure 3.39 SPICE circuit simulation using behavior model matches TLP testing well for a sample RC-coupled LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=90/0.35/3µm, C=1pF and R=10KΩ

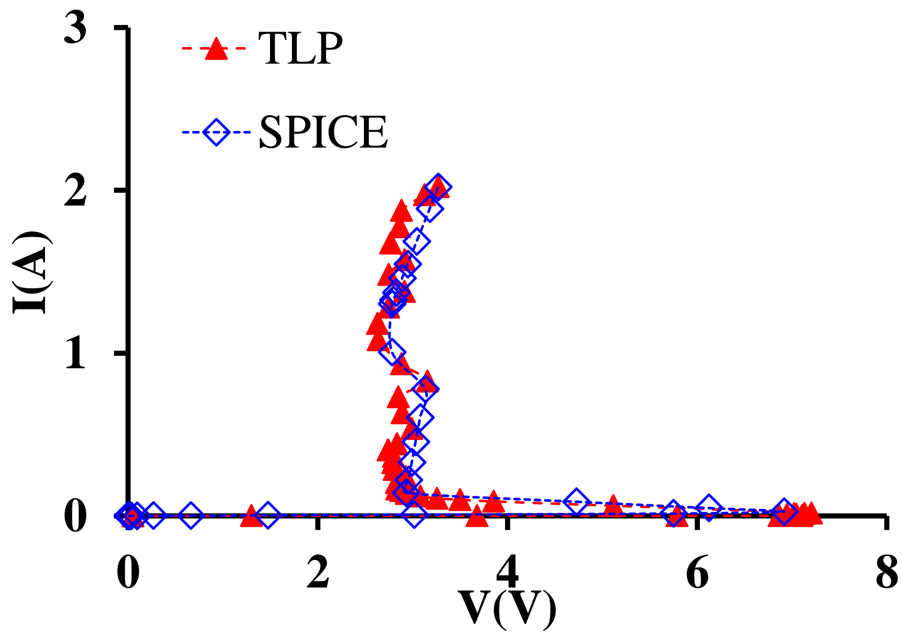


Figure 3.40 SPICE circuit simulation using behavior model matches TLP testing well for a sample gate-R LVSCR structure featuring $W/L/L_{mid\text{-}N+}$=30/0.35/1µm and R=100KΩ

3.6 HV ESD Protection Model Method and Verification

We report a new accurate Verilog-A ESD device behavior modeling technique developed for HV ESD protection IC fabricated in a BCD30V process.

3.6.1 HV ESD Protection Structure

The HV ICs designed in this work using a BCD30V require supply V_{CC}=35V and gate bias of V_{GS}=12V for operation. The breakdown voltages are BV_{GS}=36V and BV_{DS}=45V [34]. Figure 3.41 shows the full-chip HV ESD protection scheme used featuring a HV 2-SCR stack as a power clamp and a HV diode for I/O ESD protection [23]. The required HV ESD design window (Figure 1.5) is $V_{CC}<(V_{t1}, V_h)<BV$ and $I_h>>I_{CC}$ where the ESD-critical parameters (triggering and holding voltage, V_{t1} & V_h and holding current I_h) must be carefully designed to ensure proper ESD discharging while avoiding IC latch-up. Figure 3.42 shows a cross-section for the HV ESD diode (P+/NW/DNW/LNW to obtain the required V_{t1}) designed for I/O ESD protection, which achieves the required V_{t1}~15V in ESD TLP testing to meet the I/O ESD design window of (V_{GS}=12V, BV_{GS}=36V). Figure 3.43 illustrates a cross-section for the HV power clamp using a bi-directional SCR structure. In this design, a two-SCR stack is used to achieve V_{t1}~38V to meet the HV ESD design window (V_{CC}=35V, BV_{DS} =45V) for the power bus, which is confirmed in ESD TLP testing.

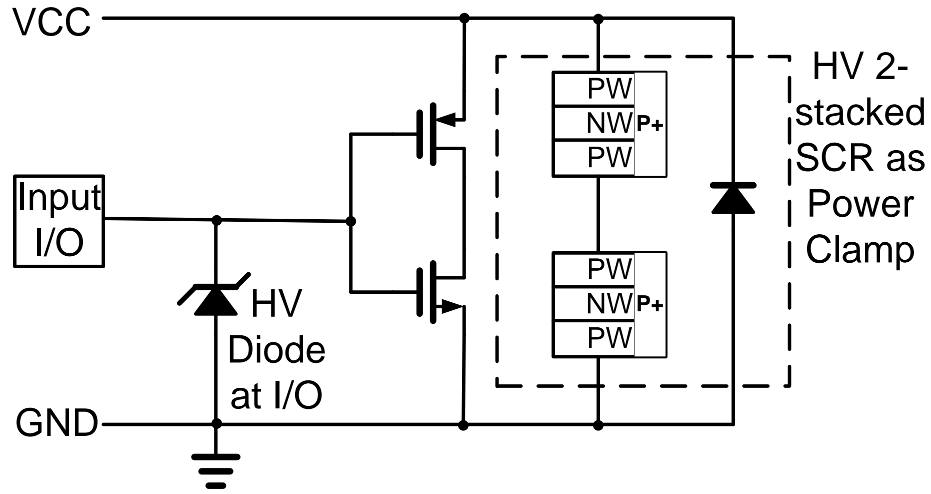
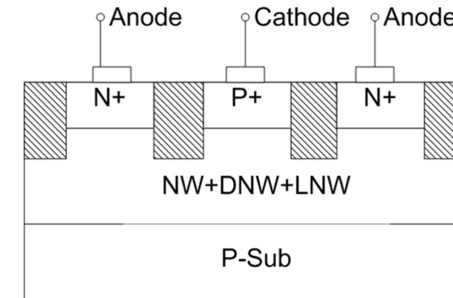
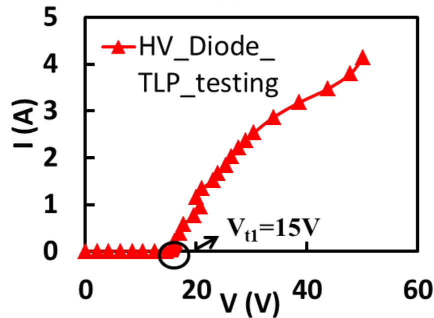


Figure 3.41 The whole-chip HV ESD protection scheme in this design consists of HV ESD diodes at I/O and stacked bi-directional SCR ESD power clamp



(a)



(b)

Figure 3.42 A cross-section (a) and measured ESD I-V curve by transmission line pulse (TLP) testing (b) for the HV ESD diode

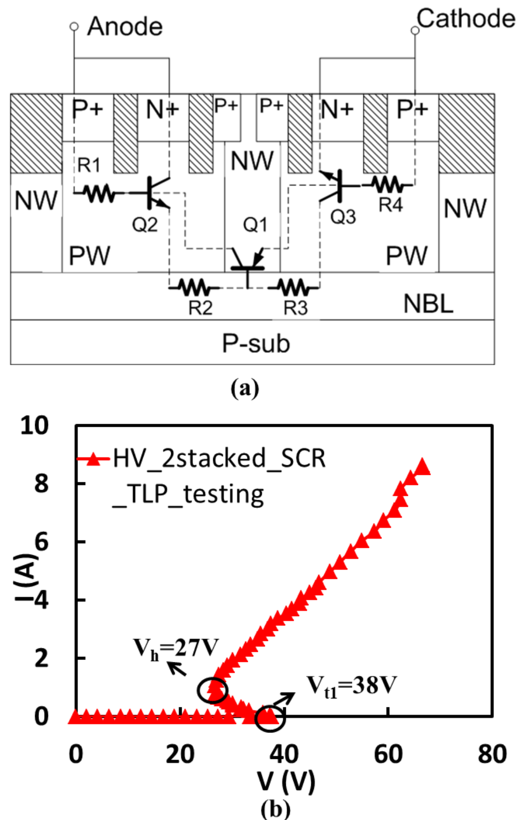


Figure 3.43 A cross-section (a) and measured ESD I-V curve by TLP testing (b) for the 2-stacked SCR HV power clamp

3.6.2 HV ESD Device Model Method

First, HV ESD devices are designed, fabricated and measured to obtain the ESD-critical parameters including triggering (V_{t1}, I_{t1}), holding (V_h, I_h), ESD discharging resistance (R_{ON}) and ESD thermal failure threshold (V_{t2}, I_{t2}). Second, the TLP testing curves are divided into several sections according to ESD functions (e.g., device off/snapback/on). Each section can be described in Verilog-A, and the fitting parameters are extracted from the TLP curve. Behavioral ESD modeling can accurately describe ESD discharging I-V behaviors piece-wisely using Verilog-A based on ESD TLP testing data. Figs. 3.44 and 3.45 show ESD curve fitting of the HV ESD diode and two-SCR

stack ESD power clamp, respectively. Next, the extracted ESD behavior model is validated by SPICE circuit simulation.

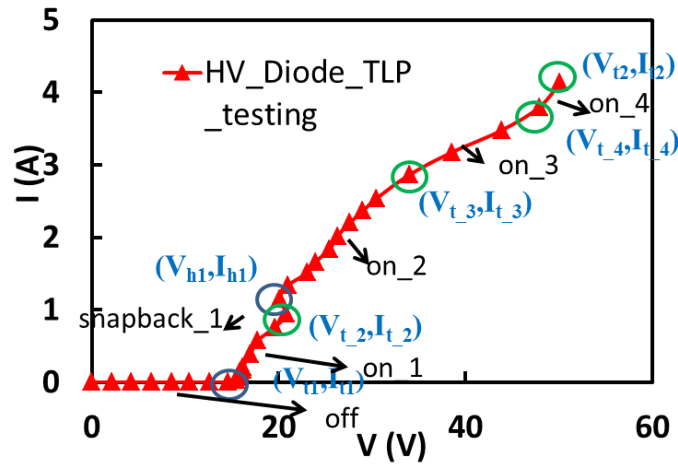


Figure 3.44 The measured, by TLP testing, ESD I-V curve for the HV I/O ESD diode is partitioned for ESD behavior modeling

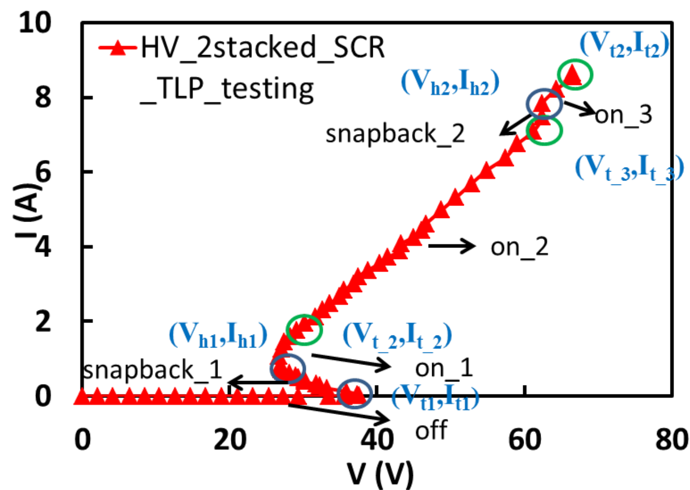


Figure 3.45 The measured, by TLP testing, ESD I-V curve for the 2-stacked SCR HV power clamp is partitioned for ESD behavior modeling

3.6.3 HV ESD Device Model Verification

Figs. 3.46 and 3.47 show that simulated ESD circuit function using the new ESD models matches TLP testing curve very well for the HV ESD diode and stacked SCR

power clamp designed in a BCD30V process. The new HV ESD behavior modeling technique, while avoiding the complexity in physics-based ESD modeling, can provide accurate and scalable ESD behavior models, which enables whole-chip ESD protection circuit design simulation, optimization and prediction that resolves one of the biggest design problems in practical HV IC designs.

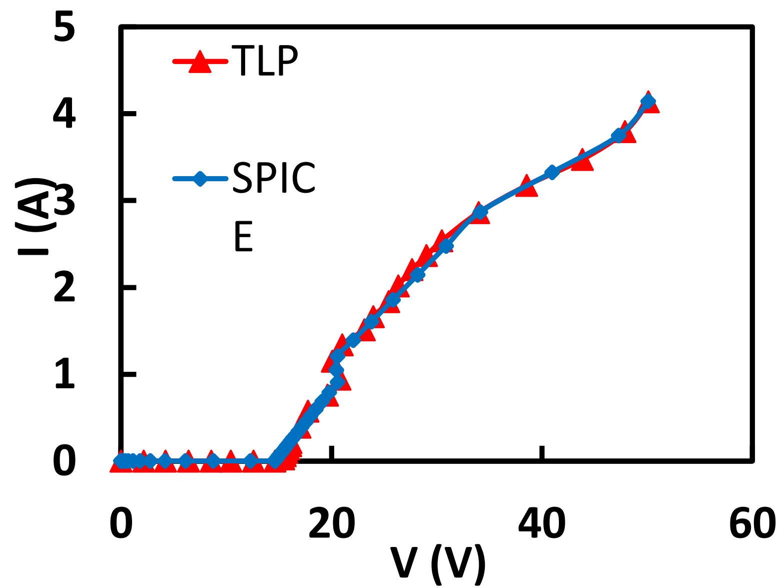


Figure 3.46 SPICE circuit simulation for a sample HV diode ESD device matches the TLP testing curve well

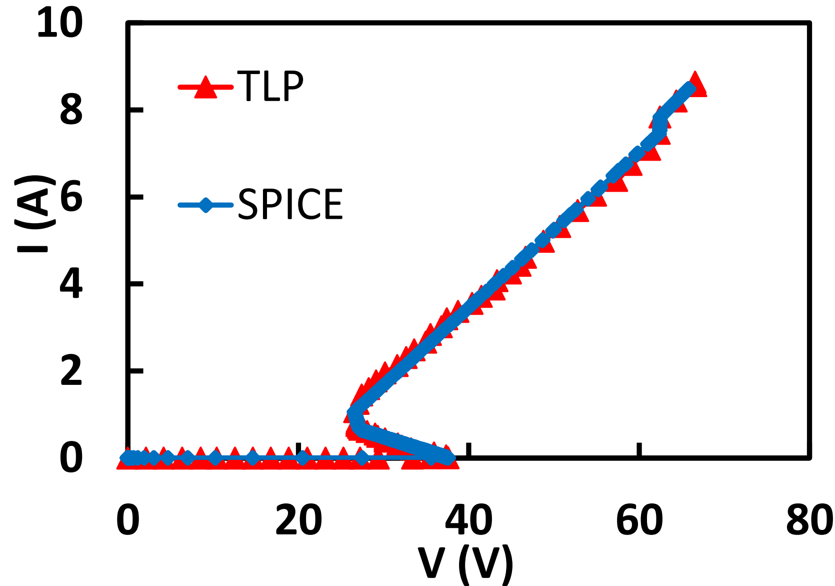


Figure 3.47 SPICE circuit simulation for a sample HV 2-stacked SCR ESD device matches the TLP testing curve well

3.7 28nm CMOS ESD Protection Model Method and Verification

ESD design is very challenging to high-frequency multi-Gbps IC designs in sub-32nm CMOS because ESD-induced capacitance (C_{ESD}) can inevitably and fatally affect IC data rates [3]. The solution is to explore novel ESD structure and ESD-IC co-design technique to achieve design balance at chip level [44]. We report a new accurate Verilog-A ESD device behavior modeling technique developed for Gated diode and DTSCR ESD protection IC fabricated in foundry 28nm CMOS.

3.7.1 28nm CMOS ESD Protection Structure

Splits of various ESD structures were designed including gated diodes and diode-triggered SCR (DTSCR) ESD structures. Step-1 was to conduct mixed-mode ESD

simulation to optimize ESD devices and evaluate ESD I-V behaviors and parasitic effects [22].

Figure 3.48 indicates the Gated N+PW diode x-section in 28nm CMOS. Gated diode contains a PN junction, which is formed by N+/P-Well in CMOS IC process. Its transient ESD behaviors is evaluated by ESD simulation shown in Figure 3.49, revealing the ESD discharging and thermal details. It clearly shows that a poly-gated diode has high ESD capability due to straight ESD discharging current flow. These details are critical to properly optimize ESD structures per high-speed IC design specs [41].

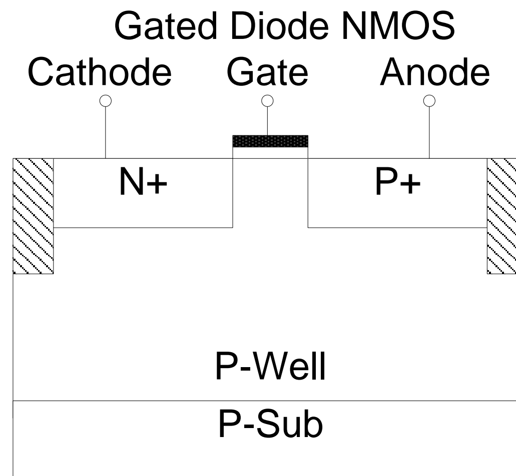


Figure 3.48 Gated diode cross-section

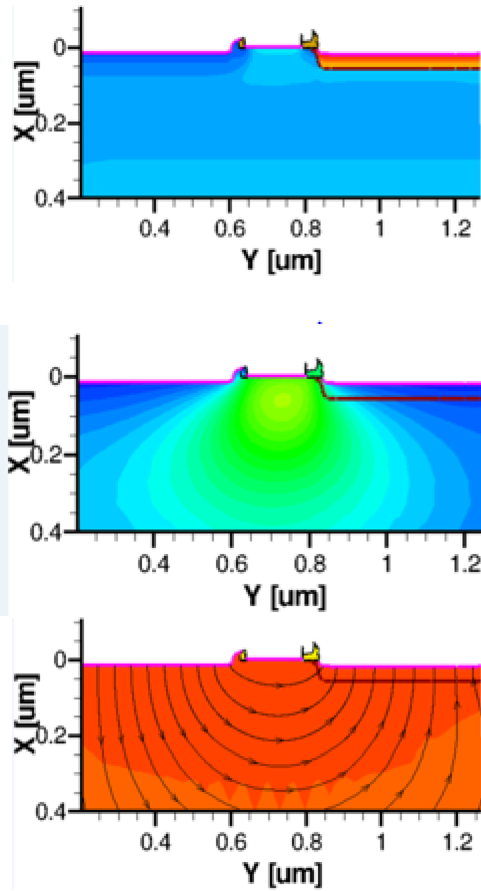


Figure 3.49 Simulation reveals ESD behaviors for gated diode ESD structures: X-section (upper), temperature contours and heating effect (middle), and ESD discharging current flows (lower)

Diode triggered silicon controlled rectifiers (DTSCR) is an attractive ESD protection device in advanced CMOS technologies due to their low capacitive loading and high failure current compared to diode based or NMOS based devices [31]. The DTSCR's tunable trigger/holding voltages offer design flexibility for a range of different I/O voltage requirements. Figure 3.50 shows simulated ESD discharging details for a sampled DTCSR ESD structure using mixed-mode ESD simulation. The external trigger diode chain injects enough current into the SCR gates G2 and so has a hot spot during ESD stress conditions, as shown in Figure 3.50.

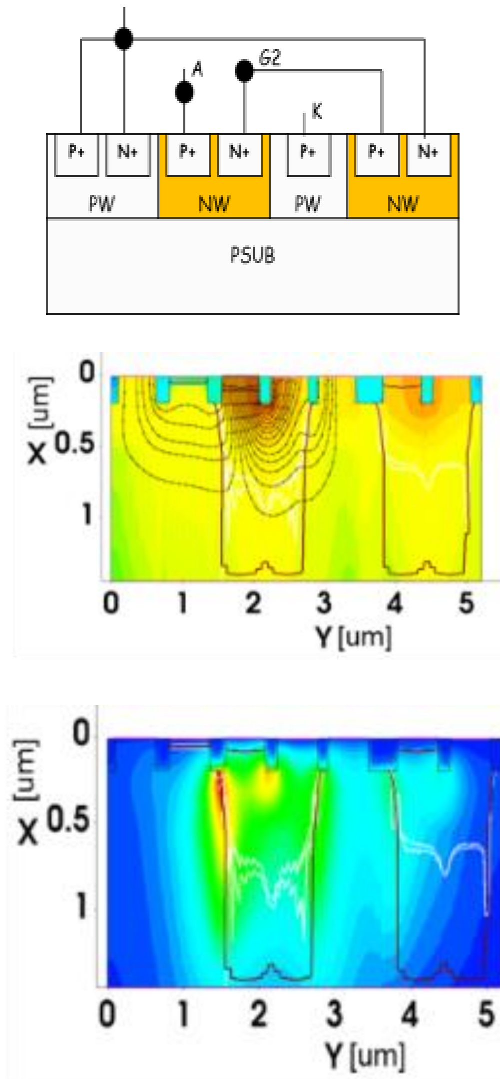


Figure 3.50 X-section of a sample DTSCR ESD structure (upper) and its simulated ESD discharging current flow (middle) and temperature contours (lower)

3.7.2 28nm CMOS ESD Device Model Method

Accurate ESD device models are essential to chip-level ESD circuit simulation, which is not supported by the typical ESD parasitic models from foundries. New scalable ESD behavioral modeling technique is developed in this work. Figure 3.56 shows measured I_{t2} and R_{ON} results for sample gated diode ESD devices of varying sizes by TLP testing.

The ESD I-V curves by TLP testing are partitioned into segments for accurate ESD parameter extraction for behavioral modeling using Verilog-A language. Figure 3.57 shows partitioning for sample gated diode and DTSCR ESD devices.

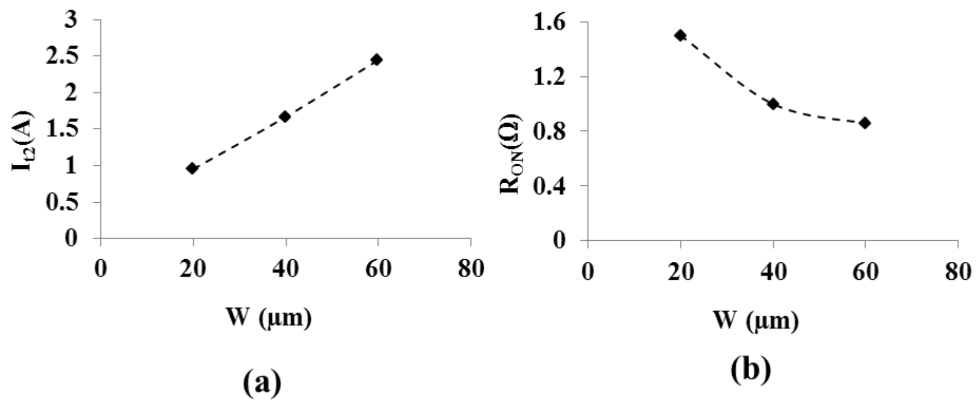


Figure 3.51 Measured I_{t2} (a) and R_{ON} (b) for sample N+PW gated diodes ESD devices of varying sizes (W) by TLP testing

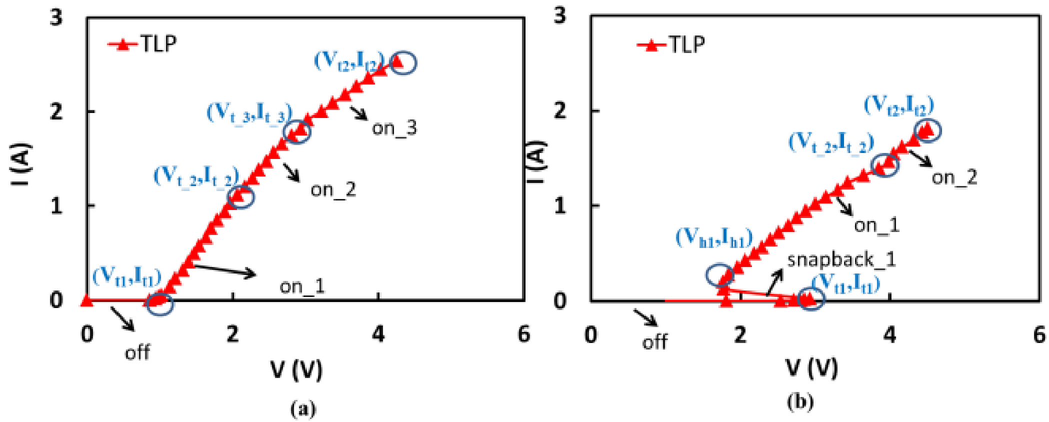


Figure 3.52 Partitioning transient ESD I-V curves from TLP testing for ESD behavior modeling for sample (a) N+PW gated diode and (b) DTSCR

3.7.3 28nm CMOS ESD Device Model Verification

ESD size splits and TLP testing are critical to develop accurate and scalable ESD behavioral models, which are used to conduct chip-level ESD circuit simulation using ESD test equivalent circuits, as shown in Figure 3.58 for a HBM ESD testing standard.

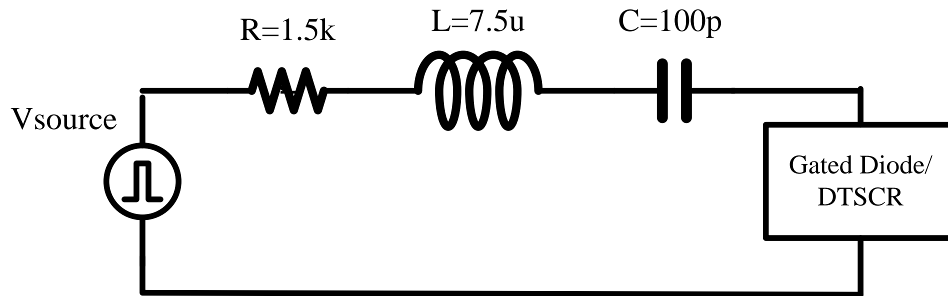


Figure 3.53 A HBM ESD test equivalent circuit for ESD circuit simulation

Figure 3.54 and Figure 3.55 compare TLP testing curves and SPICE-based ESD circuit simulation using the extracted ESD behavioral models for sample gated diode and DTSCR ESD devices of various sizes, which shows excellent ESD circuit simulation accuracy compared to ESD testing results. This is very critical to realizing ESD circuit simulation and ESD-IC co-design simulation at full chip level [45].

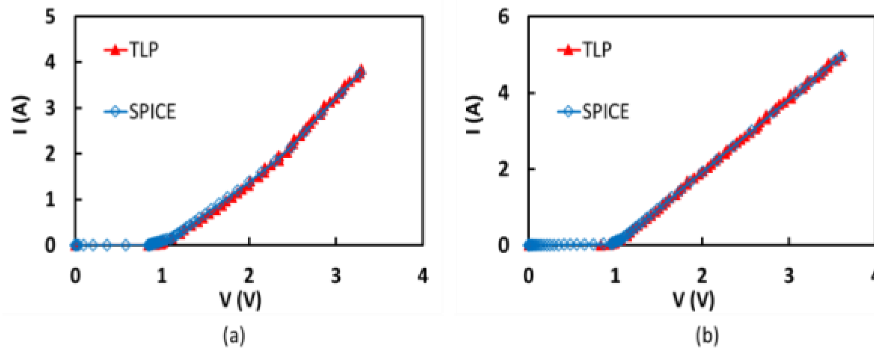


Figure 3.54 SPICE ESD circuit simulation using the extracted ESD behavioral models matches ESD TLP testing curves well for sample N+PW gated diode: (a) W/L=100μm/0.54μm (HBM 3KV), and (b) 120μm/0.54μm (4KV)

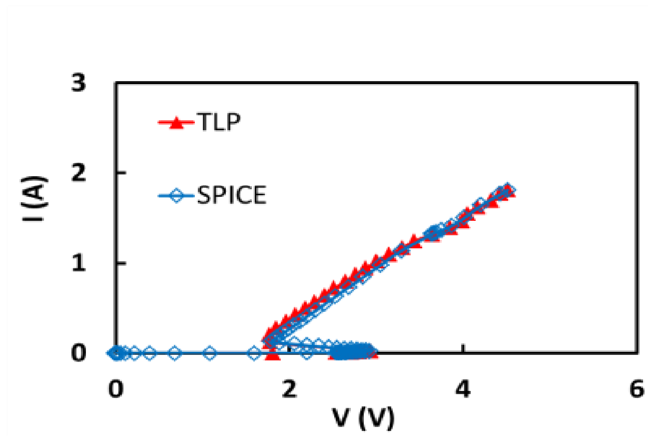


Figure 3.55 SPICE ESD circuit simulation using the extracted ESD behavioral models matches ESD TLP testing curve well for a sample DTSCR (W=50μm, 2KV)

Chapter 4 Design BGA Pad-Ring Array ESD Design Verification

4.1 Introduction

There are two popular types of IC assembly methods: wire bonding and flip-chip. For complex and advanced ICs, flip chip technique using ball grid array (BGA) pad-ring arrays is a popular technology for small footprint chips used in size-sensitive electronics, such as mobile phones and wearable device [42]. Figure 4.1 shows a BGA pad-ring array used in this design of a VLC transceiver implemented in 180nm BCD technology [30]. ESD protection structure is integrated to each IO pad in the array where the supply and GND pad locations are fixed. However, ESD protection design for ICs using large BGA pad-ring array is an emerging challenge due to several reasons. First, unlike chips using wire bonding, ICs using BGA pad-ring arrays have constraints in on-chip ESD protection design where I/O pads, supply and ground (GND) pads are fixed in a given BGA pad-ring array determined by the chip performance. Hence, where to place an ESD structure becomes a real layout design headache [53, 54]. Second, with no layout flexibility for placing ESD structures in a BGA pad-ring array, ESD metal routing is very challenging that will seriously affect ESD protection performance at chip level. Between any given IO pad with an ESD protection structure underneath and a supply/GND pad with a fixed location, there will be many possible ESD metal routes. For a large chip using BGA pad-ring array, different ESD metal routing may significantly take effect on-chip ESD protection design due to the substantially different bus resistance associated with ESD metal routes even using the same ESD device for a given pad.

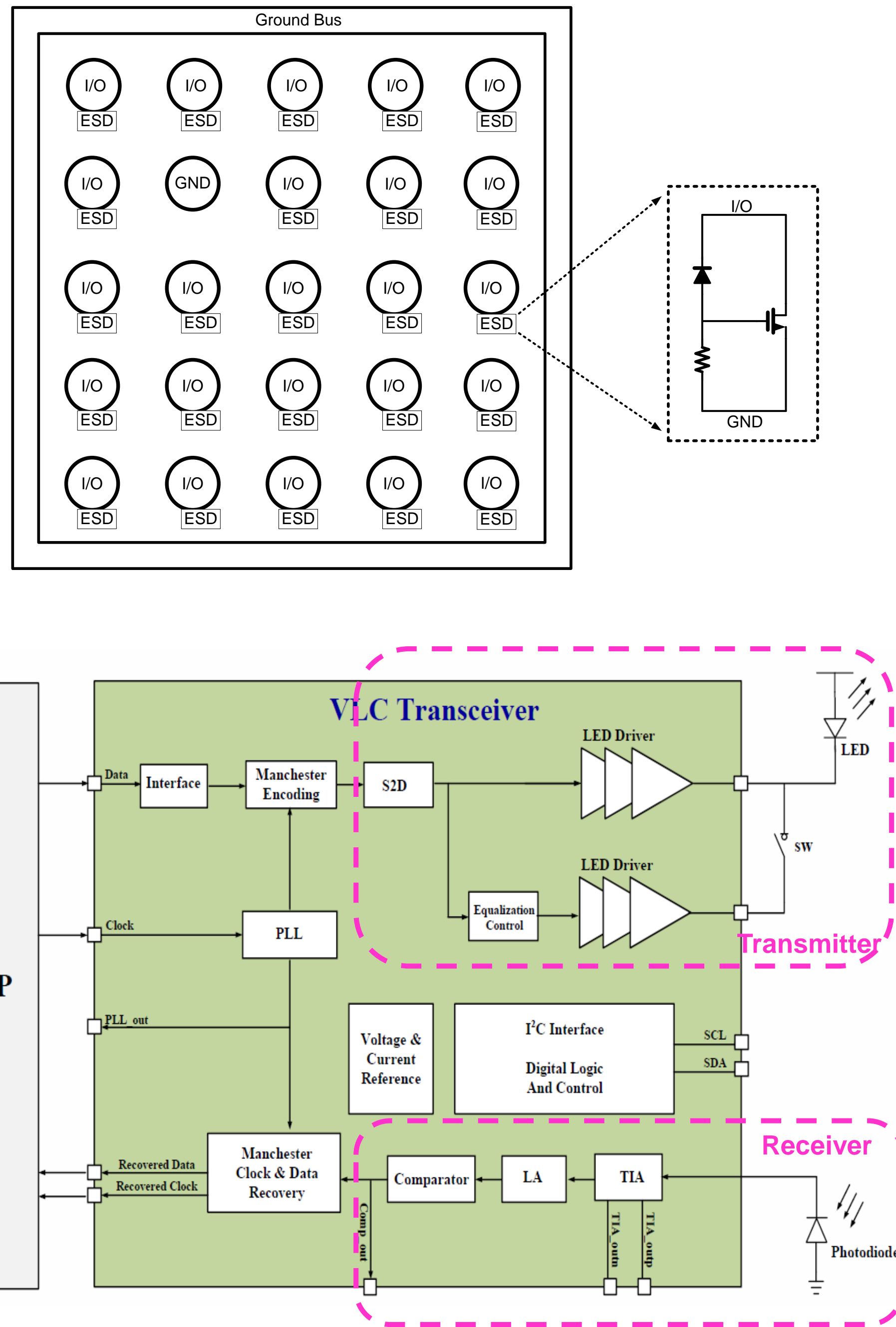


Figure 4.1 Illustration of BGA pad-ring array (Upper) used for flip-chip based VLC transceiver (Lower) in this design.

4.2 ESD Design Split and ESD Netlist Extraction

Flip chip technique using BGA pad-ring arrays is a popular technology for small footprint chips used in size-sensitive electronics, such as mobile phones and wearable device. Figure 4.1 shows a BGA pad-ring array used in this design of a VLC transceiver implemented in 180nm BCD technology [30]. ESD protection structure is integrated to each IO pad in the array where the supply and GND pad locations are fixed.

Design splits were used in this VLC chip design to investigate path resistance impacts on full-chip ESD protection for different ESD metal interconnect routes. Figure 4.2 shows the design splits consists of two different ESD metal routes between an IO pad and GND pad where two IO pin were used (i.e., SCL pin and SDA pin in the VLC transceiver) and the same ESD device was used for the SCL and SDA pads for all ESD metal route splits.

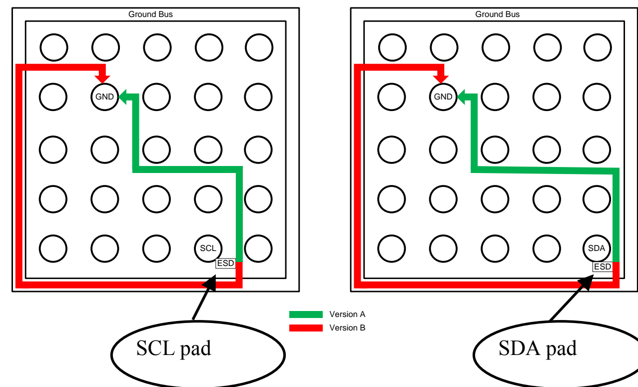


Figure 4.2 Two ESD metal route splits were designed between a given IO pad and a fixed GND pad in the flip-chip VLC IC showing two possible ESD current discharging paths for ESD route A and B in this design.

To enable ESD-function-based whole-chip ESD protection design verification at layout level, it is critical to have the capability of extracting arbitrary ESD structures and their ESD-critical parameters from full-chip layout design (GDSII data file), which is enabled by our ESD Extractor CAD tool introduced in chapter 2.

For accurate chip-level ESD protection circuit simulation, bus resistance of ESD structures must be included in addition to considering the ESD-critical parameters, because the ESD bus resistance may have significant impact on ESD clamping voltage, which is a key factor to breakdown-induced ESD failure on a chip. The ESD metal bus resistance can be extracted by ESD Extractor tool. The geometrical dimension width and length of ESD metal interconnects are extracted from the layout file and the bus resistance can be calculated according to related metal sheet resistivity and layout data.

The VLC transceiver IC in this design uses two types of ESD structures. Figure 4.3 shows the simplified schematic and layout of a gate-coupled NMOS (GCNMOS) ESD structure used for the digital and analog domain. Figure 4.4 depicts a diode type ESD protection structure used for the power domain. These ESD devices are integrated to the pads in the BGA pad-ring array. Using the ESD Extractor, ESD-critical parameters for the extracted pad ESD devices and the ESD metal bus resistance associated with the given IO pad and GND pad in the BGA pad-ring array are extracted as summarized in Table 4.1 . It clearly shows that the ESD protection schemes using the same GCNMOS and diode ESD devices for a given pair of IO and GND pads with different ESD metal routes result in different ESD metal bus resistance, which will affect chip-level ESD protection.

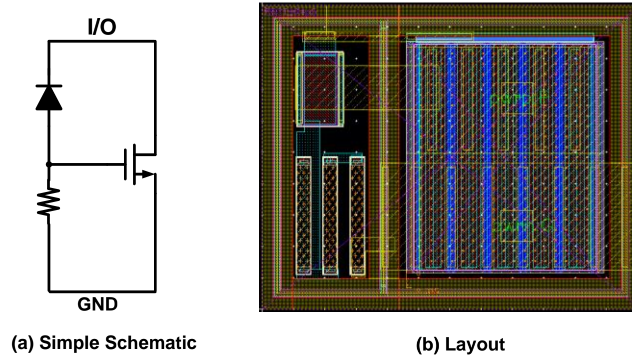


Figure 4.3 Schematic and layout for a GCNMOS ESD protection structure used for the digital and analog domain in this design

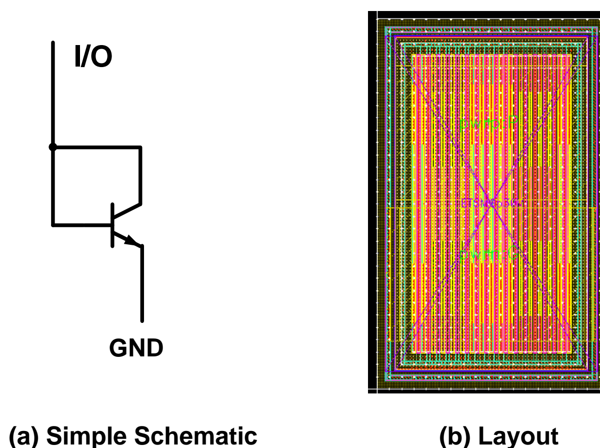


Figure 4.4 Schematic and layout for ESD protection in power domains used in this design

Table 4.1 Extracted ESD-critical parameters and ESD bus resistance for ESD metal route A and B

	V_{t1} (V)	I_{t1} (mA)	V_h (V)	I_h (A)	V_{t2} (V)	I_{t2} (A)	R (ohm)
GCNMOS	8.2	1.1	5.7	0.17	7.8	3.92	0.6
Diode type	29.5	15.5	25.5	0.43	46.5	2.6	17.3
SCL_VersionA	N/A	N/A	N/A	N/A	N/A	N/A	0.27
SCL_Version B	N/A	N/A	N/A	N/A	N/A	N/A	0.76
SDA_Version A	N/A	N/A	N/A	N/A	N/A	N/A	0.34
SDA_Version B	N/A	N/A	N/A	N/A	N/A	N/A	0.76

4.3 Full-Chip ESD Circuit Verification

The new ESD behavior modeling technique introduced in chapter 3 is used to model the GCNMOS ESD structures fabricated in this work to enable whole-chip ESD

circuit design simulation and verification. It utilizes Verilog-A language to describe ESD-critical parameters extracted from ESD Extractor CAD tool.

Figure 4.5 depicts the flow chart for the new ESD behavior model and ESD metal interconnect resistance extraction technique developed in this work. The ESD-critical parameters of the extracted ESD protection structures and the ESD bus resistance associated with a specific ESD metal route between a given IO pad and GND pad are extracted by ESD Extractor CAD tool for the given layout. The behavior model of the extracted ESD device is described section-wisely by the ESD-critical parameters in Verilog-A. Comprehensive ESD TLP testing was conducted according to human body model (HBM) ESD standard where ESD pulse rise time and duration are t_1~10ns and t_d~100ns, respectively. The ESD discharge path formed by ESD behavior model and bus resistance is then verified in SPICE circuit simulation for the VLC IC and is compared with chip level ESD TLP testing results to verify whole-chip ESD protection circuit design.

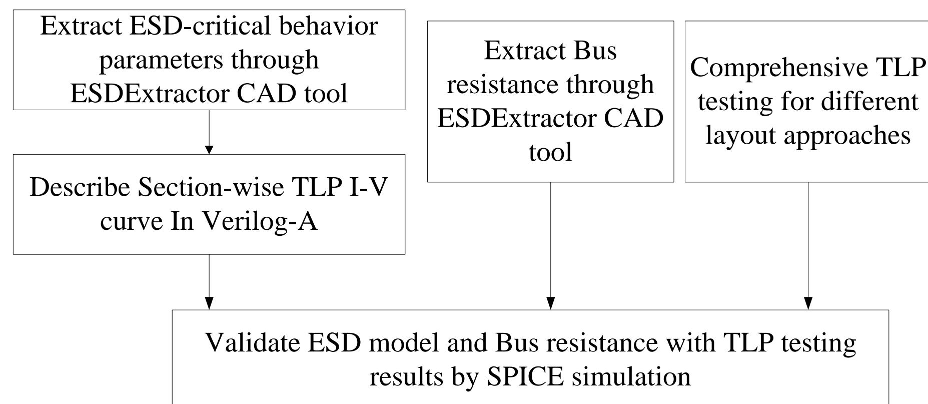


Figure 4.5 A flow chart for ESD behavior model and ESD bus resistance extraction and validation

Figure 4.6 is the layout for the VLC transceiver chip designed and fabricated in a commercial 180nm BCD technology in this work. For comparison, two ESD pad-ring patterns, i.e., version A (VA) and version B (VB), were designed between the SCL/SDA and GND pads using the same diode ESD device. Figure 4.7 shows layout floor plan of the BGA pad-ring array where an ESD structure is integrated to each pad including the SCL/SDA IO pads in the design splits.

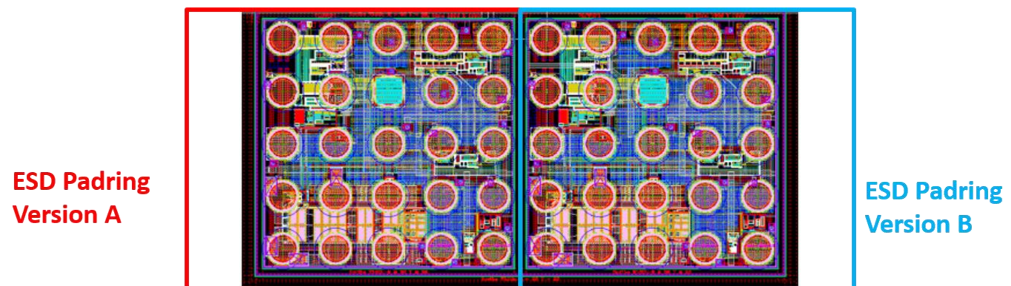


Figure 4.6 The VLC die diagram shows the ESD metal path splits (i.e., path A and path B) in the BGA pad-ring array

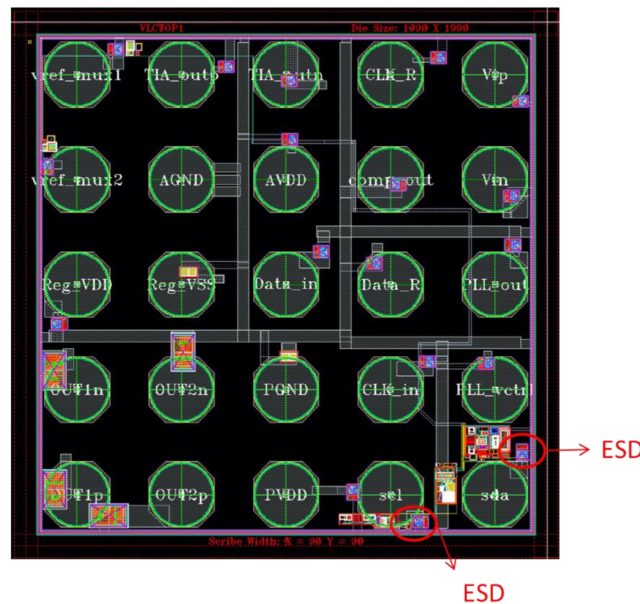


Figure 4.7 Layout floorplan for one VLC IC split where each PI pad has its own ESD device integrated

Complete ESD characterization was performed for all design splits by ESD TLP testing. Figure 4.8 and Figure 4.9 show the ESD discharging I-V curves obtained by TLP testing for the SCL-GND and SDA-GND cases, respectively, both have two ESD metal routes (i.e., A and B). It is readily observed that different ESD metal routes resulted in substantial difference in the total ESD discharging path resistance, which will determine the actual chip-level ESD protection performance. The V_{t1} and V_h remain the same for the two splits because they are determined by the same ESD device used. However, the change in ESD metal resistance resulted in change in ESD clamping voltage (V_{t2}) and ESD heating, which will determine the actual chip-level ESD protection level, i.e., about 40% chip-level ESD performance degradation for ESD route-B with a narrower and longer ESD discharging path.

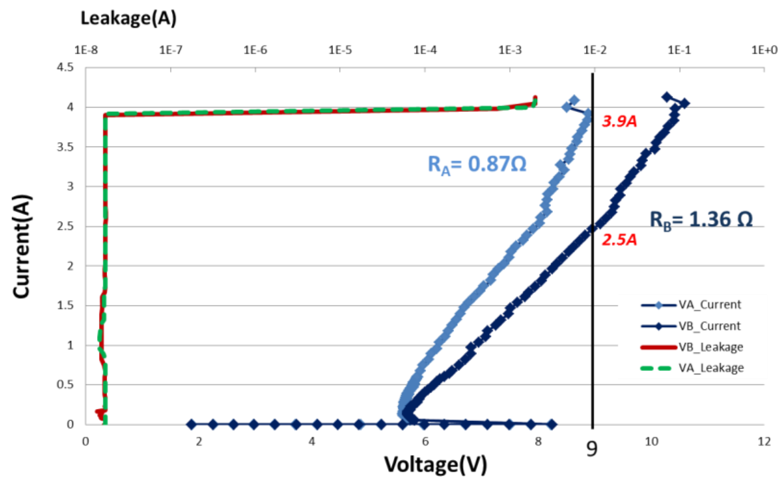


Figure 4.8 SCL ESD TLP testing results with version A (VA) and version B (VB)

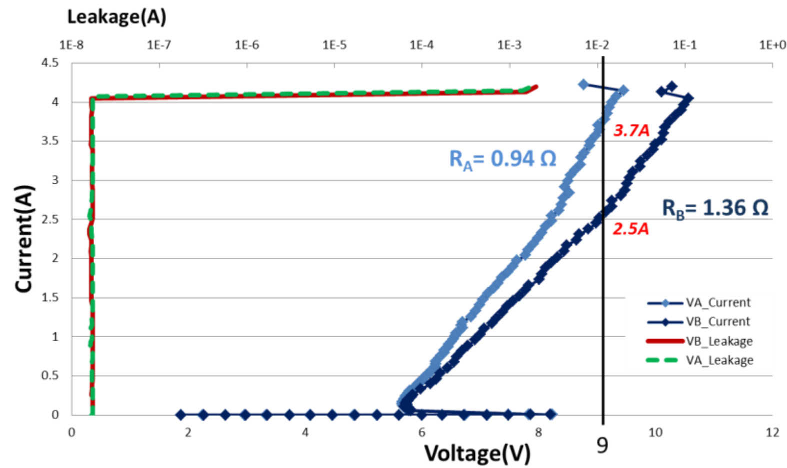


Figure 4.9 SDA ESD TLP testing results with version A (VA) and version B (VB)

The new function-based chip-level ESD circuit verification technique was validated by SPICE simulation and TLP testing. Figure 4.10 shows a schematic for ESD circuit simulation for GCNMOS ESD structure. HBM ESD testing standard was used to compare with TLP testing results for the ESD metal routing splits. ESD Extractor tool was used to extract the ESD devices, their ESD-critical parameters and the ESD metal path resistance from the layout file. ESD behavior models were obtained for the extracted ESD devices. SPICE circuit simulation for ESD performance was then conducted for all design splits using the extracted ESD models and path resistance. Figure 4.11 - Figure 4.14 show comparison between SPICE ESD circuit simulation and TLP testing for all design splits. Clearly, ESD circuit simulation results match TLP testing curves very well for all design splits thanks for the accurate extraction of ESD behavior models and ESD metal path resistance from the layout data using the new function-based ESD circuit verification method.

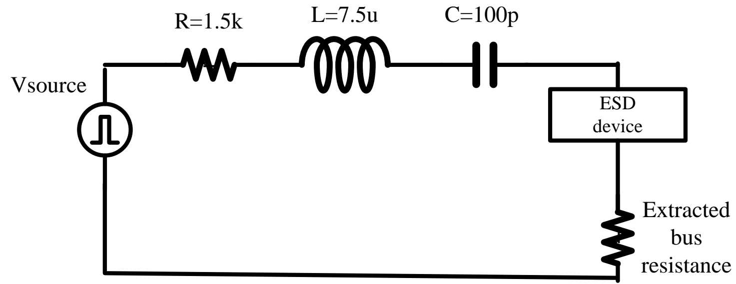


Figure 4.10 Schematic for HBM ESD circuit simulation for ESD protection circuit including ESD device and ESD metal path resistance

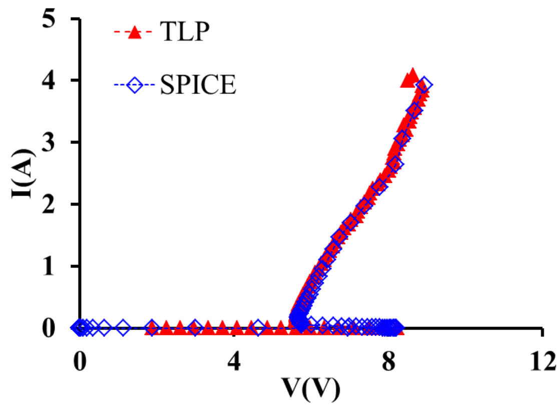


Figure 4.11 SPICE ESD circuit simulation matches TLP testing well for the design split of SCL-GND with ESD metal route Version A

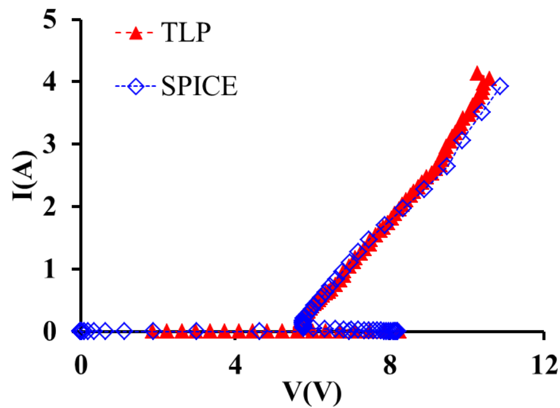


Figure 4.12 SPICE ESD circuit simulation matches TLP testing well for the design split of SCL-GND with ESD metal route Version B

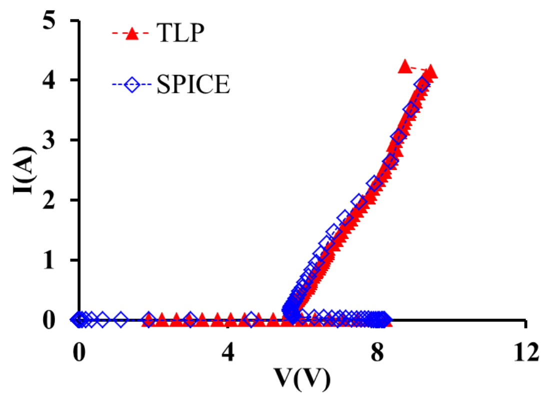


Figure 4.13 SPICE ESD circuit simulation matches TLP testing well for the design split of SDA-GND with ESD metal route Version A

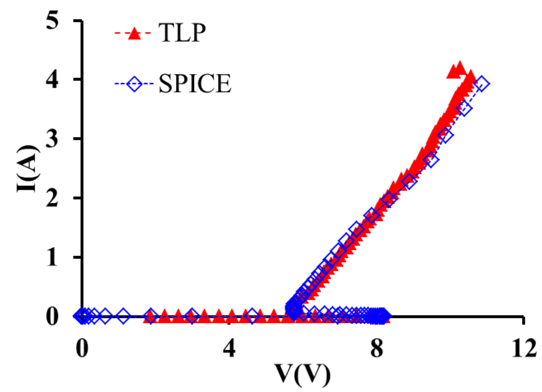


Figure 4.14 SPICE ESD circuit simulation matches TLP testing well for the design split of SDA-GND with ESD metal route Version B

Chapter 5 Conclusions

This dissertation reported a new chip-level ESD CAD tool, which extracts ESD devices from layout files, generates ESD netlist, simulates ESD discharge function on chip level and conducts full-chip ESD zapping test by simulation. In consideration of achieving truly full-chip level ESD protection design verification and prediction, challenges and issues of current TCAD-based and ECAD-centric ESD CAD tools are discussed and investigated. Regarding to all these issues, the new CAD tool is designed with several unique algorithms and a smart ESD parametric checking mechanism, which takes full consideration of ESD protection operation principles.

This CAD tool consists of three modules: ESD Extractor, ESD Inspector and ESD Zapper. ESD Extractor is a new function to extract arbitrary ESD structures at full chip level. Decomposed-based subgraph isomorphism algorithm is invented for ESD devices extraction to improve time efficiency. ESD Inspector is to remove non-critical ESD devices extracted based upon a novel smart parametric checking mechanism. In addition, ESD Zapper is developed to perform ESD protection zapping test simulation by implementing Dijkstra's algorithm to resolve the problem of finding the critical ESD discharging path. Last but not the least, full chip ESD protection was designed and verified the CAD tool implemented in 0.35 μm BiCMOS technology.

To enable ESD-function-based whole-chip ESD protection design verification at layout level, ESD Extractor CAD module was at first investigated and designed. Several challenges exist for ESD protection device extraction tool and so the ESD Extractor was designed to have the capability of extracting any possible ESD-type structures and their

ESD-critical parameters from full-chip layout design. According to the unique features of ESD protection devices, a new device recognition algorithm based on a decomposition approach, called decomposition-based subgraph isomorphism approach, to improve ESD device recognition efficiency was designed. Unlike the top-down approach that handles each MG individually, this new algorithm first explores the relationship between the device MGs by a decomposition procedure, and then the TG is matched with the decomposition results. The novel decomposition procedure makes the device recognition procedure not heavily dependent upon the number of device MGs as does the top-down approach, and heavily improves the time efficiency than the top-down approach.

The ESD extractor extracts all intentional and parasitic ESD devices from a layout file, however, the number of the ESD devices are so large that it will take effect to the time efficiency for the schematic level simulation. Therefore, it is critical to identify those life-threatening ESD-type parasitic devices that designers should really concern. Therefore, ESD Inspector is developed to remove non-critical ESD devices extracted based upon a novel smart parametric checking mechanism. Several criteria, including triggering criteria, holding criteria, was designed to implement the smart parametric checking to remove the non-critical ESD devices.

To resolve the problem of identifying the critical ESD discharging paths on a chip for whole-chip ESD protection circuit design verification ESD zapper was designed to perform whole-chip checking to identify critical ESD discharging paths. The procedure that the ESD netlist is transformed to a novel weighted graph was presented. Then

Dijkstra's algorithm was discussed in details and designed to find the critical ESD discharging paths.

Finally, a full chip ESD protection application example was designed and verified the CAD tool implemented in 0.35 μm BiCMOS technology. The extraction netlist, final netlist, and the critical discharging path was observed from the example.

Among all the ESD device models reported for traditional diode and MOSFET type ESD structures, due to complex ESD behaviors, particularly the electro-thermal-process-device-circuit-layout coupling effects, existing ESD models have limited accuracy in describing complex ESD physics, such as thermal boundary condition and snapback I-V behavior. In this thesis a new scalable ESD behavioral modeling technique is presented, which uses Verilog-A to develop accurate ESD behavior models for novel nano crossbar ESD protection structures, novel 3D field-programmable ESD protection structures including SONOS and NCD ESD devices, silicon controlled rectifier (SCR) based ESD protection structures, HV diode and SCR ESD protection structures, 28nm gated diode and DTSCR ESD protection structures.

The new ESD behavior modeling technique enabled accurate description of ESD device behaviors without being limited by the complex, and often unknown, ESD device physics. And it overcame the difficulties to extract complicated parameters based on high current and thermal physics. Firstly, the relationship between ESD-critical parameters and design splits was established. After extracting ESD-critical parameters from TLP testing results and analysis, a scalability model per device dimensions can be set up. Next, the TLP curves are divided into several section-wise segments according to ESD

functions. Each segment of the TLP testing curve can be modeled by a formula to describe the corresponding ESD function in Verilog-A and the fitting parameters can be extracted from the TLP curve directly correlated with device dimensions. The new ESD behavior modeling technique was fully verified by SPICE circuit simulation and TLP testing, which will enable whole-chip ESD circuit design optimization and verification.

At last, flip chip technique using ball grid array (BGA) pad-ring arrays is a popular technology for small footprint chips used in size-sensitive electronics. However, for a large chip using BGA pad-ring array, different ESD metal routing may significantly take effect on-chip ESD protection design due to the substantially different bus resistance associated with ESD metal routes even using the same ESD device for a given pad.

In this dissertation, a BGA pad-ring array with different ESD metal routing for a VLC transceiver implemented in 180nm BCD technology was verified at whole-chip level. Two types of ESD were designed, one for the digital & analog domain (up to 5V) and the other for the power domain (up to 30V). The ESD structures and their ESD-critical parameters from full-chip layout design (GDSII data file), were extracted by our ESD Extractor CAD tool. For accurate chip-level ESD protection circuit simulation, the ESD metal bus resistance was extracted by ESD Extractor tool. The geometrical dimension width and length of ESD metal interconnects are extracted from the layout file and the bus resistance can be calculated according to related metal sheet resistivity and layout data. The new ESD behavior modeling technique was used to model the GCNMOS ESD structures fabricated in this work to enable whole-chip ESD circuit design simulation and verification. It utilizes Verilog-A language to describe ESD-critical

parameters extracted from ESD Extractor CAD tool. The extraction and modeling was validated by SPICE simulation and TLP testing for different ESD metal routing.

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