UNIVERSITY OF CALIFORNIA, SAN DIEGO

Ultra-Low Noise Current Measurement Front-Ends for Biological Applications

A dissertation submitted in partial satisfaction of the
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in

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by

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Professor Daniel Sievenpiper

2018

The Dissertation of Chung-Lun Hsu is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California, San Diego

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DEDICATION

To my family.

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PUBLICATIONS

Chung-Lun Hsu, Alexander Sun, Yunting Zhao, Eliah Aronoff-Spencer, and Drew A. Hall. A 16×20 Electrochemical CMOS Biosensor Array with In-Pixel Averaging Using Polar Modulation. *IEEE Custom Integrated Circuits Conference* (*CICC*), San Diego, CA, USA, Apr. 8-11, 2018.

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Chung-Lun Hsu, A. G. Venkatesh, Haowei Jiang, and Drew A. Hall. Hybrid Semi-Digital Transimpedance Amplifier for Nanopore-Based DNA Sequencing. *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Lausanne, Switzerland, October 22-24, 2014.

PATENTS

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Chung-Lun Hsu, Drew A. Hall. Wide Dynamic Range Current Measurement Front-End. US Provisional Patent

Abstract OF THE DISSERTATION

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Chung-Lun Hsu

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2018

Professor Drew A. Hall, Chair

Current measurement front-ends are widely used to provide a high precision, real-time signal acquisition for biological applications where charge perturbations occur during biological interactions. The requirement of the high dynamic range in front-ends has become imperative for high sensitivity biosensors; however, designing front-ends with high dynamic range is challenging in advanced CMOS process nodes with reduced supply voltages where the minimum and maximum detectable signals are determined by circuit noise and power supply voltage, respectively.

In this dissertation, I present several ultra-low noise current measurement front-ends for biosensing applications that aim to address this issue. The first work was designed for nanopore-based DNA sequencing. A hybrid semi-digital transimpedance amplifier senses the minute current signatures introduced by single-stranded DNA (ss-DNA) translocating through a nanopore, while discharging the baseline current using a semi-digital feedback loop. The amplifier achieves fast settling by adaptively tuning a DC compensation current when a step input is detected. A noise cancellation technique reduces the total input-referred current noise caused by the parasitic input capacitance. The amplifier has 31.6 MΩ mid-band gain, 950 kHz bandwidth, and 8.5 fA/√Hz input-referred current noise, a 2× noise reduction due to the noise cancellation technique. This system is demonstrated by capturing ssDNA translocation events.

The second front-end is a new current-input analog-to-digital converter (ADC) architecture, an asynchronous Hourglass structure that provides both low-noise amplification while decoupling the maximum detectable signal from the supply voltage, and first-order quantization noise-shaping. By eliminating the need for the reset switch in a capacitive transimpedance amplifier (C-TIA) and the feedback digital-to-analog converter in a delta-sigma modulator and compensating the excess loop delay, this Hourglass ADC achieves over 160 dB dynamic range (sub-pA to >10 μA), sub-pA_{rms} input-referred noise, and a conversion time of 400 ms – 2.5× faster than the state-of-the-art.

The linearity and power efficiency of the Hourglass ADC is further improved when implementing the ADC in a closed loop structure where a predictive I-DAC provides a coarse estimate of the current and the Hourglass ADC processes only the residue. A calibration technique is proposed to optimize the power consumption in the C-TIA and improve the current-to-frequency (*I*-to-*F*) linearity. This closed-loop Hourglass ADC achieved Shreier FOM of 197 dB with a 7 ppm linearity error over a 160 dB dynamic range from 100 fA to 10 μA.

Chapter 1

Introduction

1.1 Research Motivation

Over the past three decades, biosensors have been promising tools to provide better stability and sensitivity compared to traditional methods in many fields, namely medical and biological applications. The recent trend in biosensing technology has taken this equipment from simple and cheap components to the integration of several sensor systems into a single unit capable of detecting multiple analytes, making these systems smaller and tailored for particular applications. For example, biosensors can be integrated into mobile phone systems, making them user-friendly and accessible to a large number of users. To further reduce the cost and size, novel signal measurement front-ends with an ultra-low noise and high input dynamic range are needed to make these innovations possible.

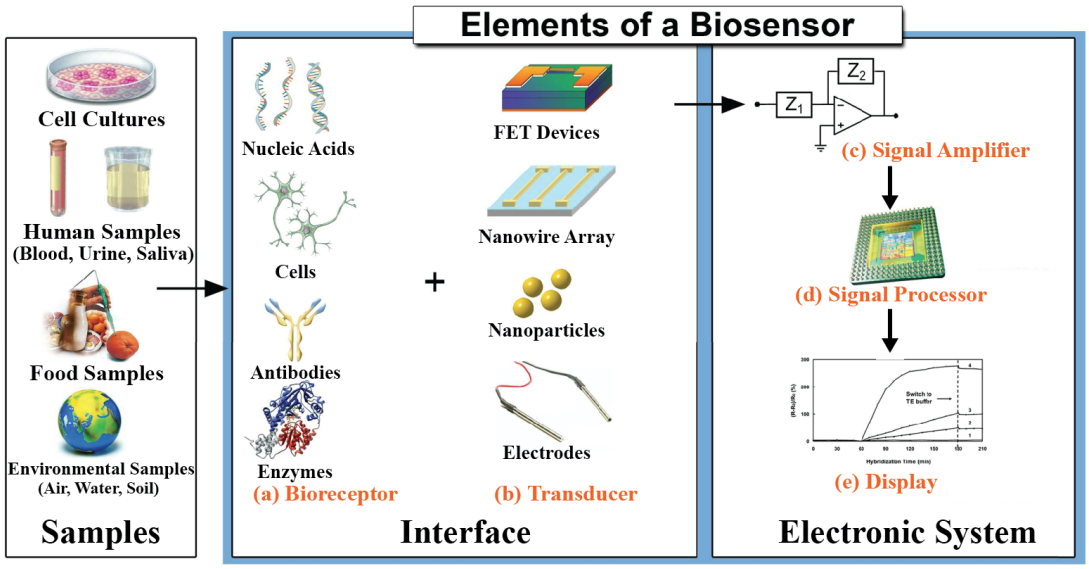


Figure 1.1: Elements of a typical biosensor [1].

1.2 Biosensors and Electronic Readout

A biosensor is an analytical device that converts a biological interaction (e.g., a binding event, DNA passing through an orifice, etc.) into a quantifiable and processable electric signal [2]. Figure 1.1 shows the various elements of a typical biosensor [1] where a transducer is coated with bioreceptor molecules that provide specificity to the analyte of interest. The sensor response is converted to an electric signal and amplified by an electronic front-end. A signal processor and a graphical user interface analyze and quantify binding events. Biosensors can be applied to a large variety of analytes including small molecules (e.g., antibodies, proteins, nucleic acids), food samples, and even environmental samples.

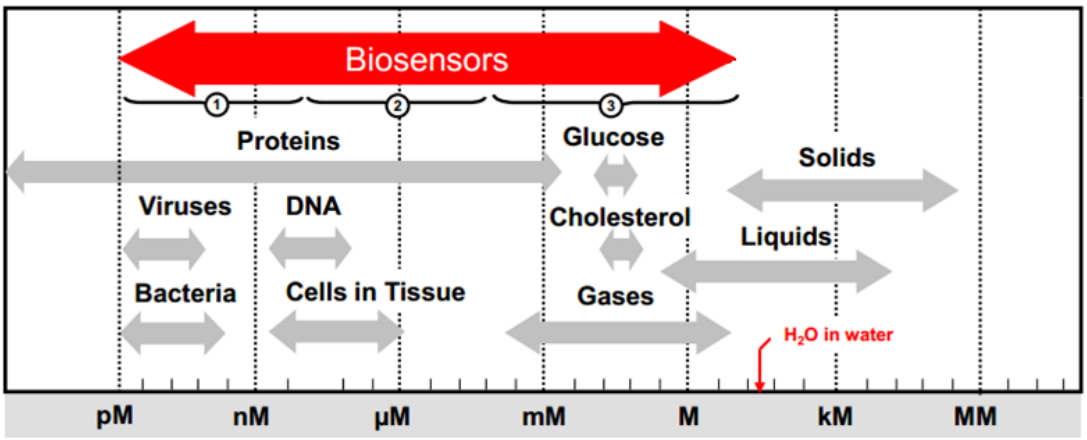


Figure 1.2: Sensitivity requirements for biological applications.

Compared to conventional instruments such as optical microscopy, electronic biosensors have the advantages of lower cost and smaller size. One of the biggest challenges today is dealing with the wide dynamic range of analytes present in biological samples. For example, some analytes exist in concentrations as low as a few fM (10^{-15} M) in the early stages of disease (e.g., cardiac troponins [3]) while other analytes (e.g., glucose [4-6]) are over 12 orders of magnitude higher. Several biosensors have demonstrated detection of analytes at concentrations less than pM (10^{-12} M) [7] as shown in Fig. 1.2, but none have enough dynamic range to cover the vast range of analytes. As such, researchers are working on designing biosensors and front-end circuitry with higher dynamic range while maintaining the high sensitivity. While it would not cover the entire dynamic range, the ability to detect pM concentrations to more than µM concentrations (>120 dB) would significantly advance the state-of-the-art and is the focus of this work.

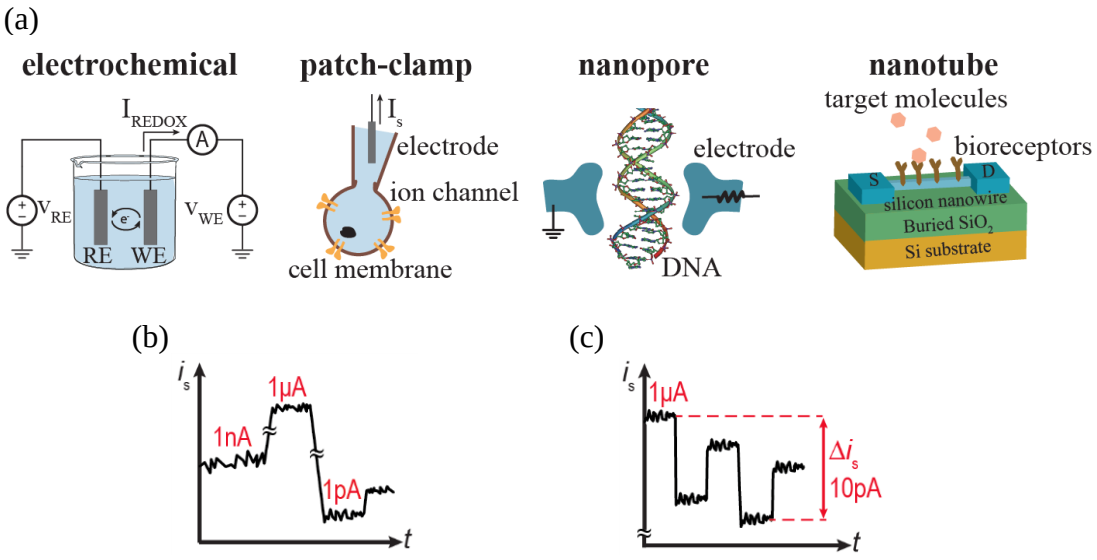


Figure 1.3: (a) Examples of current-input electrochemical biosensors where (b) and (c) show representative waveforms.

1.3 Current-based Biosensors

In current-based biosensors, a signal in the form of a change in charge is generated when biological events perturb the charge distribution of the electrode/electrolyte interface. Figure 1.3 shows some examples of current-based biosensors. In electrochemical cells, a charge transfer current, I_{redox}, occurs when the target molecule reduces (gains an electron) or oxidizes (loses an electron) on the surface of the working electrode (WE) with an applied analyte specific potential (V_{WE} - V_{RE}) between the working and reference electrodes (RE), respectively [8, 9]. Intracellular dynamics can be studied using a patch-clamp system [10] and DNA can be sequenced as it passes through a nanopore where it modulates the conductance across or through the pore [11, 12]. Finally, binding events on a nanoFET (e.g., a

nanotube or a nanowire) coated with bioreceptors are detected by the modulation in surface charge acting as the gate of the device [13].

The amplitude of the current in these sensors can vary by over 6 orders of magnitude. For example, the detection of neurotransmitters using an electrochemical biosensor requires more than 120 dB of dynamic range (DR), where the concentration of Dopamine can vary from 1 nM to >1 mM due to spontaneously spike activity or pharmacological stimulus [7]. The current in a patch-clamp setup covers several orders of magnitude depending on the number and the types of ion channels on the cell membrane. The high DR requirement has become even more critical with single molecule biosensors, e.g., nanopores and nanotubes, where the signal is a sub-pA current superimposed on a slowly varying nA to μA background current from the ion channel. These biosensing applications require a current readout front-end with a DR higher than 140 dB and an input-referred current noise less than 1 pA_{rms} [14, 15].

1.4 Challenges

Conventional current measurement front-ends have been extensively reported and analyzed in the literature [14, 15]. The dynamic range of these circuits is fundamentally determined by the circuit noise and supply voltage, which limits the minimum and maximum input currents, respectively. The decreasing supply voltage in advanced CMOS process nodes further limits the DR of conventional current-sensing front-ends [16, 17]. Furthermore, an output with a digital format is often desirable for further signal processing in the digital domain, so the front-end should

function both as a low-noise signal amplifier and an analog-to-digital converter (ADC). The design and optimization of such a front-end that achieves high linearity and reduces power consumption is a very attractive research topic, especially for high DR biosensing applications.

1.5 Scope of Dissertation

This dissertation presents the development of ultra-low noise current measurement front-ends for high dynamic range biosensing applications. In Chapter 2, performance and design trade-offs of conventional front-ends are discussed and analyzed. Chapter 3 presents a wide-band low-noise hybrid transimpedance amplifier for nanopore-based DNA sequencing. Chapter 4 presents a high dynamic range asynchronous Hourglass ADC with first-order noise shaping. Chapter 5 expands on this architecture showing a closed-loop Hourglass ADC achieving 160 dB dynamic range and 7 ppm linearity error. Lastly, concluding remarks and future research directions are presented in Chapter 6.

Chapter 2

Current Measurement Front-Ends for Biosensing Applications

In this chapter, current measurement front-ends for biosensing applications are introduced and the design and properties of different architectures is analyzed. Due to the various design trade-offs, comparisons of these architectures are discussed.

2.1 Background

Many biosensors provide a current signal during the detection of target molecules or proteins, and this current signal is captured by a signal amplifier for further signal processing. The most critical current signals in biosensing applications typically range from sub-pA to more than a few μA within a ~kHz bandwidth. Thus, the amplifier requires a dynamic range of greater than six orders, i.e., more than 120

dB, and very low input-referred noise (tens to hundreds of fA_{RMS} in the kHz bandwidth). In addition, the input impedance of the signal amplifier should be low compared to the sensor's output impedance to avoid attenuation.

To design an amplifier and analyze the effect of the noise, a current input biosensor can be modeled as a current source i_s with a shunt capacitance C_s and a shunt resistance R_s, as shown in Fig. 2.1., where the shunt capacitance is formed by the ionic double layer in an electrochemical cell, the gate oxide in a nanotube or an ion-sensitive field-effect transistor (ISFET), or the lipid bilayer membrane in a nanopore. The capacitance is on the order of a few pF when the sensor is tightly integrated with a CMOS readout circuit [14, 15] and can be more than nF for off-chip biosensors [9, 18]. Meanwhile, the shunt resistance is a charge transfer resistance of 1 - 100 MΩ in an electrochemical cell or the leakage in a nanotube/nanopore and often >1 GΩ. This simplified model with an output impedance Z_s provides a first-order circuit for the analysis of the amplifier's performance while more accurate models of each type of biosensor can be found in the literature, if needed [14].

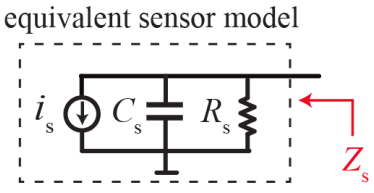


Figure 2.1: Simplified model for a current-based biosensor.

The amplifier can be categorized into either: 1) a current-to-current amplifier or 2) a current-to-voltage amplifier. The conventional implementations of these are a current conveyor (CC) and a transimpedance amplifier (TIA), respectively. The signals after amplification can be filtered and then quantized into a discrete-time digital signal by an ADC for further analysis. Although the amplifier and the ADC can be designed separately, a current-input ADC provides a lower noise, higher linearity, and lower power consumption when the ADC is designed to amplify and quantize the input signal at the same time. For example, a current-input $\Delta\Sigma$ modulator (DSM) uses global feedback to improve the linearity as well as reduce power consumption. An oscillator-based ADC is another example that provides signal amplification from current to time domain and quantizes this time information efficiently in a mostly digital way.

Most commercial instrumentations are based on different TIA architectures, such as the Axon Axopatch 200B [19, 20] and Stanford Research Systems SR570 [21]. However, being more general-purpose instrumentation, these are quite large and power-hungry devices. CMOS integrated circuit miniaturization shrink complex current-sensing architectures into silicon chips and offer a unique opportunity to co-integrate biosensors directly with the readout circuit. The integration of the sensor and amplifier provides a lower noise due to a reduction in interconnection capacitances. This enables biosensing and point-of-care applications and arranges high, density compact arrays for high throughput applications. The implementation and

performance details of a CC, TIA, and current-input ADC are discussed in the following section.

2.2 Current Conveyor

A current conveyor amplifies low currents while providing a clamping voltage bias for the biosensor. The CC is essentially a buffer decoupling the input and output impedances while providing amplification so the noise and performance requirement of the following stages are relaxed. Fig. 2.2 shows a schematic of a CC. The CC takes an input current from node *X* and provides an amplified output current at a high output impedance node *Z*. Node *Y* can be connected to a well-defined voltage to clamp the voltage at node *X* for the necessary bias voltage of the sensor.

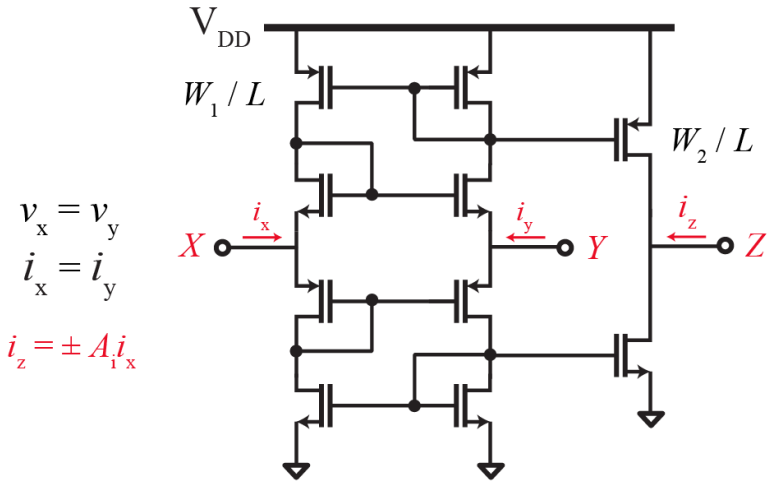


Figure 2.2: Schematic of a current conveyor.

The sensor current flowing into node *X* is copied to node *Z* with a high impedance output. The gain of the CC is determined by the ratio of the current mirror between branch *X* and *Z*, which can be simplified as $A_i = W_2/W_1$ when all the transistors have the same channel length, *L*. This current is also mirrored to node *Y*, so the voltage at the node *X* is a virtual short to an external voltage applied at node *Y* by the feedback loop.

The input-referred current noise of the CC can be calculated by adding the current noise from the all the transistors together directly when both the input and output are currents

$$S_{\mathrm{i,CC}} = 8\left(4kT\gamma g_{\mathrm{m1}} + \frac{K_{\mathrm{f}}}{C_{\mathrm{ox}}W_1Lf}\right) + \frac{2}{A_i}\left(4kT\gamma g_{\mathrm{m2}} + \frac{K_{\mathrm{f}}}{C_{\mathrm{ox}}W_2Lf}\right), \tag{2-1}$$

where *k* is Boltzmann's constant, *T* is the absolute temperature, C_{ox} is the gate oxide capacitance per unit area, γ and K_{f} are the process dependent thermal and flicker noise coefficients, respectively, *f* is the frequency, and g_{m} is the transconductance of each stage, which is determined by both the input signal and the bias current of the CC. The overall noise resulting from the sum of the sensor current plus the conveyor bias current. The current noise of a CC can be reduced by biasing the current mirror in deep saturation region, i.e., larger V_{gs}-V_{t} with a smaller $g_{\mathrm{m}}/I_{\mathrm{d}}$. When the input current increases, the $|V_{\mathrm{gs}}|$ of the current mirror increases and moves the operation of the cascode transistors into the triode region. This causes a feedback error and sets the maximum allowable input current of a CC. A CC usually achieves a noise power spectrum density higher than 1 pA/√Hz and a dynamic range of 60 dB [14, 22].

2.3 Transimpedance Amplifier

A TIA converts a current input to a voltage output. The basic TIA structure is implemented based on an amplifier with a feedback element Z_f, either a resistor, a capacitor, or a diode, which determines the gain of the TIA, as shown in Fig. 2.3. The virtual ground at the input of the amplifier provides: 1) a DC voltage V_b to bias a sensor in the wanted operation region and 2) a near-zero input impedance for current measurement.

The input-referred noise of a TIA can be analyzed when the two noises source are uncorrelated. The amplifier noise can be modeled as an input-referred voltage source e_n at the non-inverting input node of the amplifier, so the output-referred noise is $(1+Z_F/Z_s)e_n$ where Z_s is the output impedance of the sensor. Thus, the total input-referred current noise can be obtained from this quantity divided by the closed loop gain. V_b, e_n and Z_s are not drawn in the later figures for simplicity but included for analysis.

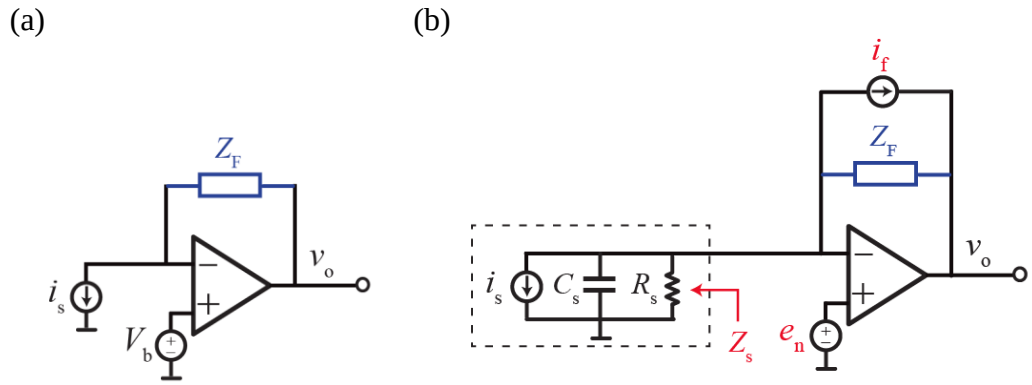


Figure 2.3: Schematic of (a) a transimpedance amplifier, and (b) equivalent circuit with noise sources.

2.3.1 Resistive Feedback TIA

Figure 2.4 shows a schematic of a resistive feedback TIA (R-TIA). The gain of the R-TIA is determined by the feedback resistor, R_f, where the output voltage $v_o = i_s \times R_F$. The noise from the feedback component is $i_f^2 = 4kT/R_f$, so the total input-referred current noise power density is

$$S_{i,\mathrm{R-TIA}} = \frac{4kT}{R_f} + \left(\frac{1}{(R_s//R_f)^2} + s^2 C_s^2\right) e_n^2. \qquad (2\text{-}2)$$

The feedback resistor generates noise in addition to the noise from the amplifier, so the noise from R_f should be minimized. For example, R_f should be larger than 165 MΩ to obtain a current noise density less than 10 fA/√Hz. An additional shunt capacitor C_{BW} can be used to reduce the total noise by controlling both the bandwidth of the R-TIA and the wideband white noise. This C_{BW} can also stabilize the amplifier when the parasitic capacitances from R_F and the inverting input node of the amplifier affects the stability of a R-TIA. Therefore, the minimum detectable signal of R-TIA can be determined and is usually limited by the extra noise from the feedback resistor in a well-designed low noise amplifier.

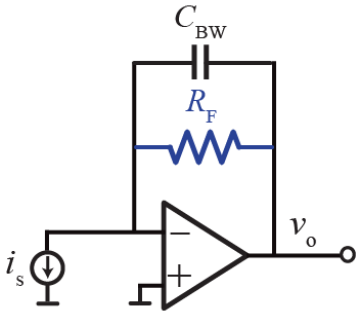


Figure 2.4: Schematic of an R-TIA.

2.3.2 Capacitive Feedback TIA

A capacitive feedback TIA (C-TIA) as shown in Fig. 2.5(a) is an amplifier with a capacitor, C_F, in feedback. The C-TIA provides a gain of $1/sC_F$, which decreases by 20 dB/decade. The total input-referred current noise density can be derived as

$$S_{i,\mathrm{C-TIA}} = \left(\frac{1}{R_s^2} + s^2(C_s + C_F)^2\right) e_n^2. \tag{2-3}$$

As such, a smaller C_F increases the gain and reduces the input-referred noise but must be reset more often for large currents. The noise in a C-TIA is less than that of an R-TIA because of the lack of noise from the feedback element.

Due to the infinite gain at DC, a periodic reset switch is required to prevent the saturation of C_F, so the DC gain equals to T_p/C_f, with an amplifying period of T_p. This periodic reset limits the maximum input current to be less than $i_{s,max} = C_f V_{DD}/T_p$ so the C-TIA does not saturate before the next reset phase, as shown in Fig. 2.5. To improve the DR of a C-TIA, a smaller T_p or larger C_f can be chosen, but this results in a trade-off with a decreased DC gain and increased noise.

(a) (b)

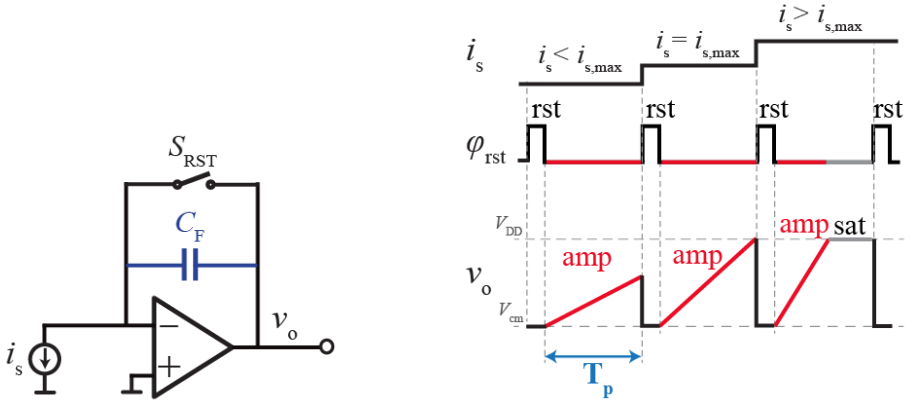


Figure 2.5: (a) Schematic and (b) waveform of a C-TIA.

2.3.3 Log TIA

A logarithmic TIA (Log-TIA) with a diode in feedback provides a wide input dynamic range by converting the input current in linear scale to an output voltage in log scale, as shown in Fig. 2.6 [23]. The gain of a Log-TIA is obtained by the current-voltage relationship of the feedback diode: $v_o = V_{th}\ln(i_s/I_S)$, where V_{th} is the thermal voltage (i.e., kT/q) and I_s is the reverse bias saturation current.

The total input-referred current noise density can be derived as

$$S_{i,\mathrm{Log-TIA}} = 2qi_s + \left(\frac{1}{(R_s||r_D)^2} + s^2C_s^2\right)e_n^2, \qquad (4)$$

where r_D is the small-signal resistance of the diode (i.e., V_{th}/i_s). Both the noise and feedback impedance from the diode are signal dependent, where the noise of a Log-TIA is dominated by the second term in (4) due to the squaring relationship between the noise power and input current i_s. Therefore, this noise only limits the maximum SNR rather than the DR.

The design challenges in a Log-TIA are the temperature stability and linearity. Due to the temperature dependence of the current-voltage relationship, a Log-TIA requires an additional compensation circuit which contributes extra noise [24]. Also,

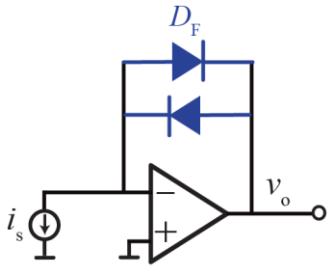


Figure 2.6: Schematic of a bidirectional Log-TIA.

the higher-order non-linearity of this current-voltage relationship introduces distortion in a Log-TIA of more than 1% (in linear scale) over a 100 dB DR, such as Analog Device ADL5304 [25] or Texas Instruments LOG112 [26].

2.3.4 Wideband TIA

In Fig. 2.7, a wide, flat-gain bandwidth and low noise TIA is obtained using an integrator-differentiator structure where the C-TIA serves as a low-noise amplifier and the pole of the C-TIA is cancelled by the zero in the differentiator [16, 17, 27, 28]. The gain is constant as R_dC_d/C_f up to over 1 MHz, which is limited by the bandwidth of the amplifiers or the parasitic capacitance from R_d. The DC servo loop discharges the slowly varying background signal, i.e., near DC components, so that the C-TIA only amplifies the AC signal of interest. Therefore, the transfer function of TIA is a bandpass filter with a low cutoff frequency, and the overall DR of is improved by 2 to 3 orders depending on the maximum available current from the DC servo loop.

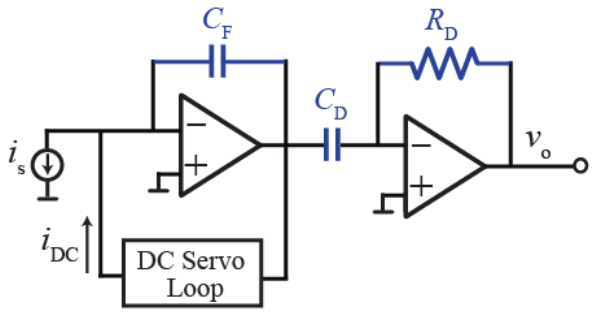


Figure 2.7: Schematic of a wideband TIA.

The total input-referred current noise density can be derived as

$$S_{i,\mathrm{WB-TIA}} = i_{\mathrm{FB}}^2 + \left(\frac{1}{R_{\mathrm{s}}^2} + s^2(C_{\mathrm{s}} + C_{\mathrm{F}})^2\right) e_{\mathrm{n1}}^2 + \left(\frac{C_{\mathrm{F}}}{C_{\mathrm{D}}}\right)^2 \left(\frac{1}{R_{\mathrm{D}}^2} + s^2 C_{\mathrm{D}}^2\right) e_{\mathrm{n2}}^2, \qquad (2\text{-}4)$$

where i_{FB} is the total current noise contributed by the DC servo loop, and e_{n1} and e_{n2} are the input-referred voltage noises from the first and the second amplifier, respectively.

2.4 Current-Input ADC

In this section, two types of current-input ADCs are discussed.

2.4.1 Delta-Sigma Modulator

Figure 2.8 shows a current-input ΔΣ modulator providing high resolution by oversampling and placing the C-TIA in a global feedback loop where the C-TIA provides the necessary high transimpedance gain and low input-referred noise. With a fixed feedback current, this DSM can quantize small input current by reducing the duty cycle, *D*, of the feedback current . This is because the equivalent feedback current is scaled down by the same ratio, e.g., 1-bit I-DAC equals to multi-bit I-DAC by tuning the duty cycle. By programming the duty cycle over 5 orders, this DSM can achieve 160 dB dynamic range with the oversampling technique while the DSM with a fixed *D* provides 60 dB dynamic range.

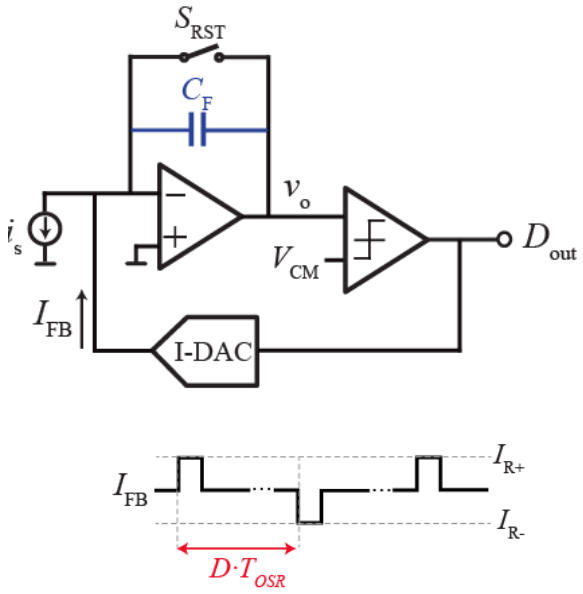


Figure 2.8: Schematic of a DSM.

2.4.2 Oscillator-based ADC

An input signal can also be used to control the frequency of an oscillator, where the signal is subsequently quantized in either the frequency or phase domain [29, 30]. An oscillator-based ADC is essentially an open-loop DSM, so the linearity is very sensitive to any circuit non-idealities. This can be overcome when such an ADC is implemented as a closed-loop current input DSM, as shown in Fig. 2.9, where a passive current-to-voltage integrator, i.e., a capacitor C_E, is used as the first stage and a voltage-controlled oscillator (VCO) is used as a first-order, noise-shaping quantizer. The input current is amplified and converted to a voltage when the charge integrates on C_E, and this voltage is quantized by the VCO-based ADC. The feedback loop with an I-DAC minimizes the voltage swing on C_E, so the non-linearity of the VCO-based ADC is suppressed. The passive integrator C_E can be implemented using an explicit

designed on-chip capacitor [29] or the intrinsic capacitance from the sensor [30]. The structure should be very carefully design when the capacitance is either voltage dependent or introducing larger input-referred current noise when C_E increasing the equivalent sensor impedance C_s in (2).

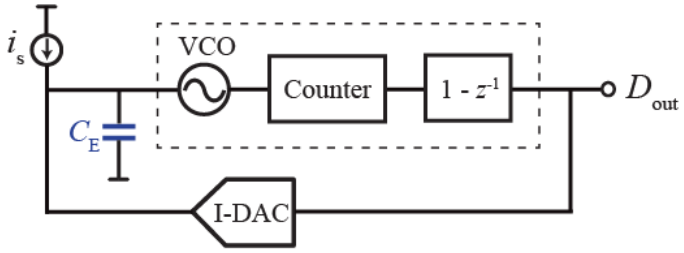


Figure 2.9: Schematic of a VCO-based ADC.

2.5 Summary and Comparison

The performance of each type of current amplifier and current-input ADC was analyzed, and Table 2.1 summarizes the design trade-offs of these front-ends. Because the requirements of low noise in biological applications, a C-TIA based architecture is preferable, such as a wideband TIA or a current-mode DSM. However, the DR and power efficiency of these architectures should be further improved to detect wide-range signals from biosensors.

Table 2.1: Comparison of conventional current-sensing front-ends.

	Bandwidth	**Gain**	**Noise**	**Dynamic Range**	**Operation**	**Quantizer**	**Linearity**
Current Conveyer	++	-	--	--	Continuous	No	-
R-TIA	--	+	--	-	Continuous	No	+
C-TIA	-	++	+	+	Discrete	No	+
Log-TIA	+	+	-	++	Continuous	No	-
Wideband TIA	++	++	+	-	Continuous	No	+
Current-Mode DSM	--	++	+	++	Discrete	YES	+
Signal-based ADC	+	++	+	+	Continuous	YES	+

Chapter 3

A Hybrid Semi-Digital Transimpedance Amplifier with Noise Cancellation Technique for Nanopore-Based DNA Sequencing

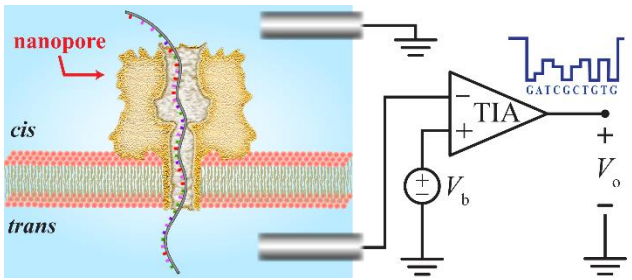
In this chapter, I present a hybrid semi-digital transimpedance amplifier (HSD-TIA) to sense the minute current signatures introduced by single-stranded DNA (ss-DNA) translocating through a nanopore, while discharging the baseline current using a semi-digital feedback loop. The amplifier achieves fast settling by adaptively tuning a DC compensation current when a step input is detected. A noise cancellation technique reduces the total input-referred current noise caused by the parasitic input capacitance. Measurement results show the performance of the amplifier with 31.6 MΩ mid-band gain, 950 kHz bandwidth, and 8.5 fA/√Hz input-referred current noise,

a 2× noise reduction due to the noise cancellation technique. The settling response is demonstrated by observing the insertion of a protein nanopore in a lipid bilayer, and ssDNA translocation events were measured by the HSD-TIA.

3.1 Introduction

Nanopore-based DNA sequencing has been under active development since 1995 [11, 12, 31-38]. It is a biophysical technique to sequence DNA based on the physical properties of the four types of nucleotides - guanine (G), adenine (A), thymine (T), and cytosine (C) - the building blocks of DNA. A nanopore is a small orifice, usually only a few nanometers in diameter, sandwiched between two fluidic chambers, the cis and trans, as shown in Fig. 3.1(a). When the nanopore is immersed in an ionic buffer with a bias voltage V_b applied between the two chambers, a baseline current $I_{baseline}$ is generated from the ions that drift through the nanopore. As DNA, being negatively charged, translocates through the pore, a current blockade occurs due to the different size and charge distribution of the nucleotides inside of the nanopore. One can, in theory, reconstruct the nucleotide sequence of single-stranded DNA (ssDNA) by observing the characteristic amplitude changes. Compared to conventional sequencing methods [31], nanopore-based methods are more efficient using only electrical and physical features of DNA without the need for complicated optical detection steps or custom nucleotides.

(a)



(b)

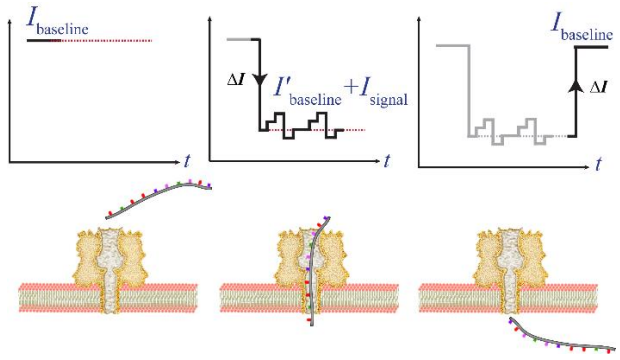


Figure 3.1: (a) Illustration of a nanopore-based DNA sequencing platform. (b) The baseline current shift that occurs when a ssDNA translocates.

Two main techniques are used to create nanopores: solid-state fabrication [11, 33, 34] and biological proteins (porin) [35-38]. Solid-state nanopores utilizes semiconductor manufacturing techniques, whereas a porin is a natural protein in the shape of a tube inserted in a lipid bilayer. Controlling the spatial and temporal resolution of nanopores is an active area of research where researchers are investigating methods to control the translocation speed and engineering thin, narrow pores to reduce the interrogation region [34]. Both types of pores require instrumentation to measure the small current differences between nucleotides, often less than 10 pA, in the presence of the baseline ionic current, which can be more than 1,000× larger [34]. Uncontrolled, the speed of ssDNA translocating through a

nanopore can be faster than one nucleotide per microsecond. Thus, the requirements of the current-sensing circuits for nanopores are quite demanding: high gain (>10 MΩ), high bandwidth (>10 kHz), low noise (<10 pA_{RMS}), and wide dynamic range.

Another more application specific challenge in nanopore-based DNA sequencing is the abrupt change in baseline current that occurs when a protein nanopore inserts or leaves a lipid bilayer [28]. Considering the protein nanopore lifetime, the time period when a pore is inserted into a lipid bilayer, can be as short as several seconds at room temperature [39], it is essential to minimize the settling time of the amplifier. This requirement for low settling time also applies when ssDNA enters or leaves the pore impeding the flow of ions, reducing the baseline current by 30-90% [34], as shown in Fig. 3.1(b). This change in $I_{baseline}$ is inversely proportional to the size of the pore. In our setup, using a protein nanopore with a diameter of 1.4 nm, the baseline current is reduced by 83-95% by the presence of ssDNA. Therefore, the step response of the current-sensing circuit must be minimized to prevent missing any current signatures during the settling of the circuit [28].

A TIA functions as a current-sensing circuit to convert the current input into a voltage output for further processing and analysis [14, 15]. Resistive and capacitive TIAs are widely used in many commercial instruments, such as the Axopatch 200B [20]. However, these topologies have notable drawbacks in this application. Namely, they either have large input-referred noise and low bandwidth, as is the case for a resistive feedback TIA [14, 15], or must be constantly reset since $I_{baseline}$ can saturate the amplifier in a capacitive feedback TIA [40, 41]. This large $I_{baseline}$ also increases

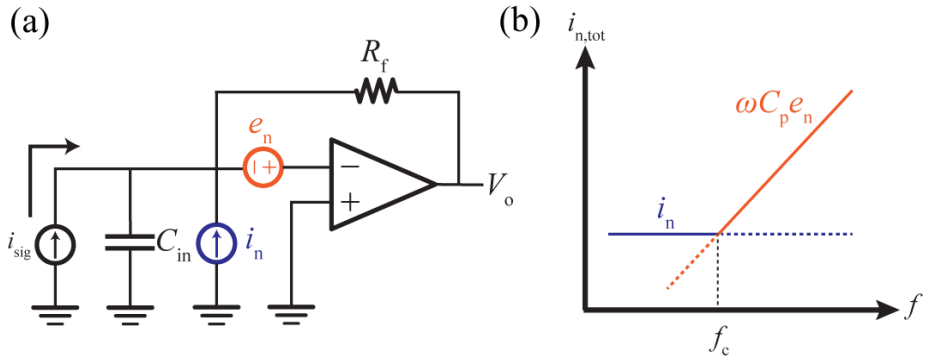


Figure 3.2: (a) Conventional resistive feedback TIA with voltage and current noise model. (b) The corresponding power spectrum density (PSD) of the input-referred current noise. The high frequency noise of the TIA is dominated by the input capacitor C_{in} and the voltage noise e_n.

the dynamic range requirement of the TIA [33]. A TIA with a DC feedback loop is one method to achieve low noise and high bandwidth [17, 27] without the need for a reset network; however, the limited bandwidth of the feedback loop requires long settling time for a step-input current, such as when a pore is inserted into the lipid bilayer [28].

As the bandwidth is increased, the sensitivity of a TIA is limited by the quadratic growth of total integrated input-referred current noise [14, 15]. The TIA in Fig. 3.2 has two noise sources: a current noise in and a voltage noise e_n from the OPAMP, neglecting noise from the feedback resistor. The input-referred current noise density is:

$$\overline{i_{n,tot}^2(\omega)} = \overline{i_n^2} + \overline{e_n^2}\omega^2 C_{in}^2, \tag{3-1}$$

where C_{in} is the total capacitance at the input node of the TIA. At low frequencies, the input-referred current noise density is approximately equal to the current noise in and the noise from e_n can typically be ignored. However, the second term in (1) produced

by the e_n and C_{in} dominates when the bandwidth increases beyond the noise corner frequency f_c, which is often only several kilohertz because C_{in} is predominantly caused by the capacitance of the nanopore [33]. Depending on how the pore is realized, it may not be possible to reduce this capacitance. Hence, the input-referred current noise must be reduced by either using circuit techniques or actively cooling the system [14] when the bandwidth is greater than 10 kHz.

In this paper, we describe a hybrid semi-digital TIA (HSD-TIA) with high flat-gain bandwidth and very low noise. The HSD-TIA continuously measures the input current without a reset switch by discharging the baseline current through a semi-digital feedback loop. In addition to servoing out the DC and low frequency baseline currents, this loop also adaptively provides a DC compensation current for fast step response. A noise cancellation technique is shown to reduce the input-referred current by partially cancelling the second term of (3-1).

The architecture of the proposed HSD-TIA with noise cancellation technique is introduced in Section 3.2. In Section 3.3, the semi-digital feedback loop with fast step response is explained. The noise cancellation technique and noise performance of the TIA are analyzed in Section 3.4. Section 3.5 focuses on the implementation of the proposed TIA, and the measurement results are presented in Section 3.6. Using the designed TIA, the biological measurements are shown in Section 3.7. Finally, conclusions are in Section 3.8.

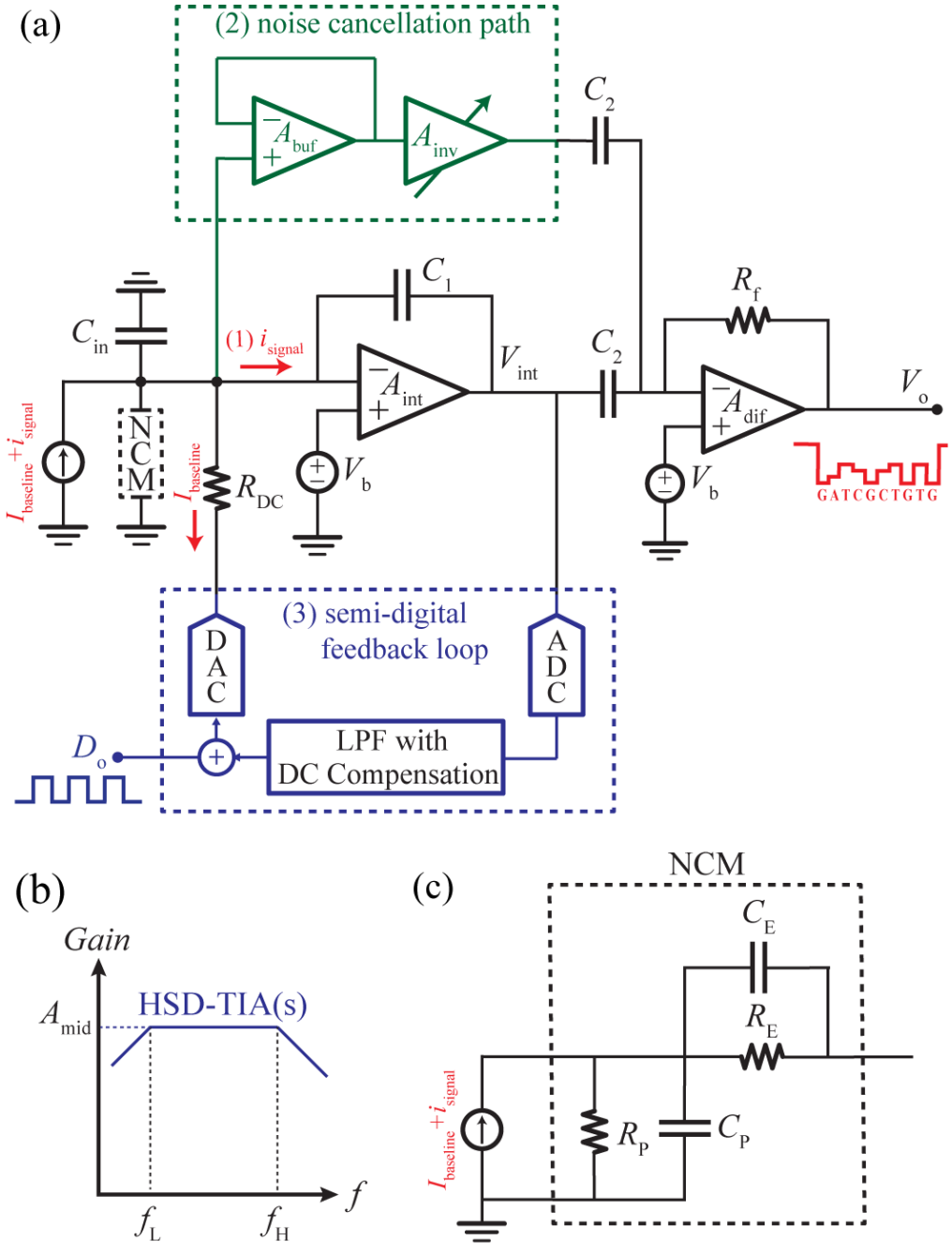


Figure 3.3: (a) Architecture of the HSD-TIA with noise cancellation technique. (b) The frequency response of HSD-TIA with low cutoff frequency f_L introduced by the semi-digital feedback loop and high cutoff frequency f_H. (c) Equivalent nanopore circuit model. R_p and C_P are the nanopore resistance and capacitance, and R_E and C_E are from the Ag/AgCl electrodes.

3.2 The Architecture of the HSD-TIA

We describe a HSD-TIA with a noise cancellation technique to obtain low noise, fast settling time, and continuous operation for nanopore-based DNA sequencing as shown in Fig. 3.3. The HSD-TIA contains three paths: (1) the signal path to amplify the input current at mid-band, (2) the feedback path to discharge the low-frequency components, including the baseline current and flicker noise (1/*f*), and (3) the feed-forward noise cancellation path to remove the voltage noise from the integrator. The signal path of the TIA consists of a capacitive feedback integrator that is cascaded with a differentiator to obtain high flat-gain bandwidth. The high cutoff bandwidth, f_H, is obtained by cancelling a DC pole from the integrator with a DC zero from the differentiator. The mid-band gain is:

$$A_{\text{mid}} = R_f \times C_2/C_1 \tag{3-2}$$

where C_1 is the feedback capacitor in the integrator, and C_2 and R_f form the differentiator. The transfer function of the HSD-TIA is shown in Fig. 3.3(b).

The semi-digital feedback path is wrapped around the integrator to discharge the low frequency components, particularly the baseline current and 1/*f* noise. The feedback loop introduces poles and zeros to shape the low-frequency response [17, 27]. The lower cutoff frequency f_L needs to be as low as a few tens of Hz to prevent loss of signal for nanopores with low DNA translocation speed, such as engineered MspA [36, 37] and motor controlled pores [38]. The frequency of these poles and zeros must be carefully designed to avoid attenuating the signal at mid-band and to maintain stability of the amplifier. Here, the poles and zeros are implemented by a

digital low-pass filter (LPF) in the feedback path. Compared to the variation of an analog implementation using discrete components with large resistances and capacitances [17, 27], the frequency of the poles and zeros can be precisely controlled in the digital domain.

Another advantage of this approach is the direct accessibility of the digitized low-frequency component, which is filtered out in an analog implementation that contains relevant biological information, such as the size of the nanopore and the number of nanopores inserted in a lipid bilayer. Compared to an analog feedback loop, an additional ADC, DAC, and FPGA are needed to implement the filter. However, the feedback signal may be digitized anyway, so we are merely pushing the ADC inside the feedback loop. The low-frequency nature of this loop does not necessitate high performance data converters.

The settling behavior of the HSD-TIA is determined by the bandwidth of the feedback loop, i.e., the low cutoff frequency, f_L. When a step-input current occurs, the baseline current accumulates on the integrator capacitor during the settling of the feedback loop. This step-input current can be as large as 95% of $I_{baseline}$ [34], which can easily saturate the output of the integrator since the feedback loop discharges the accumulated current slower than the integrator saturation rate, resulting in loss of the input signal during settling. We utilize an adaptive DC compensation current in the feedback loop to improve the settling behavior. A digital logic circuit in the FPGA detects the occurrence and magnitude of the input step by tracking the integrator output and checking if it exceeds a predefined window. The feedback loop then

adaptively produces a DC compensation current by adding a digital code D_o with the opposite sign of the step to the output of the filter. This compensation current reduces the difference between the feedback current and baseline current without having to wait for the LPF to settle and prevents saturation of the integrator resulting in a significant reduction of the settling time.

The noise of a high bandwidth TIA is dominated by C_{in} and $\bar{e}_n^2$ at high frequencies (3-2) where C_{in} is the capacitance of nanopore including the fluidic interface [33, 42], the input capacitance of the OPAMP, and cable parasitic capacitances. C_{in} is often 10 pF, even when co-integrating the nanopore and TIA [33]. Thus, there is a fundamental limit to how much C_{in} can be reduced necessitating alternative methods to reduce the noise. Here, we propose a noise cancellation technique to reduce the input-referred current noise by sensing and subtracting the voltage noise e_n. This feed-forward noise cancellation path contains a voltage-sensing amplifier and an inverting amplifier with matched gain, such that the noise from the signal and noise cancellation paths add destructively when the output of the two stages are combined. As shown in Fig. 3.3, the condition to cancel this voltage noise is:

$$e_n \times (C_i + C_p)/C_i = e_n \times |A_{inv}| \tag{3-3}$$

Thus, the voltage noise e_n from the integrator is cancelled by summing the inversely duplicated version of the same voltage noise from the noise cancellation path. Note that no input signal is amplified by the noise cancellation path [43, 44] because the input voltage of the HSD-TIA is clamped by the virtual ground. The equivalent nanopore circuit model (NCM) [14, 15, 45], shown in Fig. 3.3(c), is considered when

analyzing the stability and noise performance of the TIA.

In summary, the semi-digital feedback loop performs several functions: 1) it discharges the baseline current preventing saturation of the integrator and allowing continuous operation without the need for the reset network that is common in a capacitive TIA [40, 41], 2) it provides precise control of the low-frequency response and 3) it improves the settling response through an adaptive current. The TIA noise performance is improved by feed-forward cancellation of the integrator voltage noise and the removal of the $1/f$ noise in the feedback loop. Collectively, these relax the requirements of the integrator, particularly the voltage noise and input capacitance.

3.3 Semi-Digital Feedback Loop

The semi-digital feedback loop consists of two main components: a low pass filter and a DC compensation block, as shown in Fig. 3.4(a). The circuits are implemented digitally to guarantee the stability of the feedback loop without attenuating the desired signal. The frequency response of the feedback path, shown in Fig. 3.4(b) and (c), can be controlled efficiently, precisely, and adaptively in the digital domain.

3.3.1 Digital Filter

The semi-digital feedback path is composed of an ADC, a LPF, and a DAC. The LPF removes the high frequency signals from the output of the integrator and feeds the resulting signal back to the input of HSD-TIA. Thus, the baseline current is

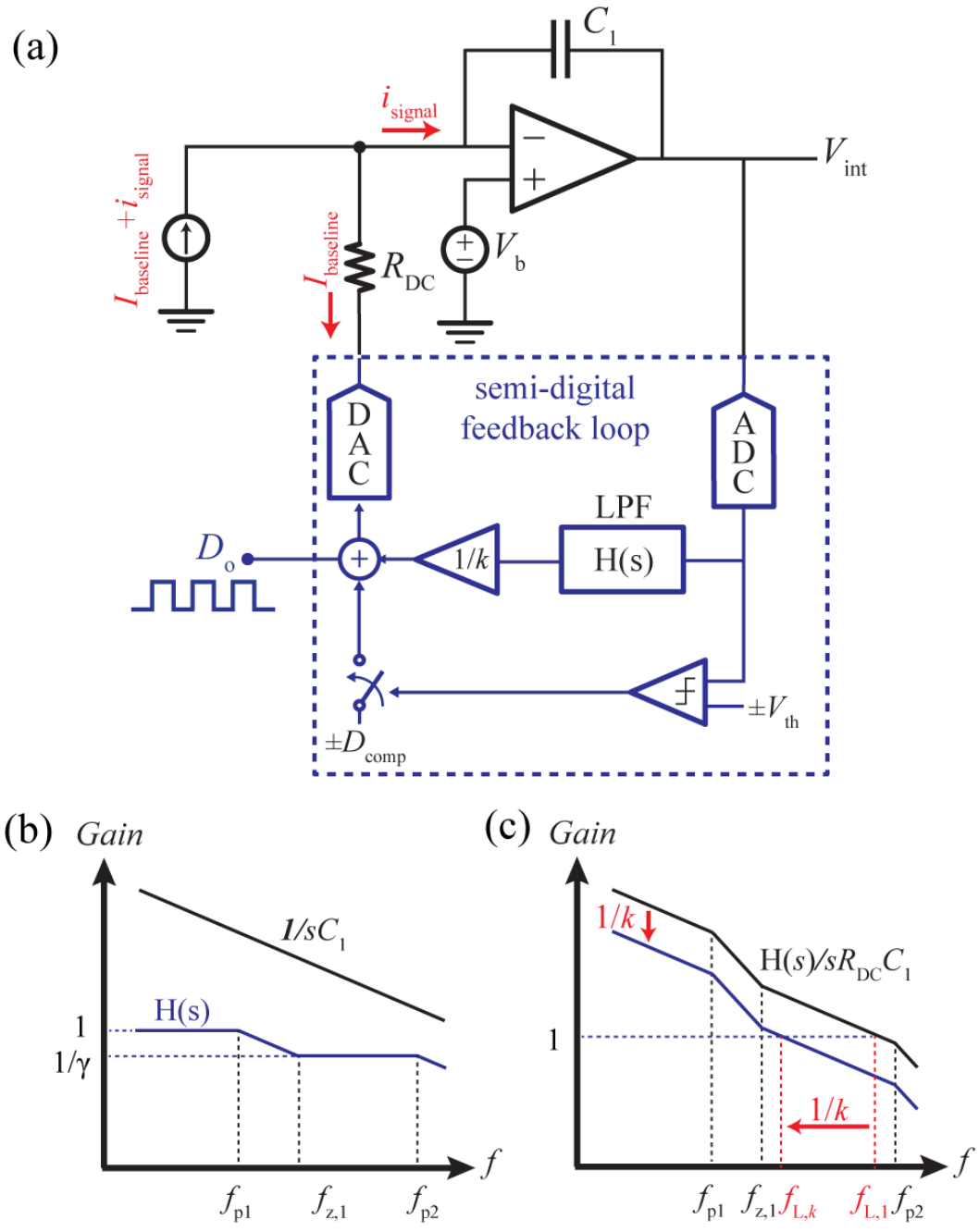


Figure 3.4: (a) Concept of the semi-digital feedback loop. (b) Frequency response of integrator and LPF. (c) Frequency response of the loop gain with the tuning factor $1/k$. The tuning factor $1/k$ is implemented to tune the low cutoff frequency f_L and the stability of the feedback loop.

discharged through a resistor RDC by the feedback loop. The ideal loop gain of this feedback path (Fig. 3.4) can be derived as,

$$G(s) = -\frac{H(s)}{sR_{\mathrm{DC}}C_1}, \tag{3-4}$$

where H(s) is the transfer function of the digital LPF. Without loss of generality, H(s) is assumed to have a pole f_{p1}, one or more high frequency poles f_{p2}, a zero f_{z1}, passband gain of unity, and an attenuation ratio of γ in the stopband. The low cutoff frequency f_L of the HSD-TIA can be derived from unity gain frequency of this loop, i.e., $|G(2\pi f_L)|=1$:

$$f_L = \frac{1}{2\pi\gamma R_{\mathrm{DC}}C_1}. \tag{3-5}$$

Considering the stability of a feedback loop, the additional poles introduced by the digital filter reduce the closed loop phase margin [17, 27]. A positive tuning factor *k* added in the digital domain to control the frequency response of the feedback loop and set the low cutoff frequency f_L. Changing the value of *k* shifts the magnitude response and the unity gain frequency f_L while keeping the phase response unchanged, thus allowing one to tune the frequency of f_L dynamically while guaranteeing the phase margin of the feedback loop. We define $f_{L,k}$ as the unity gain frequency with a tuning factor of 1/*k*. When 1/*k* is less than 1, the magnitude response shifts down, and f_{Lk} decreases by *k* with respect to $f_{L,1}$; that is:

$$f_{\mathrm{L},k} = \frac{1}{2\pi\gamma kR_{\mathrm{DC}}C_1}. \tag{3-6}$$

By carefully choosing *k* and the -3dB frequency of the LPF, it is possible to maintain a phase margin of the low-frequency feedback loop greater than 45º. Hence, the

stability of the feedback loop is obtained by tuning k even with variation of R_{DC} and C_1. A DC gain larger than unity in $H(s)$ could also be implemented to improve the stability; however, a higher order filter is required resulting in longer settling time.

The LPF is implemented in the digital domain with a sampling frequency of f_s. With a fixed f_s and f_L, one can save power and area in the LPF using a lower order LPF with a large f_{p1} and small $1/k$. However, the static gain error at the output of the integrator depends on the feedback factor at low frequency. That is:

$$\Delta V_{int} = \Delta I_{baseline} R_{DC}/k, \tag{3-7}$$

where ΔV_{int} is the static gain error. The static gain error shifts the output common-mode voltage and limits the output swing of the integrator, so the value of k must be chosen carefully. For example, an input-step current of 100 pA with R_{DC} of 1 GΩ and $1/k$ of 0.1 causes a static gain error of 1 V. This large static gain error can saturate the integrator especially with a low power supply voltage. The DC compensation current described later mitigates this problem and allows one to reduce the area and power of this digital LPF by using a lower order filter.

3.3.2 DC Compensation Current

A DC compensation current is added to reduce the settling time and prevent the integrator from saturating when a step-input current occurs. In order to implement this, a digital comparator monitors the digitized integrator output. Once the integrator output exceeds a predefined voltage range, a DC compensation code D_{comp} is added to the output of the LPF. The output voltage of the integrator with the DC compensation current can be written as:

$$D_{\mathrm{o,norm}}(t) = D_{\mathrm{comp,norm}} + (1 - D_{\mathrm{comp,norm}})(1 - e^{-t/\tau}), \tag{3-8}$$

where $D_{\mathrm{o,norm}}$ and $D_{\mathrm{comp,norm}}$ are the digital codes of the feedback loop and DC compensation normalized to the amplitude of the step-input current, τ is the closed-loop time constant, and $V(D)$ is the corresponding analog voltage of the digital code D. The feedback loop estimates the size of the step-input current by measuring the static gain error of the feedback loop from (3-7), and a digital code D_{comp} is calibrated based on this static gain error. The gain error is readily obtained in the digital domain because this gain error shows up at the output of the integrator and is digitized by the ADC. The algorithm is as follows: initially, D_{comp} is set to zero; once a step current is detected, the current of this step-input is measured. Then, a new digital code D_{comp} is updated and used for all later measurements since the size of the step-input current is roughly constant throughout the experiment. Using this technique, the settling time is reduced from 5τ to 2τ, a 60% reduction in settling time with a settling error of 0.7% when D_{comp} is 95% of the step.

The other benefit of the DC compensation current is the reduction in the static gain error due to the tuning factor in (3-7). When the D_{comp} is used, most of the discharging current is provided by D_{comp} rather than the feedback loop. The loop gain error can be reduced to:

$$\Delta V_{\mathrm{int}} = \left|\Delta I_{\mathrm{baseline}} R_{\mathrm{DC}} - V(D_{\mathrm{comp}})\right|, \tag{3-9}$$

Hence, the DC compensation current can both decrease the static gain error of the integrator and reduce the settling.

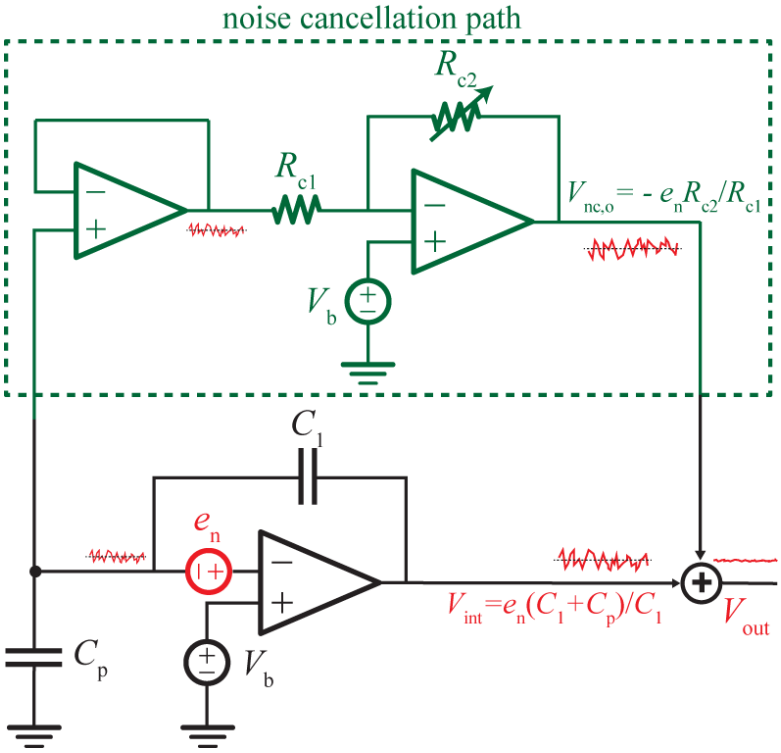


Figure 3.5: Schematic of feedforward noise cancellation circuit. The integrator voltage noise is sensed and amplified by the noise cancellation path.

3.4 Noise Cancellation Technique and Noise Analysis

3.4.1 Noise Cancellation Technique

The proposed noise cancellation technique requires a low-noise voltage buffer to sense the voltage noise from integrator, and an amplifier to provide the matched gain between the noise cancellation path and the integrator [43, 44], as shown in Fig. 3.5. Due to the virtual ground at the input of the integrator, the voltage noise of the integrator can be sensed by a unity gain buffer. This sensed voltage noise is then amplified by a tunable inverting amplifier. From (3-3), the value of R_{c1} and R_{c2} are tuned to obtain the optimized noise cancellation effect with respect to the input

capacitance from nanopore and cable connections.

3.4.2 Noise Analysis

To analyze the total-referred input current noise density of the HSD-TIA in the signal band, we first neglect the noise cancellation path. The equivalent input noise is given by

$$\overline{\iota_{\mathrm{n,tot}}^2}(\omega) = \overline{\iota_{\mathrm{n1}}^2}+\overline{e_{\mathrm{n1}}^2}\omega^2\left(C_1 + C_{\mathrm{p}}\right)^2 + \frac{\overline{e_{\mathrm{n1}}^2}}{R_{\mathrm{DC}}^2} + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e_{\mathrm{Q}}^2}}{k^2\gamma^2 R_{\mathrm{DC}}^2} \tag{3-10}$$

$$+\left(\frac{C_1}{C_2}\right)^2\left(\overline{\iota_{\mathrm{n1}}^2} + \overline{e_{\mathrm{n1}}^2}\omega^2 C_2^2 + + \frac{\overline{e_{\mathrm{n2}}^2}}{R_{\mathrm{f}}^2} + \frac{4kT}{R_{\mathrm{f}}}\right),$$

where $\overline{\iota_{\mathrm{n1}}^2}$, $\overline{e_{\mathrm{n1}}^2}$, $\overline{\iota_{\mathrm{n2}}^2}$, and $\overline{e_{\mathrm{n2}}^2}$ are the current and voltage noises of the OPAMPs in the integrator and differentiator, respectively; C_{in} is the total capacitance at the input of the HSD-TIA, including the input node of integrator, the connection between the TIA, and the capacitance of the lipid bilayer; and $\overline{e_{\mathrm{Q}}^2}$ is the noise from the digital circuits, including the quantization error of the ADC and digital LPF. For simplicity, the integrated digital noise $\overline{e_{\mathrm{Q,rms}}^2}$ is taken to be only the ADC quantization noise, $V_{\mathrm{LSB}}^2/12$ over the bandwidth of the feedback loop which is attenuated by the tuning factor k. The ratio of C_2/C_1, which forms part of the gain of the TIA, is much greater than unity by design, so the input-referred noise of the TIA is approximately

$$\overline{\iota_{\mathrm{n,tot}}^2}(\omega) \cong \overline{\iota_{\mathrm{n1}}^2} + \overline{e_{\mathrm{n1}}^2}\omega^2(C_1 + C_{\mathrm{in}})^2 + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e_{\mathrm{Q}}^2}}{k^2\gamma^2 R_{\mathrm{DC}}^2} + \left(\frac{C_1}{C_2}\right)^2\frac{4kT}{R_{\mathrm{f}}}. \tag{3-11}$$

Note that the input-referred current noise of the TIA, like the resistive feedback TIA, is dominated by the second term in (11) at frequencies higher than f_{c}.

Next, we analyze the input-referred current noise with the noise cancellation

technique using similar steps

$$\overline{\iota_{\mathrm{n,tot}}^2}(\omega) \cong \left(\overline{\iota_{\mathrm{n1}}^2} + \overline{\iota_{\mathrm{nc1}}^2}\right) + \alpha^2\overline{e_{\mathrm{n1}}^2}\omega^2(C_1 + C_{\mathrm{in}}')^2 \tag{3-12}$$

$$+\left(\overline{\iota_{\mathrm{nc2}}^2} \cdot R_{\mathrm{c1}}^2 || R_{\mathrm{c2}}^2 + 4kTR_{\mathrm{c1}}\frac{R_{\mathrm{c2}}^2}{R_{\mathrm{c1}}^2} + 4kTR_{\mathrm{c2}}\right)\omega^2 C_1^2$$

$$+\overline{e_{\mathrm{nc1}}^2}\omega^2(C_1 + C_{\mathrm{in}}')^2 + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e_{\mathrm{Q}}^2}}{k^2\gamma^2 R_{\mathrm{DC}}^2} + \left(\frac{C_1}{C_2}\right)^2\frac{4kT}{R_{\mathrm{f}}},$$

where $\overline{\iota_{\mathrm{nc1}}^2}$, $\overline{e_{\mathrm{nc1}}^2}$, $\overline{\iota_{\mathrm{nc2}}^2}$, and $\overline{e_{\mathrm{nc2}}^2}$ are the current and voltage noises of the OPAMPs in the voltage buffer and the inverting amplifier and C_{in}' is the total input capacitance at the input of the HSD-TIA after adding the noise cancellation path. We define a α as the residual noise factor after noise cancellation where

$$\alpha = \left|1 - \frac{R_{\mathrm{c2}}/R_{\mathrm{c1}}}{(C_{\mathrm{i}}+C_{\mathrm{in}}')/C_{\mathrm{i}}}\right|. \tag{3-13}$$

The noise at frequencies higher than fc is reduced significantly, by a factor of α, with the trade-off of slightly increased noise at low frequencies due to the additional term $\overline{\iota_{\mathrm{nc1}}^2}$. The noise from the inverting amplifier can be neglected because R_{c1}, R_{c2}, and $\overline{e_{\mathrm{nc2}}^2}$ can be designed with smaller values compared to $\overline{e_{\mathrm{n1}}^2}$, since no signal is processed in the noise cancellation path. Thus, the TIA input-referred current noise can be approximated as

$$\overline{\iota_{\mathrm{n,tot}}^2}(\omega) \cong \left(\overline{\iota_{\mathrm{n1}}^2} + \overline{\iota_{\mathrm{nc1}}^2}\right) + \alpha^2\overline{e_{\mathrm{n1}}^2}\omega^2(C_1 + C_{\mathrm{in}}')^2 \tag{3-14}$$

$$+\overline{e_{\mathrm{nc1}}^2}\omega^2(C_1 + C_{\mathrm{in}}')^2 + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e_{\mathrm{Q}}^2}}{k^2\gamma^2 R_{\mathrm{DC}}^2} + \left(\frac{C_1}{C_2}\right)^2\frac{4kT}{R_{\mathrm{f}}},$$

From (3-14), the performance of the noise cancellation is limited: by (1) the residual noise factor α and (2) the voltage noise $\overline{e_{\mathrm{nc1}}^2}$ from the buffer. The residual noise factor is optimized by tuning the gain of the inverting amplifier to match the

signal path. The unity gain buffer can be designed/chosen with lower voltage noise $\overline{e_{\mathrm{nc1}}^2}$ than $\overline{e_{\mathrm{n1}}^2}$ because the requirement of this buffer is relaxed with a feedback factor of unity, which is much larger than the integrator. Hence, the total integrated noise of the HSD-TIA with the noise cancellation in (3-14) is reduced compared to (3-11).

3.5 Implementation

We verified the proposed HSD-TIA with noise cancellation technique using discrete components on a PCB (Fig. 3.6). This design has a mid-band gain of 31.6 MΩ and a flat-gain bandwidth of 950 kHz. The component values for the design are listed in Table 3.1. A 6th order Bessel LPF with a gain of 10 dB is cascaded with the HSD-TIA as an anti-aliasing filter. The gain of the HSD-TIA was designed based on (3-2). The differentiator is implemented as a band-pass filter to set the high cutoff frequency f_{H} and improve the stability of the TIA. f_{H} is readily changed for different types of nanopores by simply tuning the feedback capacitor in the band-pass filter without increasing the input-referred noise or decreasing the gain. Currently, f_{H} is limited by the parasitic capacitance on the PCB in the feedback path of the differentiator rather than the OPAMPs when the bandwidth is increased.

To obtain low noise and low leakage current, the considerations of the integrator OPAMP were a voltage noise less than 10 nV/√Hz , a current noise less than 10 fA/√Hz, and an input capacitance of only a few pF. A MOS-input OPAMP with low input bias current is used for the integrator. The total input bias current of the HSD-TIA is designed to be less than 10 pA to minimize signal leakage. The requirements of low voltage noise and low input capacitance are relaxed because of

the noise cancellation path from (3-14). The noise requirement of the differentiator OPAMP is reduced because of the gain from the integrator.

The semi-digital feedback loop was realized with a 12-bit ADC, FPGA, 12-bit DAC, and a resistor RDC. The FPGA implemented the LPF, DC compensation logic, and all control logic. The LPF was designed based on the values of f_L and k in (3-6), (3-8) and (3-9). The LPF is implemented as an equal-ripple finite impulse response (FIR) filter with a -3dB frequency of 100 Hz and a gain factor $1/k$ of 0.1 which results in an f_L of 26 Hz. The -3dB frequency could be lower with a larger value of k, but the area/power overhead is increased due to a higher order FIR LPF. R_{DC} was chosen according to the discharging current capability and the current noise $4kT/R_{DC}$. Furthermore, R_{DC} should be on the same order of magnitude as the resistance of nanopore channel, so the baseline current caused by the bias voltage V_b can be discharged by R_{DC}. Here, an R_{DC} of 1 GΩ provides a maximum baseline discharging capability of 2 nA with $V_{o,peak}$ of 2 V and low input-referred noise based on (3-14).

The noise requirements of the noise cancellation path are higher than the signal path to reduce the total noise of TIA. The OPAMP in the unity-gain buffer has the same requirements as the integrator, except lower input capacitance and lower voltage noise. However, the feedback factor of this OPAMP is unity, which is much larger than the feedback factor of the integrator, so the open-loop bandwidth requirement of the buffer is reduced. We chose an OPAMP with a voltage noise $\overline{e_{nc1}^2}$ lower than $\overline{e_{n1}^2}$. Next, the voltage noise requirement of inverting amplifier should also be lower than the integrator to minimize the noise overhead. We used a BJT-input OPAMP with

lower voltage noise because the input bias current is provided by the buffer. The voltage noise from the resistors in the inverting amplifier are also optimized, thus minimizing the noise contribution from the noise cancellation path. The differentiator in the signal path is used to subtract the amplified signal V_{int} from the sensed noise $V_{nc,o}$, as shown in Fig. 3.5. We use OPAMPs with closed-loop bandwidth higher than 1 MHz in the noise cancellation path to prevent phase mismatch between signal path and noise cancellation path at high frequency. The offset voltage from OPAMPs in the noise cancellation is removed by the differentiator. Due to limited selection of commercially available OPAMPS, it may be possible to find a single OPAMP that outperforms the proposed solution in the noise cancellation path. However, a CMOS implementation allows the designer greater flexibility in the amplifier design and benefits from the decoupling of the requirements gained with the noise cancellation path.

A 5 V LDO is used to provide a stable power supply voltage, and a low-noise reference voltage generator for the common-mode and bias voltage V_b are also implemented on the PCB. All the components for the designed HSD-TIA are listed in Table 3.1, and the photo of the implemented PCB is shown in Fig. 3.6.

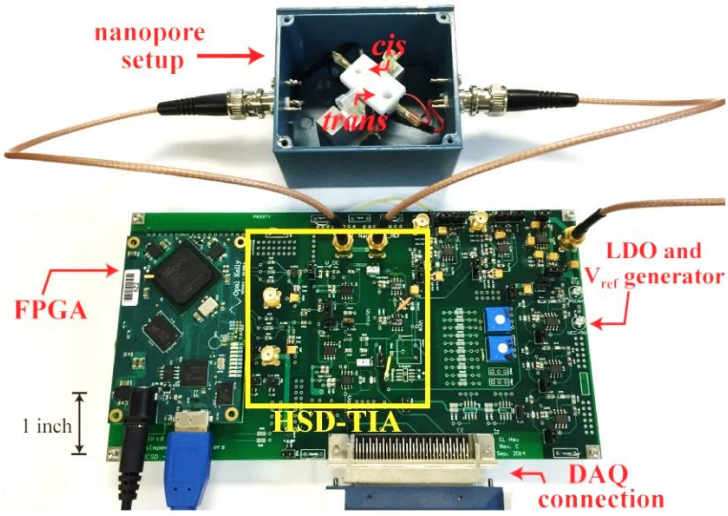


Figure 3.6: Photograph of nanopore and TIA.

Table 3.1: List of Discrete Components and Values.

Active Device	Part Name		Passive Component	Part Name
OPAMP	A_{int}	AD8033	R_{DC}	1 GΩ
	A_{dif}	AD8065	R_f	200 kΩ
	A_{buf}	LTC6240	C_1	2.2 pF
	A_{inv}	LTC6200	C_2	110 pF
ADC	AD7276		FPGA	Opal Kelly XEM6300
DAC	AD5320			

3.6 Circuit Performance

We characterized the performance of the designed HSD-TIA with the NCM at the input. The TIA operates with a single supply voltage of 5 V and a common-mode voltage of 2 V. All measurements were analyzed using a National Instruments data acquisition system (DAQ) with 16-bit resolution.

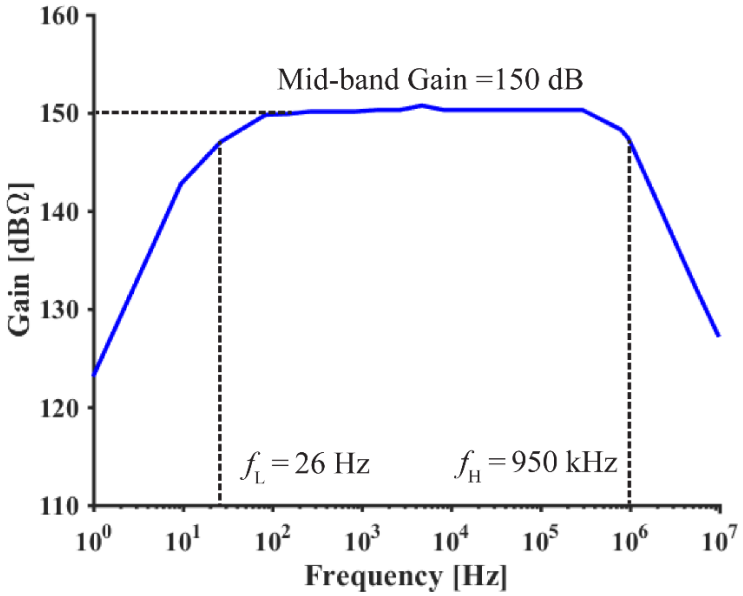


Figure 3.7: Frequency response of reported HSD-TIA.

3.6.1 Frequency Response

The frequency response was measured by sweeping the frequency of a sinusoidal input current connected to the NCM. The measurement results in Fig. 3.7 show the frequency response of the design. The measured flat-band gain is 31.6 MΩ over a 26 Hz – 950 kHz bandwidth. The measurement results correspond well with the theoretical analysis.

3.6.2 Noise Performance

The measured noise power spectral density is shown in Fig. 3.8 with zero input current applied. First, we measured the input-referred current noise without the noise cancellation path; i.e., disconnecting both the input of the unity gain buffer and the output of the inverting amplifier from the integrator. The TIA had a measured spot noise of 8.5 fA/√Hz at 1 kHz. The corner frequency f_c was 1.5 kHz, and the noise increases at higher frequencies due to the parasitic capacitor C_p and the voltage noise of the integrator. The total integrated input-referred current noise was 6.9 pA_{rms} for a bandwidth of 10 kHz without the noise cancellation technique.

Next, we tested the noise of the TIA with the noise cancellation path and using values for R_{c1} and R_{c2}. The corner frequency $f_{c,NC}$ of the TIA was 3 kHz, which is 2× higher compared the original TIA without noise cancellation. The total integrated input-referred current noise of the designed TIA was 3.4 and 13.5 pA_{rms} for a bandwidth of 10 kHz and 100 kHz, which is a 2× improvement, with noise cancellation technique. We also calculated the total integrated input-referred current noise of 1.8 nArms for a bandwidth of 950 kHz by extrapolating the noise power spectrum. The proposed design shows a ~2.2× reduction in the input-referred current noise compared to Axopatch, and this could be further reduced to 2.9 pA_{rms} with the same active cooling system at -15 ºC used in the Axopatch 200B [20, 33]. Note that the noise at low frequency is caused by output offset voltage of 10 µV, which has a negligible

contribution on the integrated input-referred current noise over the designed bandwidth.

Table 3.2 lists this work and recent works on TIAs for nanopores. One key feature of our design is the higher dynamic range afforded by discharging baseline current rather than current noise using a noise cancellation technique. The bandwidth of the described design and the total integrated input-referred noise is currently limited by the parasitic capacitance on the PCB and could be further improved with CMOS integration.

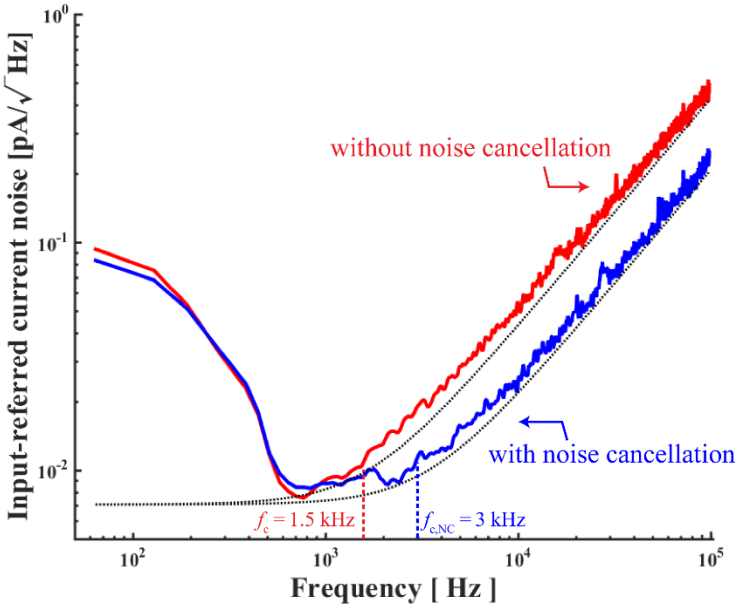


Figure 3.8: Photograph of nanopore and TIA. Measured input-referred noise spectrum density of reported HSD-TIA with and without noise cancellation circuit. The dotted lines are theoretical noise spectrum density with and without noise cancellation path calculated from (14) and (11), respectively.

Table 3.2: Performance Comparison.

SPEC	[33]	[27]	[17]	[45]	This Work
Gain (MΩ)	100	20	20	250	31.6
Bandwidth (kHz)	1,000	1,400	4,000	10	950
Input-Referred Noise (fA/√Hz)	10	8	3	42.1	8.5
Settling Time (s)	N/A	> 10	N/A	N/A	0.04
Supply (V)	± 1.5	± 10	+ 1.5	± 1.5	+5
Power (mW)	45	640	N/A	0.52	65*
Implementation	CMOS	Discrete IC	CMOS	CMOS	Discrete IC

3.7 Biological Measurement Results

We verified the performance of the reported TIA by measuring nanopore insertions into a lipid bilayer. We used wild type α-Hemolysin (α-HL), a natural protein, to form the nanopore in a lipid bilayer composed of 1,2-dipalmitoyl-sn-glycero-3-phosphocholine (DPhPC) from Avanti.

3.7.1 Creating Lipid Bilayer

The lipid bilayer was formed using the painting method [35] with a clean pipette tip on 25 μm diameter PEEK tubing in a buffer consisting of 0.3 M KCl and 10 mM HEPES. Ag/AgCl electrodes were used to bias the cis and trans chambers and to sense the current. The bias voltage was set to 180 mV, which was determined by the salt concentration of the buffer. The entire setup was placed inside of a Faraday cage to minimize environmental interference, such as 60 Hz power line noise.

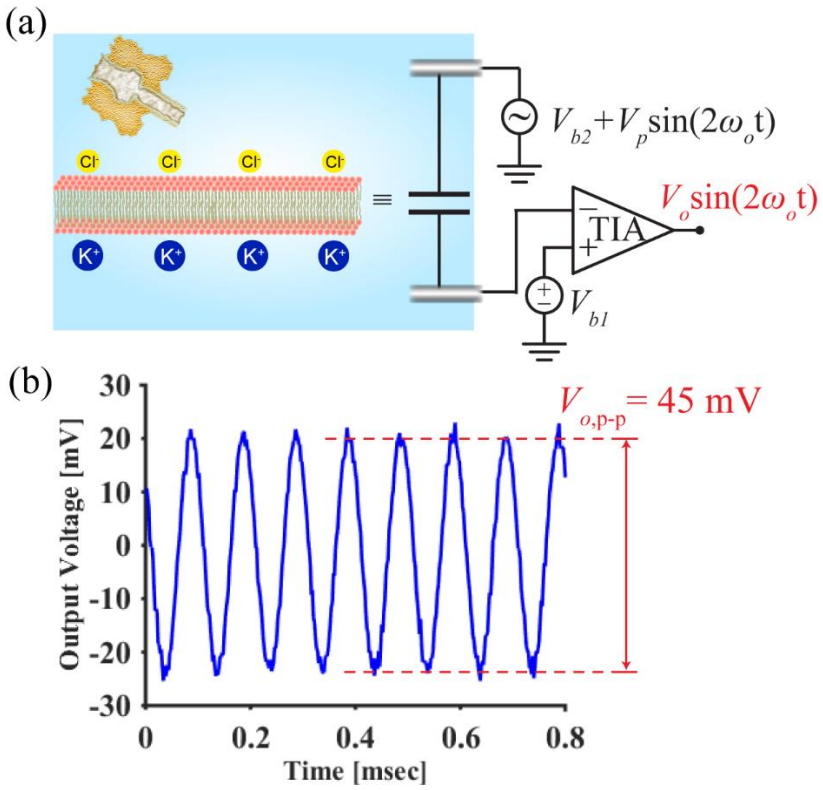


Figure 3.9: (a) Equivalent test circuit with the HSD-TIA for verifying the existence of a lipid bilayer. (b) Measured output waveform of the HSD-TIA with a single-tone sine-wave input.

To verify the formation of the lipid bilayer rather just a clogged tube, a saw-tooth waveform is typically applied at the cis chamber with a conventional resistive feedback TIA [46]. The principle of this test method is that the impedance of the lipid bilayer is mainly capacitive, with a unit area capacitance C_u of ~1-2 μF/mm2 [42]. The output waveform will be a square wave when the TIA works as an R-C differentiator with a capacitor of the lipid bilayer at the input of the designed TIA. However, in our design the low-frequency component of the saw-tooth waveform is discharged by the feedback path.

Instead of a saw-tooth waveform, we verify the existence of a bilayer by applying a single-tone sinusoidal wave to the lipid bilayer. The output voltage of the HSD-TIA with a capacitor at the input is equal to

$$V_{\mathrm{o}}(s) = \frac{C_1}{C_{\mathrm{u}} A_{\mathrm{bilayer}}} s R_{\mathrm{f}} C_2, \tag{3-15}$$

where A_{bilayer} is the area of a lipid bilayer. We apply a sine wave with a frequency of 10 kHz and peak-to-peak amplitude of 10 mV to guarantee the stability of the lipid bilayer, i.e., the lipid bilayer will not break with the 10 mV voltage variation across these two chambers. The output waveform of the HSD-TIA is shown in Fig. 3.9. The peak-to-peak output voltage of the HSD-TIA is 45 mV, which equates to a capacitor of 3.2 pF in series with the input of the designed TIA. This capacitance corresponds well with the theoretical value.

3.7.2 Measurement of Nanopore Insertion

We verified the fast step response by measuring the settling time of the feedback loop when a nanopore is inserting into a lipid bilayer. A nanopore, α-HL, was prepared in the same buffer with a surfactant and added to the cis chamber. Initially, no current channel forms when only the lipid bilayer exists, so the feedback current, I_{baseline}, in the feedback path was zero. An ion channel formed when α-HL spontaneously inserted into the lipid bilayer. A baseline current step, $\Delta I_{\mathrm{baseine}}$, of 58 pA was measured when a single nanopore was inserted into the lipid bilayer. Figure 3.10 shows the settling of the feedback current over time. The settling time of the

designed HSD-TIA was 140 milliseconds without the DC compensation current. After the calibration of DC compensation code D_{comp}, the settling time with the DC current compensation current was reduced to 40 ms, a 3.5× improvement.

Furthermore, the integrator did not saturate during the settling period because of this DC compensation current. In contrast, the settling time of an analog feedback TIA [27] was longer than several seconds and the output was saturated with the same step-input current [28].

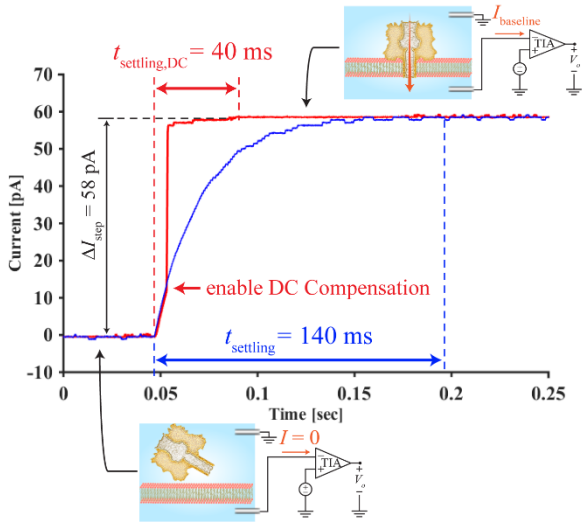


Figure 3.10: Comparison of the step responses of the reported TIA with and without the DC compensation current when a protein nanopore is inserted in the lipid bilayer.

3.7.3 Measurement of DNA Translocation

We observed ssDNA (200 nucleotides) translocation events by adding 0.1 nM of ssDNA to the cis chamber after a nanopore was inserted into the lipid bilayer. The baseline current was ~50 pA measured by the low frequency code D_o with a bias

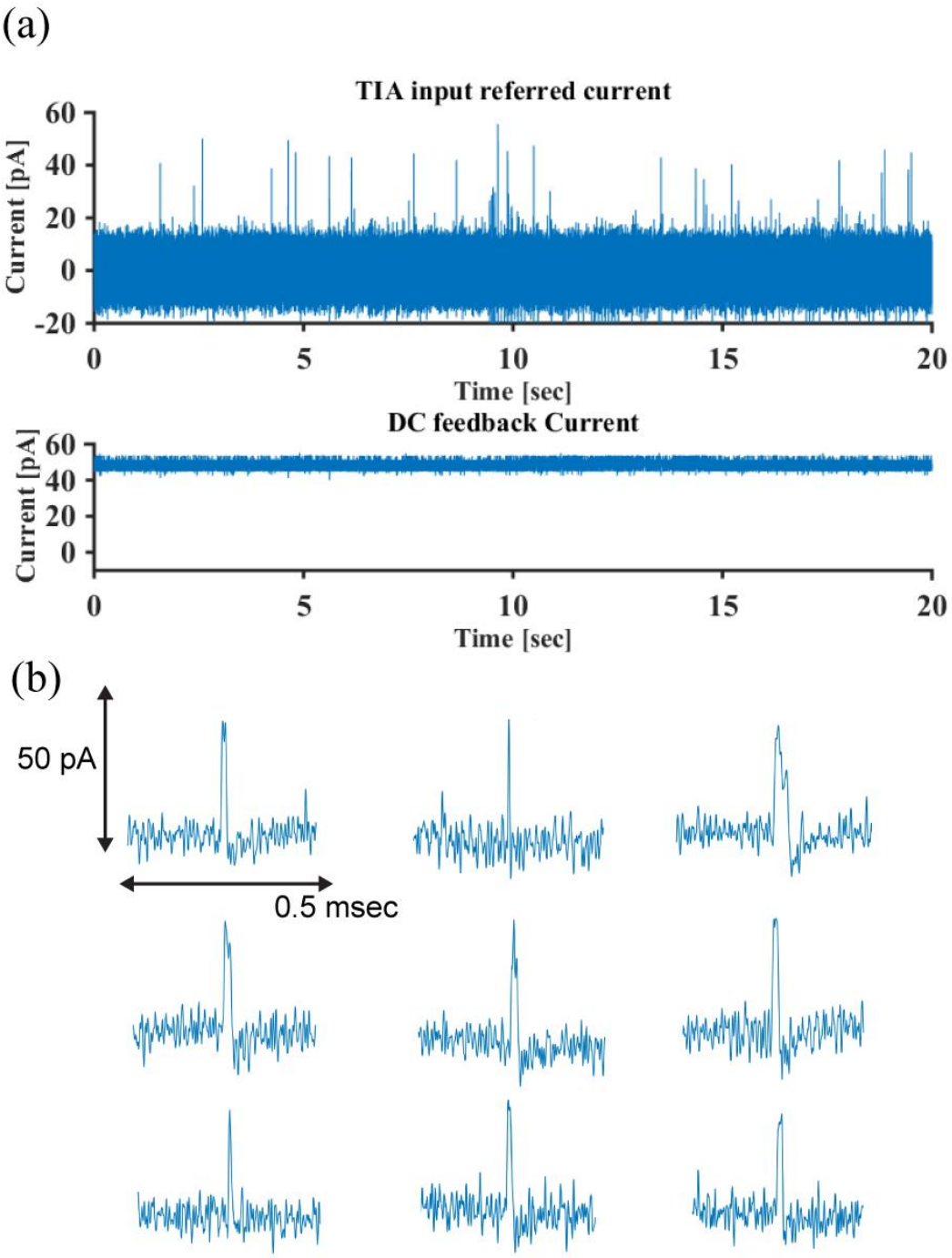


Figure 3.11: Comparison of the step responses of the reported TIA with and without the DC compensation current when a protein nanopore is inserted in the lipid bilayer.

voltage of 150 mV. The output of the HSD-TIA captured the current changes caused by the translocation of ssDNA while the baseline current remained unchanged. As shown in the Fig. 3.11, the ssDNA caused a current change of 30-50 pA with an average translocation time of 0.1 msec. The amplitude and translocation time of the measured data agree well with the results in [2, 3], and demonstrate the feasibility of the proposed HSD-TIA for nanopore-based DNA sequencing.

3.8 Conclusion

In this paper we identified the key requirements for nanopore-based DNA sequencing approaches. We reported a hybrid semi-digital TIA with a noise cancellation technique to achieve the necessary high flat-gain, high-bandwidth, low input-referred noise, and fast step response. The baseline current from ionic diffusion is discharged through a semi-digital feedback loop that improves the dynamic range. The sensitivity of the TIA was increased with the reduction of the input-referred current noise using a noise cancellation technique. Fast settling was obtained with a DC compensation current in this feedback loop. ss-DNA translocation data demonstrate the feasibility of the HSD-TIA for the nanopore-based DNA sequencing. In the future, we will investigate increasing the bandwidth and decreasing the high frequency noise by implementing the proposed concept in a CMOS process and co-integrating the amplifier with the nanopore.

Part of this chapter is reprint of the material as it appears in IEEE TBioCAS 2015. Chung-Lun Hsu, Haowei Jiang, A. Venkatesh, and Drew Hall. A Hybrid Semi-

Digital Transimpedance Amplifier with Noise Cancellation Technique for Nanopore-Based DNA Sequencing. IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), vol. 9, no. 5, pp. 652-661, 2015. The thesis author was the first author of this paper.

Chapter 4

An Hourglass ADC with 162 dB DR Using First-Order Noise-Shaping

4.1 Introduction

This chapter presents a current measurement front-end using an asynchronous Hourglass ADC providing both low-noise amplification and first-order quantization noise shaping. This front-end achieves over 160 dB dynamic range (sub-pA to >10 μA), sub-pA_{rms} input-referred noise, and 2.5× faster readout by eliminating the need for the C-TIA reset switch and compensating the excess loop delay (ELD).

The principle of the asynchronous Hourglass ADC is introduced in Section 4.2, and Section 4.3 discusses the advantages of the proposed Hourglass ADC architecture over conventional architectures. Section 4.4 describes the implementation

and measurement results are presented in Section 4.5. Finally, Section 4.6 concludes the paper.

4.2 Hourglass ADC Architecture

The concept of this current measurement front-end shown in Fig. 4.1 is to process a high DR input current i_s by: 1) amplifying i_s using a C-TIA with a feedback capacitor C_F, 2) folding the output voltage of the C-TIA asynchronously resulting in a current-to-frequency (*I*-to-*F*) conversion, 3) quantizing the output frequency using a time-to-digital converter (TDC). To implement the concept, the front-end consists of a C-TIA followed by two continuous-time comparators that control an Hourglass switch at the input of the C-TIA. By eliminating the need for periodic reset in a conventional C-TIA, it can be shown that this architecture is equivalent to an open-loop delta sigma modulator with a digital first-order differentiator clocked at an oversampling frequency. An adaptive, tunable feedback capacitor array further increases the dynamic range whereby using a larger C_F maintains a moderate switching frequency. This ADC provides >8-bit linearity due to this C_F array and ELD compensation.

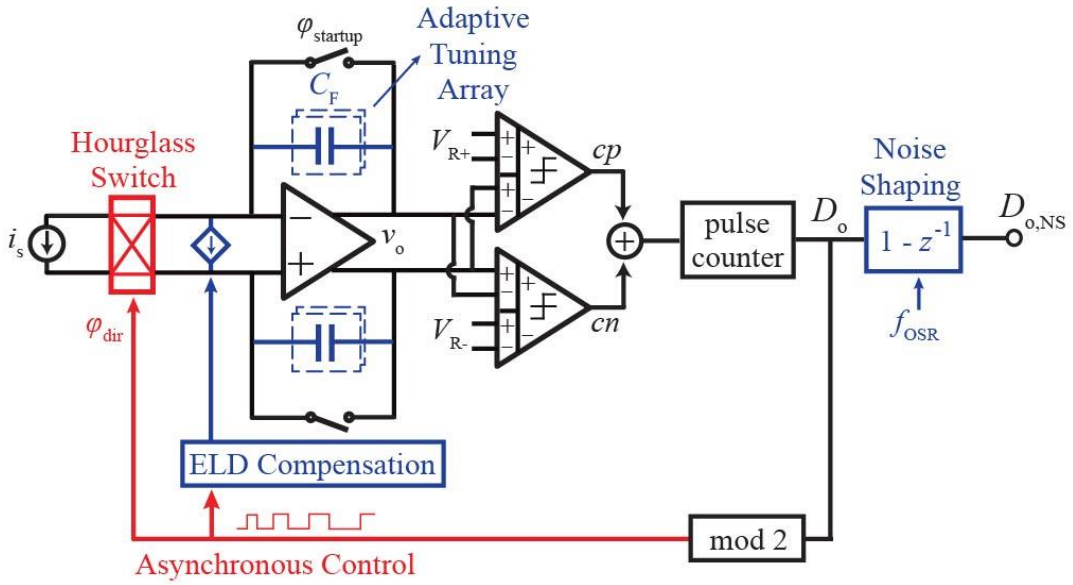


Figure 4.1: Architecture of the current measurement front-end.

4.2.1 *I*-to-*F* conversion

A conventional C-TIA with periodic reset has a DC gain $A_\Omega = T_p/C_F$ with an integration period T_p when the input signal i_s is smaller than or equal to $i_{s,max} = C_F V_{DD}/T_p$. Once $i_s > i_{s,max}$, C_F is saturated and C-TIA cannot amplify the signal before the next rest, as shown in Fig. 4.2(a).

To achieve a high dynamic range, the output voltage of the C-TIA in Fig. 4.2(b) is folded into a predefined voltage window, $V_{R\pm}$, when $i_s > i_{s,max}$. The operation is as follows: the C-TIA with an Hourglass switch modulates the polarity of i_s: during the start-up, the charge on C_F is nulled by the reset switch, and the integrator output voltage, v_o, is set to the common-mode voltage, V_{CM}. Next, the reset switch is deasserted and the C-TIA begins to integrate and amplify i_s. When v_o crosses a predefined threshold voltage, V_{R+} or V_{R-}, the corresponding comparator is triggered

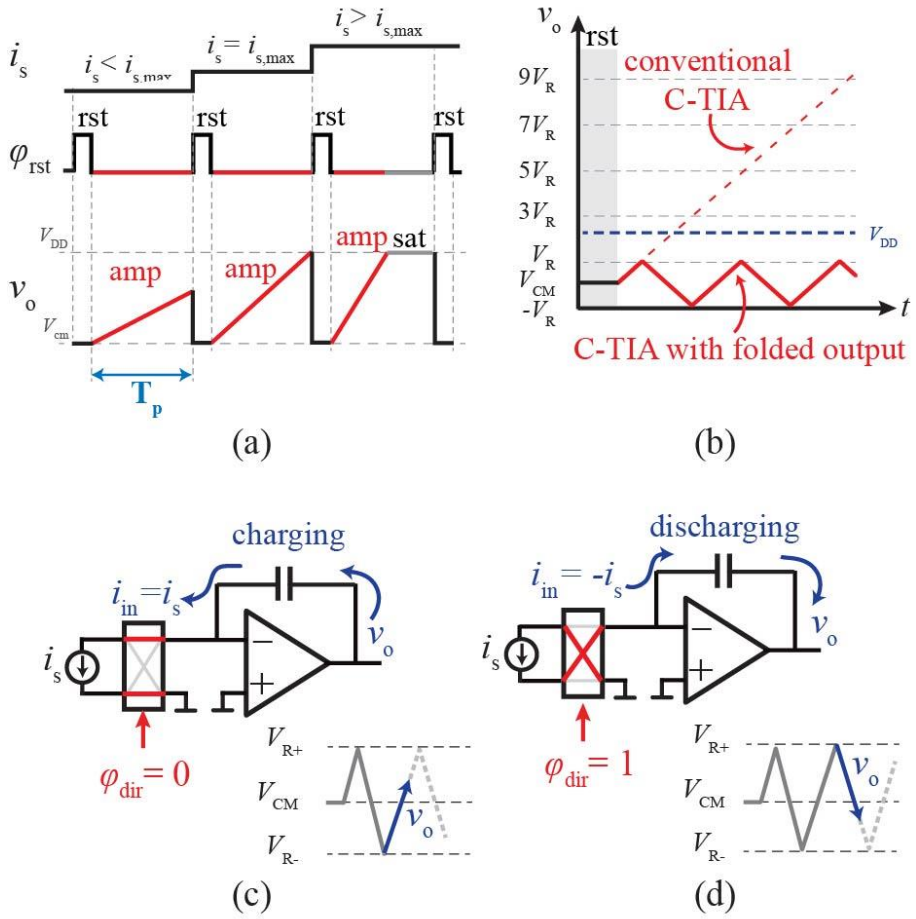


Figure 4.2: Waveform of (a) a conventional C-TIA with period reset, the C-TIA with folded output. The C-TIA with the Hourglass switch folds the output by charging and discharging C_f alternatively in (c) and (d) respectively.

And the direction of the Hourglass switch as well as the polarity of i_s is flipped. The C-TIA keeps integrating i_s by charging (Fig. 4.2c) or discharging (Fig. 4.2d) C_F according to the polarity of the input signal controlled by the Hourglass switch with an asynchronous clock, φ_{dir}. Therefore, the output of the C-TIA with Hourglass switching is bounded by $V_{R\pm}$ without saturation, so the maximum input current i_s is not limited by V_{DD} and the DR of the C-TIA is improved.

The polarity of i_s is asynchronously controlled by the Hourglass switch, and the flipping of the polarity occurs every flipping period $T_{dir/2} = C_f (V_{R+} - V_{R-})/i_s$ when v_o changes by (V_{R+} - V_{R-}). The output waveform v_o of this front-end is a triangular waveform with a peak-to-peak voltage of (V_{R+} - V_{R-}) and a frequency f_{dir}

$$f_{\mathrm{dir}} = 1/(2T_{\mathrm{dir}/2}) = i_{\mathrm{s}}/[2(V_{\mathrm{R+}} - V_{\mathrm{R-}})C_{\mathrm{F}}], \tag{4-1}$$

when the input signal i_s is a DC current. The ideal frequency f_{dir} of the triangular wave is linear proportional to the input amplitude i_s in (1), so this Hourglass structure provides a linear *I*-to-*F* conversion.

4.2.2 Analog-to-Digital Conversion

The input signal is translated into a time domain signal with the linear *I*-to-*F* relationship in (4-1), so the digital output of the front-end can be obtained by quantizing the time information. Here, a discrete-time sampled counter is implemented as a TDC to quantize the converted frequency f_{dir} when the counter accumulates the number of input polarity flips, D_o, in one integration period T_s. As shown in Fig. 4.3, the comparators generate a narrow pulse when v_o crosses $V_{R\pm}$ each time, so the counter detects the number of pulses at the output of both comparators.

The analog-to-digital relationship can be derived by unfolding the triangular wave at v_o, so the total voltage change in one T_s is

$$v_{\mathrm{o,unfold}}[n] \equiv i_{\mathrm{s}}T_{\mathrm{S}}/C_{\mathrm{F}} = (D_{\mathrm{o}}[n] - 1)(V_{\mathrm{R+}} - V_{\mathrm{R-}}) + e_{\mathrm{Q,V}}[n] \tag{4-2}$$

where $e_{q,v}[n]$ is the quantization residue. Because $D_o[n]$ is incremented by one when v_o changes every (V_{R+} - V_{R-}), the LSB at v_o, can be defined as $2V_{REF}$, and the input-referred digital output is

$$D_o[n] = \lfloor i_s T_p / [2(V_{R+} - V_{R-})C_F \rfloor, \tag{4-3}$$

where $\lfloor x \rfloor$ is the greatest integer less or equal to a real value x. Also, $e_{q,v}[n]$ can be mapped from $v_o(t)|_{t=T_p}$ with respect to the phase of φ_{dir}:

$$e_{Q,V}[n] = \begin{cases} v_o - V_{R-}, & \text{with } \varphi_{dir} = 0 \\ V_{R+} - v_o, & \text{with } \varphi_{dir} = 1' \end{cases} \tag{4-4}$$

as shown in Fig. 4. By substituting (4-4) with (4-2) and (4-3), the output residual voltage can be derived as

$$e_{Q,V}[n] \ = i_s T_S / C_F - 2V_R D_o[n]. \tag{4-5}$$

The input-referred quantization error can also be obtained by divided (4-5) to the gain of the C-TIA, A_Ω.

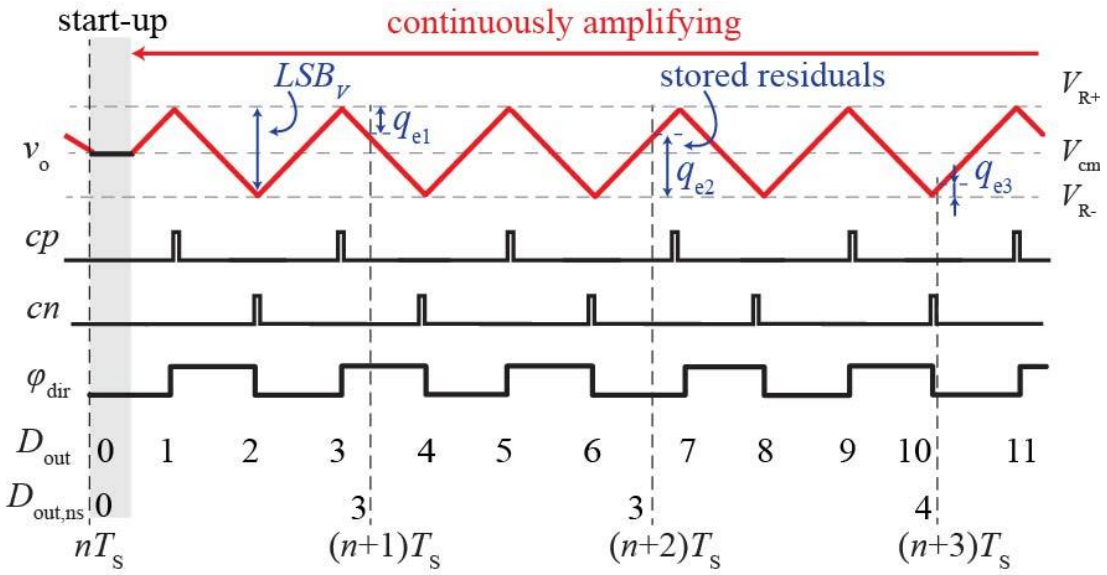


Figure 4.3: Illustration of LSB and quantization error in the Hourglass ADC. The ADC providing the first-order noise shaping behavior when the C-TIA stores residuals at each sampling phase.

4.2.3 First-Order Noise-Shaping Behavior

The C-TIA with an Hourglass switch enables continuous-time amplification without the need for a reset phase, as shown in the waveform in Fig. 4.3. After eliminating the periodic reset, the residual voltage at each sampling phase $t = nT_s$ is stored at the C-TIA as the initial value for the next quantization cycle. Meanwhile, the number of flips occurring in one sampling cycle can be obtained by differentiating the two sampled counter outputs using an oversampling clock φ_{OSR} when the C-TIA and counter are only reset at start-up. Considering a conventional sigma-delta modulator with the stored quantization noise at every sampling time, the Hourglass ADC is an open-loop sigma-delta modulator with the first-order noise-shaping behavior to reduce the quantization noise and improve the resolution.

4.2.4 ELD Compensation

The excess loop delay, T_d, is from the propagation delay of the continuous-time comparators and digital logic for controlling the Hourglass switch. This delay introduces a finite pulse width at the output of two comparators in Fig. 4.3 and the overshoot voltage $\Delta = i_s T_d / C_F$ when v_o exceeds $V_{R\pm}$, so the peak-to-peak voltage of v_o is (V_{R+} - V_{R-} + 2Δ) rather than (V_{R+} - V_{R-}). This overshoot voltage is signal dependent, so finite T_d causes harmonic distortion with decreased f_{dir} in (4-1).

The ELD compensation is achieved by storing and cancelling the overshoot at the start of each φ_{dir}, as shown in Fig. 4.4(a). The feedback capacitor $C_{1,n/p}$ stores both the signal and overshoot voltage at the end of the previous phase in Fig. 4.4(b), and the additional capacitor $C_{2,n/p}$ as well as the $C_{1,n/p}$ sets the initial voltage of v_o as (V_{R+} - V_{R-} - 2Δ) in Fig. 4.4(c). Therefore, the v_o change in one φ_{dir} phase remains constant as (V_{R+} - V_{R-}), and the signal dependent distortion caused by ELD is removed.

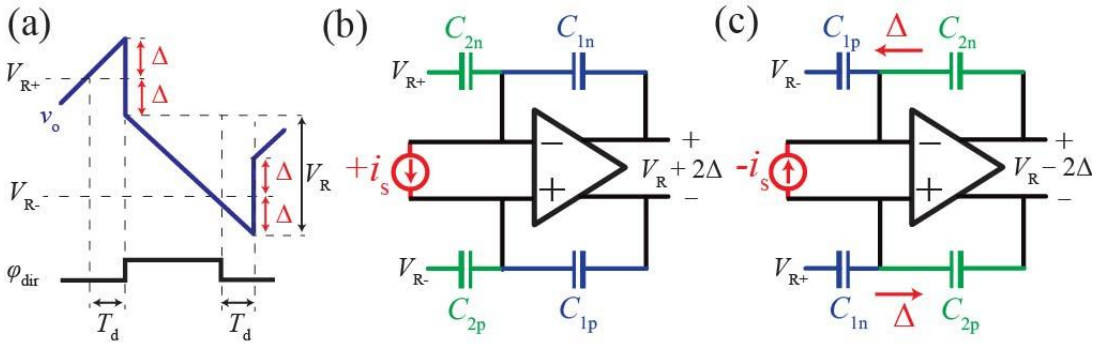


Figure 4.4: The waveform of ELD compensation in (a) by switching the integrating capacitor to compensate the overshoot before and after the polarity of the input flips in (b) and (c) respectively.

4.2.5 Adaptive Feedback Capacitor Array

The power consumption of the Hourglass ADC is a trade-off between DR and conversion time $T_{dir/2}$ with a fixed feedback capacitor. For example, the front-end with a DC input signal of 10 pA to 10 µA generates a triangular waveform with a frequency of 6.25 Hz to 6.25 MHz from (4-1) when C_f and (V_{R+} - V_{R-}) are chosen as 1 pF and 0.8 V, respectively. A fast conversion time can be obtained with a smaller C_f by generating a higher frequency of triangular waveform. A power hungry amplifier with bandwidth higher than 1 MHz is required for a high DR signal of >1 µA, and the conversion time of < 10pA is longer than 1 s with a fixed C_F.

Here, the adaptively tuned feedback capacitor array is implemented to increase the power efficiency and decrease the conversion time of the front-end. The feedback capacitor is tuned adaptively according to the quantized output: a large capacitance is used to maintain the f_{dir} in the bandwidth of C-TIA with a large amplitude i_s while a small capacitance is chosen to decrease the conversion time with a small amplitude i_s. Hence, the power efficiency of the front-end can be improved when the C-TIA generates a 1 Hz – 1 MHz triangular waveform with the >160 dB DR of i_s.

4.3 Asynchronous Sigma-Delta Modulator

The Hourglass ADC operates as an asynchronous sigma-delta modulator (A-SDM) when an input signal is modulated asynchronously by the Hourglass switch according to the signal amplitude. The fundamental and advantages of this asynchronous control loop in the Hourglass ADC comparing with the function of a

conventional A-SDM [47] and a current controlled oscillator (CCO) based ADC are addressed here.

4.3.1 Asynchronous SDM

Both the A-SDM and Hourglass ADC modulate input signal and provide a digital output in time domain, where the A-SDM with a feedback DAC obtains a pulse-width modulated (PWM) output and the Hourglass ADC achieves the current-to-frequency conversion without a feedback DAC. The time information in both architectures can be resynchronized using a time-to-digital converter, which is a counter with a discrete-time sampler in the Hourglass ADC.

Here, the Hourglass ADC with the asynchronous control loop provides advantages: 1) precise control of the linearity with an explicitly defined threshold voltage in the continuous-time comparators rather than a Schmitt Trigger or a hysteretic comparator with a PVT variated build-in threshold voltage, 2) improved input DR without using an explicit DAC in the feedback loop when the maximum input is no longer limited by this DAC as I_{DAC}, 3) the scalability of DR when the maximum input signal of Hourglass ADC is proportional to the bandwidth of the C-TIA and continuous-time comparator, which can be further improved in an advanced process , 4) the modulated tones is proportional to the input amplitude due to the *I*-to-*F* conversion rather than inversely proportional with the input signal as i_s-I_{DAC} in a conventional A-SDM.

4.3.2 CCO-Based ADC

The Hourglass ADC works as a CCO-based ADC when the input current directly controls the oscillating frequency as f_{dir}. The CCO-based ADC contains a 2-level quantizer with the first-order noise-shaping property when the triangular waveform can be mapped from voltage to phase domain: $v_o=[V_{R-},V_{R+}]\equiv[0, \pi]$ with $\varphi_{dir}=0$, and $v_o=[V_{R+},V_{R-}]\equiv[\pi, 2\pi]$ with $\varphi_{dir}=1$. Unlike a CCO-based ADC with a finite input impedance, the Hourglass ADC provides a relatively low input impedance compared to the sensor impedance due to the virtual ground at the input of the C-TIA, so the Hourglass ADC minimizes the loading effect to the sensor in current-sensing applications.

4.4 Integrated Circuit Implementation

4.4.1 System

The current measurement front-end was implemented to obtain more than 160 dB DR, which is from sub-pA to more than 10 μA. The fully-differential topology was designed to reduce common-mode noise with a matched sensor impedance at the differential input in a 0.18μm CMOS SOI process. The power supply is 1.5 V and common-mode voltage is 0.75 V to maximize the output swing of C-TIA. The reference voltage $V_{R\pm}$ is chosen 0.35 V and 1.15 V to minimize the noise when the system noise is dominated by the jitter noise in the *I*-to-*F* conversion [48]. C_F was

adaptively selected as 0.1, 1, and 10 pF according to the digital output code. The integration gain is variable allowing the ADC to quantize 100× DR by changing C_F.

4.4.2 Amplifier

The bandwidth of amplifier was designed according to the range of *I*-to-*F* conversion in the front-end, and a high gain > 80 dB is preferred to prevent the finite input swing modulating the sensor with a finite resistance R_p. Therefore, a two-stage, gain-boosted topology, and a dual cascode compensation technique was implemented to increase the power efficiency, extend the bandwidth, and to reduce the gain peaking beyond the unity-gain frequency [49] , as shown in Fig. 4.5. The amplifier achieved a DC gain of 99 dB and a unity-gain bandwidth of 28 MHz from the simulation results. The stability of the C-TIA was guaranteed when phase margin was larger than 71° phase margin across all loading conditions from the tunable C_F array and up to 5 pF of sensor capacitance C_p. In addition, the amplifier was implemented with an autozeroing structure in conjunction of C-TIA to minimize both the offset and the low-frequency noise of the amplifier [50], so the sensor modulated by the offset during the Hourglass switching was minimized.

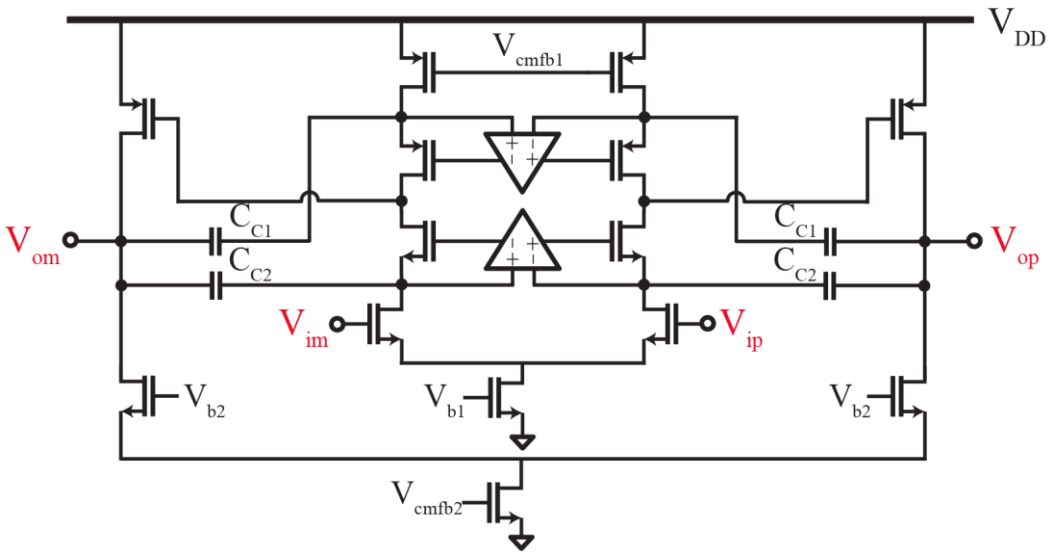


Figure 4.5: Schematic of dual cascode compensation gain-boosted amplifier

4.4.3 Switch

To prevent the loss of input signal during the amplifying phase, i.e., to minimize the partial of i_s flowing into the reset switch rather than integrating by the C-TIA, a low-leakage switch was designed using three transmission gates to minimize the off-leakage current [51]. When this low-leakage switch is off, the V_{DS} of the transmission gate connecting to input node is approximately zero with both drain and source voltage as V_{CM}, so the off-leakage current at the input node of C-TIA is reduced to less than 100 fA.

The hourglass switch contains four identical transmission gates were used in the hourglass switch to minimize the charge injection and clock feedthrough when the voltages across these switches remain constant and cause negligible off-leakage current.

4.4.4 Continuous-Time Comparator

The continuous-time comparators are implemented using the auto-zeroed switch-capacitor structure [52]. The comparators samples both the reference and offset during the start-up phase, and the comparator keeps comparing with the synchronized reset in the C-TIA. The comparator was design with two stage amplifiers to provide a high gain and minimize the propagation delay. The simulated propagation delay of the comparator is less than 5 ns, and the overshoot as well as the harmonic distortion caused by the loop delay is compensated.

4.4.4 Digital Blocks

The digital outputs from two continuous-time comparators were first combined into one pulse train by a XOR logic. A carry-ripple counter was implemented to accumulate the number of pulses from the XOR. The first D-Flip Flop in the counter is reused as the modulo-2, when the LSB of the counter is the control signal φ_{DIR} of the hourglass switch. Therefore, the total propagation delay of the digital block is only two logic gates delay and less than the delay of comparators.

4.5 Measurement Results

The current measurement front-end including pads occupied 1×2mm^2, as shown in Fig 4.6. The common-mode and reference voltage were provided off-chip. For performance characterization of the ADC, the input current sweeps were

performed using a Keithley 6430 source meter and an Opal Kelly XEM6310 FPGA was used to implement the digital blocks and capture the digital output.

The function of the front-end was characterized with a single-ended input signal and an equivalent electrical model at both the differential inputs. First, the ADC was measured with a DC input: Figure 4.7 shows a measured transient signal for a 200 pA DC input current as an example of output of C-TIA and control signal for the hourglass switch when the ADC was only reset at start-up. The overshoot at the input polarity flipping instant is removed with the ELD compensation. Spectrum of 20 pA and 200 pA input currents are shown in Fig. 4.8(a) and (b) where f_{dir} is 126 Hz and 1.2 kHz, and the integrated noise over the noise bandwidth (NBW), the same as the maximum signal bandwidth f_{dir}, is 101 fA_{RMS} and 3.1 pA_{RMS}, respectively. Because the ADC is not reset after start-up, the ADC operates exhibit the first-order noise-shaping behavior in the PSDs with an oversampling frequency of 100 kHz.

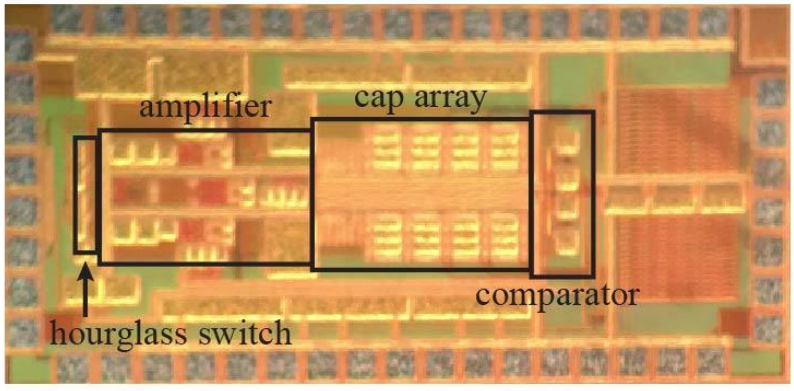


Figure 4.6: Photograph of the chip.

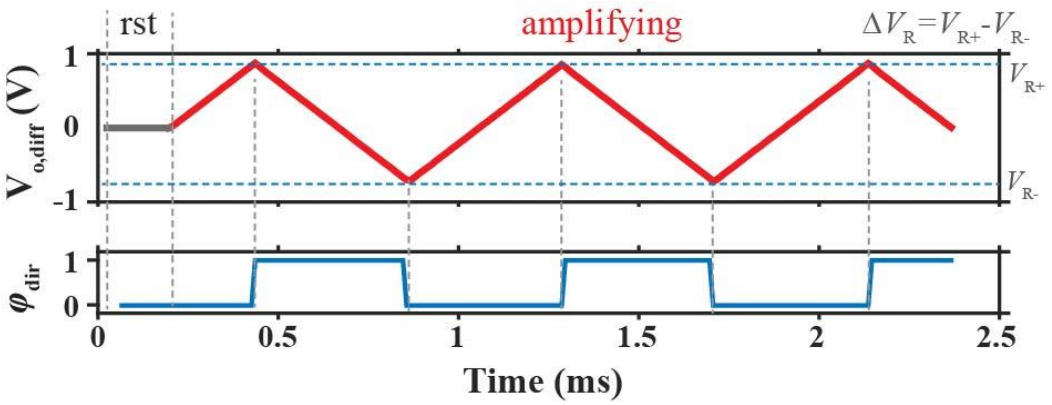


Figure 4.7: Photograph of the chip.

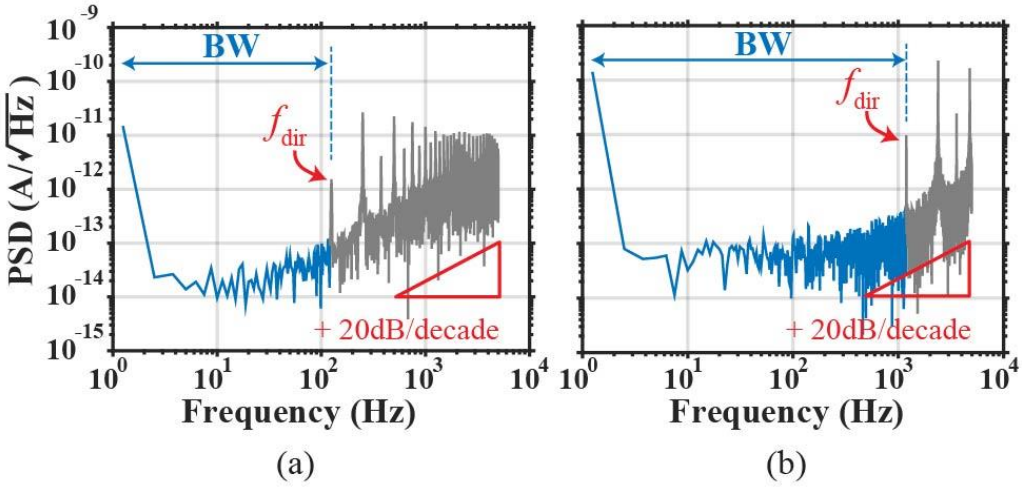


Figure 4.8: Photograph of the chip.

The linearity and the DR of the designed ADC was measure using a DC input signal and shown in Fig. 4.9 with different feedback capacitor. The measured current and linearity demonstrating that the Hourglass ADC can measure up to 12.5 µA and down to 100 fA (C_F = 10 pF) with a maximum conversion time, $T_{conv,max}$, of 100 ms (C_F = 0.1 pF).

The overall power consumption of the ADC was 3.5 mW while the most part of power was consumed in the OPAMP. The measurement results of the front-end are summarized in Table 4.1. The results show that this work has the highest dynamic range (162 dB) and 5× faster normalized conversion time, and Shreier FOM of 191 dB compared to the state-of-the-art.

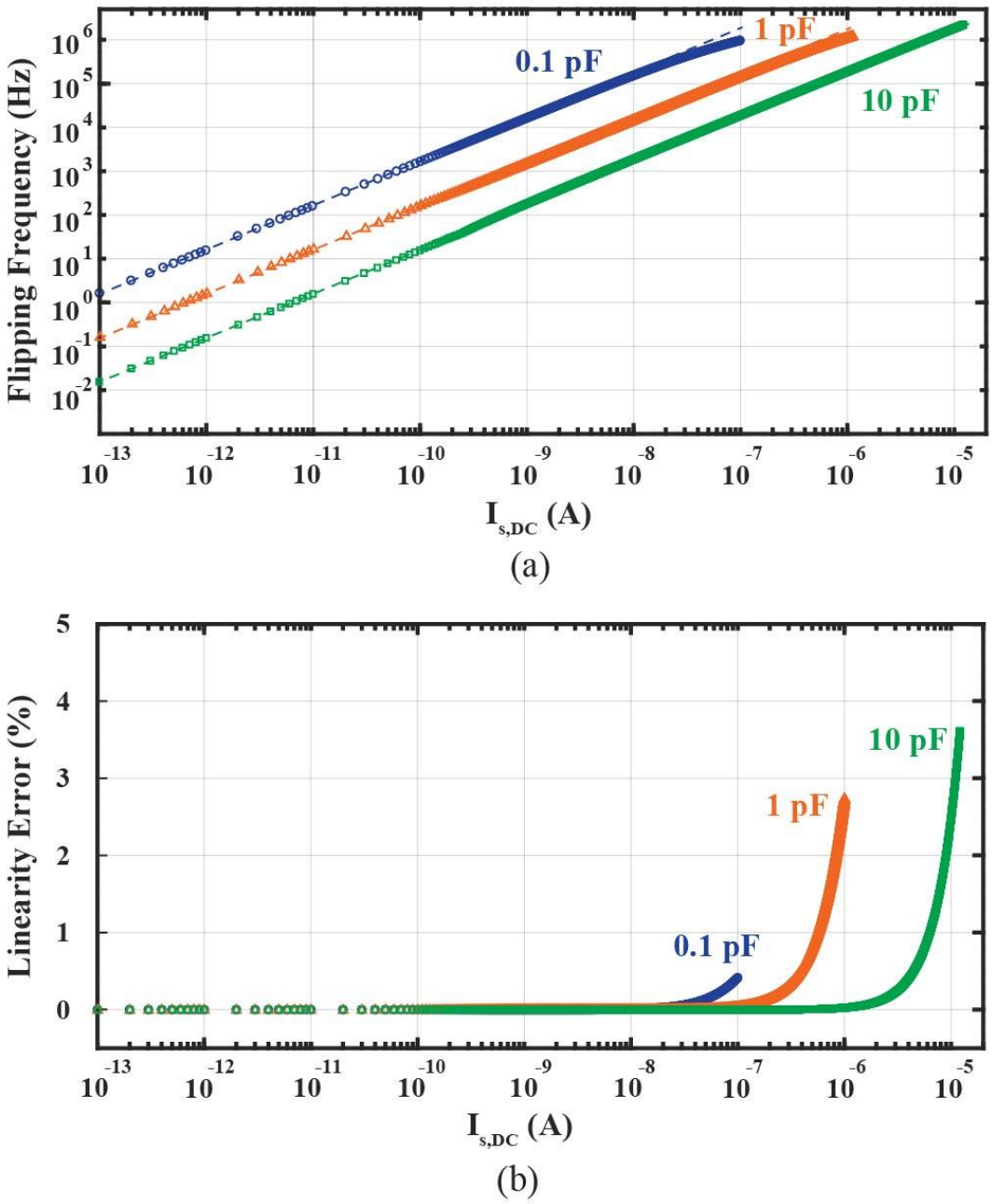


Figure 4.9: Dynamic range and linearity error.

Table 4.1: Performance Comparison.

Parameter	Stanacevic TBioCAS'07	Roham TBioCAS'08	Ahmadi TBioCAS'09	Sutula TCAS-I'14	Prabha JSSC'15	Dai TBioCAS'16	Li TBioCAS'16	Son TBioCAS'17	This Work
Architecture	SDM	SDM	Osc.	SDM	SDM	Osc.	C.C. + SDM	SDM	**SDM**
Tech. (µm)	0.5	0.5	0.18	2.5	0.18	0.18	0.5	0.18	**0.18 SOI**
Power (mW)	0.08	0.06	0.11	0.03	0.08	5.22	0.24	0.02	**3.5**
$I_{max,RMS}$ (µA)	1	0.43	1	32	4	11.6	16	3	**12.5**
$I_{min,RMS}$ (pA)	0.1	12	1,000	2,000	1,000	0.2	0.1	100	**0.1**
(NBW (Hz))	(N/A)	(100)	(N/A)	(1,000)	(N/A)	(100)	(1)	(1,000)	**(100)**
$T_{conv,max}$ (s)	8.0	10.0	1.0	2.0	0.4	0.25	1	0.004	**0.1**
$T_{conv,norm}$* (s)	8.0	1.2	> 10	> 10	> 10	0.5	50**	4	**0.4**
DR (dB)	140	91	60	84	72	155	164	88.9	**162**
$FOM_{Shreier}$ (dB)	172	132	90	120	103	181	183**	158	**191**

4.6 Summary

This paper proposes a current measurement front-end using an asynchronous Hourglass ADC. The fundamental outlines the design trade-offs and explains the advantages of this current measurement front-end. The designed front-end has several advantages including the low-noise, increased input dynamic range, continuous-time operation, and excess loop delay compensation. Moreover, the C-TIA with the Hourglass switch works as an asynchronous sigma-delta modulator to further reduce the quantization noise and improve the dynamic range without the use of a feedback DAC. Such advantages are very beneficial for the design of low-noise, high dynamic range, low-power current-mode ADC.

An experimental prototype demonstrates the ability of a 162 dB dynamic range of currents that span from sub-pA to tens-μA. This prototype of the proposed front-end achieves a state-of-the-art of Shreier FOM of 191 dB and 5x faster normalized conversion time, which is difficult to achieve in conventional front-end architectures.

Portions of this chapter contains both a reprint of the material and currently being prepared for submission for publication of the materiel as it appears in IEEE ISSCC 2018. A Current Measurement Front-end with 160dB Dynamic Range and 7 ppm INL. IEEE International Solid-State Circuits Conference (ISSCC). The dissertation author was the first author of this paper.

Chapter 5

An Hourglass ADC with 160 dB Dynamic Range and 7 ppm INL

5.1 Introduction

This paper presents a wide DR current measurement AFE (Fig. 5.1) [53]. The core of this work is the asynchronous Hourglass ADC which uses a C-TIA and an Hourglass switch to achieve the wide DR and the first-order noise shaping. A foreground linearity correction technique is proposed to reduce the power consumption in the C-TIA. To further improve the linearity and power efficiency, a predictive I-DAC closes the loop by generating a coarse estimation of the input current such that the Hourglass ADC only processes the difference. The resulting AFE achieves a 7 ppm linearity error over a 160 dB dynamic range from 100 fA to 10 μA.

This chapter is organized as follows. Section 5.2 introduces the system architecture. Section 5.3 analyzes the performance of the AFE. Section 5.4 derives the noise limitation of the system. Section 5.5 describes the implementation and measurement results are provided in Section 5.6 to demonstrate the performance. Finally, Section 5.7 concludes this paper.

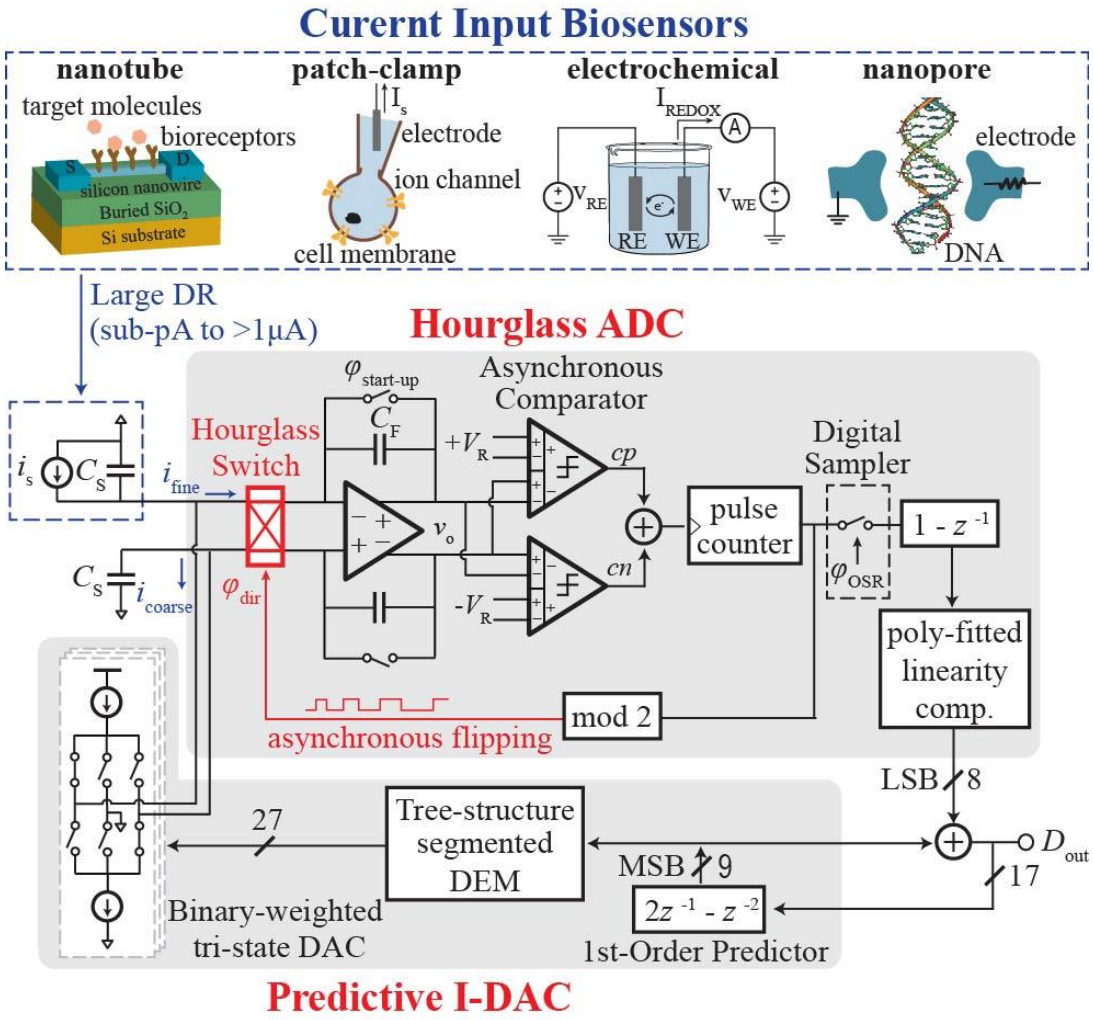


Figure 5.1: Illustration of the closed-loop Hourglass ADC with a corresponding equivalent circuit model for current input biosensors.

5.2 Architecture Overview

Figure 5.1 shows a block diagram of the wide DR current-mode AFE that consists of two main blocks: an oversampling asynchronous Hourglass ADC and a *N*-bit predictive I-DAC. The core of the Hourglass ADC is an open-loop asynchronous ΔΣ consisting of a C-TIA in conjunction with an Hourglass switch driven by the outputs of two continuous-time comparators (Fig. 5.2a). In contrast to a conventional periodically reset C-TIA with a DC input signal, the C-TIA with the assistance of the Hourglass switch obtains a high DR and continuous-time operation by folding the C-TIA output within a predefined window, $\pm V_R$, by flipping the polarity of the input signal, as shown in Fig. 5.2(b) and (c). This asynchronous folding prevents the C-TIA from saturating and therefore improves the DR by alternating between charging and discharging the feedback capacitors, C_F. The behavior of the asynchronous folding is equivalent to a single bit quantizer with a quantization level of (V_{R+} - V_{R-}). A counter accumulates the number of comparator pulses, *cp* and *cn*, within a sampling period, T_S. The least significant bit (LSB) and quantization error can be defined as $LSB = (V_{R+} - V_{R-}) \times C_F/T_S$ and $q_e = [V_{R+}, V_{R-}] \times C_F/T_S$ at $t = nT_S$, respectively.

Because the C-TIA with the Hourglass switch eliminates the need of the period reset, the quantization error is retained by not resetting C_F after each sampling instance. By not doing so, this structure provides first-order noise shaping with an oversampling clock, as shown in Fig. 5.2(d). Like oscillator-based quantizers, a digital representation of the signal is obtained by sampling the output of the counter and digitally differentiating at the oversampling frequency, f_{OSR}. Thus, the signal transfer

function is flat over the singal bandwidth, and noise transfer function is first-order noise shaped as $1\text{-}z^{-1}$ provided by this digital differentiator. The purpose of the sampler is to synchronize the asynchronous signal φ_{DIR} to a known clock frequency, and this step may be bypassed in some continuous-time systems [54]. Therefore, this structure is an open-loop ΔΣ without the need for an explicit DAC as in a conventional asynchronous DSM, which limits the DR in terms of the maximum input signal [55]. Due to the open-loop operation, the linearity error caused by circuit non-idealities, e.g., finite gain and bandwidth of the amplifier in the C-TIA, is corrected using a poly-fitted digital calibration (described later).

The power efficiency and linearity of the Hourglass ADC is further improved when an I-DAC subtracts an estimated current from the input signal. The I-DAC is controlled by a first-order digital predictor that extrapolates the input based on the previous data. The I-DAC linearity is improved through dynamic element matching (DEM) . This structure is similar to a conventional two-step coarse-fine ADC [56]; however, the use of the predictor instead of an explicit coarse quantizer prevents the additional noise introduced from a current amplifier such as current-conveyer and thus improves the DR of the proposed ADC. The digital code D_{out} of the AFE is obtained by combining the *M*-bit and *N*-bit digital output of the predictor and the Hourglass ADC, respectively. Thus, this AFE enables wide dynamic range and low quantization noise while simultaneously providing the necessary low input impedance for current measurements.

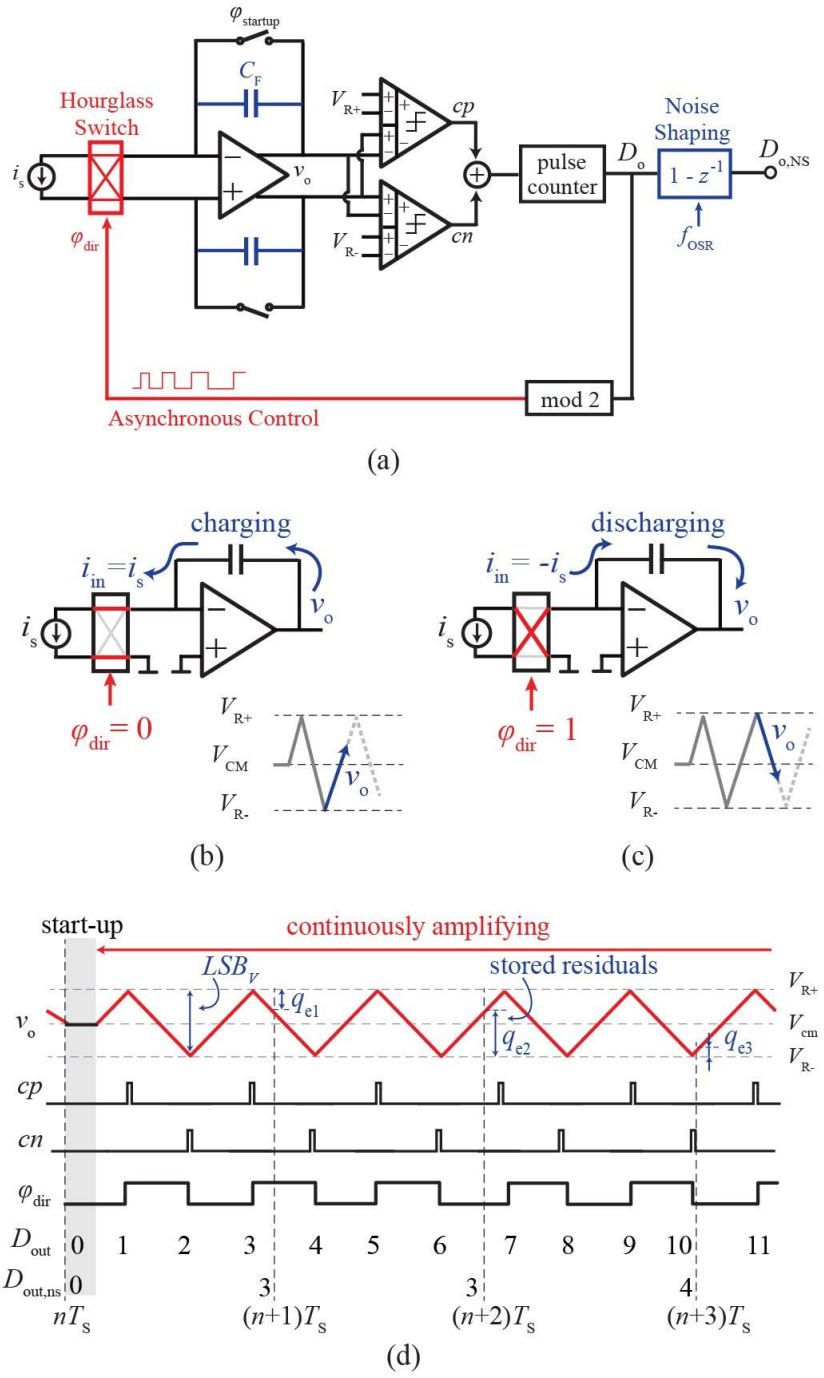


Figure 5.2: (a) Schematic of Hourglass ADC with an asynchronous control loop. The C-TIA and the Hourglass switch fold the output by charging and discharging C_F alternatively, as shown in (b) and (c), respectively. (d) Complete waveforms illustrating operation.

5.3 System Analysis

5.3.1 Open-Loop Delta-Sigma Modulation

A block diagram of the Hourglass ADC is shown in Fig. 5.3(a), which is equivalent to an open-loop ΔΣ. The signal transfer function of the Hourglass ADC is constant over signal bandwidth since the pole at DC introduced by the C-TIA is cancelled by the zero at DC of the digital differentiator. Quantization noise is introduced at each oversampling instant by the digital sampler in Fig 3(b), so this noise can be modeled at the input of digital sampler. Hence, the noise transfer function is the same as the digital differentiator.

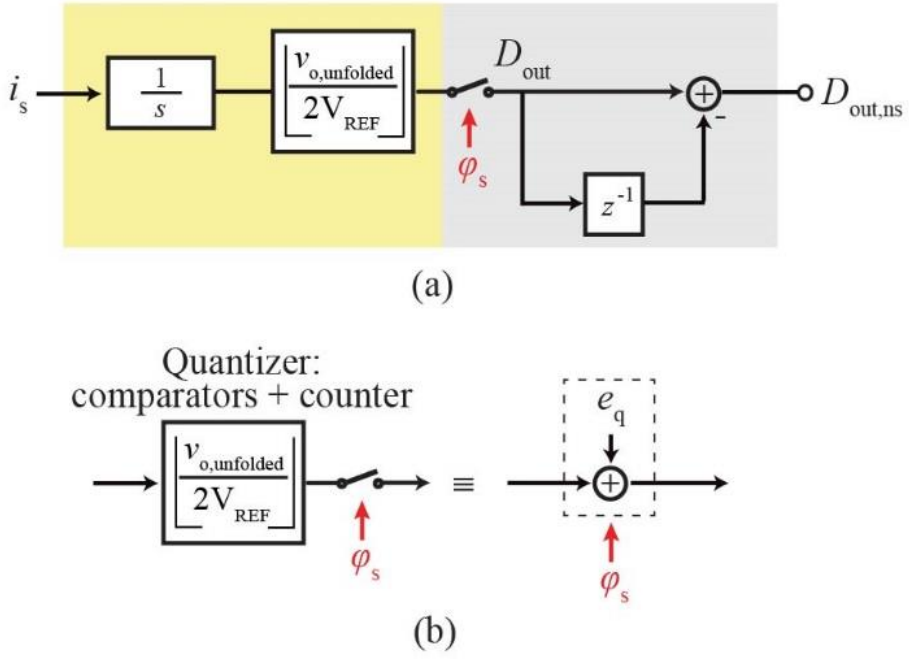


Figure 5.3: (a) Block diagram of Hourglass ADC and (b) the quantizer.

Although the STF is constant, the relationship between minimum quantizable amplitude and signal bandwidth is limited by the gain of the C-TIA with -20 dB/decade due to the constant threshold voltage $V_{R\pm}$ in asynchronous control loop. Thus integrating a sinusoid with an amplitude of I_p and frequency of f_{sig} triggers the comparator when

$$|v_o| = \left| \int_{t_1}^{t_2} I_p \sin(2\pi f_s t + \varphi_0)\, dt \right| / C_f \geq V_R. \tag{5-1}$$

where φ_0 is the initial phase of the input at $t = t_1$. The minimum detectable signal with such signal frequency can be derived by integrating the input current over either [t_1, t_2] = [0, 1/2f_s] when $\varphi_0 = 1$ or [1/2f_s, f_s] when $\varphi_0 = 0$. Thus,

$$I_{p,min} \geq 2\sqrt{2} f_{s,max} C_f V_R, \tag{5-2}$$

That is, when the integration of the positive or negative half cycle is greater than or equal to V_R, the comparator flips the polarity of the input switch to neutralize the charge stored on C_F. If a input signal is less than $I_{p,min}$, the charge is "self-neutralized" and the Hourglass ADC cannot quantize it. Since this sinusoid triggers the comparators every half cycle, the the feedback loop is locked with the signal frequency, (i.e., $f_{dir} = f_s$), which defines the bandwidth.

5.3.2 *I*-to-*F* Conversion Linearity

This structure results in a current-to-frequency (*I*-to-*F*) conversion where the polarity is flipped asynchronously according to the amplitude of input signal. Unlike in an asynchronous ΔΣ which has an asymmetric triangular waveform with a

frequency inversely proportional to input amplitude, the C-TIA output in Fig. 5.2 is a symmetric triangular waveform with a fundamental frequency

$$f_{\mathrm{dir}} = \frac{i_{\mathrm{s}}}{2(V_{\mathrm{R+}} - V_{\mathrm{R-}})C_{\mathrm{F}}}. \tag{5-3}$$

which is linearly proportional to the input amplitude. Due to the high *OSR* and DAC, the harmonic tones (equivalent to idle tones in a conventional ΔΣ) are guaranteed to be out-of-band and are removed by the decimation filter.

The linearity of the Hourglass ADC can be understood by examining the *I*-to-*F* behavior. A low-frequency input signal is up-modulated by the Hourglass switch as a square wave due to the asynchronous flipping frequency f_{dir} in (5-3), and this up-modulated signal is integrated and amplified as a triangular wave at the same frequency f_{dir} by the C-TIA as shown in Fig. 5.4(a). The Fourier transform of an ideal triangle is an infinite frequency series with the fundamental tone at f_{dir} and the odd order harmonics.

If the amplifier has finite gain and bandwidth, the output is filtered resulting in distortion (Fig. 5.4b) that can be expressed as

$$v_{\mathrm{o,real}}(s) = \frac{1}{s^2 C_{\mathrm{f}}} \tanh\left(\frac{s}{2}\right) \frac{1-\varepsilon_{\mathrm{gain}}}{1+s/\omega_{\mathrm{p,loop}}} i_{\mathrm{s}}(s), \tag{5-4}$$

where $\varepsilon_{\mathrm{gain}}$ and $\omega_{\mathrm{p,loop}}$ are the loop gain error and -3-dB gain bandwith, respectively. The frequency of this distorted triangular waveform can be calculated when the output reaches $\pm V_{\mathrm{R}}$ in time domain

$$\left| v_{\mathrm{o}}\left(t = \frac{1}{2f_{\mathrm{dir}}}\right)_{\mathrm{peak}} \right| = V_R. \tag{5-5}$$

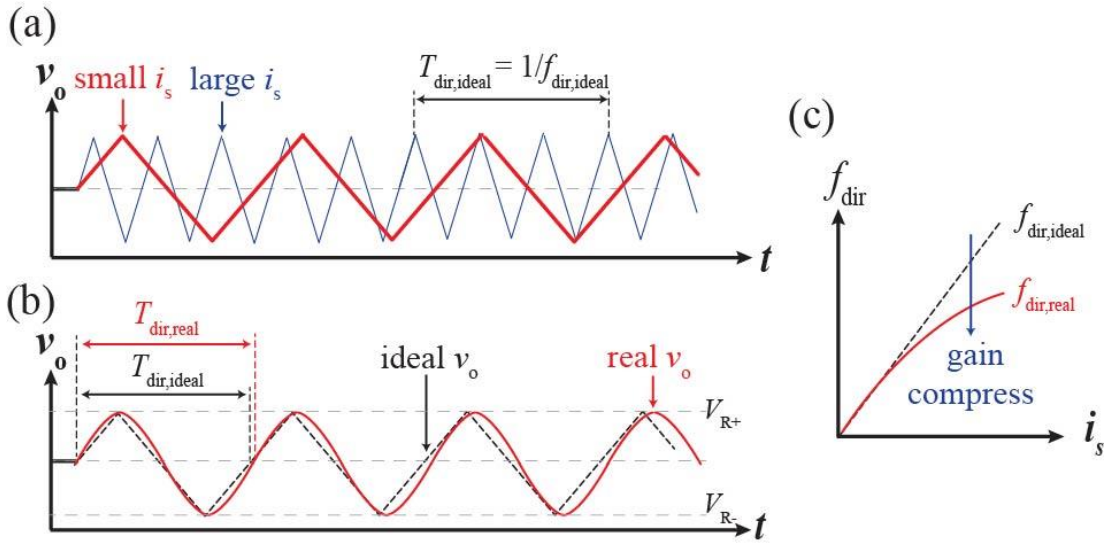


Figure 5.4: (a) Waveform showing the *I*-to-*F* conversion. (b) Distortion caused by the finite-bandwidth of the amplifier and (c) resulting *I*-to-*F* compression.

Because the amplitude of the *n*-th harmonic in a triangle wave is inversely proportional to n^2, the *I*-to-*F* distortion is negligible if $2\pi f_{dir} << \omega_{p,loop}$. However, f_{dir} increases when more harmonics are filtered resulting in *I*-to-*F* gain compression, as shown in Fig. 5.4(c). Numerical results for the linearity as a function of the bandwidth are shown in Fig. 5.5 allowing one to design the C-TIA according to the desired linearity and bandwidth. For example, $\omega_{p,loop}$ must be greater than 3.2× f_{DIR} to obtain a 4-bit linearity whereas 52× f_{DIR} is reqruied to achieve 8-bit linearity. Compared to the distortion in a CCO caused by the higher order *I*-*V* relationship of a transistor, the linearity of the Hourglass ADC is precisely expressed when C_F, V_R, ε_{gain}, and $\omega_{p,loop}$ are known.

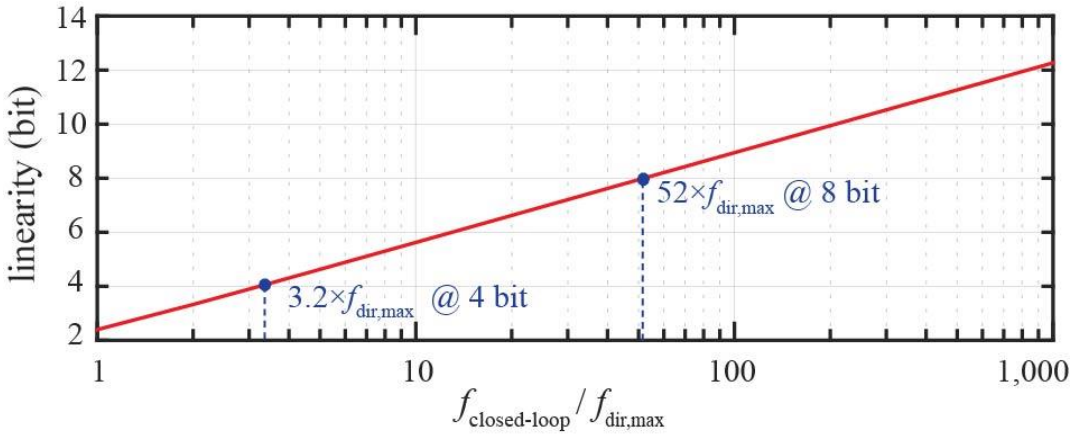


Figure 5.5: Relationship between *I*-to-*F* linearity and the normalized amplifier bandwidth.

5.3.3 Predictive DAC

The Hourglass ADC can quantize a high DR input current when this ADC is an open-loop ΔΣ modulators without an DAC in the feedback loop, which limits the DR smaller than the full range of the DAC in both a conventional synchronous and asynchronous closed-loop ΔΣ modulators. The Hourglass ADC alone can process a higher DR input current by providing a wider range of *I*-to-*F* conversion with reduced linearity and requiring a power hungered amplifier as described before.

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To improve the power efficiency of a ADC, a conventional two-step coarse-fine ADC can be designed when a coarse ADC and DAC pair provides a coarse signal component, i_{coarse}, to subtract the input signal, and the Hourglass ADC as a fine quantizer can only quantize the coarse residual by constraining the input range of Hourglass ADC as $i_{\text{coarse}} - i_{\text{sig}}$. Due to the input signal as a current rather than a voltage, an extra current amplifier, such as current conveyer, is required to mirror an input current into two paths for coarse and fine conversion. This current amplifier, which is usually a current conveyer [57], degrades the noise, distortion, and input impedance of the AFE [14, 15].

Here, the I-DAC is controlled using a digital predictor [58] to extrapolate the incoming signal in the next oversampling phase from previous two digital outputs:

$$D_{\text{coarse}}[n] = D_{\text{out}}[n-1] + \frac{dD_{\text{out}}}{dt}T \approx D_{\text{out}}[n-1] + \{D_{\text{out}}[n-1] - D_{\text{out}}[n-2]\}. \quad (5\text{-}6)$$

This is equivalent to a digital filter of $2z^{-1} - z^{-2}$ in the feedback control loop shown in Fig. 5.1. The difference between i_{sig} and i_{coarse}, which is the extrapolated error, is the residual current as the input of the Hourglass ADC:

$$i_{\text{fine}}[n] = i_{\text{sig}}[n] - \{2D_{\text{out}}[n-1] - D_{\text{out}}[n-2]\} = 2I_{\text{p}}\left\{(1-\cos(\frac{\pi}{OSR}))\cdot\sin(\frac{n\pi}{OSR}+\varphi)\right\}, \quad (5\text{-}7)$$

where input signal is $i_{sig} = I_{\text{FS}}\cdot\sin(2n\pi f_{\text{sig}}/f_{\text{OSR}} + \varphi)$ with the full-scale value of i_{sig}, maximum signal frequency of f_{sig}, phase of φ. *OSR* is the oversampling ratio $f_{\text{OSR}}/2f_{\text{sig}}$. Therefore, the required OSR_{min} to ensure $i_{\text{fine}}/i_{\text{FS}}$ less than *N* bit LSB can

be derived:

$$OSR_{\min} = \pi / \cos^{-1}[1 - 2^{-(N+1)}/i_{\mathrm{FS}}]. \quad (5\text{-}8)$$

For example, the residual signal for the input of Hourglass ADC is less than 9 bit LSB, $i_{\mathrm{full}}/2^9$, when $OSR_{\min}$ is larger than 72.

Due to the high-pass behavior of the predictor, the extrapolating error is less than the required N bit LSB in (5-8) when the bandwidth of an input signal is less than $2OSR_{\min} f_{\mathrm{sig}}$. Any out-of-band noise will cause the increase of the extrapolating error i_{fine} and hence degrades the linearity of following ADC especially when the input signal is directly processed by the ADC without an anti-aliasing filter. Here, the C-TIA in the Hourglass ADC provides a first-order low-pass filtering to remove any out-of-band noise, so the prediction error can be further minimized.

Note that even though the residual is less than N bit LSB, the Hourglass ADC is designed to quantize the input range of N-1 LSB, i.e. 2× LSB, to accommodate the mismatch from I-DAC and extrapolating error even when the mismatch of the I-DAC can be randomized and linearized using a DEM technique [59]. In addition, an over-ranging detection method is used to obtain the correct control code for the I-DAC to guarantee i_{fine} smaller than $i_{\mathrm{full}}/2^N$ once a large out-of-band noise or step input occurs. The detail of this method will be described in Section 5.5.6.

5.4 Noise Analysis

The noise of the AFE is contributed by the Hourglass ADC and I-DAC, which can be analyzed separately when these two noise sources are uncorrelated. The power

optimization of the system respect to the range of i_{coarse} and i_{fine} is also discussed here based on the noise analysis.

5.4.1 Noise in Hourglass ADC

First, the noise of the Hourglass ADC is analyzed based on the *I*-to-*F* conversion. This behavior is like a relaxation oscillator when a fixed input DC current generates a constant oscillating frequency, which is f_{dir}, so the circuit noise causes the jitter of f_{dir}, as shown in Fig. 5.6. The root-mean-square (rms) of this jitter noise is obtained by calculating the ratio between the voltage noise, $v_{n,rms}$, at the output of C-TIA and slope of the triangle wave [48]:

$$\sigma(\Delta T) = \sqrt{6} v_{n,rms} / [2(V_{R+} - V_{R-}) f_{dir}] \tag{5-9}$$

and

$$v_{n,rms}^2 = v_{n,amp}^2 \left(1 + \frac{C_P}{C_F}\right)^2 \frac{\pi}{2} f_{p,loop} + v_{n,comp,rms}^2 \tag{5-10}$$

where $v_{n,amp}$ and $v_{n,comp,rms}$ is the input referred-voltage noise density of the amplifier in the C-TIA and the input-referred rms voltage noise of the two continuous-time comparator, respectively. In this design, the white noise is dominated in $v_{n,amp}$ when the $f_{p,loop}$ >1MHz is required for the proper I-to-F conversion. The input-referred current noise $i_{n,rms}$ is obtained by normalizing the DC gain of the C-TIA in one flipping period $T_{dir}/2$:

$$i_{n,rms} = \frac{C_F V_{n,rms}}{T_{dir}/2} = \frac{\sqrt{6} V_{n,rms}}{2V_R} i_{sig} \tag{5-11}$$

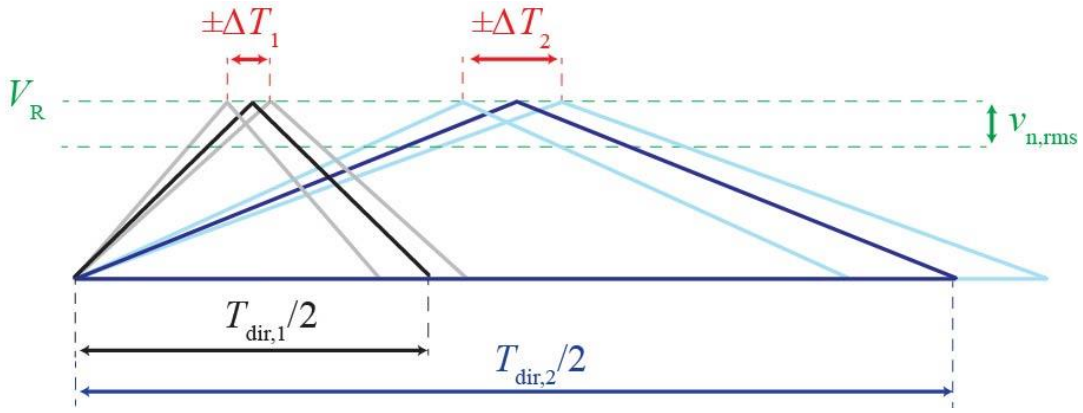

Figure 5.6: The output-referred voltage noise at the output of C-TIA causes the jitter of the triangle wave.

Interestingly, the ratio of input-referred current noise over the signal is constant and inversely proportional to the reference voltage V_R. The is because a white noise has a zero mean at the output of the C-TIA, and the Hourglass switch will not be triggered by the wide-band white noise without existing of a signal; once the output of C-TIA is approaching V_R, the jitter is proportional to the slope of the triangular waveform at v_o, which is also the linear relationship between input current and output frequency, e.g., a faster oscillating frequency generating a larger slope of the triangular wave thus more susceptive to any voltage noise to trigger the comparator. Once a flicker noise is considered in (5-9) to (5-11), this frequency dependent noise causes a long-term frequency drifting which is still a zero-mean value of the frequency change. Therefore, the flicker noise can be reduced by averaging the digital output, i.e., decreasing the bandwidth of a decimation filter after the ADC and limiting the signal bandwidth, when the flicker noise is larger than wide-band white noise in (5-10) in some design.

5.4.2 Noise in I-DAC

The noise from the I-DAC directly contributes to the system without any noise shaping or suppressing. current noise of this I-DAC is from the white noise and flicker noise of the tail current transistor.

$$i_{\mathrm{n,DAC}}^2 = \int \left(4kT\gamma g_{\mathrm{m}} f + \frac{g_m^2 K_f}{WLC_{\mathrm{ox}} f} \right) df \tag{5-12}$$

where k is Boltzmann's constant, T is the absolute temperature, γ and K_{f} is the white and flicker noise coefficient, respectively, W and L are the size of the current transistor, g_{m} is the transconductance, and C_{ox} and gate capacitance per unit of this transistor. The flicker noise contributes the major source when the signal bandwidth is around the frequency corner of the flicker noise while the white noise is first-order filtered by the C-TIA. The quantities analysis of this noise can be obtained using the same procedures in the Hourglass ADC by output-referring the current noise to a voltage noise at the output of the C-TIA and then input-referred as the equivalent current-noise using (5-9) and (5-11).

5.5 Implementation

5.5.1 System

The front-end was implemented in a 0.18µm CMOS process to obtain 160 dB DR, covering sub-pA to 10 µA current measurements. A fully-differential topology was designed to reduce common-mode noise with a matched sensor impedance at the differential input. The nominal supply voltage is 1.8 V and a common-mode voltage

of 0.9 V was used to maximize the output swing of the C-TIA while the reference voltages $V_{R\pm}$ were chosen to be 0.5 V and 1.3 V to minimize the noise per (5-9). A C_F of 100 fF was selected as a trade-off between the noise and conversion time in (5-3). A sensor capacitance up to 5 pF was assumed when considering the stability of the C-TIA and the noise of the AFE [15]. Stacked ESD diodes (4×) were used on all sensitive nodes to reduce leakage currents.

5.5.2 Power Optimization

The major power consumption of the Hourglass ADC is from the amplifier in the C-TIA when this power is calculated according to both the input range and the requirement *I*-to-*F* linearity. The power consumption of the amplifier is lower when the input range of the Hourglass ADC is smaller with more resolution, e.g., smaller LSB current, provided by the multi-bit I-DAC, but the noise from both the I-DAC and amplifier with a smaller tranconductance g_m contributes higher circuit noise in (5-9) and (5-11) and reduce the minimum detectable current of the AFE.

The optimization of the power is determined by both the calibrated *I*-to-*F* linearity and the total noise. When the transistor in a current source operates in the deep saturation region, the total noise from the multi-bit I-DAC is obtained in a SPICE simulation due to the non-linear relationship among the flicker noise coefficient K_f, transistor gate area, *WL*, and DC bias voltage V_{GS} and V_{DS} in the transistor model of BSIM v3.3. The optimized result shows the total noise of a 9-bit DAC generates 41 pA_{rms}. In this case, the input range of the Hourglass ADC is 20 nA when the full range

of the AFE is 10 μA while the noise is at the same order of the calibrated I-to-F linearity error of 40 pA. The I-DAC was implemented with 9-bit resolution and Hourglass ADC provided fine quantization with 8-bit linearity, so the total current noise from I-DAC is about half of the linearity error after *I*-to-*F* calibration.

5.5.3 *I*-to-*F* Linearity Calibration

The distortion of the *I*-to-*F* conversion can be compensated by measuring *I*-to-*F* error and reversely calculating these four variables with few discrete points. Thus, the I-DAC is used to sweep the transfer function of *I*-to-*F* conversion. By fitting these four variables from the coarse discrete point of the *I*-to-*F* curve, the current smaller than the LSB of the I-DAC on this curve from the output of the Hourglass ADC can be calibrated. The behavioral simulation result shows that using the 5-th order polynomial fitting can calibrate the linearity from 4 to 8 bit. The power efficiency of the system can be improved using the digital calibration when the bandwidth of the amplifier is reduced by 16×.

5.5.4 Amplifier

The amplifier was designed to obtain 8-bit linearity over the full input range with a gain > 80 dB to prevent the input from modulating the sensor output resistance R_p, which is usually larger than 1 GΩ. For an 8-bit linearity, the amplifier loop bandwidth must be at least 52× larger than the maximum f_{dir} (75 MHz). Rather than implement such a wide bandwidth, power hungry amplifier, the linearity is corrected

digitally using an amplifier with a bandwidth only 3.2× larger than the maximum f_{dir}. This approach results in 16× lower power compared to simply implementing a faster amplifier while ensuring 8-bit linearity.

A two-stage amplifier with a dual cascode compensation technique was implemented to further increase the power efficiency, extend the bandwidth, and to reduce the gain peaking beyond the unity-gain frequency [49, 60], as shown in Fig. 5.7. This compensation scheme increases the unity-gain frequency with 2-4× smaller compensation capacitance than the equivalent conventional Miller capacitor because both the non-dominant pole at the output of the second stage and right-hand plane zero in Fig. 5.7 are moved to a higher frequency. From simulation, this amplifier achieved a DC gain of 99 dB and a unity-gain bandwidth of 28 MHz. The stability of the C-TIA was simulated with a phase margin larger than 71° with the addition of the 5 pF sensor capacitance. The amplifier is auto-zeroed to minimize both the offset and the low-frequency noise of the amplifier [50], so the sensor modulated by the offset during the Hourglass switching was minimized.

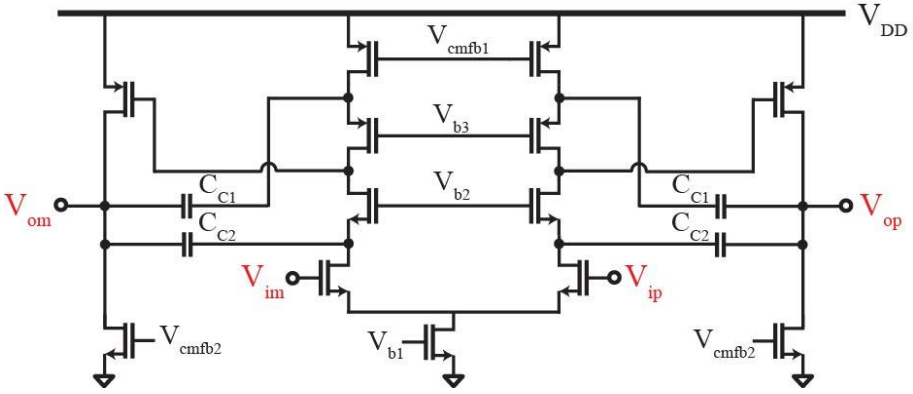

Figure 5.7: Schematic of dual cascode compensation amplifier.

5.5.5 I-DAC

The I-DAC needs to provide linearity greater than the entire AFE while minimizing the current noise and limiting the input capacitance, as in (5-10). The I-DAC was implemented using a tri-state topology [61]. Compared to a conventional I-DAC, all the unit cells are turned off when the input signal is smaller than the input range of the Hourglass ADC, so no noise is contributed from this I-DAC. In addition, this I-DAC is designed as fully segmented binary weighted to decrease the parasitic capacitance from the switches and routing. The total noise from the I-DAC was designed to be less than the linearity error from the Hourglass ADC as discussed in Section III B.

To minimize the total noise and maximize the output impedance of the I-DAC, the tail current is cascoded with two transistors which were biased in the deep saturation region. Sizing (W/L = 1 μm /10 μm) is used to further decrease the flicker noise and improve the matching. The linearity is guaranteed by randomizing the mismatch using a tree-structure, segmented DEM [62]. Each unit current is duplicated for this DEM technique.

5.5.6 Digital Blocks

Over-range detection of the predictor is required when the residual between input signal and I-DAC exceeds the predefined input range of the Hourglass ADC. This occurs with a step input or at the start-up of the AFE when the input of the predictor, i.e. the output of AFE, contains larger *I*-to-*F* non-linearity. The detection of this event was implemented by monitoring f_{dir}. Once f_{dir} is larger than the 250 kHz

(corresponding to a current of larger than 40 nA), the control block uses a binary search algorithm until f_{dir} is bounded below 250 kHz. This loop requires 9 oversampling cycles to settle and the the Hourglass ADC was designed to tolerate 2× LSBs of the I-DAC. All digital blocks, including the pulse counter, *I*-to-*F* linearity calibration, DEM, and the over-range detection, were implemented on an Opal Kelly XEM6310 FPGA for testing flexibility.

5.5 Measurement Results

This AFE was characterized with one of the inputs connected to a test source while the other was connected to a matched impedance network. To characterize less than 100 fA input current, the chip was measured using a Roger 4003C low leakage substrate and the input routes were guarded with traces at the same voltage V_{cm} as the inputs to reduce leakage through the PCB. A micrograph of the 1.5 × 2.0 mm^2 chip is shown in Fig. 5.8 where the AFE occupies an active area of only 0.5mm^2.

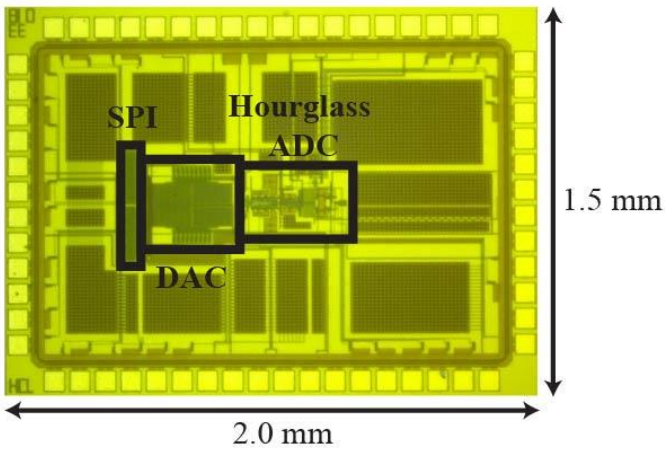

Figure 5.8: Die micrograph.

Figure 5.9(a) shows the measured *I*-to-*F* conversion of the Hourglass ADC. The linearity error in Fig. 5.9(b) was measured and improved from larger than 150 ppm to less than ±4 ppm after enabling the calibration where the fitted parameters, $A_{DC,closed\text{-}loop}$ = 64 dB and $f_{p,loop}$ = 1.5 MHz closely match the simulation results. The total leakage current of the setup and the AFE was 34.2 fA without an input signal. Fig. 5.10 shows a spectrum of the Hourglass ADC with f_{OSR} = 100 kHz illustrating the first order noise shaping, and an input-referred noise of 79 fA_{rms} was measured with the maximum available BW of $f_{dir}/2$. Note that out-of-band tones are the harmonics f_{dir}, as expected. The even order harmonics were introduced when the duty cycle of φ_{dir} was not exactly 50% which is caused by the unbalanced differential input current superimposed with the non-zero leakage current.

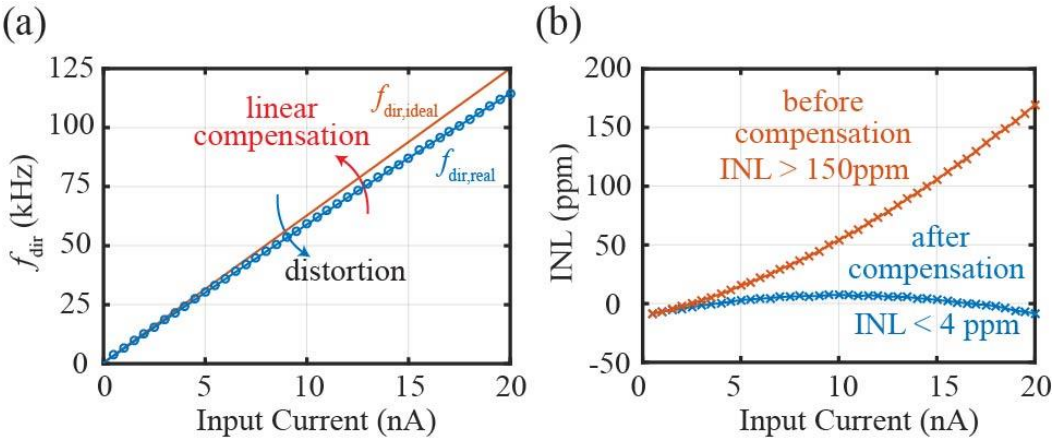

Figure 5.9: *I*-to-*F* conversion of the Hourglass ADC: (a) transfer function and (b) linearity error.

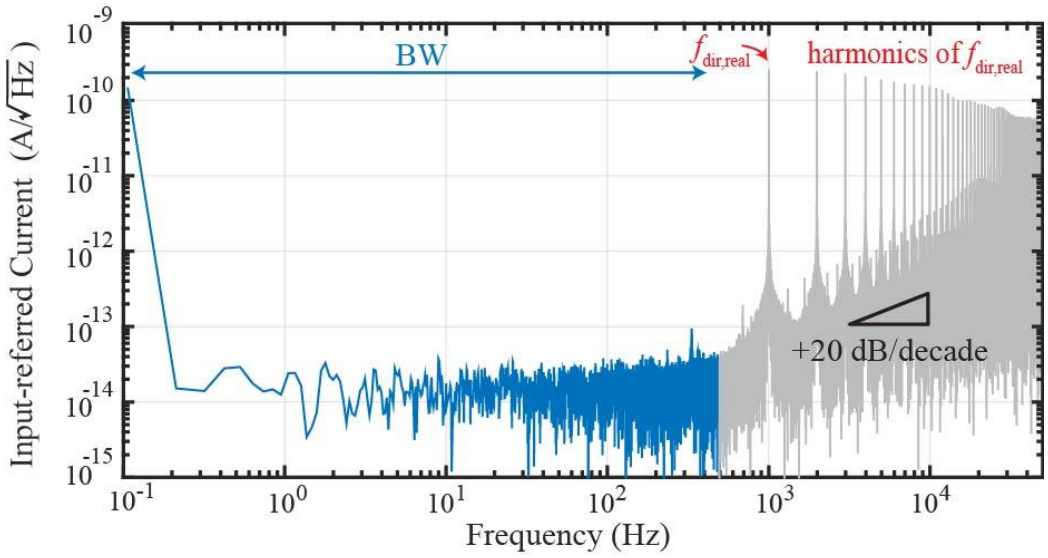

Figure 5.10: PSD of Hourglass ADC with a DC input.

The linearity of the AFE was measured when both Hourglass ADC and I-DAC

were on. A high precision current was provided using the equivalent Thevenin network and a low distortion voltage generator, Stanford Research Systems DS-360 measured using a Keithley 6430. Fig. 5.11 shows the full DR of the AFE as the current is swept from 100 fA to 10 μA covering the entire 160 dB with a measured linearity less than ±7 ppm.

This AFE consumes 295 μW with the amplifier consuming most of the power to provide the necessary bandwidth for *I*-to-*F* linearity. The synthesized digital logic consumes 8μW and was included in the total power consumption of the AFE as shown in Fig. 5.12.

Table 5.1 summarizes the AFE's performance in comparison to state-of-the-art current-input ADCs with similar DR and conversion time. The conversion time is faster than other works with a smaller design C_F while saturation of the C-TIA is prevented. The ADC achieves a Schreier FOM of 197 dB with a signal bandwidth of 1.8 Hz (Fig. 5.13). Note that the noise of this AFE is a non-sampled current noise and is dependent on the sensor model. The FOM exceeds that of a conventional voltage-input ADC where the FOM is limited by a sampled voltage noise, which is kT/C [63]. The FOM of the Hourglass ADC is -10dB/decade when the signal bandwidth increases by 10× because the minimum detectable signal increases by 10×, i.e., DR decreases by 20×, with the *I*-to-*F* relationship in (5-3), where the FOM of a conventional ADC is constant with a fixed DR when the minimum detectable signal is limited by a white noise.

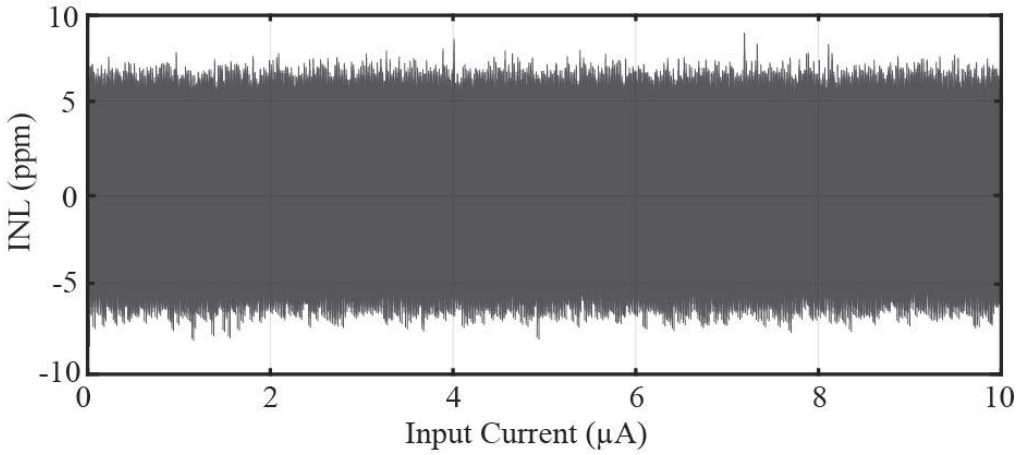

Figure 5.11: Linearity error of the AFE.

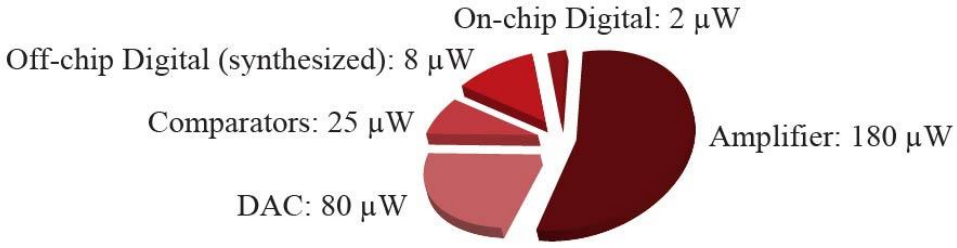

Figure 5.12: Power breakdown of the AFE.

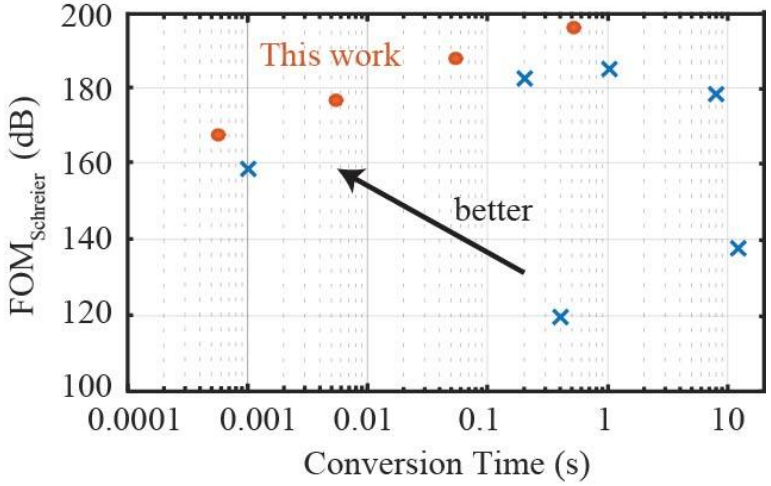

Figure 5.13: FOM of this work and state-of-the-arts.

Table 5.1: Performance Comparison.

Parameter	Stanacevic TBioCAS'07	Roham TBioCAS'08	Ahmadi TBioCAS'09	Sutula TCAS-I'14	Prabha JSSC'15	Dai TBioCAS'16	Li TBioCAS'16	Son TBioCAS'17	This Work
Architecture	SDM	SDM	Osc.	SDM	SDM	Osc.	C.C. + SDM	SDM	**SDM**
Tech. (µm)	0.5	0.5	0.18	2.5	0.18	0.18	0.5	0.18	**0.18**
Power (µW)	80	60	110	30	80	5,220	240	17	**295**
$I_{max,RMS}$ (µA)	1	0.43	1	32	4	11.6	16	3	**10**
$I_{min,RMS}$ (pA)	0.1	12	1,000	2,000	1,000	0.2	0.1	100	**0.1**
(NBW (Hz))	(N/A)	(100)	(N/A)	(1,000)	(N/A)	(100)	(1)	(1,000)	**(100)**
$T_{conv,max}$ (s)	8.0	10.0	1.0	2.0	0.4	0.25	1	0.004	**0.04**
$T_{conv,norm}$* (s)	8.0	1.2	> 10	> 10	> 10	0.5	50**	4	**0.4**
DR (dB)	140 @ < 0.1 Hz	91 @ <0.1 Hz	60	84	72 @ 2.5 Hz	155 @ 1.4 Hz	164 @ 1.0 Hz	88.9 @ 1 kHz	**100 @ 1.8 kHz** **120 @ 180 Hz** **140 @ 18 Hz** **160 @ 1.8 Hz**
$FOM_{Shreier}$ (dB)	172	132	90	120	103	181	183**	158	**167 @ 1.8 kHz** **177 @ 180 Hz** **187 @ 18 Hz** **197 @ 1.8 Hz**

5.6 Conclusion

This paper proposes a current measurement front-end using an asynchronous Hourglass ADC. The fundamental and analysis developed in this paper outlines the design trade-offs and explains the advantages of this current measurement front-end over conventional transimpedance amplifiers and synchronous sigma-delta modulators. Theoretical derivations were presented to show the advantages of the proposed architecture including the low-noise, increased input dynamic range, and continuous-time operation. Moreover, the I-DAC controlled by a first-order predictor relaxes the dynamic requirement of the Hourglass ADC as well as improves the power efficiency of the AFE. The linearity calibration and dynamic element matching provides the necessary linearity of the AFE. Such advantages are very beneficial for the design of low-noise, high dynamic range, low-power current-mode ADC.

An experimental prototype demonstrates the ability of a 160 dB dynamic range of currents that span from sub-picoamperes to tens-microamperes. This prototype of the proposed front-end achieves a state-of-the-art performance: linearity error less than 7 ppm, Shreier FOM of 197 dB, and 5× faster conversion time for 1nA current, which are often difficult to achieve in conventional current measurement front-end architectures.

Portions of this chapter contains both a reprint of the material and currently being prepared for submission for publication of the materiel as it appears in IEEE ISSCC 2018. A Current Measurement Front-end with 160dB Dynamic Range and 7

ppm INL. IEEE International Solid-State Circuits Conference (ISSCC). The dissertation author was the first author of this paper.

Chapter 6

Summary

6.1 Summary of Dissertation

This dissertation described improvements in current measurement front-ends for biosensing applications. I achieved the primary goal of this research, which was to investigate and design ultra-low noise readout circuits for high sensitivity biosensors. Here, I briefly revisit some of the key results and significant contributions of this work.

Chapter 1 oriented the reader by providing a background of biosensing and described how the research trends have been enabled in this space. The general concepts in biosensors and a survey of biosensors were presented. Chapter 2 presented a survey of different current measurement front-ends and a brief analysis of the performance and design trade-offs.

The following chapters described the designs of several ultra-low noise current measurement front-ends. In chapter 3, I described a wide flat-gain bandwidth TIA for next-generation nanopore-based DNA sequencing technique. The key contributions here are the new readout architecture based on a C-TIA to achieve low noise design while the hybrid semi-digital DC feedback loop provides a precise control of the transfer function and a low area implementation in digital domain. Also, a fast step response of the architecture is designed specifically to increase the sequencing efficiency for the short settling time when the DNA translocation occurs. This design was demonstrated to capture the DNA translocation events in a wild-type natural nanopore. This design was published in the special issue of the IEEE Transaction on Biomedical Circuit and Systems (TBioCAS) by invitation.

In Chapter 4, I explored a completely new current-input analog-to-digital converter, an Hourglass ADC, where the input current is directly used to control an oscillator. This work is substantial in that it allows amplifying a wide dynamic range input current while not being limited by the power supply voltage. This design also allows continuous-time operation and provides asynchronous control to obtain first-order noise-shaping. Chapter 5 further achieved high linearity with the calibration technique and closed-loop operation. The performance of this closed-loop Hourglass ADC achieved state-of-the-art. All the current measurement front-ends achieve the key abilities of ultra-low noise and high dynamic range to monitor the high sensitivity biological events in real-time allowing one to study the properties of biological reactions.

6.2 Areas for Future Work

The front-ends presented in this dissertation could be expanded in many ways. In the readout circuit for nanopore-based DNA sequencing, the design could be migrated from a discrete component on a printed circuit board to a fully integrated circuit. A solid-state nanopore can be also implemented on the same silicon chip [33, 64]. I believe the presented front-end can achieve a higher flat-gain bandwidth and a lower input-referred current noise when the parasitic capacitances from interconnections between nanopore and circuit and between each circuit component are reduced significantly. This enables scientists an opportunity to understand the physical and kinetic behaviors of DNA translocation in a nanopore as well as to achieve a low-cost next generation DNA sequencing technology.

The Hourglass ADC shows a lot of promise but is the most premature sensor interface presented. To be used in a system without significant human intervention, a compensation technique needs to be developed that automatically tunes the modulator for the variability in sensor impedance. This is not unrealistic and is frequently done in CT ΣΔ modulators today.

For the integrated design, I would be more aggressive in the future and explore different techniques to further improve the performance. For example, to improve the resolution as well as reduce the quantization noise of the open-loop Hourglass ADC with an implementation of a multi-bit, discrete-time quantizer in conjunction with the two continuous-time comparators. The other opportunity to improve the sensitivity of

the Hourglass ADC is utilizing chopper stabilization to sufficiently reduce the 1/*f* noise from the I-DAC in the feedback loop and decrease the size of the devices needed.

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