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DEVELOPMENTS IN LINEAR INTEGRATED CIRCUITS

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SUMMARY

The paper reviews recent developments of monolithic linear integrated circuits. Attention is given to operational amplifiers, voltage comparators and voltage regulators. Other developments including the monolithic four-quadrant analog multiplier and the phase-locked loop are also described.

INTRODUCTION

This paper is intended as a survey of recent developments in analog integrated circuits. The survey is limited to monolithic integrated circuits, where the functional block is contained in a single silicon chip. This leaves out hybrid circuits, here more than one silicon chip is mounted on a single header and interconnections are subsequently made. It is not the intent to describe applications for these integrated circuits, but rather to describe the circuits themselves, their characteristics, and perhaps their advantages or disadvantages.

The range of analog circuits now being produced in quantity by the integrated circuit manufacturers includes the linear circuits such as audio power amplifiers, RF and IF amplifiers, video and wideband amplifiers, sense amplifiers and operational amplifiers. Also being manufactured are voltage comparators, voltage regulators and the more recently announced analog multipliers and the phase-locked loop circuits. Digital-to-analog converters are also now becoming available as monolithic integrated circuits.

Component Parameters

Before describing the circuits it is well to first review some of the limitations that restrict the designer of a linear integrated circuit.

With passive components his greatest restriction is the virtual lack of reactive components. Inductors can be processed as an IC component--as a flat conductive spiral--but they occupy a large area, have a low value of inductance, and a low Q. They are therefore, generally unavailable to the IC designer. The situation with capacitors is only a little better. A monolithic capacitor has silicon dioxide as the dielectric and a minimum thickness of 1000Å is required to prevent pin holes and shorts in the insulating medium. Thus the area of a 25 pF capacitor is about 100 sq. mils. A transistor will occupy an area of 5 sq. mils. The large amount of surface area taken by the capacitor serves as a limitation to the IC designer. The choice of resistance values is almost unlimited. Resistance values in the range 50 Ω to 1 KΩ can be fabricated at the same time as the emitter is processed, while those in the 500 Ω to 10 KΩ can be made along with the base diffusion. Where larger values of resistance are required, the output resistance of a transistor in the common-emitter configuration can be utilized. Values to 100 KΩ are then possible.

Mention should also be made of a valuable characteristic of resistors fabricated by the diffusion process. Errors in etching, doping and diffusing all contribute to the absolute value of the resistor being only within ± 20% of the design center value. However,

these errors are common to all similar resistors on the wafer. Therefore the relative error between resistors on the same wafer can be as low as 2%. Additionally all resistors on a wafer will have the same temperature coefficient.

It is usual in fabricating linear IC's to start with a p-type silicon wafer upon which an n-type layer has been epitaxially grown. At selected areas an isolation diffusion of p-type material is then made through the epitaxial layer to yield isolated islands of n-type silicon surrounded by p-type. A circuit component is fabricated within each of these islands. Linear IC's predominently make use of vertically diffused NPN transistors. That is, the base is diffused into an area of the collector region followed by an emitter diffusion into the base region. The collector is the n-type epitaxial material. Where PNP transistors are required, they are generally fabricated in a lateral fashion along the surface of the silicon wafer. The epitaxial layer is now the base region. Typical parameter values for these two types of transistors are shown below.

	NPN	PNP
β	50 - 200	2 - 20
f_T	~600 MHz	~5 MHz

The characteristics of an integrated NPN transistor are similar to a general purpose discrete device, except for the value of the collector bulk resistance ($r_{c'}$). This is a resistance in series with the

collector junction. With a discrete transistor a back or bottom connection is made to the collector with a resulting low value for $r_{c'}$ of about 10 to 20 Ω. However, with integrated transistors the connection to the collector must be from the top, requiring a narrower conducting path and increasing the collector series resistance. This resistance along with the collector-substrate capacitance is a serious limitation in the design of wideband integrated amplifiers.

The long base region of the lateral PNP transistors decreases both the β and the f_T of these transistors. For low frequency amplifiers (< 1 MHz) the PNP transistors are useful for voltage level shifting between NPN transistor stages. The lack of capacitors requires a dc connection through the amplifier. For designs greater than 10 MHz, the designer is restricted to NPN transistors only.

Operational Amplifiers

Predominant in the linear IC field is the operational amplifier. The ideal operational amplifier has been described as having infinite gain, infinite input impedance, zero output impedance and having infinite bandwidth. Unfortunately, the cost would also be infinite.

Basic to the input of all monolithic operational amplifiers is the emitter-coupled differential pair (this is shown in Fig. 1 using bipolar transistors). The circuit requires close matching of all characteristics of both transistors and resistors over a wide temperature range, 0 to 70°C or possibly -55 to + 125 °C. This is an ideal situation for an integrated circuit. Also a large current gain is required of the

transistors to minimize the effect of loading at the input to the amplifier. Large valued resistors are also required to realize a large voltage gain for the input stage. Ideally the characteristics of the two transistors are exactly the same, as are the characteristics of the two resistors. Then considering the dc situation, with both inputs at ground potential there are equal currents in each transistor. The collector voltages are both the same and the differential output voltage is zero. However, the situation is not quite ideal. There are differences in the characteristics of the transistors which result in an input offset voltage and an input offset current. The current gain of the transistor is finite and so are the input bias currents.

The infinite input impedance would require zero offset voltage and zero input current. Recent developments in the design of monolithic operational amplifiers has been largely directed to obtaining these input characteristics. Generally there have been three approaches to the problem. They are the Darlington input stage using bipolar transistors, the field effect transistor (FET) input[1] and the use of super-beta transistors[2,3] in the input stage.

The Darlington input, using conventional transistors, is shown in Fig. 2. The input bias currents are reduced by a factor of $(\beta + 1)$ compared to the base currents of Q3 and Q4. This allows for input bias currents in the 10 to 100 nA range, but the input offset voltage is twice that of a simple differential pair. The drift of the offset voltage is also increased by a factor of two. In this design the Darlington input gives an effective current gain for the input stage of

more than β^2--where β is the current gain of just one transistor. The transistor Q8 is used as a source of current for the differential pair. The biasing of Q8 by Q9 is standard with IC's and tends to set a current for the differential pair independant of the β of Q8. The PNP transistor, Q5 and Q6, serve as active collector loads for the input transistors.

The high input resistance of an FET would seem to indicate its natural selection for the input stage of an operational amplifier. However, it has been shown[4] that for the same geometrical tolerances the input offset voltage and voltage drift are much greater for an FET differential pair than they are for a bipolar transistor pair. Where very low input currents are a necessity, there is now available a monolithic FET input operational amplifier and this is shown in Fig. 3. The input transistors are p-channel junction FET's, which are fabricated in the n-type epitaxial layer of the IC in a manner similar to an NPN transistor. An additional diffusion is necessary to form the high resistivity p-channel region. For this amplifier the current source for the FET's is from the PNP transistor Q6 which is biased by Q7. Transistors Q3 and Q4 are the active loads for the input transistors.

Over the industrial temperature range of 0 to 70°C, input bias currents of 100 pA are obtained by using an FET input stage. However, the FET does require some voltage between the drain and the gate which leads to leakage current problems as the ambient temperature is increased. This leakage current approximately doubles for each 10°C rise in temperature, so that extending their use to the maximum military temperature of +125°C leads to input currents in the 10 nA area.

The use of the super-beta transistor in the input stage of IC operational amplifiers has yielded input characteristics for the monolithic devices that are comparable to, or better than those for the discrete types. Incorporating the super-beta transistor means adding another diffusion cycle in the fabrication of the integrated circuit. In this process step, the emitter is diffused almost all the way through the base region to the collector. This makes for a very narrow base region yielding transistors with very high β, even at very low collector currents. Current gains of 5000 are typical at collector currents of 0.5 μA. The very narrow base region, however, means the emitter almost touches the collector and the breakdown voltage from collector to emitter is rather low, less than four volts. In the example shown in Fig. 4, the super-beta transistors Q1 and Q2 are operated in cascode with the conventional transistors Q5 and Q6. The bases of Q5 and Q6 are bootstrapped to the emitter of Q1 and Q2 through Q3 and Q4 so that the input transistors are operated with near zero collector-base voltage. The conventional transistors Q5 and Q6, with collector breakdown voltages of 25 V, stand off the common mode input voltage. With no voltage across the collector-base junction. leakage current in the input transistor is effectively eliminated. The differential output voltage is obtained from the collectors of Q5 and Q6 with Q7 and Q8 serving as active loads for those transistors.

The input characteristic of the three circuits are compared along with a standard operational amplifier in Fig. 5. The lowest input bias current and offset current is obtained with the FET input. But this

circuit also has the highest offset voltage and offset voltage drift. The lowest input offset voltage is obtained with the super-beta input of the LM108, but this unit also has the lowest slew rate which is indicative of low operating currents in the input stage of the amplifier. Notice also that the LM108 has the lowest power dissipation. The open loop voltage gain of all amplifiers should be considered adequate (the MC1531 is only included for comparison of the input stage characteristics).

A possible drawback in the use of monolithic operational amplifiers is the small bandwidth and slew rates. There is a definite relationship between these two, and one limit is due to the f_T of the lateral PNP transistors which are used in the signal path. An improvement in the performance of these transistors has recently been reported.[5] As shown in Fig. 6, two extra base contacts are used, with a small dc voltage (1 to 3 V) applied between them, to cause an aiding electric field to appear between the emitter and collector. Measurements have shown over an order of magnitude increase for the f_T and β of these transistors when compared with a conventional lateral transistor. That is f_T's of 300 MHz and β's of 100 have been reported. The slew rate is further limited by the current available to change the voltage across capacitors, both internal and external to the amplifier. Operating super-beta transistors at higher currents and the development of the improved PNP transistors should yield an operational amplifier with a unity gain bandwidth of 200 MHz and slew rate of 200 V/μs.

Another limitation in the use of operational amplifiers has been the problem of frequency compensation. Unrestricted use of negative feedback around an uncompensated amplifier can lead to disastrous oscillations. At some frequency the phase angle at the output of the open-loop amplifier will be greater than 180°. Now with simple negative feedback if the loop gain (from the amplifier input to the output of the feedback network) is greater than one at this frequency, oscillation will result. With a 180° phase change due to the negative feedback, the additional 180° phase angle will result in positive feedback at this frequency--an unstable situation.

Some of the more recently developed IC operational amplifiers have internal frequency compensation. That is the roll-off of the open-loop gain, with increasing frequency, is at -6 dB/octave through the unity gain point. This is the response of a simple single RC network. For this case, where the gain is greater than one, the phase angle at the output is never greater than 90°. Then, even with 100% negative feedback, the amplifier--as a voltage follower or unity gain stage--is unconditionally stable. However, wider bandwidths and greater slew rates are generally possible with the uncompensated amplifiers. These amplifiers, with frequency compenstaion terminals available, do allow for closer matching of the operational amplifier to its application.

An area which is currently receiving much attention is the development of micro-power operational amplifiers. These amplifiers have an open-loop voltage gain to 20,000 and input characteristics similar to those that have already been described. But, total power consumption

is less than 200 μw. Their use, however, is limited to dc, or low-frequency applications. Continued improvements will be in greater gain at lower power consumption.

Another area of development for the operational amplifiers is the low-noise amplifier. Though improvements in the noise performance of the amplifier are inherent in the low-current input stages, work continues in this area. Here again the emphasis is on low-frequency applications.

Voltage Comparators

The emitter-coupled differential pair has other useful properties beside its use in the input stage of the operational amplifier. The configuration is particularly useful as a voltage comparator stage--one input is connected to the reference or bias voltage, the other the actual signal input. Followed by an amplifier with sufficient gain, the integrated device makes an excellent amplitude discriminator. Commonly used as sense amplifiers with magnetic core memory units, these devices have minimum input threshold voltages of less than 5 mV with output voltage levels which are compatible with digital integrated circuits. Temperature compensation is inherent in the design and the differential input voltage temperature coefficient is typically 5 to 10 μV per °C. The propagation delay times are about 20 ns with comparable rise and fall times. The maximum input bias current of these sense amplifiers is about 10 μA, with the offset current about one-tenth this value. Their application is therefore restricted to where

a low-input resistance is possible. A voltage comparator is now available with a maximum input bias current of 100 nA and offset current of 10 nA, but the response time is 200 ns.

Voltage Regulators

Following the operational amplifier and the voltage comparator, the device which has received the most attention from the IC manufacturer is the voltage regulator. A second generation of monolithic voltage regulators is now becoming available.[6] The new devices have higher output current ratings (to 1.5 A) and require fewer external components and adjustments. Currently 5 W can be handled in a conventional power package. The trend will probably be towards a fixed output voltage for the high current regulators, + 5 V at 1 A for digital IC applications; with some small variation in the output voltage for regulators used with linear IC's (maybe 9 to 15 V with current ratings of 200 milliamps). With a standardizing of voltage and current ratings there will be an accompaning reduction in price.

Analog Multipliers

The assets of the monolithic emitter-coupled differential pair are further exploited in the design of the four-quadrant analog multiplier.[7,8] A basic schematic of the circuit is shown in Fig. 7. Initially, the analog voltages X and Y are converted to small signal currents I_x and I_y by the large resistors R_X and R_Y in the emitter-

coupled pairs Q1 and Q2, Q7 and Q8. A differential voltage is obtained across diodes D1 and D2 in the collector circuit of Q1 and Q2 respectively. This voltage, V_d is related to the logarithm of the signal current I_x. Now the voltage V_d is used to control the flow of the signal current I_y in the two emitter-coupled pairs Q3 and Q4, Q5 and Q6. Finally the currents are summed at the collectors of these transistors and a differential output voltage, V_{d_o}, is obtained, that is directly related to the product of the input voltages X and Y. A requirement of the linear multiplier is the close matching of the characteristics of the three emitter-coupled pairs and the diodes D1 and D2. This is a basic property of the monolithic integrated circuit.

With the multiplier, analog signals may be multiplied, divided, squared or square roots may be obtained. Other possible uses of the device are as a phase detector, a frequency doubler or as a balanced modulator or demodulator element. These and other possible applications of the multiplier are described in Ref. #8.

The only presently available monolithic four-quadrant multiplier accepts input voltage of ± 10 V and has a linearity of better than 1%. There are also many adjustments which have to be made before the device can be effectively used. However, a new version of the multiplier will shortly be available which will have an improved linearity (0.2%) with the same output voltage swing (± 10 V), but requiring fewer external adjustments.

Phase-Locked Loop

The problem of fabricating integrated circuits requiring tuned circuits, consisting of inductors and capacitors, has been avoided with the introduction of the phase-locked loop.[9] The phase-locked loop is a complete monolithic IC which is able to perform many of the functions usually regarded as requiring tuned circuits.

As shown in Fig. 8, the phase-locked loop is basically a servo system in which the output of a voltage-controlled oscillator (VCO) is made to track with an incoming signal. When the input and VCO frequencies are the same, the system is in lock. Any change of frequency by the input signal or the VCO is detected by the phase comparator and a dc correction voltage is applied to the VCO to bring the system into lock. The low-pass filter sets a limit on the maximum allowable difference frequency and still have the system lock.

Generally the phase comparator is a variation of the analog multiplier already described. The VCO is typically a non-saturating emitter-coupled multivibrator. The correction voltage controls the charging and discharging of the coupling capacitor. The low-pass filter can be a simple RC integrator.

With a frequency-modulated (FM) input signal, the input to the VCO is proportional to the frequency deviation of the input signal. A FM demodulator is an immediate application of the phase-locked loop. In a similar manner the phase-locked loop can be used to extract information from noisy signals. Many other applications are now being suggested

for the phase-locked loop in communications, instrumentation and data processing. The typical phase-locked loop will operate with input signal amplitudes down to 100 μV at frequencies up to 30 MHz.

D/A Converters

Another development is the completely monolithic D/A converter. The aim is to have a complete package; switching circuits, resistor ladder network and output amplifier, all on a single chip.

At this time one manufacturer is marketing a 6-bit D/A converter that is a totally diffused device. However, tolorances for diffused resistors used in the ladder network will limit the accuracy, and 6-bits is about the maximum for such a device. A more promising approach is to fabricate the resistor network as a thin film resistive layer, deposited on the top of the SiO_2--the passivation surface of the silicon chip. Such a device is also currently available as an 8-bit D/A converter.

With many hybrid packages as competition to monolithic designs, the hope is to realize a product that is more reliable, and have a better temperature specification. The batch fabrication of such a device should also lead to a lower cost.

Other Developments

Perhaps the greatest activity of development with linear IC's is in the so-called consumer markets of entertainment and the automobile. Color television, stereo radio, controlled fuel injection and anti-skid devices are receiving full attention. This market will eventually dominate in volume the linear IC field.

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REFERENCES

1. G. R. Wilson, "A monolithic junction FET-NPN operational amplifier", IEEE J. Solid-State Circuits, Vol. SC-3, pp 341-348, December 1968.

2. R. J. Widlar, "Design techniques for monolithic operational amplifiers", IEEE J. Solid-State Circuits, Vol. SC-4, pp. 184-191, August 1969.

3. R. J. Widlar, "Designing with super-beta transistors op-amp IC's", EEE 17, No. 12, pp. 70-73, December 1969.

4. H. C. Lin, "Comparison of input offset voltage of differential amplifiers using bipolar transistors and field-effect transistors", IEEE J. Solid-State Circuits, Vol. SC-5, pp. 126-128, June 1970.

5. E. L. Long, "A 15-watt monolithic power amplifier", 1970 ISSCC Digest Tech. Papers, Vol. 13, pp. 108-109.

6. R. J. Widlar, "New developments in IC voltage regulators", 1970 ISSCC Digest Tech. Papers, Vol. 13, pp. 158-159.

7. B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response", IEEE J. Solid-State Circuits, Vol. SC-3, pp. 365-372, December 1968.

8. E. L. Renschler, "Theory and application of a linear four-quadrant monolithic multiplier", EEE 17, No. 5, pp. 60-67, May 1969.

9. A. B. Grebene and H. R. Camenzind, "Frequency-selective integrated circuits using phase-lock techniques", IEEE J. Solid-State Circuits, Vol. SC-4, pp. 216-224, August 1969.

FIGURE CAPTIONS

Fig. 1. Circuit Diagram of an emitter-coupled differential amplifier.

Fig. 2. The Darlington input stage.

Fig. 3. An FET input stage.

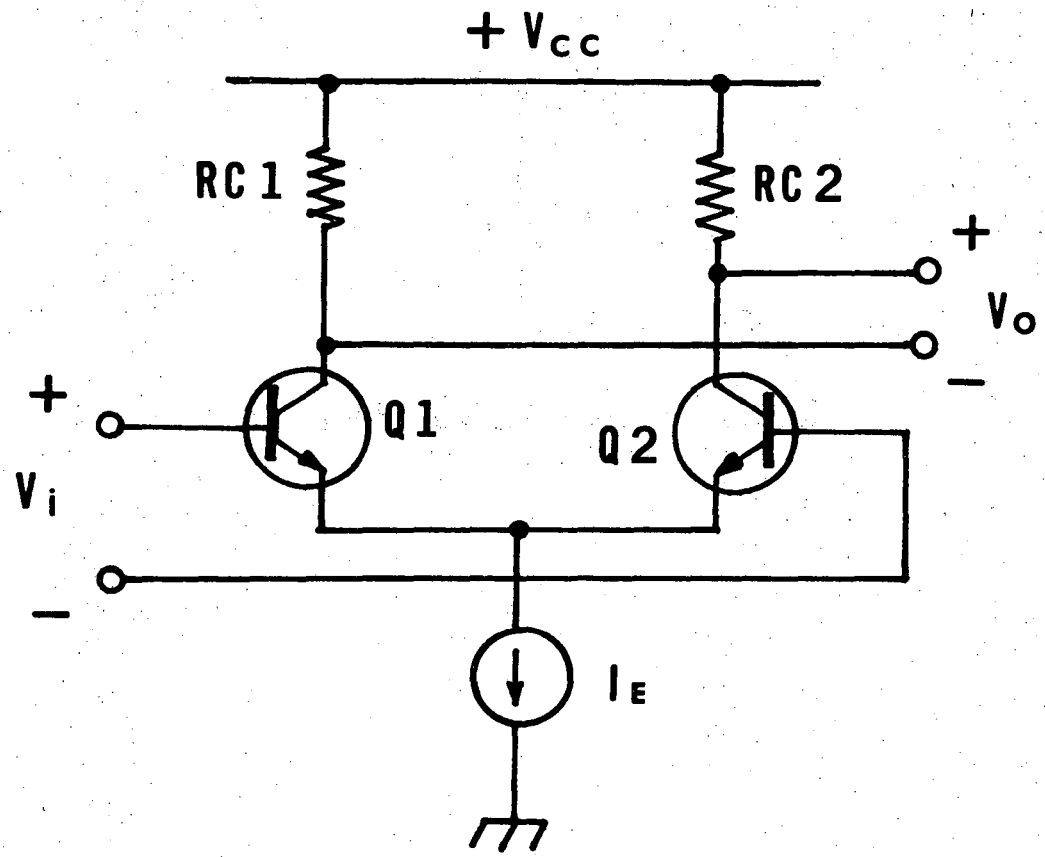
Fig. 4. A super-beta transistor input stage.

Fig. 5. A comparison of operational amplifier specifications.

Fig. 6. The field aided lateral PNP transistor.

Fig. 7. Basic circuit diagram of an analog multiplier.

Fig. 8. Block diagram of a phase-locked loop.



DIFFERENTIAL PAIR

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Fig. 1

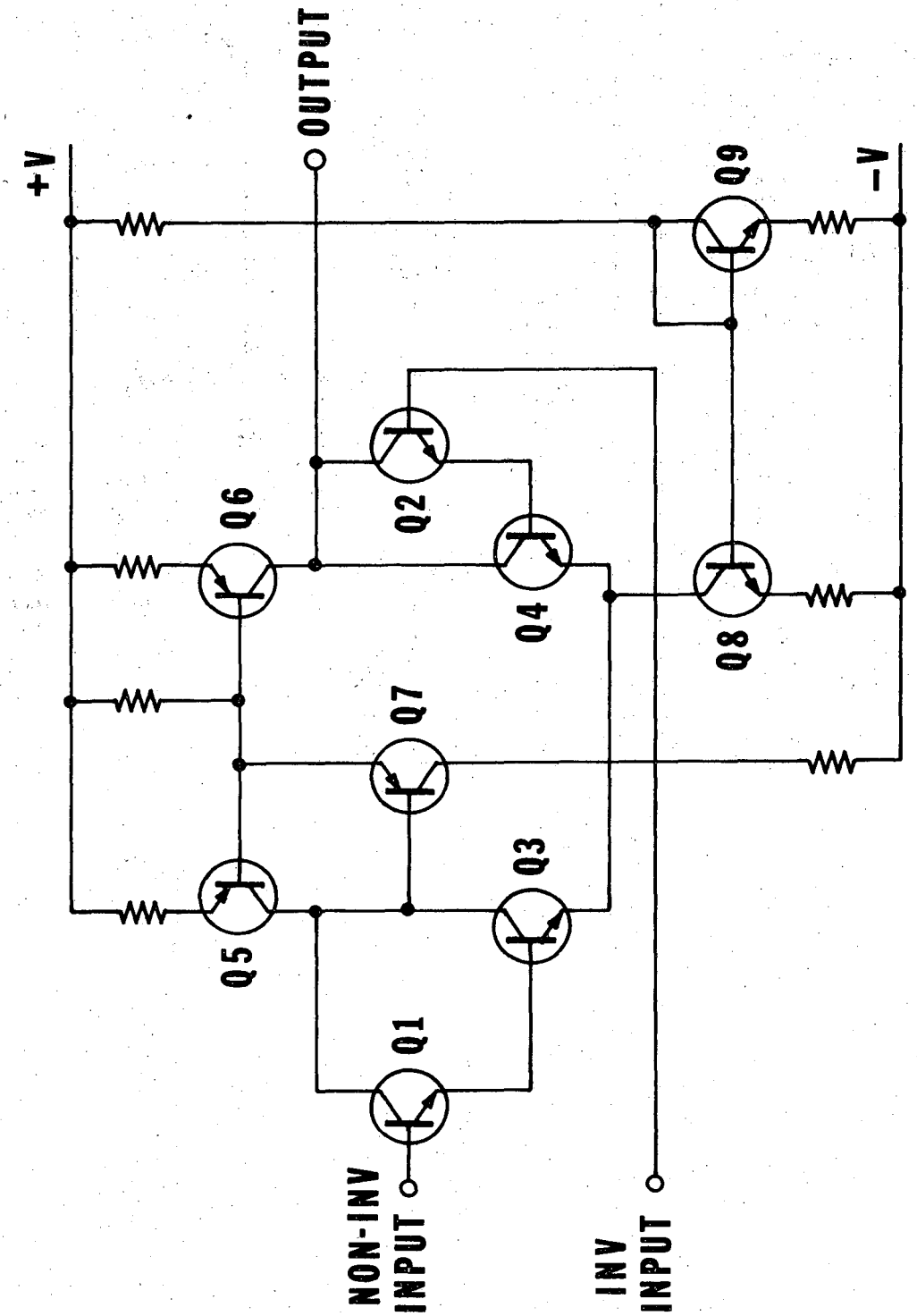
+V
OUTPUT
-V
Q9
Q2
Q6
Q4
Q8
Q7
Q3
Q5
Q1
NON-INV
INPUT
INV
INPUT
DARLINGTON INPUT
XBL 7010-6779

Fig. 2

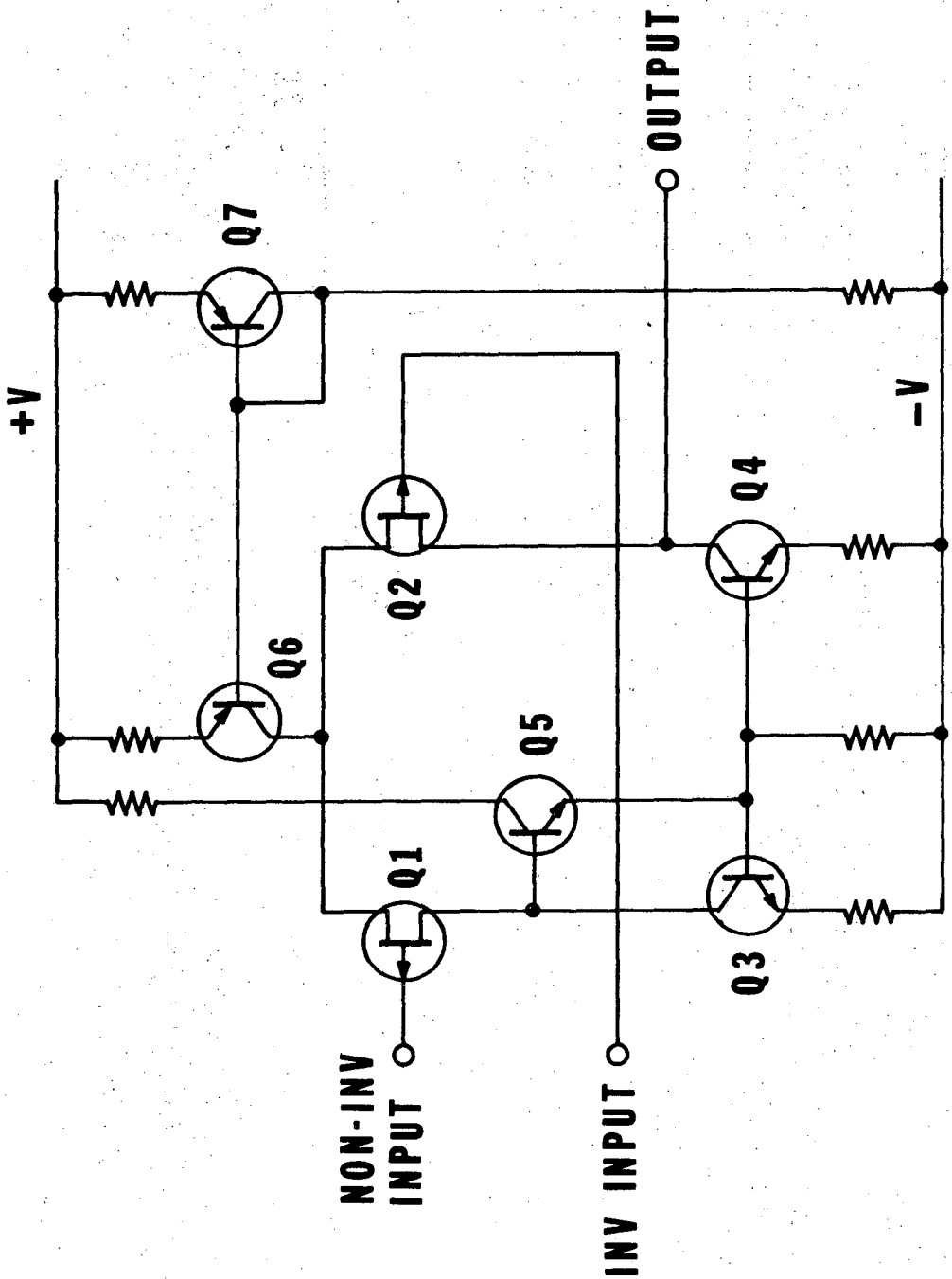

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Fig. 3

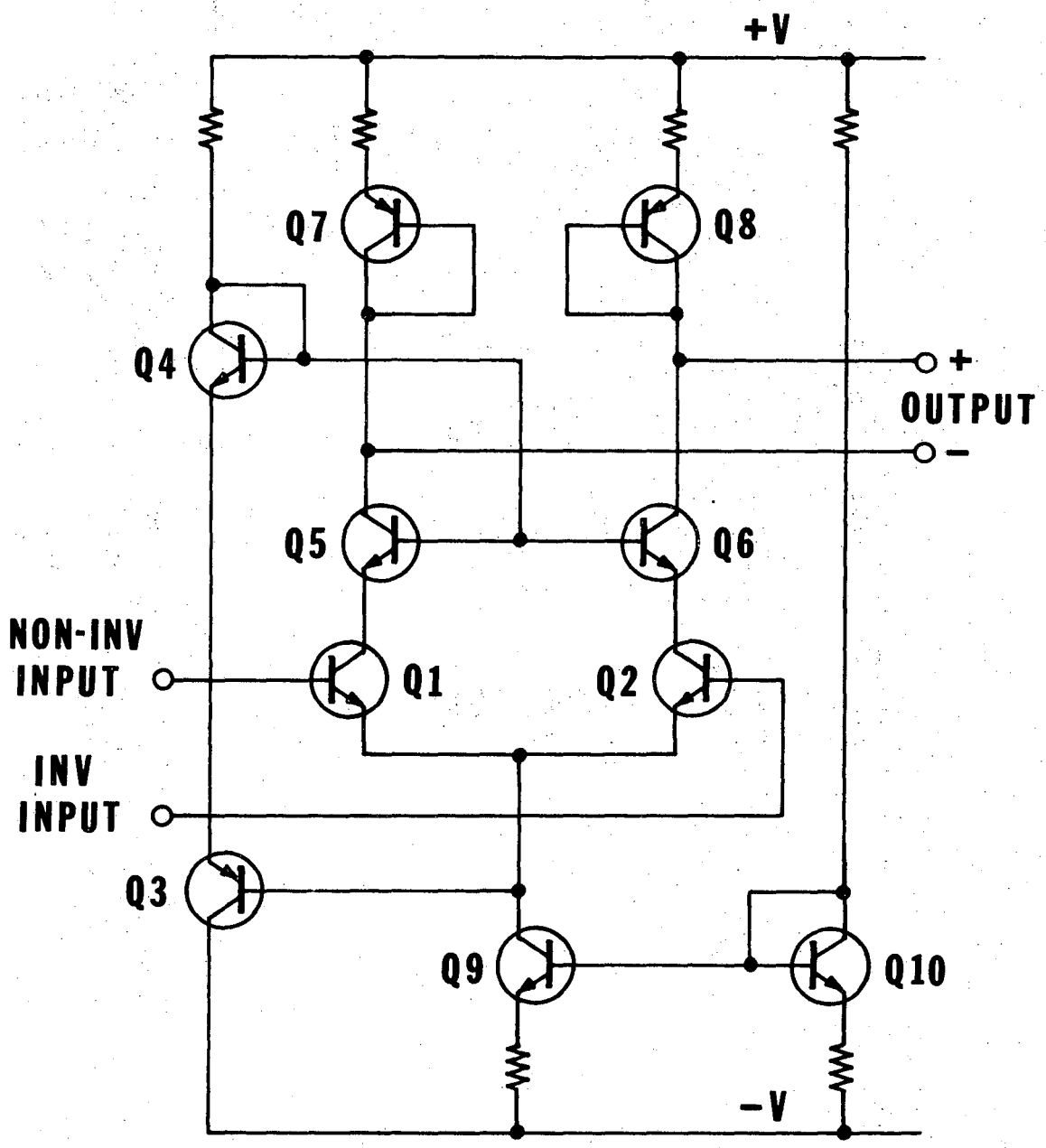
+V
Q7
Q8
Q4
+
OUTPUT
−
Q5
Q6
NON-INV
INPUT
Q1
Q2
INV
INPUT
Q3
Q9
Q10
−V
SUPER-BETA INPUT
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Fig. 4

COMPARISON OF OPERATIONAL AMPLIFIERS

	Standard μA741	Darlington MC1531	FET μA740	Super-Beta MC1556	Super-Beta LM108
T_A =25°C					
Input bias current — max	500nA	150nA	200pA	15nA	2.0nA
Input offset current — max	200nA	25nA	40pA	2.0nA	0.2nA
Input offset voltage — max	5.0mV	10mV	20mV	4.0mV	2.0mV
T.C. offset voltage — typ	6μV/°C	20μV/°C	50μV/°C	30μV/°C	15μV/°C
Open loop voltage gain — min	50,000	2,500	50,000	100,000	50,000
C.M.R. — min	70dB	60dB	64dB	80dB	85dB
Slew rate — typ	0.5V/μs	1V/μs	6V/μs	2.5V/μs	0.3V/μs
Output voltage swing — typ	±14V(10K)	±5V(5K)	± 13V(2K)	± 13V(2K)	± 14V(10K)
Supply voltage	±15V	±6V	± 15V	± 15V	± 15V
Power dissipation — max	85mW	150mW	156mW	45mW	12mW
Internal freq. compensation	Yes	No	Yes	Yes	No

Fig. 5

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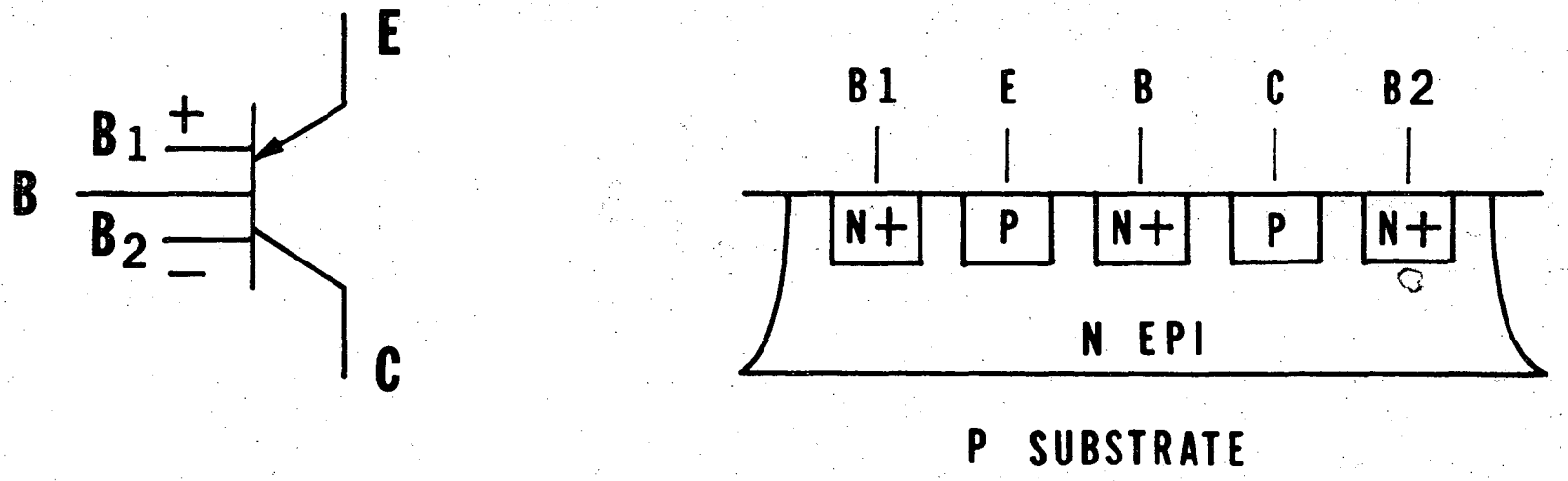

FIELD AIDED LATERAL PNP TRANSISTOR

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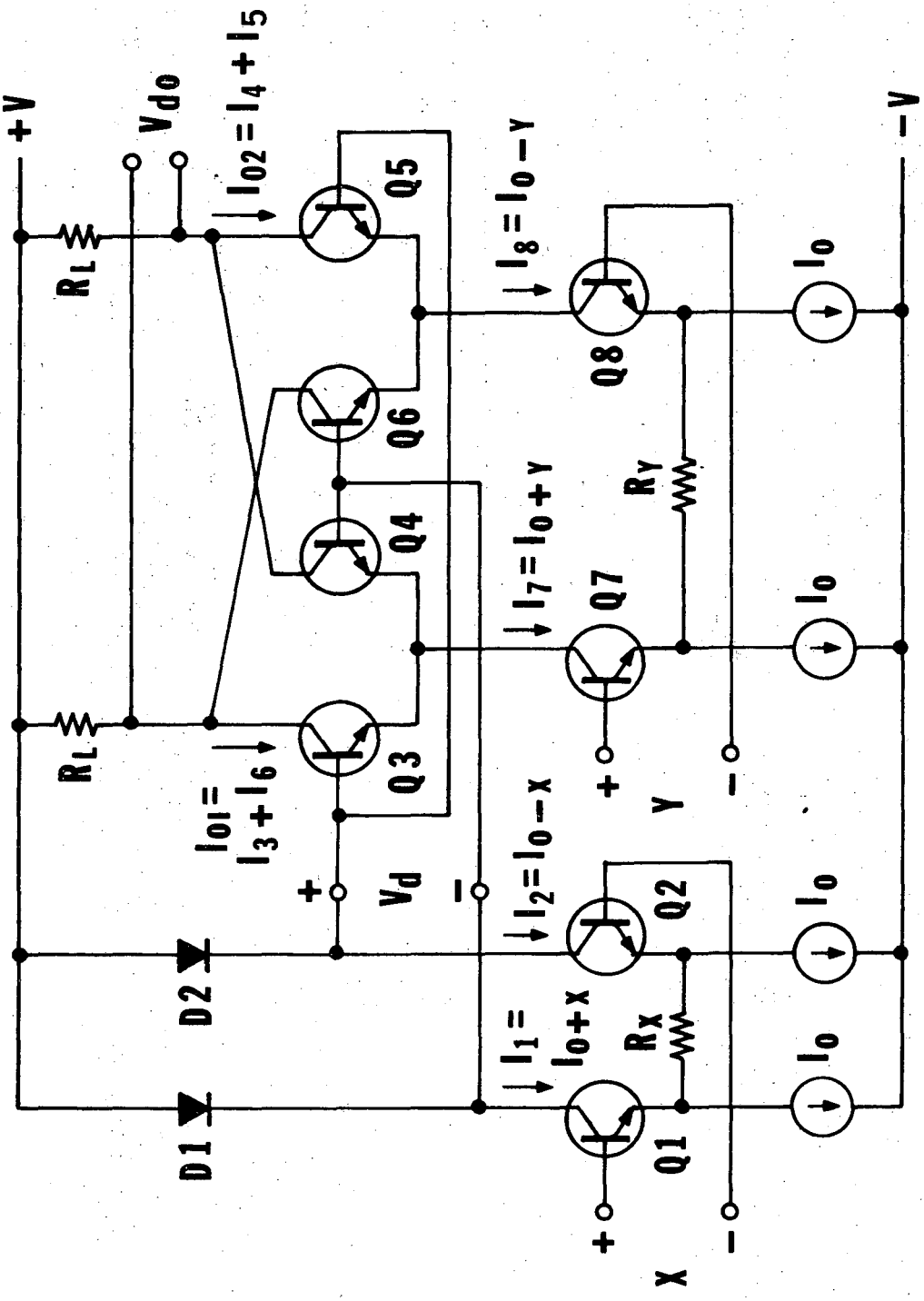
Fig. 6



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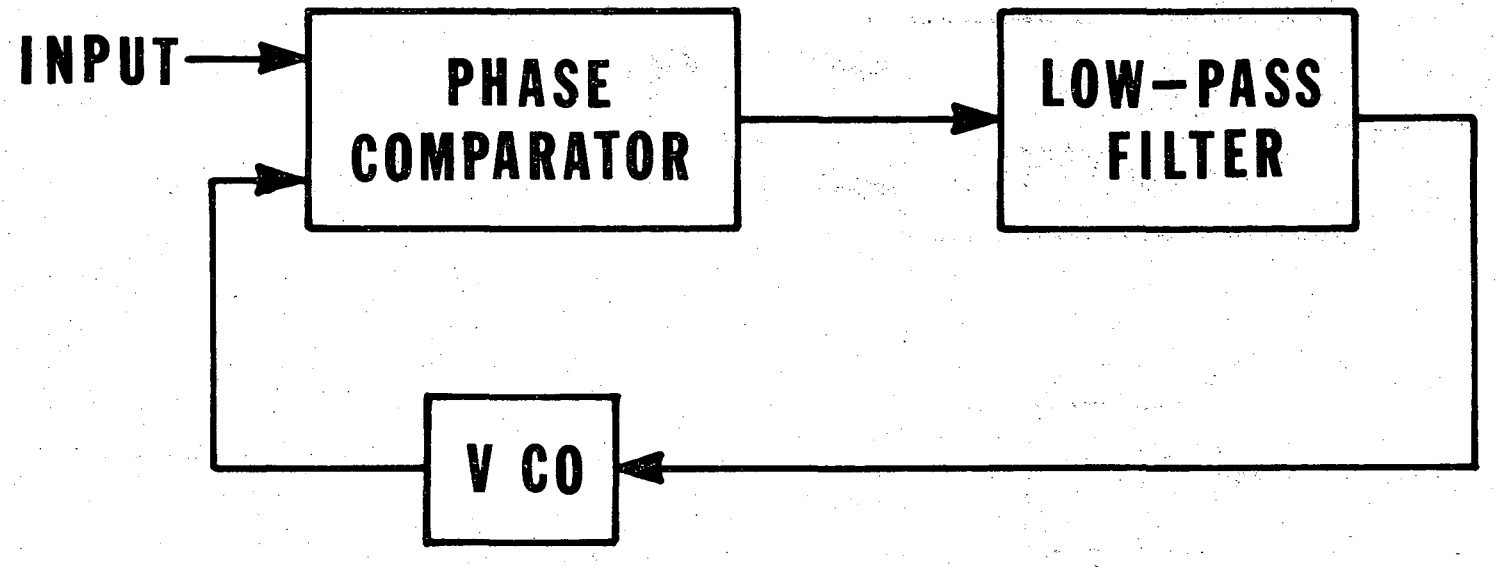
ANALOG MULTIPLIER

Fig. 7



PHASE-LOCKED LOOP

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Fig. 8

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