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Tunable Lasers with Ring-based Mirrors for Photonic Integrated Circuits on Heterogeneous Silicon-III/V

A dissertation submitted in partial satisfaction of

the requirements for the degree

Doctor of Philosophy in Electrical and Computer Engineering

by

Jared Hulme

Committee in charge:

Professor John E. Bowers, Chair

Professor Larry A. Coldren

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March 2017

The dissertation of Jared Hulme is approved.

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Professor John E. Bowers, Committee Chair

October 2016

Tunable Lasers with Ring based mirrors for Photonic Integrated Circuits on Hybrid Silicon

Jared Hulme

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Acknowledgements

It is no secret that graduate school can be a very challenging period of life. Between the frustrations of cleanroom processing and device testing, and the time spent on difficult homework and raising three children I often found myself thoroughly exhausted and stressed. However, I look back at this time as an incredibly rewarding experience that has stretched and bettered me. My thanks go out to the many people who have helped me through this process.

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Vita of Jared Hulme

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Abstract

Tunable Lasers with Ring-based Mirrors for Photonic Integrated Circuits on Heterogeneous Silicon-III/V

by

Jared Hulme

Semiconductor tunable diode lasers have applications in various fields such as spectroscopy, remote sensing, and fiber optic communications. They are used as the sources in wavelength division multiplexing (WDM) systems, as local oscillators in coherent detection schemes, and as a key component in various photonic integrated circuits (PIC). In recent years there has been increasing interest in hybrid silicon-III/V as a platform for photonics. Silicon processing has been well defined in CMOS fabrication facilities, has low waveguide loss at telecommunications wavelengths, and has the capability of being integrated closely with electronics. Combining silicon with active III/V materials, such as InP, allows a higher level of integration on a single chip. Additionally, new types of tunable lasers can be created that utilize the strengths of both materials. This work explores the design, fabrication and measurement of several ring-based tunable lasers and their application in two photonic integrated circuits.

The first PIC is the first fully integrated two-dimensional beam-steering chip. The tunable wavelength from the laser is utilized to change the angle of emission from an output surface grating array. The second dimension of tuning is controlled by an optical phased array. Coherent light is split into multiple channels with individually tuned phases which are

emitted from an array of surface gratings. By proper tuning of the phases an arbitrary beam angle can be formed from the interfering outputs of the array. Beam-steering from a fully-integrated chip is demonstrated over 23˚ x 3.6˚ with respective beam widths of 1˚ x 0.6˚, allowing for 138 resolvable points.

The second PIC is a tunable photonic microwave signal generator. This is created by heterodyning the output from two lasers on a fast photodetector and reading the beat tone at the frequency difference between them. The output frequency of the device can be shifted by tuning one of the laser sources relative to the other laser thus creating a tunable microwave source. The photodiode exhibits 65 GHz 3 dB bandwidth. Microwave signals from 1 to 112 GHz are demonstrated from a fully integrated PIC.

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Chapter 1

Introduction

In recent years there has been much discussion about and research into the field of heterogeneous silicon photonics. Silicon is an attractive medium for several reasons. First, silicon processing has been finely tuned over decades in large-scale fabrication facilities. The industry is mature and reliable. Silicon wafers 300 mm in diameter are now the standard, with 450 mm wafers currently being investigated as a possible next step. This allows for an industry of scale where cost per device is much lower due the sheer quantity of devices. Silicon, as a material, is also very inexpensive.

Second, silicon is attractive due to its optical properties. It boasts a wide band of infrared transparency (1.2 μm to 7.0 μm), and waveguide losses below 0.3 dB/cm have been reported over the C-band. The high index of refraction (around 3.5 depending on wavelength) allows for small guided bend radii which is useful for photonic integrated circuits (PIC). Other effects, such as two-photon absorption, Kerr-nonlinearities, and the Raman effect can be utilized in specific applications. Free-carriers can be introduced to both absorb light and

change the index of refraction. Silicon has a high heat conductance, and is also a strong material capable of withstanding fairly high levels of stress.

Third, silicon photonics has the potential to be monolithically integrated with CMOS circuitry, allowing for closer interconnects and reducing limitations on input/output pins.

However, monolithic silicon photonics lacks the ability to efficiently amplify light due to its indirect bandgap. III/V materials are far better suited to this. Indium phosphide (InP) is a common material choice for PICs. Based on the growth stack and processing, InP can efficiently amplify, modulate, and detect light. Devices can be operated at high speeds due to the high electron velocity. However, InP growth is expensive and wafer size is limited.

The heterogeneous silicon-III/V platform provides the benefits of both materials. Silicon waveguides allow for larger PICs, and higher levels of integration. Many photonic applications use several individually packaged photonic devices. There is loss in the transition from device to fiber and back to a new device, as well as the complexity in assembling separate pieces. By integrating all the devices onto a single chip the losses can be kept down and the packaged device made simpler to operate.

Trends of the level of complexity in photonic integrated circuits can be seen in Figure 1. The figure of merit shown is the number of components connected to a single waveguide in a photonic integrated circuit. Indium phosphide PICs have been growing steadily more complex over the past three decades. In a single decade, monolithic silicon photonics has already surpassed the number of integrated devices, and heterogeneous silicon-III/V is increasing even more rapidly.

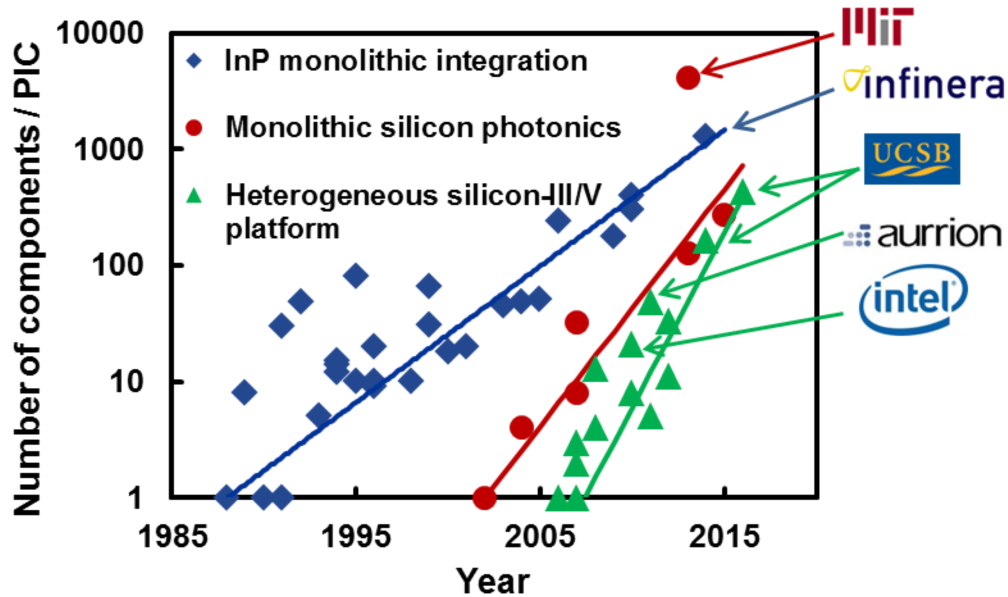

Figure 1. Plot showing the trend towards higher levels of integration in monolithic InP, monolithic silicon, and heterogeneous silicon-III/V.

It should be noted that the MIT result of over 4000 devices was a completely passive circuit and required no I/O other than an input laser. Integration of large numbers of active components is more difficult from a packaging and operation perspective. Eventually the number of I/O pins limits the ability to integrate further on a single chip, as it has with CMOS circuitry.

Another limitation in integrated heterogeneous silicon photonics is the lack of certain devices. For example, isolators on silicon have not been satisfactorily integrated with lasers. However, work is being done in this regard [2], and more types of integrated devices and materials can be expected in the future.

One of the most versatile components for photonic integrated circuits is the tunable laser. Heterogeneous silicon photonics offers a unique advantage for ring-based tunable lasers due to the long life-time in a resonant ring with low losses. This work explores the

design, fabrication, and testing of several ring-based tunable lasers on the heterogeneous silicon-III/V platform. Two fully integrated photonic integrated circuits which utilize these lasers are also presented: a two-dimensional beam-steering chip, and a photonic microwave generator chip. The final iteration of both of these PICs employ integrated lasers, phase modulators and photodiodes.

After this introduction, Chapter 2 explores ring-based tunable lasers. Chapter 3 describes the design and characterization of several phases of the beam-steering chip. Chapter 4 shows photonic microwave generators, with some emphasis on the high-speed photodiode used in conjunction with the lasers. Chapter 5 is a description of the semiconductor processing used to fabricate these chips. A conclusion is given, followed by appendices which describe processing recipes, III/V epitaxy layers, and detailed process followers used for various process runs.

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[6]

Chapter 2

Tunable lasers

Tunable lasers are key components for many applications, including spectroscopic measurements, variable sources for wavelength-division multiplexing (WDM) systems, in Light Detection and Ranging (LIDAR), beam-steering, photonic microwave generation, and many others. Through the use of adjustable optical filters the output wavelength can be changed to meet the different needs.

One approach for achieving wide tunability is to physically change the cavity dimensions. In the case of [1], a vertical cavity surface-emitting laser (VCSEL) has fixed bottom mirror and gain layers, but the top mirror is suspended on a membrane that moves with applied bias. The result is over 150 nm of continuous wavelength tuning. A similar design in [2] was used as an effective source in optical coherence tomography (OCT). However, for many applications a vertically emitting laser is not practical. A planar laser allows for integration with other on-chip components, which is one of the goals of this work.

Another common approach to tuning lasers is evident in the sampled-grating distributed feedback (SGDBR) laser. In this design the reflection spectrum of the two mirrors overlaps in a narrow region using the Vernier effect. By making small dynamic adjustments to one mirror via thermal heating, the selected wavelength can jump by several nanometers

The double-ring resonator approach for widely tunable lasers also utilizes the Vernier effect to allow for a wide tuning range. This idea was proposed by Liu et al. in [3]. It is particularly suited to the heterogeneous silicon-III/V platform because of the low loss in the silicon waveguides. Lower losses allow for improved performance in the rings and their ability to act as wavelength filters[4].

This chapter explores several ring-based tunable lasers on the heterogeneous platform[5].

2.1 Concepts

The silicon-III/V platform utilizes adiabatic coupling to transfer between the silicon waveguide and the bonded III/V gain sections [6]. A simulation of the mode profile is overlaid on an illustration of a gain region cross-section in Figure 2. The light is transferred from the silicon waveguide up into the III/V such that some percentage of the mode is confined in the quantum well region. After passing through the gain section the light is transferred back to the silicon waveguide layer that contains ring filters and mirrors.

The filters in these lasers utilize the Vernier principle that occurs when combining two rings of different circumference. As shown in Figure 3, the free spectral range (FSR) of the rings is sufficiently different to suppress all peaks but the one shared by the two rings. However, the other peaks are close enough that a small amount of tuning will shift the filter comb of one ring such that a different set of peaks will line up. Eventually there will be

another set of peaks that line up, but by using two rings with sufficiently similar circumferences the second overlap of the peaks will be outside the gain bandwidth, which acts as a broad filter.

The equation for free spectral range of a ring resonator is found in Equation 1 where λ is the wavelength, n_g is the group velocity (Equation 2), and L is the roundtrip length. By changing the effective index (n_{eff}) with thermal tuning, the FSR will change minutely and the whole ring comb will shift.

$$FSR = \frac{\lambda^2}{n_g L}$$ **Equation 1.**

$$n_g = n_{eff} - \lambda_0 \frac{dn_{eff}}{d\lambda}$$ **Equation 2.**

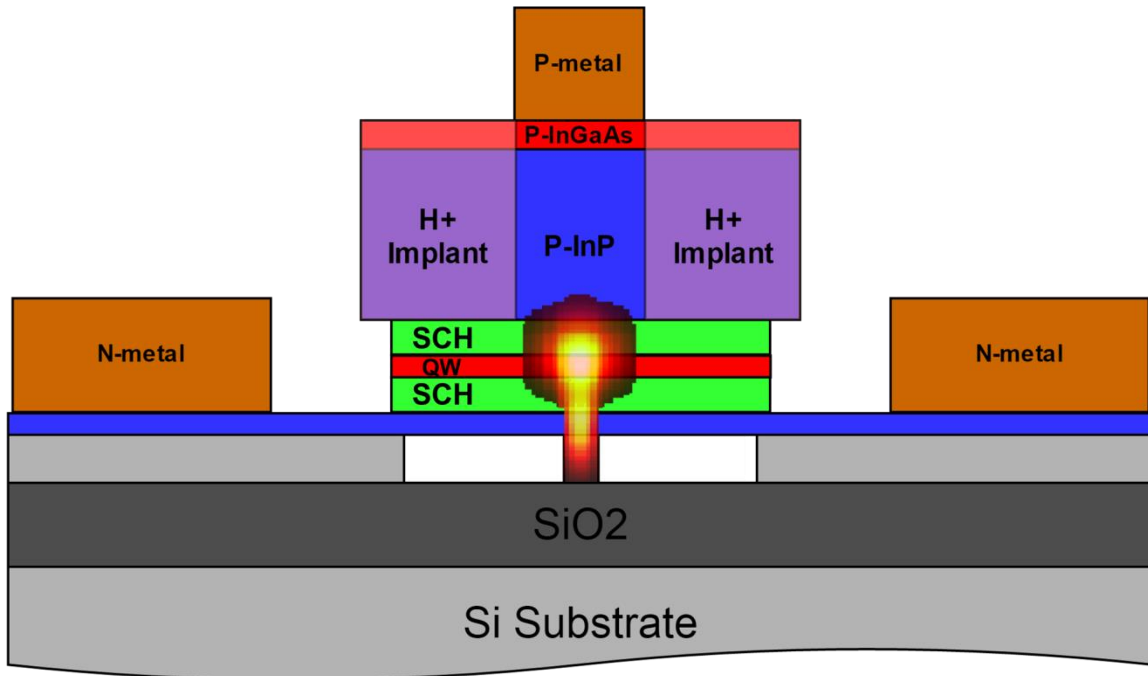

Figure 2. Illustration of the cross-section of the gain region with the simulated mode overlaid.

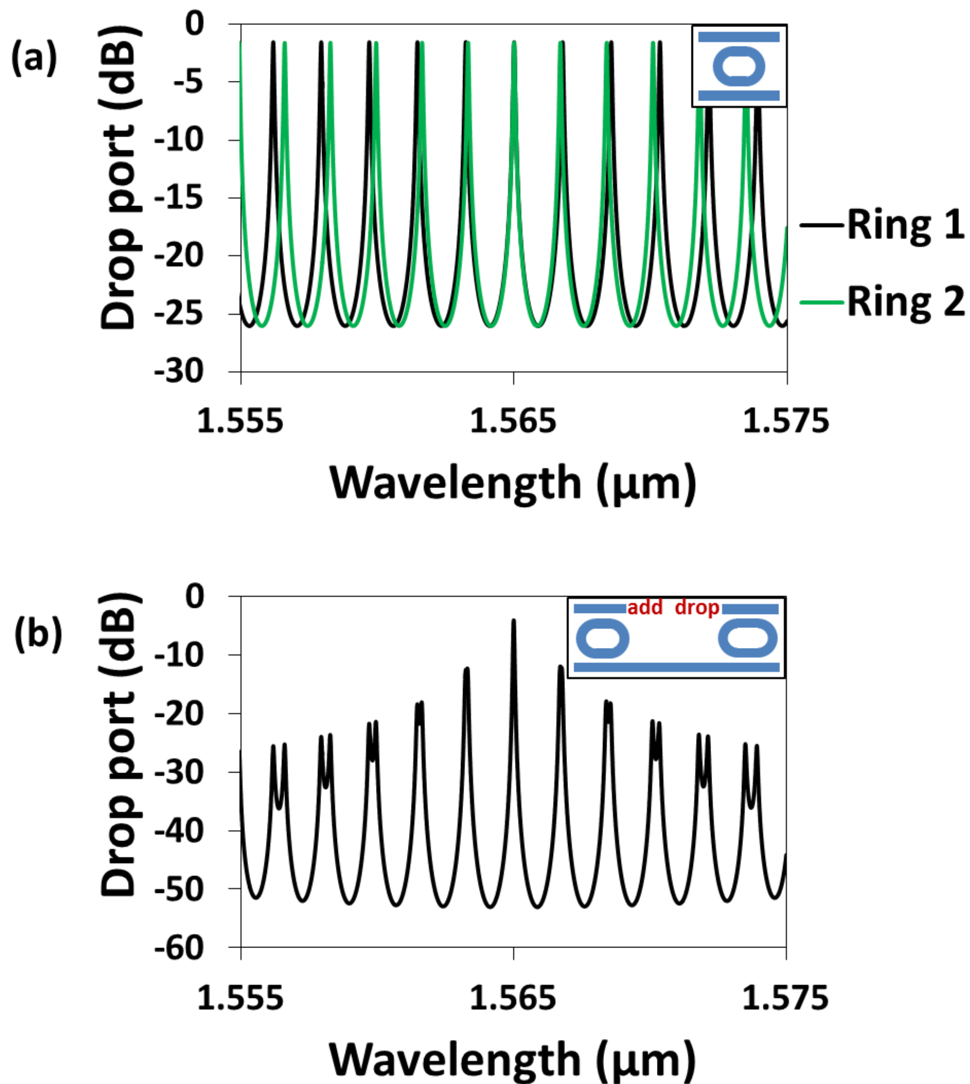

Figure 3. (a) Calculated spectra of two ring resonators of 400 and 420 μm circumferences. (b) Spectrum of light passing through two ring resonators of different circumference.

There are some benefits in linewidth that come from using rings with low waveguide loss. First, as the rings near resonance the photons circulate longer in the rings and the effective cavity length increases as shown in Figure 4. This can reduce the linewidth of the lasers.

Also, when slightly off resonance, a ring filter causes negative or positive optical feedback, depending on which side of the resonance is chosen. For negative optical

feedback, the laser is operated at slightly lower frequency than the resonance. When frequency noise increases the operating frequency slightly that causes the mirror reflectivity to increase. The photon density then increases which reduces the carrier density. This increases the refractive index which reduces the frequency and thus reduces the frequency noise and the laser linewidth. However, operating off-resonance at higher frequencies will have the opposite effect and will increase linewidth. More detailed calculations are contained in[5][7].

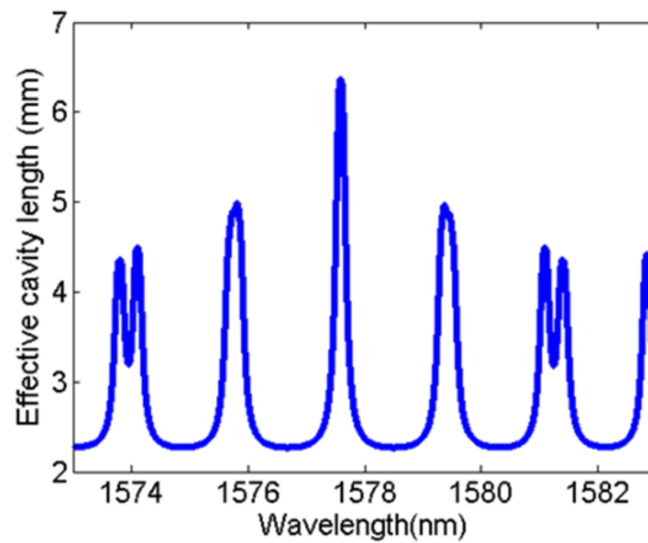

Figure 4. Effective cavity length vs. wavelength for ring-bus-ring laser [5].

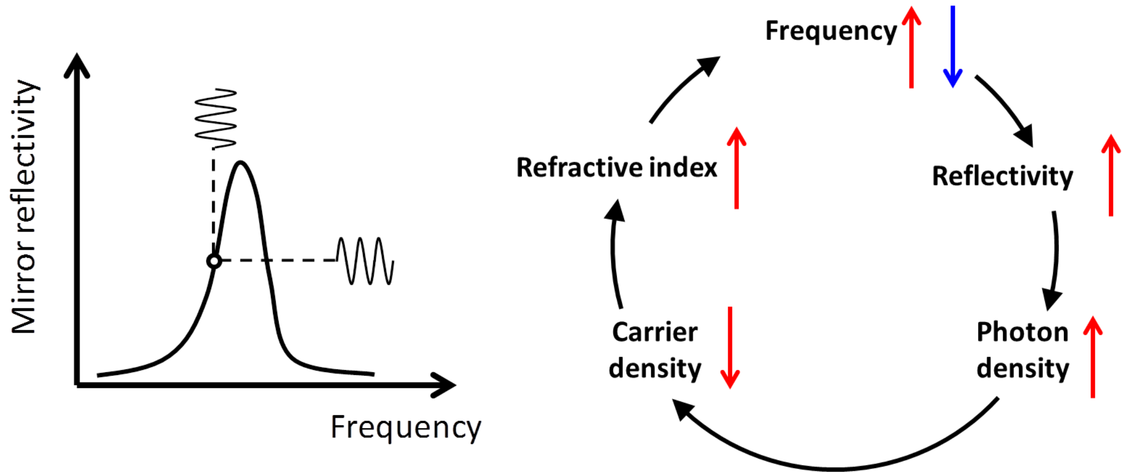

Figure 5. Negative optical feedback from off-resonance operation of ring-based laser [5].

2.2 Vernier ring laser

The vernier ring laser (VRL) is designed as a racetrack laser with two ring filters as illustrated in Figure 6. A calculation of the expected round-trip passive spectrum is shown in Figure 7. This includes the two ring filters but also the modes from the entire racetrack cavity.

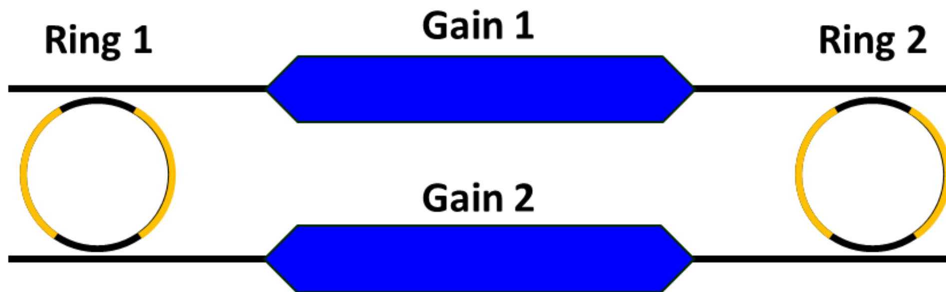

Figure 6. Illustration of the Vernier ring laser first iteration.

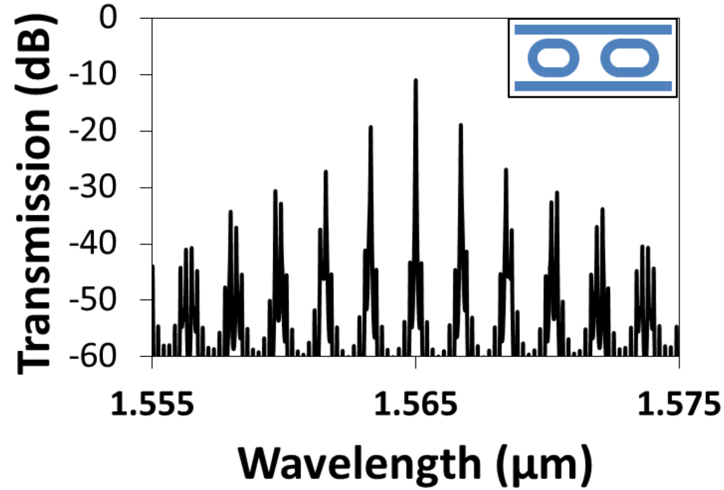

Figure 7. Calculated spectrum of Vernier ring laser waveguides. Transmission refers to power remaining in the cavity after one round-trip [8].

Vernier ring laser first iteration

The first iteration design used two gain sections, but did not include a phase section. Very slight changes to the gain current allows for phase tuning. The ring resonators, Ring 1 and Ring 2, are 400 µm and 420 µm long with an expected FSR of 1.74 nm and 1.66 nm respectively. The offset in the FSR of the rings is designed to be large enough to avoid low round-trip losses in adjacent peaks, but small enough so that the next Vernier overlap occurs at ±21 FSRs, or 37 nm, which was the expected gain bandwidth – in this way single wavelength operation was assured. The combined FSR is calculated by Equation 3.

$$Combined_FSR = \frac{FSR1 * FSR2}{|FSR1 - FSR2|} \qquad \textbf{Equation 3}$$

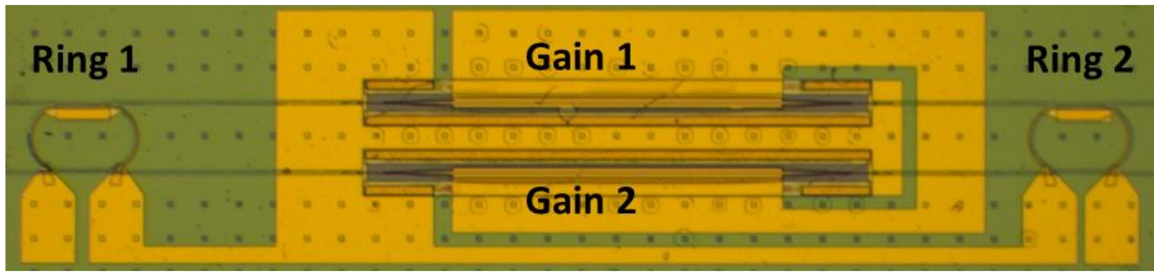

Figure 8. Optical photo of Vernier ring laser [8].

Transmission measurements of the ring resonators were performed on polished and anti-reflection coated passive devices using an external tunable laser, two single-mode lensed fibers, and a power meter. Light was fiber coupled to a bus waveguide that was coupled to a ring resonator and a wavelength sweep was performed. The output of the bus waveguide with the two ring spectra superimposed is shown in Figure 9 where the resonant wavelengths of the rings show a drop in throughput power. The data show individual ring FSRs of 1.60 and 1.53 nm and a coupled FSR greater than 32 nm. The FSRs of both rings are lower than designed, resulting in a lower expected tuning range, but 40 nm tuning may still be achieved by aligning the FSR peaks of the full laser cavity. The difference between the expected results and the simulation is attributed to etch depth variation. Fine tuning data of a single peak is also shown with a least squares fit modeling transmission. Ring 1 and 2 have unloaded round trip losses of 0.20 dB and 0.15 dB respectively (5.1 and 3.5 dB/cm) and power coupling coefficients to the bus waveguides of 2.6% and 1.7%. The FSR of the full passive cavity is measured to be 0.16 nm.

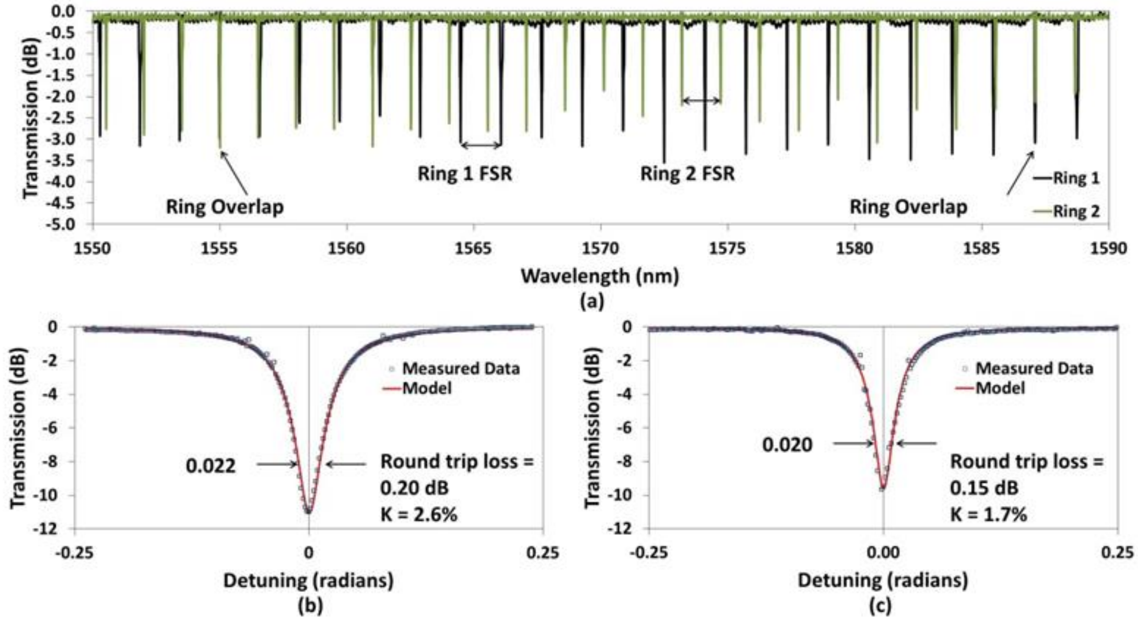

Figure 9. (a) Transmission data for full FSR of coupled rings. (b) Fine tuning data from ring filter 1 and (c) ring filter 2 [8].

Loss measurements of the silicon waveguides were performed using the cutback method. Light from an external laser source was passed through waveguides of increasing length to distinguish between fiber coupling and waveguide losses. Waveguide and fiber coupling losses were measured to be 0.58 cm-1 and 11.5 dB respectively. The tapered transitions from silicon waveguides to III-V gain sections as well as the gain section itself were characterized by Davenport et al. [9]. The tapered transitions were 100 µm long. Transition losses were measured to be 10 dB per transition at threshold (there were four such transitions in this device). Gain section losses were measured to be 11.7 cm^{-1}. The total intracavity loss is calculated to be 45 dB, which is largely dominated by tapered transition losses. As a result of such high losses, room temperature operation of this laser resulted in insufficient gain for widely tunable operation. Active measurements were taken with the chip mounted on a thermally controlled chuck maintained at 10^0 C. The gain epi used on this device was epi E (Appendix B — Epi). Details of the fabrication process after several

years of process optimization are discussed in Appendix C. A list of the actual process steps used here can be found in Appendix D under the heading Beam-steering: Phase 2 / Tunable laser.

A maximum on-chip output power of 3.3 mW from a single output was achieved with a threshold current of 160 mA at 10^0 C. This value was measured using a lensed fiber and adjusted to subtract out the measured coupling loss. Threshold current density was 2350 A/cm2 for the combined gain element length of 1360 μm. Such high current density is attributed to high losses in the tapered transition sections.

Later designs eschew the 80 μm taper used in this laser in favor of a 20 μm taper. It is believed that the tapers are not being efficiently pumped either due to the large side wall recombination or from hydrogen passivation. The hydrogen passivation is common for narrow devices in our process, which is why we opt for 24 μm gain widths with proton implantation as a means of current confinement. However, the tapers are necessarily narrow to provide a transition between the mode in the silicon and the mode in the combined silicon-III/V, which makes them susceptible to passivation. So, with the tapers being un-pumped, the 80 μm tapers each generate 10 dB of loss. It was found that 20 μm tapers greatly reduce the loss. The negative tradeoff that comes with shortened tapers is an increase in reflection. However, at 20 μm the tapers still maintain a sufficiently low taper reflection to avoid complications from an extra cavity.

Linewidth measurements were made by the delayed self-heterodyne method using a delay length of 5.5 km of fiber and a modulation frequency of 100 MHz (Figure 10) [10]. The beat signal captured using an RF spectrum analyzer is shown in Figure 11(a). A Lorentzian function was fitted to the data with a 3 dB bandwidth of 676 kHz corresponding

to a laser linewidth of 338 kHz at 10^0 C and 260 mA pump current. Figure 11(b) shows single wavelength emission at 1575 nm with SMSR greater than 45 dB under the same conditions. Emission is nearly identical for clockwise and counterclockwise propagating modes for both power and wavelength.

One of the challenges with linewidth measurement is isolating the linewidth of the laser from external noise sources. In this experiment a homemade setup was used which consisted of a battery with a variable current output. The experiments for later laser designs used commercial low-noise current sources which were both more reliable and more accurate. Temperature was maintained with a large water-cooled copper chuck with thermal paste to reduce thermal resistance.

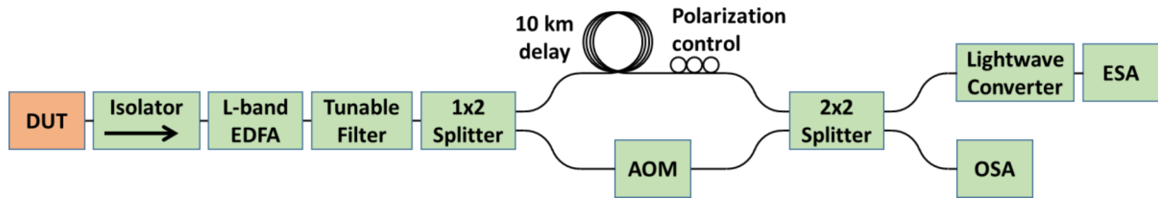

Figure 10. Schematic of self-heterodyne linewidth measurement setup.

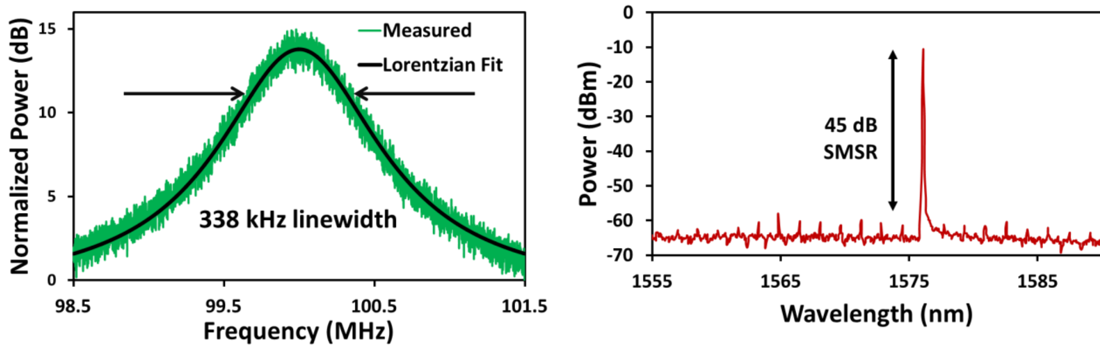

Figure 11. (a) Beat signal from a delayed self-heterodyne measurement of laser measuring 338 kHz linewidth at 10^0 C and 260 mA pump current. (b) Single wavelength lasing showing SMSR greater than 45 dB at 10^0 C and 260 mA pump current [8].

Wavelength tuning is accomplished by pumping current through a resistive heater above one or both of the ring resonators. Wavelength tuning was measured using a single-mode

tapered fiber connected to an optical spectrum analyzer with resolution of 0.06nm. Fine wavelength tuning was demonstrated with an arbitrarily chosen resolution of 0.1 nm and is shown in Figure 12(a) for a range of 2.5 nm by tuning both rings simultaneously. The heater tuning powers used are shown in Figure 12(b); the trend is generally linear with power for Heater 1. No clear trend was shown for Heater 2, which is attributed to thermal crosstalk. Thermal tuning over 40 nm was achieved with a SMSR greater than 35 dB and on-chip output powers greater than 0.45 mW at an operating temperature of 10^0 C as shown in Figure 12(c).

This first iteration of the Vernier ring laser was successful in many ways but also showed room for improvement. The tuning range was even larger than expected, although a satisfactory tuning map was not generated before one of the ring heaters was damaged. The SMSR was good but not impressive. In particular, the need to operate below room temperature was disappointing. However, many of these problems were overcome in the second iteration.

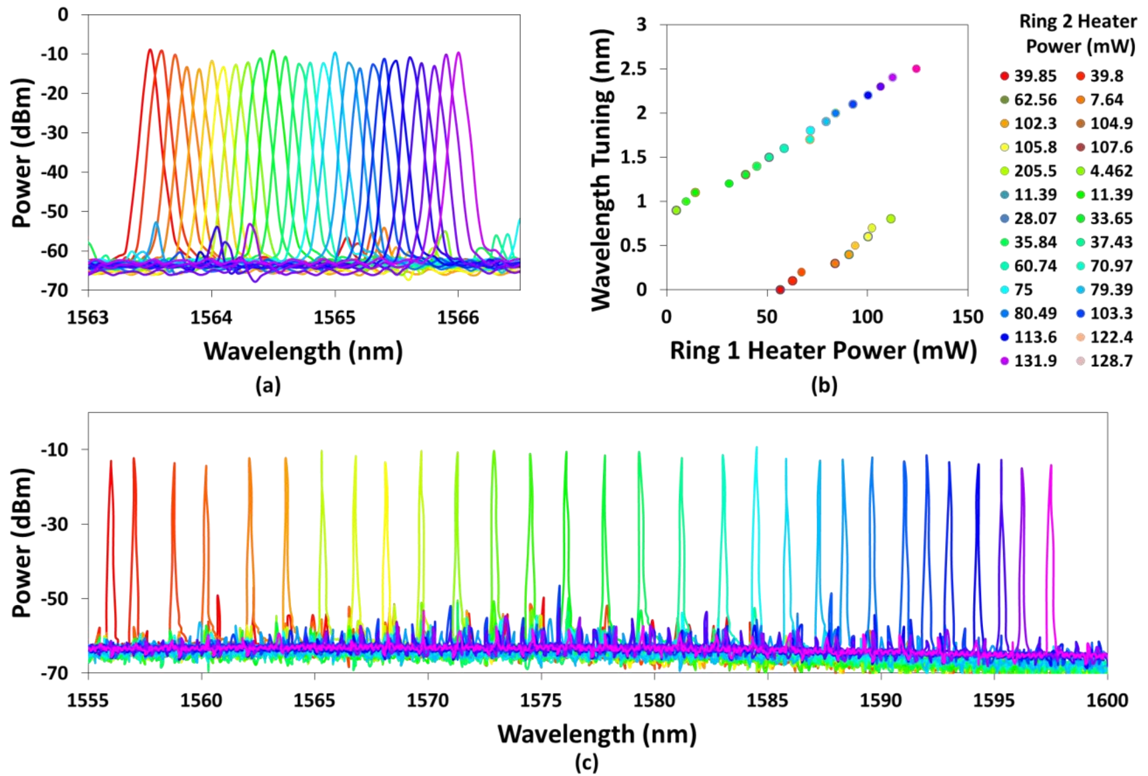

Figure 12. (a) Superimposed spectra showing 0.1 nm resolution tuning over 2.5 nm. (b) Wavelength tuning as a function of heater power. (c) Superimposed spectra of coarse wavelength tuning over more than 40 nm with SMSR greater than 35 dB [8].

Vernier ring laser second iteration

The second iteration of the Vernier ring laser removed one of the gain sections as shown in Figure 13. This was done to reduce the threshold current, to allow room for a dedicated phase section, and to remove two out of the four tapered transition sections to reduce loss. In addition, the tapered transitions were reduced to 20 μm long to further reduce losses. Measurements show the shorter transition to have as low as 0.5 dB loss, a factor of 20 improvement. Also, epi H was used for the gain section which only uses three quantum wells and is expected to have lower threshold currents and higher saturated output powers. The design and characterization of the epi was done by Michael Davenport and is not included in detail here.

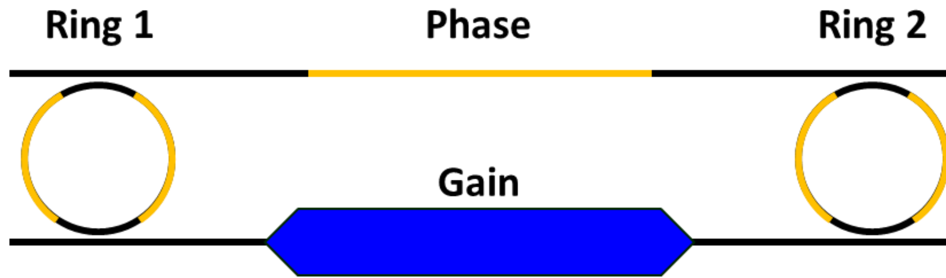

Figure 13. Illustration of the Vernier ring laser second iteration.

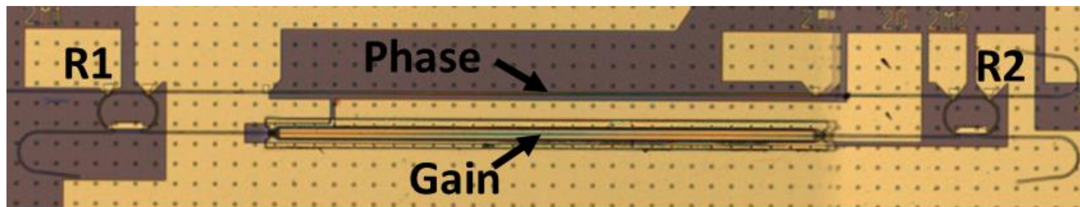

Figure 14. Optical photo of the second iteration of the Vernier ring laser.

A maximum single-sided power of 14.8 mW was measured on an integrating sphere. Both directions of propagation were found to have equal output powers, so we can conclude that the single-facet output power is 7.4 mW. A threshold current of 32 mA at 20^0 C was measured. A tuning map showing a 48 nm range is shown in Figure 15 with the corresponding SMSR in Figure 16. The teeth in the tuning map are attributed to a coupled FSR that is smaller than the gain bandwidth. When selecting a mode on the edges of the tuning range, the next selected Vernier peak also receives appreciable gain, causing the tuning map to jump back and forth between the longest and shortest wavelengths of the range. The side mode suppression is as high as 50 dB in single mode regimes. There are also regions where the laser is no longer single mode as it hops to the next mode. The peak power at each heater setting is shown in Figure 17. The ~10 dB of facet coupling loss was not subtracted from this figure due to the wavelength variance (see Figure 89 in Chapter 4). The best linewidth was measured to be 163 kHz (Figure 18) using the technique described in the section detailing the first iteration of the Vernier ring laser. The linewidth is not constant

across the tuning range, so the change in linewidth at various wavelengths is shown in Figure 19. Linewidths were kept under 212 kHz.

The second iteration of the laser was much improved over the first. It shows higher output power, larger tuning range, higher SMSR and lower linewidth. It operates at room temperature, making it more suitable for use in photonic integrated circuits.

Although this laser shows 48 nm of tuning, the tuning map is not ideal. The hoping between sides of the gain peak makes it more difficult to use on the extremes of the tuning range. However, with a simple adjustment to the ring circumference (see Equation 1Equation 2Equation 3), the combined FSR could be stretched to 50 nm which would remove the aberrations on the tuning map.

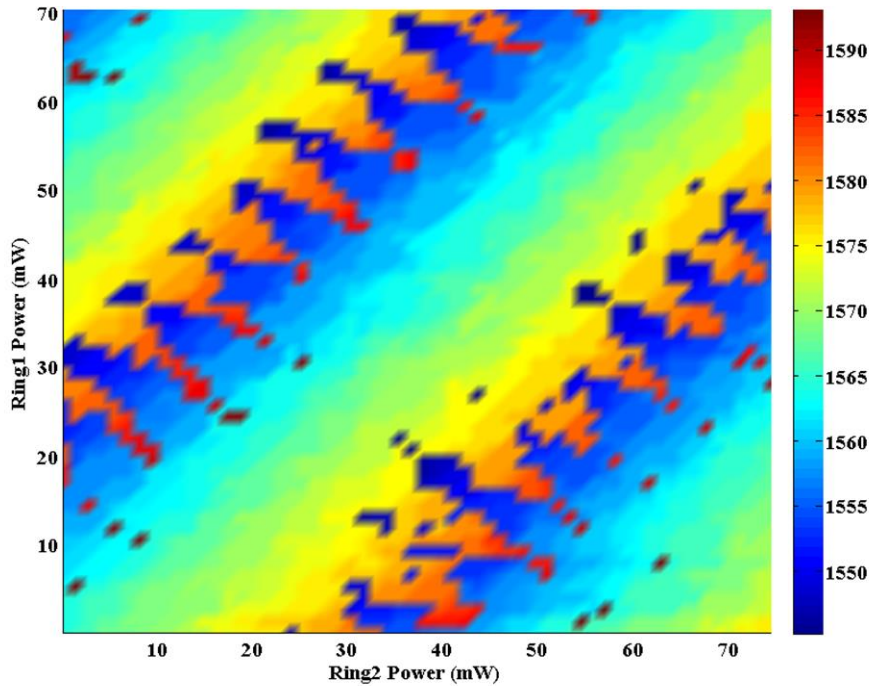

Figure 15. Wavelength (nm) vs. electrical power for both ring heaters of the Vernier ring laser second iteration.

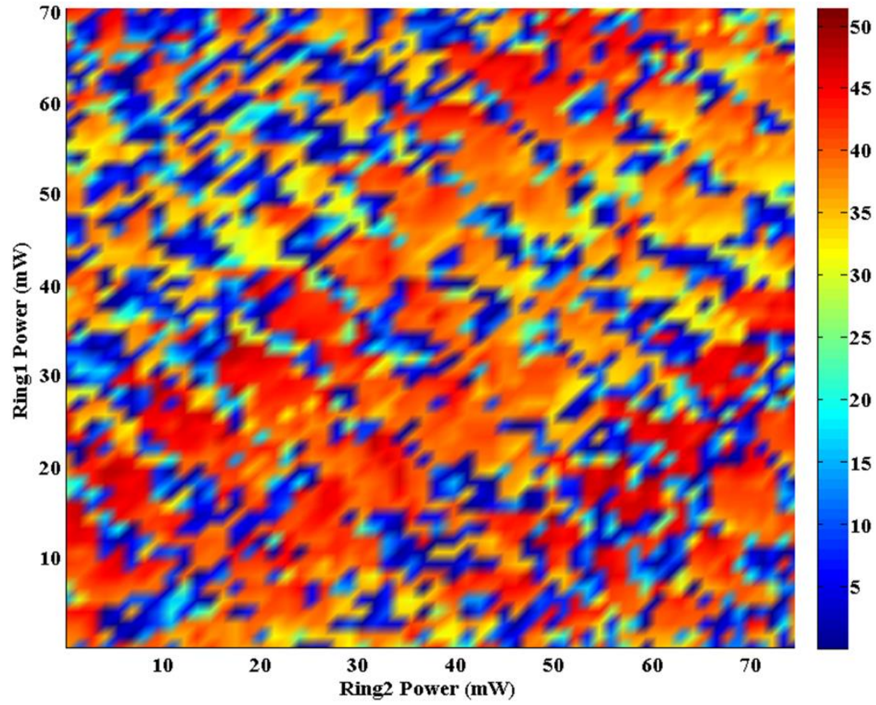

Figure 16. Side mode suppression (dB) vs. electrical power for both ring heaters of the Vernier ring laser second iteration.

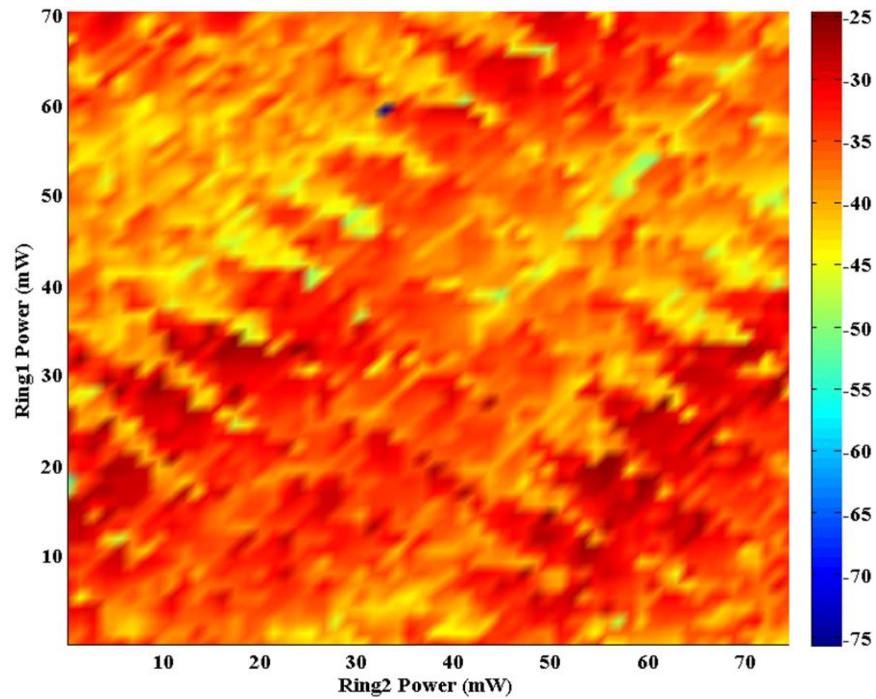

Figure 17. Peak fiber-coupled power (dBm) vs. electrical power for both ring heaters of the Vernier ring laser second iteration. On-chip power is ~10 dB higher.

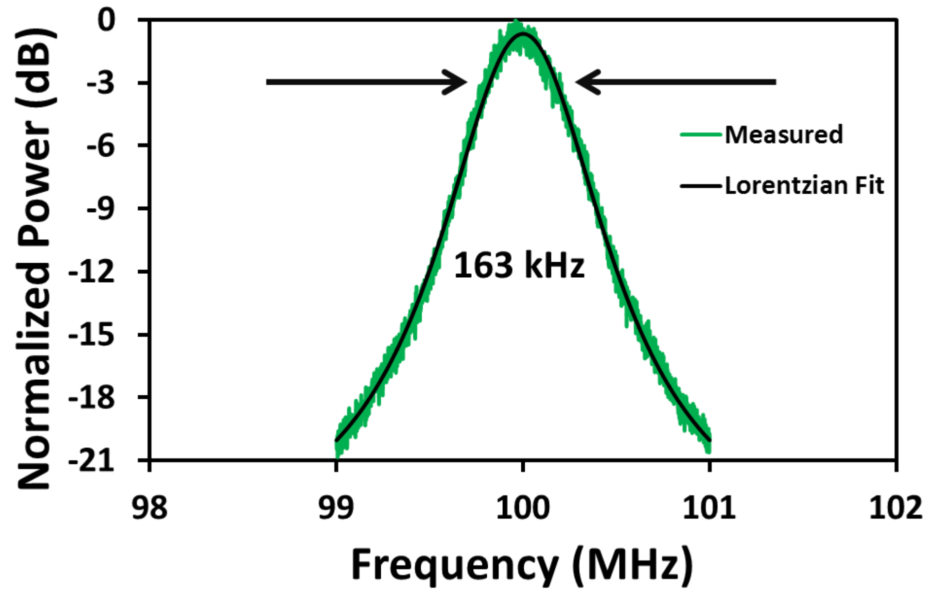

Figure 18. Linewidth measurement of Vernier ring laser second iteration showing 163 kHz.

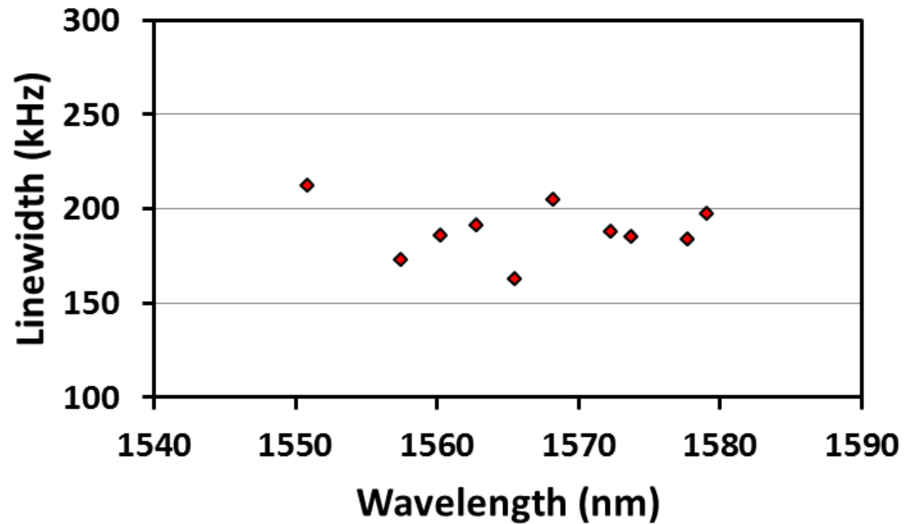

Figure 19. Linewidth of second iteration VRL laser vs. wavelength.

2.3 Coupled ring resonator laser

The single-sided coupled ring resonator (CRRx1) laser utilizes two different mirror structures[11][12]. On one side, a loop mirror is used. For a loop mirror with a 50% coupler

and no waveguide loss, the mirror should theoretically reflect 100% of power as shown in Figure 21. In reality, the presence of waveguide loss and a wavelength dependent coupling coefficient means the reflectivity will be somewhat lower as detailed in Equation 4 where R is reflectivity, L is the length of the loop, α is the waveguide loss, and k is the field coupling coefficient.

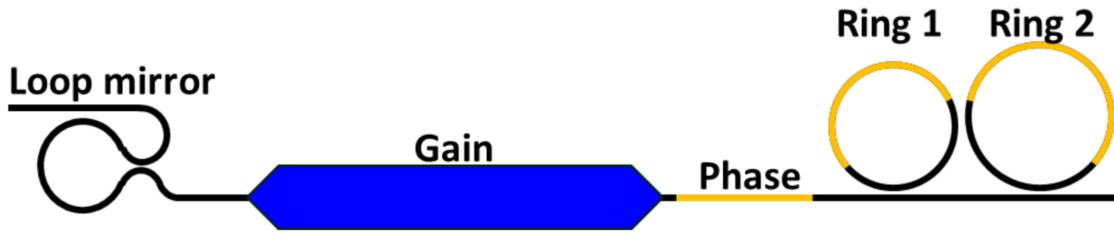

Figure 20. Schematic of one-sided coupled ring resonator laser.

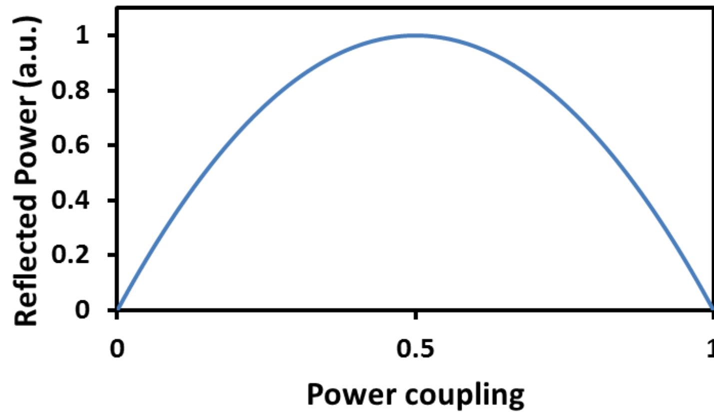

Figure 21. Reflected power vs. power coupling of a loop mirror.

$$R = 1 - \left| e^{-j\beta L} e^{-\alpha L} (1 - 2k^2) \right|^2 \qquad \textbf{Equation 4}$$

The other mirror is made from a coupled-ring resonator (CRR). In this configuration two rings are coupled to the same bus and are also coupled to each other as illustrated in Figure 22. The reflectivity spectrum of the CRR mirror is dependent on the ring circumference, the coupling coefficients, and the waveguide loss. The equations governing the reflection are shown below[13][14] [15]. The selected circumference values for Ring 1 and Ring 2 were

337 μm and 368 μm respectively, and the selected power coupling coefficient values for K_1, K_2, and K_3 are 2.25%, 2.25%, and 36% respectively. The calculated reflection spectrum is shown in Figure 17.

$$V = e^{-\alpha_1 R_1 \theta_1} e^{-j\beta_1 R_1 \theta_1}$$ **Equation 5**

$$W = e^{-\alpha_2 R_2 \theta_2} e^{-j\beta_2 R_2 \theta_2}$$ **Equation 6**

$$X = e^{-\alpha L} e^{-j\beta L}$$ **Equation 7**

$$Y = e^{-\alpha_1 R_1 (2\pi - \theta_1)} e^{-j\beta_1 R_1 (2\pi - \theta_1)}$$ **Equation 8**

$$Z = e^{-\alpha_2 R_2 (2\pi - \theta_2)} e^{-j\beta_2 R_2 (2\pi - \theta_2)}$$ **Equation 9**

$$A = 1 - \tau_1^* \tau_2 VY$$ **Equation 10**

$$B = 1 - \tau_2^* \tau_3^* WZ$$ **Equation 11**

$$D = 1 + \frac{|\kappa_2|^2 \tau_1^* \tau_3^* VWYZ}{AB}$$ **Equation 12**

$$P = \frac{\kappa_1^* \kappa_2^* \kappa_3 \tau_1 XZV}{DAB}$$ **Equation 13**

$$\left|\frac{E_2}{E_1}\right|^2 = \left| P \left(\frac{1 - \frac{|\kappa_1|^2}{AD}}{1 - |\kappa_1|^2} \right) \left(1 - \frac{\kappa_1 \kappa_2 \kappa_3^*}{\kappa_1^* \kappa_2^* \kappa_3} \right) \right|^2$$ **Equation 14**

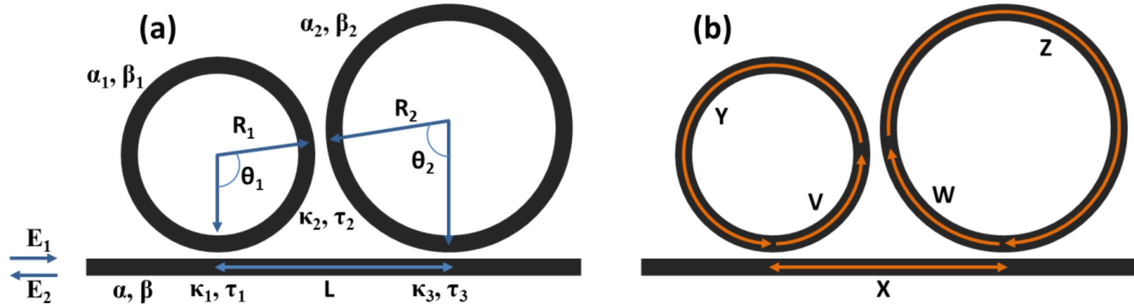

Figure 22. Illustration of a coupled-ring resonator mirror with parameters relevant to the reflectivity equations labeled.

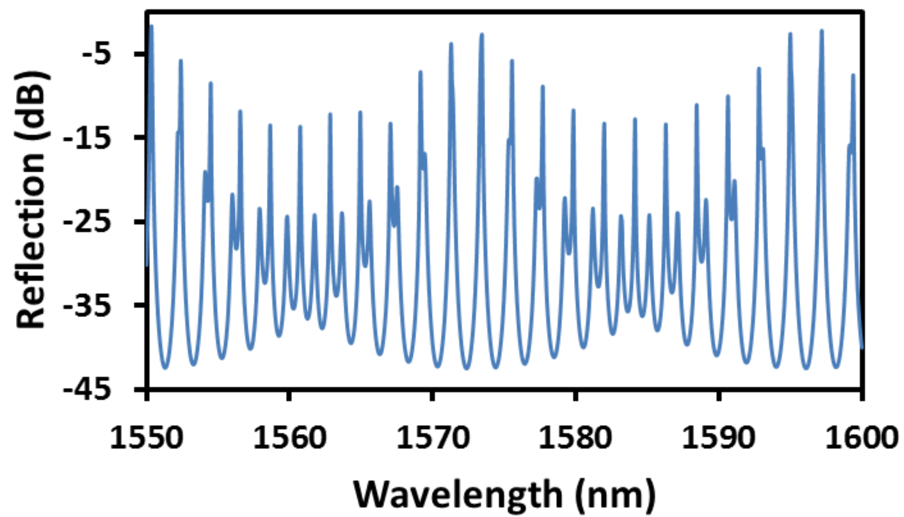

Figure 23. Calculated reflection spectrum from the CRR mirror.

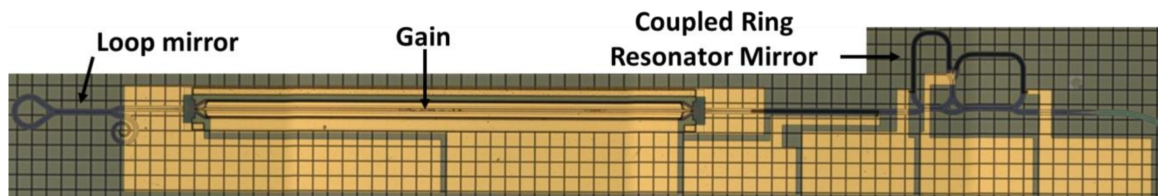

Figure 24. Optical photo of one-sided coupled-ring resonator laser.

The gain epi and the taper design utilized for this laser are identical to that of the second iteration of the Vernier ring laser (section 2.2) and the ring-bus-ring laser (section 2.4), and they were processed together. See Chapter 5 for details of the process.

An optical microscope image of the finished CRRx1 laser can be seen in Figure 24. The wavelength tuning map, SMSR map, and peak power map vs. ring tuning power are shown in Figure 25, Figure 26 and Figure 27. It exhibits 21 nm of wavelength tuning. However, the laser does not exhibit single mode behavior for much of the tuning map. When it is single mode the SMSR usually reaches 50 dB. The plotted output power is the fiber-coupled power and would be around 10 dB higher on-chip. The best linewidth was measured to be 148 kHz (Figure 28). The linewidth at various wavelengths changes, but was kept under 200 kHz (Figure 29). The maximum single-sided output power was measured to be 11.9 mW on an integrating sphere. The threshold was measured to be 45 mA.

While this laser performs respectably in some regards, we cannot overlook the poor side mode suppression for the majority of tuning conditions. The complexity of the CRR mirror makes it difficult to control, and as the rings are tuned it can easily shift into a multiple lasing mode regime. It is the authors opinion that a CRR mirror is better suited to a fixed wavelength design where it can perform well. Other laser designs work better for tuning, such as the Vernier ring laser (section 2.2) and the ring-bus-ring laser (section 2.4).

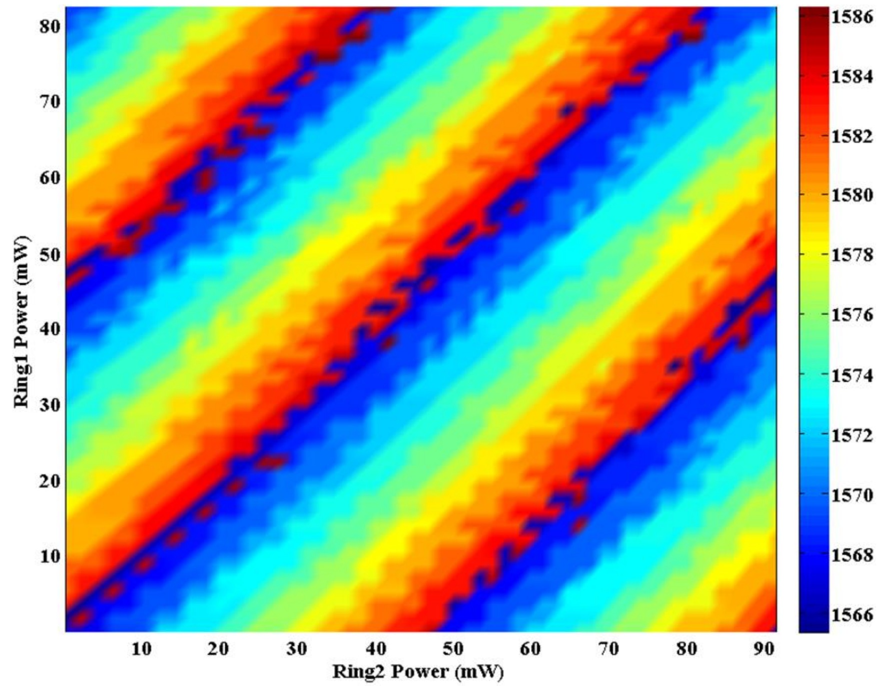

Figure 25. Wavelength (nm) vs. electrical power for both ring heaters of the one-sided coupled ring resonator laser.

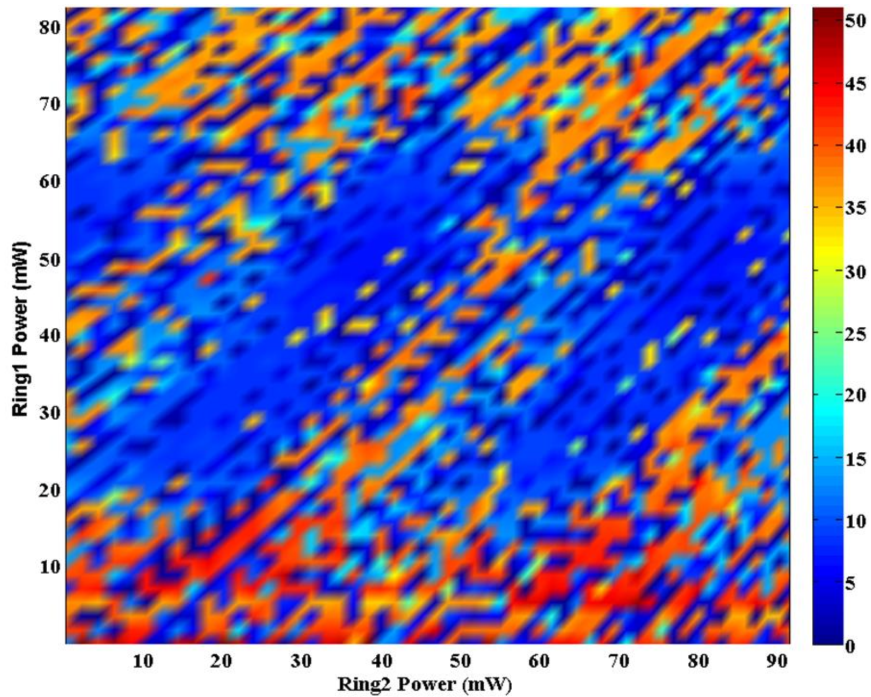

Figure 26. Side mode suppression (dB) vs. electrical power for both ring heaters of the one-sided coupled ring resonator laser.

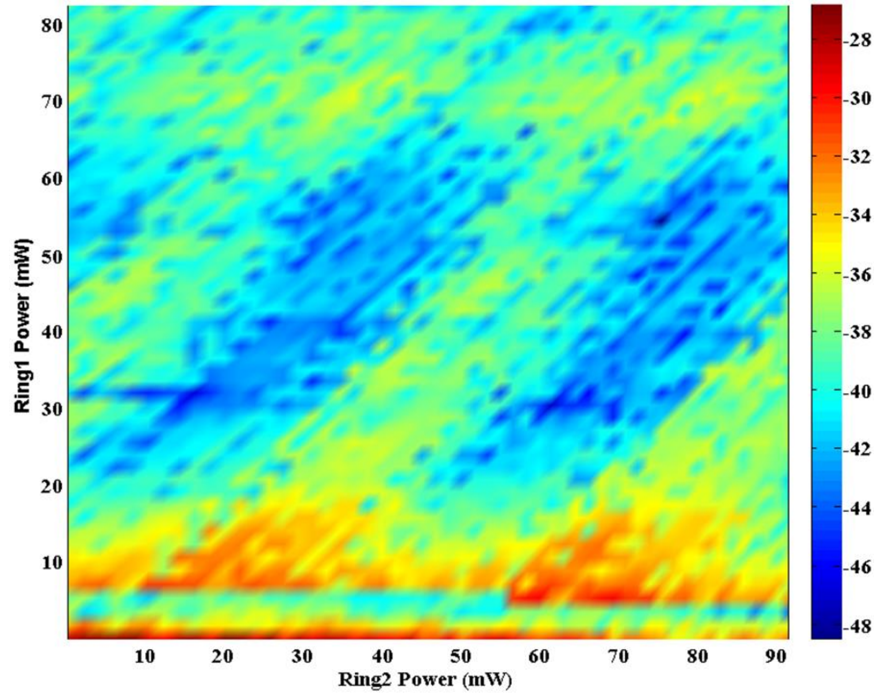

Figure 27. Peak fiber-coupled power (dBm) vs. electrical power for both ring heaters of the one-sided coupled ring resonator laser.

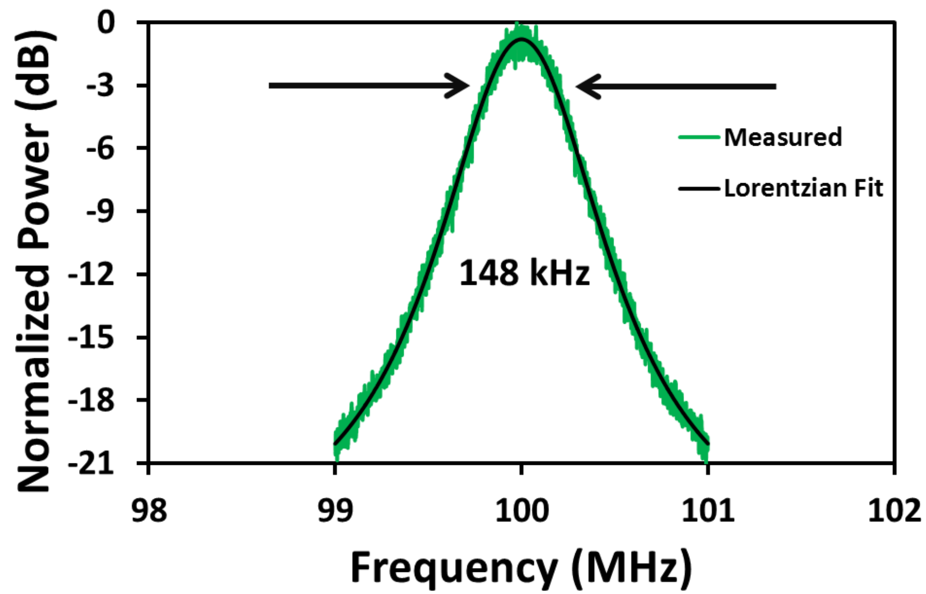

Figure 28. Linewidth measurement of CRRx1 laser showing 148 kHz.

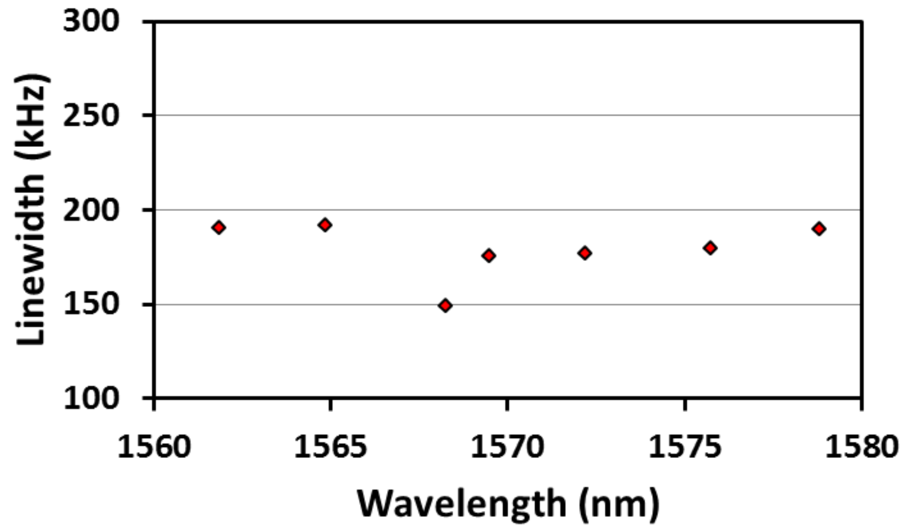

Figure 29. Linewidth of CRRx1 laser vs. wavelength.

2.4 Ring-bus-ring laser

The ring-bus-ring (RBR) laser utilizes two loop mirrors with two ring filters in between, similar to the design by Matsuo and Segawa[16]. The calculated spectrum for two passes through the ring-bus-ring filter is shown in Figure 31. The selected circumference values for Ring 1 and Ring 2 were 256 μm and 271 μm respectively, and the power coupling values were all selected to be 20%.

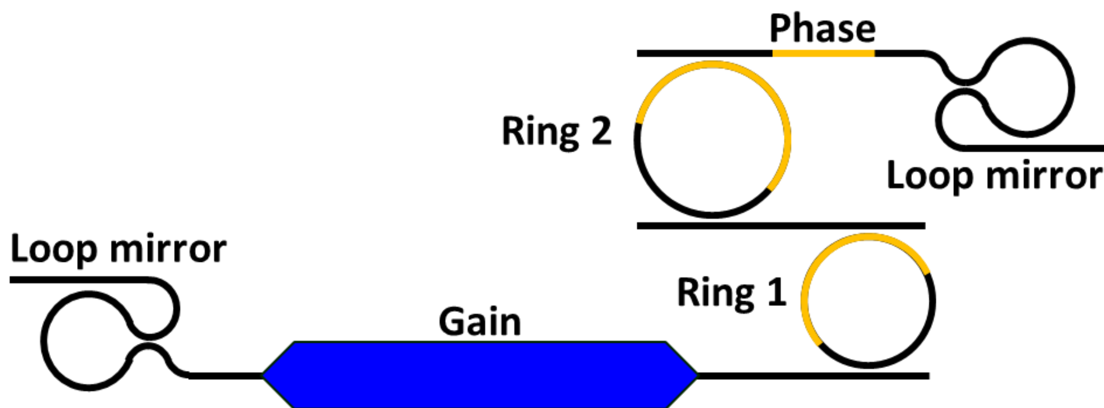

Figure 30. Schematic of ring-bus-ring laser.

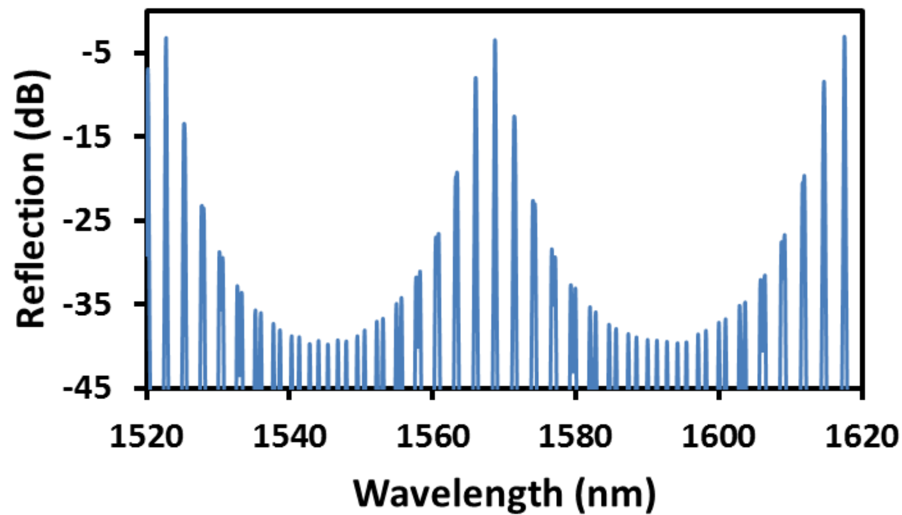

Figure 31. Calculated spectrum from two passes through the RBR filters.

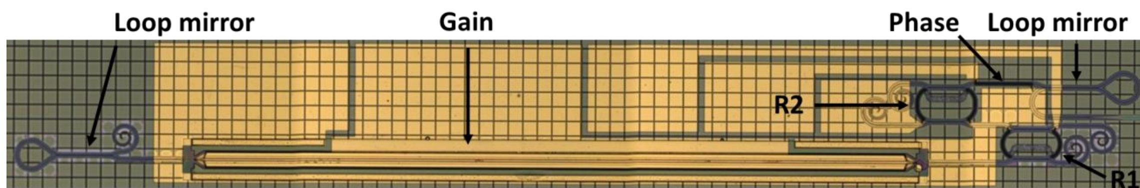

Figure 32. Optical photo of ring-bus-ring laser.

An optical microscope image of the finished RBR laser can be seen in Figure 32. The wavelength tuning map, SMSR map, and peak power map vs. ring tuning power are shown in Figure 33, Figure 34, and Figure 35. It exhibits 42 nm of wavelength tuning. The side mode suppression was fairly consistent for much of the map but not very high. This is primarily due to problems with fiber coupling that resulted in lower measured power levels such that the side modes were below the noise level of the optical spectrum analyzer. The best linewidth was measured to be 148 kHz (Figure 36). The linewidth was kept under 280 kHz for a wide span of wavelengths (Figure 37). The measurement with an integrating sphere showed a maximum single-sided output of 10.2 mW, and a threshold current of 45 mA.

The ring-bus-ring design is far simpler to operate than the CRR design and is much more consistent. The SMSR and output power are dependent on the accuracy of the directional couplers in the mirrors and in the rings. Much better performance can be expected in these areas when using a more repeatable process. As with the Vernier ring laser there are more than two output ports which creates additional loss. However, it is clear that the maximum output power is not much different than that of the other laser designs.

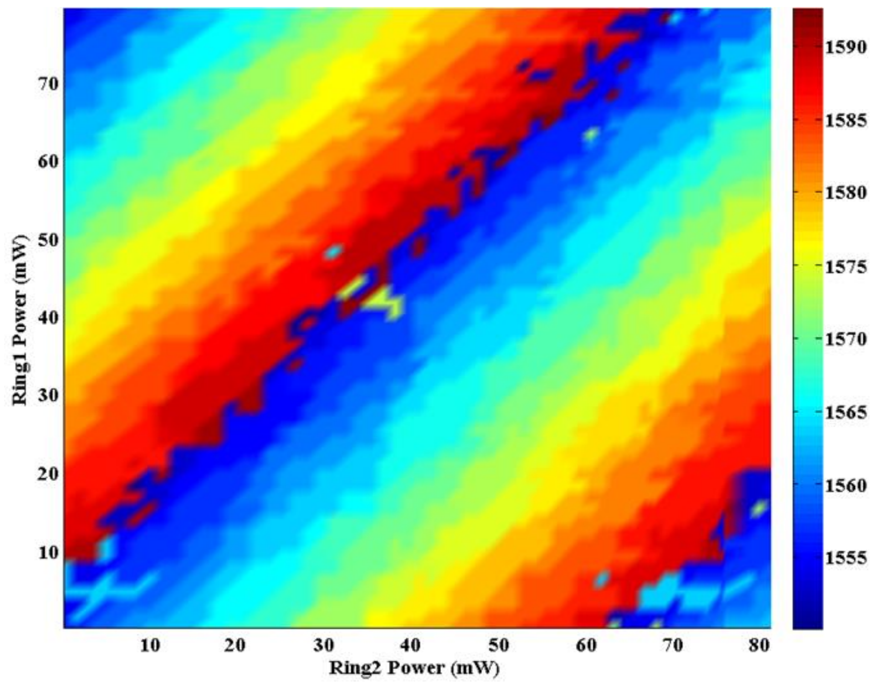

Figure 33. Wavelength (nm) vs. electrical power for both ring heaters of the ring-bus-ring laser.

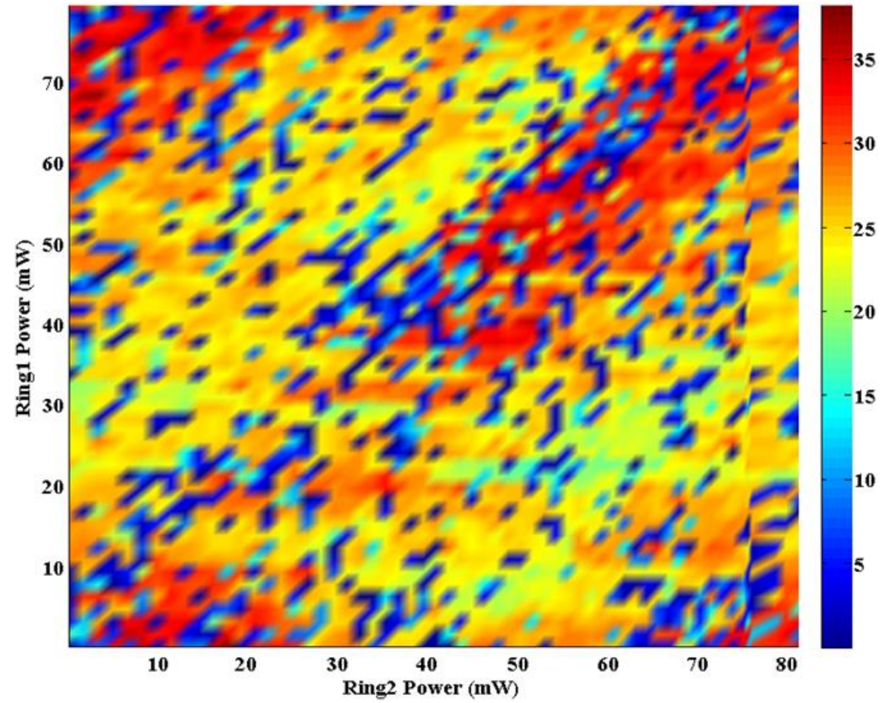

Figure 34. Side mode suppression (dB) vs. electrical power for both ring heaters of the ring-bus-ring laser.

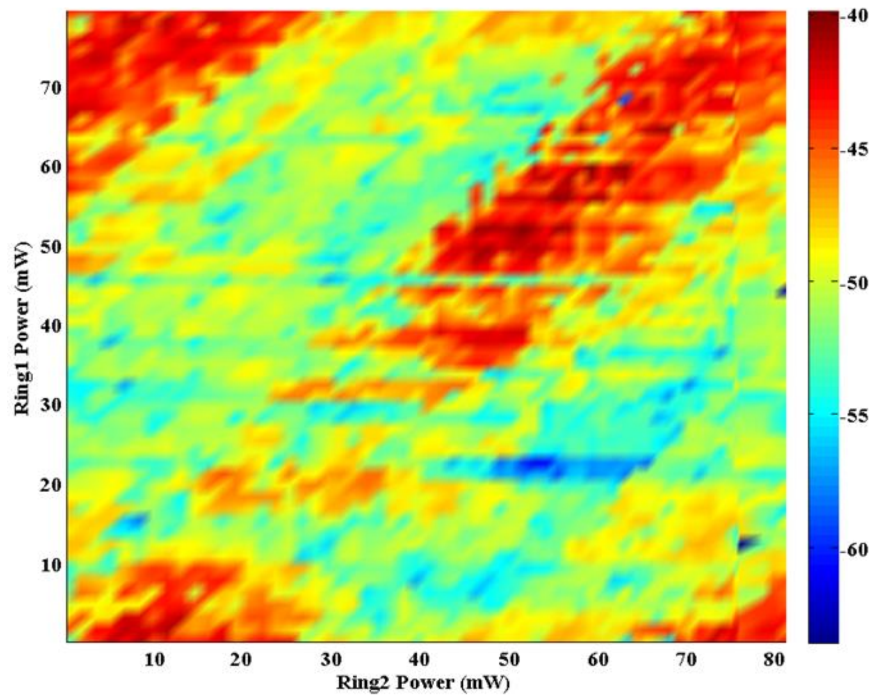

Figure 35. Peak fiber-coupled power (dBm) vs. electrical power for both ring heaters of the ring-bus-ring laser.

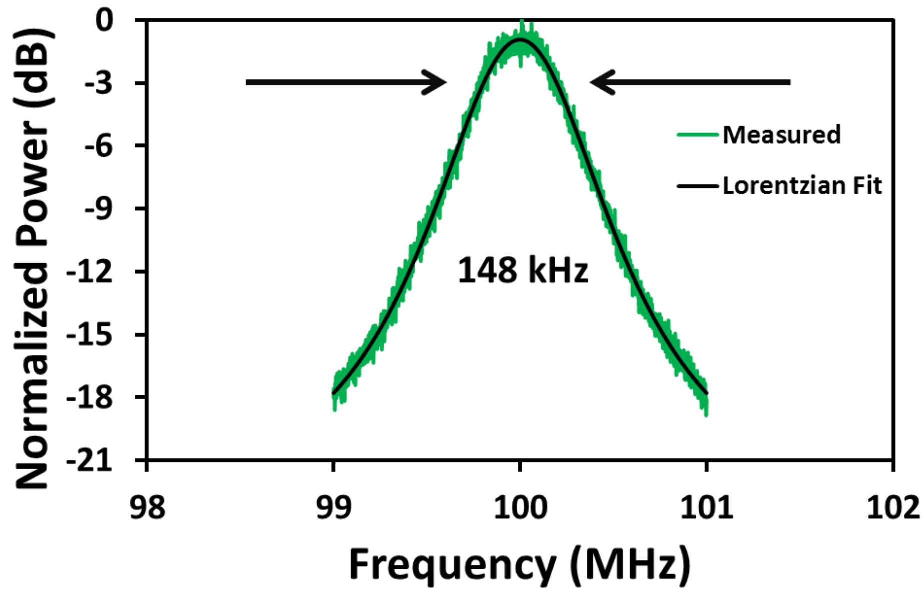

Figure 36. Linewidth measurement of ring-bus-ring laser showing 148 kHz.

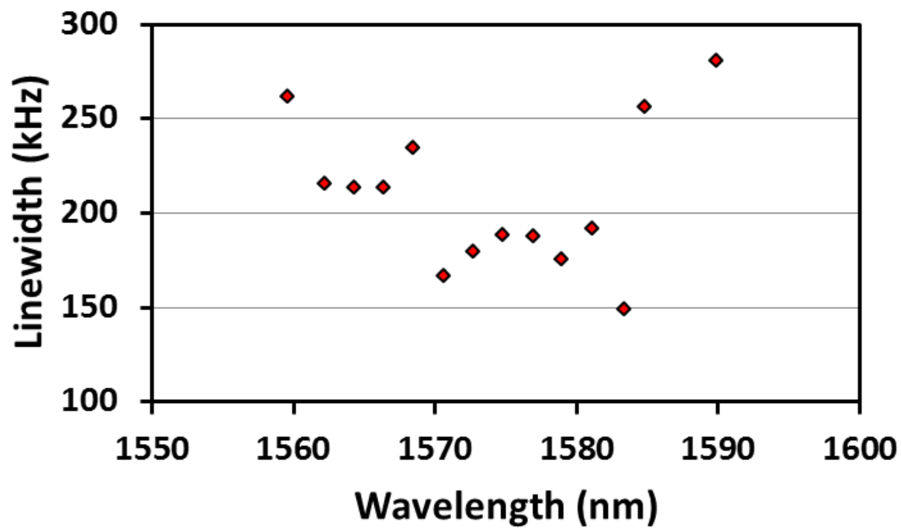

Figure 37. Linewidth of ring-bus-ring laser vs. wavelength.

2.5 Summary

Several tunable lasers have been examined here. The Vernier ring laser has the widest tuning range (48 nm). It has consistently high output power and fairly consistent SMSR.

However, the tuning map has teeth that suggest that we should have designed it to have an even larger tuning range. It also has a consistently low linewidth near 200 kHz.

The ring-bus-ring laser shows the most consistent tuning map and SMSR but is lower power than the others for the implementation here. The VRL second iteration also has a respectable tuning map. The low power in the RBR laser could be improved by changing the coupling coefficients and by maximizing the loop mirror reflectivity. The linewidth spreads a bit more than the other two laser types, but it is still below 300 kHz.

The CRRx1 laser has the best SMSR but is very inconsistent about being single mode. It is difficult to control because of the complex relation between coupled rings. During single mode operation, it has linewidths below 200 kHz. A two-sided CRR laser was also fabricated, but is not included here due to the extreme difficulty in aligning four rings simultaneously.

Tables comparing the results and the relative advantages and disadvantages of these lasers is shown below. Both the Vernier ring laser and the ring-bus-ring laser designs are good choices for the heterogeneous silicon platform, but the CRR laser should not be pursued further as a tunable laser design.

Laser type	Threshold (mA)	Max power (mW)	Max SMSR (dB)	Linewidth (kHz)	Tuning range (nm)
VRL iteration 1	160	3.3	45	338	41
VRL iteration 2	**32**	7.5	**50**	212	**48**
CRRx1	37	**11.9**	**50**	**191**	21
RBR	45	10.2	37	280	42

Table 1. Comparison of the performance of different lasers. Linewidth shown here is the worst case measured from the linewidth vs. wavelength plots.

Laser type	Advantages	Disadvantages
VRL	• Large tuning range • Good output power • High SMSR	• Four outputs dilutes power

	• Low linewidth • Simple to operate	
CRRx1	• High SMSR • Good output power • Low linewidth	• Often lases in multiple modes • Complicated
RBR	• Large tuning range • Good output power • High SMSR • Low linewidth • Simple to operate	• Four unused output ports dilutes power, depending on coupling

Table 2. List of some advantages and disadvantages of the lasers.

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Chapter 3

Free-space beam-steering

The ability to dynamically shift the direction of a beam has many important applications. For example, light detection and ranging (LIDAR) scans a laser beam over a range of angles and reads the reflected optical echo. By discretizing the data the system is able to generate three-dimensional images. The smaller wavelengths of light allow it to have much higher resolution than radar. It is conceivable that in the near future every vehicle will employ a LIDAR system to improve safety, collect data for mapping, traffic, and weather, and to provide feedback for automated driving. This will require LIDAR technology to advance beyond the current state. The Velodyne HDL-64E, which is used by the autonomous Google car, is sold for about $80,000. Models with 32 beams and 8 beams are sold for $40,000 and $8,000 respectively. They are so bulky that they are mounted to the roof of the vehicle, and the price makes it unrealistic to use more than one per vehicle. They use mechanical elements to steer the beam which limits the speed at which data can be acquired. The mechanical elements also reduce the lifetime of the system, particularly in high stress

environments such as aircraft. Future designs must be small enough that even multiple chips placed on a vehicle could be integrated in a cosmetically pleasing way. Smaller, lighter, and cheaper chips without moving parts are needed.

With advanced chips, it is possible that cameras and LIDAR systems will be paired in handheld devices, such as smartphones, to couple high resolution photography with high resolution spatial mapping to create realistic virtual settings. Augmented reality applications which currently use GPS and camera software would be greatly enhanced.

Other applications for beam-steering include point-to-point free-space communications where small angle adjustments allow the beam to track the intended detector without the need for fiber installation. Also holographic displays and biomedical imaging can utilize an adjustable beam angle. The increasing integration of photonic elements [1] makes is possible for optical phased arrays to demonstrate more compact, highly stable beam-steering, at lower costs than have previously been available.

Non-mechanical beam steering in two dimensions using silicon photonic chips has been demonstrated by several groups [2]-[6] by utilizing optical phased arrays (OPA). However, each of these examples requires an off-chip fiber-coupled laser. This complicates packaging, thus increasing cost, and greatly reduces the tolerance to mechanical stress.

A phased array uses coherent emitters to concentrate a beam in the far field. The phase difference between emitters determines the angle at which the light will interfere constructively. Sun et al. [7] demonstrated a 64x64 element OPA which emits the MIT logo by precisely tailoring the phases between elements in a passive silicon photonic circuit. They were able to demonstrate that any arbitrary image can be created in the far field with an OPA by using Fourier analysis to determine the required phase of each element. To take

it a step further, by adding phase shifters before each element, the beam can be actively steered and shaped. However, a two-dimensional OPA which has NxM elements requires N*M phase shifters. An array this size requires 4096 phase shifters, a challenge to implement in both power and circuitry. Scaling is an inherent problem with the two-dimensional array.

In this chapter, three phases of a beam-steering project will be detailed [8]-[11], including work with integrated on-chip lasers, amplifiers, phase tuners and photodetectors. The approach for this work utilizes a tunable laser to remove one dimension of the optical phased array while still allowing for two dimensions of beam-steering. This integrated chip solves the problem of mechanical instability and reduces the complexity of the electrical circuitry.

3.1 Concept

To reduce the number of active components, the beam-steering chip detailed here uses a one-dimensional optical phased array in conjunction with a tunable laser. Light is emitted from each channel of the OPA by a surface grating emitter. Each tooth of the grating scatters power from the optical mode with a phase delay determined by grating pitch and the effective index. In essence, the grating works as its own fixed OPA with precise linear phase differences for each tooth. By reducing the kappa of the grating and extending the effective length, one can achieve a highly focused beam in one dimension. In the far field, emission from a grating is a line perpendicular to the grating. The combined emission from several grating emitters interferes and produces outputs from the optical phased array which can steer in the first dimension.

The angle of emission (θ) of the mth order from a single grating is dependent on wavelength (λ), the grating period (Λ), and the effective index of the mode (n_{eff}), as shown in the Bragg equation (Equation 15). This allows us to change the angle of emission by changing the effective index of the grating with thermal or electro-optic tuners, or by changing the wavelength of the beam. As the circuitry required to alter the effective index of the grating is likely to increase losses, a tunable laser was chosen as the vehicle to produce beam-steering in the second dimension. By combining a tunable laser with a one-dimensional optical phased array, we are able to produce two-dimensional beam-steering with a linear scaling of controls elements. The total number of control elements required is N+M where N is number of phased array channels, and M is the number of elements used to control the laser (typically fewer than 4). This work will define θ to be the angle of emission determined by the wavelength and ψ to be the angle of emission determined by the optical phased array.

$$\sin\theta = \frac{\Lambda n_{eff} - m\lambda}{\Lambda} \qquad \textbf{Equation 15.}$$

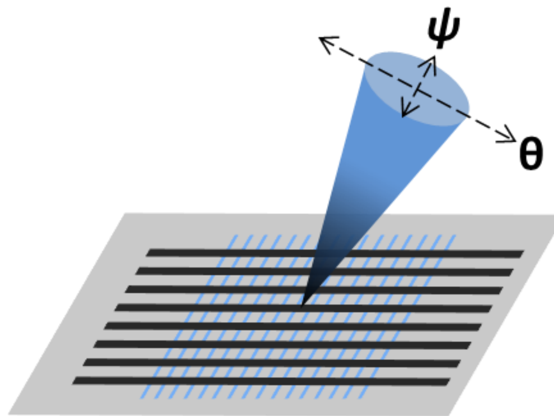

Figure 38. Illustration of an optical phased array with grating emitters showing the angle of emission tuned by wavelength (θ) and the OPA (ψ).

3.2 Optical phased array design

Phased array antennas have been around since 1905 when Karl F. Braun made them the study of his research. Optical phased arrays use the same principles at a much smaller scale.

For the design of a one dimensional array it is desirable to maximize the range over which the beam can be steered, and the number of spots that can be distinguished in that range. These parameters are largely controlled by channel count and channel spacing.

For a uniformly spaced array the angular separation ($\Delta\psi$) between the peaks of the main lobe and aliasing lobes is based on the wavelength (λ) and the pitch (d) between emitter elements as in Equation 16. A smaller distance between emitters is preferred, which is another reason to use a one-dimensional OPA. The emitter pitch in a two-dimensional OPA is inherently larger because of the need to route waveguides and circuitry between rows and/or columns. In a one-dimensional OPA the emitter pitch is only limited by cross-talk between channels through evanescent coupling.

$$\sin(\Delta\psi) = \frac{\lambda}{d} \qquad \textbf{Equation 16.}$$

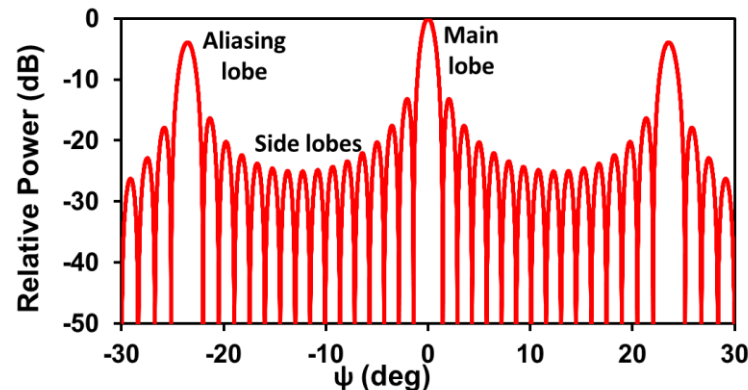

Figure 39. Calculated output of a uniformly spaced array with 16 channels and an emitter pitch of 4 μm.

The useful field of view (FOV) is the range of angles where the beam can be steered while maintaining the range free from aliasing lobes. The FOV is slightly smaller than Δψ due to the finite beam width of the lobes. The number of resolvable spots within the FOV is the FOV divided by the full-width half-max (FWHM) of the beam. An illustration of the need for a finite FOV is shown in Figure 40. The equation governing output angle for a linear phase shift (ϕ) between channels is found in Equation 17.

$$\sin(\psi) = \frac{\lambda\phi}{d}$$ **Equation 17.**

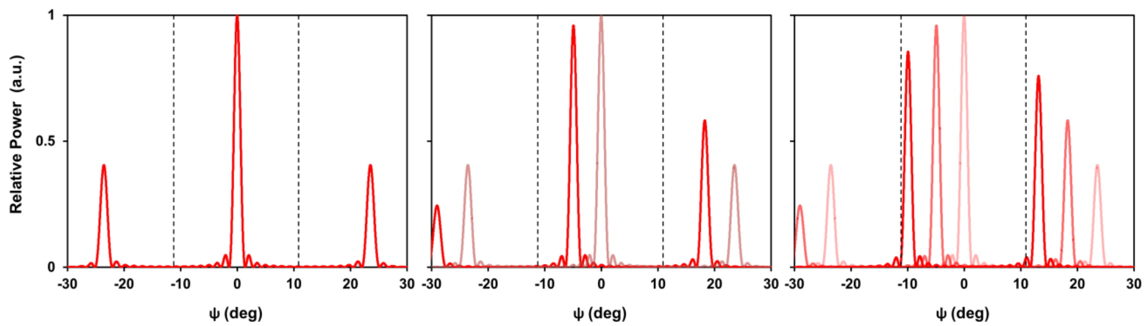

Figure 40. Calculated far field emission from a uniform OPA steered to 0, 5, and 10 degrees. The field of view excludes aliasing lobes for all angles of the main lobe within it.

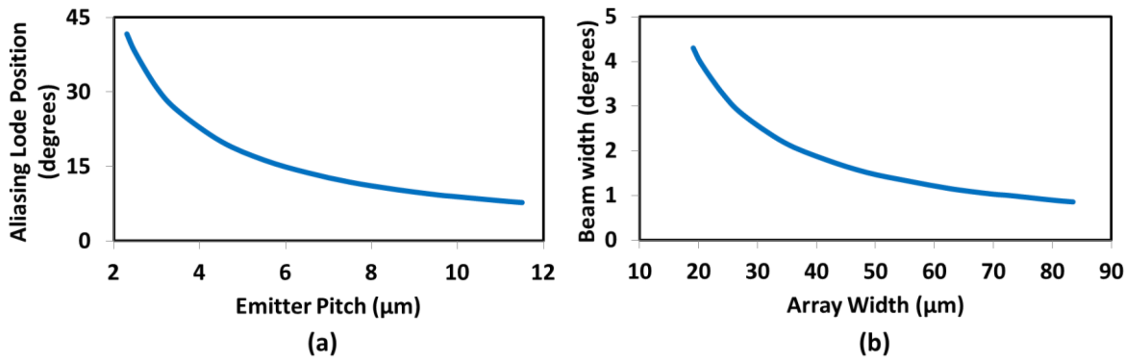

Figure 41. (a) Calculated far field separation between main lobe peak and side lobe base (i.e. where the side lobe rises above -10 dB relative to the main lobe peak) vs. emitter pitch. (b) Calculated far field beam width vs. total array width. Values are chosen using an 8-channel array but are very similar when using other channel number values. This is calculated for operation at 1.55 μm.

The beam FWHM scales inversely with the total width of the OPA. Changing the emitter pitch has almost no effect on the number of resolvable spots because as the FWHM decreases, the FOV will also decrease. However, increasing the number of output channels will increase the array width without increasing pitch, and thus give a wide FOV with a narrow beam width. Thus, using a large number of channels with a small pitch is ideal for the OPA output in a uniformly spaced array.

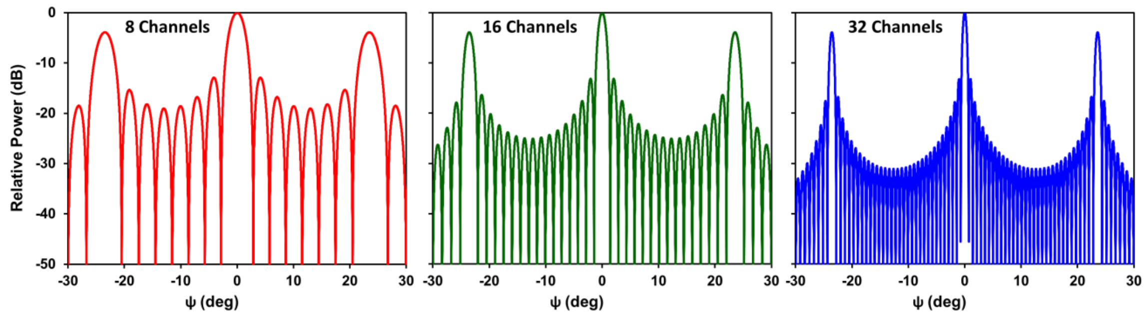

Figure 42. Calculated far field emission for a uniform OPA with 8, 16 and 32 channels, showing narrowing beam width with increasing channels.

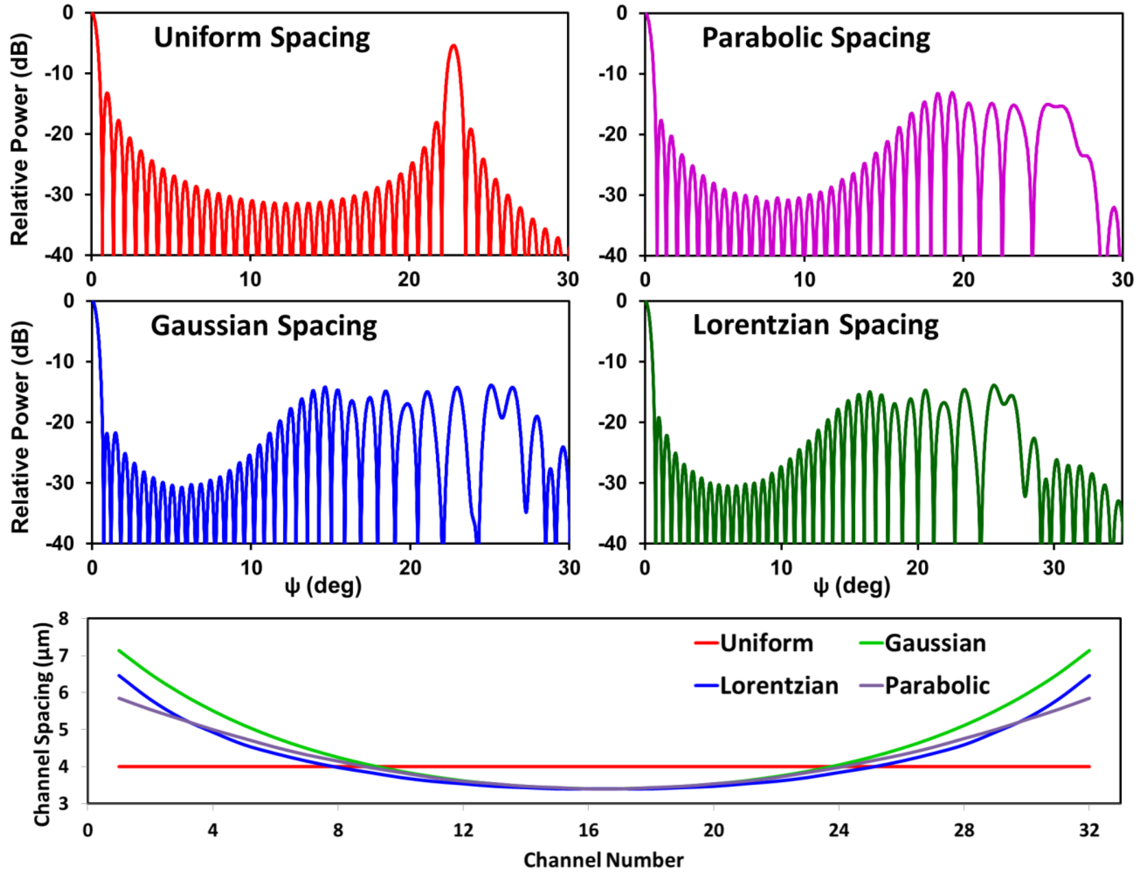

Figure 43. Calculated emission from OPAs with different emitter spacing. The uniform array uses 4 µm spacing, while the parabolic, Gaussian, and Lorentzian spaced arrays start with 3.4 µm center spacing and increase according to the described function.

There are other non-uniform emitter spacing configurations that should be considered as alternatives to the uniformly spaced array. Several possible configurations based on common functions are shown in Figure 43. The benefit of an alternative spacing function is the reduction in power in the aliasing lobes. However, as the power in the aliasing modes is lowered, that power is shifted into the side lobes. Thus, the main lobe can be steered over a wide range, but the SMSR is not very large. Even better side lobe suppression can be achieved with an optimized semi-random spacing between channels, but it should be noted that this requires non-linear phase shifts between channels to steer the beam which adds

complexity to the tuning algorithm. However, a look-up table can be implemented to store the settings for all desired angles of any spacing configuration.

3.3 Phase I

This section is included for completeness, but it should be noted that the design and testing of the first phase were performed primarily by Jonathan Doylend.

Design

The first phase of the beam-steering project has a relatively simple design and was intended as a proof of concept. An off-chip tunable laser capable of tuning from 1525 to 1625 nm is fiber-coupled onto the chip where it is split into 16 channels with a tree of 1x2 MMI splitters. Each channel is equipped with a resistive thermo-optic phase tuner overlaying the waveguide, separated by a layer of SiO_2 to prevent absorption losses.

The goals for this phase of the project include a steering range of 20˚ with the OPA (ψ) and 10˚ through wavelength steering (θ), a FWHM beam-width less than 2˚ in both axes, and a side lobe suppression ratio greater than 10 dB within the field of view. This can be achieved with any array of 10 x 5 resolvable spots and the use of lenses, but we would like to reach this goal with an unpackaged chip.

For a 20˚ FOV excluding aliasing lobes with greater than 10 dB SMSR over the wavelength range of the tunable laser, the maximum emitter pitch is approximately 4.2 μm. A pitch of 3.5 μm was chosen for this phase, which should allow the FOV to be as wide as 23˚ when the beam width is 2˚. To achieve this beam width, the total array width must exceed 35 μm, which for this emitter pitch means 10 channels. Since an MMI tree is being used, the number of channels should be a power of 2, thus 16 is the number of channels

selected. Conveniently, that also corresponds with the number of channels available in our ILX laser driver controller used to interface with the device.

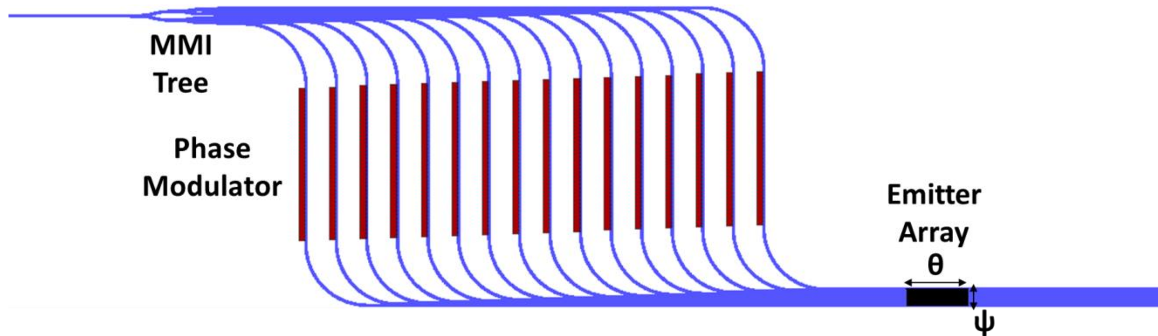

Figure 44. Layout of the first phase of the beam-steering device.

The emitter design used a 1 μm wide rib waveguide etched to a depth of 280 ± 20 nm. The surface gratings were chosen to have a pitch of 600 nm with a duty cycle of 50%, an etch depth of 75 nm and a total length of 200 μm. The shallow etch depth of the grating reduces the coupling strength of each tooth, allowing the beam to be emitted over a longer range which reduces the width of the beam in θ. See Chapter 5 for details on the fabrication process.

Characterization setup

To measure the beam in the far field an aspheric lens with high numerical aperture (NA = 0.83, effective focal length = 15 mm) was used in conjunction with two other lenses with focal lengths of 180 mm and 60 mm. They both magnified the beam and imaged the far field to the Fourier plane. To switch from far to near field images the 180 mm lens was placed in a rotating mount so it could be easily removed. A polarization controller was also placed in the lens tube to ensure that any TM light scattered off the chip would be filtered out. The lenses focus the beam onto an infrared camera with 320 x 256 pixels set at 25 μm pitch. With the lens tube normal to the surface of the chip, the far field resolution is 0.3° with

maximum measurable angles of 39° x 33° (θ x ψ). This system will be referred to as the Fourier imaging system. A schematic of the setup can be seen in Figure 45. A second setup in conjunction with test grating emitters was used to calibrate the Fourier imaging system. For this calibration a large-area detector (Newport 818) was mounted on a motorized stage (Newport ILS PP150) at a distance of 14.7 cm from the surface of the PIC, which is a sufficient distance to be far field. This setup will be referred to as the beam profiler setup.

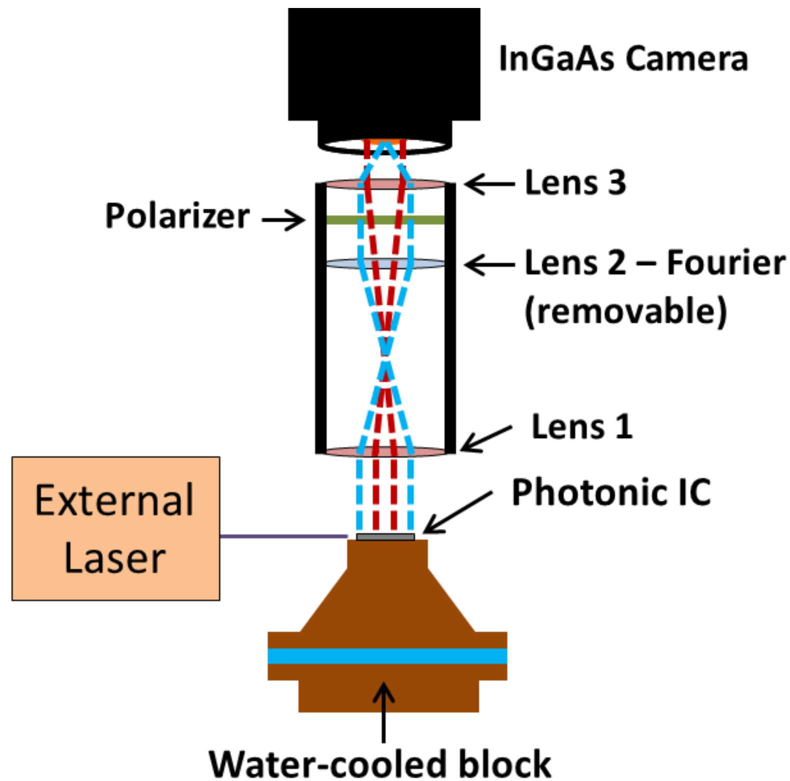

Figure 45. Schematic of Fourier imaging setup used to characterize near and far field emission. Red and blue dotted lines show the near and far field imaging respectively [11].

The calibration was done using a test grating with 600 nm pitch. The grating emission was measured with both the beam profiler and the Fourier imaging setup. These results, along with similar measurements from a 16 channel array, are shown in Figure 46. The

tuning efficiency in θ was measured to be 0.14 ±0.01 ˚/nm across the 100 nm wavelength range. This matches well with simulation, although the absolute angle was off by 4˚ which is attributed to non-ideal etch profiles.

It is clear that the Fourier imaging setup is a good design for testing these devices and it will be used exclusively in the future for this project.

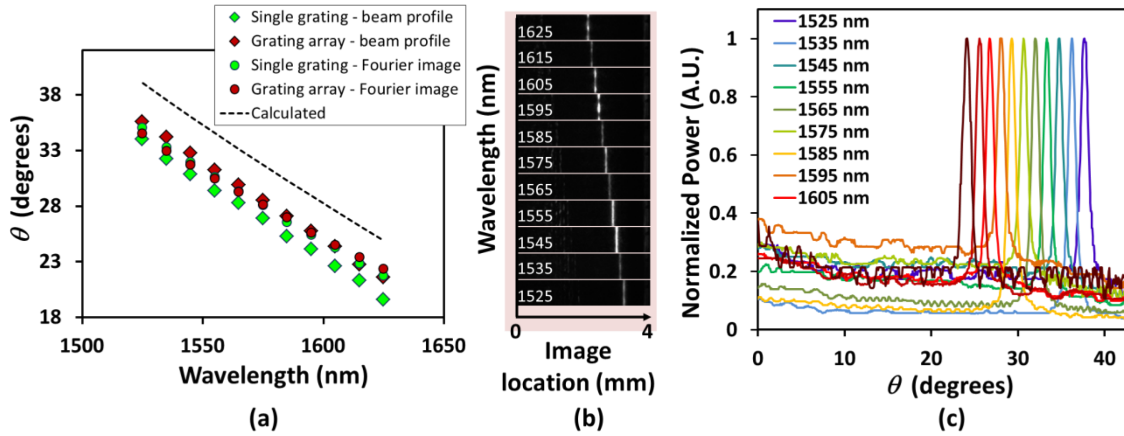

Figure 46. (a) Plot of the angle in θ in the far field measured using a single grating (green) and a 16-channel grating array (red). Both the beam profiler and Fourier imaging system are shown, with the calculated beam angle from the Bragg equation shown with the dotted line. (b) Images in the far field using the Fourier imaging setup of the beam angle θ for wavelengths in the range of the tunable laser. (c) Normalized angular output in the far field measured with the beam profiler.

Phase tuning

The lateral beam angle ψ can be actively adjusted with a linear phase shift between adjacent channels, as described in Equation 17. There will also be phase errors from path length differences between channels that need to be resolved before a linear phase shift is introduced. To allow for active tuning of each channel, a resistive heater was placed near the waveguide. The heater was 580 μm in length and 10 μm in width. The metal stack consisted of four layers of Ni/Cr 125/60 Å (Appendix D). The phase tuning efficiency of an individual heater element was measured using a Mach-Zehnder interferometer, and was found to be

215±15 mW/π. The resistance was 65±5 Ω, allowing a 2π phase shift with under 6 V. To control all 16 channels, an ILX 3916 laser driver array was used, with modulation inputs driven by a National Instruments analogue output data acquisition unit. This allowed for rapid changes in driving current for quick optimization of the beam.

Thermal simulations were performed to determine the temperature change at a variable distance from the heater (Figure 47). The temperature change is shown as a percentage of the temperature change of the waveguide under the heater. Even with waveguides spaced at 50 μm there is more than 10% temperature change in neighboring waveguides which suggests significant thermal cross-talk will be present.

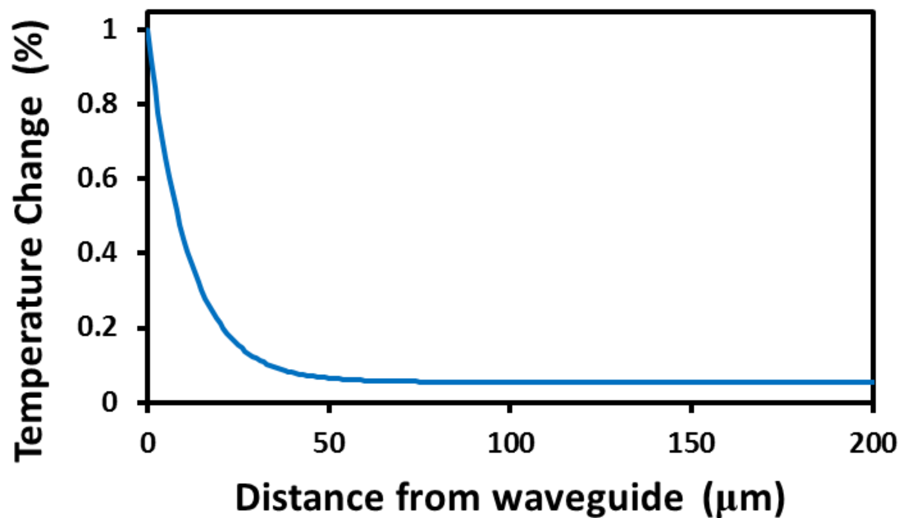

Figure 47. Percentage of temperature shift on the top silicon layer at a variable distance from the heated waveguide.

Thermal crosstalk between channels makes linear phase shifts much more difficult to achieve, so measurements were taken to experimentally determine the level of crosstalk. First, the resistance of the thermal tuners with respect to temperature was measured by slowly heating the chip with a thermoelectric cooler (TEC). Next, the resistance of each channel was measured to ascertain the temperature change caused by power dissipation from

a single heater in the middle of the array. During this test 15 of the 16 channels were dissipating 30 mW while channel 9 was dissipating substantially higher amounts. It can be seen in Figure 48 that there is significant crosstalk which will make optimization much more difficult. This matches the trend we expect from simulation.

Although the thermal cross-talk will be problematic, we still choose to use thermal tuning on this device for simplicity. Heater fabrication is much simpler than alternative methods of phase tuning which require doping or III/V processing.

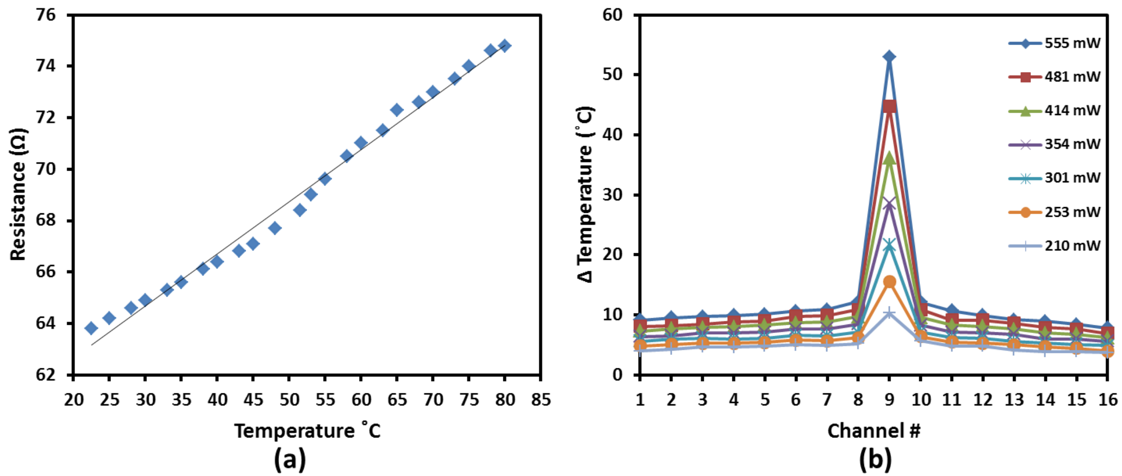

Figure 48. (a) Plot showing resistance change with temperature for thermal tuners. (b) Plot showing temperature change in each channel while dissipating 30 mW in all channels except channel 9.

Integrated PIC

Images of the phase tuning section and the grating array can be seen in Figure 49. It is clear from Figure 48 that there is significant crosstalk between channels, suggesting the need for either a thermal blocking layer or an alternative method for phase tuning. The level of crosstalk also makes applying a linear power difference between channels an unreliable method for steering the output beam. Instead, a hill-climber algorithm was used to optimize the beam angle. The algorithm used a parameter R, where R is the ratio of power $P(\psi_0,\theta_0)$

measured within a specified beam width of the desired angle to the total power $\int P(\psi,\theta_0)d\psi$ measured within the field of view. The parameter $R(i,\psi,\theta)$ was determined by using 5 closely spaced drive currents for a given channel and measuring the ratio at each point. Then $\delta R/\delta i$ and $\delta^2 R/\delta i^2$ were determined using a polynomial fit, and the current was adjusted up or down by 0.2, 1 or 2 times a specified step size. The 0.2 step was used instead of 0 to prevent the algorithm to repeatedly keep the same settings. This process was repeated for each channel continually until a desired SMSR was achieved. In this way, phase tuning solutions were put into a look up table (LUT) for 1 degree spacing with 10 dB SMSR for a field of view of 14˚ (θ) by 20˚ (ψ). Fewer than 100 iterations of each channel were required to create this solution. The speed was limited by a 60 Hz refresh rate from the IR camera, making an iteration through the 16 channel array require 1.3 seconds, or a total of 130 seconds to solve for a point. Many of the points required far less time to converge. Once placed in the LUT, each point could be pointed to arbitrarily without the need to iterate through the algorithm again. Plots of the output in ψ for optimized and non-optimized tuning are shown in Figure 50. The measured FHWM beam width along ψ was 1.6˚, and the beam width in θ was 0.7˚. Plots of the beam profile in ψ tuned across the field of view in 1˚ increments can be seen in Figure 51. Three dimensional plots are shown in Figure 52 for the center and the limits of the field of view in both axes.

This result shows the great potential of this method of beam-steering. There are 20x12 resolvable spots using this device. However, this still uses an off-chip laser. The next iterations will attempt to integrate a laser. This will reduce packaging time and costs and make the production of these devices more scalable.

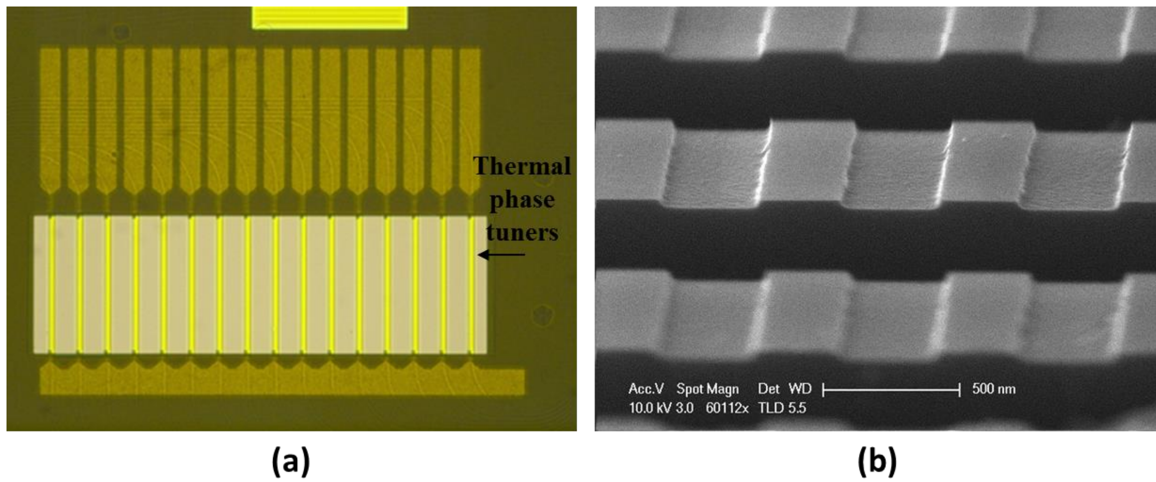

Figure 49. (a) Optical microscope image of the phase tuning section of the PIC. (b) SEM image of the output grating array.

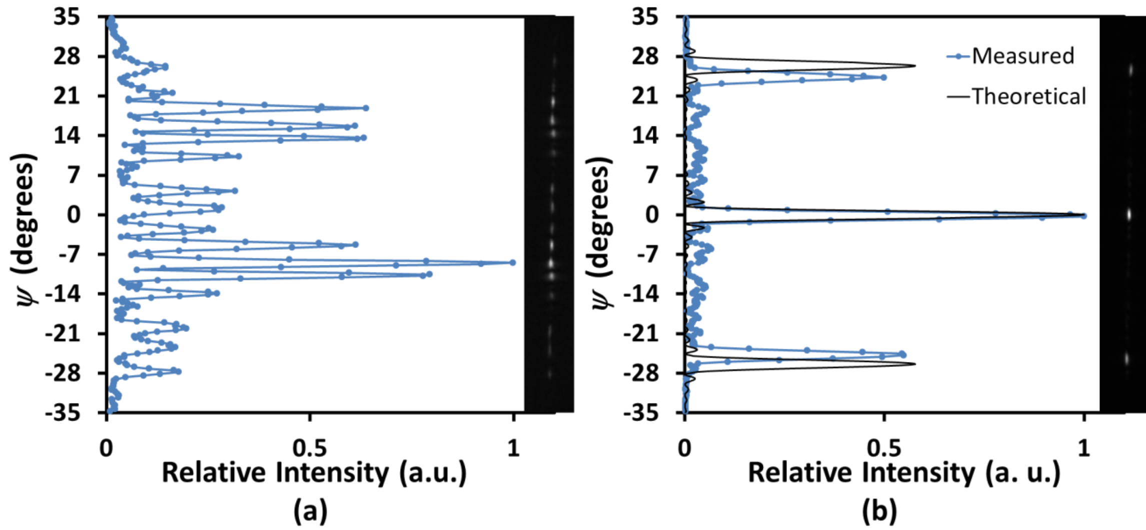

Figure 50. Beam profile in ψ axis (a) without phase tuning and (b) with phase tuning optimized at 1555 nm. The discrepancy of 2˚ between measured and calculated aliasing lobes is attributed to lens Seidel aberrations.

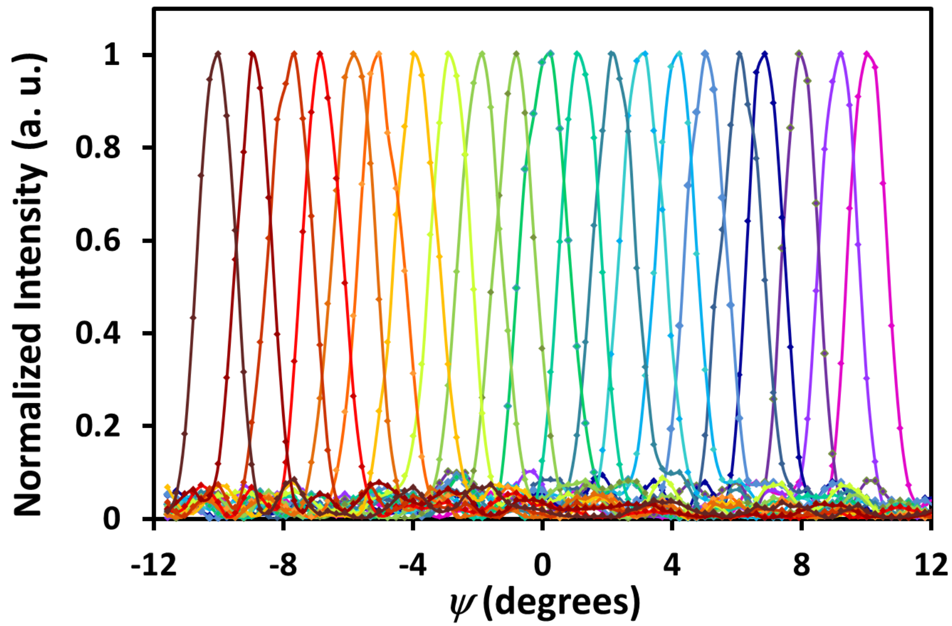

Figure 51. Measured beam profiles in ψ across the field of view in 1° increments at 1555 nm.

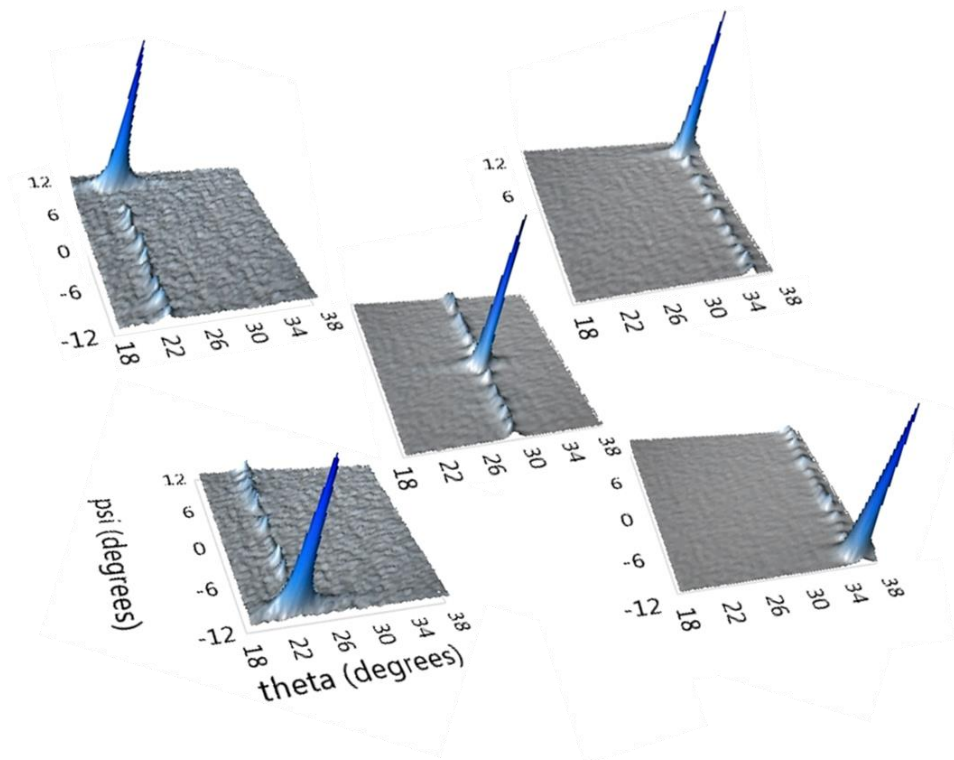

Figure 52. Plots of the beam intensity in two dimensions for the center and the limits of the field of view. Total beam steering is 14° (θ) by 20° (ψ) with

beam widths of 0.7° (θ) by 1.6° (ψ). The channel phases were taken from the LUT.

3.4 Phase II

Design

The goal of the second phase beam-steering chip was to include the integration of an on-chip laser, and to reach a steering range of 12° with a beam width not exceeding 2°. In practice, lens optics can expand both the range and the beam width, so the true goal is for a 6x6 grid of resolvable spots with a SMSR of 10 dB. This is pertinent because the steering range from an on-chip laser is reduced from that of an off-chip source. The reduced goal in steering range from Phase I (which was 20°) was due to the increased complexity of this device and the desire to add amplifiers on each channel.

To achieve a 12° steering range with 2° beam width, the aliasing lobes must be more than 14.8° away from the main lobe to achieve 10 dB SMSR. The channel spacing then must not exceed 6.5 μm. For extra tolerance a channel spacing of 5.5 μm was chosen. For a beam width <2° the total array width must be >35 μm, which for this channel spacing requires a minimum of 7 channels. For a binary MMI tree this rounds up to 8 channels. This allows us to continue using the same 16-channel ILX driver (8 phase modulators and 8 amplifiers). The output grating design used is identical to that in the first phase of this project and is expected to perform similarly.

In additional to an on-chip tunable laser, amplifiers were added to mitigate any channel dependent losses from the MMI tree or the phase modulators, and to boost the total output power. The phase modulators were also redesigned to enable electro-optic tuning. The layout of the PIC can be seen in Figure 53.

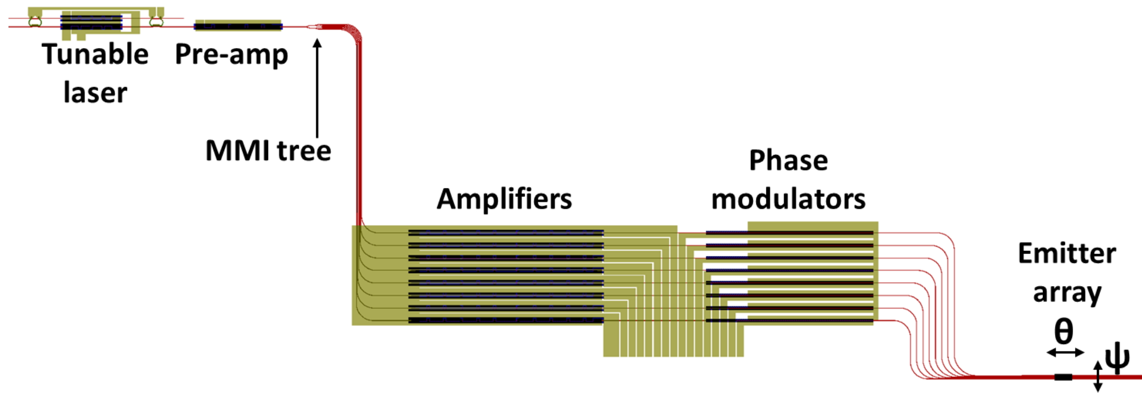

Figure 53. CAD layout for phase two beam-steering PIC.

Laser and amplifiers

The laser used in this chip is identical to the first iteration of the Vernier ring laser (first iteration) described in [14] and Chapter 2, with 5 mW output power, <340 kHz linewidth, >45dB SMSR, and a wavelength tuning range of 40 nm (1561 to 1601 nm). With the measured tuning efficiency of 0.14°/nm this corresponds to a longitudinal (θ) steering range of 5.6 degrees. Unfortunately, the on-chip laser within this integrated system was not tunable due to faulty tuner probe pads.

The semiconductor optical amplifier (SOA) uses the typical gain design described in Chapter 2, but with a rib waveguide width of 2.5 µm and a length of 2.3 mm. The increased width confines the mode more in the waveguide causing a lower confinement factor in the quantum wells. This allows for higher saturation output power. The pre-amplifier is only 1 mm long with a 2 µm rib width for higher gain/mm. Epi E (Appendix B) was used for the gain elements on this chip.

Phase modulator

The phase modulators used a *p-i-n* diode structure with the intrinsic region running through the lower half of the waveguide, as shown in Figure 54. Two versions of this

modulator were explored where the separation between *p* and *n* doping regions were 11 µm (type 1) and 6 µm (type 2).

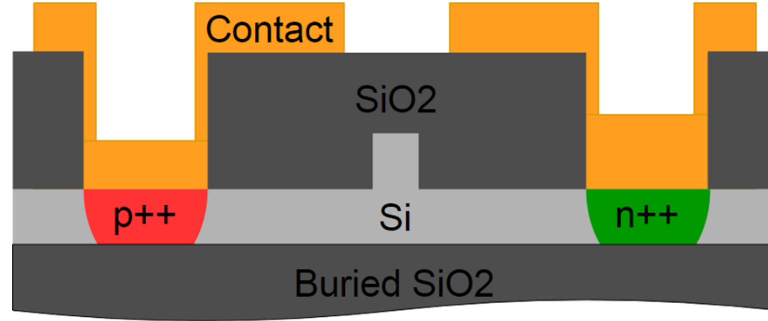

Figure 54. (a) Cross section of silicon phase modulator design.

The type 1 phase modulator was highly resistive and so was dominated by thermo-optic tuning. The large resistance allowed for significant power dissipation with minimal carrier density within the optical mode, thus preventing phase-dependent loss due to free-carrier absorption. However, the phase modulators heated the chip to the point that SOA gain was reduced. So although there was negligible free-carrier absorption, there was still phase-dependent loss, removing one of the main advantages of thermo-optic tuning.

The dopant profile and the current-voltage characteristics were simulated using Silvaco ATHENA and ATLAS software packages respectively. The carrier lifetime within the waveguide was assumed to be 0.9 ns based on data in [19]. Thermal tuning is expected to follow Equation 18, where λ is wavelength, σ = 1.35x10^{-2} W cm^{-1} K^{-1} [20] is the thermal conductivity of the buried oxide, w is the effective width where the heat is being dissipated, t = 1 µm is the thickness of the buried oxide, and dn/dT = 1.86x10^{-4} K^{-1} [21] is the thermo-optic coefficient of the silicon. The thermal efficiency is predicted to be 57 mW/π.

$$P_{\pi} = \frac{\lambda \sigma w}{2t \frac{dn}{dT}}$$ **Equation 18**

Expected phase tuning and expected free-carrier induced loss are shown in Figure 55 along with the measured transfer function of a Mach-Zehnder interferometer test structure. The effective carrier lifetime in the phase modulators were estimated using the current-voltage characteristics, and was determined to be 1.9 ns instead 0.9 ns. Calculations of carrier densities suggest a free-carrier induced loss and phase shift of 0.75 dB and -0.8 radians respectively at 100 mW of dissipated power. Free-carrier effects will be discussed further with the type 2 modulator.

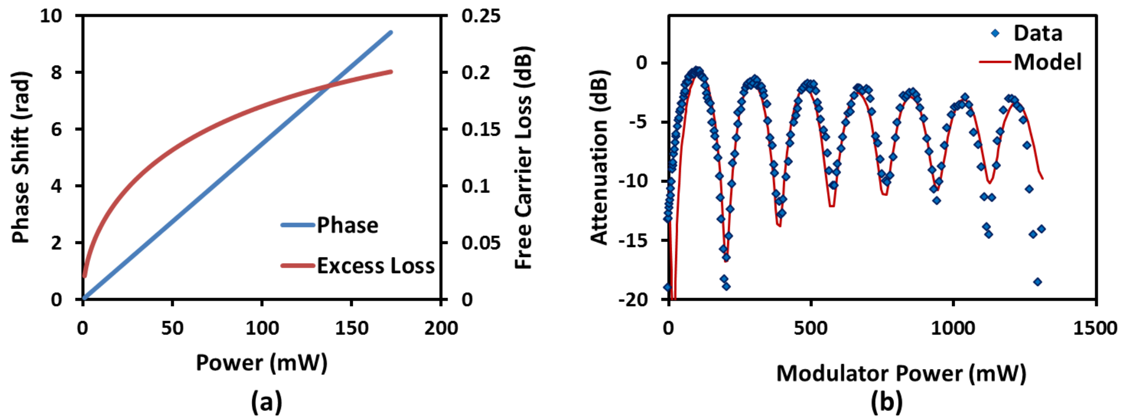

Figure 55. (a) Predicted thermo-optic phase shift and free-carrier absorption induced excess loss vs. dissipated power. (b) Transfer function for a Mach-Zehnder interferometer with thermo-optic phase tuner. The fitted curve is calculated using the measured phase tuning efficiency and the free-carrier absorption loss (calculated from effective carrier lifetime).

The type 2 phase modulator was explored as a way to use plasma dispersion for phase tuning without crosstalk and with increased modulation speeds. The plasma dispersion effect is based on the free carrier density in the silicon. The relation between carrier density, change in index of refraction, and change in absorption can be seen in the Drude-Lorenz equations.

$$\Delta\alpha = \frac{e^3\lambda_0^2}{4\pi^2c^3\varepsilon_0 n}\left(\frac{\Delta N_e}{\mu_e(m_{ce}^*)^2}+\frac{\Delta N_h}{\mu_h(m_{ch}^*)^2}\right) \qquad \textbf{Equation 19}$$

$$\Delta n = \frac{-e^2 \lambda_0^2}{8\pi^2 c^2 \varepsilon_0 n} \left(\frac{\Delta N_e}{m_{ce}^*} + \frac{\Delta N_h}{m_{ch}^*} \right) \qquad \textbf{Equation 20}$$

The index of refraction in silicon increases with increasing temperature (scales approximately as current squared) but decreases with carrier injection (scales approximately linearly with current). So for lower bias currents the plasma dispersion effect dominates, and the device is dominated by thermal effects at higher currents. It should be noted that carrier injection switching speeds are much faster than thermal switching speeds.

Due to time constraints the type 2 modulator was fabricated on a silicon chip without III/V bonding and processing. The transfer function of a Mach-Zehnder interferometer along with the modulation response is shown in Figure 56. The fitted curve was calculated using thermal tuning efficiency in conjunction with the calculated index and absorption shifts due to plasma dispersion. A 3dB bandwidth of 40 MHz was measured. This high speed will allow rapid tuning of the optical phased array for fast beam-steering.

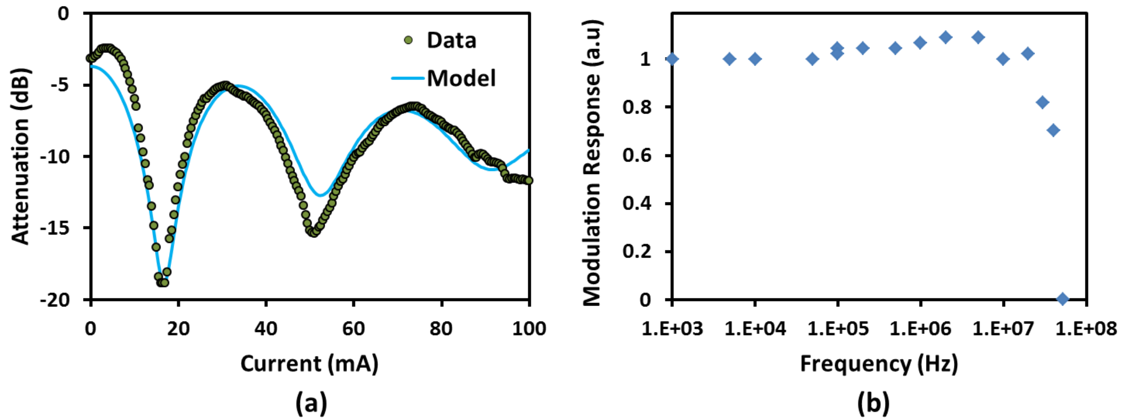

Figure 56. (a) Transfer function for a Mach-Zehnder interferometer with a carrier injection based modulator (type 2). The fitted curve is calculated using the measured phase tuning efficiency, thermal tuning efficiency and the free-carrier absorption loss. (b) Modulation response of type 2 phase modulators.

Integrated PIC

The integrated PIC for the second phase was characterized using the Fourier imaging system and the hill-climber optimization algorithm described in Phase I, although this time with only 8 channels. The powers from individual channels were equalized by individually observing them and using the SOAs to compensate for any discrepancies. It was found that channel 5 was faulty, limiting the output channel number to seven and the maximum possible SMSR within the field of view to 8.3 dB.

The gain of the SOAs was limited by significant heating of the chip and was found to be highly dependent on the phase tuning of the type 1 phase modulators. To mitigate this effect the SOA and phase modulator drive currents were cycled at 125 Hz with 20% duty cycle. During the ramp up time, as the SOAs and modulators stabilized, the pre-amplifier was switched off to avoid non-optimized far-field contamination of the signal. The beam was blanked for 800μs and switched back on for the remaining 800 μs, giving a 125 Hz beam with 10% duty cycle. The chip was mounted on a chuck held at 18˚C.

Beam steering in the far field of ±6˚ with 1˚ spacing was measured in the lateral direction (ψ) for a single wavelength. As mentioned earlier, the ring tuning pads on the laser were faulty and prevented tuning across a large range. However, with an identical laser, 40 nm of tuning was measured, which corresponds to 5.6˚ of lateral (θ) beam-steering in the far field. The beam width was measured to be 1.8˚ in ψ and 0.6˚ in θ. This corresponds to 7 x 9 resolvable spots. Plots of the beam cross-section can be found in Figure 57. Plots showing 12˚ of beam-steering in ψ can be seen in Figure 58.

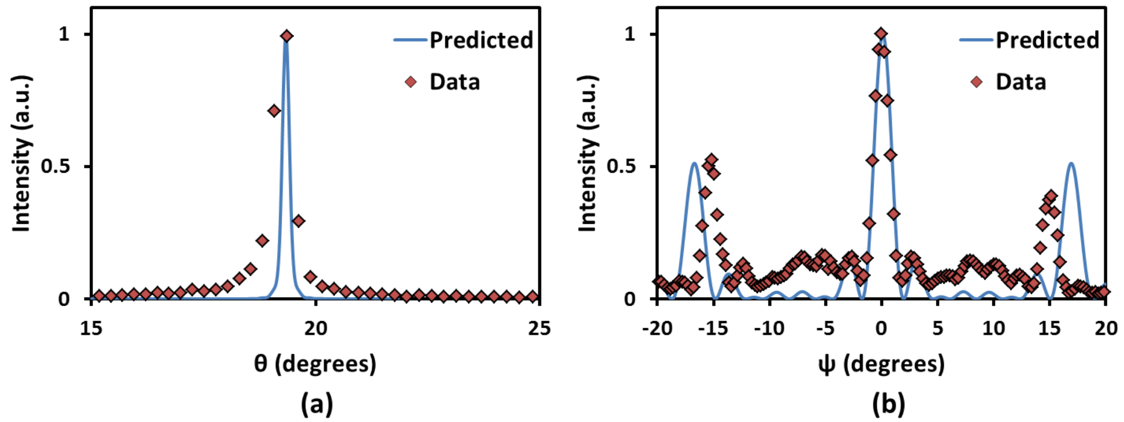

Figure 57. Beam profiles in (a) the longitudinal (θ) and (b) the lateral (ψ) directions for both predicted and measured values.

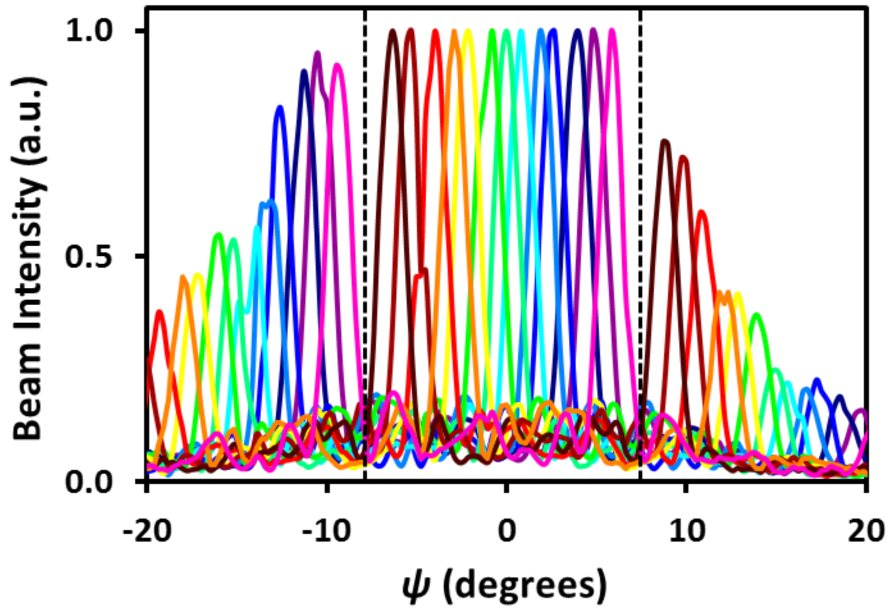

Figure 58. Beam profiles measured in the far-field with 1˚ spacing across the field of view (±6˚) in ψ. Dotted lines show the extents of the field of view.

Although the beam output power varied while tuning across the field of view, the power difference was able to be compensated by varying the pump current of the pre-amplifier. The relative beam powers vs. steering angle for a fixed pre-amplifier pump current, and the relative beam power vs. pre-amplifier pump current is shown in Figure 59.

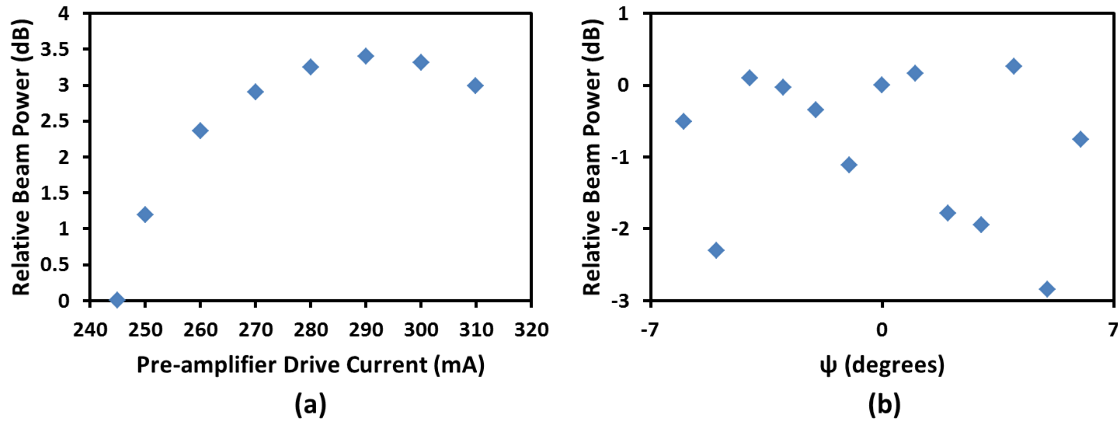

Figure 59 (a) Relative beam power vs. pre-amplifier drive current showing 3.4 dB possible power compensation. (b) Relative beam power vs. steering angle for a fixed pre-amplifier drive current showing 3.2 dB variation.

Beam power in the far field was measured with the beam profiler setup to be 4.1μW. The far-field SMSR and linewidth were measured by steering the beam to a fiber collimator and reading the output on a high resolution optical spectrum analyzer (APEX 2051A). The linewidth was measured to be 36 MHz and the SMSR was 30 dB. The spectra of the output from the PIC are shown in Figure 60.

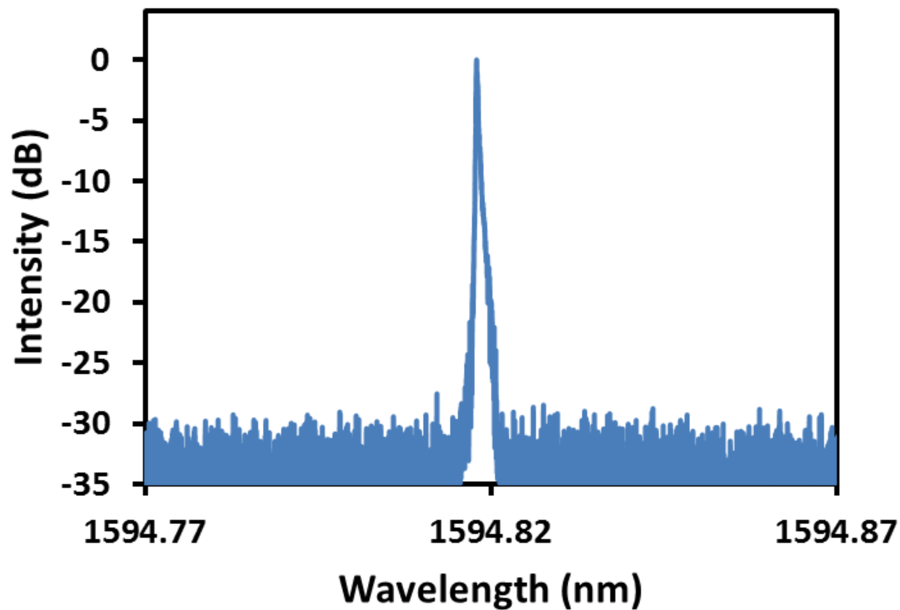

Figure 60. Spectral data of the output from the integrated PIC.

A second chip was fabricated during this phase to determine the suitability of the type 2 modulators. This was done without on-chip lasers or amplifiers, but steering in the lateral direction was still performed using an 8 channel array. Switching speeds of 31 MHz were demonstrated, leading to beam-steering speeds of $3.7\text{x}10^8$ °/s. In addition to greatly increasing the speed of tuning, the type 2 modulators also reduced the necessary phase tuning power to below 25 mW/channel. This reduced crosstalk to the point that the beam was able to be steered analytically instead of by use of a look up table. Optimization for a starting angle (ψ) is necessary for each wavelength, but all additional angles can be calculated by applying an additional linear current difference between channels.

3.5 Phase III

Design

The third phase of the beam-steering project had metrics of >20dB SMSR, tuning speeds greater than 4 x 10^6 °/sec, beam widths of <1° FWHM in both axes, and a 12° x 6° steering window, which translates to 12 x 6 resolvable spots. In addition, integrating some form of on-chip feedback was desirable.

To achieve a beam-width of 1° the total width of the output array must be >73 μm. In order to increase the array width without increasing the emitter pitch and thus decreasing the FOV we must add more channels. To achieve these metrics, 16 channels at a pitch between 5 μm and 6.5 μm is sufficient. However, due to a desire to push the boundaries of integration on this platform, as well as to increase the number of resolvable spots as much as possible during the final phase, a channel count of 32 was selected. Also, a Gaussian channel distribution was selected to reduce aliasing lobes (Figure 43), with a center channel spacing of 3.4 μm and a total array width of 144 μm. However, even though the aliasing lobes are reduced to < 10 dB at 0° steering, they increase as the steering increases. Thus, the expected FOV for this configuration is not arbitrarily large, but closer to 22°.

The PIC was designed with a redundant Vernier ring laser and pre-amplifier to improve yield. One of the lasers only used a single gain section to reduce loss from the III/V taper and to reduce the threshold current (see the Vernier ring laser second iteration in Chapter 2). A 5 stage MMI array split the light into 32 channels after which each channel experiences phase modulation and amplification. Then the channels were brought into the output array spacing.

The emitters consisted of waveguides that were etched to a depth of 260 ± 20 nm, with surface gratings etched to 50 ± 10 nm. The grating pitch was 550 nm with a duty cycle of 50%, and a total length of 200 μm.

After the output emitter array, the waveguides feed into a 1 dimensional graded index (GRIN) lens which images the far-field onto a photodiode array for on-chip feedback of power and the lateral angle (ψ). A schematic of the full PIC is shown in Figure 61.

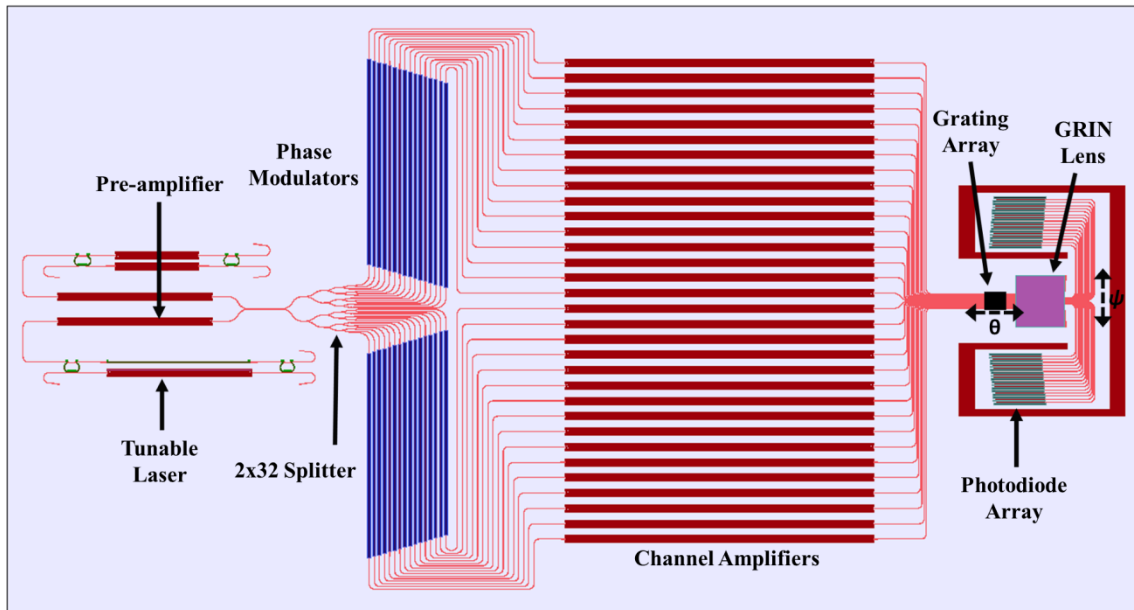

Figure 61. Layout of the fully integrated beam-steering PIC.

Phase modulator

The phase modulator selected for this device was the type 2 modulator explored during Phase II. However, the III/V processing steps, which were not present when first fabricating these modulators, significantly added to the phase modulator resistance. Consequently, the index shift was dominated by thermal dissipation and not carrier injection. Resistance and power dissipation vs. current can be seen in Figure 62. It is clear that phase shift is more heavily dependent on power dissipation, although the plasma dispersion reduces the

efficiency of the thermal tuning. Tuning efficiency was measured to be 160 mW/π, which is worse than both type 1 and type 2 as measured in phase II.

The cause of such high resistance in the phase modulators is attributed to large contact resistance, as well as possible damage to the trench region around the silicon rib. The contact metal for these modulators was deposited after the majority of the III/V processing which left the doped silicon more easily damaged. This delay was included to avoid bonding failure between the silicon and the III/V. For best bonding both surfaces must be flat and metal deposition could easily cause widespread failure. However, it is possible that depositing a thin layer of contact metal within the etched silicon trench prior to the bond would allow for good contact resistance and good bond yield. See Chapter 5 for more details on the process.

There was 97% yield for the phase-modulators.

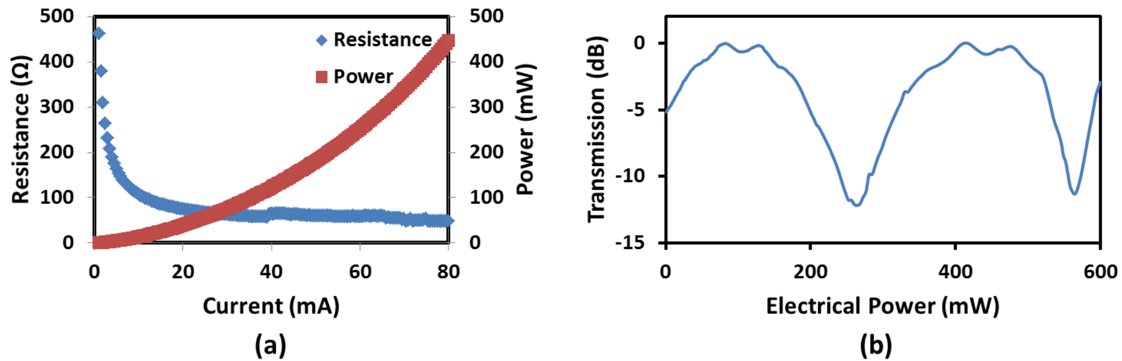

Figure 62. (a) Phase modulator resistance and power dissipation vs. current. (b) Transmission vs. power dissipation for a Mach-Zehnder interferometer test structure. Clear dependence on power is shown.

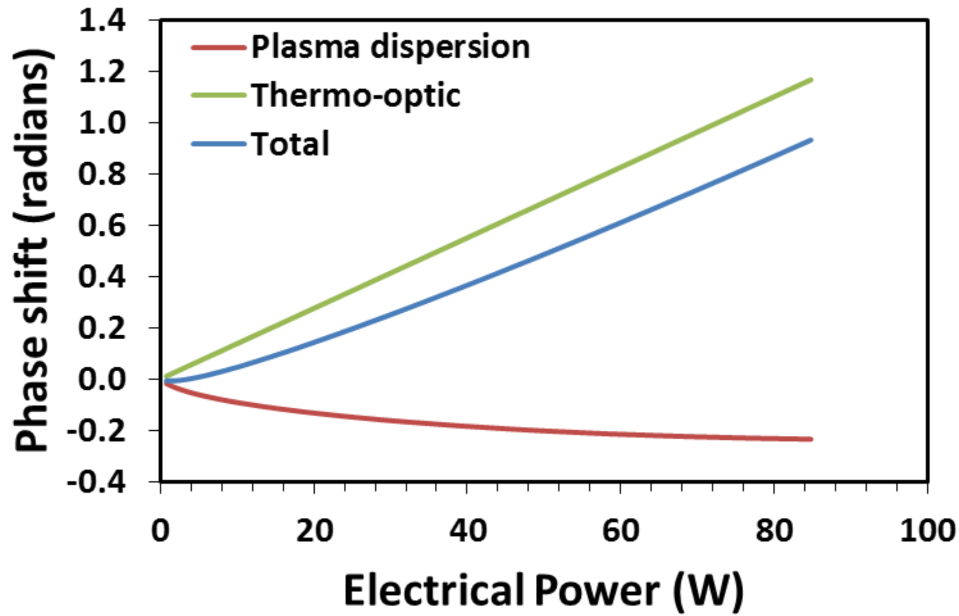

Figure 63. Calculated phase shift for plasma-dispersion and thermo-optic effects based on MZI fitting and IV data.

Lasers and amplifiers

The measurements of the integrated PIC used a Vernier ring laser (VRL) second iteration (Chapter 2). The gain section was 1350 μm long. The threshold current of this device was 94 mA, and the threshold for the dual-gain device (VRL first iteration) was 168 mA. The epi used for these devices was Epi-E (Appendix B).

The laser output power was not able to be measured directly as a facet was not provided. This was to minimize reflections back into the laser cavity. However, the wavelength of light for different ring tuning was measured using a lens above the laser that collected scattered light into a fiber. The tuning range is shown in Figure 64 as spectra and vs. single mirror power, and the measured and expected angle vs. single mirror power is shown in Figure 65. Tuning of 34 nm was demonstrated. The wavelength shift was linear with ring heater power as expected, and the output angle closely matched the predicted angle (based on the measured wavelength).

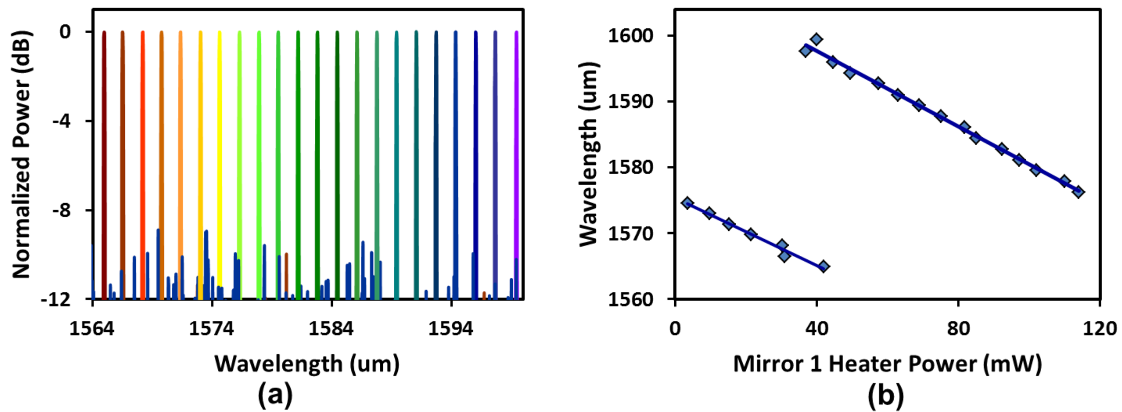

Figure 64. (a) Measured laser tuning across 34 nm range. (b) Measured wavelength vs. single mirror tuning power.

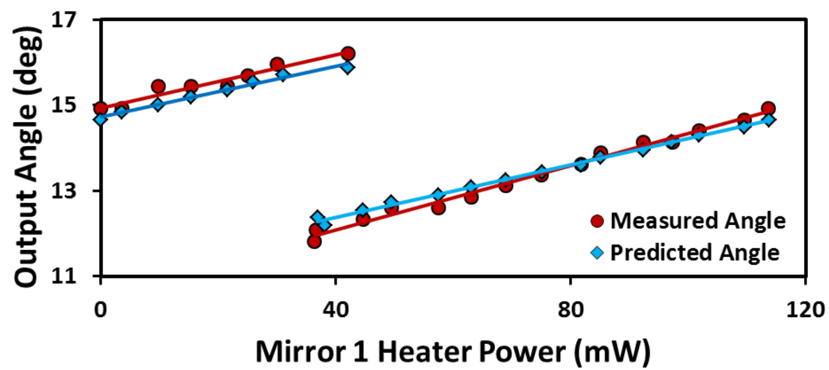

Figure 65. Measured and predicted angle vs. single mirror tuning power.

The pre-amplifier was 1.5 mm long and was placed after the laser to amplify the total signal before the 32 channel splitter. Each of the channel amplifiers was chosen to be 3 mm in length to maximize the total output power. In retrospect, the channel amplifier length was excessive and caused problems. Amplified spontaneous emission from such a long device reduces the signal to noise ratio (SNR). This was only exacerbated by the on-chip heating generated from the amplifiers and the phase modulators, which also significantly reduces gain. Images of the laser and amplifiers can be seen in Figure 66.

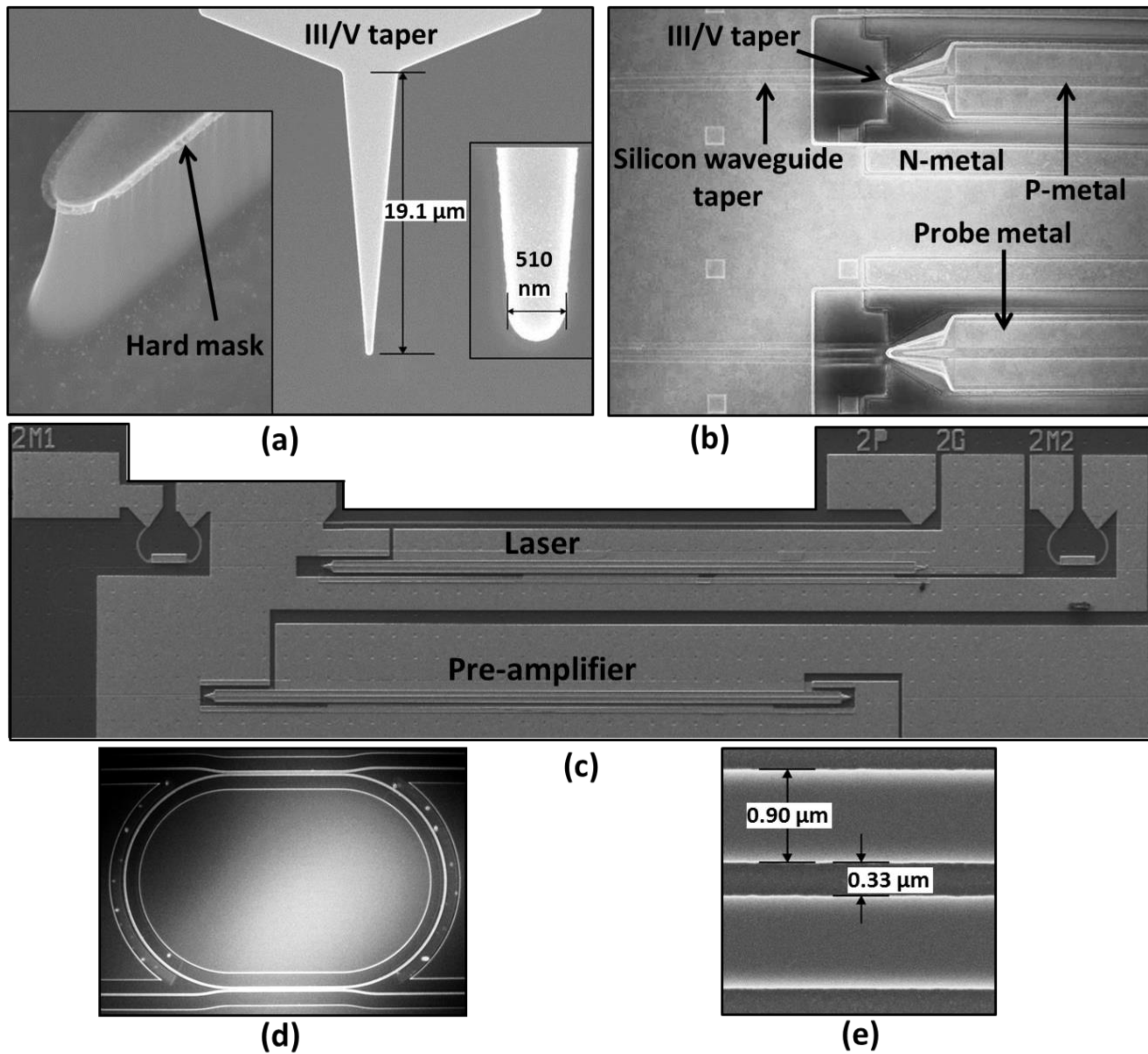

Figure 66. SEM images of (a) III/V tapers immediately after etch definition used for adiabatic transitions between silicon waveguides and III/V. High magnification images of the taper tip showing 510 nm width are included; (b) gain elements on the completed chip; (c) Completed laser and pre-amplifier; (d) silicon ring used as a filter and mirror element in Vernier ring laser; (e) high magnification image of directional coupler used in ring filter.

On-chip feedback

When calibrating the chip, a look up table is needed to calibrate out phase differences from path length and other sources, and in the case of a thermo-optic chip to define the settings for every steering angle. However, even with this calibration, fluctuations in

external temperature or degradation of individual components can cause the optimal settings to drift over time. For this reason, an on-chip optical feed-back system was designed.

Following the emitter array, a GRIN lens has been placed to focus the excess light remaining in the waveguide onto another set of waveguides feeding a photodiode array. The lens was designed to have an index profile as shown in Figure 67 (a) such that the output from the lens would focus to a point as illustrated in Figure 67 (b). The index difference was made by etching holes in the top silicon layer with different diameters at a pitch much smaller than the wavelength. The holes were defined using e-beam lithography with proximity correction, etched to a depth of 165 $\pm$ 20 nm, and filled with SiO2. The calculated output power from the lens for a linear phase difference between adjacent channels of a uniform array is shown in Figure 68. The total output waveguide array width is 63 μm. There are 32 photodiodes spanning a 41° field of view in the far field, and giving 1.3° resolution. The focal point of the lens is calculated to be 473 μm.

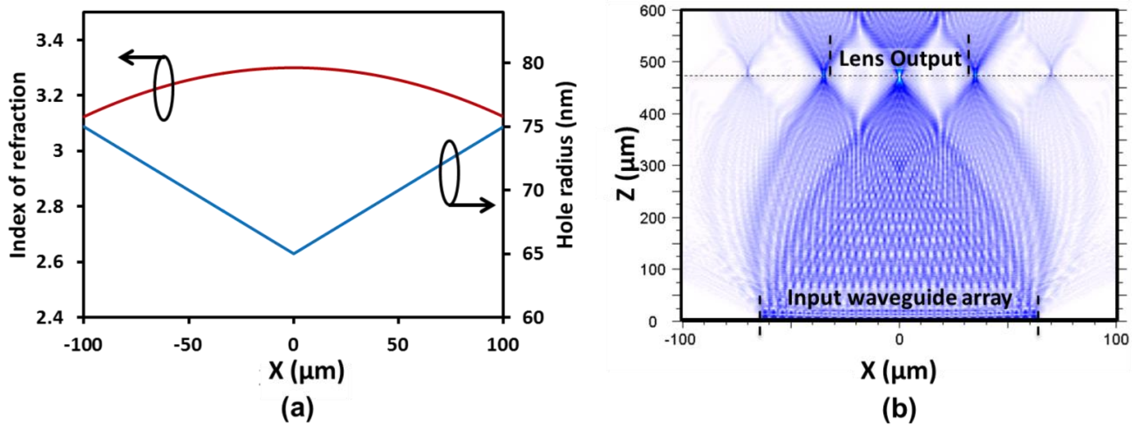

Figure 67. (a) Index profile and etch radius of cross-section of the GRIN lens. (b) Simulated intensity passing through the lens with zero phase shift between channels.

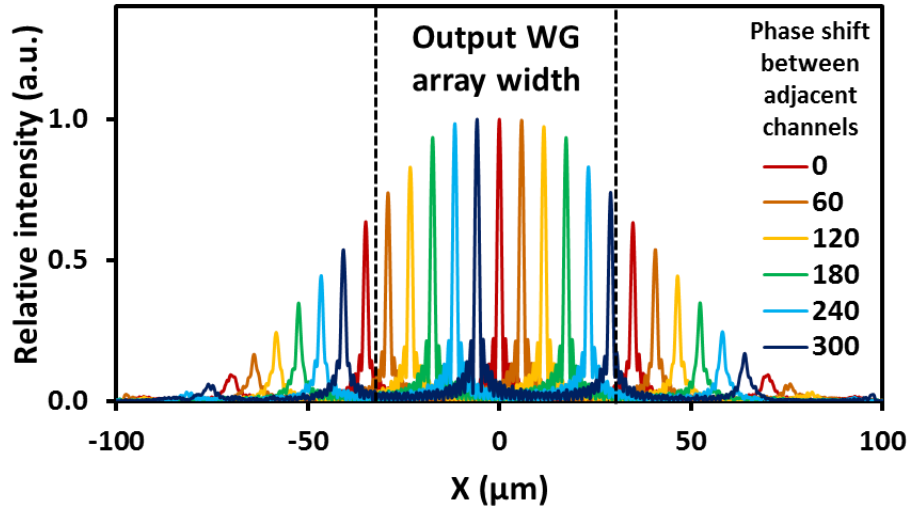

Figure 68. Calculated lens output for different values of linear phase difference between adjacent channels.

The photodiodes designed for this loop were made using the same 7 quantum well Epi-E (Appendix B) as the lasers to avoid processing complications. They were 470 µm long and 9 µm wide and were designed for maximum responsivity rather than speed. On-chip test photodiodes were measured using an external laser. The quantum efficiency and the responsivity are shown in Figure 69. For the wavelengths used in the PIC the average responsivity is 0.57 A/W, and the average quantum efficiency is 45%. Figure 70 shows the photocurrent for different input powers across 100 nm. As expected from the epi, lower wavelengths have a lower saturated output power.

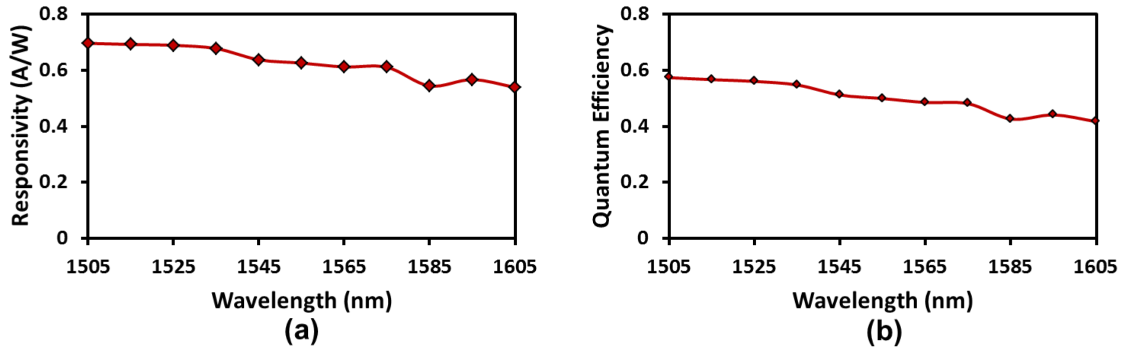

Figure 69. Plots of (a) responsivity and (b) quantum efficiency for a 470 μm x 9 μm test photodiode biased at -5 V.

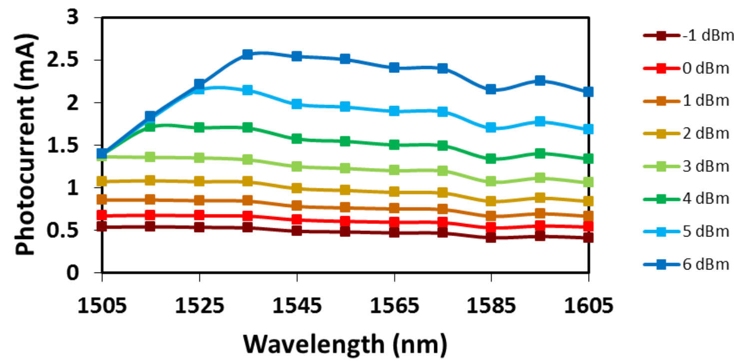

Figure 70. Photo current on a test photodiode at increasing input powers while biased at -5 V.

The integrated photodiodes were tested by measuring them individually while doing a current ramp on one of the central channel SOAs. This test was primarily to verify they were working electrically as it was difficult to ascertain the actual power reaching the device. There was 100% yield for the integrated photodiodes. Plots of the SOA crossing the lasing threshold and the photodiode response for all channels are shown in Figure 71. Images of the GRIN lens and photodiode array can be seen in Figure 73 and Figure 74.

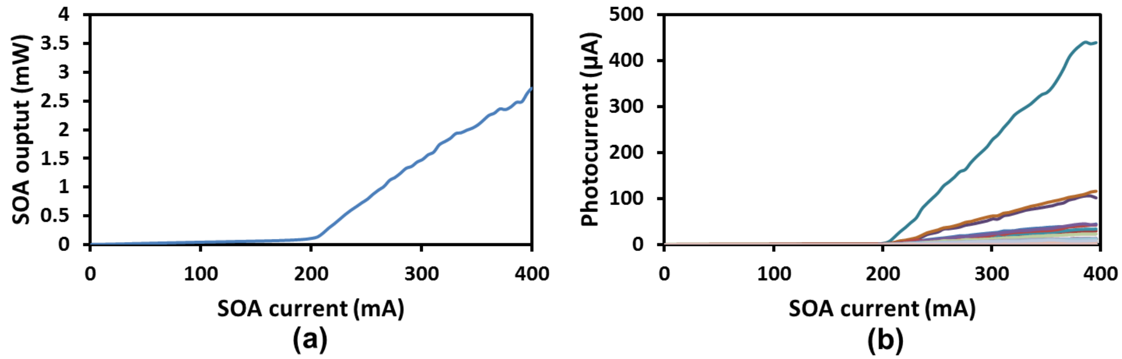

Figure 71. (a) Plot of the output power from SOA 13 as a function of pump current and captured using an integrating sphere. (b) Plot of photocurrent for each of the 32 photodiodes vs. SOA 13 pump current. Light passes through the output emitter grating and the GRIN lens before entering the photodiode array.

It appears that the GRIN lens was unsuccessful as fabricated. Measurements of the photodiodes during beam-steering operation show no discernible correlation between output angle and photodiode location. The photocurrent for each photodiode is shown for steering angles of 0˚ and 5˚ in Figure 72, illustrating the lack of correlation. It is possible that the results would be improved for higher beam power or with additional iterations of the device. Due to lack of time this lens was not pursued further. Possible reasons for the lens failure are incorrect proximity correction during e-beam lithography, and etch depth inaccuracies.

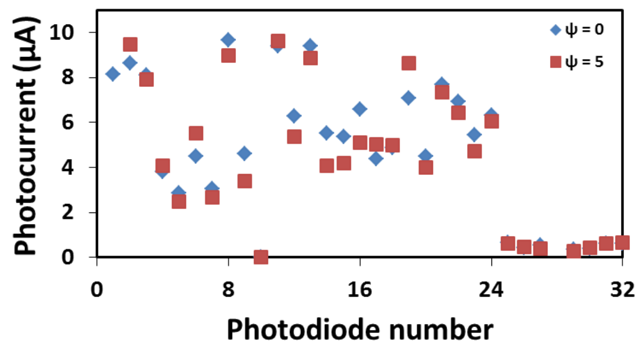

Figure 72. Photocurrent for integrated photodiodes with two angles of steering chosen.

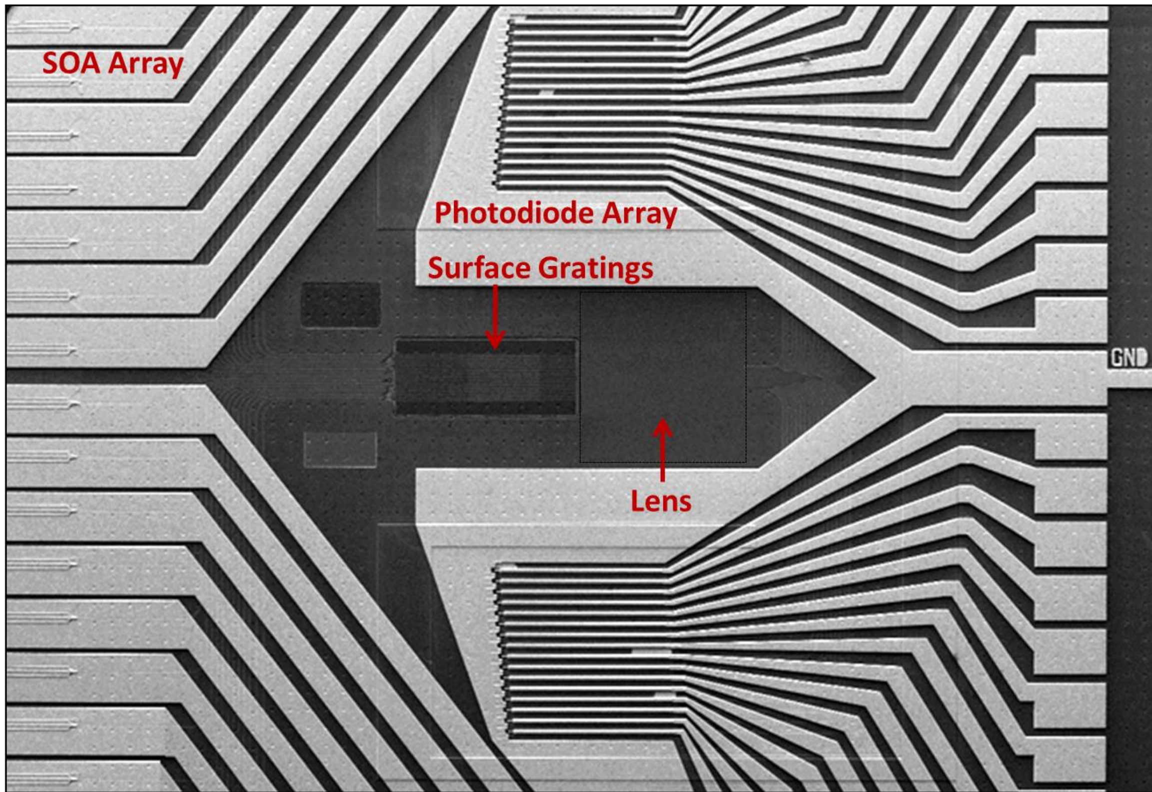

Figure 73. SEM image of the on-chip feedback system, including output surface grating array, GRIN lens and photodiode array.

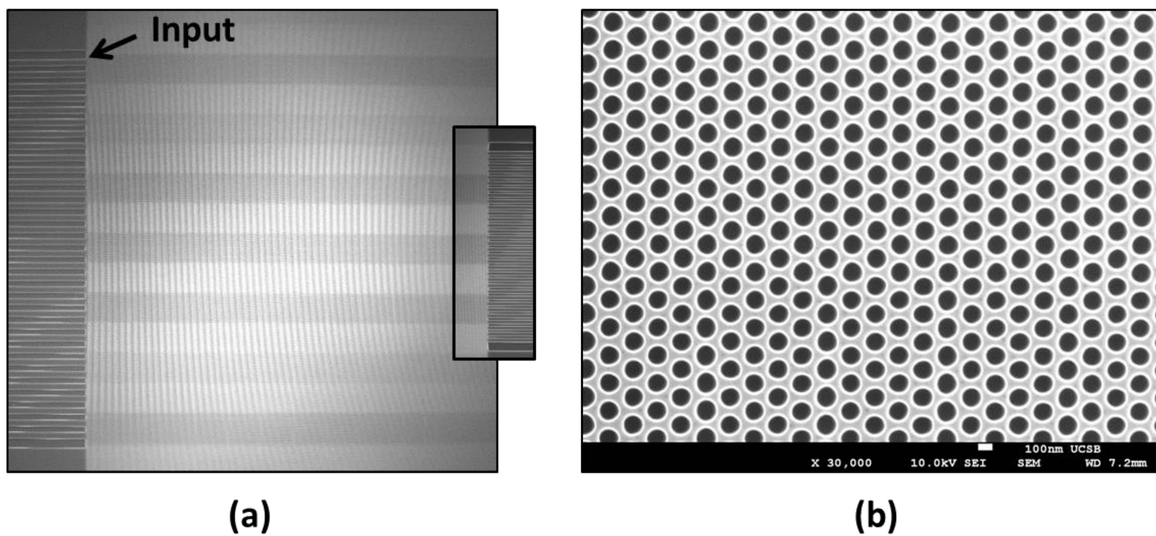

Figure 74. (a) SEM image of GRIN lens input with output shown in the inset. (b) High magnification image of GRIN lens.

Integrated PIC

The power budget for the integrated PIC is shown in Table 3. The laser was expected to produce 7 dBm power, and the pre-amp was expected to have 5 dB of gain. Insertion loss from the MMI tree of 2 dB was assumed along with the 15 dB of power reduction from splitting into 32 channels. The phase modulator loss was expected to be 2.5 dB and 5 dB/cm * 0.8 cm = 4 dB was expected for waveguide loss. The channel amplifiers were expected to produce around 18 dB of gain. The grating configuration for 1 μm of buried oxide shows -4.6 dB of loss to the power emitted through the silicon substrate and calculations of the phased array showed -3.6 dB of power in the side and aliasing lobes. By combining the 32 channel output the beam gains back the 15 dB lost from the MMI tree for a total expected output power of 13.3 dBm. This chip did not hit the hoped for output power. Power collected via a lens to fiber was measured to be -50dBm. Most of the difference here is attributed to much lower gain for the III/V sections due to general chip heating. Additionally, the amplifiers did not work uniformly. Three channels would not function at all due to short circuits, and the remainder had differing levels of gain for a given pump current. It was discovered that the best operation for noise was achieved when the SOA current was kept below 30 mA, at which point the amplifiers are absorbing instead of amplifying. At higher operation, the ASE would overwhelm the signal. An image of the noisy output for higher pump currents is shown in Figure 75. As such, the total output power was less than a microwatt. The yield for electrically working gain elements was 93%.

Designed power budget	Gain (dB)	Power per Channel (dBm)
Laser	7	7
Pre-amp gain	5	12
MMI tree loss	-2	10
MMI tree split	-15	-5
2 mm phase mod	-2.5	-7.5

WG loss	-4	-11.5
Channel amp	18	6.5
Loss to substrate	-4.6	1.9
Side lobe power	-3.6	-1.7
Combined Beam	15	13.3

Table 3. Power budget for beam-steering chip design.

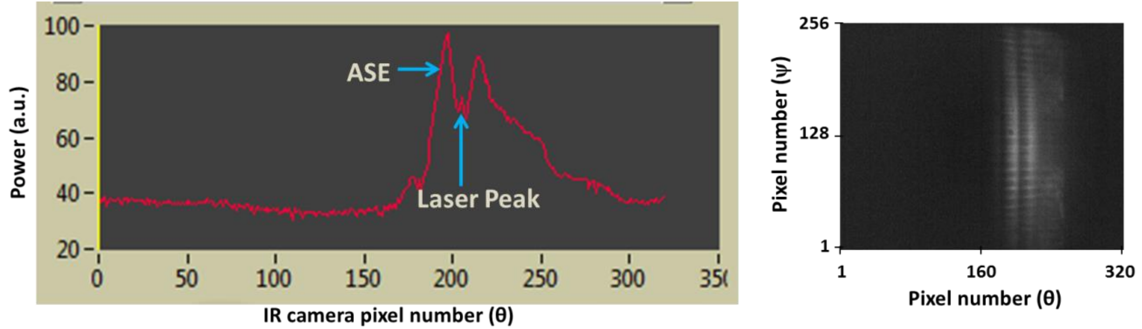

Figure 75. (a) Longitudinal (θ) output and (b) camera image with laser pump current set to 260 mA, pre-amplifier current set to 240 mA, and channel 11 SOA set to 150 mA. All other amplifiers were switched off. ASE is dominating the output.

To measure the two-dimensional beam-steering properties of the PIC the laser was set to 260 mA pump current, and the pre-amplifier was set to 240 mA. The laser was tuned to the desired wavelength, and then the channel amplifiers and phase modulators were optimized by using the hill-climber algorithm described in other phases of the project. More intricate algorithms were also attempted, but it was found that the simplicity of the hill-climber algorithm worked best in practice. A steering window of 23˚ (ψ) x 3.6˚ (θ) was demonstrated with beam widths of 1˚ (ψ) x 0.6˚ (θ). This corresponds to 23 x 6 resolvable spots which is nearly double the desired goal. The SMSR was limited to 70% by inconsistent gain characteristics in the channel amplifiers, including 3 failed amplifiers. Images of several points across the field of view are shown in Figure 76. This is the first demonstration of fully integrated two-dimensional beam-steering on a silicon-based platform.

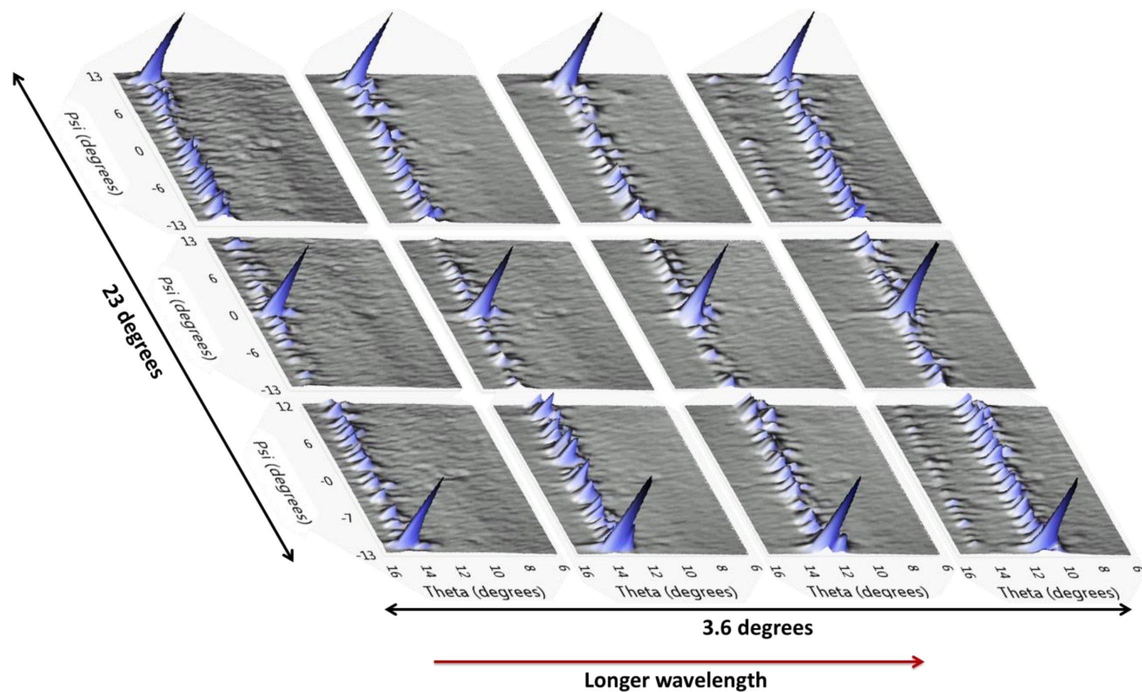

Figure 76. Plots of beam-steering across a field of view of 23˚ laterally (ψ) and 3.6˚ longitudinally (θ).

Packaging

Many of the measurements done on this chip were done after packaging was completed. The completed chip was diced to a size of 6 mm x 11.5 mm. The substrate was mechanically thinned to 100 μm to reduced thermal impedance, and metal was deposited on the backside. The stack was Ti/Ni/Au 20/50/200 nm. An image of the finished chip can be seen in Figure 77.

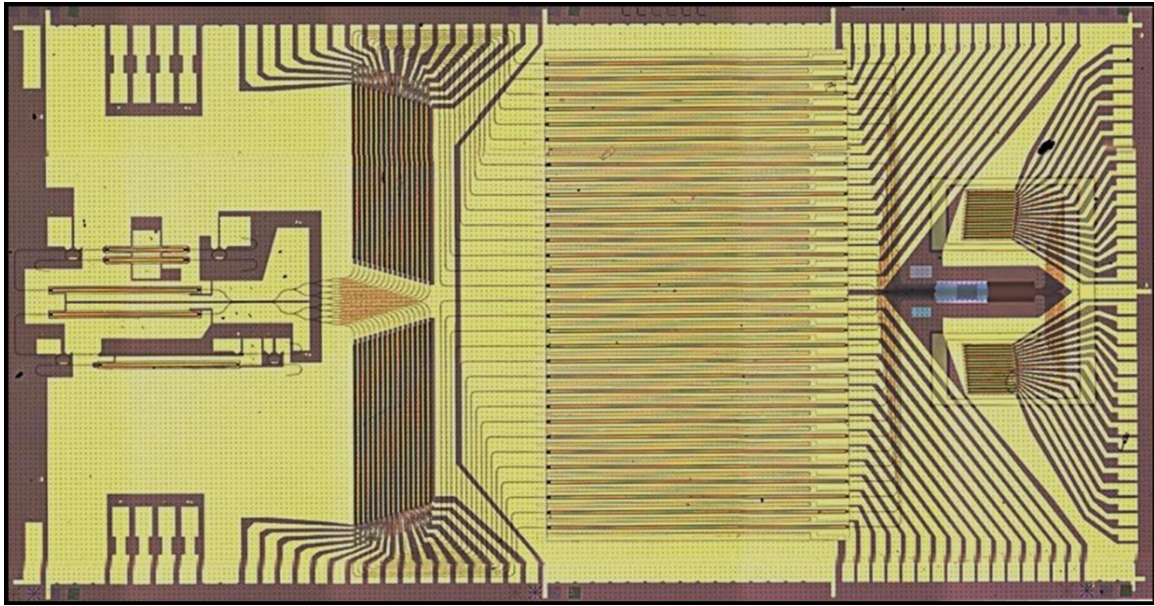

Figure 77. The completed fully integrated beam-steering chip, measuring 6 mm x 11.5 mm.

The chip was mounted on a BeO carrier. The carrier material was chosen for its high thermal conductivity (370 W/m K [23]), and because the thermal expansion coefficient is close to that of silicon and InP. However, BeO is toxic and should be handled with care.

The BeO carrier was patterned with a series of pads to match the I/O pads of the beam-steering chip. These lead to additional pads farther from the chip which are used to connect to a printed circuit board via a pogo-pin connector. The carrier was also patterned with a large solder area designed to be directly under the chip. However, the soldering was not uniform and the chip easily separated from the carrier. To remount the chip, a thin thermally conductive epoxy was applied. Then the chip pads were wire-bonded to the carrier. A total of 106 separate signal wires (5 of these were for the redundant laser and pre-amplifier) plus ground wires led to 163 wire-bonds.

A copper chuck was manufactured with a shallow cutout to precisely fit the BeO carrier, and aligned to the pogo-pin connector by way of two holes for alignment pins. The copper

chuck also had a full-depth cutout to fit a micro-channel cooler block. The cooling block allowed water cooling to be directly below the BeO carrier under the chip.

The PCB was originally intended to connect to a large driver board via high-speed connectors. The driver board was provided by a third party vendor. However, after extensive debugging and long delays it became clear that the board would never be completed in a way that would successfully drive the chip.

As an alternative, wires were soldered into PCB through-hole vias and connected to three ILX laser drivers at low speed. Although this did not allow testing of rapid tuning, it was sufficient to test the DC performance of the chip. Images of the test setup and components can be seen in the figures below.

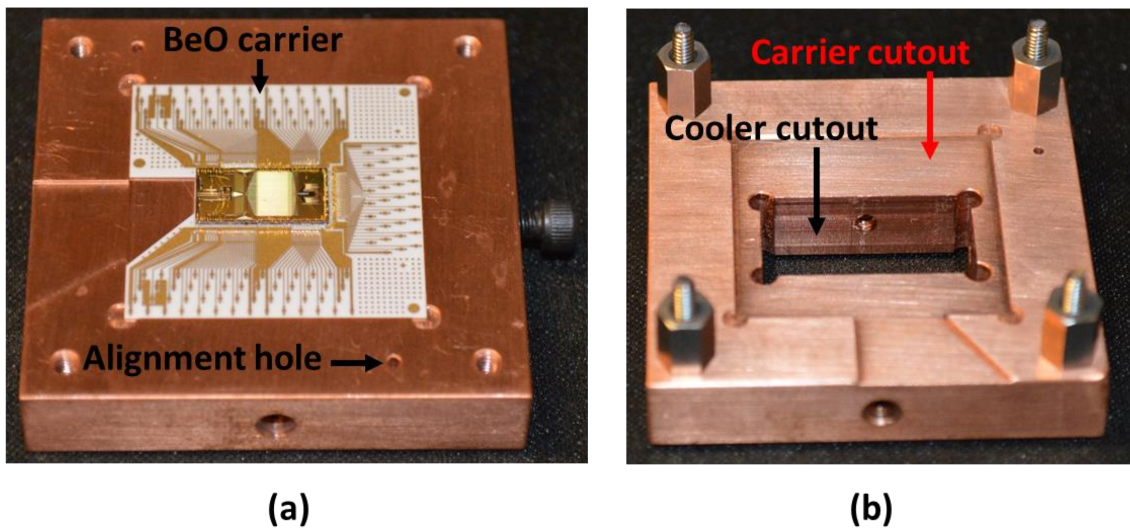

Figure 78. (a) Image of the mounted and wire-bonded chip on a BeO carrier placed on the copper chuck. (b) Image of the copper chuck with cutouts for the BeO carrier and for the micro-channel cooler.

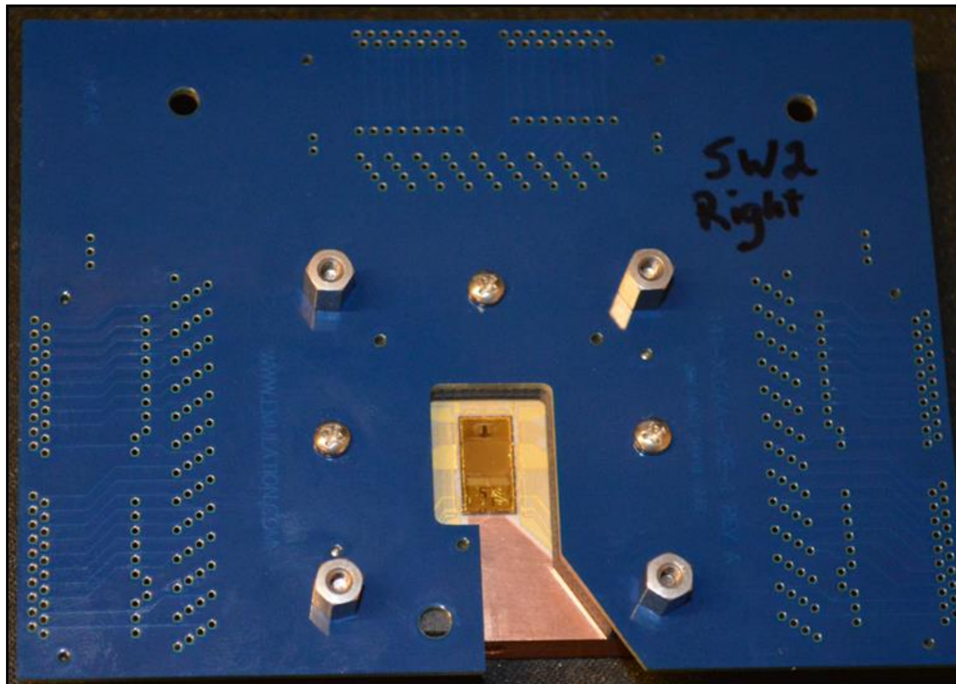

Figure 79. Image of PCB board electrically connected to BeO carrier via pogo pins.

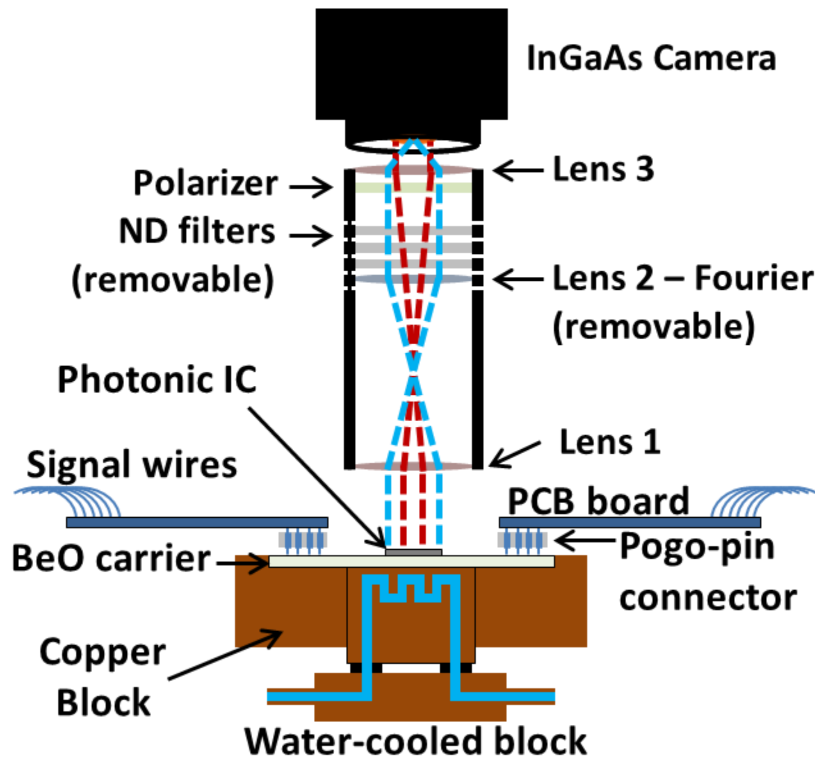

Figure 80. Diagram of the fully-integrated beam-steering setup.

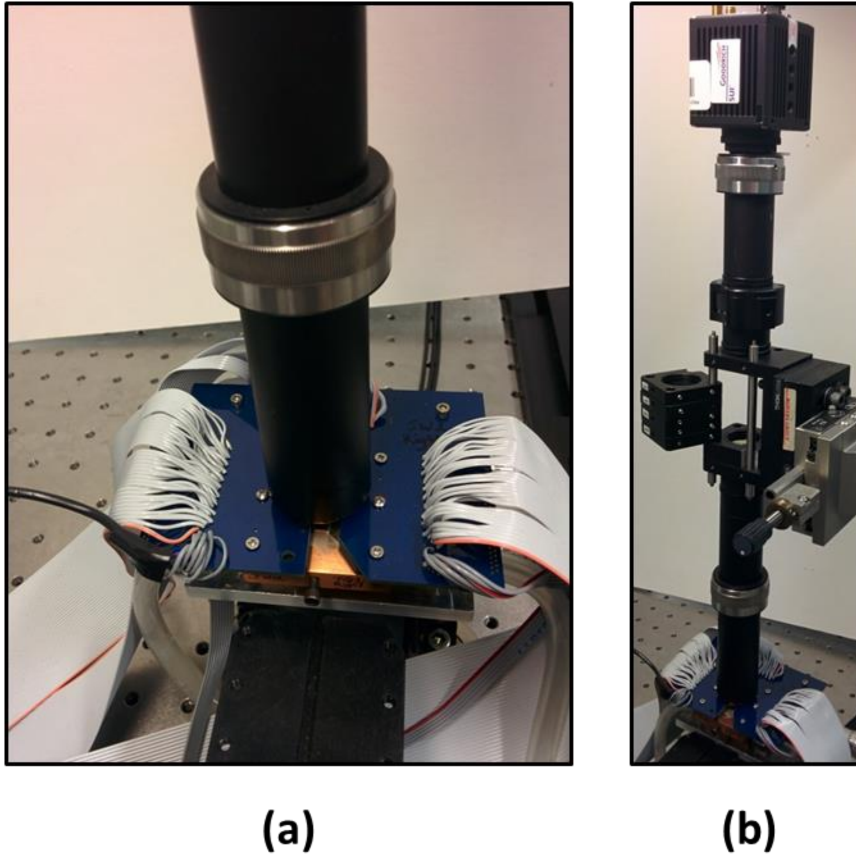

Figure 81. Images of the beam-steering setup.

Measurements show that the average electrical power consumption for this device as it was operated was 2.1 W, or 65.9 mW per facet.

The original driver board is shown in Figure 82. It is significantly larger than the small chip it is driving and emphasizes the fact that interfacing with photonic integrated circuits grows much more difficult as the complexity of the circuits increases.

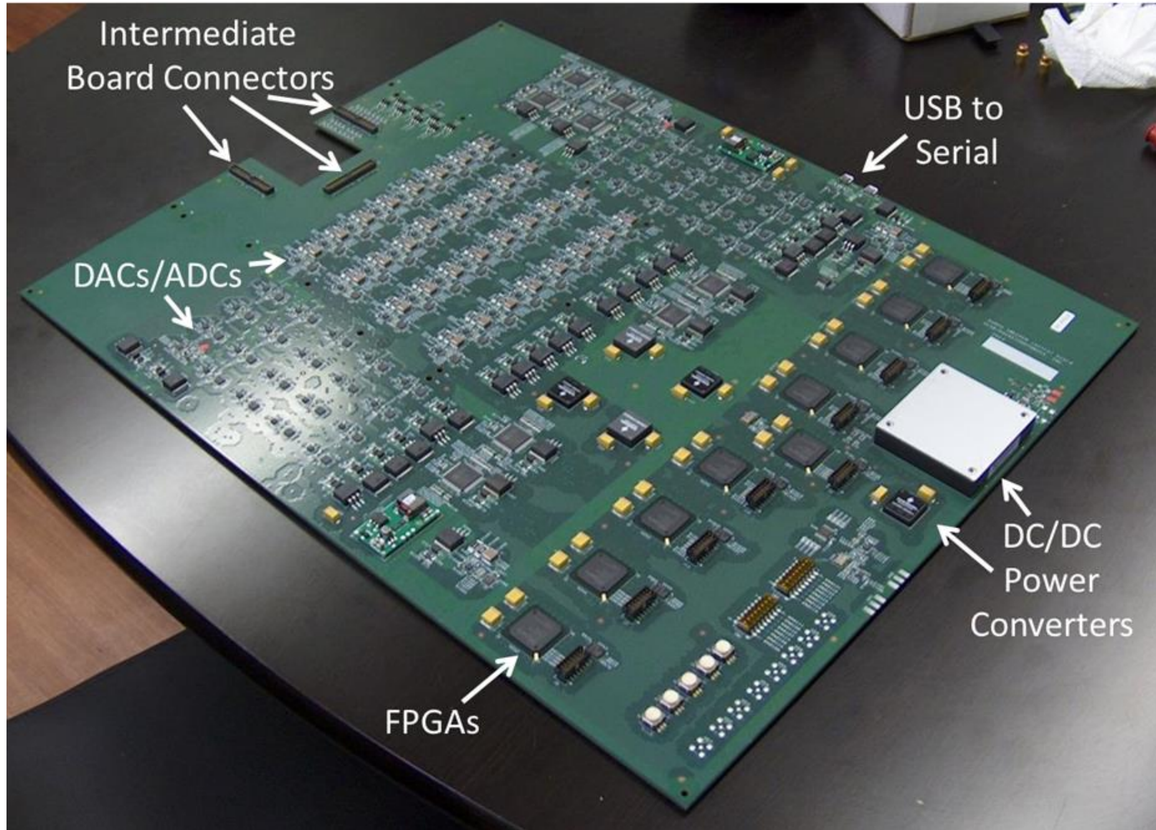

Figure 82. Image of the almost-functional driver board.

3.6 Summary

Three phases of silicon-photonic beam-steering have been explored. The first phase achieved 20˚ (ψ) x 14˚ (θ) of steering with respective FWHM beam widths of 1.6˚ x 0.7˚ and SMSR greater than 10 dB with the use of an off-chip laser.

Phase II integrated gain elements and demonstrated tuning of 12˚ in ψ with beam-widths of 1.8˚ (ψ) x 0.6˚ (θ) and SMSR greater than 7 dB. A tunable laser was demonstrated during this phase with 40 nm of tuning, corresponding to 5.6˚ of steering. A fast phase modulator was also demonstrated that allows for rapid, linear phase tuning up to 40 MHz and beam-steering up to 3.7×10^8 ˚/s. This is the first demonstration of beam-steering on a silicon-based platform with an integrated laser.

Phase III brought the level of integration up significantly, with 164 integrated optical components. At the time this was the largest number of integrated components on a heterogeneous silicon-III/V platform. A steering window of 23˚ (ψ) x 3.6˚ (θ) was demonstrated with beam widths of 1˚ (ψ) x 0.6˚ (θ) and SMSR of 5.5 dB. This is the first demonstration of fully integrated two-dimensional beam-steering on a silicon-based platform.

Future devices should include a transmit and receive functionality to fully realize a LIDAR system. Additionally, as this could be used for free-space point-to-point communication, a test of the data transmission capabilities should be tested.

This is a promising step toward cheaper and more ubiquitous use of optical beam-steering chips. While the electrical power usage is still far too high for hand-held devices, these chips could be used in vehicles with a little optimization to increase optical output power.

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Chapter 4

Photonic Microwave Generators

Electronic devices are continuously reaching for higher bandwidths to accommodate ever-expanding demand. This increase has put similar bandwidth requirements on the devices used to test and measure them. Network analyzers traditionally operate up to tens of gigahertz and with frequency up-conversion may extend to a broader range. This is costly, bulky, and fragile and can be difficult to operate. There is demand for a simpler, smaller, less-expensive option for microwave generation.

Another market for a compact and cheap microwave generator is wireless communications. For example, the 57-64 GHz band has been made available by many the communications regulators of many countries[1]. In the United States there are open frequencies in the lower 70s, 80s and 90s of gigahertz totaling 12.9 GHz of spectrum which could reduce wireless congestion.

Rather than directly driving an electronic signal, photonics can be utilized to generate a high frequency signal. The signal is generated by using the outputs from two lasers and

beating them on a photodiode. The heterodyne beat tone is generated at the frequency difference between the two laser outputs. With a tunable laser, an arbitrary frequency difference can be generated, and the microwave signal can be swept from low frequencies to hundreds of gigahertz. The main limitations on this signal are the speed and responsivity of the photodetector, and the laser output power and linewidth.

Integrated on-chip microwave generation has been explored as a compact solution by several groups [2]-[3]. To meet the requirements for high performing lasers and photodiodes, separate specialized III/V growth stacks need to be optimized for each. This chapter looks into the first fully-integrated microwave solution on a heterogeneous silicon-III/V platform.

4.1 Design

The chip design consists of two tunable lasers, each with a phase modulator, a directional coupler to combine the beams, and a waveguide photodiode. The second output arm of the directional coupler leads to a facet for external monitoring on an optical spectrum analyzer or microwave generation on an off-chip photodiode. A schematic of the chip can be seen in Figure 83.

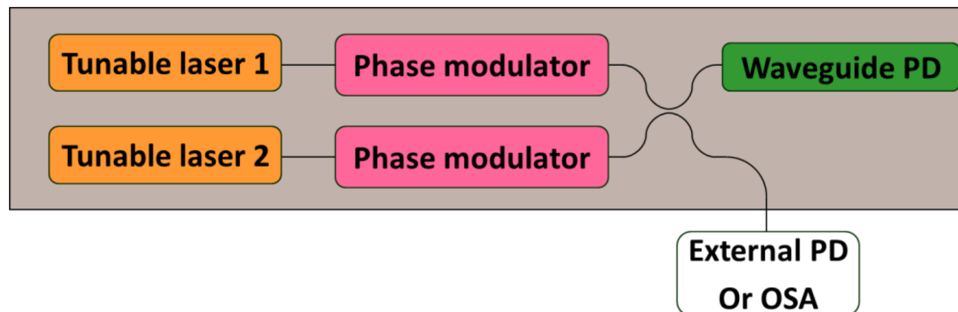


Figure 83. Schematic of microwave generator chip with three different epi stacks bonded.

The beat tone of the lasers creates an RF signal on the photodiode. One or both of the lasers can be tuned to generate a frequency sweep over a large bandwidth. The signal generation follows Equation 21 where A is the amplitude, ω_1 and ω_2 are the frequencies of the two lasers, and ϕ_1 and ϕ_2 are the laser phases.

$$I_{RF} = A\cos[(\omega_1 - \omega_2) + (\phi_1 - \phi_2)] \qquad \textbf{Equation 21}$$

The lasers used on this chip are of the ring-bus-ring (RBR) and the one-sided coupled-ring-resonator (CRRx1) designs described in chapter 2. The gain III/V stack used was epi-H and had three quantum wells (Appendix B), and the modulator epi was centered at 1360 nm to reduce loss. The epi stacks for laser and modulator were nearly identical except for the separate confined heterostructure (SCH) and quantum well layers. This allowed them to be co-processed. Details of the process can be found in Appendix C and D.

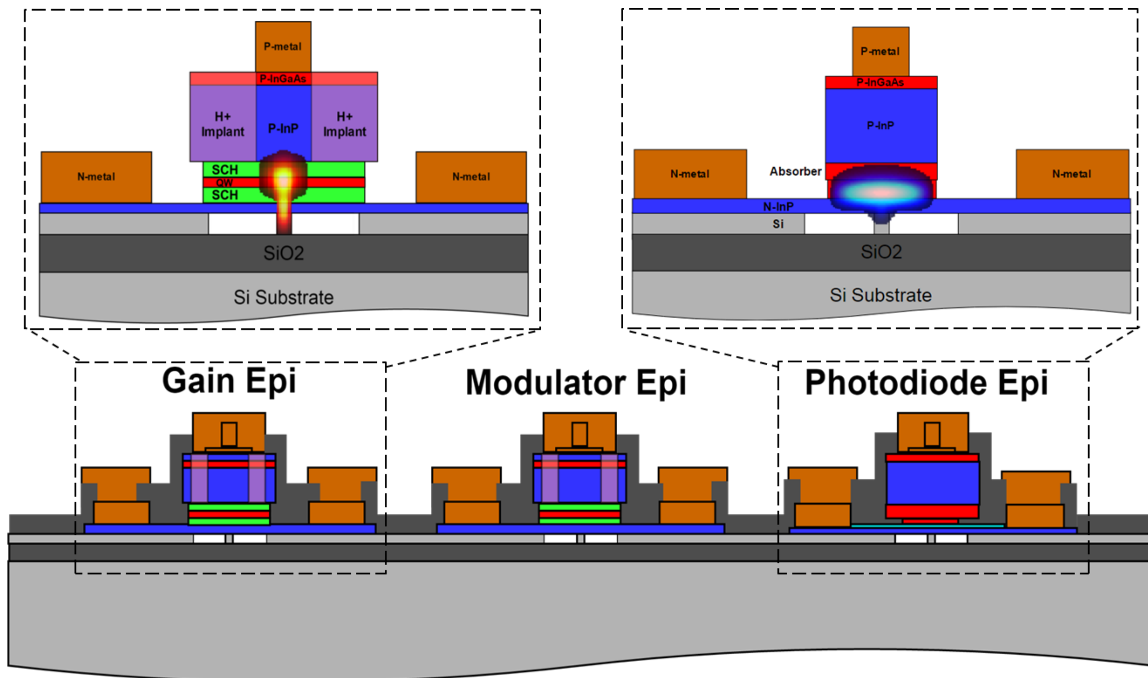


Figure 84. Illustration of the cross-section of the three types of III/V diode integrated on the chip with close-up views of the gain and photodiode epis showing the simulated mode. The gain inset is also representative of the modulator stack in regards to the mode profile.

4.2 Photodiode

An ideal photodiode for this chip would have high bandwidth, high responsivity, and be processed in the same manner as the gain and modulator sections. A *p-i-n* waveguide photodiode with a 400 nm thick $In_{0.53}Ga_{0.47}As$ absorber region (epi stack PD-J) was designed to accommodate these needs. Two photodiode designs were investigated in detail. Photodiode Type 1 is 30 µm long, 4 µm wide, and has a 2 µm starting waveguide width. Photodiode Type 2 is 15 µm long, 3 µm wide, and has a 1.5 µm starting waveguide width. Schematics for both types can be seen in Figure 85 and an SEM image of the completed PD can be seen in Figure 86. The view of the waveguide in the SEM is obscured by 1 µm of SiO_2 and 3 µm of BCB, which is used to reduce pad capacitance.

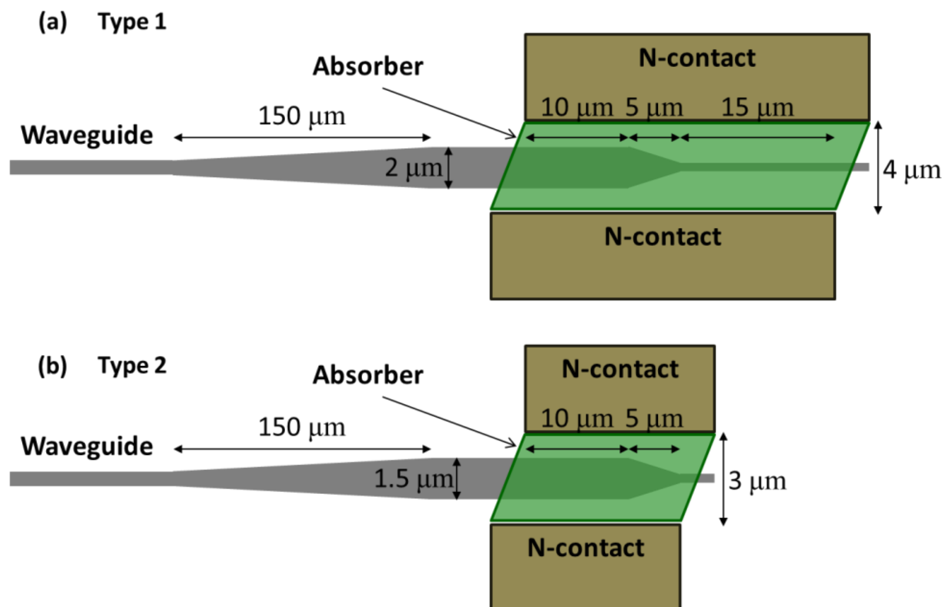


Figure 85. Top view schematics of waveguide photodiodes. The n-contact region extends to 26 µm on either side of the absorber region.

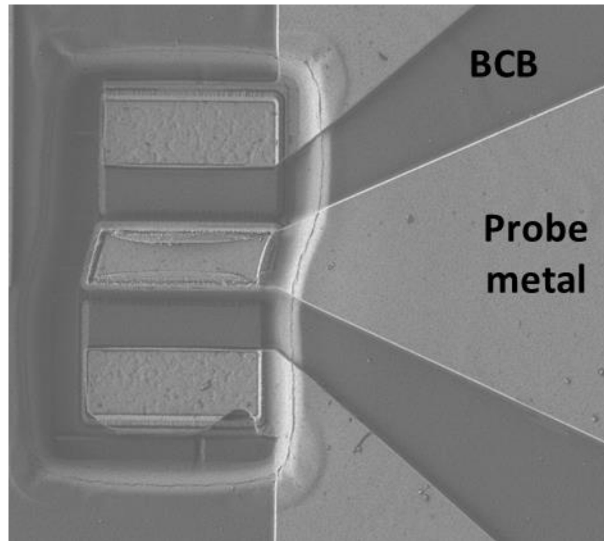


Figure 86. SEM image of completed photodiode.

The dark I-V characteristics of both types of photodiodes are shown in Figure 87 for 1550 nm continuous wave (CW) input. Measurements of the photodiodes were performed at 23 °C. Both types of photodiodes are clearly rectifying with low dark currents (10 nA for a 120 μm^2 device biased at -2V). Type 2 shows higher reverse dark current in spite of having a smaller active area, which implies the dark current doesn't originate from bulk defects in the III-V. Rather it suggests the dark current originates mainly from the surface state induced leakage current instead, which is proportional to the perimeter [6].

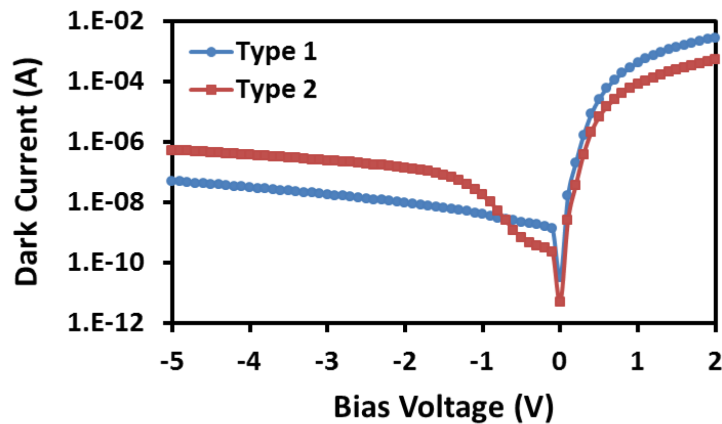


Figure 87. Measured dark current for both photodiode types at 23°C for CW 1550 nm input.

Simulations shown in Figure 88 (a) indicate that most of the power launched can be absorbed within the 30 µm device. The 15 µm device (Type 2) is expected to absorb approximately 0.75 that of the Type 1 device. After de-embedding the facet coupling loss (Figure 89) and fiber loss, the DC internal responsivity is approximately 0.4 and 0.3 A/W for Type 1 and Type 2, respectively. Responsivity from 1510 to 1610 nm can be seen in Figure 90.

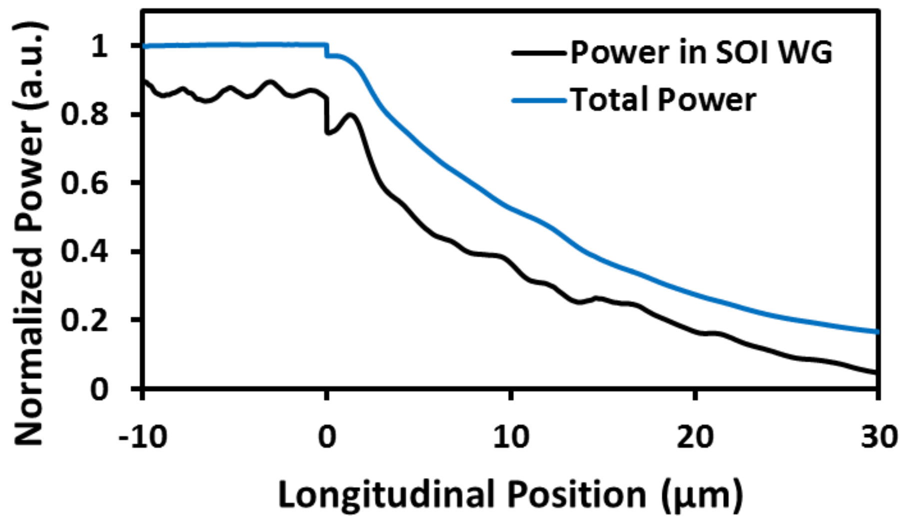


Figure 88. Simulated optical power as the field propagates through the photodiode.

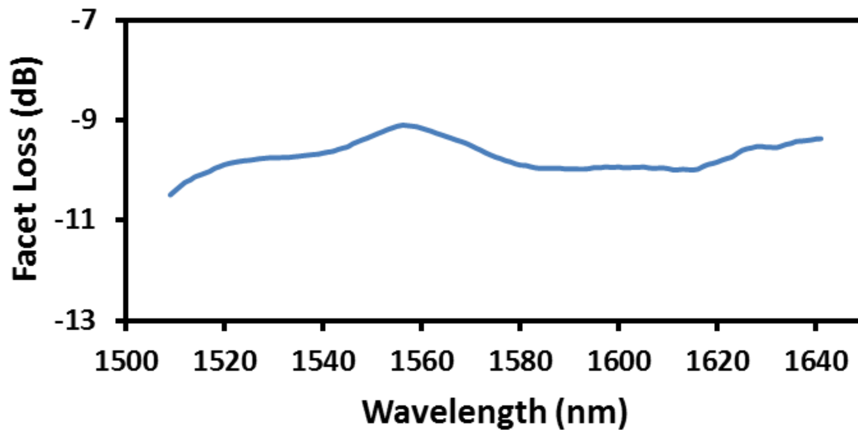


Figure 89. Measured facet loss.

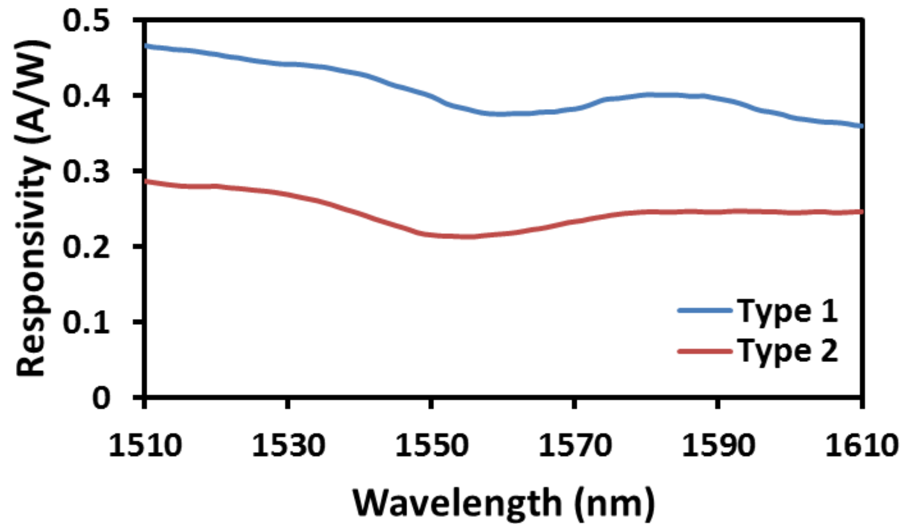


Figure 90. Extracted CW responsivity of photodiodes Type 1 and 2.

The optical-to-electrical (O-E) frequency response was measured using two different techniques. First, the response from 100 MHz to 67 GHz was measured using an Agilent N4373 D lightwave component analyzer. An EDFA was used to increase the laser output power. For frequencies above 67 GHz a heterodyne-beating system using two external lasers was set up. The photo-generated microwave power from the photodiode under test was measured with a Keysight E8486A E-band power sensor and a GGB model 90 waveguide probe.

The measured O-E frequency response with different bias voltages is shown for the Type 1 photodiode in Figure 91. This was taken with two levels of output photocurrent (1 mA and 3 mA). Under low output photocurrent, the measured 3 dB bandwidth is close to 65 GHz for -5 V bias, and 58 GHz for -3 V bias. At higher output photocurrents the 3 dB bandwidth reduces for -3 V bias due to an increase in space-charge screening, which is commonly observed in high-speed photodiodes operated at high powers [7]. The degradation in performance is even more significantly pronounced when biasing at -1 V when the absorber

region is not sufficiently depleted. However the 3 dB frequency response remains the same for low and high photocurrents when using -5 V bias.

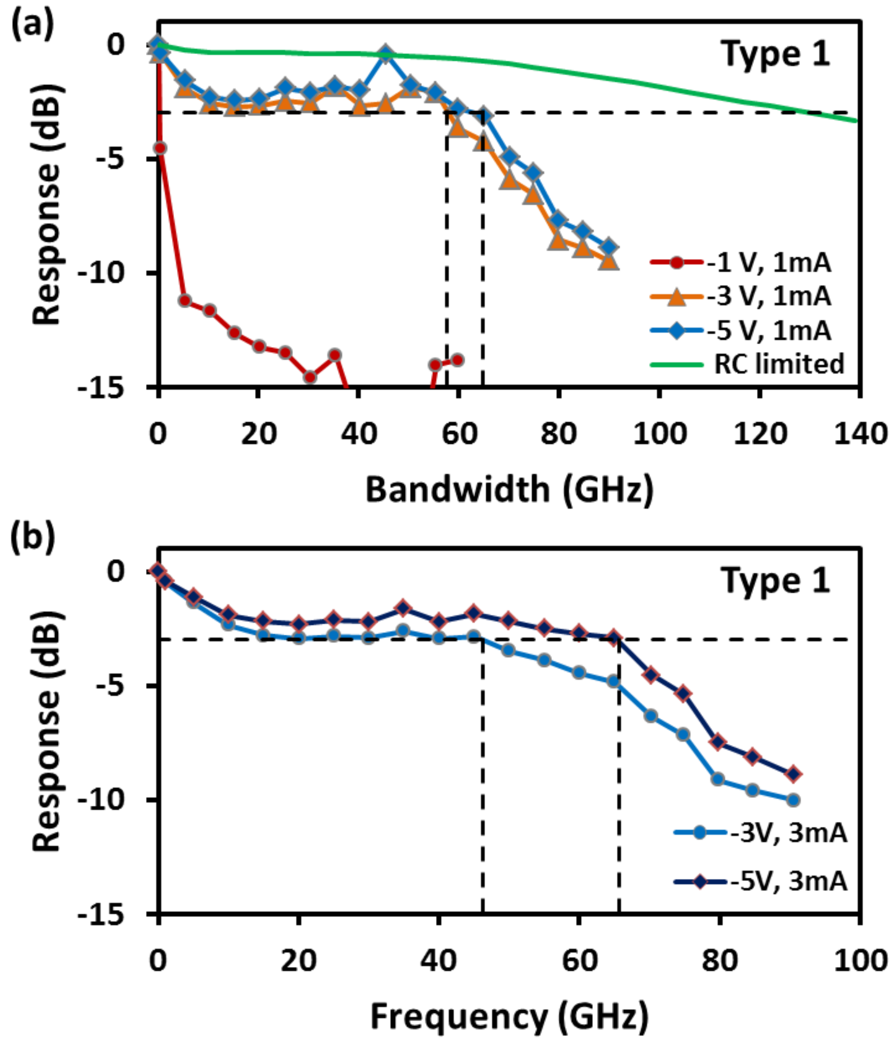


Figure 91. O-E response for Type 1 photodiode with (a) 1 mA and (b) 3 mA output photocurrent. The extracted RC-limited frequency response is shown in (a) in green.

The bandwidth in many photodiodes is RC limited due to parasitic and junction capacitances. Reducing the active area of the photodiode allows for a reduced junction capacitance while using the same epi stack. Thus, the Type 2 device is expected to have a larger RC limited bandwidth. The O-E measured frequency response for the Type 2

photodiode is shown in Figure 92. It is notable that the reduced active area (45 vs. 120 μm^2) only slightly increases the bandwidth of the device (67 vs. 65 GHz), which suggests the device bandwidth is not dominated by RC time constants.

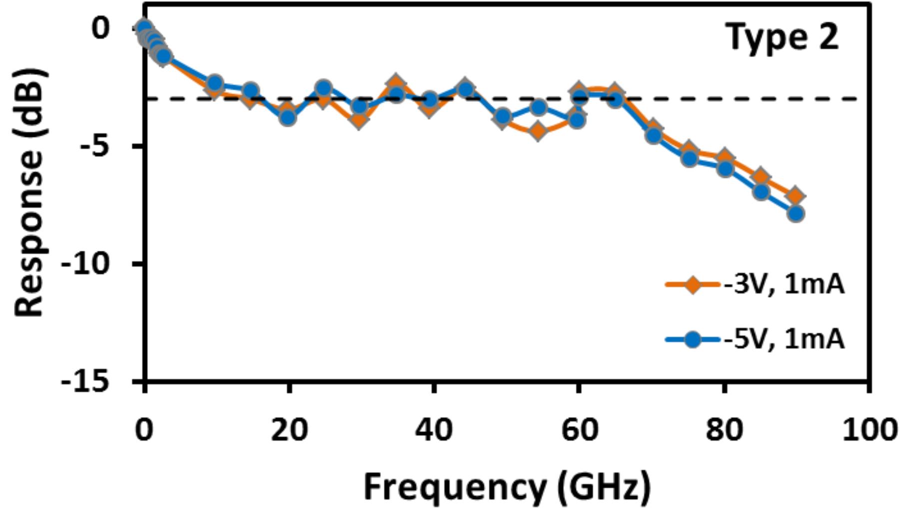
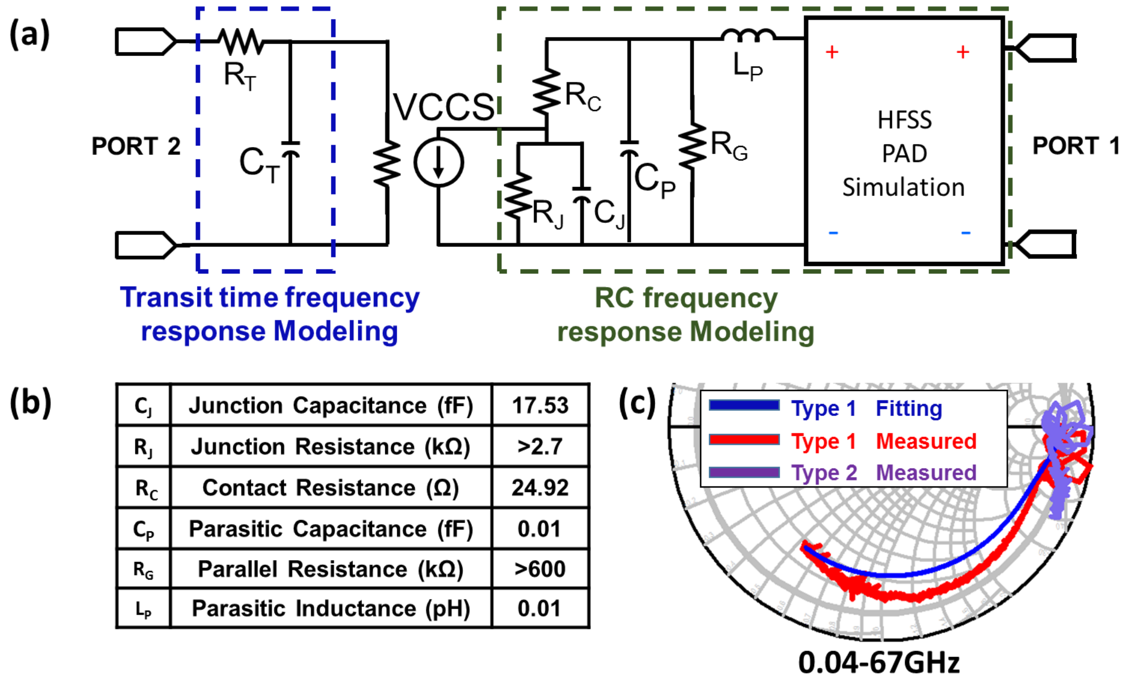


Figure 92. O-E response for Type 2 photodiode with 1 mA output photocurrent at -3 V and -5 V biases.

To achieve a more clear understanding of the relationship between the O-E bandwidth roll-off, the RC limitations and the carrier transit time, an equivalent circuit model was created for the Type 1 device. The RC-limited bandwidth (f_{RC}) was extracted using the measured microwave reflection coefficients (S_{11}) of the photodiode [8]. The equivalent circuit model used is shown in Figure 93. The extracted values of all circuit elements except R_T and C_T are included in a table, as well as a Smith chart with the measured and fitted S_{11} curves. C_J and R_J, are the junction capacitance and resistance, respectively. R_C represents the differential resistance of the active diode. C_P is the parasitic capacitance induced by the probe-pad co-planar waveguide configuration. R_P and L_P represent the ohmic loss and inductance, respectively, of these metal lines. R_G and C_G are the dielectric loss and capacitance from the dielectric layer (BCB and SiO_2) below the probe metal. VCCS

signifies voltage-controlled source. The PAD simulation blocks used included the parasitic effects of the co-planar waveguide. These parameters were calculated using momentum simulation software (HFSS).



C_J	Junction Capacitance (fF)	17.53
R_J	Junction Resistance (kΩ)	>2.7
R_C	Contact Resistance (Ω)	24.92
C_P	Parasitic Capacitance (fF)	0.01
R_G	Parallel Resistance (kΩ)	>600
L_P	Parasitic Inductance (pH)	0.01

Figure 93. (a) Photodiode equivalent circuit model. (b) Table of circuit element values used in modeling. (c) Measured and fitted S_{11} from 40 MHz to 67 GHz under -3V DC bias for Type 1 PD. Also measured S_{11} for Type 2 PD.

To extract f_{RC} from the photodiode model, the elements R_T and C_T were removed, as these are used to model the low-pass frequency response of the internal carrier transit time. The fitted curve matches the measured fairly well for the Type 1 PD from near DC to 67 GHz, but the fitting of the smaller Type 2 PD proved difficult. The extracted RC-limited frequency response is shown in Figure 91 in green and exhibits a 3 dB roll-off at 133 GHz. Comparing the expected RC-limit to the 67 GHz 3 dB bandwidth of the photodiode leads to the conclusion that the combined O-E bandwidth is predominately carrier transit time limited. Assuming an average carrier drift velocity of 5.3×10^4 m/s in the InGaAs active layer

with 400 nm thickness, the calculated transit-limited bandwidth is ~74 GHz which matches the 67 GHz measured result fairly well. Additional improvements in speed could be accomplished by reducing the thickness of the active region, and thus reducing the transit time. However, this has the drawback of reducing the mode overlap with the active region and thus reducing responsivity.

The photo-generated microwave power from a 70 GHz sinusoidal beat tone is shown for both photodiode Types 1 and 2 in Figure 94 and Figure 95, respectively. The output power was measured with an E-band power sensor and de-embedded from the 1.12 dB of loss from the E-band WR-12 waveguide probe. There is about 10~11 dB difference between the ideal output power and that measured. The discrepancy in power is attributed to high-frequency roll-off which was measured to be 4~5 dB at 70 GHz, and a 50% optical modulation depth in our optical system during measurement which corresponds to another 6 dB of power loss. The maximum saturation current is 9 mA at -5 V bias for the Type 1 PD, and 6.5 mA for Type 2.

The Type 1 photodiode exhibits higher responsivity, higher saturated output current and power, and a nearly identical 3 dB roll-off point. These are excellent results and it will be our photodiode of choice for the microwave generator.

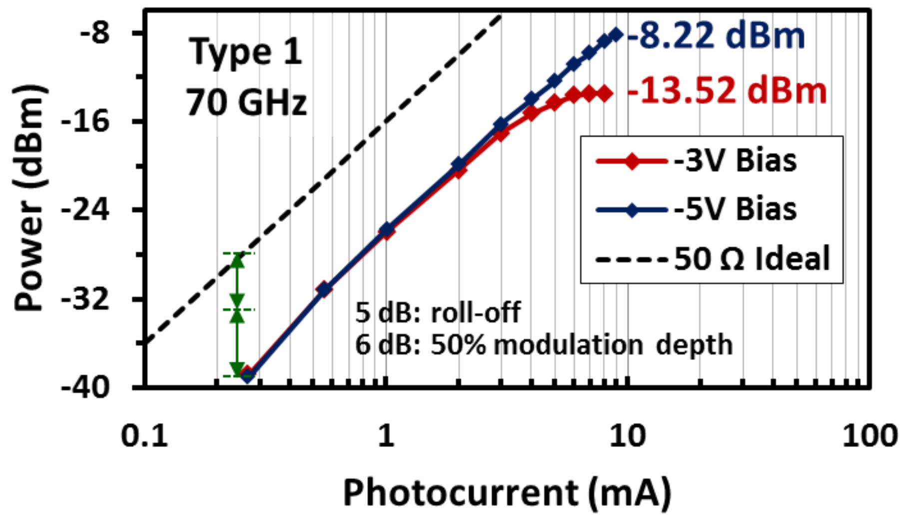


Figure 94. Measured photo-generated microwave power for the Type 1 device with a 70 GHz input signal at -3 V and -5 V bias and varying levels of photocurrent. The dotted line shows the ideal curve with 100% modulation depth and a 50 Ω load.

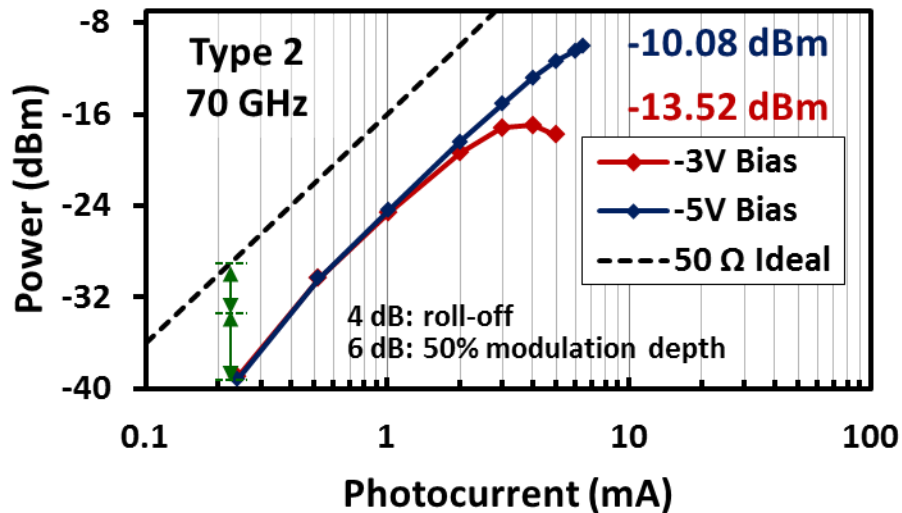


Figure 95. Measured photo-generated microwave power for the Type 2 device with a 70 GHz input signal at -3 V and -5 V bias and varying levels of photocurrent. The dotted line shows the ideal curve with 100% modulation depth and a 50 Ω load.

4.3 Microwave generation

The completed photonic microwave generator chip is shown in Figure 96. Testing of the completed chip included 8-pin probe cards for each laser, and a 67 GHz ground-signal-ground (GSG) probe for the photodiode. The electrical signal was measured using a Rhode and Schwarz 50 GHz FSU Spectrum Analyzer (ESA), and the optical signal was captured through a lensed fiber and monitored on a Yokogawa AQ6370C optical spectrum analyzer (OSA). The optional amplifier was a Centellax UA1L65VM 3-stage broadband amplifier. Figure 97 shows a schematic of the setup for testing up to 50 GHz. Higher frequency measurements used an E-band WR-12 waveguide probe in conjunction with a Keysight E8486A E-band power sensor as shown in Figure 98.

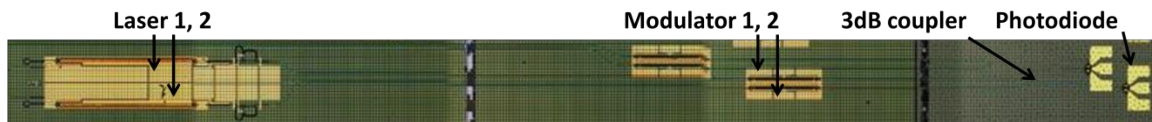


Figure 96. Optical microscope image of the fully integrated photonic microwave generator chip.

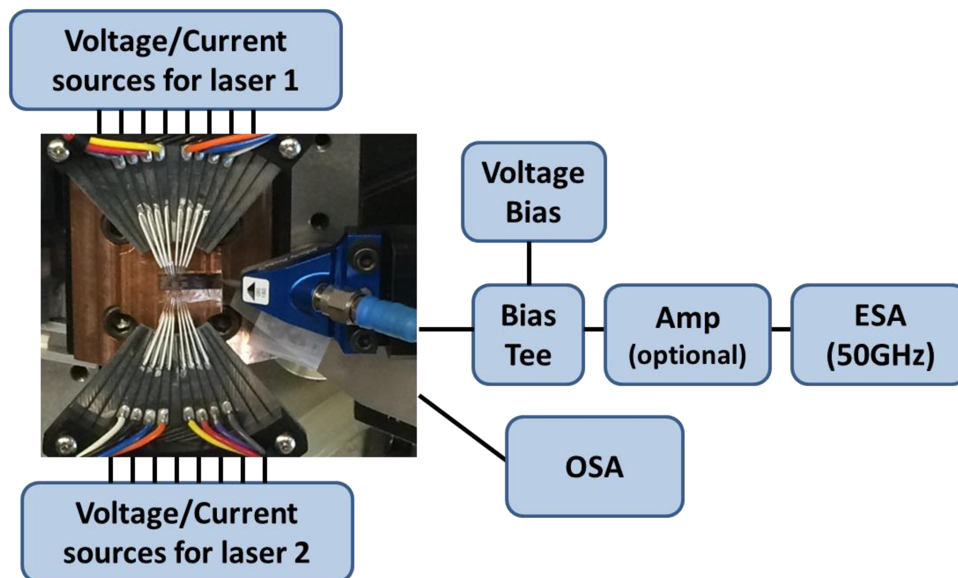


Figure 97. Test setup for microwave generator chip up to 50 GHz.

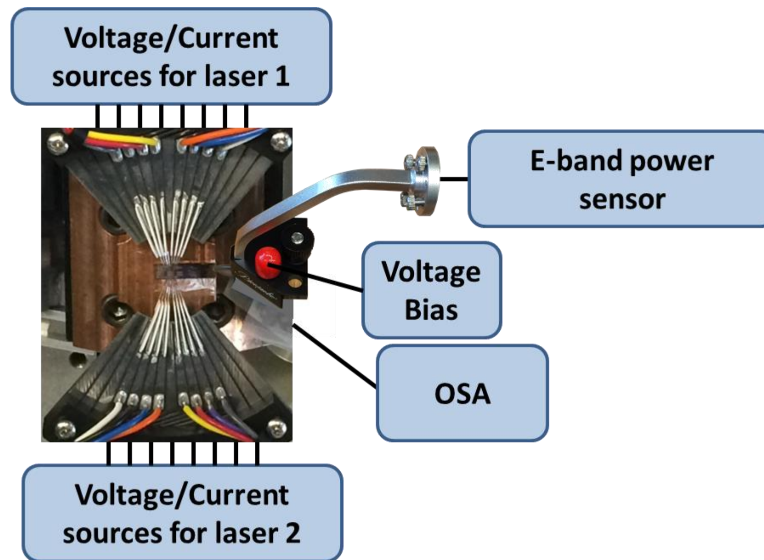


Figure 98. Test setup for microwave generator chip beyond 50 GHz.

A plot of the measured microwave power is shown in Figure 99. By tuning one laser relative to the other the beat tone frequency is swept across 1 to 112 GHz. The measured power roll-off does not correspond exactly with the photodiode roll-off, which is attributed to differences in laser power at different tuning settings. The optical spectrum scans for the first 50 GHz are plotted in Figure 100. It is notable that this is the first fully integrated microwave generator on the heterogeneous silicon-III/V platform. It is also notable that these results were accomplished without any off-chip amplification.

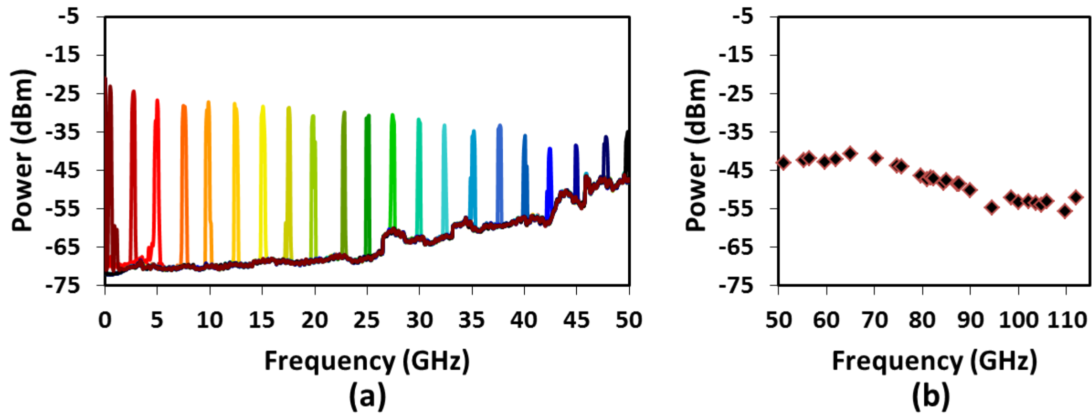


Figure 99. Measured microwave signals (a) from 1 to 50 GHz on an ESA, and (b) from 50 to 112 GHz on an E-band power meter.

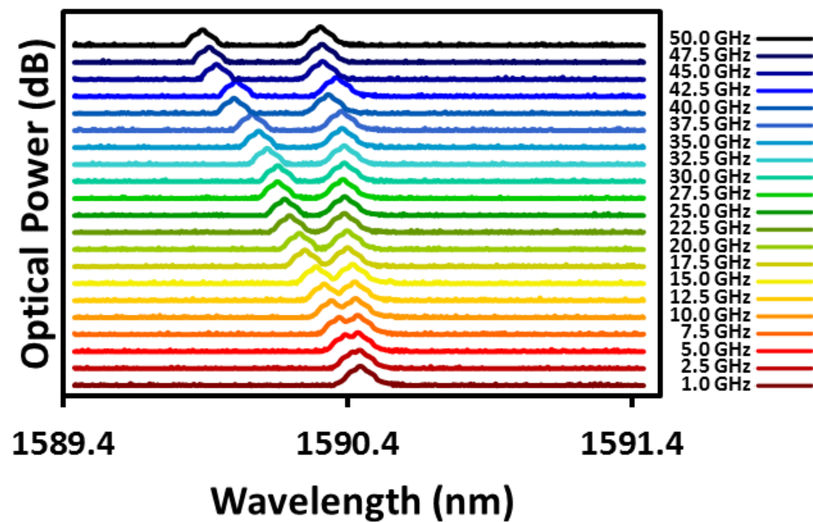


Figure 100. Optical spectrum from fiber-coupled facet for microwave signals from 1 to 50 GHz.

Adding a broad-band amplifier to the setup as in Figure 97 allows for much higher power as shown in Figure 101. However, adding in the amplifier also added in harmonic overtones not consistent with the stand-alone device. Also, due to the limited bandwidth of the amplifier the output power at higher frequencies is nearly identical to the non-amplified signal.

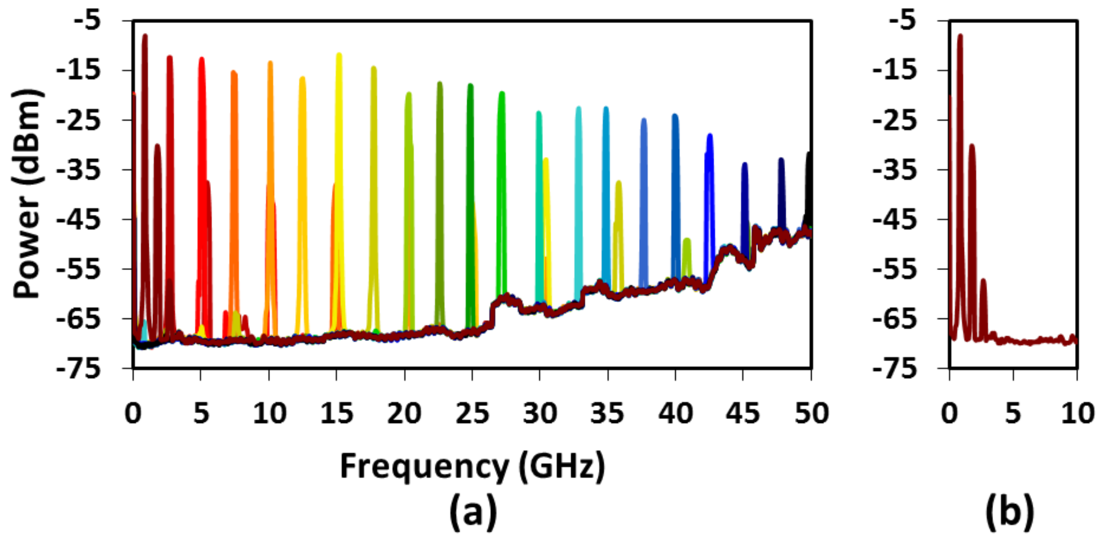


Figure 101. Measured microwave signals with amplifier in the setup for (a) 1 to 50 GHz and (b) the 1 GHz beat tone with harmonics.

The measured linewidth of these devices was high. Figure 102 shows a linewidth of 189 MHz on the ESA. Having two lasers increases the linewidth, especially when considering the jitter from each laser. In this case, only gain pumping used a low noise current source, so the laser frequency was constantly shifting. An attempt was made to lock the two lasers together using an external circuit as shown in Figure 103. The lasers were driven by low-noise ICE laser drivers. The combined laser output was read by an optical spectrum analyzer (OSA). The laser output was also amplified by an erbium-doped fiber amplifier (EDFA) and fed into a lightwave converter where the optical beat-note signal was converted into voltage. This voltage signal was used as feedback to lock the frequency difference between the lasers. The locking utilized the gain pump current to make the small frequency changes that allowed for some locking. This was only marginally successful due to the low-frequency probes used in the laser probe cards. The linewidth was reduced by a factor of 3.

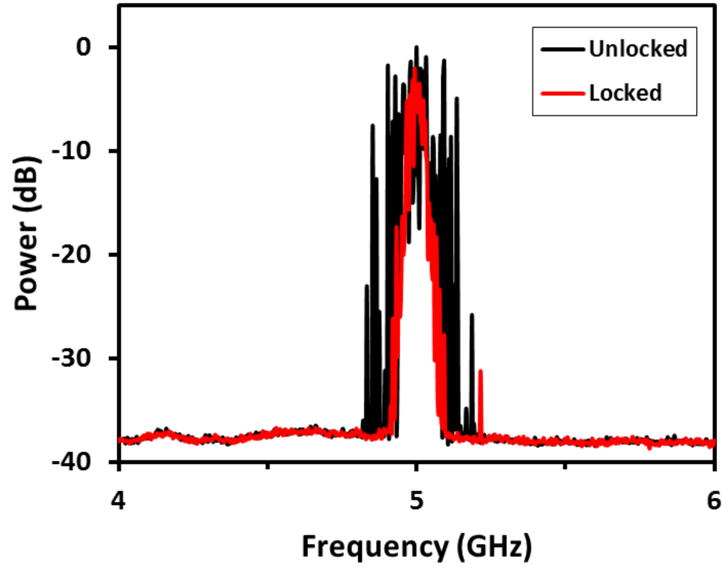


Figure 102. Close-up of microwave signal for locked and un-locked configurations, showing 54 MHz and 189 MHz 3dB linewidth respectively.

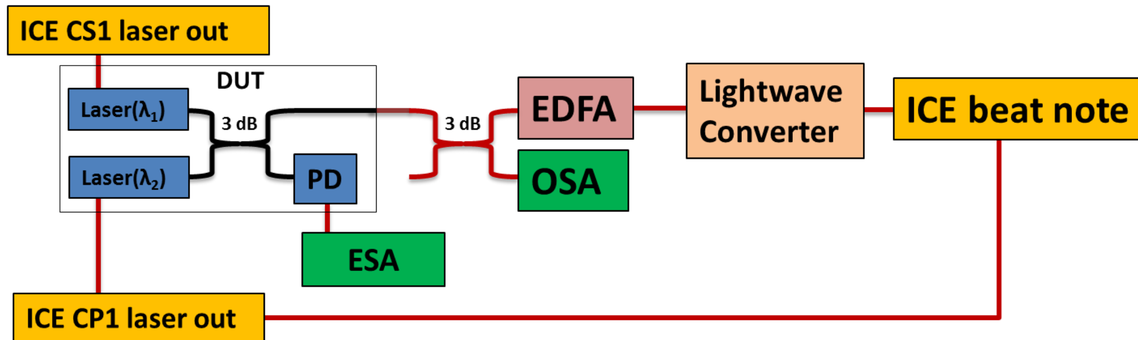


Figure 103. Schematic of locking circuit to maintain frequency difference between lasers.

4.4 Summary

A heterogeneously integrated silicon-III/V PIC was demonstrated including tunable lasers and p-i-n photodiode. By use of an evanescently coupled structure and a thick BCB layer for planarization, this device can achieve a 3-dB O-E bandwidth as wide as 65 GHz, a wide optical operation window (1520 to 1600 nm) with a reasonable internal responsivity (~0.4 A/W), and a high saturation current (9 mA) at 70 GHz operating frequency. Two ring-

based tunable lasers were demonstrated. Tuning of 42 nm was demonstrated with mostly consistent SMSR for the RBR laser. Both lasers exhibit linewidths below 300 kHz. The photodiode and lasers were integrated to demonstrate on-chip microwave generation. Signals from 1 to 112 GHz were achieved. These are excellent results for a fully integrated chip.

Future improvements can be made to individual components. The RBR laser should be the laser of choice due to its simple operation and low linewidth. The output power can be raised by increasing mirror reflectivity and optimizing ring coupling through more precise processing. The speed and saturation power of the photodiode can be further improved by replacing the p-i-n PD with a UTC-PD structure. These changes would improve the output power and extend the bandwidth range of this device.

This device shows that the heterogeneous silicon-InP platform is a viable option as a key component in MMW-over-fiber systems.

This work was supported by Keysight Technologies.

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Chapter 5

Conclusion and Next Steps

Photonic integration will continue to grow. The industry is constantly moving to make things smaller, faster, cheaper, and higher performing, all of which can be achieved by higher levels of integration. The heterogeneous silicon-III/V platform offers a way forward. Here we have explored one of the basic building blocks of photonics, the tunable laser, and seen how this platform offers new options for mirror filters. We also saw a glimpse into how versatile a tunable laser is in its applications by looking at two fully integrated PICs.

We have looked at free-space beam-steering, driven in one axis by a tunable laser. A steering window of 23° (ψ) x 3.6° (θ) was demonstrated with 23 x 6 resolvable spots. This is a viable configuration for use in vehicle LIDAR.

We have looked at photonic microwave generation, again driven by tunable lasers. Microwave generation was achieved from near DC to 112 GHz. Also, a fast waveguide photodiode was designed with a 3 dB frequency roll-off of 65 GHz. This is a viable option as a key component in MMW-over-fiber systems.

Clearly the heterogeneous silicon-III/V platform has much to offer.

Tunable lasers: next steps

There are many possible changes to the tunable lasers. The most pressing ones are included here. First, although it did not perform the best in terms of output power, the ring-bus-ring design is the most promising. It was consistent in output power, SMSR, and had the most straightforward wavelength tuning map. A correction to the process such that the ring coupling and the loop-mirror reflectivity are optimized would improve the power. Also, at the time of fabrication there was no silicon-etch laser monitor, meaning the etch depth was not precise. This led to a choice of deeply etching the waveguides to reduce the number of variables in the directional couplers. However, it was found on Fabry-Perot test structures that deeply etched waveguides under the III/V greatly reduced the optical output power. Further work should use partially etched waveguides.

Beam-steering: next steps

There are several areas in which the beam-steering chip can be improved. First, the process must be altered so the phase-modulators do not operate thermo-optically. This will reduce heating on-chip and remove thermal crosstalk between channels. Second, the amplifiers should be reduced in length. This will remove noise and will also greatly reduce heating. They might also be laid out in a staggered configuration to spread out the heat. Third, additional channels could be added to increase the number of resolvable spots. Fourth, the on-chip feed-back system should be reexamined to get it operational. Fifth, the output channel spacing should be optimized to reduce the side lobes for all angles of steering, similar to recent work done by Hutchison et al. [1]. Sixth, an improved version of the laser should be used. Finally, one of the biggest challenges with these chips is the heat

dissipation. Flip-chip bonding the chip to place the III/V amplifiers in contact with the cooling source would greatly improve the output power.

Photonic microwave generation: next steps

Future work on the microwave generator should focus on improving the RF linewidth. This would require more stable electrical sources and packaging the device. Some of the instability is attributed to poor contact between the probe pads and the probe card.

Also, the large linewidth did not allow for use of the phase modulator. By modulating the phase of the laser additional RF tones would be present in the output signal. These tones allow for interesting measurements, such as measuring the dispersion of an electrical device.

Finally, the next iteration of the photonic microwave generator is a pair of tracking photonic microwave generators. This was fabricated on the same chip but was not tested due to some errors in one of the components. This device uses two fixed DFB lasers locked at an offset frequency. A shared tunable laser is then used to generate a beat tone with both lasers on separate photodiodes. This creates two microwave signals at a fixed offset from each other.

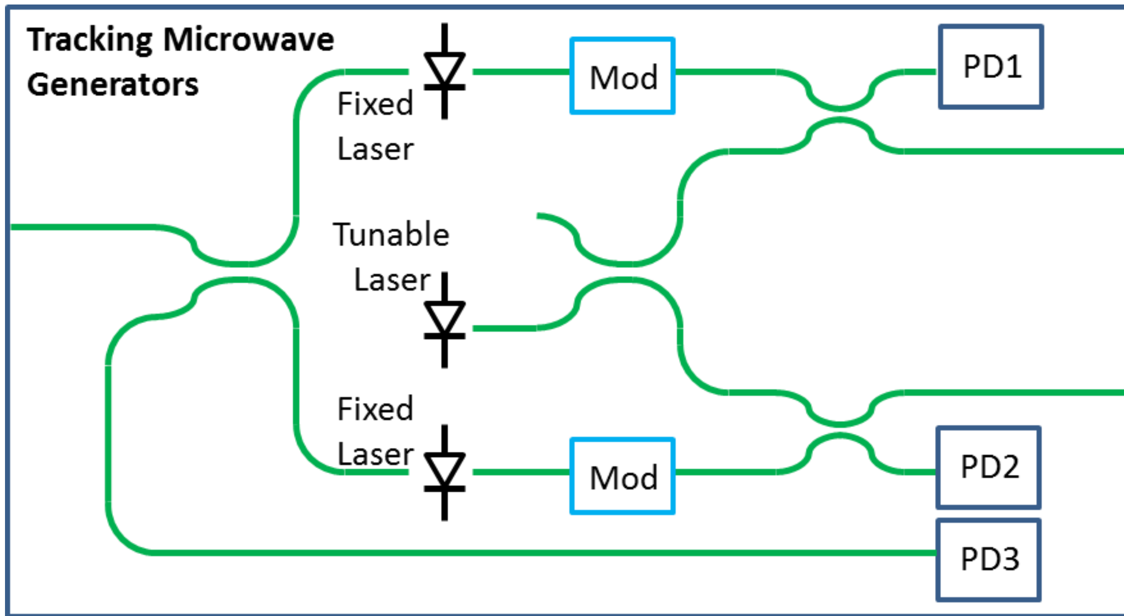

Figure 104. Schematic of tracking photonic microwave generators.

References

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Appendix A – Recipes

	RECIPE	Step	Gas flows (SCCM)	Pressure (mT)	Power / Bias	Time
1	AR2-600 Etch	Chamber Prep	45 – O_2	50	300 W	300 s
		Etch	20 – O_2	10	100 W	30 s
2	O2 descum		100 – O_2	300	100 W	Variable
3	InP MHA etch	Chamber clean	20 - O_2	125	500 V	30 m
		Chamber season	CH_4/H/Ar - 4/20/10	75	500 V	20 m
		Etch	CH_4/H/Ar - 4/20/10	75	500 V	25-35 m
		O2 clean	20 - O_2	125	300 V	10 m
4	O2 ash (recipe 306)		450 – O_2	50	900 W	40 m

Table 4. Some dry recipes.

	RECIPE	Use	Mixture	Temp	Notes
1	Piranha	Si cleaning	H2SO4:H2O2 3:1	80C	Acid can be heated to 80°C before adding
2	Dilute phosphoric acid	InGaAs etch	H_3PO_4:H_2O_2:H_2O 1:1:38		Used for slow, controlled etch
3		InP etch	HCl:H_2O 1:2		

Table 5. Some wet recipes.

Appendix B – Epi

EPI - E1 (6QW)

	Layer Name	Material	Thickness (um)	Doping (cm3)
0	**Substrate**	N-InP substrate	360	S-doped 2~8e18
1	**Buffer**	U-InP buffer layer	0.5	
2	**Etch stop**	P-InGaAs	0.05	1.00E+19
3	**P-sacrificial**	P-InP	0.02	1.00E+18
4	**P-contact**	P-$In_{0.53}Ga_{0.47}As$	0.2	1.00E+19
5	**Grading**	P-1.5Q $In_{0.586}Ga_{0.414}As_{0.888}P_{0.112}$	0.025	3.00E+18
6	**Grading**	P-1.3Q $In_{0.729}Ga_{0.271}As_{0.587}P_{0.413}$	0.025	3.00E+18
7	**P-cladding**	P-InP	1	1.50E+18
8	**P-cladding**	P-InP	0.2	8.00E+17
9	**P-cladding**	P-InP	0.25	5.00E+17
10	**Old Etch stop**	P-1.05Q $In_{0.9029}Ga_{0.0971}As_{0.213}P_{0.787}$	0.015	5.00E+17
11	**P-cladding**	P-InP	0.015	5.00E+17
12	**P-SCH**	P-$In_{0.528}Al_{0.131}Ga_{0.341}As$	0.125	1.00E+17
13	MQW	U-6 x $In_{0.653}Al_{0.055}Ga_{0.292}As$ Well (+0.85% CS)	0.007	
		U-7 x $In_{0.450}Al_{0.089}Ga_{0.461}As$ Barrier (-0.55% TS)	0.01	
		λPL = 1545 nm		
14	**N-SCH**	N-$In_{0.528}Al_{0.131}Ga_{0.341}As$ SCH	0.125	1.00E+17
		λg = 1360 nm		
15	**N-Contact**	N-InP	0.25	1.00E+18
16	**Superlattice**	2 x N - $In_{0.850}Ga_{0.150}As_{0.327}P_{0.673}$	0.0075	1.00E+18
		2 x N - InP	0.0075	
17	**Bonding layer**	N-InP	0.01	1.00E+18
18	**Cap layer**	N-InGaAs	0.2	1.00E+18

Table 6. Layer stack for epi E1 (6 quantum wells).

EPI-E (8QW) GAIN

	Layer Name	Material	Thickness (um)	Doping (cm3)
0	**Substrate**	N-InP substrate	360	S-doped 2~8e18
1	**Buffer**	U-InP buffer layer	0.5	
2	**Etch stop**	P-InGaAs	0.05	1.00E+19
3	**P-sacrificial**	P-InP	0.02	1.00E+18
4	**P-contact**	P-$In_{0.53}Ga_{0.47}As$	0.2	1.00E+19
5	**Grading**	P-1.5Q $In_{0.586}Ga_{0.414}As_{0.888}P_{0.112}$	0.025	3.00E+18
6	**Grading**	P-1.3Q $In_{0.729}Ga_{0.271}As_{0.587}P_{0.413}$	0.025	3.00E+18
7	**P-cladding**	P-InP	1	1.50E+18
8	**P-cladding**	P-InP	0.2	8.00E+17
9	**P-cladding**	P-InP	0.25	5.00E+17
10	**Legacy etch stop**	P-1.05Q $In_{0.9029}Ga_{0.0971}As_{0.2130}P_{0.7870}$	0.015	5.00E+17
11	**P-cladding**	P-InP	0.015	5.00E+17
12	**P-SCH**	P-$In_{0.528}Al_{0.131}Ga_{0.341}As$	0.015	1.00E+17
13	MQW	U-8 x $In_{0.653}Al_{0.055}Ga_{0.292}As$ Well (+0.85% CS)	0.007	
		U-9 x $In_{0.450}Al_{0.089}Ga_{0.461}As$ Barrier (-0.55% TS)	0.01	
		λPL = 1545 nm		
14	**N-SCH**	N-$In_{0.528}Al_{0.131}Ga_{0.341}As$ SCH	0.125	1.00E+17
		λg = 1360 nm		
15	**N-Contact**	N-InP	0.11	1.00E+18
16	**Superlattice**	2 x N - $In_{0.850}Ga_{0.150}As_{0.327}P_{0.673}$	0.0075	1.00E+18
		2 x N - InP	0.0075	
17	**Bonding layer**	N-InP	0.01	1.00E+18
18	**Cap layer**	N-InGaAs	0.2	1.00E+18

Table 7. Layer stack for epi E (8 quantum wells).

EPI-F (7QW) GAIN

	Layer Name	Material	Thickness (um)	Doping (cm3)
0	**Substrate**	N-InP substrate		S-doped 2~8e18
1	**Buffer**	U-InP buffer layer	0.5	
2	**Etch stop**	P-InGaAs	0.05	1.00E+19
3	**P-sacrificial**	P-InP	0.02	1.00E+18
4	**P-contact**	P-$In_{0.53}Ga_{0.47}As$	0.2	1.00E+19
5	**P-cladding**	P-InP	1	1.50E+18
6	**P-cladding**	P-InP	0.2	8.00E+17
7	**P-cladding**	P-InP	0.2	5.00E+17
8	**Legacy etch stop**	P-1.05Q $In_{0.9029}Ga_{0.0971}As_{0.213}P_{0.787}$	0.05	5.00E+17
9	**P-cladding**	P-InP	0.05	5.00E+17
10	**U-GRIN**	P-$Al_xGa_{0.47-x}In_{0.53}As$ (x: 0.34->0.155)	0.1	1.00E+17
11	**MQW**	U-7 x $Al_{0.0600}Ga_{0.2642}In_{0.6758}As$ Well (+1% CS)	0.006	
		U-8 x $Al_{0.0850}Ga_{0.4739}In_{0.4411}As$ Barrier (-0.6% TS)	0.009	
		λPL = 1545 nm		
12	**U-GRIN**	N-$In_{0.53}Al_xGa_{0.47-x}As$ (x:0.155->0.34)	0.1	1.00E+17
		λg = 1360 nm		
13	**N-Contact**	N-InP	0.11	1.00E+18
14	**Superlattice**	2 x N - $In_{0.850}Ga_{0.150}As_{0.327}P_{0.673}$	0.0075	1.00E+18
		2 x N - InP	0.0075	
15	**Bonding layer**	N-InP	0.01	1.00E+18
16	**Cap layer**	N-InGaAs	0.2	1.00E+18

Table 8. Layer stack for epi F (7 quantum wells).

EPI-H (3 QW) Gain

	Layer Name	Material	Thickness (um)	Doping (cm3)
0	Substrate	N-InP substrate		S-doped 2~8e18
1	Buffer	U-InP buffer layer	0.5	
2	Etch stop	P-InGaAs	0.05	1.00E+19
3	P-sacrificial	P-InP	0.05	1.00E+18
4	P-contact	P-$In_{0.53}Ga_{0.47}As$	0.1	1.50E+19
5	Smoothing	P-1.5Q $In_{0.586}Ga_{0.414}As_{0.888}P_{0.112}$	0.025	3.00E+18
6	Smoothing	P-1.3Q $In_{0.729}Ga_{0.271}As_{0.587}P_{0.413}$	0.025	3.00E+18
7	P-cladding	P-InP	1	1.50E+18
8	P-cladding	P-InP	0.2	8.00E+17
9	P-cladding	P-InP	0.25	5.00E+17
10	SCH	N-$In_{0.530}Al_{0.183}Ga_{0.287}As$	0.125	1.00E+17
11	MQW	U-3 x $In_{0.6758}Al_{0.0600}Ga_{0.2642}As$ Well (+1% CS)	0.006	
		U-4 x $In_{0.4411}Al_{0.0850}Ga_{0.4739}As$ Barrier (-0.6% TS)	0.009	
		λPL= 1545 nm		
12	SCH	N-$In_{0.530}Al_{0.183}Ga_{0.287}As$	0.125	1.00E+17
		λg= 1.2 um		
13	N-Contact	N-InP	0.11	2.00E+18
14	Superlattice	2 x N - $In_{0.850}Ga_{0.150}As_{0.327}P_{0.673}$	0.0075	1.00E+18
		2 x N - InP	0.0075	
15	Bonding layer	N-InP	0.01	1.00E+18

Table 9. Layer stack for epi H (3 quantum wells).

EPI - 1360nm Modulator

	Layer Name	Material	Thickness (um)	Doping (cm3)
0	**Substrate**	N-InP substrate		S-doped 2~8e18
1	**Buffer**	U-InP buffer layer	0.5	
2	**Etch stop**	P-InGaAs	0.05	1.00E+19
3	**P-sacrificial**	P-InP	0.05	1.00E+18
4	**P-contact**	P-$In_{0.53}Ga_{0.47}As$	0.1	1.50E+19
5	**Smoothing**	P-1.5Q $In_{0.586}Ga_{0.414}As_{0.888}P_{0.112}$	0.025	3.00E+18
6	**Smoothing**	P-1.3Q $In_{0.729}Ga_{0.271}As_{0.587}P_{0.413}$	0.025	3.00E+18
7	**P-cladding**	P-InP	1	1.50E+18
8	**P-cladding**	P-InP	0.25	8.00E+17
9	**P-cladding**	P-InP	0.25	5.00E+17
10	**SCH**	N-$In_{0.5284}Al_{0.1930}Ga_{0.2786}As$	0.1	1.00E+17
11	**MQW**	U-15 x $In_{0.574}Al_{0.111}Ga_{0.315}As$ Well (+0.3% CS)	0.008	1.00E+17
		U-16 x $In_{0.468}Al_{0.217}Ga_{0.315}As$ Barrier (-0.41% TS)	0.005	1.00E+17
		λPL= 1360 nm		
12	**SCH**	N-$In_{0.5284}Al_{0.1930}Ga_{0.2786}As$	0.05	3.00E+18
		λg= 1.25 um		
13	**N-Contact**	N-InP	0.11	3.00E+18
14	**Superlattice**	2 x N - $In_{0.850}Ga_{0.150}As_{0.327}P_{0.673}$	0.0075	1.00E+18
		2 x N - InP	0.0075	
15	**Bonding layer**	N-InP	0.01	1.00E+18

Table 10. Layer stack for modulator epi.

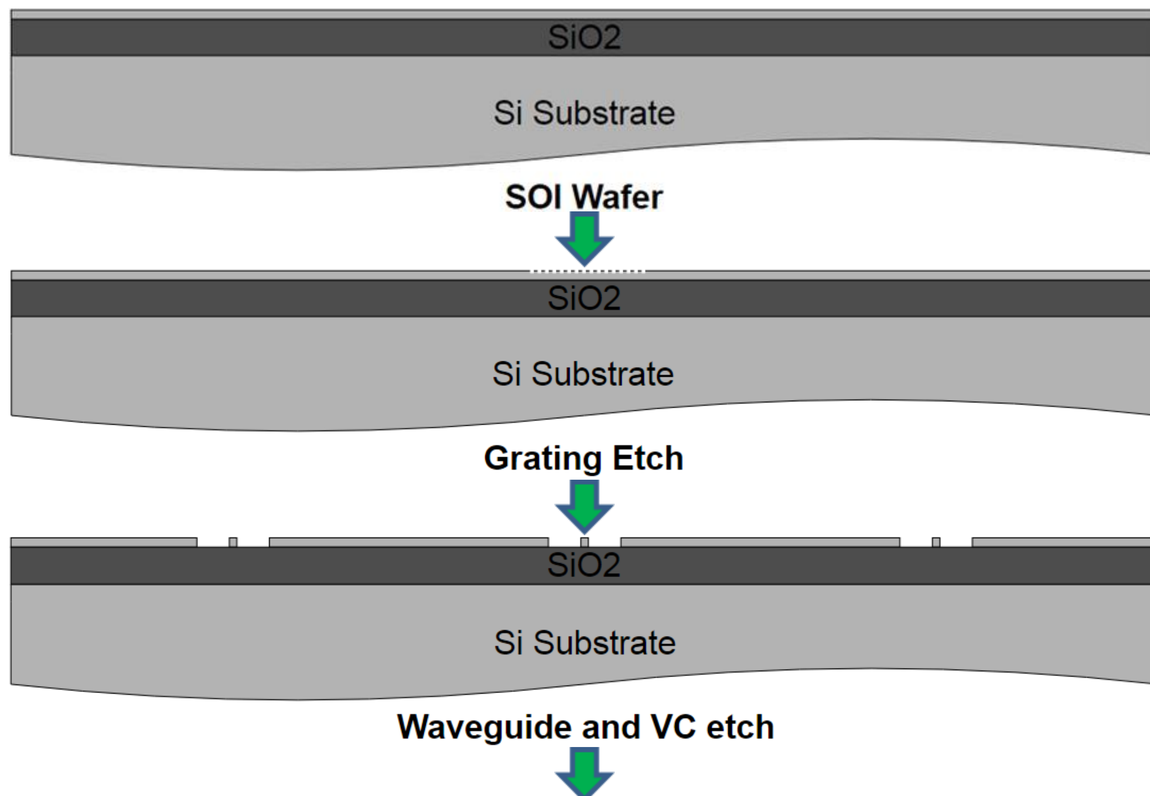
EPI - PD-J Photodiode

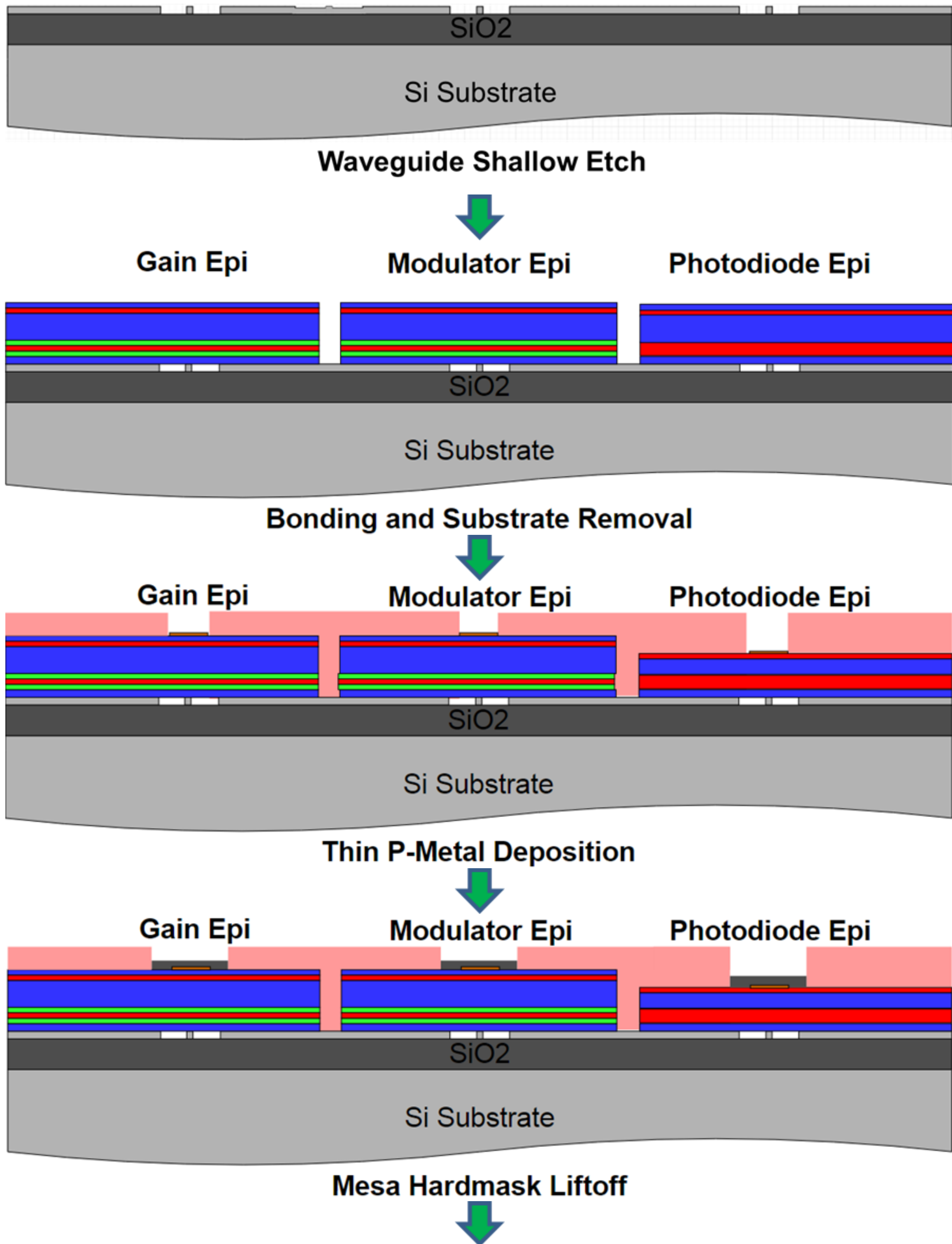
	Layer Name	Material	Thickness (um)	Doping (cm3)
0	**Substrate**	N-InP substrate		S-doped 2~8e18
1	**Buffer**	U-InP buffer layer	0.5	
2	**Etch stop**	P-$In_{0.53}Ga_{0.47}As$	0.05	1.00E+19
3	**P-sacrificial**	P-InP	0.02	1.00E+18
4	**P-contact**	P-$In_{0.53}Ga_{0.47}As$	0.2	1.00E+19
5	**Grading**	P-1.25Q $In_{0.729}Ga_{0.271}As_{0.587}P_{0.413}$	0.025	3.00E+18
	Grading	P-1.05Q $In_{0.9029}Ga_{0.0971}As_{0.2130}P_{0.7870}$	0.025	3.00E+18
7	**P-cladding**	P-InP	1	1.50E+18
8	**P-cladding**	P-InP	0.25	8.00E+17
9	**P-cladding**	P-InP	0.25	5.00E+17
10	**Active region**	i-$In_{0.53}Ga_{0.47}As$	0.4	undoped
11	**N-Contact**	N-InP	0.04	3.00E+18
12	**N-Contact**	N-InP	0.11	2.00E+18
13	**Superlattice**	2 x N - $In_{0.850}Ga_{0.150}As_{0.327}P_{0.673}$	0.0075	1.00E+18
		2 x N – InP	0.0075	
14	**Bonding layer**	N-InP	0.01	1.00E+18
15	**Cap layer**	N-$In_{0.53}Ga_{0.47}As$	0.2	1.00E+18

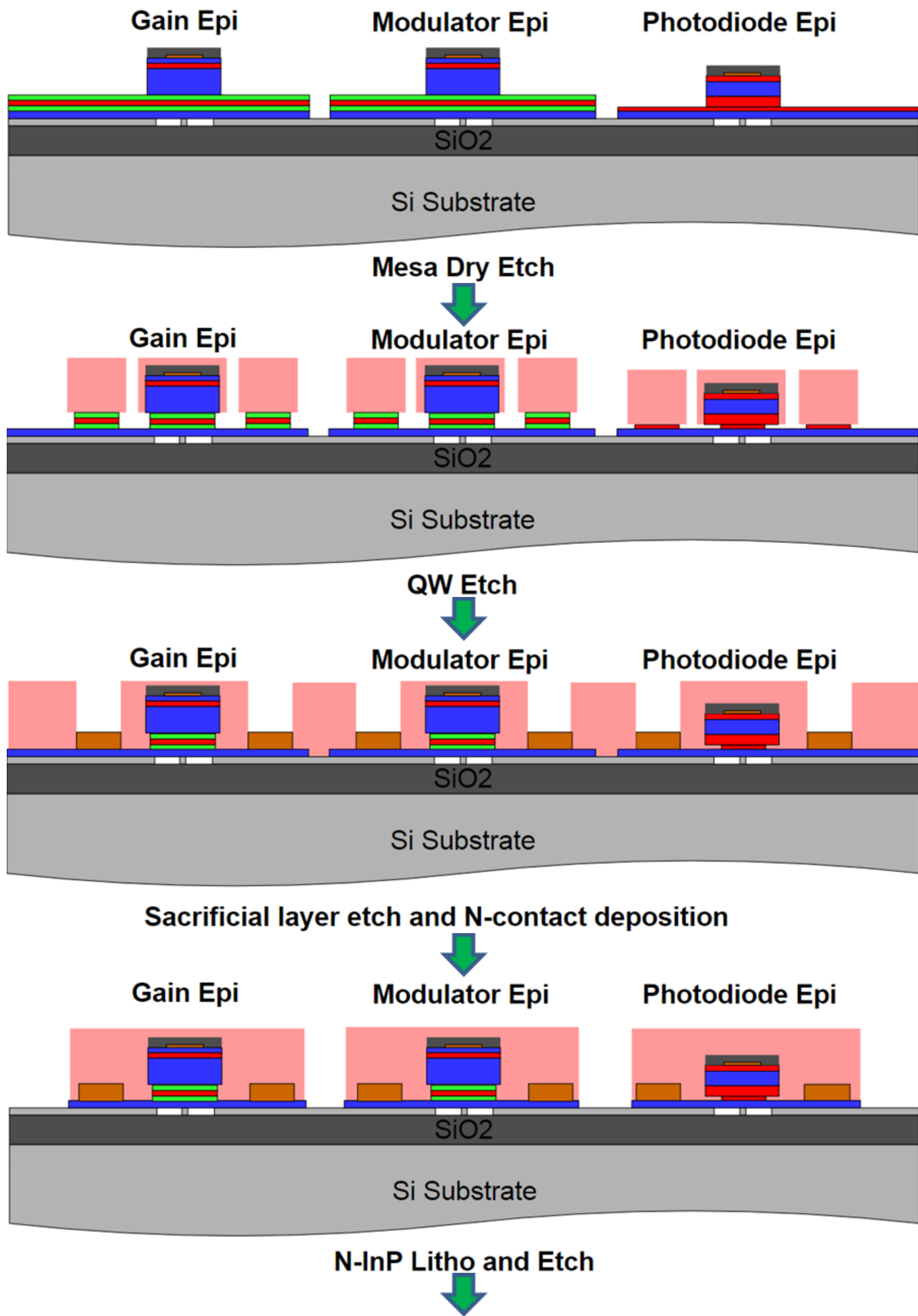
Appendix C – Heterogeneous Silicon-III/V Platform Process

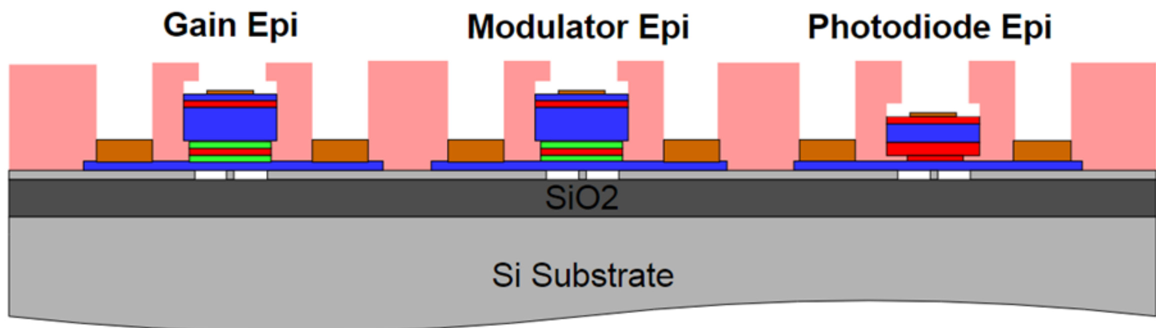
For the devices described in this work the silicon and III-V wafer growth and ion implantation were performed by outside vendors. The remainder of the process took place at the Nanofab at the University of California at Santa Barbara (UCSB).

The process combines waveguides and other passive silicon elements with various III/V capabilities by directly bonding InP pieces onto the processed silicon wafer. The InP elements are then defined using photolithography aligned to the silicon wafer. This chapter will detail the process used in making the devices described in this work. Over time, many of these processes changed, either due to improvements in the process or changes in available resources. The most up to date methods will be described here. A set of conceptual cross-sectional illustrations are shown here to visually represent the process.

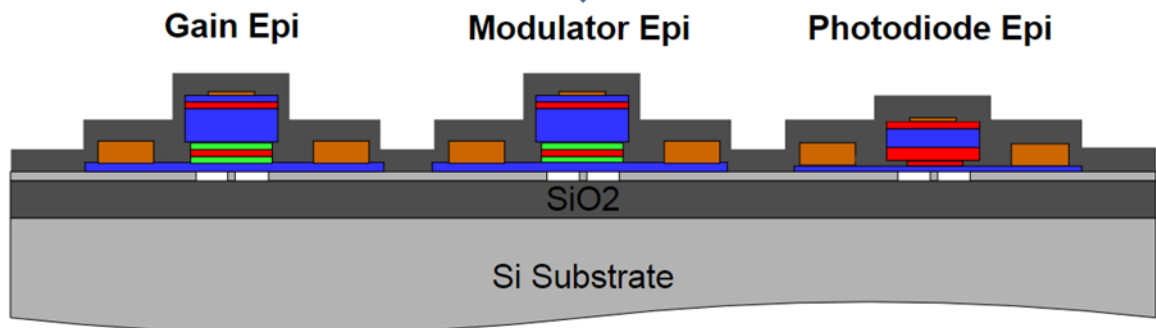



SiO2
Si Substrate
Waveguide Shallow Etch
Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
Bonding and Substrate Removal
Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
Thin P-Metal Deposition
Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
Mesa Hardmask Liftoff

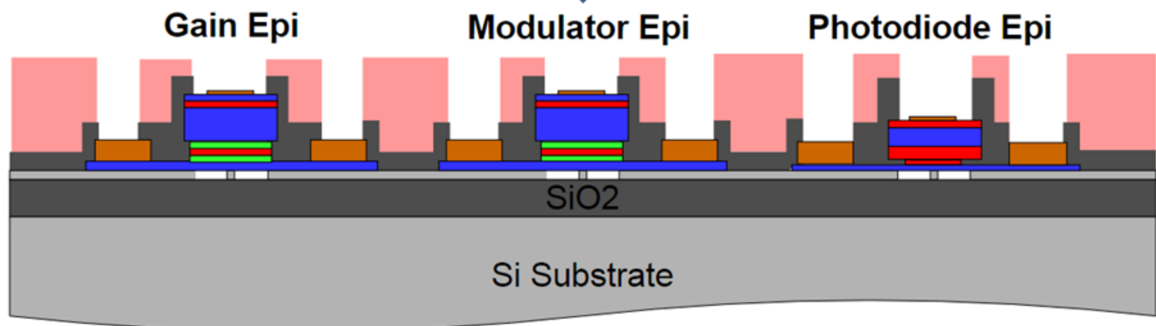

Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
Mesa Dry Etch
Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
QW Etch
Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
Sacrificial layer etch and N-contact deposition
Gain Epi
Modulator Epi
Photodiode Epi
SiO2
Si Substrate
N-InP Litho and Etch



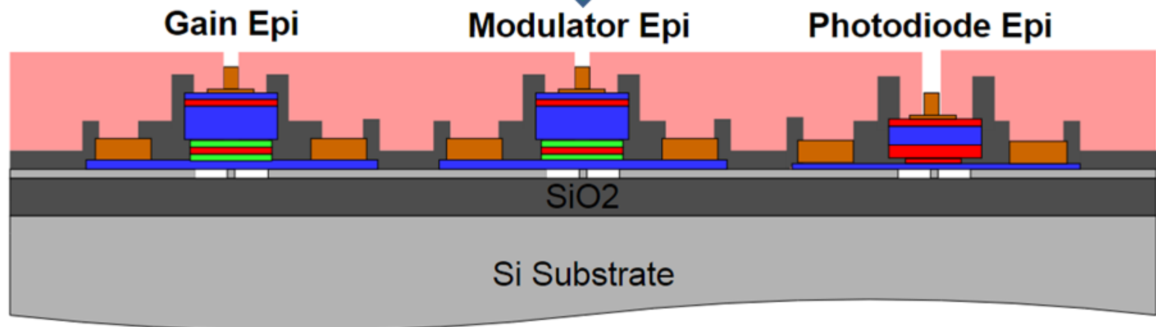
P hardmask cleanup



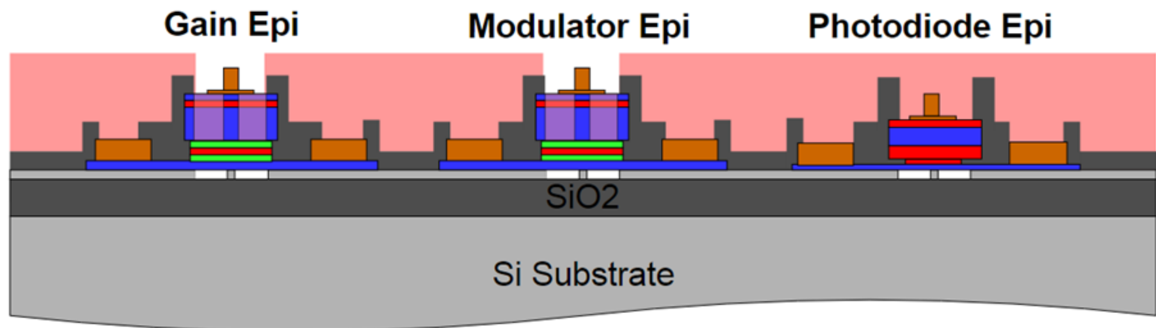
Buffer Layer Deposition



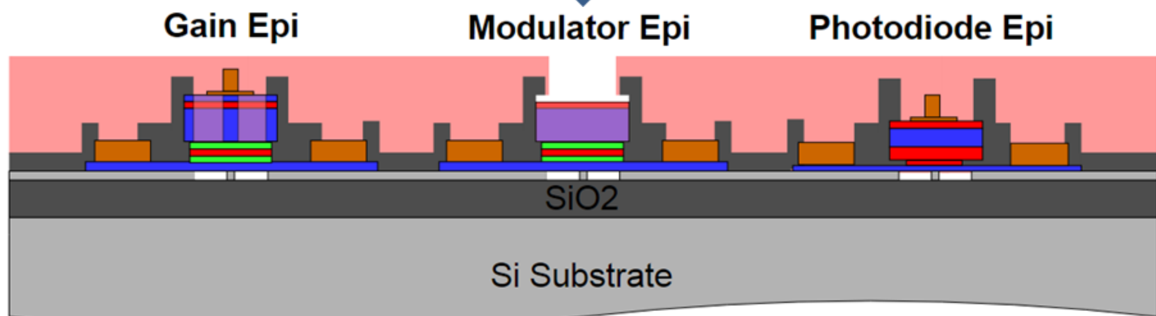
Via Litho and Etch



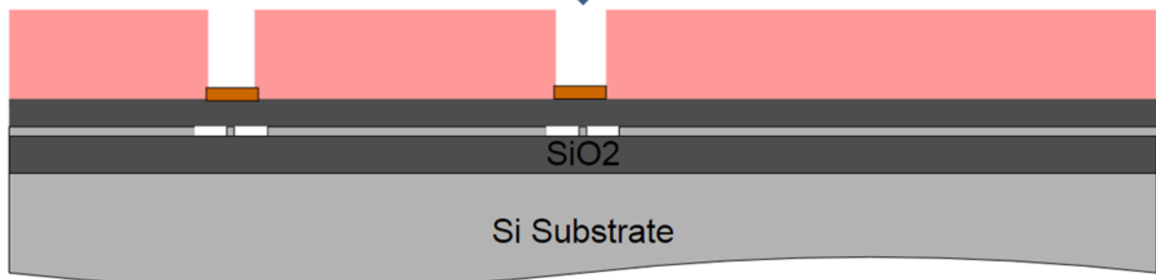
P-Metal Deposition



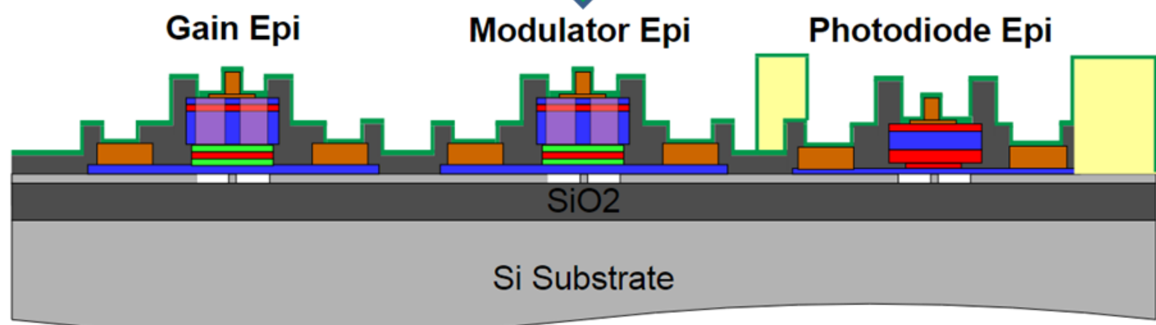
Ion Implantation



Isolation Etch
(on modulator epi without thin p-metal)



Heater deposition
(over waveguides)



Bottom nitride deposition, BCB spin and litho, top nitride deposition

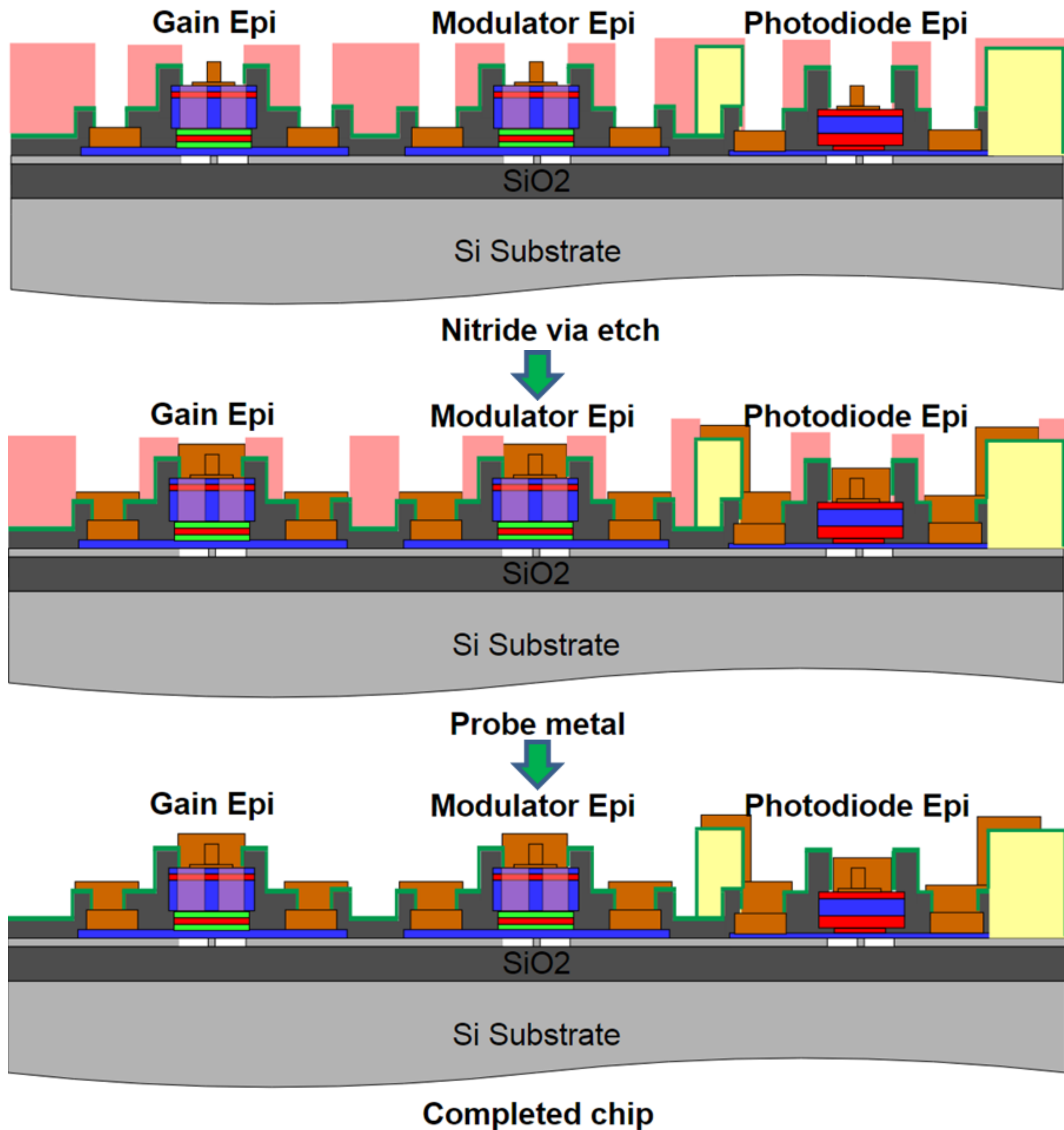


Figure 105. Conceptual illustrations of semiconductor process with three epi stacks.

C.1 Photolithography

The various photolithography methods used in the fabrication process will be described first. I-line lithography is most commonly used and employs several photoresist (PR) types. Deep ultra-violet (DUV) lithography is used for waveguide definition. E-beam lithography (EBL) is used for very fine features such as sub-wavelength gratings.

I-line lithography

I-line lithography in this work uses four different resist thicknesses: SPR 955 CM-0.9, SPR 955 CM-1.8, SPR 220-3 and SPR 220-7 where the final number denotes thickness in µm at typical spin speeds. First, HMDS adhesion promoter is puddled on the wafer for 20 seconds, and then spun off using spin recipe 7 (Table 11). The wafer is baked at 125˚C for 3 minutes to ensure the HMDS has been removed from any partially enclosed channels. Then the resist is applied and spun on, followed by a soft bake typically of 90 seconds at 95˚C for thinner resists and 90 seconds at 110˚C for thicker resists. To improve resolution for small features, an anti-reflection coating CEM is sometimes applied to 0.9 µm resist through a filter. The resist is then exposed with the pattern in an I-line Autostepper, CEM, if present, is rinsed off in deionized (DI) water, and a post-exposure bake is performed. The resist is typically developed in AZ726MIF and a 30 second, 100 watt O_2 descum is performed.

Recipe #	Spin Speed (rpm)	Ramp Speed (rpm/s)	Spin Time (s)
1.1	500	400	10
1.2	1500	1000	30
2.1	500	500	10
2.2	4000	400	60
3	2000	400	40
4	2500	500	30
5	3000	600	30
6	3500	700	30
7	4000	800	30
8	5000	1000	30
9	6000	1250	30

Table 11. Photoresist spin bench recipes.

Bi-layer liftoff process

For liftoff patterns required for hard-masks, metal deposition, or particularly difficult etches, a thick layer of PMGI is applied in place of the HMDS. An extra bake is performed before spinning on the upper layer of resist. This bake is ramped to prevent rapid outgassing

which can cause bubbles in the resist, particularly where a trench runs under bonded material. These bubbles can rupture and allow metal to be deposited where it will short-circuit devices or cause excess losses. The hotplate begins at 90˚C and is ramped to 130˚C, where it is held for 30 seconds. Then it is ramped to 155 ˚C, held 30 seconds, and ramped to 180˚C. There is no hold time before ramping to 200˚C where it is held for 120 seconds. The post-exposure bake is removed to avoid cracking in the PMGI. After the initial pattern development, two or three cycles of a 10 minute DUV flood expose followed by a 60 second develop in SAL101A developer is required. This will develop the PMGI while leaving the upper resist pattern intact. It will also undercut the upper layer which is desirable for liftoff patterns.

Deep UV lithography

Deep ultra-violet (DUV) lithography is performed by spinning a 53 nm layer of AR2-600 DUV anti-reflectant using recipe 6, followed by a 3 minute hotplate bake at 220˚C. Next, 650 nm of UV6-0.8 photoresist (PR) is applied (recipe 8) and baked at 135˚C for 1 minute. The resist is exposed in an ASML DUV stepper, baked at 135˚C for 90 seconds, and developed for 15 seconds in AZ300MIF developer. To improve sidewall roughness for small features, the resist is made to reflow slightly by baking it at 140˚C for 3 minutes. Next, a 30 second O_2 ash at 100 W is used to remove the layer of AR2 without damaging the PR pattern.

E-beam lithography

EBL is performed on wafers with only the DUV alignment marks defined to minimize errors caused by feature topology. A layer of CSAR:Anisol 1:1 is spun using recipe 5, and the wafer is baked for 4 minutes at 180˚C. A conducting polymer (Aquasave) is applied

using recipe 5 and then baked at 100˚C for 15 seconds. Ebeam lithography is performed with varying dose and lens based on the desired pattern. Then the conducting polymer is removed with a 30 second DI rinse. The resist is developed in MIBK:isopropyl alcohol (IPA) 1:1 for 60 seconds and then rinsed in MIBK:IPA 9:1 for 20 seconds, followed by an N_2 dry (no DI). After a 7 second O_2 descum the chip is ready for processing.

Removing resist pattern

After processing the chip with the photoresist mask, the resist is typically stripped in 1165 (Microposit Remover 1165) at 80˚C. Two baths are sometimes required for more stubborn resist or for liftoff patterns to ensure the cleanliness of the chip. AR2 and residual resist can be removed with an O_2 ash, or with H_2SO_4:H_2O_2 3:1 (Piranha) when III/V is not present.

C.2 Silicon Process

The process of fabricating PICs using the heterogeneous silicon-III/V platform begins with selecting a silicon on insulator (SOI) wafer with a 500 nm thick top silicon layer and a 1 um thick buried oxide layer. Low surface roughness, typically below 1 nm, is required to achieve a high-yield silicon/InP bond. Due to size limitations of the tools in the UCSB facility, only four-inch silicon wafers are used in this process, however the process itself can accommodate much larger wafers. The silicon process defines alignment marks, waveguides, vertical channels, and sometimes includes silicon phase modulators.

Alignment marks, gratings, waveguides, vertical Channels

The alignment marks are patterned using DUV lithography and etched down to the buried oxide. All silicon etching is done using deep reactive-ion etching (DRIE). EBL and

DRIE is then used to define gratings for DFB mirrors (< 20 nm) and vertical grating emitters (170 nm), and to etch holes of variable width for an in-plane Fourier lens (50 nm). More DUV lithography and DRIE is used to form a deep waveguide layer. This step is repeated with a rib waveguide mask and the silicon is etched to a depth typically between 200 and 300 nm. The rib waveguides are used in most areas of the mask to prevent high propagation losses and the deeply etched waveguides are used in devices that are highly sensitive to small process variations. The deep etch is also used to define a grid of vertical channels throughout the die improve bonding yield by allowing the bond to relax.

Silicon implantation

For devices with silicon phase modulators (Chapter 3) the chip is patterned with 1.8 um resist. It is implanted with a phosphorus dose of 8e14 cm^{-2} at an energy of 90 keV and the resist is removed. This is repeated with a different pattern and the chip is implanted with a boron dose of 8e14 cm^{-2} at an energy of 50 keV. These make up the n- and p- regions of the silicon phase modulator. After stripping the resist the chip is annealed at 900°C for 10 minutes to activate the dopants. On chips where the III/V was bonded across the whole die, metallization of the modulator contacts was delayed until after most of the III/V process to avoid particles that would reduce bond yield. Delaying the metallization caused greater contact resistance and hurt the performance of these modulators on some chips. A better solution may have been to add a thin contact metal in a trench before bonding.

The silicon is cleaned aggressively to ensure a smooth interface for III/V bonding.

C.3 Heterogeneous Bonding

Heterogeneous bonding allows the InP to be placed with coarse alignment and then patterned with fine alignment using marks defined in the silicon. Different III/V epitaxial (epi) material stacks can be placed on the same die to optimize different devices such as lasers, modulators and photodiodes. One or more III/V pieces are cleaved to the desired dimensions and then carefully cleaned in 1165. The pieces are examined and gently swabbed in isopropyl alcohol if large particles are found, although any handling of III/V should be avoided if possible. If present on the epi stack, the InGaAs cap layer is removed in dilute phosphoric acid (H_3PO_4:H_2O_2:H_2O, 1:1:38) for 5 minutes. The epi pieces and the silicon wafer are then placed in an EVG O_2 plasma activation chamber which forms a thin layer (~10 nm) of SiO2.

The top of the III/V is placed in contact with the silicon by means of vacuum tweezers for rough alignment. For tighter alignment tolerances, such as those needed when bonding multiple epi stacks to the same die, a flip-chip bonder is used. Then the wafer is moved into a bonding fixture that exerts 1 MPa of pressure. The fixture is placed in a 300 ˚C oven for 1 hour to improve the bonding strength. A 1 μm layer of SiO2 is deposited to protect the sides of the epi, and crystal wax is pressed up to the edges and between the epi pieces as an added layer of protection. This greatly reduces the undercut to the epi stack during wet removal.

The InP substrate, which is now the uppermost section, is mostly removed by mechanical polishing, leaving 50-100 um of total epi height. Removing more mechanically requires highly accurate leveling to avoid destroying epi in some areas. Instead, the remaining InP substrate is removed in HCl:DI (3:1) at an etch rate of about 4 um per minute. The wet etch is crystallographic and stops on the InGaAs layer, but can leave tall

mountainous InP structures at opposite edges of the epi piece. For this reason it is important to mechanically polish as much as possible, and to allow the epi to overlap the edge of the die in the direction the mountains form. If any mountains are present due to the limitations of the fabrication facility, thick PR is applied, and the mountains can be carefully removed with mechanical force.

Before removing the resist, the chip is baked at 200°C for 30 seconds to create a controlled environment for bond failure. Regions without vertical channels or waveguide trenches are typically filled with large bubbles in the epi, which is why blank regions of the mask are populated with vertical channels. In regions where the bond strength is poor, such as these bubbles, the epi sometimes ruptures during bakes as the gas expands. Devices in these regions may be ruined but so will other devices where particles are redeposited. Redeposition is minimized by inducing the ruptures while the chip is covered with thick PR.

The PR is stripped in 1165 and the epi is gently swabbed in a surfactant (Tergitol) to further clean the surface. Finally the InGaAs etch-stop layer is removed in dilute phosphoric acid (H_3PO_4:H_2O_2:H_2O, 1:1:38).

C.4 Heterogeneous Process

Pre-p-metal

After bonding is completed a thin p-metal layer is defined using a bilayer liftoff process defined with I-line lithography. Depositing this layer prior to most of the III/V processing results in much lower and consistent contact resistances. The p-sacrificial layer is etched off (HCl:H_2O, 1:2) and the metal is deposited (Pd/Ti/Pd/Au/Ti, 3/17/17/200/30 nm). Liftoff is completed in consecutive 10 minute 80°C 1165 soaks as needed.

Mesa etch

The III/V mesa pattern is defined using SF-11 resist as an undercut layer, and UV6 DUV resist. An SiO_2 hard mask is deposited between 250 and 300 nm, and the resist and excess SiO_2 is lifted off in 1165. The mesa pattern is larger than the thin p-metal so the metal is completely covered by the hard mask. Any metal exposed during the etch can be partially sputtered off by argon gas. This metal can redeposit on the chip and create small masked regions around the mesa, forming unwanted pillars as the etch continues.

The mesa is etched in a reactive ion etching (RIE) chamber flowing MHA (CH_4/H/Ar 4/20/10 SCCM) at 75 mT, with a 500 V bias. The etch time varies based on the amount of III/V material exposed but a laser etch monitor makes clear the transition between layers. For laser and modulator epi the etch should finish in the quantum well region, and for p-i-n photodiode epi the etch should finish in the intrinsic region. Material layer thicknesses were chosen to allow them to be etched simultaneously. Loading InP dummy pieces are placed around the die to provide a more uniform etch. The edges of the die typically etch faster as they are more exposed to the gases. One way to circumvent this is to leave most of the die un-etched, except around the mesas. These regions can be wet-etched later.

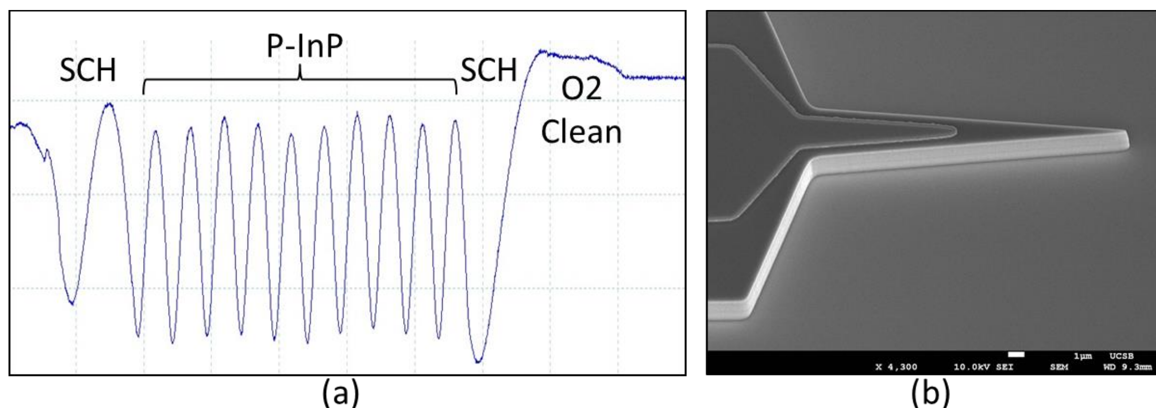


Figure 106. (a) Typical etch rate monitor trace during MHA dry etch for mesa definition of gain epi stack. The etch is finished approximately one

period past the material change, or about halfway through the n-side separate confined heterostructure (SCH) layer. (b) SEM image of a typical etched mesa taper with pre-p-metal.

Mesa fill hardmask etch

Before more of the epi is removed, and consequently exposes the silicon, the hardmask which covers the mesa fill areas needs to be removed. The mesa fill etch uses 7 μm resist spun at recipe 5 with a long exposure time. With resist this thick it is important to delay before the post-exposure bake or the resist will bubble. A wait time of 60 minutes was used for excess safety. After development the resist was reflowed at 115˚C for 5 minutes. Then a 2 minute BHF was used to remove the SiO_2 hardmask. The remainder of the mesa fill area will be removed later in the process.

Quantum well etch

The quantum well etch, or the absorber layer etch for PDs, is defined with I-line lithography and 1.8 μm resist. The active layer is removed with H_3PO_4:H_2O_2:H_2O 1:5:15 down to the n-contact layer which works as an etch-stop. This removes any height variance from the dry etch. It is desired that the etch undercuts the resist mask. A desired undercut of ~700 nm is confirmed by measuring in a confocal microscope. During the etch the color of the epi will change. In particular, the regions with vertical channels underneath will appear pink. About 10 seconds after the color change is complete gives the appropriate undercut. Extra 10 second etches can be performed if needed. The quantum well region directly over the n-contacts is not etched until immediately before metal deposition. The resist is stripped in 1165.

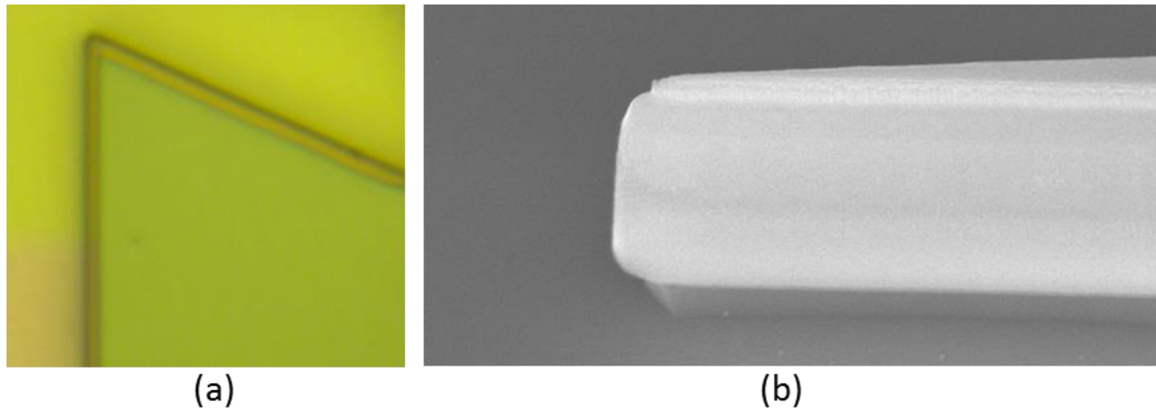


Figure 107. (a) Microscope image showing the undercut of the quantum well etch with photoresist intact. (b) SEM of an undercut mesa tip after resist has been stripped.

N-metal deposition

N-contact lithography is formed using a bilayer process with PMGI SF-15 as the bottom layer and 1.8 µm resist spun for the upper. After exposure and development, the chip is subjected to 4 minutes of O2 plasma at 300mT and 100W to remove any residual resist. The quantum well and SCH layers are etched off with the same phosphoric acid mixture used for the quantum well etch. The vertical channels in this region should be clearly defined and pink. The etch should be performed immediately before loading the chip for e-beam metal deposition. The layer stack for n-contacts is Pd/Ge/Pd/Au/Ti 10/110/25/1000/25 nm. Resist is stripped in 1165.

N-InP etch

The final layers of III/V for most of the chip are removed in the N-InP etch. An 8 minute 150˚C dehydration bake is performed prior to lithography using 1.8 µm resist. The resist is overexposed (about 60%) to narrow the taper tip which overlays the silicon waveguide. This is important for minimizing reflections in the transition from silicon to III/V. After development the resist is hard baked at 135˚C for 5 minutes, followed by a 60 second O_2

descum. Then an MHA etch, similar to the one detailed for the mesa etch, is performed. The difference is that the bias voltage is only 200V this time, and the etch lasts for about 14 minutes. After the etch monitor trace flattens out an extra 3 minutes of etch is added for a total of about 17 minutes.

The MHA etch tends to polymerize the resist, making it difficult to remove at feature edges. This is solved by performing a 40 minute O_2 ash with 450 SCCM O_2 at 50 mT with 900 W ICP power. The ash removes the polymer buildup from the MHA etch and the remaining resist is removed in 1165.

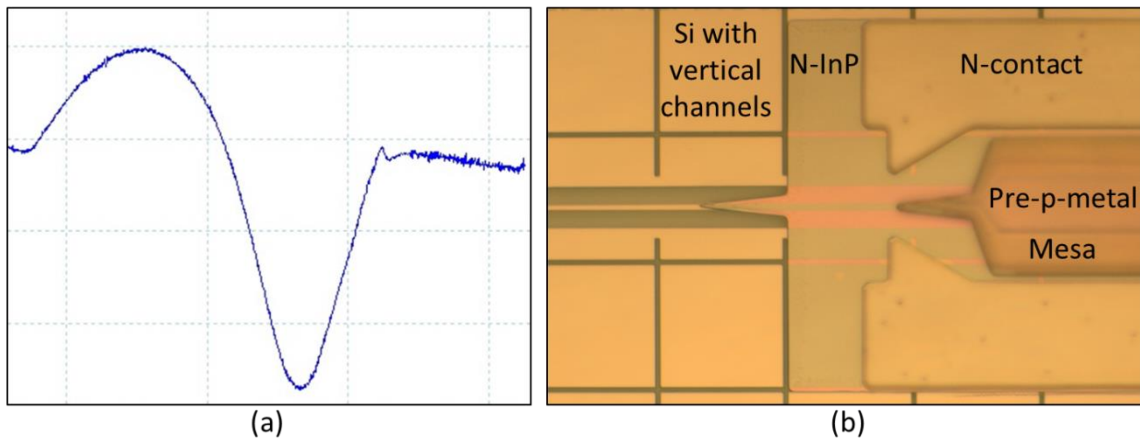


Figure 108. (a) Typical etch rate monitor trace during MHA dry etch for n-InP layer. Approximate time is 17 minutes, including 3 minutes of flat trace. (b) Microscope image

Mesa fill etch

Later processing iterations have disposed of loading epi during the mesa etch. Instead, the mesa etch is only performed on the regions around the mesas. This ensures even better uniformity than the loading epi provides, and is much simpler to fabricate. However, it leaves epi over the waveguides in many places that needs to be removed.

The mesa fill etch uses 7 μm resist spun at recipe 5 with a long exposure time and the 60 minute wait time before post exposure bake. After development and descum a 3 minute resist reflow was performed at 135˚C. Then the mesa fill areas were completely wet etched.

The wet etch process used is as follows: First 2 minutes of H_3PO_4:HCl:H_2O 1:1:1 removes the InP p-sacrificial layer. Then the p-contact InGaAs is etched in 2 minutes of H_3PO_4:H_2O_2:H_2O 1:5:15. H_3PO_4:HCl 3:1 removes p-InP cladding region in 7 minutes with additional 1 minute increments as needed. The mesa fill height is measured by Dektak to determine if when this is finished. Next, the active layer is removed in 2 minutes of H_3PO_4:H_2O_2:H_2O 1:5:15. The vertical channels should appear pink at this point. Then the InP n-contact is removed in H_3PO_4:HCl:H_2O 1:1:1 in 2 minutes. Finally two to three cycles of alternating between 30 second InGaAsP etches with H_2SO_4:H_2O_2:H_2O 1:1:10 (cooled for 10 minutes after mixing) and InP etches with H_3PO_4:HCl:H_2O 1:1:1 removes the super-lattice and bonding layers. Finally the photoresist is stripped in 80˚C 1165.

Mesa hardmask clean

Some of the previous processes can leave some amount of polymer and scum. It is important to remove this before the p-metal is deposited. To that end the via mask is used to expose the important regions. The chip is spun at recipe 4 with 1.8 μm resist, exposed and developed. A 2 minute O_2 descum is performed, and then a 15 second BHF dip is used to remove both the scum and part of the remaining hardmask on the mesa. The resist is stripped in 80˚C 1165.

Oxide cladding and via etch

A 900 to 1000 nm SiO_2 layer is deposited. This acts both as a top cladding for the waveguides and as an electrical barrier between n- and p-contacts. After deposition the via

lithography is defined using 3 μm resist spun with recipe 3. Then vias are etched down to the pre-p-metal and the n-metal using CF_4/O_2 50/5 SCCM at 2 Pa. with 500 W forward power. This takes approximately 18 minutes, with the last few minutes being done in 1 or 2 minute increments. It is critical that this etch be completed so careful inspection with an SEM is required. A 20 minute O_2 ash with 450 SCCM O_2 at 50 mT with 900 W ICP power cleans up polymer residue from the etch. The remaining resist is removed in 20 minutes of 80˚C 1165, with a second bath for an hour. This may still leave small strings of polymer on the chip. If needed, these strings can be removed with another 10 minute O_2 ash. If that has not removed them then a very gentle swabbing in IPA can remove them mechanically.

P-metal

The p-metal lithography uses SF-15 as an under layer and 1.8 μm resist for the exposure, both spun using recipe 5. Immediately after development and descum the chip should be placed in the e-beam chamber for metal deposition. The stack is Pd/Ti/Pd/Au 3/17/27/1500 nm. Liftoff is done in 80˚C 1165 for 75 minutes with a separate bath for 5 minutes. P- and n-metal contacts are then annealed at 350˚C for 30 seconds in a rapid thermal anneal with N_2 flowing.

Implant

A proton implant is used to confine the current in the mesa. Lithography uses SF-15 and 1.8 μm resist spun at recipe 5. The resist masks the chip except for the mesas, and the p-metal masks a 4 μm strip on the mesa to provide a current channel. The implant is done by an external vendor at a 7˚ angle from vertical. The dose and energy values are shown in Table 12.

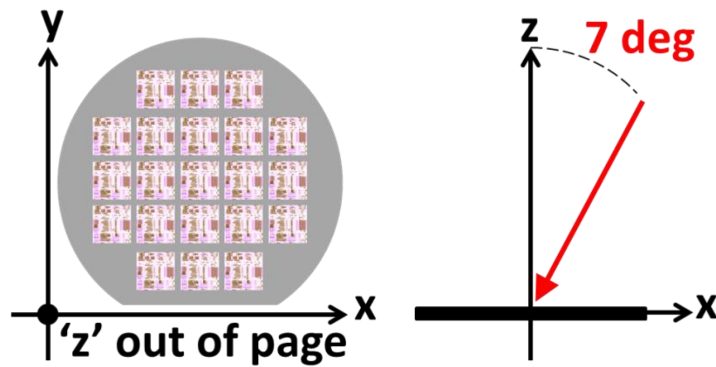


Figure 109. Illustration of implant angle.

Step	Energy (keV)	Dose (cm^{-2})
1	10	5e13
2	35	8e13
3	70	9e13
4	110	1e14
5	150	8e13
6	170	8e13
7	195	8e13

Table 12. Proton **i**mplant energies and dose.

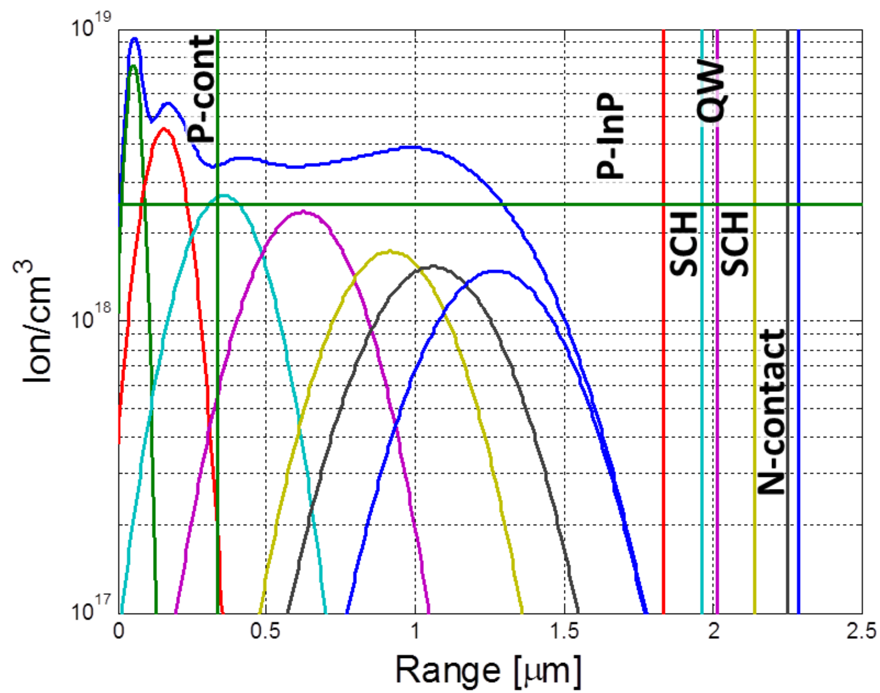


Figure 110. Calculation of implant profile for each dose. The combined ion density is shown in blue.

Isolation etch

Certain mask designs require an isolation section which separates two sections of the p-contact. For example, the tapers on the modulators are very narrow and would potentially cause a large amount of sidewall recombination. The modulator epi does not exhibit much loss when unpumped so it is desirable to separate the taper electrically. The lithography uses 1.8 μm resist spun with recipe 4. The regions are often narrow so extra care needs to be taken to ensure it develops fully. Also the O_2 descum is 2 minutes long. The p-sacrificial layer is still intact in these regions and is etched off with 1 minute of $HCl:H_2O$ 1:2. Then the p-contact layer is removed with 2 minutes of $H_3PO_4:H_2O_2:H_2O$ 1:5:15. Measurements with a laser microscope are taken before and after the etch to measure the height difference and ensure the etch is complete.

Heater

Metal strips are placed on the SiO_2 cladding over the waveguides to provide thermal index tuning. The bilayer resists are SF-11 and 1.8 μm resist spun with recipe 5. The metal stack is Ti/Pt 10/100 nm. Liftoff takes place in 80˚C 1165 for 45 minutes with an additional 10 minutes in a separate bath. In retrospect, the heater step might be better to do after the BCB is finished, and the adhesion nitride has been etched in the appropriate places. The nitride etch may have negative results on heater performance.

BCB

Processes that require high speed devices need a layer of non-conductive, high dielectric constant material. For this process photo-BCB 4024-40 was used. Low adhesion can be a problem when applying BCB, so several steps were taken to improve it. First, a 180 nm layer of SiN is deposited to promote good adhesion. Then a 20 second O_2 plasma at 300 mT

and 100W is performed. Next the chip is dipped in HCl:H_2O 1:10 for 60 seconds. Finally AP3000 BCB adhesion promoter is spun on using recipe 5. The BCB is spun on with a ramped acceleration using recipe 1. A 90 second 80˚C softbake is performed and the BCB is exposed. The post-exposure bake is 55˚C for 30 seconds after which the BCB should be immediately developed.

The BCB is developed using DS1000 BCB developer. The chip is placed on a spinner and the developer is puddled on for 60 seconds. Then recipe 2 is used to rinse and dry the wafer. While at 500 rpm the developer DS1000 is applied in the center of the chip drop by drop. This is the rinsing step. Next the chip is allowed to dry at the increased 4000 rpm. These development steps are repeated one or two more times as needed. Then the chip is baked at 90˚C for 60 seconds to further dry out the DS2100. The BCB is measured in a Dektak to ensure the development is completed.

The BCB is baked in a nitrogen-filled oven using ramped cycles. The oven is ramped over 5 minutes to 50˚C, and then allowed to soak for 5 minutes. Next it ramps for 15 minutes and reaches 100˚C, and then soaks for 15 minutes. Then 150˚C with 15 minute ramp and soak times. Then 250˚C with 60 minute ramp and soak times. Finally the oven is allowed to cool over the several hours. The height is measured by Dektak again.

The development of BCB still leaves a scum layer as thick as 1 µm. To remove the scum layer a blanket etch is performed using O_2/CF_4 200/50 SCCM at 40 Pa. with 1000 W ICP power for 1 minute. Another Dektak measurement is performed to find the final thickness. Desired thickness for this layer is 3 µm. Next, another 180 nm SiN adhesion layer is added. It should be noted that 1165 should no longer be used to remove resist as it reacts with the BCB and causes it to swell. Long exposure to other solvents should also be minimized.

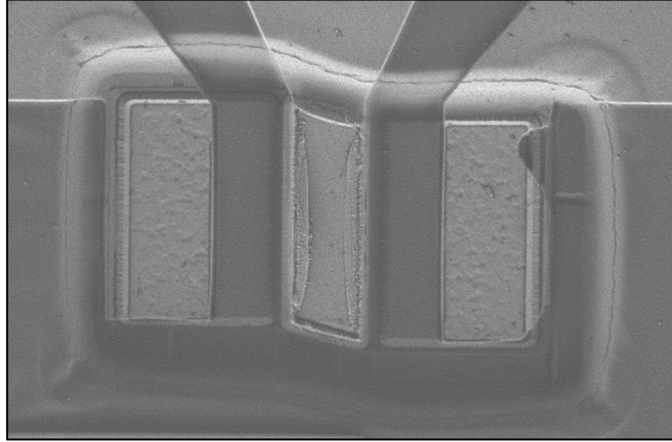


Figure 111. SEM image of developed BCB. The side wall lies at about 45˚ and allows the probe metal to transition smoothly between the BCB and open areas.

Nitride etch

The nitride adhesion layer needs to be removed over the heaters and vias so the probe metal can contact them. The lithography uses 3 μm resist spun with recipe 3. Both the Via and Heater masks are exposed. The nitride is etched with 40 SCCM CHF_3 at 0.5 Pa. with 900 W forward power for about 2 minutes. A 20 minute O_2 ash with 450 SCCM O_2 at 50 mT with 900 W ICP power is performed to remove the polymer buildup on the resist, and the resist is stripped in acetone for 60 minutes and additional baths as needed. An additional 10 minutes of O_2 ash can be performed if polymer remains.

Probe metal

The probe metal layer requires a bilayer process. SF-15 and 1.8 μm resist are spun with recipe 5. After exposure and development, a 1 minute O_2 descum is performed, and the chip is placed in the e-beam deposition chamber. The metal stack is Ti/Au 23/1500 nm. Liftoff is in acetone and takes 45 minutes with an additional 10 minute bath. Acetone will only remove the upper layer of resist, so 5 minutes of AZ726MIF developer is used to remove it. The chip is ready for dicing, polishing, and testing.

C.5 Summary

Semiconductor processing is becoming increasingly complicated and challenging. This process required bonding three different epis and twenty lithography steps. All of this was done with a human operator which greatly increases the likelihood of accident and catastrophic failure, and makes it difficult to produce repeatable devices. However, it also allows for continual improvements in the process to be made. Under these circumstances we have fabricated multiple highly complex photonic integrated circuits, as described in earlier chapters.

There are some parts of this process that can and should be improved. For example, the heater metal deposition should be postponed until after the adhesion nitride for the BCB is deposited and etched. This prevents the heaters from being attacked during the etch which should make them more reliable.

A change to the vertical channel mask would also benefit the process. In this instance the vertical channels were a series of thin channels that ran the length of the chip in X and Y, except where it would intersect a waveguide. This allowed acids and other liquids to run under the bonded epi where it was more difficult for the H_2O rinse to remove them. However, this design is good for bond yield. To improve it there should be a small gap in the vertical channel periodically to prevent liquids from flowing.

Improving the process is a continual challenge. Each change brings about unexpected consequences, often requiring multiple corrective steps.

Appendix D – Process Followers

Beam-steering: Phase I

INDEX	STEP	Time
1	**Waveguide**	
1-a	**SiO2 HARD MASK DEPOSITION**	
	ACE/ISO/N2 Clean U/S	
	Piranha H2SO4:H2O2=4:1	10 min
	BHF Dip	30 sec
	DI Rinse	
	PECVD Oxide deposition	
	Chamber clean (w/o sample)	30 min
	Deposit SiO2 (Recipe JonP_VarSIO) (Target 280 nm)	~7.5 min
	Measure Oxide on dummy si	
	DI Rinse	30 sec
2	**Rib etch patterning**	
2-a	**PR**	
	ACE/ISO/N2 Clean	
	Dehydration Bake 150 C	5 min
	Spin HMDS 3K	30 sec
	SPR955-0.9 (positive) - 3k rpm	30 sec
	Bake 95 C	90 sec
	Si mask - autostepper - 0 Focus	.72 sec
	Post-Exposure-Bake 110C	90 sec
	Developer MIF 726	90 sec
	O2 descum 300 mT/100W	30 sec
2-b	**ICP hard mask etch**	
	Switch to CHF3 if necessary	
	#100 O2+CHF3 clean and coat **(w/o sample)**	5min,3min
	#101 SiO2vert etch (CHF3): 40 sccm, 0.5 Pa, 900W ICP, 200W bias, ~220nm/min	90 sec
	#103 O2 clean	5 min
2-c	**Strip PR**	
	Strip PR in 80C PRX127	10-20 min
	(U/S 5 Freq, 5 sweep, high toggle)	
	Rinse in ISO	
	swap sample in ISO if necessary	
	ACE/ISO/N2 Clean U/S	
	Piranha H2SO4:H2O2=4:1	10 min
	Dektak	
2-d	**ICP Si Etch (Waveguide etch)**	
	#107 O2, CF4/CL2 clean and coat **(w/o sample)**	5min,3min
	#127 Si etch BCl3 20 sccm, CL2 40 sccm, 2.5 Pa, 500W ICP, 120W bias, ~4nm/s	1 min
	# 106 CF4/O2 clean	5 min
	Dektak	
2-e	**Strip PR**	
	ACE/ISO/N2 Clean U/S	
	Piranha H2SO4:H2O2=4:1	10 min
	Do Not Strip Oxide-Needed for Ebeam Via Protection	
3	**Ebeam Isolation Via Etch**	
3-a	**PR**	
	ACE/ISO/N2 Clean	
	Dehydration bake 110 C	1 min
	Spin HMDS 3K	30 sec
	SPR955-1.8 (positive) 3K	30 sec

	Bake 95 C	90 sec
	Isolation Mask(EBeam Via) (autostepper) Focus 0	0.4 sec
	Post-Exposure-Bake 110C	90 sec
	Developer MIF 726	60 sec
	O2 descum 300 mT/100W	30 sec
3-b	**Si Etch**	
	#107 O2, CF4/CL2 clean and coat **(w/o sample)**	5 min,3 min
	#127 Si etch BCl3 20 sccm, CL2 40 sccm, 2.5 Pa, 500W ICP, 120W bias, ~4nm/s	75 sec
	# 106 CF4/O2 clean	5 min
4	**ICP hard mask etch -BOx etch**	
	Switch to CHF3 if necessary	
	#100 O2+CHF3 clean and coat **(w/o sample)**	5 min,3 min
	#101 SiO2vert etch (CHF3): 40 sccm, 0.5 Pa, 900W ICP, 200W bias, ~220nm/min	5 min
	#103 O2 clean	5 min
4-a	**Strip PR**	
	Strip PR in 80C PRX127 (U/S 5 Freq, 5 sweep, high toggle)	10-20 min
	Rinse in ISO	
	swap sample in ISO if necessary	
	ACE/ISO/N2 Clean U/S	
	Piranha H2SO4:H2O2=4:1	10 min
	Dektak	
5	Give to Jock for EBEAM Write of gratings	
6	**SU-8 support layer (negative resist)**	
6-a	**Clean**	
	ACE/ISO/N2 Clean U/S	
	Piranha H2SO4:H2O2=4:1	10 min
	BHF Dip	60 sec
6-b	**SU-8 Litho**	
	Dehydration bake 200C	5 min
	Spin-coat SU-8 2002: ramp 100rpm/s to 500rpm	10 sec
	ramp 500 rpm/sec to 3000 rpm	30 sec
	Soft bake 95C	3 min
	Su8 Mask, Focus -12	0.4 sec
	Post exposure bake 65 C	1 min
	95 C	2 min
	Developer 60sec dip and shake + 15sec pipet flush	
	ISO/DI rinse and N2 dry	-
	inspect if vernier tip is open, if not, continue to develop	
	30sec dip and shake + 10sec pipet flush (option)	
	(until vernier tip shows up)	
	ISO/DI rinse and N2 dry	
	Dektak	
6-c	**Hard bake**	
	hot plate start 95 C	
	ramp up to 150C and stay 5min	
	ramp up to 205C and stay 5min	
	ramp up to 260C and stay 30min	
	ramp down to 205C and stay 5min	
	ramp down to 150C and stay 5min	
	ramp down to 95C and remove from hot plate	
	* color will become dark red when hard bake in air	
	Dektak	
7	**NiCr depostion**	
7-a	**Litho**	
	ACE/ISO/N2 Clean	
	Dehydration bake 110 C	1 min

	Spin SF-11 - 4K rpm	30 sec
	Bake 200C	2 min
	Use blue tape, lots of SF-11, and very fast ramp rate ~ 6000rpm/s	
	Use larger chuck	
	Spin AZnLoF 2020 (negative) - 3000K rpm	30 sec
	Bake 110C	1 min
	NiCr mask - autostepper Focus -6	0.55 sec
	Post-Exposure-Bake 110C	1 min
	Developer : AZ-300 MIF (5" after color changing stop)	55 sec
	1st Deep UV exposure (1000W)	300 sec
	Developer : XA101	70 sec
	2nd Deep UV exposure (1000W)	300 sec
	Developer : XA101	60 sec
	O2 descum 300 mT/100W	30 sec
7-b	**NiCr depostion**	
	Dehydration bake 110C	1 min
	Native oxide removal - Buffered HF dip	30 sec
	H20 dip	1 min
	Ebeam1 - Ni/Cr x4 = 125/60 x3 + 125/40, total 720A	
	deposition rate	Ni : 1A/s
		Cr : 0.5A/s
	Lift off in 1165 80C. Rinse in ISO	
	O2 descum 300 mT/100W	1 min
7-c	**Anneal**	
	RTA anneal 360 C	30 sec
8	**P PROBE METAL DEPOSITION**	
8-a	**Litho**	
	ACE/ISO/N2 clean	
	Dehydration 110 C	1 min
	Spin SF-11 - 4K rpm	30 sec
	Bake 200C	1 min
	Use blue tape, lots of SF-11, and very fast ramp rate ~ 6000rpm/s	
	Use larger chuck	
	Spin SF-11 - 4K rpm	30 sec
	Bake 200C	1 min
	Spin SF-11 - 4K rpm	30 sec
	Bake 200C	2 min
	AZ nLOF 2020 (negative) - Spin 3K rpm	30 sec
	Bake 110C	1 min
	Align 'probe' pattern (autostepper) Focus -12	0.55 sec
	Post-Exposure-Bake 110C	1 min
	Developer : AZ-300 MIF	55 sec
	1st Deep UV exposure (1000W)	300 sec
	Developer : XA101	70 sec
	2nd Deep UV exposure (1000W)	300 sec
	Developer : XA101	70 sec
	3rd Deep UV exposure (1000W)	300 sec
	Developer : XA101	70 sec
	Repeat Expose/Dev as needed up to 7X	
	O2 descum 300 mT/100W	1 min
8-b	**P PROBE DEPOSITION**	
	Dehydration bake 110C	1 min
	Load into e-beam 1or 4 (rotate) and deposit Ti;Au (200A;1um)	
	Lift off in 1165 80C. Rinse in ISO. O2 descum in necessary to remove resist residue	
	O2 descum 300 mT/100W	1 min

Beam-steering: Phase 2 / Tunable laser

INDEX	STEP
1	**Sample parameters.**
1.1.	Silicon
1.1.1.	SiO2 Hard mask thickness:
1.1.2.	Top Silicon height:
1.2.	III-V Epi wafer:
1.2.1.	Epi design and growth ID:
2	**Dice and cleave samples**
2.1.	Silicon:
2.1.1.	16 mm x 16 mm die, 2 per chip works, ideal is 24 mm x 46 mm total size.
2.2.	III-V
2.2.1.	Sample: 8.5 mm x 16 mm, opening: 8 mm x 17 mm à leave 50 um gap a top and bottom. Cleave such that short dimension is along minor flat. Mountains will appear along minor flat direction and break off.
3	**WG etch**
3.1.	Sample prep
3.1.1.	Acetone with ultrasonic 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min
3.1.2.	Dry with N2, dehydration bake 3 min 100 C
3.1.3.	Piranha Clean - H_2SO_4:H_2O_2 (3:1) 10 min or until Bubbling on sample stops.
3.1.4.	BHF dip 60 sec, Di Rinse
3.1.5.	Dehydration bake 3 mins 100 C
3.2.	PECVD hard mask deposition
3.2.1.	SiO2 clean, 30 min
3.2.2.	SiO2 deposition, 2750 A (clean, check oxide thickness on dummy with Filmetrics)
3.3.	WG litho (WG mask)
3.3.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
3.3.2.	Dehydration / HMDS
3.3.2.1.	bake 150 C, 5 mins
3.3.2.2.	spin HMDS 3K, 30 sec
3.3.3.	Spin PR
3.3.3.1.	Blow sample with N2
3.3.3.2.	Dispense PR: SPR955CM0.9
3.3.3.3.	Spin @ 3k for 30 s (recipe 5)
3.3.3.4.	Soft bake: 95C, 90 sec
3.3.4.	Autostep 200: “WG2” mask, time: 0.5–1 sec as req’d, focus offset: 0 or as req’d
3.3.5.	Post exposure bake 110 C, 90 sec
3.3.6.	Develop pattern ~90 s MIF 726
3.3.7.	N2 dry, dehydration bake 110 C, 30 sec
3.3.8.	O2 descum 300 mT/100W 30 sec
3.3.9.	Inspect under microscope:
3.3.9.1.	rib clusters top left at -5950,5500. Check rib width>850nm.
3.3.9.2.	gaps in MMI’s for 7 SWEEPER devices (top priority)
3.3.9.3.	gaps in Vernier lasers (couplers in rings) (lower priority)
3.3.9.4.	narrow waveguides in V lasers – check that they are present (lowest priority)
3.4.	SiO2 Hard mask etch
3.4.1.	Panasonic ICP2 (switch to CHF3 if necessary)
3.4.1.1.	Recipe 100: O2 clean, CHF3 coat (5 min/3 min) without sample
3.4.1.2.	Recipe 101: SiO2Vert etch (2200 A/min) with sample: Etch time: 90 sec (20% over etch)
3.4.1.3.	Recipe 103: O2 clean (5 min)
3.4.2.	Remove PR
3.4.2.1.	PR ash in PE2 O2 300 mT, 100 W, 120 s
3.4.2.2.	PRX127 soak 1: 10 min @ 70 C with sonication
3.4.2.3.	PRX127 soak 2: 10 min @ 70 C with sonication
3.4.2.4.	DI rinse for 5 min
3.4.2.5.	Pirhana 10 mins or until bubbling stops. DI rinse.

3.5.	Si WG etch
3.5.1.	Panasonic ICP 2, check recipe
3.5.1.1.	Recipe 107: (5min, 1 min)
3.5.1.2.	Recipe 127: Si etch. Etch time: ~1:00
3.5.1.3.	Recipe 106: CF4/O2 clean (10 min)
3.6.	Dektak step height
3.6.1.	Step height:
4.	**BOX Etch**
4.1.	Sample prep
4.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
4.2.	BOX Etch litho (BOX_ET mask)
4.2.1.	Dehydration / HMDS
4.2.1.1.	bake 150 C, 5 mins
4.2.1.2.	spin HMDS 3K, 30 sec
4.2.2.	Spin PR
4.2.2.1.	N2 blow
4.2.2.2.	Dispense PR: SPR955-1.8, Spin 3krpm for 30 s (recipe 5)
4.2.2.3.	Soft bake: 95C, 90 sec
4.2.3.	Autostep 200: "BOX_ET" mask, time: ~1.0 sec or as req'd, focus offset: 0 or as req'd
4.2.4.	Post exposure bake 110 C, 90 sec
4.2.5.	Develop pattern ~120 s MIF 726
4.2.6.	N2 dry, dehydration bake 110 C, 30 sec
4.2.7.	O2 descum 300 mT/100W 30 sec
4.2.8.	Inspect under microscope: open holes, no residue
4.3.	Si etch to BOX, Panasonic ICP2
4.3.1.	Recipe 107: (5min, 1 min)
4.3.2.	Recipe 127: Si etch, etch to BOX, Etch time: ~1 min 15 sec, overetch 10%
4.3.3.	Recipe 106: CF4/O2 clean (10 min)
4.4.	Remove PR
4.4.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
4.4.2.	PRX127 soak 1: 10-20 min, 80 C with U/S freq 5, 5 sweep, high toggle
4.4.3.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
4.5.	Remove Oxide hard mask
4.5.1.	BHF 5 mins
4.5.2.	DI 5 mins, N2 dry, dehydration bake 110C 5 mins.
5.	**Vertical Channels**
5.1.	PECVD hard mask deposition
5.1.1.	SiO2 clean, 30 min
5.1.2.	SiO2 deposition, 4000 A (clean, check oxide thickness on dummy with Filmetrics)
5.2.	Vertical Channel litho (VC mask)
5.2.1.	Dehydration / HMDS
5.2.1.1.	bake 150 C, 5 mins
5.2.1.2.	spin HMDS 3K, 30 sec
5.2.2.	Spin PR
5.2.2.1.	N2 blow
5.2.2.2.	Dispense PR: SPR955-1.8, Spin 3krpm for 30 s (recipe 5)
5.2.2.3.	Soft bake: 95C, 90 sec
5.2.3.	Autostep 200: "VC" mask, time: ~0.4 sec as req'd, focus offset: 0 or as req'd
5.2.4.	Post exposure bake 110 C, 90 sec
5.2.5.	Develop pattern ~120 s MIF 726
5.2.6.	N2 dry, dehydration bake 110 C, 30 sec
5.2.7.	O2 descum 300 mT/100W 30 sec
5.2.8.	Inspect under microscope: open holes, no residue
5.3.	SiO2 Hard mask etch, Panasonic ICP2
5.3.1.	Recipe 100: O2 clean, CF3 coat (5 min/3 min) without sample
5.3.2.	Recipe 101: SiO2Vert etch (2200 A/min). Etch time: 2.5 min (CHF3 40 sccm, RF Pwr SRC-900W, Bias-200W) with sample

5.3.3.	Recipe 103: O2 clean (5 min)
5.4.	Si etch to BOX, Panasonic ICP2
5.4.1.	Recipe 107: (5min, 1 min)
5.4.2.	Recipe 127: Si etch, etch to BOX, Etch time: ~2.5 min 15 sec, overetch 10%
5.4.3.	Recipe 106: CF4/O2 clean (10 min)
5.5.	Remove PR
5.5.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
5.5.2.	PRX127 soak 1: 10-20 min, 80 C with U/S freq 5, 5 sweep, high toggle
5.6.	Remove oxide hard mask
5.6.1.	BHF 2 mins
5.6.2.	DI 5 mins, N2 dry, dehydration bake 110 C 5 mins
6.	**N-doping**
6.1.	Sample prep
6.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
6.1.2.	Pirhana 10 mins or until bubbling stops
6.1.3.	BHF dip 60 sec, DI rinse
6.1.4.	Dehydration bake 150 C, 5 mins
6.2.	PECVD oxide deposition
6.2.1.	Deposit 50 nm SiO2
6.2.1.1.	Solvent clean dummy sample
6.2.1.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)
6.2.1.3.	Oxide thickness:
6.3.	N-doping litho (NDOPE mask)
6.3.1.	N2 blow (No O2 plasma, may cause problems with coating over the thermal shunt patterns)
6.3.2.	SPR 955 1.8
6.3.2.1.	HMDS 3000 rpm 30 sec
6.3.2.2.	Coating: 3000 rpm *30 sec
6.3.3.	Soft bake 95 C, 1.5 mins
6.3.4.	Autostep 200: “NDOPE” mask, time: 1.0 sec or as req’d, focus offset: 0 or as req’d
6.3.5.	Post-exposure bake 110C, 1.5 min
6.3.6.	Develop 2 min in MF726
6.3.7.	DI rinse, N2 dry
6.3.8.	Inspect if Vernier tip is open
6.3.9.	O2 Plasma 30 sec 100 W
	*** SEND OUT FOR IMPLANT *** (JKD)
6.4.	N-doping strip
6.4.1.	1165 Soak resist hard to remove. Use 1165 with U/S, possibly Gasonics instead.
6.4.2.	If necessary use a BHF dip (60 sec) to remove the underlying oxide, but ideally leave this on for the P-doping step. It is not a big deal if the resist does not get completely stripped as long as the P-doping windows are clear.
7.	**P-doping**
7.1.	Sample prep
7.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
7.1.2.	Pirhana 10 mins
7.1.3.	BHF dip 60 sec, DI rinse
7.1.4.	Dehydration bake 150 C, 5 mins
7.2.	PECVD oxide deposition (skip this if the NDOPE oxide is still intact)
7.2.1.	Deposit 50 nm SiO2
7.2.1.1.	Solvent clean dummy sample
7.2.1.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)
7.2.1.3.	Oxide thickness:
7.3.	P-doping litho (PDOPE mask)
7.3.1.	N2 blow (No O2 plasma, may cause problems with coating over thermal shunt patterns)
7.3.2.	Spin SPR 955 1.8
7.3.2.1.	HMDS 3000 rpm 30 sec
7.3.2.2.	Coating: 3000 rpm *30 sec
7.3.3.	Soft bake 95 C, 1.5 mins

7.3.4.	Autostep 200: "NDOPE" mask, time: 1.0 sec or as req'd, focus offset: 0 or as req'd
7.3.5.	Post-exposure baks 110 C, 1.5 mins
7.3.6.	Develop 2 mins in MF726
7.3.7.	DI rinse, N2 dry
7.3.8.	Inspect if Vernier tip is open
7.3.9.	O2 Plasma 30 sec 100 W
	*** SEND OUT FOR IMPLANT *** (JKD)
7.4.	p-doping strip
7.4.1.	1165 Soak Resist hard to remove. Use 1165 with U/S. Possibly Gasonics instead.
7.4.2.	Piranha 10 mins ß *** make sure all resist is gone ***
7.4.3.	BHF dip 60 sec, longer if necessary to remove resist fragments, but no longer than absolutely necessary given the problems we've been seeing with surface damage.
7.4.4.	Once sample is clean (inspect under microscope), follow immediately with anneal
8.	**Activation Anneal**
8.1.	Anneal
8.1.1.	RTA 1050 C in flowing N2, 10 mins, 30 sec ramp up/down
8.2.	AFM inspect
8.2.1.	Measure roughness in bonding half outside trench areas
9.	**Grating Definition**
9.1.	Pre-clean: Remove native oxide and/or dielectric hardmask
9.1.1.	HF dip
9.1.2.	Ebeam PR spin coat (2:1 ZEP)
9.1.3.	ACE,ISO,DI
9.1.4.	PEII - O2 Descum (100W, 300mTorr, 60sec)
9.1.5.	Dehydration Bake (150C, 5min)
9.1.6.	N2 Gun (1min) Cools and cleans wafer
9.2.	Spin 2:1 ZEP-520A:Anisol("A Thinner") (3000rpm, 30sec) - Recipe 5 ~225nm, Use a filtered syringe
9.2.1.	Pre-Exposure Bake (180C, 4min) Cover hotplate top to prevent additional particulate
9.3.	Thermal Au Evaporation
9.3.1.	Evaporate 11nm Au
9.4.	ALTERNATE to Au: Conductive Polymer (This is recommended if you have Si electrical processing or regrowth after this module)
9.4.1.	Spin on Conductive Polymer (Aquasave) (3000rpm, 30sec)
9.4.2.	Pre-Exposure Bake (90C, 1min) Cover hotplate top to prevent additional particulate
9.5.	Ebeam Writing Conditions
9.5.1.	Shallow Grating write file
9.5.2.	4th Lens
9.5.3.	Dose 350uC/cm2 (Please be aware this is pitch dependent, but has shown good results over a range of pitches if the substrate is not highly doped)
9.5.4.	Development
9.5.5.	(If thermal Au is used) Remove Au in wet Au etchant 10s
9.5.6.	DI Rinse 1min (required to rinse Au etchant AND remove conductive polymer)
9.5.7.	N2 Dry (be gentle on the gratings)
9.5.8.	1:1 MIBK:ISO Development - 60s Use a fresh batch
9.5.9.	9:1 MIBK:ISO Rinse - 15s DO NOT RINSE WITH DI
9.5.10.	N2 Dry DO NOT RINSE WITH DI
9.6.	Grating Etch
9.6.1.	AFM etch depth calibration recommended
9.6.2.	30min chamber clean in manual mode with cleaning wafer - 30mT, O2/Ar flow-rate=20/10sccm, bias/ICP powers=0/825W (especially after a prior users long Bosch etch)
9.6.3.	Single Step Bosch Etch Process - BOV_J_01 (19mT, 18/850W, C4F8/Ar/Ar flow-rate=56/24/20sccm)
9.6.4.	Rough Rates:
9.6.4.1.	~170nm/min w/o Sanovac 5
9.6.4.2.	~141nm/min w/ Sanovac 5
9.7.	Strip ZEP (2:1)
9.7.1.	1165 Soak at 80C - 10min

9.7.2.	PEII - O2 Descum (100W, 300mTorr, 60-120sec)
9.8.	Pre-clean: Remove native oxide and/or dielectric hardmask
9.8.1.	HF dip
9.9.	Ebeam PR spin coat (%100 ZEP)
9.9.1.	ACE,ISO,DI
9.9.2.	PEII - O2 Descum (100W, 300mTorr, 60sec)
9.9.3.	Dehydration Bake (150C, 5min)
9.9.4.	N2 Gun (1min) Cools and cleans wafer
9.9.5.	Spin 100% ZEP-520A (2000rpm, 30sec) - Recipe 5 ~225nm, Use a filtered syringe
9.9.6.	Pre-Exposure Bake (180C, 4min) Cover hotplate top to prevent additional particulate
9.10.	Thermal Au Evaporation
9.10.1.	Evaporate 11nm Au
9.10.2.	ALTERNATE to Au: Conductive Polymer (This is recommended if you have Si electrical processing or regrowth after this module)
9.10.3.	Spin on Conductive Polymer (Aquasave) (3000rpm, 30sec)
9.10.4.	Pre-Exposure Bake (90C, 1min) Cover hotplate top to prevent additional particulate
9.11.	Ebeam Writing Conditions
9.11.1.	Deep Grating (DBR) write file
9.11.2.	4th Lens
9.11.3.	Dose 500uC/cm2 (Please be aware this is pitch dependent, but has shown good results over a range of pitches if the substrate is not highly doped)
9.12.	Development
9.12.1.	(If thermal Au is used) Remove Au in wet Au etchant 10s
9.12.2.	DI Rinse 1min (required to rinse Au etchant AND remove conductive polymer)
9.12.3.	N2 Dry (be gentle on the gratings)
9.12.4.	1:1 MIBK:ISO Development - 60s Use a fresh batch
9.12.5.	9:1 MIBK:ISO Rinse - 15s DO NOT RINSE WITH DI
9.12.6.	N2 Dry DO NOT RINSE WITH DI
9.13.	Grating Etch
9.13.1.	AFM etch depth calibration recommended
9.13.2.	30min chamber clean in manual mode with cleaning wafer - 30mT, O2/Ar flow-rate=20/10sccm, bias/ICP powers=0/825W (especially after a prior users long Bosch etch)
9.13.3.	Single Step Bosch Etch Process - BOV_J_01 (19mT, 18/850W, C4F8/Ar/Ar flow-rate=56/24/20sccm)
9.13.4.	Rough Rates:
9.13.4.1.	~170nm/min w/o Sanovac 5
9.13.4.2.	~141nm/min w/ Sanovac 5
9.14.	Strip ZEP (2:1)
9.14.1.	1165 Soak at 80C - 10min
9.14.2.	PEII - O2 Descum (100W, 300mTorr, 60-120sec)
10.	**Protection litho**
10.1.	Sample prep
10.1.1.	Acetone with ultrasonic 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min
10.1.2.	Dry with N2, dehydration bake 3 min 100 C
10.1.3.	Dehydration bake 3 mins 150 C
10.2.	PECVD oxide deposition
10.2.1.	SiO2 clean, 30 mins
10.2.2.	Deposit 700 nm SiO2 (350 nm + 350 nm)
10.2.2.1.	Solvent clean dummy sample
10.2.2.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)
10.2.2.3.	Oxide thickness:
10.3.	PECVD nitride deposition
10.3.1.	SiN clean, 30 min
10.3.2.	Deposit 700 nm SiN (350 nm + 350 nm) (actual and dummy)
10.3.2.1.	Solvent clean dummy sample
10.3.2.2.	Measure nitride thickness of dummy using Filmetrics (do not discard dummy)
10.3.2.3.	Nitride thickness:
10.4.	Litho (Prot1 mask)

10.4.1.	Sample prep
10.4.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
10.4.1.2.	Pirhana 5 mins / DI rinse
10.4.1.3.	PE2 O2 descum 300 mT, 100 W, 60 s
10.4.1.4.	Dehydration bake 150 C, 5 mins
10.4.2.	Spin HMDS
10.4.2.1.	Blow sample with N2
10.4.2.2.	Dispense HMDS
10.4.2.3.	Spin 30 s, 3 krpm (recipe 5)
10.4.3.	Spin PR
10.4.3.1.	Blow sample with N2
10.4.3.2.	Dispense PR: nLOF5510
10.4.3.3.	Spin 30 sec, 3krpm
10.4.3.4.	Pre exposure bake 60 sec, 90 C
10.4.4.	Autostep 200: 0.25 s, focus offset: -1
10.4.5.	Bake 60 sec, 110 C
10.4.6.	Develop 1 min in AZ726MIF, until color change stops + 20%
10.4.7.	DI rinse
10.4.8.	N2 dry
10.4.9.	Inspect pattern in microscope
10.4.10.	PE2 O2 descum 300 mT, 100 W, 30 s
10.4.11.	Hard bake PR: 10 min @ 120 C
10.5.	SiN and SiO2 dry etch (Panasonic ICP2)
10.5.1.	Check gasses (CHF3)
10.5.2.	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
10.5.3.	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
10.5.4.	Etch nitride (700 nm) and ~50% (350 nm) of oxide layer in ICP2: 3 min etch (Double check!)
10.5.5.	Recipe 103: O2 clean (5 min)
10.6.	SiO2 wet etch
10.6.1.	Etch remaining 50% (350 nm) in BHF, ~90 s. Etch in 30 s steps.
10.6.2.	Active silicon should be oxide/nitride protected; rest of sample should be hydrophobic. Inspect edge of protective cover. Undercut visible?
10.7.	Strip PR
10.7.1.	PRX127 @ 80 C, 10 min with sonication, repeat if PR remains
10.7.2.	Dektak step height:
11.	**Bonding**
11.1.	Sample prep (silicon)
11.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry) with particle swab in Isopropanol
11.1.2.	Microscope inspection. Repeat until sample is particle free. Use piranha/BHF if needed. Rinse thoroughly.
11.2.	Sample prep (III-V)
11.2.1.	Quick Acetone rinse
11.2.2.	Acetone bath, no sonication
11.2.3.	Isopropanol bath, no sonication
11.2.4.	Particle swab in Isopropanol
11.2.5.	DI rinse
11.2.6.	Microscope inspection. Repeat until sample is particle free. Use BHF if needed. No Piranha. Rinse thoroughly.
11.2.6.1.1	PE2 O2 descum 300 mT, 100 W, 1 min
11.3.	InGaAs Cap removal
11.3.1.	H_2O:H_2O_2:H_3PO_4 (38:1:1, 190:5:5 mL) 5 min - Surface color should change
11.3.2.	DI rinse
11.3.3.	Microscope inspection. Repeat until sample is particle free.
11.4.	Ozone organic clean (Si and III-V)
11.4.1.1.	20 min ozone treatment
11.5.	Surface activation
11.5.1.	EVG O2 plasma activation- Run Dis0.2mBar on all samples
11.5.2.	OH surface treatment

11.5.2.1.	NH_4OH vaporization
11.5.2.1.1	Set hotplate to 125 C
11.5.2.1.2	Place vaporization glassware on hotplate and let NH_4OH warm for two minutes. The cover glass should be covered in OH condensation after 2 minutes.
11.5.2.1.3	Place samples on small glass dish and place inside vaporization glassware for 5 minutes.
11.5.2.1.4	Cool samples in covered dish on bench for 4-5 minutes.
11.6.	Wafer bonding
11.6.1.	Conduct physical bond - Intel run III-V: 10.5 mm x 4.3 mm
11.6.1.1.	
11.6.1.2.	Anneal bonded pairs w/ external pressure > 3 Mpa (0.6 on torque wrench), 300 C, 45 mins
11.6.2.	Remove samples and let cool
11.7.	Substrate thinning (thin by ~ 230 um)
11.7.1.	Substrate removal
11.7.1.1.	Mount samples on glass slide with crystal bond wax
11.7.1.2.	Heat hotplate to 130 C
11.7.1.3.	Melt a small pool of wax onto the glass side slightly larger than the sample.
11.7.1.4.	Place the sample in the wax with the silicon side down.
11.7.1.5.	Let the wax flow such that it covers the sides of the III-V chip but not the top.
11.7.1.6.	1 sample per glass slide
11.7.1.7.	Place samples in substrate removal solution
11.7.1.8.	Etch in HCl : H_2O (3:1) for ~15min (until bubbling stops)
11.7.1.9.	Rinse samples well (5-10 min)
11.7.1.10.	Remove the samples from the glass slide
11.7.1.11.	Place the glass slide on the heated hot plate (130C)
11.7.1.12.	Use a wooden stick to push the sample into a aluminum dish
11.7.1.13.	Clean the sample with acetone in the aluminum dish until all the wax is gone. Change the acetone a few times
11.7.1.14.	Rinse in IPA
11.7.1.15.	Rinse in DI
11.7.1.16.	Dry with an N_2 gun
11.8.	Dehydration bake
11.8.1.	Start the samples on a 95 C hotplate for 2 minutes
11.8.2.	Move the samples to a 115 C hotplate for 2 more minutes
11.8.3.	Move the samples to a 150 C hotplate for 2 minutes
11.8.4.	Move the samples to a 200 C hotplate for 5 minutes
12.	**Gap fill**
12.1.	Sample prep
12.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
12.1.2.	Dehydration bake 3 min 120 C
12.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
12.2.	PECVD oxide deposition
12.2.1.	SiO2 clean, 30 mins
12.2.2.	Deposit 700 nm SiO2 (350 nm + 350 nm)
12.3.	PECVD nitride deposition
12.3.1.	SiN clean, 30 min
12.3.2.	Deposit 700 nm SiN (350 nm + 350 nm) (actual and dummy)
12.4.	Litho (GF mask)
12.4.1.	Sample prep
12.4.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
12.4.1.2.	Dehydration bake 3 min 120 C
12.4.1.3.	PE2 O2 descum 300mT, 100 W, 1 min
12.4.2.	Spin resist
12.4.2.1.	Blow sample with N2
12.4.2.2.	Dispense PR: SPR220-3
12.4.2.3.	Spin 30 sec, 2.5 krpm
12.4.3.	Pre exposure bake 90 s, 115 C
12.4.4.	Autostepper (settings?)

12.4.4.1.	Post exposure bake 90 sec, 110 C
12.4.5.	Develop
12.4.5.1.	60 s in AZ726MIF, develop until color change stops + 20%
12.4.5.2.	DI rinse
12.4.5.3.	Inspect. Make sure PR covers edge of III/V.
12.4.5.4.	Hard bake PR for 10 min @ 120C
12.5.	Remove SiN and SiO on top of III/V
12.5.1.	Panasonic ICP2
12.5.1.1.	Check gasses (CHF3)
12.5.1.2.	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
12.5.1.3.	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
12.5.1.4.	Etch nitride (700 nm) and ~50% (350 nm) of oxide layer in ICP2: 3 min etch
12.5.1.5.	Recipe 103: O2 clean (5 min)
12.5.2.	SiO2 wet etch
12.5.2.1.	Etch remaining 50% (350 nm) in BHF, ~90 s. Etch in 30 s steps.
12.5.2.2.	III-V should be exposed
12.5.3.	Remove PR
12.5.3.1.	PRX127 @ 80 C, 10 min, repeat if PR remains
13.	**Mesa Definition**
13.1.	Metal deposition (E-beam 3) (actual samples and one unpatterned Si or SOI dummy)
13.1.1.	Oxide removal, to be immediately followed by metal deposition
13.1.1.1.	20:1 DI:HF dip (5 s)
13.1.1.2.	DI rinse
13.1.1.3.	Pd/Ti/Pd/Au (30/170/170/1000)
13.1.1.4.	Set dummy sample aside for step 11.2.
13.2.	SiN deposition
13.2.1.	Dehydration bake 5 min @ 150 C
13.2.2.	Deposit 3000A of SiN
13.3.	Mesa litho (Mesa Def mask)
13.3.1.	Sample prep
13.3.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
13.3.1.2.	dehydration bake 3 min 120 C
13.3.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
13.3.2.	Spin resist
13.3.2.1.	Blow sample with N2
13.3.2.2.	Dispense HMDS, 30 sec, 3 krpm
13.3.2.3.	Blow sample with N2
13.3.2.4.	Dispense nLOF 5510, 30 sec, 3 krpm
13.3.2.5.	Soft bake 1 min, 90 C
13.3.3.	Expose in stepper 0.25 sec, offset: -1
13.3.4.	Post bake 1 min, 110 C
13.3.5.	Develop AZ300MIF, 1 min
13.3.6.	Inspect: If bent tapers -> try a longer descum in next step to etch some of PR.
13.3.7.	PE2 O2 descum 300 mT, 100 W, 1 min
13.4.	Mesa etch
13.4.1.	SiN etch in RIE3
13.4.1.1.	O2 chamber clean: O2, 20 sccm, 50 mT, 500 V, 30 min
13.4.1.2.	CF4 etch: CF4/O2, 20 sccm/1.8 sccm, 10 mT, 250 V, ~13 min
13.4.1.3.	PR burn: O2, 20 sccm, 10 MT, 250 V, 5 min
13.4.1.4.	? PR strip in 1165 @ 80 C (AZ300T?, check with Di if Pd is attacked.) ?
13.4.1.5.	ISO, DI, N2 blow dry
13.4.1.6.	PE2 O2 descum 300 mT, 100 W, 1 min
13.4.2.	Au etch
13.4.2.1.	20 s in gold etchant with mild agitation
13.4.2.2.	Thorough DI rinse
13.4.3.	Metal dry etch in ICP2, to be immediately followed by Mesa etch
13.4.3.1.	Recipe 107, CF4/O2 clean/coat: 5 min, 1 min

13.4.3.2.	Recipe 128, Ti etch: 1 min 20 sec
13.4.3.3.	Recipe 106, CF4/O2 clean: 5 min
13.4.4.	Mesa etch in RIE 2
13.4.4.1.	O2 chamber clean: 20 sccm, 125 mT, 500 V, 30 min
13.4.4.2.	MHA precoat: CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V, 20 min
13.4.4.3.	MHA etch: CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V, ~35 min, use laser monitor (Go 2.5 more periods after period change ? Check this with Geza or Di)
13.4.4.4.	O2 descum: O2, 20 sccm, 125 mT, 300V, 10 min
14.	**SCH etch**
14.1.	Lower SCH litho (QW mask)
14.1.1.	Sample prep
14.1.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
14.1.1.2.	Dehydration bake 3 min, 120 C
14.1.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
14.1.2.	Spin resist
14.1.2.1.	Blow sample with N2
14.1.2.2.	Dispense HMDS, 30 sec, 3 krpm
14.1.2.3.	Blow sample with N2
14.1.2.4.	Dispense SPR955CM-1.8
14.1.2.5.	Spin 30 sec, 3 krpm
14.1.2.6.	Soft bake 90 sec, 95 C
14.1.3.	Expose in stepper 0.35 sec, offset: 0
14.1.4.	Post bake for 90 sec, 110 C
14.1.5.	Develop AZ726MIF, 1 min
14.2.	Lower SCH etch
14.2.1.1.	H2O/H2O2/H3PO4, 15/5/1, until color change stops, etched area will be purple~5 – 10 sec
14.3.	Strip PR
14.3.1.	1165, 80 C
15.	**N Metal**
15.1.	N Metal litho (NMET mask)
15.1.1.	Sample prep
15.1.1.1.	Acetone 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min
15.1.1.2.	Dehydration bake 3 min, 120 C
15.1.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
15.1.2.	Spin resist
15.1.2.1.	Blow N2
15.1.2.2.	Dispense SF11, spin 30 sec, 4 krpm
15.1.2.3.	Bake 2 mins, 170 C, cool for 1 min, blow N2
15.1.2.4.	Dispense SF11, spin 30 sec, 4 krpm
15.1.2.5.	Bake 2 mins, 170 C, cool for 1 min, blow N2
15.1.2.6.	Dispense SPR955CM-1.8, spin 30 sec, 3 krpm
15.1.2.7.	Bake 90 sec, 95 C
15.1.3.	Expose in stepper 0.35 sec, offset: 0
15.1.4.	Post bake 90 sec, 110 C
15.1.5.	Develop AZ726MIF, 1 min
15.1.6.	UV exposure 300 sec
15.1.7.	SAL101A 70 sec
15.1.8.	UV exposure 300 sec
15.1.9.	SAL101A 70 sec
15.1.10.	Inspect pattern, verify undercut
15.2.	Remove SiN (from mesa hard mask)
15.2.1.	PE2 CF4 etch, 4 min
15.2.2.	PE2 O2 descum 300 mT, 100 W, 30 sec
15.3.	Metal deposition
15.3.1.	HCl:DI (1:10), 30 sec
15.3.2.	DI rinse (thorough)
15.3.3.	Ni/Ge/Au/Ni/Au (50/300/300/200/10000)

15.4.	Liftoff
15.4.1.	Acetone with flushing using pipette
15.4.2.	Rinse thoroughly
15.4.3.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
15.4.4.	Strip Annealer: 30 sec, 360 C
15.4.5.	TLM measurements (JKD)
16.	**Proton implant litho (HIMPL mask)**
16.1.	Sample prep
16.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
16.1.2.	Dehydration bake 3 min, 100 C
16.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
16.2.	Litho (3 layers SF11, 1 layer SPR955CM-1.8)
16.2.1.	Layer 1
16.2.1.1.	N2 blow
16.2.1.2.	Dispense SF11, spin 30 sec, 4 krpm
16.2.1.3.	Bake 2 min, 200 C, cool 1 min
16.2.2.	Layer 2
16.2.2.1.	N2 blow
16.2.2.2.	Dispense SF11, spin 30 sec, 4 krpm
16.2.2.3.	Bake 2 min, 200 C, cool 1 min
16.2.3.	Layer 3
16.2.3.1.	N2 blow
16.2.3.2.	Dispense SF11, spin 30 sec, 4 krpm
16.2.3.3.	Bake 2 min, 200 C, cool 1 min
16.2.4.	Layer 4
16.2.4.1.	N2 blow
16.2.4.2.	Dispense SPR955CM-1.8, spin 30 sec, 3 krpm
16.2.4.3.	Bake for 90 sec @ 95 C
16.2.5.	Autostepper expose HIMPL mask 0.35 s, offset 0
16.2.6.	Post bake 90 s, 110 C
16.2.7.	Develop AZ726MIF 1 min
16.2.8.	UV exposure: 300 sec; SAL101A: 70 sec
16.2.9.	UV exposure: 300 sec; SAL101A: 70 sec
16.2.10.	Inspect pattern
16.3.	Ion implant (JKD à Kroko)
16.4.	Channel isolation etch
16.4.1.	PE2 O2 descum, 300 mT, 100 W, 1 min
16.4.2.	Au etch
16.4.2.1.	20 s in gold etchant with mild agitation
16.4.2.2.	Thorough DI rinse
16.4.3.	BHF dip 20 s with mild agitation
16.4.4.	Thorough DI rinse
16.4.5.	Metal dry etch in ICP2, to be immediately followed by III-V etch
16.4.5.1.	Recipe 107, CF4/O2 clean/coat: 5 min, 1 min
16.4.5.2.	Recipe 128, Ti etch: 1 min 20 sec
16.4.5.3.	Recipe 106, CF4/O2 clean: 5 min
16.4.6.	III-V etch in RIE 2
16.4.6.1.	O2 chamber clean: 20 sccm, 125 mT, 500 V, 30 min
16.4.6.2.	MHA precoat: CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V, 20 min
16.4.6.3.	MHA etch: CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V, ~10 min, use laser monitor if possible – goal is to etch through 100 nm of InGaAs and a little bit into the InP
16.4.6.4.	O2 descum: O2, 20 sccm, 125 mT, 300V, 10 min
16.5.	Strip
16.5.1.	1165, 80 C
16.6.	Inspect (SEM)
17.	**N-layer etch (NETCH mask) - does not actually etch N-layer**
17.1.	Sample prep

17.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
17.1.2.	Dehydration bake 3 min, 100 C
17.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
17.2.	Spin resist
17.2.1.	N2 blow
17.2.2.	Dispense HMDS, spin 30 sec, 3 krpm
17.2.3.	N2 blow
17.2.4.	Dispense SPR955CM-1.8, spin 30 sec, 3 krpm
17.2.5.	Bake 90 sec, 95 C
17.3.	Litho
17.3.1.	Autostepper expose 0.35 s, offset 0
17.3.2.	Post-bake 90 sec, 110 C
17.3.3.	Develop AZ726MIF, 1 min
17.4.	wet SiN Etch
17.4.1.	O2 descum, 1 min
17.4.2.	Dilute HF:DI 20:1, approx. 6 mins or until clear
17.4.3.	O2 descum, 30 sec
17.5.	Strip resist
17.5.1.	1165, 80 C
17.5.2.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
17.5.3.	Dehydration bake 3 min, 100 C
17.5.4.	PE2 O2 descum 300 mT, 100 W, 1 min
18.	**Si Via (Si-VIA mask)**
18.1.	Sample prep
18.1.1.	Dehydration / HMDS
18.1.1.1.	bake 150 C, 5 mins
18.1.1.2.	spin HMDS 3K, 30 sec
18.2.	Litho
18.2.1.1.	N2 blow
18.2.1.2.	Dispense PR: SPR955-1.8, Spin 3krpm for 30 s (recipe 5)
18.2.1.3.	Soft bake: 95C, 90 sec
18.2.2.	Autostep 200: “SVia” mask, time: ~0.4 sec or as req’d, focus offset: 0 or as req’d
18.2.3.	Post exposure bake 110 C, 90 sec
18.2.4.	Develop pattern ~120 s MIF 726
18.2.5.	N2 dry, dehydration bake 110 C, 30 sec
18.2.6.	O2 descum 300 mT/100W 30 sec
18.2.7.	Inspect under microscope: open holes, no residue
18.3.	ALTERNATE LITHO (use whichever is preferred)
18.3.1.	N2 blow
18.3.2.	Dispense PR: SPR220-3, spin 2.5krpm 30 s
18.3.3.	Soft bake 115 C, 90 sec
18.3.4.	Autostep 200: “SVia” mask, time ~0.72 s or as req’d, focus offset: 0 or as req’d
18.3.5.	Post exposure bake 115 C, 90 s
18.3.6.	Develop pattern ~60 s in AZ726MIF, develop until color change stops + 20%
18.3.7.	DI rinse
18.3.8.	N2 dry, dehydration bake 110 C, 30 sec
18.3.9.	O2 descum 300 mT/100W 30 sec
18.3.10.	Inspect under microscope: open holes, no residue
18.4.	Buffer etch
18.4.1.	Dry etch 75% through
18.4.1.1.	Panasonic ICP2 - Check gasses (CHF3)
18.4.1.2.	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
18.4.1.3.	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
18.4.1.4.	Etch nitride (700 nm) and 110% (700 nm + 70 nm) of oxide layer in ICP2: estimated 6.5 min etch (Double check!)
18.4.1.5.	Recipe 103: O2 clean (5 min)
18.4.2.	SiO2 wet etch

18.4.2.1.	Etch any remaining SiO2 in BHF, ~60 s.
18.4.2.2.	Inspect edge of vias. Undercut visible?
18.5.	Remove PR
18.5.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
18.5.2.	PRX127 soak 1: 10-20 min, 80 C with U/S freq 5, 5 sweep, high toggle
19.	**Si contacts (N-METAL mask)**
19.1.	Sample prep
19.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
19.1.2.	Pirhana 5 mins / DI rinse
19.1.3.	Dehydration bake, 5 min @ 150 C
19.2.	Photoresist
19.2.1.	N2 blow
19.2.2.	Dispense LOL2000, spin 3krpm, 30 sec
19.2.3.	Pre-exposure bake 200C, 5 min
19.2.4.	N2 blow
19.2.5.	Dispense SPR955CM-1.8, spin 4Krpm, 30 sec
19.2.6.	Pre-exposure bake 90 C, 90 sec
19.3.	Litho
19.3.1.	Autostep 200: “N-METAL” mask, time: ~0.4 sec as req’d, focus offset: -1 or as req’d, SHUTTER LEFT (III-V) HALF IF POSSIBLE
19.3.2.	Post-exposure bake 110 C, 90 sec
19.3.3.	Develop MF726, 60 sec
19.3.4.	Inspection: microscope
19.3.4.1.	verify pattern is properly developed (look for double line indicating undercut)
19.3.5.	PE O2 descum 300 mT, 100 W, 30 sec
19.4.	Metal deposition (actual samples + dummy)
19.4.1.	20:1 DI:HF dip (5 s)
19.4.2.	DI rinse
19.4.3.	Ebeam 3 Ti/Pt/Au (170/170/1000) (must follow BHF dip/rinse immediately)
19.4.4.	Liftoff 1165, 80 C for ~2 hours.
19.4.5.	ISO, DI rinse 5 mins each with gentle agitation
19.5.	Inspection
19.5.1.	microscope check alignment Verniers, metal features over vias
20.	**Gapfill removal (GF mask)**
20.1.	Litho (GF mask)
20.1.1.	Sample prep
20.1.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
20.1.1.2.	dehydration bake 3 min 120 C
20.1.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
20.1.2.	Spin resist ß this neg resist process didn’t stand up to BHF. Need other resist.
20.1.2.1.	Blow sample with N2
20.1.2.2.	Dispense HMDS, 30 sec, 3 krpm
20.1.2.3.	Blow sample with N2
20.1.2.4.	Dispense nLOF 5510, 30 sec, 3 krpm
20.1.2.5.	Soft bake 1 min, 90 C
20.1.3.	Expose in stepper 0.25 sec, offset: -1
20.1.4.	Post bake 1 min, 110 C
20.1.5.	Develop AZ300MIF, 1 min
20.1.6.	Inspect: check that resist covers everything except “gap fill” region.
20.1.7.	PE2 O2 descum 300 mT, 100 W, 1 min
20.2.	Remove SiN and SiO on top of gapfill III/V
20.2.1.	Panasonic ICP2
20.2.1.1.	Check gasses (CHF3)
20.2.1.2.	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
20.2.1.3.	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
20.2.1.4.	Etch nitride (700 nm) and ~50% (350 nm) of oxide layer in ICP2: 3 min etch
20.2.1.5.	Recipe 103: O2 clean (5 min)

20.2.2.	SiO2 wet etch
20.2.2.1.	Etch remaining 50% (350 nm) in BHF, ~90 s. Etch in 30 s steps.
20.2.2.2.	Inspect: III-V should be exposed
20.3.	Wet Etch III-V in gapfill region
20.3.1.	200 nm InP:
20.3.2.	100 nm InGaAs:
20.3.3.	1500 nm InP:
20.3.4.	400 nm AlGaInAs:
20.3.5.	110 nm InP:
20.3.6.	Remaining III-V should contain only supperlattice and n-InP layers
20.4.	Remove PR
20.4.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
20.4.2.	PRX127 soak 1: 10-20 min, 80 C
21.	**Buffer (SU8) with VIA Litho (VIA mask)**
21.1.	Sample prep
21.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
21.1.2.	dehydration bake 3 min 120 C
21.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
21.2.	Nitride dep (for adhesion)
21.2.1.	Dehydration bake 5 min @ 150 C
21.2.2.	PECVD 20 nm of SiN
21.3.	SU8 spin
21.3.1.	Blow N2
21.3.2.	Dispense SU-8 2002
21.3.2.1.	Spread 500 rpm, 10 s (ramp 100 rpm/s)
21.3.2.2.	Coating: 3 krpm, 30 s (ramp 500 rpm/s)
21.3.3.	Soft bake: 95 C, 3 min
21.4.	Litho
21.4.1.	Autostepper: 0.4 s, focus -12 (?), VIA mask
21.4.2.	Post-exposure bake:
21.4.2.1.	65 C, 1 min
21.4.2.2.	95 C, 2 min
21.4.3.	Develop
21.4.3.1.	60 s dip and shake + 15 s pipet flush
21.4.3.2.	ISO/DI rinse and N2 dry
21.4.3.3.	Inspect if vernier tip is open; if not continue to develop
21.4.3.4.	30 s dip and shake + 10 s pipet flush (optional until vernier tip is open)
21.4.3.5.	ISO/DI rinse and N2 dry
21.4.4.	Inspect: check for via's open over contacts
21.5.	Hard bake
21.5.1.	95 C to start
21.5.2.	Ramp to 150 C, hold 5 min
21.5.3.	Ramp to 205 C, hold 5 min
21.5.4.	Ramp to 260 C, hold 30 min
21.5.5.	Ramp down 205 C, hold 5 min
21.5.6.	Ramp down 150 C, hold 5 min
21.5.7.	Ramp down 95 C, remove from hot plate
21.5.8.	Colour should be dark red
21.6.	Adhesion nitride
21.6.1.	PECVD SiN clean, 30 min
21.6.2.	PECVD 300 nm SiN
22.	**TO Metal Litho**
22.1.	Sample prep
22.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
22.1.2.	dehydration bake 3 min 120 C
22.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
22.2.	Spin/bake SF-11

22.2.1.	Dispense SF-11 4 krpm, 30 s (blue tape, larger chuck, lots of SF11, fast ramp ~6000 rpm/s)
22.2.2.	Bake: 200 C, 2 min
22.3.	Spin/bake AZnLoF 2020
22.3.1.	Dispense AZnLoF 2020
22.3.1.1.	Spin 3 krpm, 30 s
22.3.1.2.	Bake 110 C, 1 min
22.4.	Litho (TOMET mask)
22.4.1.	Autostepper 0.11 s, focus ~5
22.4.2.	Post-esposure bake 110 C, 1 min
22.4.3.	Develop AZ-300 MIF ~ 55 s (count 5 s after colour change)
22.4.4.	1st DUV expose: 1000 W, 300 s
22.4.5.	Develop XA101 70 s
22.4.6.	2nd DUV expose: 1000 W, 300 s
22.4.7.	Develop XA101 60 s
22.4.8.	O2 descum 300 mT, 100 W, 30 s
22.5.	Metal liftoff
22.5.1.	Ebeam 1 Ni/Cr (Ni: 1 A/s, Cr: 0.5 A/s)
22.5.1.1.	125 A Ni, 60 A Cr (3 times)
22.5.1.2.	125 A Ni, 40 A Cr (once)
22.5.1.3.	Ni/Cr x 4 = 125/60 x3 + 125/40, total 720 A
22.5.1.4.	Au 750 A
22.5.2.	Lift off 1165 80 C
22.5.3.	Thorough IPA rinse
22.5.4.	O2 descum 300 mT/100 W, 1 min
22.5.5.	RTA anneal 360 C, 30 s
23.	**Probe metal**
23.1.	Via re-Litho (clears nitride in the via's)
23.1.1.	Autostepper: 0.4 s, focus -12 (?), VIA mask
23.1.2.	Post-exposure bake:
23.1.2.1.	65 C, 1 min
23.1.2.2.	95 C, 2 min
23.1.3.	Develop
23.1.3.1.	60 s dip and shake + 15 s pipet flush
23.1.3.2.	ISO/DI rinse and N2 dry
23.1.3.3.	Inspect if vernier tip is open; if not continue to develop
23.1.3.4.	30 s dip and shake + 10 s pipet flush (optional until vernier tip is open)
23.1.3.5.	ISO/DI rinse and N2 dry
23.1.4.	Inspect: check for via's open over contacts
23.2.	Nitride etch (RIE3) within via's
23.2.1.	O2 chamber clean: O2, 20 sccm, 50 mT, 500 V, 30 min
23.2.2.	CF4 etch: CF4/O2, 20 sccm/1.8 sccm, 10 mT, 250 V, ~13 min
23.2.3.	PR burn: O2, 20 sccm, 10 MT, 250 V, 5 min
23.2.4.	? PR strip in 1165 @ 80 C (AZ300T?, check with Di if Pd is attacked.) ?
23.2.5.	ISO, DI, N2 blow dry
23.2.6.	PE2 O2 descum 300 mT, 100 W, 1 min
23.3.	Resist dep (3 layers SF11, 1 layer SPR955CM-1.8)
23.3.1.	First layer
23.3.1.1.	Blow sample with N2
23.3.1.2.	Dispense SF11, spin 4Krpm, 30 sec
23.3.1.3.	Bake 170 C, 1 min, cool for 1 min
23.3.2.	Second layer
23.3.2.1.	Blow sample with N2
23.3.2.2.	Dispense SF11, spin 4Krpm, 30 sec
23.3.2.3.	Bake 170 C, 1 min, cool for 1 min
23.3.3.	Third layer
23.3.3.1.	Blow sample with N2
23.3.3.2.	Dispense SF11, spin 4 Krpm, 30 sec

23.3.3.3.	Bake 170 C, 2 min, cool for 1 min
23.3.4.	Fourth layer
23.3.4.1.	Blow sample with N2
23.3.4.2.	Dispense SPR955CM-1.8, spin 4Krpm, 30 sec
23.3.4.3.	Bake 95 C, 90 sec
23.4.	Litho
23.4.1.	Autostep 200: “PRMET” mask, time: ~0.4 sec as req’d, focus offset: 0 or as req’d
NOTE:	NOTE: this is not the “PR_Metal” mask used for the active Si run. It is similar, but has corrections for errors found in the original.
23.4.2.	Bake 110 C, 90 sec
23.4.3.	Develop AZ726MIF, 1 min
23.4.4.	UV exposure: 300 sec
23.4.5.	SAL101A: 70 sec
23.4.6.	Repeat 13.3.4+13.3.5 until open and undercut visible
23.4.7.	O2 descum. 1 min, 100 W.
23.5.	Metal dep
23.5.1.	Ebeam1: Ti/Au target thicknesses: 230/30000 [i.e. 230 nm, 3 um]) - rotating chuck with 10 degree tilt
23.6.	Liftoff
23.6.1.	1165, 80 C
23.6.2.	DI rinse
23.7.	Inspection: IV check (JKD)
24.	**Grating open (GO mask)**
24.1.	Sample prep
24.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
24.1.2.	dehydration bake 3 min 120 C
24.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
24.1.4.	spin HMDS 3krpm, 30 s
24.2.	Litho
24.2.1.	N2 blow
24.2.2.	Dispense PR: SPR955-1.8, Spin 3 krpm for 30 s (recipe 5)
24.2.3.	Soft bake: 95C, 90 s
24.2.4.	Autostep 200: “GO” mask, time: ~0.4 sec or as req’d, focus offset: 0 or as req’d
24.2.5.	Post exposure bake 110 C, 90 sec
24.2.6.	Develop pattern ~120 s MIF 726
24.2.7.	N2 dry, dehydration bake 110 C, 30 sec
24.2.8.	O2 descum 300 mT/100W 30 sec
24.2.9.	Inspect under microscope: open holes, no residue
24.3.	SU8 etch
24.3.1.	TBD
24.4.	Buffer etch
24.4.1.	Dry etch 75% through
24.4.1.1.	Panasonic ICP2 - Check gasses (CHF3)
24.4.1.2.	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
24.4.1.3.	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
24.4.1.4.	Etch nitride (700 nm) and 50% (350 nm) of oxide layer in ICP2: estimated 3 min etch (Double check!)
24.4.1.5.	Recipe 103: O2 clean (5 min)
24.4.2.	SiO2 wet etch
24.4.2.1.	Etch any remaining SiO2 in BHF, ~60 s. It is not critical that all oxide be removed as it was for the SVIA step.
24.4.2.2.	Inspect edge of vias. Undercut visible?
24.5.	Remove PR
24.5.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
24.5.2.	PRX127 soak 1: 10-20 min, 80 C with U/S freq 5, 5 sweep, high toggle
24.6.	DICING/POLISHING/TESTING (JKD)
25.	**Heavy ion implant**
	TBD – done after chips have been diced/polished/tested

Beam-steering: Silicon phase modulators

	General comments:
	Do DI rinse after ISO cleans.
	After bonding, use glass slides underneath samples during PECVD depos.
	After 1165, DON'T use Acetone; use Iso.
	After 1165, do a descum.
	Sample cleans are generally listed at the beginning of each step; if stopping for more than a few minutes between steps, perform a sample clean (Acetone/IPA/DI 3 mins each, N2 blow, 100C 3 mins).
	Never allow acetone or DI to dry on the sample; rinse acetone off in IPA while wet; blow DI off with N2 while wet and then immediately dehydrate on hot plate.
	ALL MASKS FOR THIS RUN ARE LABELLED WITH THE PREFIX "aSi". THIS RUN IS ALSO DENOTED "SWEEPER 3.1".
1.	**Sample parameters.**
1.1.	Silicon:
1.1.1.	BOX thickness:
1.1.2.	Top Silicon height: 500 nm
2.	**Dice and cleave samples**
2.1.	Silicon:
2.1.1.	16 mm x 16 mm die, 2 per chip works, ideal is 24 mm x 46 mm total size.
3.	**WG etch (aSi-RIBLAYER)**
3.1.	Sample prep
3.1.1.	Acetone with ultrasonic 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min
3.1.2.	Dry with N2, dehydration bake 3 min 100 C
3.1.3.	Piranha Clean - H_2SO_4:H_2O_2 (3:1) 10 min or until Bubbling on sample stops.
3.1.4.	BHF dip 60 sec, Di Rinse
3.1.5.	Dehydration bake 3 mins 100 C
3.2.	PECVD hard mask deposition
3.2.1.	SiO2 clean, 30 min
3.2.2.	SiO2 deposition, 2750 A (clean, check oxide thickness on dummy with Filmetrics)
3.3.	WG litho (aSi-RIBLAYER mask)
3.3.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
3.3.2.	Dehydration / HMDS
3.3.2.1.	bake 150 C, 5 mins
3.3.2.2.	spin HMDS 3K, 30 sec
3.3.3.	Spin PR
3.3.3.1.	Blow sample with N2
3.3.3.2.	Dispense resist: SPR955CM0.9
3.3.3.3.	Spin @ 3k for 30 s (recipe 5)
3.3.3.4.	Soft bake: 95C, 90 sec
3.3.4.	Spin CEM
3.3.4.1.	Blow sample with N2
3.3.4.2.	Dispense CEM: CEM365-1
3.3.4.3.	Spin @5k for 45s (5000 acceleration)
3.3.5.	Autostep 200: "RIBLAYER" mask, time: 0.5–1 sec as req'd, focus offset: 0 or as req'd
3.3.5.1.	.75 sec exposure
3.3.6.	DI rinse until hydrophobic
3.3.7.	Post exposure bake 110 C, 90 sec
3.3.8.	Develop pattern ~90 s MIF 726
3.3.9.	N2 dry, dehydration bake 110 C, 30 sec
3.3.10.	O2 descum 300 mT/100W 30 sec
3.3.11.	Inspect under microscope:
3.3.11.1	rib clusters top left: Check rib width ~ 1um.
3.3.11.2	gaps in directional couplers (upper left, under "trombones")
3.3.11.3	gaps in MMI splitters (below directional couplers)
3.3.11.4	gaps visible in microring couplers (above the wavy design in quads 1-3, please check quadrant 3)
3.3.11.5	gaps in MMI "trees" (lower center, left edge of quadrant 4)

3.4.	SiO2 Hard mask etch
3.4.1.	Panasonic ICP2 (switch to CHF3 if necessary)
3.4.1.1.	Recipe 100: O2 clean, CHF3 coat (5 min/3 min) without sample
3.4.1.2.	Recipe 101: SiO2Vert etch (2200 A/min) with sample: Etch time: 1min 45 sec (20% over etch)
3.4.1.3.	Recipe 103: O2 clean (5 min)
3.4.2.	Remove PR
3.4.2.1.	PR ash in PE2 O2 300 mT, 100 W, 120 s
3.4.2.2.	PRX127 soak 1: 10 min @ 70 C with sonication
3.4.2.3.	PRX127 soak 2: 10 min @ 70 C with sonication
3.4.2.4.	IPA soak: 3 min with sonication
3.4.2.5.	DI rinse for 5 min
3.4.2.6.	Piranha 10 mins or until bubbling stops. DI rinse.
3.5.	Si WG etch
3.5.1.	Panasonic ICP 2, check recipe
3.5.1.1.	Recipe 107: CF4/O2 Clean + chamber coat (5min, 1 min)
3.5.1.2.	Recipe 127: Si etch. Etch time: ~1:00
3.5.1.3.	Recipe 106: CF4/O2 clean (10 min)
3.6.	SiO2 hard mask removal
3.6.1.	BHF dip 60 sec, DI rinse
3.7.	Dektak step height
3.7.1.	Step height:
3.7.2.	Target is 275 nm +/- 25 nm
4.	**N+ doping (aSi-NDOPE1)**
4.1.	Sample prep
4.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
4.1.2.	Pirhana 10 mins or until bubbling stops
4.1.3.	BHF dip 30 sec, DI rinse
4.1.4.	Thorough DI rinse: 10 minutes in running DI
4.1.5.	Dehydration bake 150 C, 5 mins
4.2.	ALTERNATE SAMPLE PREP (OXIDATION SPLIT)
4.2.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
4.2.2.	Pirhana 10 mins or until bubbling stops
4.2.3.	BHF dip 30 sec, DI rinse
4.2.4.	Thorough DI rinse: 10 minutes in running DI
4.2.5.	Pirhana 10 mins or until bubbling stops
4.2.6.	BHF dip 30 sec, DI rinse
4.2.7.	Thorough DI rinse: 10 minutes in running DI
4.2.8.	Pirhana 10 mins or until bubbling stops
4.2.9.	BHF dip 30 sec, DI rinse
4.2.10.	Thorough DI rinse: 10 minutes in running DI
4.2.11.	Dehydration bake 150 C, 5 mins
4.3.	PECVD oxide deposition
4.3.1.	SiO2 clean, 30 min
4.3.2.	Deposit 50 nm SiO2
4.3.2.1.	Solvent clean dummy sample
4.3.2.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)
4.3.2.3.	Oxide thickness:
4.4.	N+ doping litho (aSi-NDOPE1 mask)
4.4.1.	N2 blow (No O2 plasma, may cause problems with coating over the thermal shunt patterns in standard SWEEPER runs)
4.4.2.	Spin PR
4.4.2.1.	HMDS 3000 rpm 30 sec
4.4.2.2.	SPR 955 1.8, 3000 rpm, 30 sec

4.4.3.	Soft bake 95 C, 1.5 mins
4.4.4.	Autostep 200: “aSi-NDOPE1” mask, time: 1.0 sec or as req’d, focus offset: 0 or as req’d
4.4.5.	Post-exposure bake 110C, 1.5 min
4.4.6.	Develop 2 min in MF726
4.4.7.	DI rinse, N2 dry
4.4.8.	Inspect if Vernier tip is open
4.4.9.	O2 Plasma 30 sec 100 W
	*** SEND OUT FOR IMPLANT 3A***
	Implantation parameters: species Phos, dose 8e14 cm^{-2}, energy 90 keV, incidence 7 degrees, room temp
4.5.	N+ doping strip
4.5.1.	1165 Soak resist hard to remove. Use 1165 with U/S, possibly Gasonics instead.
4.5.2.	If necessary use a BHF dip (60 sec) to remove the underlying oxide, but ideally leave this on for the P-doping step. It is not a big deal if the resist does not get completely stripped as long as the P-doping windows are clear.
5.	**P+ doping (aSi-PDOPE1)**
5.1.	Sample prep
5.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
5.1.2.	Pirhana 10 mins
5.1.3.	BHF dip 60 sec, DI rinse
5.1.4.	Dehydration bake 150 C, 5 mins
5.2.	PECVD oxide deposition (skip this if the NDOPE oxide is still intact)
5.2.1.	Deposit 50 nm SiO2
5.2.1.1.	Solvent clean dummy sample
5.2.1.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)
5.2.1.3.	Oxide thickness:
5.3.	P+ doping litho (aSi-PDOPE1 mask)
5.3.1.	N2 blow (No O2 plasma, may cause problems with coating over thermal shunt patterns)
5.3.2.	Spin photoresist
5.3.2.1.	HMDS 3000 rpm 30 sec
5.3.2.2.	SPR 955 1.8: 3000 rpm, 30 sec
5.3.3.	Soft bake 95 C, 1.5 mins
5.3.4.	Autostep 200: “aSi-PDOPE1” mask, time: 1.0 sec or as req’d, focus offset: 0 or as req’d
5.3.5.	Post-exposure baks 110 C, 1.5 mins
5.3.6.	Develop 2 mins in MF726
5.3.7.	DI rinse, N2 dry
5.3.8.	Inspect if Vernier tip is open
5.3.9.	O2 Plasma 30 sec 100 W
	*** SEND OUT FOR IMPLANT 3B ***
	Implantation parameters: species Boron, dose 8e14 cm^{-2}, energy 50 keV, incidence 7 degrees, room temp
5.4.	P+ doping strip
5.4.1.	1165 Soak Resist hard to remove. Use 1165 with U/S. Possibly Gasonics instead.
5.4.2.	If necessary use a BHF dip (60 sec) to remove the underlying oxide, but ideally leave this on for the P-doping step. It is not a big deal if the resist does not get completely stripped as long as the P-doping windows are clear.
6.	**P doping (aSi-PDOPE2)**
6.1.	Sample prep
6.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
6.1.2.	Pirhana 10 mins
6.1.3.	BHF dip 60 sec, DI rinse
6.1.4.	Dehydration bake 150 C, 5 mins
6.2.	PECVD oxide deposition (skip this if the PDOPE oxide is still intact)
6.2.1.	Deposit 50 nm SiO2
6.2.1.1.	Solvent clean dummy sample
6.2.1.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)

6.2.1.3.	Oxide thickness:
6.3.	P doping litho (aSi-PDOPE2 mask)
6.3.1.	N2 blow (No O2 plasma, may cause problems with coating over thermal shunt patterns)
6.3.2.	Spin photoresist
6.3.2.1.	HMDS 3000 rpm 30 sec
6.3.2.2.	SPR 955 1.8: 3000 rpm, 30 sec
6.3.3.	Soft bake 95 C, 1.5 mins
6.3.4.	Autostep 200: "aSi-PDOPE2" mask, time: 1.0 sec or as req'd, focus offset: 0 or as req'd
6.3.5.	Post-exposure baks 110 C, 1.5 mins
6.3.6.	Develop 2 mins in MF726
6.3.7.	DI rinse, N2 dry
6.3.8.	Inspect if Vernier tip is open
6.3.9.	O2 Plasma 30 sec 100 W
	*** SEND OUT FOR IMPLANT 3C ***
	Implantation parameters: species Boron, dose 1e13 cm^{-2}, energy 90 keV, incidence 7 degrees, room temp
6.4.	P doping strip
6.4.1.	Piranha 10 mins ß *** make sure all resist is gone ***
6.4.2.	BHF dip 60 sec, longer if necessary to remove resist fragments, but no longer than absolutely necessary given the problems we've been seeing with surface damage.
6.4.3.	Thorough DI rinse, N2 dry
6.4.4.	Once sample is clean (inspect under microscope), follow immediately with anneal
7.	**Activation Anneal**
7.1.	Anneal
7.1.1.	RTA 1050 C in flowing N2, 5 mins, 30 sec ramp up/down
7.2.	Inspect
7.2.1.	Optical microscope inspection: look for signs of cracking or of baked-on contaminant. The surface should look smooth and clean.
8.	**Protection film**
8.1.	Sample prep
8.1.1.	Acetone with ultrasonic 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min
8.1.2.	Dry with N2, dehydration bake 3 min 100 C
8.1.3.	Dehydration bake 3 mins 150 C
8.2.	PECVD oxide deposition
8.2.1.	SiO2 clean, 30 mins
8.2.2.	Deposit 700 nm SiO2 (350 nm + 350 nm)
8.2.2.1.	Solvent clean dummy sample
8.2.2.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)
8.2.2.3.	Oxide thickness:
8.3.	PECVD nitride deposition
8.3.1.	SiN clean, 30 min
8.3.2.	Deposit 700 nm SiN (350 nm + 350 nm) (actual and dummy)
8.3.2.1.	Solvent clean dummy sample
8.3.2.2.	Measure nitride thickness of dummy using Filmetrics (do not discard dummy)
8.3.2.3.	Nitride thickness:
9.	**Contact via (aSi-VIA1)**
9.1.	Sample prep
9.1.1.	Dehydration / HMDS
9.1.1.1.	bake 150 C, 5 mins
9.1.1.2.	spin HMDS 3K, 30 sec
9.2.	Litho (aSi-VIA1 mask)
9.2.1.1.	N2 blow
9.2.1.2.	Dispense PR: SPR955-1.8, Spin 3krpm for 30 s (recipe 5)
9.2.1.3.	Soft bake: 95C, 90 sec
9.2.2.	Autostep 200: "SVia" mask, time: ~0.4 sec or as req'd, focus offset: 0 or as req'd
9.2.3.	Post exposure bake 110 C, 90 sec
9.2.4.	Develop pattern ~120 s MIF 726

9.2.5.	N2 dry, dehydration bake 110 C, 30 sec
9.2.6.	O2 descum 300 mT/100W 30 sec
9.2.7.	Inspect under microscope: open holes, no residue
9.3.	Protection film etch
9.3.1.	Dry etch 75% through
9.3.1.1.	Panasonic ICP2 - Check gasses (CHF3)
9.3.1.2.	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
9.3.1.3.	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
9.3.1.4.	Etch nitride (700 nm) and 110% (700 nm + 70 nm) of oxide layer in ICP2: estimated 6.5 min etch (Double check!)
9.3.1.5.	Recipe 103: O2 clean (5 min)
9.3.2.	SiO2 wet etch
9.3.2.1.	Etch any remaining SiO2 in BHF, ~60 s.
9.3.2.2.	Inspect edge of vias. Undercut visible?
9.4.	Remove PR
9.4.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
9.4.2.	PRX127 soak 1: 10-20 min, 80 C with U/S freq 5, 5 sweep, high toggle
10.	**Contact metal (aSi-CONTACT)**
10.1.	Contact metal litho (aSi-CONTACT mask)
10.1.1.	Sample prep
10.1.1.1	Acetone 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min
10.1.1.2	Dehydration bake 3 min, 120 C
10.1.1.3	PE2 O2 descum 300 mT, 100 W, 1 min
10.1.2.	Spin resist
10.1.2.1	Blow N2
10.1.2.2	Dispense SF11, spin 30 sec, 4 krpm
10.1.2.3	Bake 2 mins, 170 C, cool for 1 min, blow N2
10.1.2.4	Dispense SF11, spin 30 sec, 4 krpm
10.1.2.5	Bake 2 mins, 170 C, cool for 1 min, blow N2
10.1.2.6	Dispense SPR955CM-1.8, spin 30 sec, 3 krpm
10.1.2.7	Bake 90 sec, 95 C
10.1.3.	Expose in stepper 0.35 sec, offset: 0
10.1.4.	Post bake 90 sec, 110 C
10.1.5.	Develop AZ726MIF, 1 min
10.1.6.	UV exposure 300 sec
10.1.7.	SAL101A 70 sec
10.1.8.	UV exposure 300 sec
10.1.9.	SAL101A 70 sec
10.1.10.	Inspect pattern, verify undercut
10.2.	Metal deposition
10.2.1.	20:1 DI:HF dip (5 s)
10.2.2.	DI rinse
10.2.3.	Ebeam 3 Ti/Pt/Au (170/170/1000 A) (must follow DI:HF dip/rinse immediately)
10.2.4.	Liftoff 1165, 80 C for ~2 hours.
10.2.5.	ISO, DI rinse 5 mins each with gentle agitation
10.3.	Liftoff
10.3.1.	Acetone with flushing using pipette
10.3.2.	Rinse thoroughly
10.3.3.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
10.3.4.	Inspect (quick, but make sure there are no contaminants on the surface. If contaminated, repeat 10.3.3. Otherwise move to step 10.3.5 as quickly as possible)
10.3.5.	Strip Annealer: 30 sec, 360 C
11.	**Buffer (nitride / SU8 / nitride)**
11.1.	Sample prep
11.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
11.1.2.	dehydration bake 3 min 120 C

11.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
11.2.	Nitride dep (for adhesion)
11.2.1.	Dehydration bake 5 min @ 150 C
11.2.2.	PECVD 20 nm of SiN
11.3.	SU8 spin
11.3.1.	Blow N2
11.3.2.	Dispense SU-8 2002
11.3.2.1	Spread 500 rpm, 10 s (ramp 100 rpm/s)
11.3.2.2	Coating: 3 krpm, 30 s (ramp 500 rpm/s)
11.3.3.	Soft bake: 95 C, 3 min
11.4.	Hard bake
11.4.1.	95 C to start
11.4.2.	Ramp to 150 C, hold 5 min
11.4.3.	Ramp to 205 C, hold 5 min
11.4.4.	Ramp to 260 C, hold 30 min
11.4.5.	Ramp down 205 C, hold 5 min
11.4.6.	Ramp down 150 C, hold 5 min
11.4.7.	Ramp down 95 C, remove from hot plate
11.4.8.	Colour should be dark red
11.5.	Adhesion nitride
11.5.1.	PECVD SiN clean, 30 min
11.5.2.	PECVD 300 nm SiN
12.	**Probe via (aSi-VIA2) - (also opens SU8 for ION, GO steps)**
12.1.	Sample prep
12.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
12.1.2.	dehydration bake 3 min 120 C
12.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
12.1.4.	spin HMDS 3krpm, 30 s
12.2.	Litho (aSi-VIA2 mask)
12.2.1.	N2 blow
12.2.2.	Dispense PR: SPR220 3 um, Spin 3 krpm for 30 s (recipe 5)
12.2.3.	Soft bake: 95C, 120 s
12.2.4.	Autostep 200: "aSi-VIA2" mask, time: ~0.4 sec or as req'd, focus offset: 0 or as req'd
12.2.5.	Post exposure bake 110 C, 90 sec
12.2.6.	Develop pattern ~120 s MIF 726
12.2.7.	N2 dry, dehydration bake 110 C, 30 sec
12.2.8.	O2 descum 300 mT/100W 30 sec
12.2.9.	Bake 120C for 10 min to increase selectivity during ICP etch.(Resist is 2.4um now)
12.2.10.	Inspect under microscope: open holes, no residue
12.3.	SU8 etch (ICP2)
12.3.1.	Recipe 103: O2 clean
12.3.2.	SiN Etch. Recipe 181: 2 min 30 sec (~175 nm/min SiN etch rate). O2=5, CF4=50, Pa = 2.0, Rf= 500W, Bias = 25W.
12.3.3.	Su8 Etch. Recipe 169: Time TBD. Etch rate: 400 nm/min.. O2 = 40, CF4= 4, Pa = 1.0, Rf = 350W, Bias = 50W. Note: Need N2 purge every 5 min. Last time etch was 7 min total but done in two steps of 3 min 30 sec with a N2 purge in between etches.
12.3.4.	SiN Etch. Recipe 181: 30 sec
13.	**Probe metal (aSi-PRMET)**
13.1.	Resist dep (3 layers SF11, 1 layer SPR955CM-1.8)
13.1.1.	First layer
13.1.1.1	Blow sample with N2
13.1.1.2	Dispense SF11, spin 4Krpm, 30 sec
13.1.1.3	Bake 170 C, 1 min, cool for 1 min
13.1.2.	Second layer
13.1.2.1	Blow sample with N2
13.1.2.2	Dispense SF11, spin 4Krpm, 30 sec

13.1.2.3	Bake 170 C, 1 min, cool for 1 min
13.1.3.	Third layer
13.1.3.1	Blow sample with N2
13.1.3.2	Dispense SF11, spin 4 Krpm, 30 sec
13.1.3.3	Bake 170 C, 2 min, cool for 1 min
13.1.4.	Fourth layer
13.1.4.1	Blow sample with N2
13.1.4.2	Dispense SPR955CM-1.8, spin 4Krpm, 30 sec
13.1.4.3	Bake 95 C, 90 sec
13.2.	Litho (aSi-PRMET)
13.2.1.	Autostep 200: “aSi-PRMET” mask, time: ~0.4 sec as req’d, focus offset: 0 or as req’d
13.2.2.	Bake 110 C, 90 sec
13.2.3.	Develop AZ726MIF, 1 min
13.2.4.	UV exposure: 300 sec
13.2.5.	SAL101A: 70 sec
13.2.6.	Repeat 13.3.4+13.3.5 until open and undercut visible
13.2.7.	O2 descum. 1 min, 100 W.
13.3.	Metal dep
13.3.1.	Ebeam1: Ti/Au target thicknesses: 230/30000 [i.e. 230 nm, 3 um]) - rotating chuck with 10 degree tilt
13.4.	Liftoff
13.4.1.	1165, 80 C
13.4.2.	DI rinse
13.4.3.	Inspection
14.	**Grating open (aSi-GO/ION mask) - (also opens windows through oxide/nitride for ION step)**
	NOTE: THIS STEP ETCHES DOWN TO THE RIBS – DO NOT DRY ETCH INTO THE SILICON
14.1.	Sample prep
14.1.1.	Solvent clean (acetone/IPA/DI 3 mins each, N2 dry)
14.1.2.	dehydration bake 3 min 120 C
14.1.3.	PE2 O2 descum 300 mT, 100 W, 1 min
14.1.4.	spin HMDS 3krpm, 30 s
14.2.	Litho
14.2.1.	N2 blow
14.2.2.	Dispense PR: SPR955-1.8, Spin 3 krpm for 30 s (recipe 5)
14.2.3.	Soft bake: 95C, 90 s
14.2.4.	Autostep 200: “aSi-GO/ION” mask, time: ~0.4 sec or as req’d, focus offset: 0 or as req’d
14.2.5.	Post exposure bake 110 C, 90 sec
14.2.6.	Develop pattern ~120 s MIF 726
14.2.7.	N2 dry, dehydration bake 110 C, 30 sec
14.2.8.	O2 descum 300 mT/100W 30 sec
14.2.9.	Inspect under microscope: open holes, no residue
14.3.	Buffer etch
14.3.1.	Dry etch 75% through
14.3.1.1	Panasonic ICP2 - Check gasses (CHF3)
14.3.1.2	Recipe 100: O2 clean, CF3 coat (5 min/1 min)
14.3.1.3	Recipe 101: SiO2Vert etch (~3100 A/min SiN etch rate).
14.3.1.4	Etch nitride (700 nm) and 50% (350 nm) of oxide layer in ICP2: estimated 3 min etch (Double check!)
14.3.1.5	Recipe 103: O2 clean (5 min)
14.3.2.	SiO2 wet etch
14.3.2.1	Etch any remaining SiO2 in BHF, ~60 s. It is not critical that all oxide be removed as it was for the SVIA step.
14.3.2.2	Inspect edge of vias. Undercut visible?
14.4.	Remove PR
14.4.1.	PR ash in PE2 O2. 300 mT, 100 W, 120 s
14.4.2.	PRX127 soak 1: 10-20 min, 80 C with U/S freq 5, 5 sweep, high toggle
14.4.3.	Inspect to ensure all PR is removed.
15.	**Photodiode implant (aSi-ION)**
15.1.	Sample prep

15.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)
15.1.2.	Dehydration bake 150 C, 5 mins
15.2.	Photodiode implant litho (aSi-ION mask)
15.2.1.	Spin photoresist
15.2.1.1	HMDS 3000 rpm 30 sec
15.2.1.2	SPR 955 1.8: 3000 rpm, 30 sec
15.2.2.	Soft bake 95 C, 1.5 mins
15.2.3.	Autostep 200: "aSi-ION" mask, time: 1.0 sec or as req'd, focus offset: 0 or as req'd
15.2.4.	Post-exposure baks 110 C, 1.5 mins
15.2.5.	Develop 2 mins in MF726
15.2.6.	DI rinse, N2 dry
15.2.7.	Inspect if Vernier tip is open
15.2.8.	O2 Plasma 30 sec 100 W
	*** SEND OUT FOR IMPLANT 3D ***
	Implantation parameters: species Boron, dose 1e12 cm^{-2}, energy 350 keV, 7 degrees, room temp
15.3.	Photodiode implant strip
15.3.1.	1165 Soak. Resist should not be hard to remove this time. Use 1165 with U/S. Possibly Gasonics instead.
15.3.2.	CAN THIS BE REPLACED WITH AN ACETONE RINSE? DO NOT WANT EXPOSED SI SEEING 1165 SOAK.
	Sample is ready for dicing/polishing.

Beam-steering: Phase 3

INDEX	STEP	TIME
0	**Sample parameters.**	
0.1.	**SOI: 4" wafers**	
0.1.1.	BOX thickness: 1 um	
0.1.2.	Top Silicon height: 500 nm	
1	**WG etch (SWP5-RIB)**	
1.1.	**Sample prep**	
1.1.1.	Acetone with ultrasonic 3 min / Isopropyl alcohol (IPA) 3 min / DI rinse 3 min	
1.1.2.	Dry with N2, dehydration bake 3 min 100 C	
1.1.3.	Piranha Clean - H2SO4:H2O2 (3:1) 10 min or until Bubbling on sample stops.	
1.1.4.	BHF dip 30 sec, or until hydrophic, Di Rinse	
1.1.5.	Dehydration bake 5 mins 150 C	
1.2.	**Litho (SWP5-RIB)**	
1.2.1.	Dispense DSK 101-307, spin at recipe 8, left spinner, bay 7	
1.2.2.	Bake DSK 101 @ 170C (ceramic hotplate in bay 7)	1min
1.2.3.	Dispense UV 210, spin at recipe 8, left spinner, bay 7	
1.2.4.	Softbake on 135C hotplate in bay 7	1min
1.2.5.	Expose in ASML. (check ephi3 program for all parameters)	
1.2.6.	**PEB on 135C hotplate in bay 7**	90s
1.2.7.	Develop in AZ300MIF, no agitation	45s
1.3.	**Rib Etch**	
1.3.1.	Bosch etcher: Manual mode O2 clean, temp 10C	30 min
1.3.2.	Etch: CAO_N_1. Etch rate ~3.4nm/s, etch 250nm. Etch rate varies, must run test piece, (1min	
1.3.3.	PR strip. Use 80C 1165 in ultrasonic. Switch to high, dials to 10	30 min
1.4.	**Measure**	
1.4.1.	Dektak patterns for rib layer at top left, mid left, lower left, and top right on each die	
1.4.2.	Etch target: 250 nm +/- 30 nm	
2	**N+ doping (SWP5-NDOPE)**	
2.1.	**Sample prep (multiple piranha cleans to improve sidewall smoothness)**	

2.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)	
2.1.2.	Pirhana 10 mins or until bubbling stops	
2.1.3.	BHF dip 30 sec, DI rinse	
2.1.4.	Thorough DI rinse: 10 minutes in running DI	
2.1.5.	Pirhana 10 mins or until bubbling stops	
2.1.6.	BHF dip 30 sec, DI rinse	
2.1.7.	Thorough DI rinse: 10 minutes in running DI	
2.1.8.	Pirhana 10 mins or until bubbling stops	
2.1.9.	BHF dip 30 sec, DI rinse	
2.1.10.	Thorough DI rinse: 10 minutes in running DI	
2.1.11.	Dehydration bake 150 C, 5 mins	
2.2.	**PECVD oxide deposition (may replace this with sputtered oxide)**	
2.2.1.	SiO2 clean, 30 min	
2.2.2.	Deposit 50 nm SiO2	
2.2.2.1.	Solvent clean dummy sample	
2.2.2.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)	
2.2.2.3.	Oxide thickness:	
2.3.	**N+ doping litho (SWP5-NDOPE mask)**	
2.3.1.	N2 blow (No O2 plasma, may cause problems with coating over the thermal shunt patterns in	
2.3.2.	Spin PR	
2.3.2.1.	HMDS 3000 rpm 30 sec	
2.3.2.2.	SPR 955 1.8, 3000 rpm, 30 sec	
2.3.3.	Soft bake 95 C, 1.5 mins	
2.3.4.	Autostep 200: “SWP5-NDOPE” mask, time: 0.8 sec or as req’d, focus offset: 0 or as req’d	
2.3.5.	Post-exposure bake 110C, 1.5 min	
2.3.6.	Develop 2 min in MF726	
2.3.7.	DI rinse, N2 dry	
2.3.8.	Inspect if Vernier tip is open. Alignment tolerance ±300 nm	
2.3.9.	**O2 Plasma 30 sec 100 W**	
Implant	SEND OUT FOR IMPLANT 5A_1: species Phos, dose 8e14 cm-2, energy 90 keV, incidence 0	
2.4.	**N+ doping strip**	
2.4.1.	1165 Soak resist hard to remove. Use 1165 with U/S, possibly Gasonics instead. Piranha also	
2.4.2.	If necessary use a BHF dip (60 sec) to remove the underlying oxide, but ideally leave this on	
3	**P+ doping (SWP5-PDOPE)**	
3.1.	**Sample prep**	
3.1.1.	Solvent clean (acetone with ultrasonic/IPA/DI 3 mins each, N2 dry)	
3.1.2.	Pirhana 10 mins	
3.1.3.	**BHF dip 60 sec, DI rinse**	
3.1.4.	Dehydration bake 150 C, 5 mins	
3.2.	**PECVD oxide deposition (skip this if the NDOPE oxide is still intact)**	
3.2.1.	**Deposit 50 nm SiO2**	
3.2.1.1.	Solvent clean dummy sample	
3.2.1.2.	Measure oxide thickness of dummy using Filmetrics (do not discard dummy)	
3.2.1.3.	Oxide thickness:	
3.3.	**P+ doping litho (SWP5-PDOPE mask)**	
3.3.1.	N2 blow (No O2 plasma, may cause problems with coating over thermal shunt patterns)	
3.3.2.	Spin photoresist	
3.3.2.1.	HMDS 3000 rpm 30 sec	
3.3.2.2.	SPR 955 1.8: 3000 rpm, 30 sec	
3.3.3.	Soft bake 95 C, 1.5 mins	
3.3.4.	Autostep 200: “aSi-PDOPE1” mask, time: 0.8 sec or as req’d, focus offset: 0 or as req’d	
3.3.5.	Post-exposure baks 110 C, 1.5 mins	
3.3.6.	Develop 2 mins in MF726	
3.3.7.	DI rinse, N2 dry	
3.3.8.	Inspect if Vernier tip is open. Alignment tolerance ±300 nm	
3.3.9.	O2 Plasma 30 sec 100 W	
Implant	SEND OUT FOR IMPLANT 5A_2: species Boron, dose 8e14 cm-2, energy 50 keV, incidence	
3.4.	**P+ doping strip**	

3.4.1.	Piranha 10 mins ⇓ *** it is critical to make sure all resist is gone ***	
3.4.2.	BHF dip 60 sec, longer if necessary to remove resist fragments, but no longer than absolutely	
3.4.3.	Thorough DI rinse, N2 dry	
3.4.4.	**Once sample is clean (inspect under microscope), follow immediately with anneal**	
4	**Activation Anneal**	
4.1.	Anneal	
4.1.1.	**RTA 900 C in flowing N2, 10 mins, 30 sec ramp up/down**	
4.2.	Inspect	
4.2.1.	**Optical microscope inspection: look for signs of cracking or of baked-on contaminant.**	
5	**Vertical Channels (SWP5-VC)**	
5.1.	Sample prep	
5.1.1.	Piranha clean – 3:1 H2SO4:H2O2 on 80C hot plate.	
5.1.2.	BHF dip 30 sec or until hydrophobic	
5.2.	Dehydration bake	
5.2.1.	150 C, 5 mins	
5.2.2.	**Cool sample; place on blue tape with puncture in middle**	
5.3.	Vertical Channel litho (SWP5-VC mask)	
5.3.1.	N2 blow	
5.3.2.	dispense HMDS. Puddle 20s.	
5.3.3.	spin HMDS recipe 5. Replace spinner bowl napkin.	
5.3.4.	**Dispense PR: SPR955 1.8, Spin recipe 5 (3krpm for 30 s)**	
5.3.5.	Soft bake: 95C, 90 sec	
5.3.6.	Autostep 200: “SWP5 VC” mask, time: ~0.8 sec as req’d, focus offset: 0 or as req’d	
5.3.7.	Post exposure bake 115 C, 90 sec	
5.3.8.	**Develop pattern ~60 s AZ726MIF; DI rinse, N2 dry**	
5.3.9.	Inspect pattern in microscope. Alignment tolerance ±500 nm	
5.4.	Descum	
5.4.1.	PE2 O2 descum 300 mT, 100 W, 30 sec	
5.5.	Si etch to BOX, Bosch etch	
5.5.1.	Bosch etcher, CAO_N_1 roughly 2.15 nm/sec varies with sample size and exposed Si area.	
5.5.2.	PE2 O2 descum 100 W/300 mT, 4 min.	
5.6.	**Remove PR**	
5.6.1.	80C 1165 ultrasonic 20 mins	
5.6.2.	Inspect for clean surface – if not clean, repeat O2 descum, piranha clean	
6	**Grating Definition**	
6.1.	Pre-clean: Remove native oxide and/or dielectric hardmask	
6.1.1.	HF dip	
6.1.2.	Ebeam PR spin coat (2:1 ZEP)	
6.1.3.	**ACE,ISO,DI**	
6.1.4.	PEII - O2 Descum (100W, 300mTorr, 60sec)	
6.1.5.	Dehydration Bake (150C, 5min)	
6.1.6.	N2 Gun (1min) Cools and cleans wafer	
6.2.	**Spin 2:1 ZEP-520A:Anisol("A Thinner") (3000rpm, 30sec) - Recipe 5 ~225nm, Use a**	
6.2.1.	Pre-Exposure Bake (180C, 4min) Cover hotplate top to prevent additional particulate	
6.3.	Thermal Au Evaporation	
6.3.1.	Evaporate 11nm Au	
6.4.	**ALTERNATE to Au: Conductive Polymer (This is recommended if you have Si electrical**	
6.4.1.	Spin on Conductive Polymer (Aquasave) (3000rpm, 30sec)	
6.4.2.	Pre-Exposure Bake (90C, 1min) Cover hotplate top to prevent additional particulate	
6.5.	Ebeam Writing Conditions	
6.5.1.	**Shallow Grating write file - Output Grating and PC lens**	
6.5.2.	4th Lens	
6.5.3.	Dose 350uC/cm2 (Please be aware this is pitch dependent, but has shown good results over a	
6.5.4.	Development	
6.5.5.	(If thermal Au is used) Remove Au in wet Au etchant 10s	
6.5.6.	DI Rinse 1min (required to rinse Au etchant AND remove conductive polymer)	
6.5.7.	N2 Dry (be gentle on the gratings)	

6.5.8.	1:1 MIBK:ISO Development - 60s Use a fresh batch	
6.5.9.	9:1 MIBK:ISO Rinse - 15s DO NOT RINSE WITH DI	
6.5.10.	N2 Dry DO NOT RINSE WITH DI	
6.6.	Grating Etch	
6.6.1.	AFM etch depth calibration recommended	
6.6.2.	30min chamber clean in manual mode with cleaning wafer - 30mT, O2/Ar flow-	
6.6.3.	**Photonic Crystal Lense Etch - Single Step Bosch Etch Process - BOV_J_01 (19mT,**	
6.6.4.	Rough Rates:	
6.6.4.1.	~170nm/min w/o Sanovac 5	
6.6.4.2.	~141nm/min w/ Sanovac 5	
6.7.	**Strip ZEP (2:1)**	
6.7.1.	**1165 Soak at 80C - 10min**	
6.7.2.	PEII - O2 Descum (100W, 300mTorr, 60-120sec)	
6.8.	Pre-clean: Remove native oxide and/or dielectric hardmask	
6.8.1.	**HF dip**	
6.9.	**Ebeam PR spin coat (%100 ZEP)**	
6.9.1.	**ACE,ISO,DI**	
6.9.2.	PEII - O2 Descum (100W, 300mTorr, 60sec)	
6.9.3.	Dehydration Bake (150C, 5min)	
6.9.4.	N2 Gun (1min) Cools and cleans wafer	
6.9.5.	Spin 100% ZEP-520A (2000rpm, 30sec) - Recipe 5 ~225nm, Use a filtered syringe	
6.9.6.	Pre-Exposure Bake (180C, 4min) Cover hotplate top to prevent additional particulate	
6.10.	**Thermal Au Evaporation**	
6.10.1.	Evaporate 11nm Au	
6.11.	**Ebeam Writing Conditions**	
6.11.1.	Deep Grating (DBR) write file	
6.11.2.	4th Lens	
6.11.3.	Dose 600uC/cm2 (Please be aware this is pitch dependent, but has shown good results over a	
6.12.	**Development**	
6.12.1.	(If thermal Au is used) Remove Au in wet Au etchant 10s	
6.12.2.	DI Rinse 1min (required to rinse Au etchant AND remove conductive polymer)	
6.12.3.	N2 Dry (be gentle on the gratings)	
6.12.4.	1:1 MIBK:ISO Development - 90s Use a fresh batch	
6.12.5.	ISO Rinse 45seconds - DO NOT RINSE WITH DI	
6.12.6.	N2 Dry	
6.12.7	PEII - 30s - 300mT/100W	
6.13.	**Grating Etch – Target Etch depth : 170 nm ± 30 nm**	
6.13.1.	**AFM etch depth calibration recommended**	
6.13.2.	O2 clean 30 min – Electrode 10C, Ar 10sccm, O2 20sccm, RF2 800	
6.13.3.	Season with PR wafer with STA_E_01 recipe – 5 min	
6.13.4.	Wait 1 hour for cool down	
6.13.5.	Dummy etch calibration on patterned wafer	
6.13.6.	Scratch PR and dektak. (nm)	
6.13.6.1.	Dektak Etch Depth:	
6.13.6.2.	Calculated etch depth from PR minus PR and Etch	
6.13.7.	Strip PR and dektak dummy	
6.13.7.1.	Dektak Etch Depth:	
6.13.8.	Etch Sample	
	Scratch PR and dektak. (nm)	
6.13.8.1.	Dektak Etch depth:	
	Calculated etch depth from PR minus PR and Etch	
6.14.	Strip ZEP (2:1)	
6.14.1.	**1165 Soak at 80C - 10min**	
6.14.2.	PEII - O2 Descum (100W, 300mTorr, 60-120sec)	
6.14.3.	Dektak Etch depth:	
7	**Bonding**	
7.1.	**Sample prep (silicon)**	
7.1.1.	Piranha clean; 3:1 H2SO4/H2O2. Use 80C hotplate. Top off H2O2 after 10 min	
7.1.2.	Isopropanol clean -ONLY IF NECESSARY- swab or spin/spray with IPA,	

7.1.3.	DI rinse until clean under 10X	
7.2.	**Sample prep (III-V)**	
7.2.1.	PR strip; soak or spin/spray 1165 then iso/di to remove cleaving PR	
7.2.2.	Post PR strip; Iso clean -ONLY IF NECESSARY- Swab or spin/spray with iso,	
7.2.3.	DI rinse until clean under 10X	
7.3.	**InGaAs Cap removal**	
7.3.1.	H2O:H2O2:H3PO4 (38:1:1, 190:5:5 mL) 5 min - Surface color should change	
7.3.2.	DI rinse	5min
7.3.2.1.	ONLY IF NECESSARY: Post cap removal Iso clean. Swab or spin/spray with iso,	
7.3.2.2.	DI rinse until clean under 10X	
7.4.	**Silicon oxide removal**	
7.4.1.	HF dip; use BHF 2 min	
7.5.	**Surface activation**	
7.5.1.	EVG O2 plasma activation on Si - Run Dis0.2mBar 20 min on EVG (see guide for details) on	
7.6.	**Wafer bonding (waveguides perpendicular to major flat)**	
7.6.1.	Stick together – using vacuum wand (check vacuum and battery charge). Align pieces so that	
7.6.2.	Clamp in bonding fixture with graphite sheet. Check torque wrench pressure	
7.6.3.	Anneal 300 C, 1+ hr	
7.7.	**Substrate thinning**	
7.7.1.	Substrate removal - 250 um by polishing in femto lab	
7.7.2.	Wet etch in 3:1 HCL/DI until film looks smooth	
	NO ULTRASONIC FROM THIS POINT FORWARD	
7.7.4.	PR coat – recommend SPR955 1.8 (or thicker)	
7.7.5.	“Mountain” removal – use razor blade ⇓ only if necessary – mountains should not bond based	
7.7.6.	PR strip/clean	
7.7.6.1.	1165 strip	
7.7.6.2.	Swab in tergitol to remove “starry night”	
7.7.6.3.	Acetone/ISO/DI – use darkfield with max lamp pwr and aperture to ensure chip is clean	
	Dice and quarter if needed (if whole wafer was bonded)	
	HMDS and resist SPR 3.0 at 3K	
	Dice and quarter if needed and whole wafer was bonded	
8	**Mesa definition (EPI 0711281-E) (SWP5-MESA2 Mask) (only expose dies with epi)**	
8.1.	**InGaAs cap (etch stop) removal**	
8.1.1.	Etch in 1:1:38 H3PO4:H2O2:DI 5 mins to remove etch stop	
8.1.2.	Inspect	
8.2.	**P-mesa litho (SWP5-MESA2 Mask)**	
8.2.1.	Microscope inspect: cleaning should not be necessary, but do solvent clean (acetone/IPA/DI 3	
8.2.2.	Dehydration bake @ 150C - 5 min	
8.2.3.	Use blue tape	
8.2.4.	Dispense HMDS. Puddle 20s, use recipe 7	
8.2.5.	Dispense SF11, spin at 3000rpm (recipe 5)	
8.2.6.	Remove from tape	
8.2.7.	Bake SF11 at 180C – 2 min	2 min
8.2.8.	Cool 2 min	2 min
8.2.9.	Put chip on blue tape	
8.2.10.	Dispense SPR955-0.9CM, spin at 3000rpm (recipe 5)	
8.2.11.	Remove from tape	
8.2.12.	Softbake at 95C	90s
8.2.13.	Use blue tape again	
8.2.14.	Spin CEM365iS (1 month or less from pour), spin at 4000rpm (recipe 7). Dispense through	
8.2.15.	Expose in autostep. +5 focus offset	0.75s
8.2.16.	DI rinse to remove CEM *BEFORE POST BAKE* (should be hydrophobic) - no agitation	4 min
8.2.17.	PEB at 110C	90s
8.2.18.	Develop in AZ726MIF	120s
8.2.19.	Inspect undercut (2.4 um or greater)	
8.2.20.	PE2 O2 descum, 300mT, 100W	30s
8.4.	**P-mesa HardMask Dep**	
8.4.4.	E-beam 2	
8.4.5.	Deposit SiO2 (300nm)	

8.4.4.	Liftoff in 80C 1165, ISO, DI - 1 hour	60 min
8.4.5.	PE2 O2 descum, 300mT, 100W	2 min
8.4.6.	SEM	
8.5.	**P Mesa Etch**	
8.5.1.	Clean. 20 sccm O2, 125 mT, 500 V, 30 min	30 min
8.5.2.	Precoat. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V, 20 min	20 min
8.5.3.	~33 min, use laser monitor. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V. Stop 1/2 period after	~60 min
8.5.4.	Descum (chip remains in chamber). O2, 20 sccm, 125 mT, 300V, 10 min	
8.6.	Inspect in SEM, capture pictures. Alignment tolerance ±100 nm – use fine align Verniers.	
9	**QW etch ("SWP5-QW2" Mask) (ONLY EXPOSE DIES WITH EPI)**	
9.1.	**QW2 litho**	
9.1.1.	Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
9.1.2.	Dehydration bake @ 150C	10 min
9.1.3.	Use blue tape	
9.1.4.	Dispense HMDS. Puddle 20s, use recipe 7	
9.1.5.	Replace spinner bowl napkin	
9.1.6.	Spin SPR955 1.8, use recipe 4	
9.1.7.	Remove from tape	
9.1.8.	Softbake at 110C	90s
9.1.9.	Expose in autostep. -10 focus offset.	.7s
9.1.10.	PEB at 110C	90s
9.1.11.	Develop in AZ726MIF	60s
9.1.12.	PE2 O2 descum, 300mT, 100W	30s
9.1.13.	Wet etch in H2O/H2O2/H3PO4 15/5/1. Watch carefully, etch time varies. Go for 10s after	~40s
9.1.14.	Strip PR in 80C 1165; use 2nd bath after 10min	10min+1
9.1.15.	If photoresist remains, do 30s PE2 descum	
9 1/2	**Hardmask removal etch ("SWP5-VIA1_3" Mask)**	
	VIA1_3 Litho	
	Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
	Dehydration bake @ 150C	10 min
	Use blue tape	
	Dispense HMDS. Puddle 20s, use recipe 7	
	Replace spinner bowl napkin	
	Spin SPR955 1.8, use recipe 4	
	Remove from tape	
	Softbake at 110C	90s
	Expose in autostep. -10 focus offset.	0.6s
	PEB at 110C	90s
	Develop in AZ726MIF	60s
	PE2 O2 descum, 300mT, 100W	30s
	BHF until silicon is hydrophobic (outside of die).	~1.5 min
	Strip PR in 80C 1165; use 2nd bath after 10min	10min+
	If photoresist remains, do 30s PE2 descum	
	Inspect	
	Inspect carefully to ensure SiO2 is removed. Use SEM.	
	Capture SEM pictures of (a) overall mesa, (b) overall taper, (c) taper tip zoomed in. Alignment	
10	**N-contacts ("SWP5-NMET" mask) (EXPOSE ALL DIES to make liftoff easier)**	
10.1.	**N-contact litho**	
10.1.1.	Sample prep	
10.1.1.1.	If necessary, do solvent clean. (should not be)	
10.1.1.2.	Dehydration bake at 150C	10 min
10.1.2.	Litho	
10.1.2.1.	Use blue tape - Spin SF-15, use recipe 5	
10.1.2.2.	Remove from tape.	
10.1.2.3.	Ramp from 90C to 180C on the "RT Elite" hotplate in bay 6	2 min
10.1.2.4.	Allow chip to cool 1 min	
10.1.2.5.	Use blue tape - spin SPR955-1.8, use recipe 5	
10.1.2.6.	Softbake at 110C	90s
10.1.2.7.	Expose in autostep. 0 focus offset.	0.56s

10.1.2.8.	No post exposure bake! Will cause cracks in SF-15	
10.1.2.9.	Develop in AZ726MIF	40s
10.1.2.10.	DUV flood expose	10 min
10.1.2.11.	Develop in SAL101A	60s
10.1.2.12.	DUV flood expose	10 min
10.1.2.13.	Develop in SAL101A	60s
10.1.2.14.	DUV flood expose (Only if needed)	10 min
10.1.2.15.	Develop in SAL101A (Only if needed)	60s
10.1.2.16.	Inspect pattern; verify resist is cleared and undercut is visible. Save microscope image of mesa	
10.1.3.	PE2 O2 descum, 300mT, 100W	4 min
10.1.4.	DO NOT Verify that PR is hydrophilic	
10.1.5.	Wet etch in H2O/H2O2/H3PO4 15/5/1. You will not be able to see color change.	40s
10.1.6.	Inspect entire III-V area in microscope to ensure etch was successful. Etched region should be	
10.1.6.1.		
10.1.7.	E-beam 4, standard dome fixture	
	Deposit Pd/Ge/Pd/Au/Ti, 10nm/110nm/25nm/1000nm/20nm (Pd and Ge at 1 A/s; Au at 2A/s at	
10.1.9.	Liftoff in 80C 1165	
10.1.10.	Inspect - Alignment tolerance ±300 nm	
11	**N-InP etch ("SWP5-NETCH" mask) (ONLY EXPOSE DIES WITH EPI)**	
11.1.	**Litho (SWP5-NETCH)**	
11.1.1.	Dehydration bake @ 150C	10 min
11.1.2.	Use blue tape. Dispense HMDS. Puddle 20s, use recipe 7	
11.1.3.	Replace spinner bowl napkin	
11.1.4.	Spin SPR955 3, use recipe 5	
11.1.5.	Remove from tape. Softbake at 110C,	90s
11.1.6.	Expose in autostep. -1 focus offset.	0.8s
11.1.7.	PEB at 110C,	90s
11.1.8.	Develop in AZ726MIF,	60s
11.1.9.	PE2 O2 descum, 300mT, 100W,	30s
11.2.	**RIE2 Etch**	
11.2.1.	Clean. 20 sccm O2, 125 mT, 500 V	30 min
11.2.2.	Precoat. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V	20 min
11.2.3.	Use laser monitor. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V. Stop immediately when trace goes	~3-5 min
11.2.4.	Descum (chip remains in chamber). O2, 20 sccm, 125 mT, 300V	10 min
11.2.5.	ICP1 - O2 ash	20 min
11.2.6.	AZ300T develop at 80C	20min +
11.2.7.	Inspect: Alignment tolerance ±300 nm	
12	**Si-contacts ("SWP5-SiMet" mask) (EXPOSE ALL DIES to make liftoff easier)**	
12.1.	**Sample prep**	
12.1.1.	Dehydration bake at 200C	10 min
12.2.	Litho (SWP5-SiMET)	
12.2.1.	Use blue tape. Spin SF-15, use recipe 5	
12.2.2.	Remove from tape.	
12.2.3.	Ramp from 90C to 180C on the "RT Elite" hotplate in bay 6	2 min
12.2.4.	Allow chip to cool	1 min
12.2.5.	Use blue tape	
12.2.6.	Spin SPR955-1.8, use recipe 5	
12.2.7.	Softbake at 110C, 90s	
12.2.8.	Expose in autostep. 0 focus offset.	0.56s
12.2.9.	No post exposure bake! Will cause cracks in SF-15	
12.2.10.	Develop in AZ726MIF	40s
12.2.11.	DUV flood expose	10 min
12.2.12.	Develop in SAL101A	60s
12.2.13.	DUV flood expose	10 min
12.2.14.	Develop in SAL101A	60s
12.2.15.	DUV flood expose (If needed)	10 min
12.2.16.	Develop in SAL101A (If needed)	60s
12.2.17.	Inspect pattern; verify resist is cleared and undercut is visible. Alignment tolerance ±200 nm	
12.2.18.	PE2 O2 descum, 300mT, 100W	4 min

12.2.19.	Go directly into Acid (do not get chip wet to verify hydrophilic)	
12.3.	Si-metal contact dep	
12.3.1.	Check this etch rate first!! Dilute BHF:DI 1:4 Dip (etch rate ~20nm/min?)	60s
12.3.2.	E-beam 4, dome fixture	
12.3.3.	Deposit Ni/Ti/Au (30nm/100nm/1000nm)	
12.3.4.	Liftoff in 80C 1165	
13	**Buffer Oxide and Via etch (“SWP5-VIA1” mask)**	
13.1.	**Oxide Dep**	
13.1.1.	Sputter 4 Mike_SiO2_DC program 5833 sec. Gun Angle 5mm	
13.1.4.	Measure oxide thickness with VASE	
13.2.	**Litho (SWP5-VIA1)**	
13.2.1.	Solvent clean	
13.2.2.	Dehydration bake @ 200C – 10 min	
13.2.3.	Use blue tape. Dispense HMDS. Puddle 20s, use recipe 7	
13.2.4.	Replace spinner bowl napkin	
13.2.5.	Spin SPR955 1.8, use recipe 4	
13.2.6.	Remove from tape. Softbake at 110C, 90s	
13.2.7.	Expose in autostep. 0 focus offset.	0.6s
13.2.8.	PEB at 110C	90s
13.2.9.	Develop in AZ726MIF	60s
13.2.10.	PE2 O2 descum, 300mT, 100W	30 s
13.2.11.	Recipe 100: O2 clean, CHF3 coat	5min/1m
13.2.12.	Recipe 101: SiO2 vert etch. Calibrate etch rate if possible. Typically 5min	5 min
13.2.13.	Recipe 103: O2 clean	5min
13.2.13.1.	Inspect visually (will be silvery when SiO2 is gone.)	
13.2.13.2.	Inspect in SEM after you are satisfied to verify SiO2 is gone.	
13.2.14.	Ash PR in ICP1. Recipe 306	20 min
13.2.15.	Strip PR in 80C 1165	10+10
13.2.16.	Careful inspection. If polymer remains, O2 ash in ICP1 for 10min steps until polymer is	
13.2.17.	Inspect alignment: Alignment tolerance ±200 nm to PMESA– use fine align Verniers.	
14	**P-contacts (“SWP5-PMET” mask) (EXPOSE ALL DIES to make liftoff easier)**	
14.1.	**Sample prep**	
14.1.1.	Dehydration bake at 200C	10 min
14.2.	**Litho (SWP5-PMET)**	
14.2.1.	Use blue tape. Spin SF-15, use recipe 5	
14.2.2.	Remove from tape. Bake at 180C (no ramp)	2 min
14.2.3.	Allow chip to cool	1 min
14.2.4.	Use blue tape	
14.2.5.	Spin SPR955-1.8, use recipe 5	
14.2.6.	Softbake at 110C, 90s	
14.2.7.	Expose in autostep. 0 focus offset.	0.56s
14.2.8.	No post exposure bake! Will cause cracks in SF-15	
14.2.9.	Develop in AZ726MIF	40s
14.2.10.	DUV flood expose	10 min
14.2.11.	Develop in SAL101A	60s
14.2.12.	DUV flood expose	
14.2.13.	Develop in SAL101A	60s
14.2.14.	DUV flood expose (if needed)	
14.2.15.	Develop in SAL101A (if needed)	60s
14.2.16.	Inspect pattern; verify resist is cleared and undercut is visible. Alignment tolerance ±100 nm to	
14.2.17.	PE2 O2 descum, 300mT, 100W	4 min
14.2.18.	Go directly into Acid (do not get chip wet to verify hydrophilic)	
14.3.	P-metal contact dep	
14.3.1.	Wet etch in 1:2 HCl:H2O. (45nm/min)	1min
14.3.2.	E-beam 4, dome fixture	
14.3.3.	Deposit Pd/Ti/Pd/Au (10nm/20nm/20nm/1500nm)	
14.3.4.	Liftoff in 80C 1165	
14.4.	**Anneal**	
14.4.1.	USE N2 anneal, not forming gas - Anneal at 350C in the RTA using	**30 s**

15	**Proton implant ("SWP5-HIMPL" mask)**	
15.1.	**Sample prep**	
15.1.1.	Dehydration bake 200 C, 10 min	
15.2.	**Litho (1 layer SF15, 1 layer SPR955CM-1.8)**	
15.2.1.	Use blue tape	
15.2.2.	Dispense SF15 recipe 5	
15.2.3.	Remove from tape	
15.2.4.	Bake 180 C, 2 min	
15.2.5.	Cool 1 min	
15.2.6.	Use blue tape	
15.2.7.	Dispense SPR955-1.8, spin recipe 5	
15.2.8.	Softbake for 90 sec @ 110 C	
15.2.9.	Autostepper expose HIMPL mask 0.56 s, offset 0	
15.2.10.	No post-bake – causes cracks	
15.2.11.	Develop AZ726MIF	40s
15.2.12.	DUV flood exposure: 10 mins;	
15.2.13.	Develop SAL101A: 60 sec	
15.2.14.	DUV exposure: 10 mins	
15.2.15.	Develop SAL101A: 60 sec	
15.2.16.	DUV exposure (if needed): 10 mins	
15.2.17.	Develop SAL101A (if needed): 60 sec	
15.2.18.	Inspect pattern; verify resist is cleared, undercut visible. Save pics. Alignment tolerance ±500	
15.2.19.	PE2 O2 descum 300 mT, 100 W, 30 s	
15.3.	**Ion implant (send out for proton implant) ⇓ see wiki SWEEPER 5A for implant recipe**	
15.4.	**Strip**	
15.4.1.	1165, 80 C – 10+10min	
15.5.	**Inspect**	
16	**Thermo-optic tuners ("SWP5-TOMET" mask) (EXPOSE ALL DIES to make liftoff**	
16.1.	Sample prep	
16.1.1.	Dehydration bake 200 C – 10min	
16.2.	Metal Litho (SWP5-TOMET)	
16.2.1.	Use blue tape. Spin SF-15, use recipe 5	
16.2.2.	Remove from tape. Bake at 180C	2 min
16.2.3.	Allow chip to cool	1 min
16.2.4.	Use blue tape	
16.2.5.	Spin SPR955-1.8, use recipe 5	
16.2.6.	Softbake at 110C, 90s	
16.2.7.	Expose in autostep. 0 focus offset.	0.56s
16.2.8.	No post exposure bake! Will cause cracks in SF-15	
16.2.9.	Develop in AZ726MIF	40s
16.2.10.	DUV flood expose	10 min
16.2.11.	Develop in SAL101A	60s
16.2.12.	DUV flood expose	10 min
16.2.13.	Develop in SAL101A	60s
16.2.14.	DUV flood expose	10 min
16.2.15.	Develop in SAL101A	60s
16.2.16.	Inspect pattern; verify resist is cleared and undercut is visible. Alignment tolerance ±300 nm	
16.2.17.	**Recipe 101: SiO2 vert etch. Calibrate etch rate if possible. Etch 500 nm +/- 200 nm.**	
16.3.	Metal liftoff	
16.3.1.	Ebeam 4 Ti/Pt/Au	
16.3.1.1.	170 A Ti (2 A/s)	
16.3.1.2.	170 A Pt (2 A/s)	
16.3.1.3.	Au 750 A (2 A/s – 200A, 4 – 400A, 5 – 750A)	
16.3.2.	Lift off 1165 80 C	
16.3.3.	Thorough IPA rinse	
16.3.4.	O2 descum 300 mT/100 W, 1 min	
17	**Probe metal ("SWP5-PRMET" mask) (EXPOSE ALL DIES to make liftoff easier)**	
17.1.	**Sample prep**	
17.1.1.	Dehydration bake 200 C, 10 mins	

17.2.	**Litho (PRMET mask)**	
17.2.1.	Use blue tape, spin SF-15 recipe 5	
17.2.2.	Remove tape, bake 180 C 2 mins	
17.2.3.	Cool 1 min	
	Use blue tape, spin SF-15 recipe 5	
	Remove tape, bake 180 C 2 mins	
	Cool 1 min	
17.2.4.	Use blue tape, spin SPR955-1.8, spin recipe 5	
17.2.5.	Soft bake 110 C, 90 s	
17.2.6.	Expose autostep 0 focus offset, 0.56 s	
17.2.7.	No post bake (cracks)	
17.2.8.	Develop AZ726MIF 40 s	
17.2.9.	DUV flood expose 10 mins	
17.2.10.	Develop SAL101A 60 s	
17.2.11.	DUV flood expose 10 mins	
17.2.12.	Develop SAL101A 60 s	
17.2.13.	DUV flood expose 10 mins (If needed)	
17.2.14.	Develop SAL101A 60 s (If needed)	
17.2.15.	Inspect pattern, verify resist cleared, undercut present. Alignment tolerance ±300 nm	
	Dektak Resist pattern	
17.2.16.	PE2 O2 descum, 300 mT, 100 W, 1 min	
17.2.17.	Verify that PR is hydrophilic after descum	
17.3.	**Metal dep**	
17.3.1.	Ebeam 4, standard dome fixture	
17.3.2.	Deposit Ti/Au (20nm/1500nm) (Needs 3000nm Au for Heat Sink process. Do first part with	
17.3.3.	Liftoff in 80C 1165	
18	**Grating open ("SWP5-GO" mask)**	
18.1.	**Sample prep**	
18.1.1.	Solvent clean	
18.1.2.	Dehydration bake @ 200 C 10min	
18.2.	**Litho (SWP5-GO)**	
18.2.1.	Use blue tape. Dispense HMDS. Puddle 20s, use recipe 7	
18.2.2.	Replace spinner bowl napkin	
18.2.3.	Spin SPR955 1.8, use recipe 4	
18.2.4.	Remove from tape. Softbake at 110C, 90s	
18.2.5.	Expose in autostep. 0 focus offset.	0.6s
18.2.6.		
18.2.7.	Develop in AZ726MIF 60s. Inspect: Alignment tolerance ±500 nm	60s
	Bake 120C for 10 min if long BHF is required	
18.2.8.	PE2 O2 descum, 300mT, 100W	30 s
18.3.	**Etch**	
18.3.1.	BHF dip 60 sec. Thorough DI rinse (flowing DI, > 10 minutes)	
18.3.2.	N2 dry, then dehydration bake 10 mins 200 C	
18.3.3.	Strip PR in 80C 1165	20 min
	Careful inspection. If polymer remains, O2 ash in ICP1 for 10min steps until polymer is	
	Dice	
	Do pretesting	
	Polish facets	
	Thin Wafer (after polishing) for lower thermal impedance	
	USE TEST WAFER FIRST	
	Mount sample upside down with crystal wax on Silicon carrier (bigger than sample)	
	Thin to 100um	
	DO NOT REMOVE CRYSTAL WAX	
	Deposit backside metal for soldering: Ti / Ni / Au (20/50/200nm)	
	Mount on carrier	
	Anneal	

Microwave Generator

	Step	Details	Time
		PUT 3 MARKS ON ALL SIDES TO USE FOR EBL ALIGNMENT	
1		**DUV Alignment Marks**	
1.1	Strip	Strip resist in 1165	20+ min
1.2	Piranha clean	3:1 sulfuric/hydrogen peroxide. Use 80C hotplate	10 min
1.3	DUV Mark Litho	Dehydration bake @ 220C	5 min
		Replace spinner bowl wipe	
		Dispense AR2-600, recipe 6, 3500rpm (53 nm from datasheet)	
		Bake AR2 at 220 C	3 min
		Dispense UV6 0.8, spin at recipe 8, 5000rpm, bay 7	
		Softbake on 135C hotplate in bay 7	1min
		Expose in ASML, "MAKE THIS" - CHECK EXPOSURE RATE	30mJ,0.0f
		PEB on 135C hotplate in bay 7	90s
		Develop in AZ300MIF, no agitation - DO NOT DO MORE - This is already 300% develop time	15s
1.4	AR2-600 Etch - RIE #5	Chamber O2 prep - 45 sccm, 50 mT, 300 W (use 1mm cleaning wafer) - recipe DavenP01	5 min
		AR2-600 O2 etch - 20 sccm, 10 mT, 100 W - recipe DavenP02	30s
1.5	Etch	Bosch etcher: Manual mode O2 clean, temp 10C	
		Season with bare Si wafer	5 min
		Allow machine to cool	30 min
		Attach wafer to 5um thermal oxide carrier (get one from Don Freeborn) with 1" of Kapton tape (before looping), use gloves to remove stickiness as much as possible, centered	
		Etch: DAVE_M02. Etch rate ~1.5nm/s, etch 500nm. Complete visually	350sec
1.6	Strip	ICP 1 O2 ash recipe 306 - 450 sccm O2 50PA 900W	20 min
		1165 to strip resist with mild ultrasonic	20+20 min
	Examine	Piranha, 2 baths to strip AR2	5+10 min
2		**Grating**	
		USE 250 uC/cm^2 for first chip and do a dose array btw dies	
		Fix dose for remaining chips if needed	
2.1	Clean	Piranha 3:1 sulfuric/hydrogen peroxide. Use 80C hotplate	10 min
		Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
2.2		BHF dip (until hydrophobic) (use Chongs container)	30 sec
	Lithography		
2.3	Grating EBL Litho	Dehydration bake at 150C	10 min
		Cool wafer	
		Spin CSAR:Anisol 1:1 (thin resist) 30seconds at 3000 rpm (~150nm)	recipe #5
		Bake 180C	4 min
		Spin AquaSave (conducting polymer) 30 seconds at 3000 rpm (~60nm)	
		Bake 15-20 sec at 100C	15 sec
2.4	Ebeam Writing Conditions	" 1209_uW3GratingArr.jdf" write file	
		4th Lens	
		Dose 250uC/cm2	
		3/100kV_500pA	
	Development	DI Rinse 30sec (remove conductive polymer)	30sec
		N2 Dry (be gentle on the gratings)	
		1:1 MIBK:ISO Development - 60s (no agitation) Use a fresh batch (within 5 min)	60sec
		9:1 MIBK:ISO rinse - 20s (DO NOT RINSE WITH DI)	20sec
		N2 Dry	
		PEII descum - 7s - 300mT/100W	7 sec

2.5	Etch	Bosch etcher: Manual mode O2 clean, temp 10C	30 min
		Season with bare Si wafer	5 min
		Allow machine to cool	30 min
		Don't mount on carrier	
		Etch: Sta_E_02. Etch rate ~1.66nm/s, etch between 5 and 10 nm	5 sec
		AFM	
2.6	Strip	ICP 1 recipe 306	20 min
		1165 to strip resist	20+20min
		Piranha	10 min
3		**Waveguide Deep**	
3.1	Strip	Strip resist in 1165	
	Piranha clean	3:1 sulfuric/hydrogen peroxide. Use 80C/140C hotplate	10 min
3.2	Lithography	Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
3.3	uW-WGD Litho	Dehydration bake @ 220C	5 min
		Replace spinner bowl wipe	
		Dispense AR2-600, recipe 6, 3500rpm (53 nm from datasheet)	
		Bake AR2 at 220 C	3 min
		Dispense UV6 0.8, spin at recipe 8, 5000rpm, bay 7	
		Softbake on 135C hotplate in bay 7	1min
		Expose in ASML, "uWExpose3" - CHECK EXPOSURE RATE	17mJ,0.0f
		PEB on 135C hotplate in bay 7	90s
		Develop in AZ300MIF, no agitation - DO NOT DO MORE - This is already 300% develop time	15s
	REFLOW	Bake 140 C for 3 min	3 min
3.4	AR2-600 Etch - RIE #5	Chamber O2 prep - 45 sccm, 50 mT, 300 W (use 1mm cleaning wafer) - recipe Daven_P01	5 min
		AR2-600 O2 etch - 20 sccm, 10 mT, 100 W - recipe Daven_P02	30s
	Etch	Bosch etcher: Manual mode O2 clean, temp 10C	
		Season with bare Si wafer	5 min
		Allow machine to cool	30 min
		Attach wafer to 5um thermal oxide carrier (get one from Don Freeborn) with 1" of Kapton tape (before looping), use gloves to remove stickiness as much as possible, centered	
		Etch: DAVE_M02. Etch rate ~1.5nm/s, etch 500nm. Complete visually	5' 50"
3.5	Strip	1165 to strip resist	20+20min
		Piranha, 2 baths to strip AR2	5+10 min
4		**Waveguide Shallow**	
4.1	Strip	Strip resist in 1165	
	Piranha clean	3:1 sulfuric/hydrogen peroxide. Use 80C hotplate	10 min
4.2	Lithography	Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
4.3	uW-WGD Litho	Dehydration bake @ 220C	5 min
		Replace spinner bowl wipe	
		Dispense AR2-600, recipe 6, 3500rpm (53 nm from datasheet)	
		Bake AR2 at 220 C	3 min
		Dispense UV6 0.7, spin at recipe 8, 5000rpm, left spinner, bay 7	
		Softbake on 135C hotplate in bay 7	1min
		Expose in ASML, "uWExpose" - CHECK EXPOSURE RATE	17mJ,0.0f
		PEB on 135C hotplate in bay 7	90s
		Develop in AZ300MIF, no agitation - DO NOT DO MORE - This is already 300% develop time	15s
	REFLOW	Bake 140 C for 3 min	3 min
4.4	AR2-600 Etch - RIE #5	Chamber O2 prep - 45 sccm, 50 mT, 300 W (use 1mm cleaning wafer) - recipe Daven_P01	5 min

		AR2-600 O2 etch - 20 sccm, 10 mT, 100 W - recipe Daven_P02	30s
	Etch	Bosch etcher: Manual mode O2 clean, temp 10C	30 min
		Allow machine to cool	30 min
		Season with bare Si wafer	5 min
		Don't mount on carrier	
		Etch: Sta_E_02. Etch rate ~1.66nm/s, etch 200nm. Chong1	120 sec
4.5	Strip	1165 to strip resist	20+20min
		Piranha, 2 baths to strip AR2	5+10 min
4.4	Strip	1165 to strip resist	20+20min
		Piranha	10 min
5		**Bonding**	
	InP prep:	Spin 1.8um resist on wafers with NO HMDS	
	CLEAVE	Cleave in precision cleaver	
	Gain Epi	Epi F = 8.5mm wide X 17 mm tall	
	Mod Epi	Chong's epi = 4mm wide x 17 mm tall	
	PD Epi	Aurrion PIN = 4.5 mm wide x 17 mm tall	
	NOTE: DO NOT HF CLEAN THE SILICON WAFER or you will undercut your waveguides		
5.1	Silicon: Piranha clean	3:1 sulfuric/hydrogen peroxide. Use 80C hotplate. Top off H2O2 after 10 min	20 min
5.2	Silicon: Iso clean	*ONLY IF NECESSARY* swab or spin/spray (depending on particle size) with iso, DI rinse until clean under 10X	
5.3	GAIN, MOD, PD InP: PR strip	Soak or spin/spray 1165 then DI to remove cleaving PR. Take off spinner before N2-dry	
5.4	GAIN, MOD, PD InP: Post PR strip Iso clean	*ONLY IF NECESSARY* Swab or spin/spray with iso, DI rinse until clean under 10X	
5.5	PD: Cap removal	H3PO4:H2O2:H2O 1:1:38; DI rinse	5min
5.6	PD: Post cap removal Iso clean	*ONLY IF NECESSARY* Swab or spin/spray with iso, DI rinse until clean under 10X	
5.7	Plasma activation	Plasma activation on Si, III-V chips. Run Dis0.2mBar (EVG tool)	~20 min
5.8	Spontaneous bonding	Stick together. place major flat perpendicular to waveguides.	
		Use offset piece on bonder. Move bonder head so it doesn't align with the edge of the epi perfectly or the head might touch the other epi	
		Lay down GAIN epi first with left side of die facing the bonder (angle of rotation on the shortest axis)	
		Flip SOI 180deg and lay down MOD epi and then PD epi.	
5.9	Anneal	Clamp in bonding fixture with graphite compressor sheet. Anneal at 300C	2hrs
	MEASURE EPI HEIGHT	MEASURE EPI HEIGHT	
	ACE/ISO/DI		
	Dehydration bake	110C	5 min
5.10		Deposit 1000nm unaxis(50C) Barton oxide	
5.11		Place crystal bond around and in between dies. To create thin pieces for in between dies place crystal bond on aluminum foil and lift 1-2 inches, allow to harden, and snap off	
		Use wooden sticks to push into sides. Crystal bond on top of dies is OK as long as the center is sufficiently clear to measure height for leveling	
5.12	Substrate thin	Polish to 75 um remaining	
5.13	Wet substrate removal	Etch in 3:1 HCL/DI until film looks smooth ~ 4um/min	

5.14	Strip crystalbond	Place on spinner chuck but don't spin and ACE/ISO/DI. Spray with no spin - ACE/Crystalbond is bad for glassware	
		MAY NEED TO REPEAT RAZOR SHAVING MULTIPLE TIMES	
5.15	PR coat	SF-11	
5.16	Mountain removal	Use razor blade to shave mountains	
5.17	Bake away bubbles	Bake at 200C	30 sec
5.18	PR strip/clean	1165 to strip PR. Swab in tergitol to remove starry night, soak in ACE/ISO/DI, use darkfield with max lamp power and aperture to ensure chip is clean. Use PEII 30 sec 300mT/100W to remove tergitol scum	
6		**Pre-Pmetal**	
6.1	Solvent clean	Should be clean	3/3/1min
6.1.5	InGaAs etch stop removal	Etch in 1:1:38 H3PO4:H2O2:DI 5 mins to remove etch stop	5 min
6.2	Thin P metal litho	Dehydration bake at 150C	5 min
		Spin SF-11, use recipe 5	
		Clean backside before bakes	
		Ramp from 90C to 130C, hold 30s, ramp to 155C, hold 30s, ramp to 180C, no hold ramp to 200 C. hold 2 min on the "IKA Ret" hotplate in bay 6. Start timer at >197C	2 min
		Allow chip to cool	1 min
		Spin SPR955-1.8, use recipe 5. Clean back side.	
		Softbake at 110C	90s
		Expose in autostep. 0 focus offset.	0.56s
		No post exposure bake! Will cause cracks in SF-11	
		Develop in AZ726MIF. Continue in 10s steps until patterns are clear.	2 min +
		Inspect	
6.3	P-sac layer etch (20nm)	PE2 O2 descum, 300mT, 100W	4 min
		Go directly into acid (do not get chip wet to verify hydrophilic)	
		Wet etch in 1:2 HCl:H2O. (45nm/min). Do this right before Ebeam 4.	1min
6.4	Thin P-metal	E-beam 4, dome fixture	
		Check shutters, replace if there is any sign of flaking or if it is later in the week than Thursday.	
		Deposit Pd/Ti/Pd/Au/Ti (3nm/17nm/17nm/200nm/30nm)	
		Liftoff in 80C 1165, ISO, DI	75+10min
7		**P-Mesa Etch**	
7.1	Liftoff P mesa litho	Dehydration bake @150C	8min
		Dispense SF-11, spin at recipe 7 (~600nm)	
		Clean backside and edges with ebr, swab	
		Bake SF-11 at 200C	2min
		spin uv6, recipe 5	
		clean backside	
		Bake 135C	1min
		Expose in DUV, bleh	12mJ, 0.2F
		PEB 135C	90s
		develop in 300mif until clear	2min 20 sec
		Check on long tapers (modulators) to verify good exposure	
		Deposit SiO2 in EBeam 2. 1-3A/s, deposit 300nm+	
		Liftoff in 1165	
7.2	Dicing	Coat in SPR 220-7 recipe 5, bake 3 min at 95C	
		Dice	
		Strip in 1165, 80C, 2 baths	10+10min
7.3	P Mesa Etch	Clean. 20 sccm O2, 125 mT, 500 V	30 min
		Precoat. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V	20 min
		~33 min, use laser monitor. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V. Stop 1/2 period after period change.	~33 min
		Descum (chip remains in chamber). O2, 20 sccm, 125 mT, 300V	10 min

8		**Mesa Fill Hardmask Etch**	
8.1	clean	1165/iso/di soak with chips vertical, only if necessary	3/3/1min
	litho	Dehydration bake @ 150C	8 min
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		Bake at 125C	3 min
		SPR 220-7, recipe 5	
		Remove from tape	
		Softbake at 110C	90s
		exp	1.5 s
		WAIT 60 MIN BEFORE POST EXP BAKE	
		PEB at 110C	90s
		Develop in AZ726MIF until clear	~90s
		PEII 30s descum 300mT 100W	30s
		Reflow, at 115C	5 min
8.2	Oxide HM etch	BHF , 200nm/min? (should be larger than 300 nm/min). Update 02/11: 290nm oxide was all gone after 20 s in BHF (Si test piece)	2min
		Strip in 1165	30+30min
9		**Quantum Well Etch**	
9.1	QW litho	If necessary: 1165/iso/di 3/3/1min, then 4x dump rinse	
		Dehydration bake @ 150C	8 min
		Dispense HMDS. Puddle 20s, use recipe 7	
		Replace spinner bowl napkin	
		Bake off HMDS, 125C hot plate	3 min
		Use blue tape	
		Spin SPR955 1.8, use recipe 4	
		Remove from tape	
		Soft bake at 110C	90s
		Expose in autostep. 0 focus offset.	0.6s
		PEB at 110C	90s
		Develop in AZ726MIF, agitation	60s
		PE2 O2 descum, 300mT, 100W	30s
9.2	QW etch	Wet etch in H2O/H2O2/H3PO4 15/5/1. Watch carefully, etch time varies. Go for 10s after color change is complete. Need to undercut by 700 nm - use LEXT to see undercut on nsac layer pads	~50 sec
		Strip PR in 80C 1165; use 2nd bath after 10min	10+10min
		If photoresist remains, do 30s PE2 descum	
10		**N- Metal**	
10.1	Solvent clean	If necessary, do solvent clean. Shouldn't be.	3/3/1min
10.2	N metal litho	Dehydration bake at 150C	10 min
		Use blue tape	
		Spin SF-15, use recipe 5	
		Remove from tape	
		Must do to remove PMGI bubbles – Inspect entire chip has no bubbles -Ramp from 90C to 130C, hold 30s, ramp to 155C, hold 30s, ramp to 180C, then ramp to 200Chold 2 min on the "IKA Ret" hotplate in bay 6	
		Allow chip to cool	1 min
		Use blue tape	
		Spin SPR955-1.8, use recipe 5	
		Softbake at 90C	90s
		Expose in autostep. 0 focus offset.	0.56s
		No post exposure bake! Will cause cracks in SF-15	
		Develop in AZ726MIF	40s
	Around 4 repeats	DUV flood expose	10 min
		Develop in SAL101A	60s
		DUV flood expose	10min
		Develop in SAL101A	60s

		Inspect pattern; verify resist is cleared and undercut is visible. Save microscope image of mesa for comparison after etch.	
10.3	N-sac layer etch	PE2 O2 descum, 300mT, 100W	4 min
		Go directly into acid (do not get chip wet to verify hydrophilic)	
		Wet etch in H2O/H2O2/H3PO4 15/5/1. (at least as long as QW etch)	40s
		Inspect entire III-V area in microscope to ensure etch was successful. Etched region should be pink, VCs in contacts clearly visible	
10.4	N-metal deposition	E-beam 4, standard dome fixture	
		Deposit Pd/Ge/Pd/Au/Ti, 10nm/110nm/25nm/1000nm/25nm	
		Liftoff in 80C 1165	
11		**N-InP etch**	
11.1	Solvent clean	1165/iso/di soak with chips vertical, only if necessary	3/3/1min
11.2	N-InP litho	If necessary: 1165/iso/di 3/3/1min, then 4x dump rinse	
		Dehydration bake @ 150C	8 min
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		bake off hmds 125C	3 min
		Replace spinner bowl napkin	
		Spin SPR955 1.8, use recipe 4	
		Remove from tape	
		Softbake at 100C	90s
		The 500nm taper tip here may actually cause some reflection - it would be worth it to try increasing this to 0.9 sec exposure or more. SEM your lookahead after the o2 ash here and see if that tip can be minimized.	
		N Mesa Mask	.9s
		PEB at 110C	90s
		Develop 726	60s
		Hard bake at 135C	5 min
		O2 ash, PE2, 300mT/100W	60s
11.3	N-InP etch	Clean. 20 sccm O2, 125 mT, 500 V	30 min
		Precoat. CH4/H/Ar, 4/20/10 sccm, 75 mT, 500 V	20 min
		Use laser monitor. CH4/H/Ar, 4/20/10 sccm, 75 mT, 200 V. 20% overetch, ~3 minutes after trace goes flat TWO HUNDRED VOLTS	~17 min
		Descum. 20 sccm O2, 125 mT, 300 V	10 min
11.4	Strip	Ash in recipe 306 in ICP1	40 min
		Strip in 80C 1165	20+20 min
12		**Mesa Fill Etch**	
12.1	clean	1165/iso/di soak with chips vertical, only if necessary	3/3/1min
12.2	litho	Dehydration bake @ 150C	8 min
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		Bake at 125C	3 min
		SPR 220-7, recipe 5	
		Remove from tape	
		Softbake at 110C	90s
		exp	1.5 s
		WAIT 60 MIN BEFORE POST EXP BAKE	
		PEB at 110C	90s
		Develop in AZ726MIF until clear	~75s
		PEII 30s descum 300mT 100W	30 s
		Reflow, at 135C	3min
12.3	InP etch (50nm) :	H3PO4:HCl:DI = 1:1:1, ~80nm/min	2min
12.4	InGaAs etch (100nm):	H3PO4:H2O2:DI=1:5:15	2min
12.5	InP etch (1500nm):	H3PO4:HCl=3:1, ~600nm/min (you should see bubbles coming off from	7 + 1 min

		the Epi)	repeats until finished
12.6		DEKTAK to make sure the P-cladding is finished etching	
12.7	Active etch (350nm):	H3PO4:H2O2:DI=1:5:15	2min
		Check for pink color and vertical channels (check all the epi, under microscope))	
12.8	InP etch (110nm):	H3PO4:HCl:DI = 1:1:1, ~80nm/min Bubbles	2min
12.9	InGaAsP etch (7.5nm):	H2SO4:H2O2:DI=1:1:10, after cool for 10 min, ~60nm/min	30sec
12.10	InP etch (7.5nm):	H3PO4:HCl:DI = 1:1:1, ~80nm/min	30sec
12.11	InGaAsP etch (7.5nm):	H2SO4:H2O2:DI=1:1:10, after cool, ~60nm/min	30sec
12.12	InP etch (17.5nm):	H3PO4:HCl:DI = 1:1:1, ~80nm/min	30sec
		Repeat last two steps if needed until finished	
		1165 strip 30+30 min as needed	
13		**P mesa hardmask cleanup**	
13.1	P HM cleanup litho	Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
	use via mask	Dehydration bake @ 150C	5 min
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		Replace spinner bowl napkin	
		Spin SPR955 1.8, use recipe 4	
		Remove from tape	
		Softbake at 110C	90s
	via mask	Expose in autostep. -1 focus offset.	0.6s
		PEB at 110C	90s
		Develop in AZ726MIF	60s
		PE2 O2 descum, 300mT, 100W	2 min
13.2	P-mesa HM etch	BHF until hydrophobic	15 sec
		Inspect carefully to ensure SiO2 is removed. Recommend SEM. Also ensure scum is removed in nvia	
13.3	PR strip	Strip in 80C 1165.	10+10min
14		**Via**	
14.0	Oxide Deposition	Sputter 3: Mike_low_r; target 900nm, ~4.47nm/min	Run at 4/44 - 3 1/2 hrs
		USE DUMMY TO CHECK THICKNESS	
14.1	Via litho	Clean should not be needed	
		Dehydration bake should not be needed if clean was skipped	
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		Replace spinner bowl napkin	
		Spin SPR 220-3, recipe 3	
		Remove from tape	
		Softbake at 110C	90s
		Expose in autostep. -20 focus offset. (under-exposed on purpose to shrink down taper length)	0.45s
		PEB at 110C	90s
		Develop in AZ726MIF	60s
		PE2 O2 descum, 300mT, 100W	30 s
14.2	Via etch-ICP2	Recipe 105: O2 clean, CF4 coat	5min/1min
		Recipe 181: GC_SiN (50nm/min), clear visually	~18 min
		Recipe 103: O2 clean (not required, run if there is time)	5min
		SEM via in JEOL before strip (if it doesn't work then do it after the strip and you can blanket etch a little bit)	
		Ash PR in ICP1. Recipe 306 (Do this if possible but it's ok to skip if you can't get a slot. Then do wet strip and 1 min in PEII)	20 min

		Strip PR in 80C 1165	20+60min
		Careful inspection. If polymer remains, O2 ash in ICP1 for 10min steps until polymer is removed	
		Possibly do light swab in ISO if still has stringers	
15		**P-Metal**	
15.1	Solvent clean	Should be clean from via process	3/3/1min
15.2	P metal litho	Dehydration bake at 150C	8 min
		Use blue tape	
		Spin SF-15, use recipe 5	
		Remove from tape	
		Bake at 200C	2 min
		Allow chip to cool	1 min
		Use blue tape	
		Spin SPR955-1.8, use recipe 5	
		Softbake at 110C	90s
		Expose in autostep. 0 focus offset.	0.56s
		No post exposure bake! Will cause cracks in SF-15	
		Develop in AZ726MIF. Continue in 10s steps until patterns are clear.	2 min +
		PE2 O2 descum, 300mT, 100W	30 sec
15.3	P-metal	E-beam 4, dome fixture	
		Check shutters, replace if there is any sign of flaking or if it is later in the week than Thursday.	
		Deposit Pd/Ti/Pd/Au (3nm/17nm/17nm/1500nm)	
		Liftoff in 80C 1165, ISO, DI	75+5min
		Pre anneal TLM contact resistivity (did on gain epi)	
15.4	Anneal	Anneal at 350C in the RTA using \Bowers\Siddharth\350_30s_1N	
16		**Implant**	
16.1	Solvent clean	Should be clean, only do if necessary (1165/Iso/DI)	3/3/1min
16.2	Implant litho	Dehydration bake at 150C	8 min
		Use blue tape	
		Spin SF-15, use recipe 5	
		Remove from tape	
		Bake at 200C	2 min
		Allow chip to cool	1 min
		Use blue tape	
		Spin SPR955-1.8, use recipe 5	
		Softbake at 110C	90s
		Expose in autostep. 0 focus offset.	0.56s
		No post exposure bake! Will cause cracks in SF-15	
		Develop in AZ726MIF	50s
	Repeat as needed	DUV flood expose	10 min
	3X should work	Develop in SAL101A	60s
16.3	Implant	Send out to implant	
16.4	PR strip	Strip PR in 80C 1165. 2 baths	60+5min
17		**Isolation Etch**	
17.1	Isolaton litho	Microscope inspect. Cleaning should not be necessary. Do solvent clean if chip is dirty	
		Dehydration bake @ 150C	8 min
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		Bake off, 110C	1 min
		Replace spinner bowl napkin	
		Spin SPR955 1.8, use recipe 4	
		Remove from tape	
		Softbake at 110C	90s
		Expose in autostep. -20 focus offset.	1.2s

		PEB at 110C	90s
		Develop in AZ726MIF	60s
		PE2 O2 descum, 300mT, 100W	2 min
17.2	Isolation etch	Remove p-sac layer with wet etch in 1:2 HCl:H2O. (45nm/min) Thickness 50 nm for Gain/Mod, 20 nm for PD	1min
		Wet etch 200nm in H2O/H2O2/H3PO4 15/5/1. Attempt before/after laser uscope or dektak. 200nm of InGaAs should take only 30s or less. Thickness 100 nm for Gain/Mod, (200 nm for PD but there is no isolation section there)	20s for 100 nm
		Strip PR in 80C 1165	10+10min
18		**Heater**	
18.1	Solvent clean		
18.2	Heater litho	Dehydration bake at 200C	5 min
		Use blue tape	
		Spin SF-11, use recipe 5	
		Remove from tape	
		Bake at 200C	2 min
		Allow chip to cool	1 min
		Use blue tape	
		Spin SPR955-1.8, use recipe 5	
		Softbake at 110C	90s
		Expose in autostep. 0 focus offset.	0.56s
		No post exposure bake! Will cause cracks in SF-11	
		Develop in AZ726MIF	120s
		Inspect pattern; verify resist is cleared and undercut is visible.	
		PE2 O2 descum, 300mT, 100W	30s
18.3	Heater metal	Ebeam 4 - NEED 4 HOUR SLOT	
		Deposit Ti/Pt 10nm/100nm	
		Liftoff in 1165 at 80C - switch baths after metal falls off	45+10min
19		**BCB**	
	PREP	Take out small BCB bottle from freezer and warm up overnight	
19.1	Solvent clean	Should be clean, only do if necessary (1165/Iso/DI)	3/3/1min
19.2	Adhesion treatment	Deposit 180nm PECVD SiN for good adhesion of BCB. Sputter 3 - Mike 10W SiN - 4/44 angle/height	
		Place sample in PEII at 100W, 300mT for 20s	
		Dip HCl:DI 1:10 for 60s, Rinse in DI 60s, Blow Dry	
		Apply AP3000 BCB Adhesion promoter, wait 30sec, and then spin recipe 5 for 30sec	3000 for 30sec
19.3	Litho	Spin BCB (step1:500rpm-400rpm/s-10sec ; step2:6000rpm-1000rpm/s-30sec)	6000 for 30sec
		Soft Bake 80C for 90sec	90 sec
		Expose 2.2" in Autostep200 with focus 0	2.2 sec
		PEB 55C for 30sec	30 sec
19.4	Develop	Immediately do puddle development using POLOS spinner program "7" (step1: 500rpm-10sec; step2:4000rpm-400rpm/s-60sec)	
		a. Apply DS2100 BCB developer on quarter, wait 60sec, then run program "7"	
		b. While it is spinning @500rpm/10sec gently apply DS2100 (drop by drop in the center of the quarter)-Rinsing step (first part of recipe 7 described above)	
		c. Spin dry at 4000rpm/60sec (second part of recipe 7)	
		d. Repeat steps 10(a-c) one or two more times until development is complete.	
		Bake@90C/60sec to further dry out DS2100	
19.5	Measure	Measure with dektak before curing	
19.6	Final Cure	Final Cure in BLUE M Oven:	
		a. Program#5	
		b. Purge oven with N2(for 1/2hr)before loading sample for curing	

		c. Edit the program	
		d. ramp up to 50C-5min(time in program is 0.05 for 5min)	5 min
		e. soak@50C-5min	
		f. ramp up to 100C-15min(time in program is 0.15 for 15min)	15 min
		g. soak@100C 15min	15 min
		h. ramp up to 150C-15min	15 min
		i. soak@150C-15min	15 min
		j. ramp up to 250C-1hour(time in program is 1.00 for 1hour)	1 hr
		k. soak@250C-1hour	1 hr
		l. Load sample in oven (using Al boat or on bottom tray directly), DO NOT cover it. Make sure the aluminum is bent in a little so the sample doesn't fall off.	
		m. Close the door, leave a note that BCB is baking!	
		n. Make sure N2 in ON(60-70)	
		o. Run the program(P5, run)	
		p. Wait few minutes to check if it is running and if T is going UP!	
		q. CURING takes 4hours	
		r. COOLING DOWN takes several hours (overnight is good)	btw 2-4 hours
		s. DO NOT OPEN door while it is cooling down! OK to open at 150C.	
19.7	Measure	DEKTAK	
19.8	Descum	Etch back BCB 0.5-1 um in ICP #1 recipe 308 using 40 O2 /10 CF4 (~300-390nm/min) to remove scum layer and improve adhesion. 100 nm should be left.	
		DEKTAK	
19.9	Adhesion	Deposit 180nm SiN on BCB for metal adhesion (MIKE 10W 5600 sec)	
		NO MORE 1165!!! IT causes swelling in BCB.	
20		**Nitride Etch**	
20.1	BCB NItride Via litho	Clean should not be needed	
		Dehydration bake should not be needed if clean was skipped	
		Use blue tape	
		Dispense HMDS. Puddle 20s, use recipe 7	
		Replace spinner bowl napkin	
		Spin SPR 220-3, recipe 3	
		Remove from tape	
		Softbake at 110C	90s
		Expose in autostep with VIA MASK. 0 focus	0.56s
		Expose in autostep with HEATER MASK. 0 focus offset. (under-exposed on purpose to shrink down taper length)	0.6s
		PEB at 110C	90s
		Develop in AZ726MIF	60s
		PE2 O2 descum, 300mT, 100W	30 s
		Use enough oil to coat at least 3/4 the chip when pressed down or the resist will burn	
20.2	BCB nitride Via etch-ICP2	Recipe 105: O2 clean, CF4 coat	5min/1min
		Recipe : SiOxvert (320-340nm/min), clear visually (20% over etch)	90 sec
		Recipe 103: O2 clean (not required, run if there is time)	5min
		Ash PR in ICP1. Recipe 306	20 min
		Strip PR in ACETONE	20+60min as needed
		Careful inspection. If polymer remains, O2 ash in ICP1 for 10min steps until polymer is removed	10 min
21		**Probe Metal**	
21.1	Solvent clean	Should be clean, only do if necessary (ACE/Iso/DI)	3/3/1min
		Gasonics, 200C	90 sec

21.2	Probe metal litho	Dehydration bake at 150C	5 min
		Use blue tape	
		Spin SF-15, use recipe 5	
		Remove from tape	
		Bake at 200C	2 min
		Allow chip to cool on metal bench	1 min
		Use blue tape	
		Spin SPR955-1.8, use recipe 5	
		Softbake at 110C	90s
		Expose in autostep. 0 focus offset. Try 1 sec to fix buildup of resist in PD area	0.56
		No post exposure bake! Will cause cracks in SF-15	
		Develop in AZ726MIF - 1 min AZ726	1 min
		4X DUV Flood expose with 60s SAL101 develop. (Prob clear after 3X)	10 min flood + 1 min dev
		Inspect pattern. Verify resist is clear, undercut should be >2um	
		Develop in 10s steps until undercut is sufficient	
		PE2 O2 Descum, 300mT, 100W,	1 min
21.3	P-Probe metal	E-beam 4, "regular" PLANETARY ROTATION	
		Deposit Ti/Au (23nm/1500nm)	
		Liftoff in ACETONE!!! Goes quickly with pipette.	45+0 min
		AZ726MIF developer : After liftoff the PMGI will still be there.	5 min
		Make sure PMGI is gone. Do 1 min extra develop if needed	
21.4	Dicing	Dispense HMDS. Puddle 20s, use recipe 7	
		Spin SPR220-3um, use recipe 5	
		Softbake at 110C	90s
		Dice and polish	