Title

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***Abstract*—This paper presents a regulating Hybrid Switched Capacitor Converter (HSCC) topology suitable for high conversion ratio Point-of-Load (PoL) applications, specifically targeting 48 V to 1 V power delivery in space-based high-performance computing systems, where size and weight are important considerations, along with device de-rating for radiation tolerance. The proposed topology merges an initial 2:1 switched capacitor conversion stage with a recently developed symmetric dual inductor hybrid (SDIH) conversion stage, reaping benefits of both. The SDIH stage offers reduced component count and an excellent switch stress figure of merit, while the initial 2:1 voltage reduction stage significantly reduces the volume of flying capacitors, enabling compact size and low weight. A high density gate drive solution is also presented, using a minimal number of driver ICs without compromising on driving capability. A preliminary hardware prototype demonstrates this topology's feasibility while employing de-rated gallium nitride (GaN) switches to safeguard against radiation total ionizing dose (TID) and single event effects (SEE). This prototype achieves a very high measured power density of 2,020 W/inch^3 (123.3 kW/liter) while performing 48 V to 1 V conversion and switching at 1 MHz.**

I. Introduction

Hybrid switched capacitor converters (HSCCs) have demonstrated high performance in regulating 48 V to point-of-load (PoL) applications (e.g., [1]–[4]), owing to both their reduced total switch stress and required passive component volume [5]–[7]. The reduced switching device voltage stress in these converter topologies makes them particularly applicable to high density and light weight space applications which additionally require immunity to radiation effects such as total ionizing dose (TID) and single event effects (SEE). Here, devices must typically be de-rated well below their terrestrial limits, motivating the use of multi-level and higher order HSCCs [8]. Assisting this effort, gallium nitride (GaN) switching devices offer inherent radiation hardness and peak figures of merit in the tens to hundreds of volts [5], [9]–[11], further motivating the use of GaN-based HSCCs in future spacecraft and satellite power delivery systems. While HSCCs have received significant development for use in terrestrial data centers, this work proposes a direct 48 V to 1 V HSCC topology (Fig. 1) that is also suitable for high performance computing in space. The remainder of this manuscript is organized as follows: Section II describes operation of the proposed topology and motivates its merged two-stage structure.

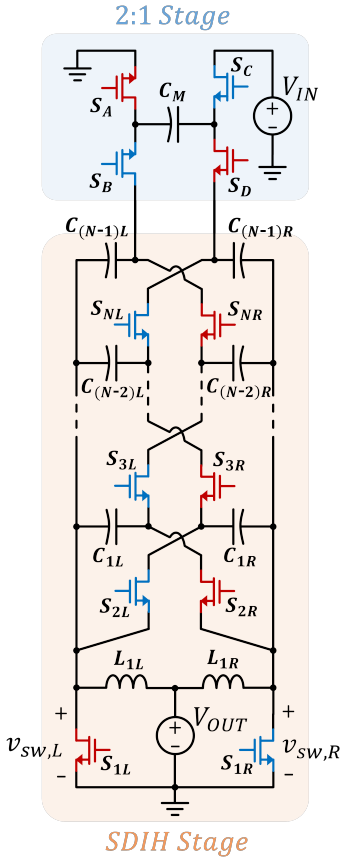
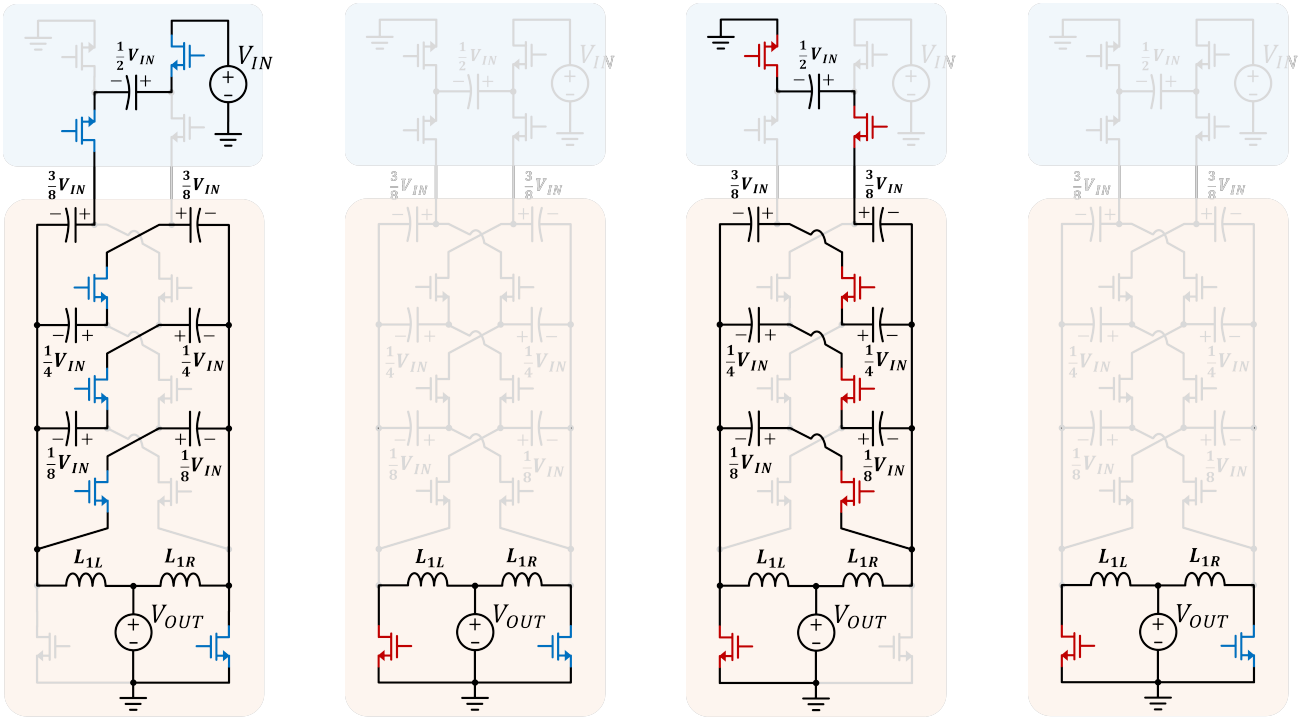


Fig. 1: Proposed power converter topology, comprising an initial 2:1 switched-capacitor stage that is fully soft-charged [12] by a subsequent merged symmetric dual inductor hybrid (SDIH) Dickson-type converter [13].

Section III presents a first hardware prototype validating the proposed structure, in addition to a compact gate drive scheme for practical implementation. Section IV concludes this work.

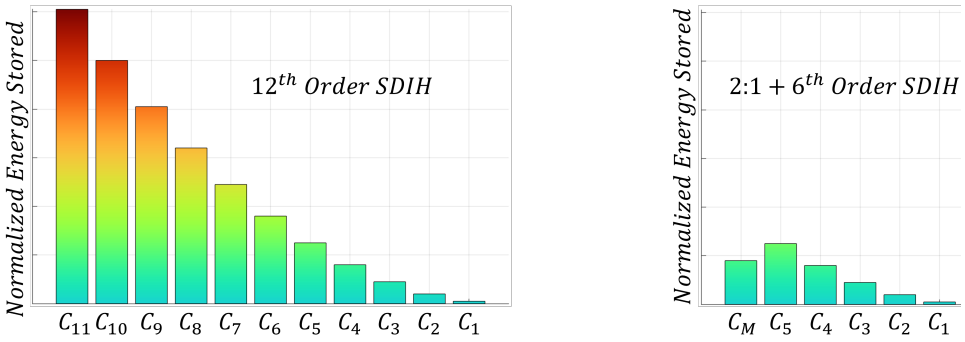
II. Proposed HSCC Topology

The proposed HSCC topology depicted in Fig. 1 comprises an initial 2:1 switched capacitor conversion stage which is merged with the recently developed symmetric dual inductor hybrid (SDIH) topology [13]; the latter being a variation on the series capacitor buck (SCB) converter [17] but with far fewer components. This merging of stages is seamlessly facilitated



(a) Phase 1 (b) Phase 2 (c) Phase 3 (d) Phase 4

Fig. 2: Simplified phase progression of the proposed topology, using a merged 4th order second-stage SDIH as an example (the hardware prototype discussed in Section III uses an increased 6th order SDIH stage). Primary phases 1 and 3 are interleaved with regulating phases 2 and 4 whose duration may be varied to effect PWM regulation. Switches experience reduced voltage stress and the output inductors are interleaved by 180°, facilitating effective use of coupled inductors for reduced size and improved transient response [14]–[16].



(a) (b)

Fig. 3: Comparison of stored flying capacitor energy in two 12:1 switched capacitor solutions. (a) A 12th order single stage SDIH converter [13], (b) the proposed two stage solution leveraging an initial 2:1 reduction followed by a 6th order merged SDIH stage. Capacitor C_X denotes the combined energy stored by both C_{XL} and C_{XR} within the SDIH stage. All capacitors are assumed equal (Farads). Solution (b) provides 7× reduction in required capacitor energy storage.

by the SDIH converter's inherent dual interleaved high-side port that can draw charge off of the 2:1 stage's flying capacitor C_M in an alternating fashion — while simultaneously removing two redundant switches. This phase progression is depicted in Fig. 2, where added free-wheeling phases 2 and 4 facilitate phase-shifted-modulation (PWM) voltage regulation. Provided that all flying capacitors are sized equally, this merging of stages has the added benefit of removing all requirements for split-phase switching[1], with the exception of the lowermost capacitor branch in both phase 1 and phase 3. Alternatively, if capacitor voltage ripple is assumed to be small, split-phase switching may be neglected as is done in Fig. 2 for simplicity.

As a Dickson-type structure [19], the SDIH stage expresses best-in-class switch stress FOM [6], [7], [20], [21], with each switch within the SDIH stage subjected to a maximum

[1]Split-phase switching [18] is a more complex clocking scheme that is required by the SDIH topology to ensure complete soft-charging of all flying capacitors. This in turn facilitates increased voltage ripple and reduced passive size. Thus the proposed structure's simplification is note-worthy.

blocking voltage of V_{IN}/N, where N defines the SDIH order as annotated in Fig. 1. This translates to smaller switches for equivalent performance. Despite this advantage, Dickson converters typically fare worse with respect to passive component volume as compromise. Fig. 3(a) depicts the normalized energy stored in each flying capacitor of an example 12th order SDIH converter, where energy $\left(\frac{1}{2}CV^2\right)$ is largely proportional to capacitor volume [22]. Here, capacitors C_{11L} and C_{11R} must be rated at $\frac{11}{12} \times V_{IN}$ and store the largest amount of energy, growing with the square of rated voltage.

In contrast, by applying an initial 2:1 stage (proposed), only a subsequent 6th order SDIH stage is required for the same overall conversion ratio, greatly reducing total part count. Moreover, due to the initial halving in voltage, capacitor C_M need only be rated for $\frac{1}{2}V_{IN}$, while capacitors C_{5L} and C_{5R} are rated at $\frac{5}{12}V_{IN}$. This results in a 7× reduction in total capacitor volume (Fig. 3(b)), assuming a continuum of available component ratings. This passive volume reduction comes in exchange for a somewhat worsened overall switch stress, since switches S_A, S_B, S_C and S_D must be rated for an increased voltage of $V_{IN}/2$, however, this compromise has generally been deemed favorable in a growing number of recent practical hardware demonstrations [3], [4], [23]–[28] and is facilitated in this application due to the availability of high performance 100 V GaN devices.

III. Hardware Prototype

A preliminary hardware prototype was constructed on a 0.9 mm thick PCB using a 6-layer stackup of 2 oz. copper metalization. Fig. 4 presents a schematic of the primary power stage which includes a 6th order SDIH to produce two interleaved switched node waveforms, $v_{sw,L}$ and $v_{sw,R}$, each with an average amplitude of 4 V $(= 48\,\text{V}/2/6)$, as illustrated in the experimentally captured waveforms of Fig. 5. The relative duration of phases 2 and 4 is modulated to provide output voltage regulation to 1 V, irrespective of load. Since the SDIH can operate with a maximum duty cycle of 50% (phases 2 and 4 reducing to zero duration), the maximum average voltage on $v_{sw,X}$ is 2 V, which leads to a symmetric upward and downwards slew rate during transient events; $L\frac{di}{dt} = (2V - 1V)$ and $L\frac{di}{dt} = (0V - 1V)$, respectively. The inherent 180° interleaving of $v_{sw,L}$ and $v_{sw,R}$ effectively accommodates the use of coupled inductors which provide improved ripple cancellation [14]–[16].

Fig. 4 also depicts the primary gate drivers and associated power delivery circuitry. Drivers U_1, U_2 and U_8 are ground referenced low-side drivers, whereas high-side drivers U_3, U_4, U_5, U_6 and U_7 leverage level-shifting circuitry integrated within a commercial half-bridge driver. Drivers U_3, U_4, U_5, U_6 and U_7 receive power via standard diode-based bootstrapping, also integrated within the chosen driver solution. Since the source of FETs S_{3L} through S_{6L} maintain a constant voltage offset, irrespective of flying capacitor voltage ripple, all may be driven directly by driver U_5, where capacitive coupling provides the necessary level-shifted V_{gs} signals, and gate-to-source zener diodes ensure correct biasing of the level-shifting

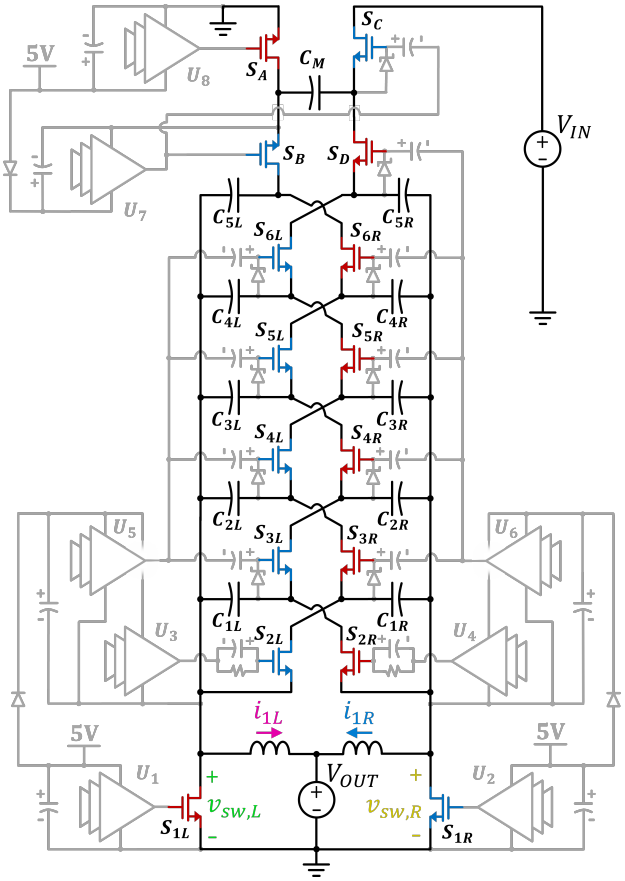


Fig. 4: Schematic of the primary power stage and associated gate driving.

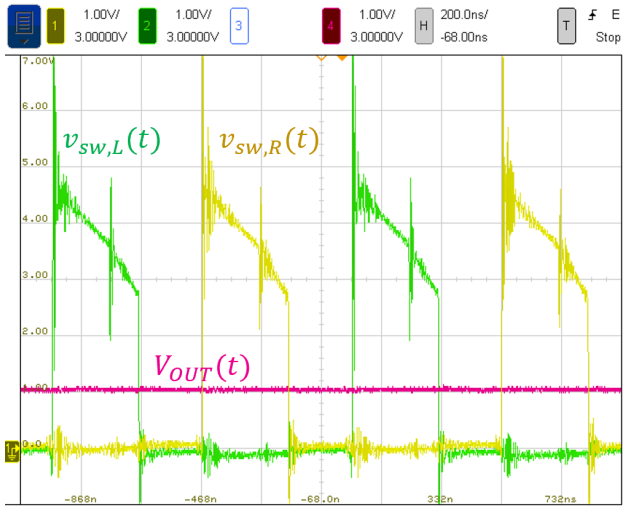


Fig. 5: Measured output and switched node voltages for $V_{IN} = 48$ V, $V_{OUT} = 1$ V, $I_{OUT} = 50$ A, and $f_{SW} = 1$ MHz. Inherent phase-shifted PWM facilitates the effective use of coupled inductors for ripple cancellation and improved transient response.

capacitors. Although U_5 would ideally be referenced to the source of S_{3L}, this would require an additional bootstrapping diode for power delivery. Instead, here U_5 is referenced to the source of S_{2L} (along with U_3); subsequently the load-induced voltage ripple imposed upon the flying capacitors is also imposed upon the V_{gs} gate signals stemming from driver

TABLE I: PRIMARY COMPONENT DETAILS

Component	Details	Part Number
$S_{A,B,C,D}$	100 V 23 mΩ	2× EPC2070
S_{1-6X}	15 V 26 mΩ	2× EPC2216
S_{1X}	40 V 1.1 mΩ	EPC2066
C_{IN}	1 μF 50 V	42× GRM155R61H105ME05D
C_{OUT}	22 μF 10 V	28× GRM158R61A226ME15D
C_M	1.5 μF (derated)	4× GRM155C61E475ME15
$C_{5,L/R}$	1.51 μF (derated)	3× GRM155C61E475ME15 1× GRM155R61E225KE11D
$C_{4,L/R}$	1.55 μF (derated)	1× GRM155C61E475ME15 3× GRM155R61E225KE11D
$C_{3,L/R}$	1.54 μF (derated)	3× GRM155R61E225KE11D 1× GRM155R61E105MA12D
$C_{2,L/R}$	1.57 μF (derated)	1× GRM155R61E225KE11D 1× GRM155R61E105MA12D 2× GRM155R61A684KE15D
$C_{1,L/R}$	1.53 μF (derated)	3× GRM155R61A684KE15D
U_X	0.7 Ω / 0.4 Ω Source / Sink	uP1966e
	5.6 V Zener 0201	GDZ5V6LP3-7
	0.1 μF 35 V 0201	GRM033R6YA104ME14D
L_{1L}, L_{1R}	7.5 mm×4.5 mm×2.3 mm, 2mil air gaps 78 nH (self), 30 nH (mutual)	E-I core ML91S material

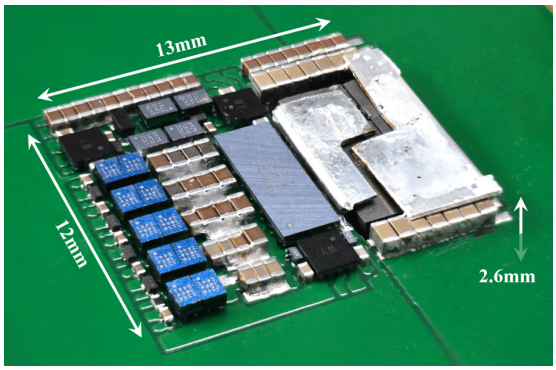


Fig. 6: Photograph of the hardware prototype (top side), including a custom single-turn coupled inductor. The PCB's bottom side is similar, due to the converter's symmetry, while also including flying capacitor C_M.

U_5. However, the 5.6 V zener clamps ensure that V_{gs}-imposed ripple can only cause slight degradation in drive strength (V_{gs} <5 V), and that when low; V_{gs} signals are kept below turn-on threshold V_{TH}, avoiding any false turn-on. A similar capacitor voltage offset strategy is used for driving S_C using U_7. Gate drivers U_3 and U_4 are used to implement split-phase switching in the SDIH stage [13] and include gate-connected capacitors biased at 0 V for delay matching purposes only.

Table I lists primary component details, while Fig. 6 depicts the top side of the constructed hardware prototype whose total volume is encompassed by a best-fit cuboid measuring 13 mm × 12 mm × 2.6 mm, or 405.6 mm^3 (0.02475 inch^3). Fig. 7 plots measured efficiency curves which achieve peak and full-load efficiencies of 91.9 % and 88 % when ignoring gate driving losses, and 90.1 % and 87.3 % when including all losses. Fig. 8 depicts the prototype's thermal behaviour in steady-state operation at full load. For a maximum tested current output of 50 A, and with regulation to 1 V, this prototype achieves a very high measured power density of 2,020 W/inch^3 (123.3 kW/liter). Finally, Table II compares this work against other recent competitive 48 V to 1 V demonstrations.

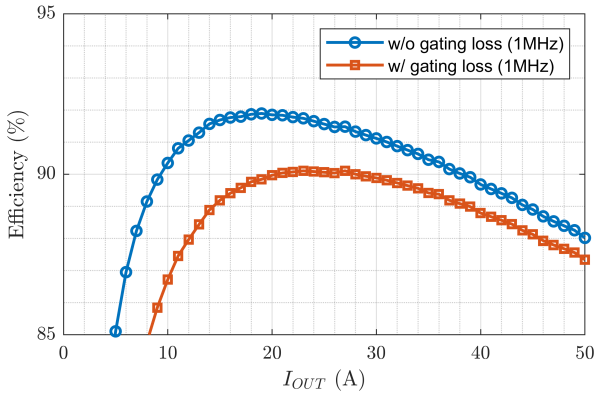


Fig. 7: Measured efficiency versus load current when operating at 1 MHz switching frequency and performing 48 V to 1 V conversion. A peak efficiency of over 90 % is recorded when accounting for gate driving losses.

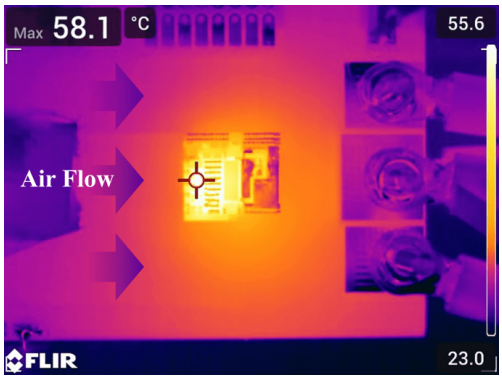


Fig. 8: Thermal photograph when operating at 50 A load current, 48 V to 1 V conversion, and after having reached thermal equilibrium. The hardware prototype reaches a steady 58°C when subject to forced air cooling using a standard 12 V computer fan.

IV. CONCLUSION

This work presents a new HSCC topology applicable to high conversion ratio PoL applications, including 48 V to 1 V power delivery. A high performance SDIH stage is employed for its effective use of switching devices, while an initial 2:1 voltage reduction stage eliminates most of the flying capacitor volume. The availability of high performance GaN devices with inherent radiation hardening makes this topology well suited for use in space applications with increasing compute power. A hardware prototype validates both the topological structure and a compact gate driving scheme which uses 8 gate drivers to drive 16 switches. When performing 48 V to 1 V conversion, this prototype demonstrates a very high power density of 2,020 W/inch^3 (123.3 kW/liter) while retaining efficiencies greater than 87 %. Future work will discuss transient response, inductor design, and the use of additional assistive circuit techniques for improved performance (e.g., Schottky diodes placed across low-side GaN-FETs).

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TABLE II: COMPARISON WITH OTHER RECENT 48 V TO 1 V CONVERTER SOLUTIONS

Year	Topology	Switching Frequency	Power Density	Power Stage Efficiency	System Efficiency (including driving losses)
2024	This Work Doubler + SDIH	1 MHz	2,020 W/inch^3 (by box volume)	Peak Efficiency: 91.9 % Full-load Efficiency: 88 %	90.1 % 87.3 %
2024	20-to-1 SBC [1]	220 kHz	759 W/inch^3 (by box volume)	Peak Efficiency: 94.1 % Full-load Efficiency: 85.9 %	92.6 % 85.6 %
2023	Mini-LEGO [2]	1515 kHz	1,390 W/inch^3 (by box volume)	Peak Efficiency: 87.1 % Full-load Efficiency: 84.1 %	84.1 % 82.3 %
2023	MSC [3]	400 kHz	621 W/inch^3 (by box volume)	Peak Efficiency: 93.1 % Full-load Efficiency: 86.2 %	91.7 % 85.8 %
2023	16-to-1 SBC [4]	150 kHz	464 W/inch^3 (by box volume)	Peak Efficiency: 94.7 % Full-load Efficiency: 86.4 %	93.4 % 86.1 %

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