Novel Integrated CMOS Pixel Structures for Vertex Detectors

Stuart Kleinfelder[1], *Member, IEEE*, Fred Bieser, Yandong Chen, Robin Gareus, Howard S. Matis, Markus Oldenburg, Fabrice Retiere, Hans Georg Ritter, Howard H. Wieman, Eugene Yamamoto

***Abstract*—Novel CMOS active pixel structures for vertex detector applications have been designed and tested. The over-riding goal of this work is to increase the signal to noise ratio of the sensors and readout circuits. A large-area native epitaxial silicon photogate was designed with the aim of increasing the charge collected per struck pixel and to reduce charge diffusion to neighboring pixels. The photogate then transfers the charge to a low capacitance readout node to maintain a high charge to voltage conversion gain. Two techniques for noise reduction are also presented. The first is a per-pixel kT/C noise reduction circuit that produces results similar to traditional correlated double sampling (CDS). It has the advantage of requiring only one read, as compared to two for CDS, and no external storage or subtraction is needed. The technique reduced input-referred temporal noise by a factor of 2.5, to 12.8 e^-. Finally, a column-level active reset technique is explored that suppresses kT/C noise during pixel reset. In tests, noise was reduced by a factor of 7.6 times, to an estimated 5.1 e^- input-referred noise. The technique also dramatically reduces fixed pattern (pedestal) noise, by up to a factor of 21 in our tests. The latter feature may possibly reduce pixel-by-pixel pedestal differences to levels low enough to permit sparse data scan without per-pixel offset corrections.**

I. Introduction

Recent work has demonstrated that standard CMOS active pixel sensors (APS) [1] can be used to detect minimum ionizing particles with high spatial resolution and good signal to noise [2-8]. These use integrated sensors and readout circuitry (Fig. 1), and do not require wire or bump-bonding between the two. The advantages over traditional hybrid approaches are greatly reduced cost and the potential for vastly larger pixel counts and densities. However, challenges remain in terms of their signal to noise, readout speed, and to obtain the benefits of sparse readout. High signal to noise is necessary in large arrays to suppress false hits that are merely due to noise. Correlated double sampling (CDS) is a traditional method of reducing noise, particularly kT/C reset noise, but in the case of typical CMOS APS, it requires two full reads, full frame storage, and an external subtraction. The two reads slows down the readout process, and a method of reducing noise while speeding the readout and processing is important. This paper presents three new attempts to increase signal to noise, reduce readout overhead, and to progress towards practical sparse readout.

Manuscript received October 29, 2003.

[1]S. Kleinfelder and Y. Chen are with the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA, 92697, USA (e-mail: stuartk@uci.edu).

F. Bieser, R. Gareus, H. S. Matis, F. Retiere, H. G. Ritter, H. H. Wieman, M. Oldenburg, E. Yamamoto are with the Lawrence Berkeley National Laboratory, Berkeley, CA, 92720, USA.

II. Native Epitaxial Silicon CMOS Photogates

One problem with the use of CMOS APS is that the photodiode node must have small capacitance in order to obtain high charge to voltage conversion gain. This rquires that the area of the photodiode be kept small, and hence a given diode will pick up only a fraction of the total liberated charge. The remaining charge will diffuse to a region of neighboring pixels or will recombine. This significantly lowers the signal to noise ratio of the system.

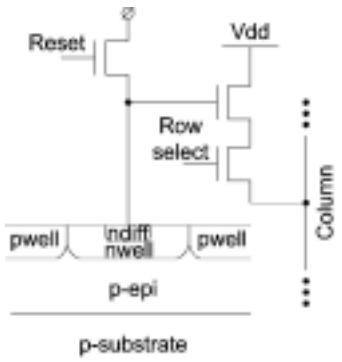

Fig. 1: Basic three-transistor active pixel sensor schematic showing a physical representation of the n-well / p-epi diode.

The use of a CMOS photogate, as opposed to a photodiode, may improve this situation. A photogate (Fig. 2) resembles one bit of a CCD. Electrons created in the epi layer diffuse to a broad field region created directly below the large area photogate, which is biased at a higher potential. They are held there until the photogate voltage is dropped to below the transfer gate voltage, at which point they migrate to the higher-potential, lower capacitance, readout node. The readout node must be periodically reset and the photogate must be continually cycled to keep the region directly under the photogate depleted. In principle, the photogate can deliver both higher local charge collection by virtue of its large area, and high charge-to-voltage conversion gain due to charge transfer to a low-capacitance readout node. Photogates can make CDS more convenient, since they eliminate the requirement, in APS, for complete frame storage of the first sample. Instead, two reads, one right before charge transfer, and one afterward, can take place within the readout of one row of pixels. Only

one row of storage is necessary, though two reads and subtraction are still required.

An example photogate pixel layout is shown in Fig. 3. The large area covering most of the pixel is the photogate (PG) transistor. The upper right hand corner shows the transfer gate (TX) and readout circuitry. In CCD's, these gates overlap, but this is not possible in a single-polysilicon process such as the one used here.

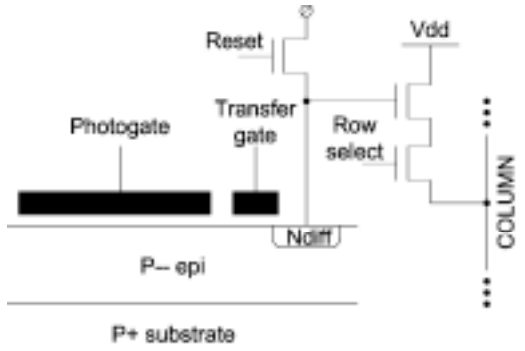

Fig. 2: Native epitaxial silicon photogate circuit. This version includes an active area only (no diffusion or field-oxide) between the photogate and the transfer gate.

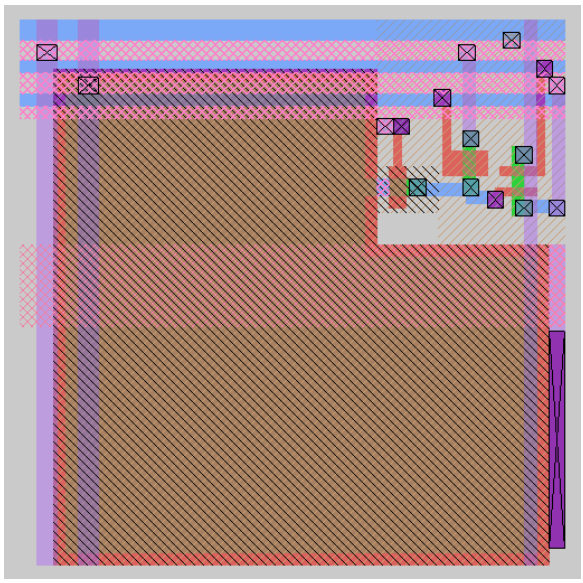

Fig. 3: Example photogate pixel layout. The large shape is the photogate, while circuitry in the upper right corner includes the transfer gate, reset and readout transistors.

Our photogate structure differs from the standard CMOS photogate in several ways (Fig. 2). It is a "native epitaxial silicon" photogate in that it is constructed directly in the higher-resistivity epitaxial silicon instead of lying in a p-well, as would be normal. This permits it to collect charge from the epi region without the interference of a p-well. In addition, there is a small gap and no diffusion or field-oxide between the PG and TX gates, a compromise solution that maximizes the charge transfer efficiency under the circumstances. The size of the gap between PG and TX is critical, however. Simulations demonstrate that too large a gap can lead to insufficient transverse field and create a potential barrier to the transfer of electrons.

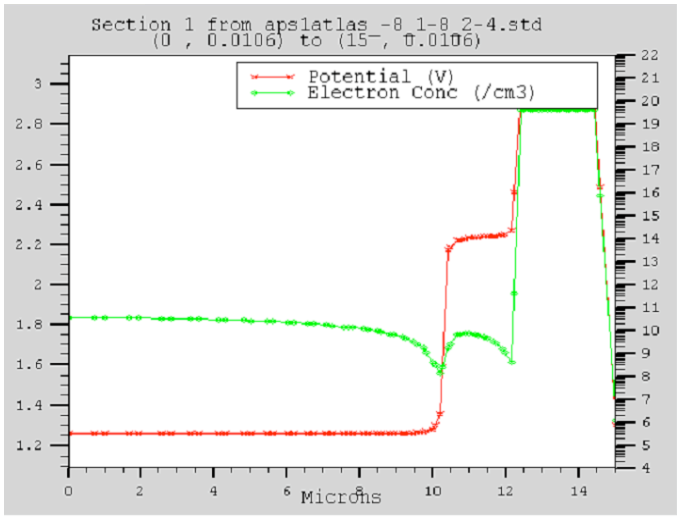

Fig. 4: Simulations of potential voltage (red, left scale) and electron concentration (green, right scale)_laterally across a photogate, where the gap between the PG and TX gates (seen around 10 microns on the x-axis) is 0.4 μm. A smooth, monotonically rising potential voltage is seen, facilitating charge transfer.

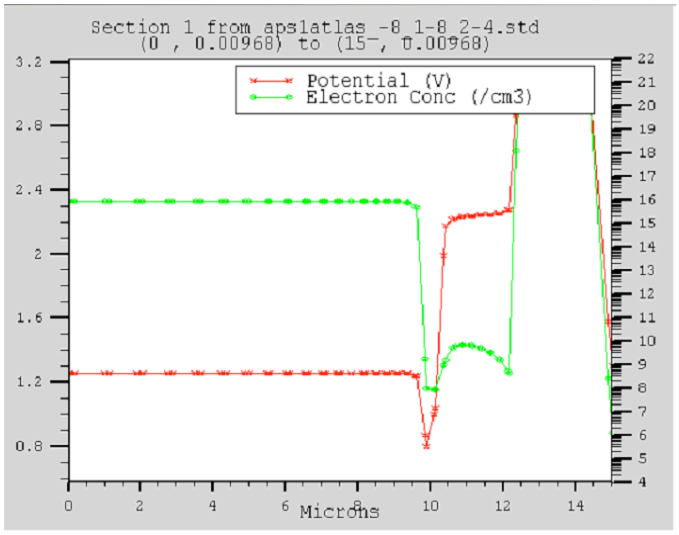

Fig. 5: Simulations of potential voltage (red, left scale) and electron concentration (green, right scale) laterally across a photogate, where the gap between the PG and TX gates (seen around 10 microns on the x-axis) is larger, at 0.8 μm. A dip in the potential voltage is seen, impeding charge transfer.

Figure 4 shows the potential voltage and electron concentration laterally across the photogate (from left to right including the PG, TX and the readout diffusion), during transfer, given a 0.4 μm gap between PG and TX. We can see a monotonic increase in potential voltage which allows an unimpeded transfer of electrons. Extend that gap to 0.8 μm, as shown in Fig. 5, and a dip in the potential voltage is seen, which would block the transfer of electrons. The distance in the actually fabricated circuit was 0.45 μm.

Tests with a variety of fabricated photogate structures are in progress. Pixels including differences in various details, such as the boundaries of the p-wells, the inclusion of diffusion between PG and TX, the elimination of the TX gate, large area photodiodes with a TX gate, etc., have been fabricated. Electrical tests of the photogate circuit have demonstrated sensitivity to Fe-55 X-rays, and that it succeeds in collecting charge. Full charge transfer has been achieved on a test structure including the same photogate shown in Fig. 3 but without transfer gate. However, proper operation of the transfer gate has not yet been established.

Figure 6 shows the response of the photogate-only (no transfer gate) structure to Fe-55 X-rays varying steady-state PG voltage. Color indicates the number of occurrences for each ADC count and PG voltage. The best response was at PG=1.5 V, however a clear 5.9 keV peak was difficult to see.

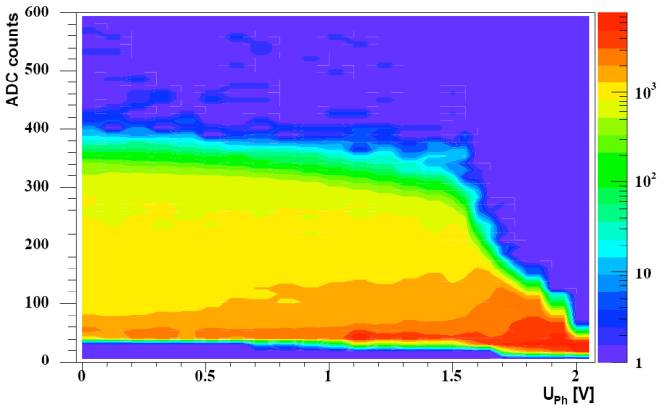

Fig. 6: A detailed DC scan, varying steady-state PG voltage, in response to Fe-55 X-rays. Vertical axis shows ADC counts. Horizontal axis shows PG voltage. Color indicates the number of occurrences for each ADC count and PG voltage.

Some other results have also been puzzling. One difficult to understand result is that charge transfer times are slow compared to simulations, and that a fraction of the expected charge is being lost. One theory that is being explored is the possibility that a large fraction of the collected charge is trapped by surface states in the very large photogate area, over which the collected charge density may only be a few electrons per square micrometer. Standard CMOS does not allow for buried channels or pinning that would reduce this trapping. It may come to pass that photogates will have difficulties in this application until more specialized processes become available.

III. Per-Pixel kT/C Noise Reduction

We have fabricated and tested a per-pixel circuit that is demonstrated to substantially reduce kT/C noise. It holds the advantage of requiring only one read and no external subtraction. Depicted in Figs. 7 and 8, it shows a photodiode, its reset switch T1, a source-follower T3-T4, a coupling capacitor C2, an additional reset switch T2, and readout circuitry T5-T6. The basic idea is to store the large kT/C noise offset from the T1 reset, which is on a low-capacitance node, across the much larger coupling capacitance C2. In this way, the over-all kT/C noise is substantially determined by the larger value of C2, and is hence reduced.

Figure 9 shows the timing operation of the per-pixel noise reduction. The small Δt between the conclusion of Reset1 and Reset2 stores the kT/C noise offset of the diode node across C2. Normal charge integration and readout follows. It is interesting to note that by switching the Reset1 and Reset2 concluding time (Fig. 9), operation with and without "CDS" can take place, allowing direct comparisons. During CDS operation, output noise is reduced by:

$$\frac{V_n}{V_{n,CDS}} = \sqrt{\frac{C_2}{C_1}} \cdot A_{SF1},$$

where A_{SF1} is the gain of the additional source follower T3-T4.

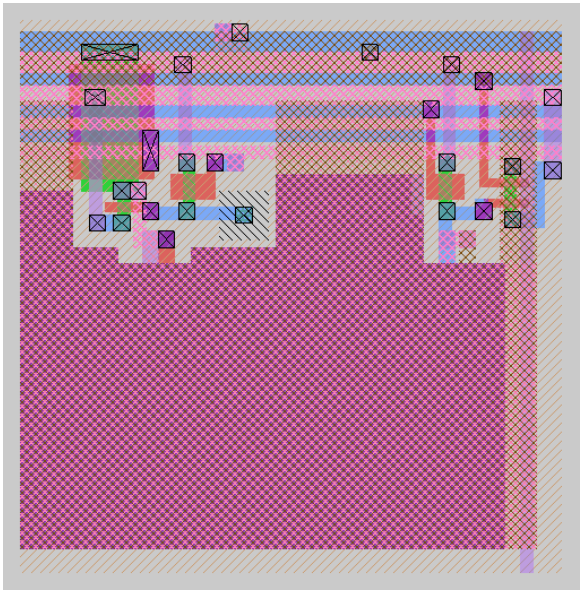

Fig. 7: Photodiode with clamp / CDS circuit. The large area is the coupling capacitor, which is formed from polysilicon and metal overlaps.

The test circuit was fabricated without the benefit of a high-density capacitor structure. Instead, a stack of polysilicon and metal layers formed the capacitor. However, measurements substantially match the theoretically expected noise reduction, and projections were also made that take into account the higher C2 value that would be possible with a typical double-polysilicon or metal-insulator-metal capacitor. The results are summarized in Table 1.

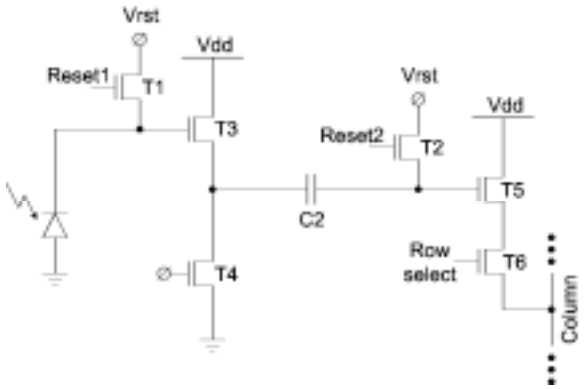

Fig. 8: Basic kT/C noise reduction pixel schematic.

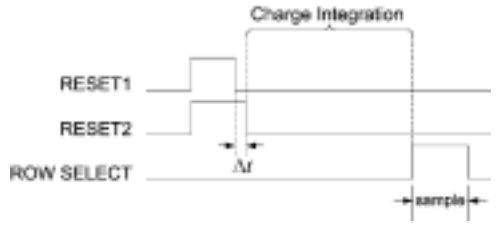

Fig. 9: Per-pixel kT/C noise reduction timing diagram.

Table 1: Per-Pixel Noise Reduction Test Results.

Measured output noise without CDS:	705 μV
Input referred noise without CDS:	32.3 e^-
Measured output noise with CDS:	279 μV
Input referred noise with CDS:	12.8 e^-
Measured noise reduction factor:	2.5
Projected noise with high-density cap:	202 μV
Input referred noise with high-density cap:	9.3 e^-
Projected noise reduction factor:	3.5

It should be noted that the measured noise, using this technique, compared very favorably to the best result using traditional CDS (10.34 e^-), and may be superior when high-density capacitors are used. Yet this technique requires only one read and no external subtraction. It's therefore much faster and more convenient. Drawbacks include having slightly reduced gain due to the extra source follower, and of requiring additional power. The added per-pixel power is only used during reset and readout however, and can be turned on one row at a time, so this is a fairly minor concern. This simple technique shows significant promise.

IV. Active Reset Noise Reduction

A chip testing a variation on a relatively new method of kT/C noise reduction, "active reset" [9], here implemented at the column level, was fabricated and measured. The technique appears particularly well suited to applications where high sensitivity and low noise are required.

Column-level active reset requires one additional transistor per pixel, bringing the total to 4 in an otherwise-traditional APS, and a per-column op-amp (Fig. 10). The added transistor per pixel controls the gate of the reset transistor M1. The test chip is in a 0.5 μm process, including a 10-12 μm epitaxial region, and contains several sectors of pixels, each with different photodiodes and/or other circuit variations. These variations allowed noise comparisons with different photodiode and feedback capacitances, including tests with explicitly added additional feedback capacitance.

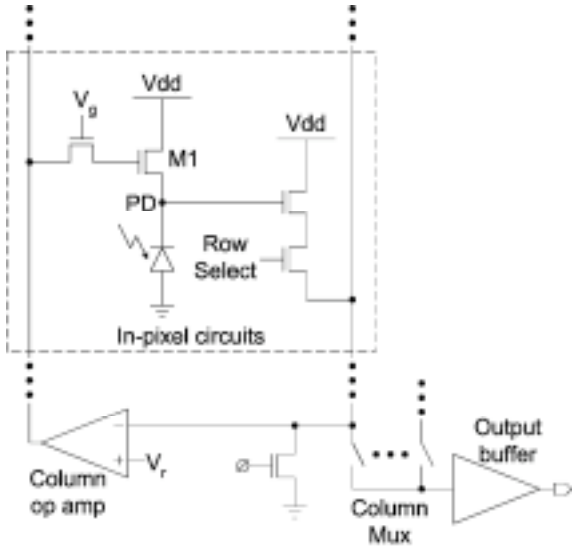

Fig. 10: Basic active reset schematic diagram. A single pixel is shown, along with the per-column op-amp and chip-wide output multiplexing.

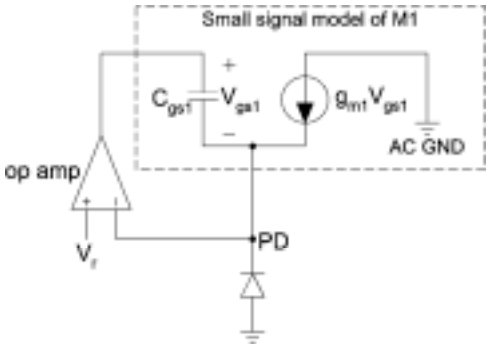

Fig. 11: Simplified active reset model. The capacitance that is amplified is the parasitic gate to source capacitance of the reset transistor M1. Some test pixels included additional explicit capacitance to strengthen the effect. The transconductance of the reset transistor is also modulated by the feedback.

The two most important feedback mechanisms of active reset are the amplification of feedback capacitance and hence the increase in the effective capacitance on the photodiode during reset due to the Miller effect (reducing kT/C reset noise), and the control of the resetting current via negative feedback. The first feedback loop is via the gate-to-drain capacitance of the photodiode reset transistor M1. This capacitance is amplified by a factor of (A+1), where A is the open-loop gain of the column-level op-amp. The second feedback is through transconductance of the reset transistor M1. Noise on the photodiode node will be reduced by the opposing, amplified, modulation of the drain current in the reset transistor. Theoretical analysis also shows that the portion of image lag due to different input signals causing different subsequent dark currents will also be reduced by a factor of (A+1). Finally,

active reset techniques can reduce FPN, particularly FPN within each column where differing op-amp offsets are not an issue, by stabilizing the different pixel outputs against a reference voltage.

Readout noise of ~44 microvolts and a dynamic range of ~90 dB (~15 bits), rms, was measured on a sector with large photodiodes. Noise measurements on small photodiodes suitable for the vertex tracking application showed the greatest improvement in noise, and the technique looks very promising. While output noise measurements are accurate, it should be stated that input-referred noise values are calculations that depend on a conservative, carefully estimated value of the read node capacitance.

The results for the small photodiode pixels are summarized in Table 2. Output noise of 120 μV, rms, was measured using active reset, as compared to 910 μV with a standard reset. Noise of ~5.1 electrons, rms, referred back to the photodiode node, was estimated on the small photodiode pixels (~5.8 fF estimated diode node capacitance). This compares to ~38.3 electrons when measured with a standard "hard" reset, for a factor of ~7.6 improvement. Row and column fixed pattern noise (FPN) were also improved, with measurements of 0.048% and 0.27%, respectively, as compared to 1% for both in an equivalent normal hard reset..

Table 2: Active Reset Test Results

Output noise without active reset:	910 μV
Input referred noise w/o active reset (est.):	38.3 e^-
Output noise with active reset:	120 μV
Input referred noise with active reset (est.):	5.1 e^-
Improvement in noise due to active reset:	7.6 x
Fixed pattern noise (FPN) w/o active reset:	1%
FPN within columns with active reset:	0.048%
Improvement in FPN within columns:	21 x

Active reset looks very promising for several reasons. It significantly reduces both temporal and fixed pattern noise, yet it does not affect the gain of the system as the previous per-pixel "CDS" circuit does. It obtains similar or better noise reduction as conventional CDS. In particular, traditional CDS actually increases all sources of noise that are not correlated between samples, while active reset does not. Although reset is slower (this can be pipelined), it requires only one read and no subtraction.

The FPN reduction becomes particularly interesting if sparse data readout is considered. In normal APS readout, FPN can be higher than the signal levels seen in vertex applications, and hence pixel-by-pixel pedestal subtraction may be required, posing a substantial burden. With active reset, the dramatic reduction in FPN noise within each column may negate that need, at least with a little additional effort, and only per column offset cancellation may be necessary – a far easier proposition.

V. Summary and Conclusions

Several new CMOS active pixel circuits for vertex tracking applications have been designed and tested. Native epitaxial silicon photogate variations are being investigated for their potential to increase local charge collection while preserving high charge to voltage gain. A fast per-pixel kT/C noise reduction circuit was tested and found to yield results competitive with traditional CDS, with 12.8 e- input referred noise measured, and 9.3 e- noise projected with the use of high-density capacitors. A column-level active reset noise reduction circuit was tested to reduce temporal noise by a factor of 7.6 and fixed-pattern (pedestal) noise by up to 21 times. Input referred noise was estimated to drop from 38.3 e^- to 5.1 e^-.

Acknowledgements

This work was supported in part by the Director, Office of Science, U.S. Department of Energy, under Contract DE-AC03-76SF00098.

References

[1] E. Fossum, "Active pixel sensors: Are CCD's dinosaurs?," in *Proc. SPIE*, vol. 1900, 1993, pp. 2–14.

[2] B. Dierickx, G. Meynants, D. Scheffer, "Near 100% fill factor CMOS active pixels," IEEE CCD & AIS workshop, Brugge, Belgium, 5-7 June, 1997; Proceedings p. P1.

[3] G. Meynants, B. Dierickx, and D. Scheffer, "CMOS active pixel image sensor with CCD performance," AFPAEC Europto/SPIE, Zürich, 18-21 May 1998; proc. SPIE, vol. 3410, pp. 68-76, 1998.

[4] R. Turchetta, et al., "A Monolithic Active Pixel Sensor for Charged Particle Tracking," Nucl. Instrum. and Methods A, 458, 8 (2001).

[5] Y. Gornushkin, G. Claus, W. de Boer, J. Bol, G. Deptuch, A. Dierlamm, W. Dierlamm, W. Dulinshki, D. Husson, M. Koppenhoefer, J. L. Riester, and M. Winter, "Test results of monolithic active pixel sensors for charged particle tracking," *Nucl. Instrum. Method*s, vol. A478, pp. 311–315, 2002.

[6] S. Kleinfelder, H. Bichsel, F. Bieser, H. S. Matis, G. Rai, F. Retiere, H. Wieman, and E. Yamamoto, "Integrated X-ray and charged particle active pixel CMOS sensor arrays using an epitaxial silicon sensitive region," in *Proc. SPIE Hard X-Ray and Gamma Ray Detector Physics IV*, Seattle, WA, July 2002.

[7] H. S. Matis, F. Bieser, S. Kleinfelder, G. Rai, F. Retiere, H. G. Ritter, K. Singh, S. E. Wurzel, H. Wieman, E. Yamamoto, "Charged Particle Detection using a CMOS Active Pixel Sensor," IEEE Transactions on Nuclear Science, Vol. 50, No. 4, August 2003.

[8] Howard S. Matis, Fred Bieser, Stuart Kleinfelder, Gulshan Rai, Fabrice Retiere, Hans Georg Ritter, Kunal Singh, Samuel E. Wurzel, Howard Wieman, Eugene Yamamoto, "A CMOS Active Pixel Sensor for Charged Particle Detection," Nuclear Science Symposium, 2002. Conference Record of the 2002 IEEE, 2002.

[9] Fowler, B., Godfrey, M., Balicki, J., Canfield, J., "Low noise readout using active reset for CMOS APS." SPIE Proc, Int. Soc. Opt. Eng., vol. 3965, pp. 126-35, 2000.