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Acquisition and Processing of Multiparametric Information from a Pixel Matrix

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Abstract

This paper addresses the design of a system intended to readout multiparametric information from a matrix of pixels.

The system presented here acquires the charge associated with the signal and provides a timing information from each pixel. Although it lends itself to a broad range of time-correlated imaging situations involving any kind of pixel matrices, the design constraints assumed here are particularly tailored to the application with pixels that sense the output charge distribution from a Micro Channel Plate (MCP).

The combination of a microchannel plate and a pixel matrix is an extremely versatile detector and the readout system must be able to fully exploit the intrinsically high position resolution and time accuracy featured by the MCP.

The behavior of the readout system described in this paper is based upon advanced concepts to meet the above application requirements and is believed to provide a significant functional improvement over the conventional pixel systems.

I. INTRODUCTION

The introduction of pixel detectors in tracking applications has set the demand for high density readout electronics consisting of one cell per pixel with the task of identifying the address of the pixels where signals above a preset threshold are recorded. The same readout electronics associated with a histogramming memory to build-up the distribution of counts recorded by each pixel in a fixed time interval is employed in imaging applications. In either case, only the presence of a signal is recorded by the readout system [1], [2], [3], [4].

There are, however, situations, where signal-related parameters are to be extracted and a readout is able to acquire and process multiparametric information is required.

For example, if the value of the charge associated with the signal is available, it is possible to increase the position resolution well beyond the geometric size of the pixel by using an interpolation approach.

Signal timing is important in several time-resolved or time-correlated position sensing and imaging applications. Examples of situations requiring both position and time information are provided by Time-of-Flight mass spectroscopy and by the analysis of reactions initiated by photo ionization (molecular dissociation), where the photo ionization produced by laser light results in fragmentation. Multi hit time-resolved detection may be required in this case [5], [6], [7].

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One more example of a situation demanding accurate timing is the principle of three dimensional imaging based upon time-domain reflectometry associated with a pixel matrix.

The idea of multiparametric acquisition from pixel matrices can be extended to more complex cases including other signal features, for instance, shape-related parameters.

The present paper aims at discussing the design of a multiparametric system to be associated with a pixel matrix.

As already pointed out, the system, though not restricted to this application, is conceived to meet the requirements set by the detector shown in fig.1, consisting of an MCP read out by a matrix of electrodes deposited on an insulating substrate.

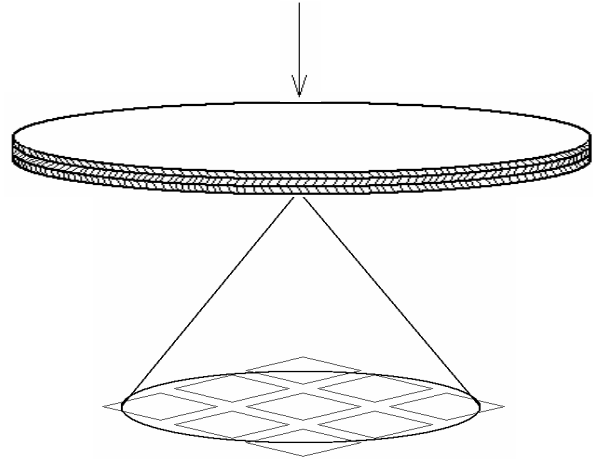


Figure 1: Micro Channel Plate read out by a pixel matrix

The detector of fig.1 is extremely versatile. By a suitable choice of the photocathode material or of the input converter, it may be employed to detect photons on a very broad range of wavelengths, from infrared to low energy X-rays as well as particles of different nature.

The intrinsic position resolution of an MCP is substantially better than that of a semiconductor pixel detector. The only way of retaining this feature by a pixel readout of the type shown in fig.1 is by making use of position interpolation. A spatial resolution five to ten times better than the geometric size of the sensing electrodes in fig.1 can be reasonably expected from this approach. A substantial improvement over the existing imaging techniques may result in such an important field like mammography.

One more important feature of the MCP is its timing accuracy, which makes the detector of fig.1 particularly suitable for time-resolved and time-correlated applications.

The design concepts presented in this paper have been developed looking at a broad spectrum of applications with highly segmented detectors, mainly pixel matrices and, as a particular case, microstrip structures. The next section is devoted to the discussion of these concepts.

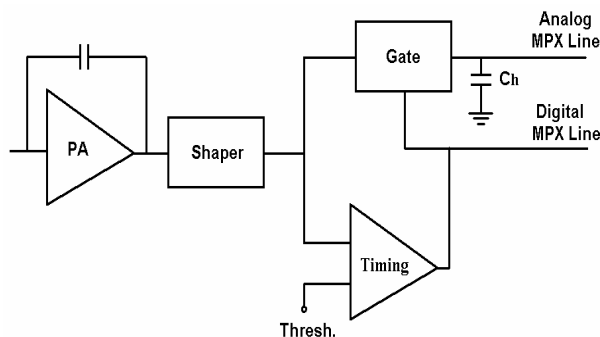
II – SYSTEM DESIGN CONCEPTS

The fundamental part of any readout system to be associated with a highly segmented detector is the elementary cell in the case of a pixel readout or the individual channel in the case of a microstrip readout. The former case sets obviously much more stringent area limitations, for the pixel size in the matrix sets the limit to the silicon area available for the elementary cell. The goal assumed in the actual design was a cell complying with the pixel area limitations, whose layout, in the case of a microstrip readout, would be modified to benefit from the more relaxed constraints in the area available.

The application considered of highest importance and originality is the acquisition and processing of charge and time information associated with the signals delivered by the pixels in a detector of the type of fig.1.

The following features were considered as the targets to be achieved with the elementary cell.

- It must be able to operate at high rates, between 10^6 and 10^7 s⁻¹
- Its input-referred equivalent noise charge (ENC) must be in the 500e region at a detector capacitance of 2pF
- It must provide a timing accuracy in the subnanosecond region on a broad range of input charge values
- It must be able to resolve in real time clusters of events, so its deadtime must be short, less than about 100 ns.
- It must lend itself to a radiation hard implementation.



The block diagram of the elementary cell is shown in fig.2.

Figure 2: Conceptual diagram of the elementary pixel cell

It consists of a linear amplifying and shaping channel whose output is split along two lines. One is a high accuracy timing channel based upon a constant fraction approach which

provides the event timing and also the sequencing signals. The other one is the amplitude storage line, basically a peak sensing analog memory whose operation is controlled by the timing circuitry.

The whole acquisition and processing system will be realized by providing an elementary cell of the type described in figure 2 for each pixel to be served and by adding the circuits that implement the additional functions like centroid finding. The centroid will be determined by applying the suitable algorithm to the values of the charge stored in the analog memories associated with the pixels that belong to a given submatrix, for instance the nine-unit region in figure 1.

The complete multiparametric readout system will be built-up arranging the described elementary cells in a monolithic matrix to match the pixel mosaic. The transmission of the acquired and processed information to the outside world will be based upon a column readout architecture [8].

The basic cell of fig. 2 may provide also the basis for the development of a microstrip readout system based upon the same concepts illustrated for the case of the pixel matrix. However, in association with a microstrip detector the centroid finding system becomes much simpler and can be based on the circuitry whose schematic diagram is shown in

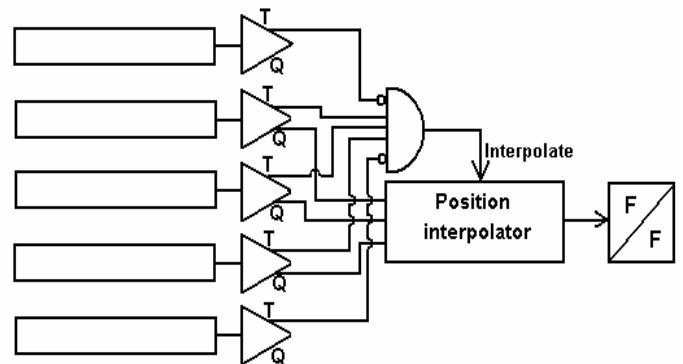


fig. 3 in the case of a three strip position interpolation.

Figure 3: Centroid finding logic in the case of a microstrip readout.

The elementary cells are schematically represented by the triangular blocks in fig.3. The Q line out of each cell transmits the charge information as it appears on the storage capacitor C_h in fig.2 to the position interpolator. The T lines carry the timing signals from each elementary cell. The position interpolator is enabled by the coincidence of the T signals from the three central strip and vetoed by a T signal which may appear on either of the strip above and below the three on which the centroid is evaluated. The circuit function can be easily extended to situations involving larger number of strips.

The elementary cell was designed in two versions that differ for the geometry of the input active device in the preamplifier and for its standing current. One version is intended for pixel applications at detector capacitances up to 200 fF, the other one is tailored to larger pads and short strips up to a detector capacitance of 2pF.

Emphasis in the design was put on achieving outstanding noise performances at shaping times of a few tens of nanoseconds, to enable the cell to operate at very high hit rates.

As a first example of a system based on the elementary cell of fig.2, the realization of a microstrip readout utilizing the logic cluster selection of fig. 3 is presently underway in a CMOS 0.5micron channel process.

Next step will be the pixel readout system to be associated with the microchannel plate.

III – THE ELEMENTARY CELL

This section provides a description of the design concepts that have been adopted in the design of the main blocks in the elementary cell, that are the charge-sensitive preamplifier, the shaper and the timing unit.

A. Concepts underlying the design of the preamplifier

In the more advanced CMOS processes, featuring values of the gate oxide thickness of 10 nm or less, the choice of a P-channel as a preamplifier input device, which would be suggested by consideration of 1/f-noise is no longer mandatory.

N-channel MOSFETs parts of a thin oxide process, feature a suitably small 1/f –noise and over the P-channel MOSFET offer the advantage of a larger transconductance-to-standing current ratio g_m/I_d .

An N-channel MOSFET was accordingly chosen as the input active device in the charge-sensitive loop of fig. 2. In the version intended for larger capacitances, up to 2 pF the input MOSFET has a gate width $W=300\mu\text{m}$ and a length $L=1\mu\text{m}$. At its design standing current of $200\mu\text{A}$ it features a transconductance g_m of about 3.3 mS. In the version for smaller detector capacitances, below 200fF, the input device has a gate width $W=30\mu\text{m}$ and a length $L=1\mu\text{m}$. At a standing current of $20\mu\text{A}$ it features a transconductance of about 0.33 mS, both being the g_m values are provided by the simulations.

The feedback capacitor is 0.14 pF in both configurations.

B. Concepts adopted in the design of the shaper

For the shaper which follows the preamplifier in fig.2, a design approach which is to be considered original in a monolithic CMOS implementation has been adopted. The idea was to transfer onto a monolithic chip the design of a triangular or trapezoidal shaper which in a discrete design would rely upon delay lines.

For this purpose a delay unit was required. It has been realized on the basis of a feedback, unity gain buffer. The Laplace-domain operator $(1-e^{-sT})$, where s is the complex variable, has been obtained as shown in the block diagram of fig. 4a), where **D** is a difference amplifier.

The actual realization is shown in fig.4 b), where the buffer is made of the long-tailed pair Q_1, Q_2 , the source follower Q_3 and associated current sources. The difference

amplifier **D**, made of transistors Q_4 through Q_{14} is an open-loop structure. In spite of this, it features a good linearity as a result of the distortion-compensating approach applied to both non the noninverting path (Q_7-Q_{13}) and the inverting one (Q_8-Q_{13}).

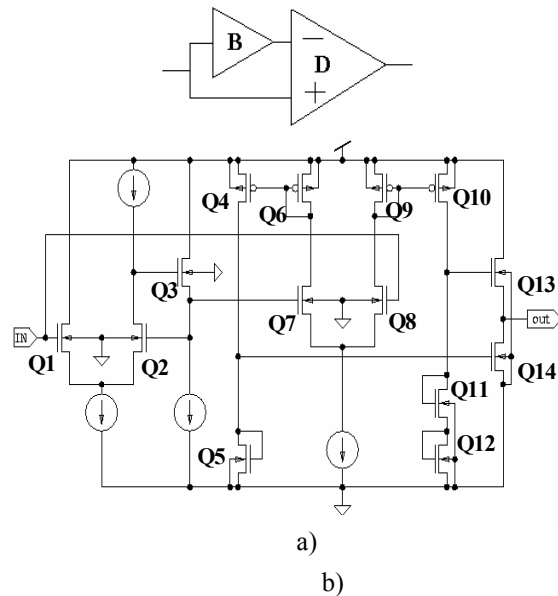
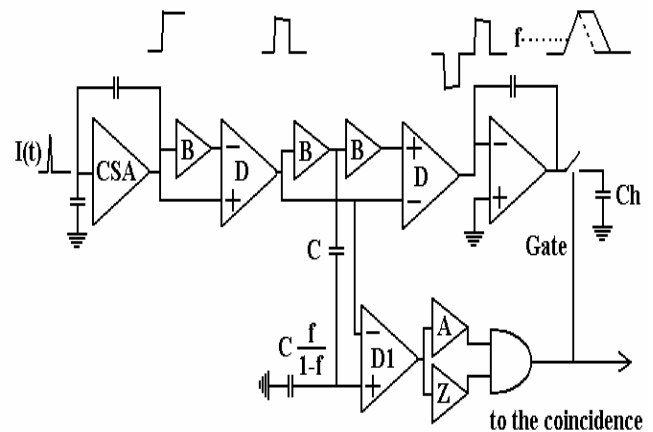


Figure 4 – On-chip realization of the $(1-e^{-sT})$ operator
a) block diagram b) detailed circuit

The delay-based shaping concept sketched in figs 4a) and b) was proven to be adequately reliable. Within a given CMOS process, indeed, the delay obtained from the feedback unity-gain buffer is to be considered stable and reproducible to the extent required by the actual application.

C The architecture of the elementary cell

The complete architecture of the elementary cell is shown in fig.5. The signal at the output of the first shaper unit, the one implementing the $(1-e^{-sT})$ operator, splits along two lines. The upper one completes the shaping by introducing a second delay-line operator $(1-e^{-2sT})$ to multiply the first one. The resulting bipolar signal goes to an integrator which produces at its output a trapezoidal signal. Blocks **B** are unity gain



buffers, Z is the zero-crossing trigger and A the preset (arming) circuit.

Fig.5: Architecture of the complete elementary cell.

The lower signal path includes the constant-fraction trigger which provides the hit timing and the command of the switch in the upper line which charges the storage capacitor. The presence of a flat-top in the trapezoidal shaper and the timing accuracy of the constant fraction trigger guarantee that the ballistic errors and the amplitude loss in the storage operation be kept within very small limits. The signal provided by the constant fraction trigger and the trapezoidal integrator output are shown in fig. 6 a) and b).

C The timing circuit

The timing circuit is a constant fraction discriminator. Its implementation benefits from the delay-based approach adopted for the shaper. As shown in fig. 5, which describes the entire analog cell, its core is the multistage difference amplifier **D1**. This subtracts the signal at the output of the first shaper section, attenuated by the capacitive divider C, $Cf/(1-f)$, which defines the constant fraction f, from a signal taken from a node inside the second section of the shaper. The amplified difference signal features, by virtue of the large amplification it undergoes, a very steep slope at the crossover point, whose time of occurrence is detected by a zero-crossing discriminator to provide the time definition of the hit.

Particular design cares had to be taken to prevent that the high gain difference amplifier **D1** in fig.5 undergo a heavy overload in presence of a large input signal.

IV CIRCUIT BEHAVIOR

In the version which is being submitted now, the circuit of fig. 5 is intended for operation with values of the input charge ranging between 2×10^4 and 5×10^5 electrons.

The simulations have provided a thorough information about the circuit behavior, adding more support to the choice made of designing the shaper on the basis of the delay principle.

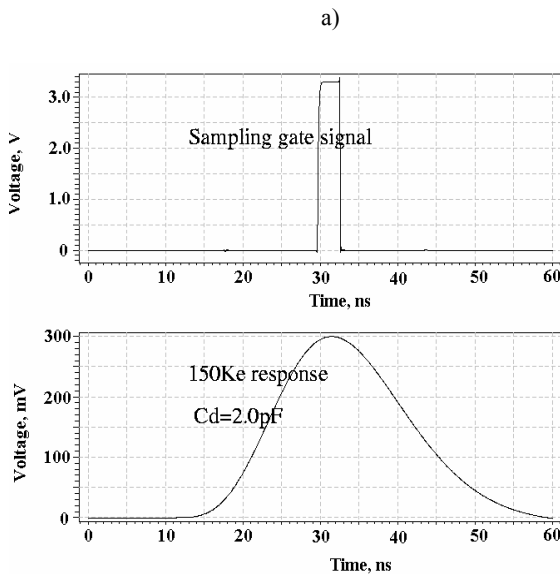


Fig.6: waveforms relevant to the elementary cell according to the simulations. a) gating signal provided by the timing circuit b) trapezoidal signal at the shaper output.

The analog signal obtained from the shaper in response to a δ -impulse detector current, shown in fig. 6b), approaches closely the trapezoidal waveform it aimed at. It has a well pronounced rounded top, which makes the sampling operation very accurate.

Besides, it has a very neat shape, with almost symmetric leading and trailing portions and features a regular, monotonic recovery to the baseline. This characteristics, associated with its short basewidth, about 45 ns according to fig.6b), makes the circuit suitable for operation at very high hit rates.

The signal shape of fig.6 b) is the same regardless of whether the charge-sensitive loop employs the larger or the smaller input transistor. This is due to the choice of the geometry and of the value of the standing currents which, as pointed out in sect II A, provides in either case a value of the transconductance which is proportional to the largest value of the detector capacitance foreseen for each configuration. This results in a preamplifier risetime which has a little dependence on the detector capacitances the cell is operating with, thus affecting the final shaped signal only to a negligible extent.

The logic signal of fig. 6 a) is the gating command provided by the timing circuitry. Comparison of the time relationship of figs. 6 a) and b) shows that the storage of the analog amplitude is achieved with a high degree of timing accuracy, in correspondence of the center of the rounded top of the analog signal.

The simulated noise behavior for the two versions of the cell was investigated with reference to the δ -response of fig. 6 b).

The cell employing the charge sensitive loop with the larger input transistor, $W/L=300/1$ operating at a 200 μ A standing current, features an equivalent noise charge ENC of 550 e rms at a 2pF detector capacitance.

The noise-induced time-resolution variance σ in the triggering instant of the timing circuit is plotted in fig. 7 as a function of the charge injected at the input by a delta-impulse.

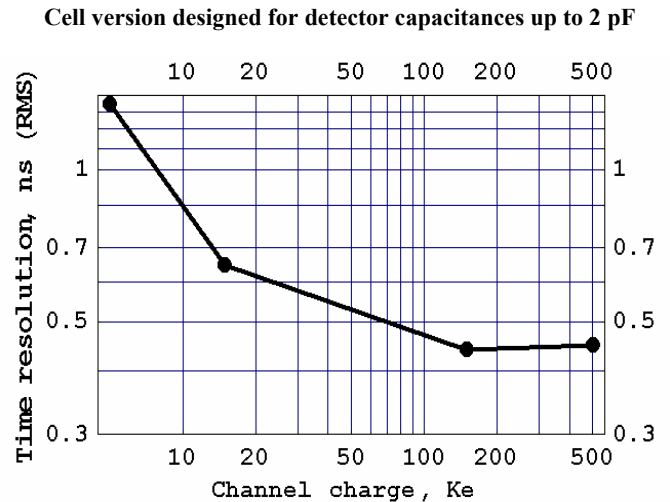


Figure 7: Noise-induced dispersion on the triggering instant of the timing circuit as a function of the charge injected at the preamplifier input by a δ -impulse.

The plot of fig.7 shows that the noise-induced dispersion of the triggering instant remains almost constant as soon as the input charge exceeds 2×10^4 electrons. This indirectly proves that the slope at the crossover point in the signal presented at the zero crossing discriminator has a high degree of independence from the value of the injected charge.

This independence results in a limited time walk which is less than 1ns over the entire range of input charge values, from 2×10^4 to 5×10^5 electrons.

The cell employing the charge sensitive loop with the smaller input transistor, $W/L=30/1$ operating at a $20 \mu A$ standing current, features an equivalent noise charge ENC of 240 e rms at a 0.2pF detector capacitance.

The noise-induced time-resolution variance σ in the triggering instant of the timing circuit is plotted in fig. 8 as a function of the charge injected at the input by a δ -impulse.

Cell version intended for detector capacitances up to 0.2 pF

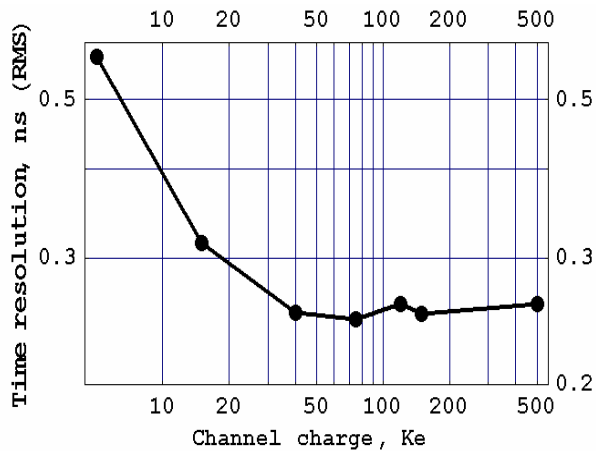


Figure 8: Noise-induced dispersion on the triggering instant of the timing circuit as a function of the charge injected at the preamplifier input by a δ -impulse.

Comparison between the curves of figs 7 and 8 shows that the values of the noise-induced dispersion in either version of the elementary cell are approximately proportional to the relevant ENC, which confirms that the values of the slope at the crossover point are independent of the geometrical features and standing current in the input device of the charge-sensitive loop. This is one more benefit of having designed the two versions with the criterion of having the same transconductance and the same feedback capacitance in the charge-sensitive loop.

The static power dissipation in the cell designed for larger capacitances, whose input device operates at a larger current is

About 3mW. As the only difference between the two cells is in the input device, the static power dissipation in the cell designed for smaller capacitances is slightly less, as determined by the difference in the input transistor current ($20 \mu A$ against $200 \mu A$). Considering the outstanding noise and timing performances of the cell, the above power levels are fully satisfactory. A substantial power reduction could be achieved by relaxing the request of a low noise charge acquisition at such a short shaping time as 50 ns.

V CONCLUSION

A monolithic readout system for highly segmented radiation detectors is being developed on the basis of an elementary cell based upon advanced design concepts.

The system stores the value of the charge associated with the detector signals to allow position evaluation by charge interpolation. Besides, it performs an accurate determination of the time of occurrence of the signals.

The noise and counting rate characteristics as well as the timing accuracy are to a large extent to be attributed to the original approach adopted in the shapers that follow the charge-sensitive loop. This approach consists in transferring onto a silicon chip the concept of trapezoidal shaping which in a discrete circuit realization would rely upon delay lines.

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