**Title**
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**Publication Date**
1960

UCRL 9046

UNIVERSITY OF CALIFORNIA

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# Radiation Laboratory

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UCRL-9046
Instruments UC-37
TID-4500 (15th Ed.)

UNIVERSITY OF CALIFORNIA

Lawrence Radiation Laboratory
Berkeley, California

Contract No. W-7405-eng-48

# DESIGN LIMITATIONS OF A BREAKDOWN DIODE COUPLED TRANSISTOR FLIP FLOP

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(Thesis)

January 1960

Printed for the U. S. Atomic Energy Commission

Printed in USA. Price $1.50. Available from the
Office of Technical Services
U. S. Department of Commerce
Washington 25, D.C.

## ABSTRACT

It is well known that the output characteristics of collector coupled transistor flip flops (Eccles Jordan type of circuit) may be stabilized by the addition of clamping diodes to the output circuit. The work presented shows that with a saturating type of flip flop this same clamping action may be accomplished with a single double-base breakdown-diode placed between the collectors of the two transistors. The advantage of such a method of clamping lies in its simplicity, as only three solid state components are necessary; one double-base breakdown-diode and two transistors. The switching time of such a flip flop is comparable with other types of saturated flip flops as the type of clamping has little effect upon switching time. The noise generated by breakdown-diodes ranges from a few m. v. to a few hundred m. v., and is considerably greater than the noise generated by a standard diode. Consequently breakdown-diode clamping should not be used where noise is likely to be a serious problem.

switching, thus the actual current switched is the same in both circuits. The second circuit has the clamping diodes and power supply as before, but in addition the transistors are prevented from saturating by the addition of two more diodes and another power supply. This circuit will have decreased switching times for the transistors never reach saturation, but the number of diodes and power supplies required is increased.

J. G. Linvill[2] has used double-base breakdown-diodes between the collectors of a collector and emitter coupled non-saturating F/F. This arrangement stabilizes the collector voltage swing of the F/F, but it does not stabilize the collector voltage swing with respect to circuit ground. If the transistors are allowed to saturate, and grounded emitter transistors are used, the collector voltage swings are then given a stable reference to ground.

When using breakdown-diode clamping, collector triggering is accomplished by replacing the double-base breakdown-diode with two single-base breakdown-diodes, and applying the trigger signal between the two diodes. This same type of triggering is obtained with the standard diode clamped collector coupled F/F (Fig. 2.5), by placing a third diode in the power supply lead of the clamping circuit and applying the trigger signal at the junction of all three diodes.

In circuits where noise is a problem breakdown-diodes may not give satisfactory service for their noise level is much greater than a normal diode. The noise is greatest at low diode currents, decreasing as the diode current increases. The level of the noise will vary greatly, ranging from a few m. v. to a few hundred m. v. .

# CHAPTER II

## INTERNAL FLIP-FLOP OPERATION

### INTRODUCTION

In this chapter the F/F will be described in a qualitative manner. This will be done without the aid of mathematical analysis, for here, only the more general aspects of the circuit are of interest. The first part of the chapter will be devoted to a description of the static characteristics, including a discussion of the external characteristics and power dissipation of the F/F. Following this is a description of the dynamic operation.

For convenience pnp transistors will be assumed in all discussions. This is done to simplify the discussions as the same arguments apply equally well for both pnp and npn types of transistors.

### STATIC CONDITIONS

The operation of this F/F is comparable to a breakdown-diode regulator circuit (Fig. 2.1) in many respects. The characteristics of the regulator circuit are much more dependent upon the characteristics of the breakdown -diode than the power supply voltage and impedance, because the breakdown-resistance of the breakdown-diode is very low (ideally zero). The F/F has two such possible regulator circuits depending upon which state the F/F is in. If transistor $T_1$ is saturated and transistor $T_2$ cut-off (Fig. 2.2), the regulator is formed by resistance $R_1$ and breakdown-diode $D_1$. The output voltage of the transistor's regulator circuit ($V_{o1}$) is negative and is equal to the breakdown-voltage of the breakdown-diode while the other output voltage ($V_{o2}$) is held at ground potential by the saturated transistor $T_1$. In the other stable state (transistor $T_2$ saturated and transistor $T_1$ cut-off) the regulator circuit is formed by resistance $R_2$ and breakdown-diode $D_2$, and the output of the transistor's regulator circuit is voltage $V_{o2}$.

In a bi-stable F/F of this type the d-c cross collector coupling maintains the F/F in either of its two stable states. For example, if transistor $T_1$ were saturated (Fig. 2.2), the voltage $V_{o1}$ would be at its most negative value, and the base-current of transistor $T_1$ would be drawn through diode $D_3$ and resistance $R_3$ to node $V_{o1}$. The amount of this base-current is approximately the node voltage $V_{o1}$ divided by the resistance $R_3$, neglecting the offset voltages of diode $D_3$ and the base-emitter junction of transistor $T_1$. Transistor $T_2$ is held off during this period by the action of diode $D_4$. This diode is a silicon diode, while transistor $T_2$ is a germanium transistor; thus the diode has a greater offset voltage than the transistor. This will leave the base-emitter junction of transistor $T_2$ back-biased; consequently, cut-off, when the voltage $V_{o2}$ is near ground potential. In the supplementary circuit (Fig. 2.3) this back-bias is obtained by the action of the voltage dividers $R_3$, $R_5$ and $R_4$, $R_6$.

The circuit using the diodes $D_3$ and $D_4$ (Fig. 2.2) has the advantage that only one power supply is required, where the supplementary circuit (Fig. 2.3) requires a second power supply for its voltage divider network. On the other hand, the supplementary circuit is cheaper; for two resistors and a common power supply replace two diodes. The circuit using the diodes is a little faster than the supplementary circuit because the base-emitter junction will never be as far back-biased. (This will be explained more fully in the next section on "Dynamic Conditions".) Both of these circuits have advantages and disadvantages; the proper choice will depend ultimately upon the particular situation being considered.

## EXTERNAL CHARACTERISTICS

The most desirable feature of this F/F are its simplicity and very

stable output characteristics, while the major disadvantage is its high cost, due to the use of a double-base breakdown-diode ($3.00-$10.00). At the sacrifice of slightly degrading the output characteristics and simplicity the high cost may be reduced if the double-base breakdown-diode is replaced with clamping diodes and a power supply (Fig. 2.6).

Simplicity is achieved by allowing the transistors to saturate, and by using a double-base breakdown-diode. Saturation allows for greater utilization of the transistor characteristics than other types of non-saturating F/F's by removing the need for clamping diodes in the "on" state. The double-base breakdown-diode replaces the two clamping diodes and power supply (Fig. 2.6) needed to provide a stable negative state of the F/F. Only one power supply is required for the F/F (Fig. 2.2). If the need or advantages of a reduced number of power supplies is not great, a reduction in costs may be obtained by increasing the number of power supplies. The supplementary circuit of Fig. 2.3 uses two power supplies while the circuit of Fig. 2.6 requires three.

The stable output characteristics of this F/F are a result of the combined action of the saturated transistors and the double-base breakdown-diode. Through their action both states of the F/F exhibit a low output impedance and an output voltage that is nearly independent of F/F toleranancing, power supply variations, and load changes.

The output characteristics are represented by the equivalent circuit of Fig. 2.4. Fig. 2.4-A shows the F/F in a stable state (Transistor $T_1$ saturated and transistor $T_2$ cut-off), and Fig. 2.4-B gives an approximate equivalent circuit for the two output voltages $V_{o1}$ and $V_{o2}$. In these two circuits $R_{s1}$ is the saturation resistance of transistor $T_1$, $R_b$ is the breakdown-resistance of the breakdown-diode, and $V_b$ is the breakdown-voltage of the breakdown-diode. The saturation resistance $R_{s1}$ is

normally small (5 to 10 ohms is typical for deep saturation) while the breakdown resistance ($R_b$) will range from a few ohms to fifty ohms, depending upon the particular breakdown-diode used. Since $R_{sl}$ and $R_b$ are both small the output impedance of both stable states is very small ($R_{sl}$ or $R_{sl}$ plus $R_b$). The output voltage $V_{ol}$ is primarily determined by $V_b$ (Fig. 2.4), for the IR drops across $R_{sl}$ and $R_b$ are small, thus the output voltage must be very stable as the breakdown-voltage ($V_b$) is not subject to change.

The breakdown-resistance ($R_b$) may be controlled by the designer as the resistance of an individual diode is fairly stable with time. However, a wide variation exists between individual diodes of the same type so that some upper limit must be set on the breakdown-resistance. Normally it is possible to use the upper limit set by the manufacturers for this.

## POWER DISSIPATION

The efficiency of the F/F will be determined by the type of load it must drive. If the load requires large currents from the most negative output state of the F/F the power dissipated will be high due to the characteristics of the breakdown-diode regulator circuit. If load current is only supplied from the ground state, the power dissipation will be low, for this current is supplied through a saturated transistor.

The same factors effect the efficiency of the F/F as effect the efficiency of the regulator circuit (Fig. 2.1). In such a regulator circuit, regulation is achieved by wasting power. There is a fixed power loss in the regulator resistance (Fig. 2.1), while the power loss in the breakdown-diode is variable. The sum of this variable power loss and the load power is always a constant, thus the total power supplied to the system is likewise constant. The most negative output of the F/F is similar to the output

of the regulator circuit; consequently, if large currents must be supplied to the load, the dissipation of the regulator will have to be increased. This entails making resistors $R_1$ and $R_2$ small (this is also a requirement for high speed operation), and using a breakdown-diode with a high power rating. If the large load currents are supplied from the ground state of the F/F, the power dissipation may be made quite small, as this does not require increasing the power dissipation of the regulator circuits, for the load current is supplied through the saturated transistor.

The power dissipation of the transistors is quite small as the transistors are operated in deep saturation, or cut-off at all times. At low repetition rates, the power dissipation of the saturated transistor is an $I^2R$ loss (where R is the saturation resistance of the transistor). At very high repetition rates, however, the power dissipation is increased, due to the high power dissipation during the switching transient. One of the advantages of using saturated transistors is that a greater amount of power can be handled with the same transistor than when the transistor is non-saturating.

## DYNAMIC CONDITIONS

The details of a change of state will now be examined to show the sequence of events that take place during switching. In a direct coupled F/F of this type, it is necessary to steer the driving current to the cut-off transistor. The cut-off transistor ($T_2$ in Fig. 2.3) is driven into its active region by application of driving current $I_{x2}$. Actually there is a short time delay before the active region is reached because initially the transistor is reverse biased. This reverse bias must be overcome by the driving current flowing into the coupling capacitor until the base voltage has changed enough to forward bias the transistor; at this point the transistor enters its active region of operation.

This time delay may be shortened by decreasing the size of the coupling capacitor, by increasing the amount of driving current, or by designing the circuit so that the required change in base-voltage is small. It is the latter possibility that makes the supplementary circuit (Fig. 2.3) slower than the circuit of Fig. 2.2, for with the supplementary circuit a greater reverse bias is required in order to allow for the necessary tolerance of the voltage divider. With the diode circuit (Fig. 2.2), however, the reverse-base voltage is very small (a few tenths of a volt) thus the change in base voltage required to forward bias the transistor is less than with the supplementary circuit.

Once the base-voltage ($V_2$) has decreased sufficiently it will be clamped by the forward-biased base-emitter junction of transistor $T_2$. With transistor $T_2$ biased into the active region, its collector current ($I_{c2}$) begins to increase, while the current through the breakdown-diode decreases by a like amount. During this period, there is no change in the collector voltage $V_{o1}$, because there is no change in the net current supplied to node $V_{o1}$. Reduction of the breakdown-diode current produces an equal decrease in the saturation collector current of transistor $T_1$ ($I_{c1}$). This is a desirable effect, for it shortens the time delay due to excess carrier storage in transistor $T_1$. As the collector current of transistor $T_2$ is increased still further, the breakdown-diode current eventually reaches zero. At this point, the breakdown-diode cuts-off (changes to a state of very high impedance) thus producing an open circuit between collectors.

Once the breakdown-diode cuts-off further increase in the collector current of transistor $T_2$ cause a corresponding decrease in the base current of the saturated transistor $T_1$, until the saturated transistor is driven

out of saturation to the edge of its active region. At this point both transistors are in their active regions of operation and the circuit will regenerate.

Regeneration takes place under nearly constant voltage conditions, i.e., the change in voltage across the coupling capacitors is small during the regeneration period, consequently at the end of regeneration the collector voltage of transistor $T_1$ ($V_{o2}$) has changed very little and will now start to decay toward the collector power supply on a RC time constant determined by the coupling capacitance and the load resistance of the collector circuit in series with the base resistance of the going "on" transistor $T_2$. When this voltage decays far enough the breakdown diode conducts thus clamping the collector voltage.

The collector voltage of the going "on" transistor $T_2$ will be driven toward ground potential primarly by the driving signal, for when saturated operation is used the driving signal is normally fairly large. In cases where the driving signal is not large this voltage is also driven toward ground potential by the going "off" transistor; the drive in this case being the charging of the other coupling condenser through the base of the going "on" transistor $T_2$.

# CHAPTER III

## ANALYSIS OF SWITCHING TIME

### INTRODUCTION

The object of this chapter is to determine the switching time of the F/F when triggering energy is supplied to the base of the cut-off transistor. When saturation is allowed, the transistors must pass through a non-linear region into a new region of linear operation. This type of operation is impossible, or at best very difficult, to handle analytically without the aid of a computer, and even this approach yields only specific solutions, which are of little value to the circuit designer. To overcome this difficulty a piece-wise-linear analysis has been used where the operation of the F/F is broken into a number of small linear segments each of which may be analyzed separately. When passing from one linear region to another the boundary conditions must be carried along in order to establish the initial conditions for the new region of linear operation. A delay time will be found for each linear region of operation by this piece-wise-linear method, and from these the total switching time of the F/F will be simply the sum of the individual delay times.

The detailed analysis will be made using the F/F circuit shown in Fig. 2.2. It will be assumed that a steady state condition has been reached before switching is started, and that Fig. 2.4-A represents the F/F in its steady state condition (transistor $T_1$ saturated and transistor $T_2$ cut-off). In this equivalent circuit the saturated transistor is represented by its saturation resistance, $R_{s1}$, while the cut-off transistor is represented by an open circuit. Switching is initiated by removing current from the base of the cut-off transistor $T_2$.

## TIME DELAY $t_1$

When driving-current, $I_{x2}$, is first applied the base voltage, $V_2$, of transistor $T_2$ will have to change by some small amount, $\Delta V_2$, before transistor $T_2$ is biased into the active-region of operation. There will be a time delay, $t_1$, associated with this change in base voltage since current must first be supplied to capacitor $C_4$. As the time-constant of $C_4R_4$ is large in relation to the delay time $t_1$ nearly all the driving current is supplied through $C_4$.

The time delay may be expressed through a simple charge balance if the driving-current is supplied under constant current conditions. As long as the time delay, $t_1$, is small in comparison with the time constant formed by the resistance of the driving circuit and capacitor $C_4$, the assumption of a constant current drive is valid. With these assumptions the charge supplied to $C_4$ must equal the charge supplied to the F/F from the driving circuit, consequently the time delay is

$$t_1 = \frac{\Delta V_2 \, C_4}{I_{x2}} \qquad (3.1)$$

$t_1$ will be in units of $m\mu$ seconds if $\Delta V_2$ is expressed in volts, $C_4$ is $\mu\mu f$, and $I_{x2}$ is m. a..

## TIME DELAY $t_2$

At the end of delay time $t_1$ transistor $T_2$ is just biased into its active region of operation. Delay time $t_2$ will start at this point and end when the breakdown-diode cuts-off. Since during this period the decrease in the breakdown-diode current is equal to the increase in collector current of transistor $T_2$ there is very little change in the node voltage $V_{o1}$, for the net current into the node is constant. To find the delay time $t_2$ the F/F

is represented by the equivalent circuit shown in Fig. 3.1. In this equivalent circuit $R_{s1}$, $R_b$, $V_b$, and $C_4$ are the same as in the previous equivalent circuit (Fig. 2.4-A). The resistances $R_{B2}$ and $R_e$ are the base and emitter resistances of transistor $T_2$, and $\alpha(s)$ is the dominant pole alpha of transistor $T_2$. (See Appendix I for a discussion of a dominant pole transistor equivalent circuit.) The shunt path consisting of diode $D_4$ and resistance $R_4$ (Fig. 2.2) has been omitted for the current though it is negligibly small in comparison with the current through $C_4$.

Delay time $t_2$ is found by solving the equivalent circuit of Fig. 3.1 for a step input of drive current ($I_{x2}$), and finding the time necessary for the collector current to build up sufficiently to unclamp the collector by driving the current of the breakdown-diode to zero, thus cutting-off the breakdown-diode. This work has been carried out in Appendix II where it is found that

$$t_2 \approx \frac{1 + D}{\omega_T} \quad \frac{I_d}{I_{x2}} \tag{3.2}$$

under the conditions that

$$\beta \gg 1$$

$$\beta I_{x2} \gg I_d$$

In these expressions

$I_d$ - Steady state breakdown-diode current.

$I_{x2}$ - Driving current.

$\omega_T$ - Measured alpha cut-off frequency of the transistor.

D - Loss factor given by

$$D = \omega_T C_4 \left\{ r_e + r_{b(1-\alpha_o)} + r_{s1} \right\}$$

## DELAY TIME $t_3$ (Saturation Delay)

The saturation delay time ($t_3$) is the time necessary to drive the saturated transistor to the edge of its active region once the breakdown-diode has been cut-off. The method of solution is to first determine the base current of the saturated transistor as a function of the collector current of the driving "on" transistor. Once this is found the response of the transistors is added, thus giving the response of the hypothetical collector current of the saturated transistor as a function of the drive current. This hypothetical collector current is the collector current that would flow in the saturated transistor if it were not in saturation, and is given by

$$I_{c1}(h) = I_{B1}(sat)\,\beta_1$$

where $I_{B1}$ is the base current of the saturated transistor and $\beta_1$ its common emitter current gain at zero collector voltage. When the hypothetical collector current decreases to the actual saturation collector current regeneration begins, thus ending the saturation delay period. The change in collector current during the saturation delay period is

$$\Delta I_{c1} = I_{B1}(sat)\,\beta_1 - I_{c1}(sat)$$

The details of this calculation have been carried out in appendix III and will not be repeated here. In making the calculations each transistor is represented by a simple one pole expression. When the saturation delay is small in relation to the dominant time constants of the circuit the saturation delay is found in appendix III to be

$$t_3 \approx \sqrt{\frac{2\left\{I_{B1}(sat)\ \beta_1 - I_{c1}(sat)\right\}}{H\left\{K_1 P_1^{\,2} + K_2 P_2^{\,2} + K_3 P_3^{\,2}\right\}}} \qquad (3.3)$$

where

$P_1$ is pole due to the coupling circuit of the F/F.

$$P_1 = \frac{1}{C_3 + \dfrac{CL}{1 + \dfrac{R_{B1}}{R_L}}} \left\{ \frac{1}{R_3} + \frac{1}{R_{B1} + R_L} \right\}$$

$P_2$ is the pole due to the driving on transistor.

$$P_2 = \frac{\omega_B}{1 + D'}$$

$P_3$ is the pole due to the saturated transistor.

$$P_3 = \frac{\omega_n \omega_i}{\omega_n + \omega_i} \quad (i - \alpha_n \alpha_i)$$

here $\omega_n$ and $\omega_i$ are the forward and reverse alpha cut-off frequencies of the saturated transistor, and $\alpha_n$ and $\alpha_i$ are the d-c alphas in the forward and reverse direction, taken at zero collector voltage.

$$H = \frac{I_{x1}\ \beta_1\ \beta_2\ P_2\ P_3}{1 + \dfrac{CL}{C_3} + \dfrac{R_{B1}}{R_L}}$$

$$K_1 = \frac{P_1 - Z_1}{P_1\,(P_2 - P_1)(P_3 - P_1)}$$

$$K_2 = \frac{P_2 - Z_1}{P_2(P_1 - P_2)(P_3 - P_2)}$$

$$K_3 = \frac{P_3 - Z_1}{P_3 (P_1 - P_3)(P_2 - P_3)}$$

DELAY TIME $t_4$ (The regeneration period)

Regeneration begins at the end of the saturation delay period for at this time the going "off" transistor is biased at the edge of its active region, thus giving the circuit a pole in the right half plane.

A first order estimate of the regeneration time may be obtained by applying the results of D. O. Pedersons[3] paper on the regeneration time of a non-saturated F/F. This work applies to the case of minimum external drive, and consequently will set an upper limit on the regeneration time, as any drive greater than the minimum will decrease the regeneration time. The regeneration time $t_4$ from Pederson's formulation is

$$t_4 = \frac{1}{(2\alpha_o - 1)P_o - P_c} \ln \frac{2 P_o}{(1 - \alpha_o)P_c} \qquad (3.4)$$

where $$P_c = \frac{G_c + \alpha_o P_o C_c}{C_1} \qquad (3.5)$$

$P_o$ = Measured alpha cut-off frequency of the transistor.

$\alpha_o$ = Average d-c common base current gain.

$G_c$ = Total collector conductance.

$C_1$ = Coupling capacitance of the F/F.

$C_c$ = Collector capacitance of the transistor.

$g_b$ = Base conductance of the transistor.

For the regeneration time given by equation 3.4 to be valid requires the following conditions to be met:

$$g_b \gg G_c + \alpha_o P_o C_c \qquad (3.6)$$

$$C_1 \gg C_c \qquad (3.7)$$

$$(2\alpha_o - 1) P_o > P_c \qquad (3.8)$$

The voltage drop across the coupling capacitors is assumed negligibly small in the development of the regeneration time expression. Actually there is quite a considerable voltage drop in the coupling capacitor supplying current to the saturated transistor, but this drop is due to the driving signal r ather than to the regeneration process. So far as the regeneration process is concenred this voltage drop does not constitute a loss in loop gain, but rather an increase in loop gain, for as the driving signal is increased the regeneration time is decreased. Consequently the regeneration time found from equation 3.4 will be an upper limit on the regeneration time.

DELAY TIME $t_5$ (Collector Voltage Recovery)

Delay time $t_4$ is the time necessary for the collector voltage of the now cut-off transistor ($T_2$) to fall to the breakdown-voltage of the breakdown-diode. Since regeneration takes place so fast in relation to the RC time constant of the collector circuit there is very little change in the collector voltage during the regeneration period. Consequently after regeneration the collector voltage will decay toward the collector power supply voltage on a simple RC time constant, where R is the total load resistance in series with the base resistance of the going "on" transistor, and C is the combined capacitance of the coupling capacitance and any stray circuit capacitance. This time delay is given by

$$t_5 = (R_L + rb)(C_L + C_3) \ln \frac{|V_s|}{|V_s| - |V_b|} \qquad (3.9)$$

where

$R_L$ = Collector load resistance.

rb = Base resistance of the going "on" transistor.

$V_s$ = Collector power supply voltage.

$V_b$ = Breakdown voltage of the breakdown-diode.

$C_3$ = Coupling capacitance.

$C_L$ = Stray load capacitance.

# CHAPTER IV

# DESIGN INFORMATION

## INTRODUCTION

In this chapter design information will be presented that should give a good grasp of the major design problems involved. As always with this type of problem it is neither worthwhile or possible to give a one, two, three, plug in the numbers, type of universal design procedures, for every designer has his own specific problems and design criteria that he must meet. The design problems of the F/F must be considered and weighed with the overall system problem before it is possible to arrive at a good design criteria, for a good design is a balanced design.

## DESIGN OF THE STATIC LOAD CIRCUIT

The static load circuit (Fig. 4.1) consists of a breakdown-diode regulator circuit where $E_{cc1}$ is the supply voltage, $R_1$ the supply resistance, $R_o$ the load resistance, and $V_b$ the breakdown-voltage. The saturation resistance $R_{s1}$ appears in series with the breakdown-resistance $R_b$ of the breakdown-diode. This equivalent circuit applies to the case when transistor $T_1$ is saturated and transistor $T_2$ is in its cut-off condition. Fig. 4.1b is the same as Fig. 4.1a, but in Fig. 4.1b $E_{cc1}$, $R_1$, and $R_o$ have been replaced by their Theven equivalent. In order to allow the breakdown-diode to operate it is necessary for

$$E_{cc1} \frac{R_o}{R_o + R_1} = NV_b \qquad (4.1)$$

where N is larger than one. If this condition were not met the node voltage $V_{o1}$ could not raise sufficiently to allow the diode to break-down; when N is large, the normal condition for a fast circuit, the delay time $t_4$ is reduced, as will be shown a little later.

In a circuit of this type power supply $E_{cc1}$ and resistance $R_1$ furnish current $I_s$

$$I_s = \frac{E_{cc1} - V_b}{R_1} \tag{4.2}$$

that is divided between the load (i.e., $I_L$ flowing through $R_o$) and the breakdown-diode. Since only current $I_L$ is useful for driving a load it should be maximized, while the breakdown-diode current $I_D$ should be minimized so that low power diodes may be used. When the circuit is switched, transistor $T_2$ must supply enought current ($I_{c2(max)}$ to node $V_{o1}$ to drive the node voltage to zero. This current may be given by

$$I_{c2(max)} = \frac{E_{cc1}}{R_1} \tag{4.3}$$

where $I_{c2(max)}$ is supplied by transistor $T_2$. The maximum value of $I_{c2(max)}$ will be determined by the maximum pulse current of the transistor, or if the repetition rate is high by the power dissipation of the transistor. In either case $I_{c2(max)}$ is limited by the transistor, not the load circuit, so that it must be used as a design limit.

To maximize the load current $I_L$ with a limited transistor current $I_{c2(max)}$ the current $I_s$ should be large, and as nearly equal to $I_{c2(max)}$ as possible. Combining equations 4.1, 4.2, and 4.3

$$I_s = I_{c2(max)} \left(1 - \frac{V_b}{E_{cc1}}\right) \tag{4.4}$$

it is seen that $I_s$ approaches $I_{c2(max)}$ as $E_{cc1}$ approaches infinity. Consequently the ideal case would be to replace power supply $E_{cc1}$ and resistance $R_1$ by a current source. This is not normally feasible, but it is possible to make the supply voltage $E_{cc1}$ large, thus approaching a true current source.

The static circuit may now be designed by specifying the maximum transistor collector current ($I_{c2}(max)$), the power supply voltage ($E_{cc1}$), the breakdown-diode voltage ($V_b$), and the recovery-factor N. With these terms the remaining circuit quanities are given by

$$R_1 = \frac{E_{cc1}}{I_{c2}(max)} \tag{4.5}$$

$$R_o = \frac{1}{I_{c2}(max)\left(\frac{1}{NV_b} - \frac{1}{E_{cc1}}\right)} \tag{4.6}$$

$$I_L = I_{c2}(max)\left(1/N - \frac{V_b}{E_{cc1}}\right) \tag{4.7}$$

$$I_D = I_{c2}(max)\,(1 - 1/N) \tag{4.8}$$

$$I_x = \frac{I_{c2}(max)}{\beta_2} \tag{4.9}$$

The stacking ratio (S), the number of similar F/F that can be driven by one F/F, may be found by subtracting the saturated transistors hold on current $V_b/R_3$ from the load current $I_L$ and dividing by the driving current $I_x$. Thus

$$S = \frac{I_L - V_b/R_3}{I_x} \tag{4.10}$$

Simplifying equation 4.10 and introducing the over-drive factor (K) (the ratio of the actual drive to the minimum possible drive current) gives

$$S = \frac{\beta_2}{K}\left[\frac{1}{N} - \frac{V_b}{E_{cc1}}\left(1 + \frac{R_1}{R_3}\right)\right] \tag{4.11}$$

Figure 4.2, derived from equation 4.7, is a plot of the load current $I_L / I_{c2}(max)$ as a function of the recovery factor N and the voltage

ratio of the breakdown voltage $V_b$ to the power supply voltage $E_{ccl}$. This figure may also be used to obtain a first order approximation to the stacking ratio (S) when the hold-on current of the saturated transistor is the same as the driving current ($I_x$) of the F/F.

$$S = \frac{\beta_2}{K} \frac{I_L}{I_{c2}(max)} - 1 \qquad (4.12)$$

The value of $I_L/I_{c2}(max)$ may be taken directly from figure 4.2 and used in equations 4.12. Even when the hold on current isn't exactly equal to the drive current, equation 4.12 may still be used as a first order approximation to the stacking ratio.

## DYNAMIC CONSIDERATIONS IN THE DESIGN OF THE LOAD CIRCUITS

In this section the various delay times will be expressed in terms of the design quanities $I_c(max)$, $V_b$, $E_{ccl}$, and N, as well as the cut-off frequency of the transistors. With this information it is then possible to proportion the various delays to fit a particular application.

Delay time $t_1$ is given by equation 3.1. $\Delta V2$ in this expression is due to current supplied through $R_5$ flowing through the hold on resistance $R_3$. The drive current $I_x$ may be expressed as

$$I_x = \frac{K\, I_c(max)}{\beta} \qquad (4.13)$$

where K is the overdrive factor, $I_c(max)$ the maximum transistor collector current, and $\beta$ the minimum beta. Expressing $t_1$ in these new terms gives

$$t_1 = \frac{C_4\ R_3\ E_{bbl}\ \beta}{K\ R_5\ I_c(max)} \qquad (4.14)$$

Delay time $t_2$ from equation 3.2 may be combined with equation 4.7 and 4.9 to give

$$t_2 = \frac{1 + D}{\omega \alpha} \frac{\beta}{K} (1 - 1/N) \qquad (4.15)$$

where $\omega_\alpha$ is the alpha cut-off frequency of the transistors and D the loss factor of the transistors given by

$$D = \omega_\alpha C_4 ( r_e + r_{s1} + r_b(1 - \alpha_o) ) \tag{4.16}$$

Delay time $t_2$ is reduced by decreasing the recovery factor N, for as N is decreased the breakdown-diode current decreases.

The recovery time $t_5$ equation 3.9 may be expressed as

$$t_5 = \left(\frac{C_3 + C_L}{I_{c(max)}}\right) V_b \left(N \ln \frac{N}{N - 1}\right) \tag{4.17}$$

where $C_3$ is the coupling capacitor (Fig. 2.2) and $C_L$ is the stray load capacitance. The effect of the recovery factor N on the recovery time is plotted in Figure 4.3. It may be seen from this figure that the useful range of N lies between 1.2 and 2. If N is too small the recovery time is excessive and is subject to large changes with small changes in the circuit tolerances, while if it is too large the stacking ratio will be severely reduced as can be seen from Equation 4.12 and Figure 4.2.

## SELECTION OF THE COUPLING CAPACITORS ($C_3$ and $C_4$)

The coupling capacitors store charge that is used to drive the saturated transistors out of saturation. If these capacitors are too small the storage delay of the transistors will be excessive, and if they are too large the collector RC time-constant will be excessively large, and the initial delay time $t_1$ will be increased in circuits employing high repetition rates.

The method chosen of approaching this problem will be that presented by Moody[4] where the amount of stored charge in the base region of the saturated transistor is determined from the intrinsic transistor equations of Ebers

and Moll.[5] Since this stored charge is removed by the application of reverse base current flowing through the coupling capacitor the coupling capacitor must hold at least as much charge as is stored in the base region of the saturated transistor. As the saturation delay time is normally small in comparison with the RC time-constant formed by the coupling capacitors ($C_3$ and $C_4$) and the hold on resistance ($R_3$ or $R_4$) nearly all the reverse base current is supplied through the coupling capacitors. Consequently a first order approximation for the coupling capacitors is found by using a capacitor that holds the same amount of charge that is stored in the base region of the saturated transistor. The stored charge in the base region is given by

$$Q_s = \frac{\beta_n}{\omega_n}\left(I_b \frac{1+\frac{\omega_n}{\omega_i}}{1+\frac{\beta_n}{\beta_i}} + I_e \frac{1-\frac{\beta_i \omega_n}{\beta_n \omega_i}}{\beta_n + \beta_i}\right) \qquad (4.18)$$

where $\omega_n$ and $\omega_i$ are the normal and inverted alpha cut-off frequencies; $\beta_n$ and $\beta_i$ the normal and inverted common emitter current gains; $I_b$ and $I_e$ are the steady state base and emitter currents just before switching starts. The charge stored in the coupling capacitor is determined by the breakdown voltage $V_b$, and is given by

$$Q = C_3 V_b \qquad (4.19)$$

Combining the last two equations and solving for the coupling capacitances gives

$$C_3 = \frac{\beta_n}{n V_b}\left(I_b \frac{1+\frac{\omega_n}{\omega_i}}{1+\frac{\beta_n}{\beta_i}} + I_e \frac{1-\frac{\beta_i \omega_n}{\beta_n \omega_i}}{\beta_n + \beta_i}\right) \qquad (4.20)$$

Examination of equation 4.20 shows the importance of using as small a hold-on

base current as possible for the coefficient associated with $I_b$ is considerably larger than the coefficient of $I_e$. For RCA 2N219 transistors the stored charge due to a hold-on base current of one ma is responsible for 70% to 80% of the total stored charge when the emitter current is 13 ma.

As the selection of coupling capacitance effects nearly all the delays of the F/F its choice is very important. For a thorough treatment of the subject the reader is refered to

thesis on

SELECTION OF THE STEADY STATE HOLD ON CURRENT

In order to take full advantage of the low saturation resistance of the transistors it is necessary to use fairly large base currents (i.e., around 1/2 ma or so) in order to keep the saturation resistance low (i.e., around ten ohms). On the other hand excess saturation increases the charge stored in the base region of the saturated transistor, thus requiring the use of large coupling capacitors which are necessary to drive the transistors out of saturation rapidly. The saturation resistance may be found from Ebers and Molls[5] model of an intrinsic transistor. Thus

$$r_s = \frac{kT}{q} \frac{1 - \alpha_i}{\alpha_n \alpha_i} \frac{1}{I_b} \qquad (4.21)$$

where $\alpha_n$ and $\alpha_i$ are the normal and inverted low frequency alpha, and $I_b$ is the steady state base current. $r_s$ the saturation resistance is the small signal resistance as seen between the collector and emitter terminals. If $I_b$ is expressed in ma, then $r_s$ will be in ohms and kT/q is about 25 at room temperature. The actual measured value of $r_s$ will be larger than that given by equation 4.21 by the amount of the ohmic contact resistance of the collector and emitter junctions. Normally this ohmic resistance is less than a few ohms so that equation 4.21 gives a good approximation for base currents of less than a few ma.

Figure 4.4 is a plot of equation 4.21 for RCA 2N219 transistors where $\alpha_n \alpha_i / 1-\alpha_i$ is around 5. For a base current of 1/2 ma the saturation resistance is about ten ohms, but also at this point the saturation resistance is still a very sensitive function to small changes in base current. If the base current is increased to one ma the saturation resistance is cut in half while its sensitivity to changes in base current is cut by a factor of four.

The output impedance of the F/F consists of the saturation resistance in one stable state, while in the other stable state the output impedance is the saturation resistance in series with the breakdown-resistance of the breakdown-diode. The saturation resistance also gives cross coupling between the two outputs, for a change in either load current produces a corresponding voltage change across the saturation resistance which is felt by both outputs. When low output impedance is required the choice of base current should be such as to keep the saturation resistance about the same order as that of the breakdown-diode or possibly a little smaller. Most breakdown-diodes have breakdown-resistances from a few ohms to fifty ohms or so, so the saturation resistance will need to be low (ten ohms was used for the 2N219).

## CHOICE OF $V_b$ (The breakdown-voltage of the breakdown-diode)

From equation 4.11 it is seen that lowering $V_b$ has the desirable effect of increasing the stacking ratio. On the other hand decreasing $V_b$ requires an increase in the coupling capacitance as can be seen from Equation 4.20. This increase in coupling capacitance does not change the collector circuits time-constant appreciably for as the coupling capacitance is increased the corresponding collector resistance is decreased. The collector circuits time constant may be given by

$$\tau_c = C_3 \frac{R_1 R_o}{R_1 + R_o} \qquad (4.22)$$

This expression may be expressed in the circuit design parameters as

$$\tau_c = \frac{N H}{I_{c(max)}} \tag{4.23}$$

where H is given by

$$H = \frac{\beta n}{\omega_n} \left( I_b \frac{1 + \frac{\omega_n}{\omega_i}}{1 + \frac{\beta n}{\beta i}} + I_e \frac{1 - \frac{\beta i \, \omega_n}{\beta n \, \omega_i}}{\beta n + \beta i} \right) \tag{4.24}$$

The important point of this discussion is that the collector circuits time-constant (Equation 4.24) is independent of the choice of $V_b$. In this discussion the stray load capacitance has been ignored. Since this stray capacitance is independent of the coupling capacitance or $V_b$ there is in reality some decrease in the collectors time-constant with decreasing $V_b$ due to the smaller equivalent load resistance ($R_1$ and $R_o$ is parallel).

As lowering the breakdown-voltage $V_b$ has only desirable effects the lower limit is set only by the circuit tolerancing. If $V_b$ becomes too low it becomes impossible to control the hold on current of the saturated transistor. This current is drawn through the base of the saturated transistor and then through the hold on resistance $R_3$ or $R_4$ (See Fig. 2.2). When the voltage across the hold on resistance becomes comparable with the base voltage ($V_1$) the hold on current is subject to wide variations due to the changes in the base-emitter characteristics of the saturated transistor. To overcome this the F/F should be designed so that the voltage drop across the hold-on resistance is several times larger than the base voltage of the saturated transistor; in this way reasonable control is maintained on the hold-on current.

# CHAPTER V

# RESULTS AND CONCLUSIONS

## EXPERIMENTAL PROCEDURE

The primary purpose of the experimental work undertaken has been to verify the delay times calculated previously. This was done by experimentally observing the step response of the F/F to a step of current applied to the base of the cut-off transistor. The delay times were then estimated from the step response oscillograms and checked against the calculated delay times.

The second phase of the experimental work was directed toward finding the maximum repetition rate of the F/F. This was done by connecting two similar units in a closed loop and observing the frequency of oscillation.

## DESIGN OF THE EXPERIMENTAL F/F

The F/F used in all experimental work was designed using RCA 2N219 transistors. These units are rated for a maximum collector current of 15 ma and have a normal Beta of 35 and an inverted Beta of 5. The normal alpha cut-off frequency is 8 mc while the inverted alpha cut-off frequency is 1.1 mc. Using a 45 volt power supply, 5.5 volt breakdown-diodes, and a recovery factor of 1.5 the circuit values are determined from equations 4.5 through 4.9. These values are

$R_1 = 3.1\ K^r$

$R_o = .67\ K^r$

$I_L = 8.2$ m.a.

$I_D = 5$ ma

$I_{x(min)} = 0.5$ ma

The steady state hold-on current must be at least as large as the minimum base current $I_{x(min)}$ of 0.5 ma in order to assure that the saturated

condition is maintained. During the course of the experimental work, a value of 0.8 ma was used for this steady state hold-on current.

For a stacking ratio of 2 the overdrive factor K is found from equation 4.11 to be 7.7. The coupling capacitors ($C_3$ and $C_4$) are found from equation 2.21 to be 120 $\mu\mu$f, but since this does not allow for any tolerancing in transistors a value of 150$\mu\mu$f was used in the actual circuit. The complete circuit is shown in Figure 5.1.

## EXPERIMENTAL RESULTS

The step response of the test circuit is shown by the oscillograms of Figure 5.2 and 5.3. The driving current ($I_{x1}$ Figure 5.1-a) is 3.8 ma; the same as the output load current available when a stacking ratio of two is used. The drive current may be considered a true step for it has a rise time of less than 1 m-$\mu$ sec., two orders of magnitude faster than any of the F/F's rise times.

The oscillograms of Fig. 5.2 and 5.3 all have the same time base and have time moving from left to right. Picture #1 (Fig. 5.2) shows the driving current $I_{x1}$. This is a step of -3.8 m.a. that lasts for .45$\mu$-sec. Picture #2 shows the collector voltage $T_1$ being the collector voltage of the going "on" transistor and $T_2$ being the collector voltage of the going "off" transistor. Picture #3 shows the base voltages; here again $T_1$ is the going "on" transistor and $T_2$ the going "off" transistor. The sharp spike of $T_2$ indicates that the going "off" transistor is being reverse biased.

The pictures in Fig. 5.3 have the same time base as those of Fig. 5.2 (These pictures were taken with a floating scope so there is some distortion due to feed-through from the trigger source.) Picture #1 shows the base currents. $T_1$ is the base current of the going "on" transistor; this current increases throughout switching, first due to regeneration and then due to charging of

the coupling capacitor through the base of the going "on" transistor. $T_2$ is the base current of the going "off" transistor; this current is actually negative while excess carriers are being removed from the base region of the transistor. The charge supplied to the transistor during this period may be estimated from the area under the reverse current oscillogram. This charge is about $5 \times 10^{-10}$ coulombs, which is about 60% of the available charge stored in the coupling capacitor. Picture #2 shows the collector currents. Current $T_2$ of the going "off" transistor has a sharp increase lasting for about 20 mμ sec. due to the driving current charging up the coupling capacitor. After this spike the collector current decreases until the breakdown diode cuts-off. There is then no further change until the transistor comes out of saturation, at which time the collector current decays to zero while the F/F regenerates. Picture #3 shows the current in the breakdown-diode. If this diode had no capacitance the current through it would decay to zero and remain there until the collector voltage of the going "off" transistor reached the reverse breakdown-voltage of the diode. As the diode does have capacitance its current never stays at zero, but continues to decrease, as can be seen in picture #3.

The following table gives a comparison of the experimental and calculated delay times of the F/F.

| Delay Time | Calculated | Experimental |
|---|---|---|
| $t_1$ | 30 | 30 |
| $t_2$ | 20 | 30 |
| $t_3$ | 82 | 90 |
| $t_4$ | 180 | 100 |
| $t_5$ | 234 | 240 |
| Total | 546 | 490 |

Table 5.1 (All times in mμ-sec)

The experimental and calculated delay times compare quite well. The measured regeneration time ($t_4$) is less than the calculated value, which would be expected for minimum drive was assumed in the calculations.

The repetition rate of the experimental F/F was checked by connecting two units in a closed loop. The frequency of oscillation was then taken as a measure of the maximum repetition rate. The frequency of this oscillation was found to be 350 K. C., but as this figure represents two F/F's in series the maximum repetition rate for a single F/F would be 700 K. C.

## CONCLUSIONS

The use of double-base breakdown-diode clamping in conjunction with a saturating collector coupled F/F gives an output voltage swing that is stable with respect to ground for both output states of the F/F. The output impedance is as low, and can possibly be lower than a similar diode clamped F/F. Switching times are comparable with other types of saturating F/F, for it is the transistors that limit the switching time, not the means of clamping.

The power drain of a F/F using breakdown clamping is constant, and the same as a comparable diode clamping F/F with the exception that with diode clamping, voltage dividers may be needed to establish the clamping voltages, consequently there will be a power dissipation in the voltage dividers that would not be present when using breakdown-diode clamping.

The noise generated by breakdown-diodes is greater than for normal diodes, so that in noise sensitive circuits breakdown-diodes must be used with care.

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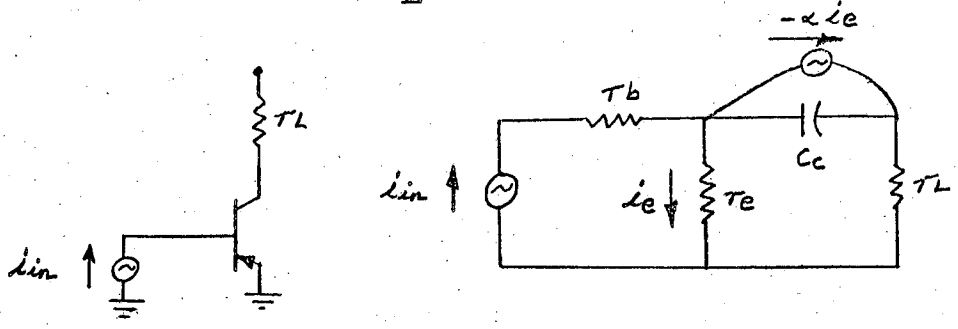
# APPENDIX I

## DOMINANT POLE REPRESENTATION OF A COMMON EMITTER AMPLIFIER

The circuit to be considered here is a common emitter amplifier with a resistive load ($R_L$), driven by a current source ($i_{in}$).




In this equivalent circuit $C_c$ is the junction capacitance, $r_b$ the base resistance, and $r_e$ the emitter resistance; $\alpha$ is the common base current gain represented by

$$\alpha = \frac{\alpha_o}{1 + S/\omega_T} \tag{I.1}$$

where $\alpha_o$ is the d-c alpha and $\omega_T$ is the measured alpha cut-off frequency. Writing the node equations for the above equivalent circuit gives

$$I_{in(S)} = \left[g_e(1 - \alpha) + SC_c\right] V_1 - SC_c V_{out(S)} \tag{I.2}$$

$$0 = (\alpha g_e - SC_c) V_1 + (g_L + SC_c) V_{out(S)} \tag{I.3}$$

Solving these equations for the network function $V_{out}/I_{in}$, and normalizing with respect to $\omega_\alpha$ gives

$$\frac{V_{out}}{I_{in}} = \frac{1}{g_e + g_L} \frac{S^2 + S - \frac{\alpha_o g_e}{\omega_T C_c}}{S^2 + \left(1 + \frac{1}{\omega_T C_c (r_L + r_e)}\right) S + \frac{1 - \alpha_o}{\omega_T C_c (r_L + r_e)}} \qquad (I.4)$$

For normal amplifier operation the following inequality holds

$$\omega_T (r_L + r_e) C_c \gg 1 \qquad (I.5)$$

thus making it possible to obtain an approximate factorization of the denominator of I. 4, for in this case

$$1 + \frac{1}{\omega_T C_c (r_L + r_e)} \gg \frac{(1 - \alpha_o)}{\omega_T C_c (r_L + r_e)} \qquad (I.6)$$

Factoring I. 4 and removing the frequency normalization gives

$$\frac{V_{out}}{V_{in}} \approx - \frac{\alpha_o \omega_T g_e}{(g_e + g_L) C_c} \frac{1}{\left(S + \omega_T + \frac{1}{C_c (r_L + r_e)}\right)\left(S + \frac{(1 - \alpha_o)\omega_T}{1 + \omega_T (r_L + r_e) C_c}\right)} \qquad (I.7)$$

This expression has a dominant pole of $\frac{(1 - \alpha_o)\omega_T}{1 + \omega_T (r_L + r_e) C_c}$ when the condition set by inequality I. 5 holds. The dominant pole representation is then given by

$$\frac{V_{out}}{V_{in}} \approx -\beta_o R_L \quad \frac{P_1}{S + P_1} \tag{I.8}$$

where $\beta_o$ is the d-c common emitter current gain and

$$P_1 = \omega_\beta / D \tag{I.9}$$

where $\omega_\beta$ is the measured common emitter cut-off frequency and D is a degradation factor

$$D = 1 + \omega_T(r_L + r_e)C_c \tag{I.10}$$

# APPENDIX II

From Figure 3.1 the following equations may be written:

$$ie\left\{(1-\alpha_{(s)})\left(r_b+\frac{1}{SC_4}\right)+r_e+r_{s1}\right\}+I_{x2}\left(r_{s1}+\frac{1}{SC_4}\right)=0 \qquad \text{(II.1)}$$

$$I_{c2} = -\,ie\,\alpha(s) \qquad \text{(II.2)}$$

From Appendix I the alpha of transistor $T_2$ may be expressed as

$$\alpha(s) = \frac{\alpha_o\,\omega_T}{S+\omega_T} \qquad \text{(II.3)}$$

The following definitions will be made

$$\omega_\beta = \omega_T\,(1-\alpha_0) \qquad \text{(II.4)}$$

$$\tau_1 = \frac{1}{r_{s1}\,C_4} \qquad \text{(II.5)}$$

$$\tau_2 = \frac{1}{(r_b+r_e+r_{s1})C_4} \qquad \text{(II.6)}$$

Solving II.1 and II.2 using the above definitions gives the transfer function of the circuit as

$$\frac{I_{c2(s)}}{I_{x2(s)}} = \frac{\alpha_o\,\omega_T\,r_{s1}}{r_b+r_{s1}+r_e}\;\frac{S+\tau_1}{S^2+S\left\{\tau_2+\omega_T\frac{r_e+r_{s1}+r_b(1-\alpha_o)}{r_e+r_{s1}+r_b}\right\}+\tau_2\,\omega_\beta} \qquad \text{(II.7)}$$

Normalizing II. 6 with respect to $\omega_\alpha$ the alpha cut-off frequency of transistor $T_2$ gives

$$\frac{I_{c2(s)}}{I_{x2(s)}} = \frac{\alpha_o r_{s1}}{r_e + r_{s1} + r_b} \quad \frac{S + \tau_1/\omega_T}{S^2 + S\left(\frac{\tau_2}{\omega_T} + \frac{r_e + r_{s1} + r_b(1-\alpha_o)}{r_e + r_{s1} + r_b}\right) + \frac{\tau_2}{\omega_T}(1-\alpha_o)} \tag{II. 8}$$

Equation II. 8 may be factored into a dominant pole expression for in general

$$\frac{\tau_2}{\omega_T} + \frac{r_e + r_{s1} + r_b(1 - \alpha_o)}{r_e + r_{s1} + r_b} \gg \frac{\tau_2}{\omega_T}(1 - \alpha_o) \tag{II. 9}$$

This identity is valid if the d-c beta $(1/1- \alpha_o)$ of transistor $T_2$ is much larger than one. The dominant pole approximation representing II. 9 is

$$\frac{I_{c2(s)}}{I_{x2(s)}} = \frac{\alpha_o}{1 + D} \quad \frac{1}{S + \frac{1 - \alpha_o}{1 + D}} \tag{II. 10}$$

where D is a loss factor given by:

$$D = \omega_T C_4 (r_e + r_{s1} + r_b(1 - \alpha_o) \tag{II. 11}$$

Solving the dominant pole expression of II. 10 for a step input of drive-current $I_{x2}$ gives

$$I_{c2(t)} = I_{x2} \frac{\alpha_o}{1 - \alpha_o} \left(1 - e^{-\frac{\omega_B}{1 + D} t}\right) \qquad \text{(II. 12)}$$

The delay time $t_2$ may be found from II. 12 by setting $I_{c2(t)}$ equal to the maximum breakdown-diode current ($I_d$) and solving for t.

$$t_2 = \frac{1 + D}{\omega_B} \ln \frac{\frac{1}{I_d(1 - \alpha_o)}}{1 - \frac{\alpha_o}{\alpha_o}} / I_{x2} \qquad \text{(II. 13)}$$

The term $\frac{I_d(1 - \alpha_o)}{\alpha_o}$ in equation II. 13 is the base current needed to just drive the breakdown-diode current to zero under d-c conditions, while $I_{x2}$ is the actual base current being supplied to transistor $T_2$. $I_{x2}$ will be larger than $I_{d(1 - \alpha_o)}/\alpha_o$ under all conditions (It is impossible to produce a change in state unless this condition is met.), and normally it will be considerably larger if any amount of overdrive is being employed. If the ratio of $I_{x2}$ to $I_{d(1 - \alpha_o)}/\alpha_o$ is greater than two or three equation II. 13 may be approximated by

$$t_2 = \frac{1 + D}{\omega_T} \frac{I_d}{I_{x2}} \qquad \text{(II. 14)}$$

# APPENDIX III

The first step is to find the base current of the saturated transistor $I_{B1}$ (Fig. 3.2) as a function of the collector current of the going "on" transistor.

Writing the node equations from Fig. 3.2 gives

$$V_{1(s)}\left(\frac{1}{R_3} + S_C\right) - V_{o1(s)}\left(S(C_3 + C_L) + \frac{1}{R_3}\ \frac{1}{R_L}\right) + \frac{V_s}{S R_L} + I_{2(s)} = 0 \qquad \text{(III. 1)}$$

$$-V_{1(s)}\left(\frac{1}{R_3} + \frac{1}{R_{B1}} + SC_3\right) + V_{o1(s)}\left(\frac{1}{R_3} + SC_3\right) = 0 \qquad \text{(III. 2)}$$

Solving for $I_{B1(s)} = \dfrac{V_{1(s)}}{R_{B1}}$

$$I_{B1(s)} = \frac{I_{2(s)}\ (SC_3 + 1/R_3)}{R_{B1}\left\{S^2 C_3 C_L + S\left[C_3\left(\frac{1}{R_{B1}} + \frac{1}{R_L}\right) + C_L\left(\frac{1}{R_3} + \frac{1}{R_{B1}}\right)\right] + \right.}$$

$$\left. + \frac{1}{R_3}\left(\frac{1}{R_{B1}} + \frac{1}{R_L}\right) + \frac{1}{R_{B1} + R_L}\right\} \qquad \text{(III. 3)}$$

For most design work it is possible to approximate equation III. 3 by a simple dominant pole expression. Under the conditions that

$$R_{B1} < R_L < R_3 \qquad \text{(III. 4)}$$

$$C_L \ll C_3 \tag{III. 5}$$

the dominant pole expression is

$$I_{B1(s)} = I_{2(s)} \; H_1 \; \frac{S + Z_1}{S + P_1} \tag{III. 6}$$

Where

$$H_1 = \frac{1}{1 + \frac{C_L}{C_3} + \frac{R_{B1}}{R_L}} \tag{III. 7}$$

$$Z_1 = \frac{1}{R_3 C_3}$$

$$P_1 = \frac{1}{C_3 + C_L \left( \frac{1}{R_3} + \frac{1}{R_{B1} + R_L} \right)} \tag{III. 9}$$
$$1 + \frac{R_{B1}}{R_L}$$

The next step in finding $I_{B1(s)}$ is to obtain an expression for the driving current $I_{2(s)}$. Equation II. 12 of Appendix II may be used for $I_{2(s)}$ if it is shifted in time, i. e., at time t = 0 $I_{c2(t)}$ (Equation II. 12) must be equal to the steady state breakdown diode current $I_d$. To accomplish this shift let

$$t = t_2 + t' \tag{III. 10}$$

where t is the time base used in Equation II. 12, $t_2$ is the delay time necessary for the breakdown diode to cut-off, and t' is the new time base. Substituting III. 10 into II. 12 gives

$$I_{c2(t')} = I_{x2} \beta_2 \left(1 - e^{\frac{-\omega_\beta}{1 + D'}(t_2 + t')}\right) \qquad \text{(III. 11)}$$

To remove $t_2$ from Equation III. 18 the equation is solved for t' = 0, at which time $I_{c2(t)} = I_d$. The resulting expression for $t_2$ is then resubstituted into Equation III. 11 giving

$$I_{2(t')} = I_{x2} \beta_2 \left[1 - \left(1 - \frac{I_d}{2I_{x2}}\right) e^{\frac{-\omega_\beta}{1 + D'} t'}\right] \qquad \text{(III. 12)}$$

The loss factor of Equation II. 11 cannot be used in Equation III. 12 for there is no longer any coupling through saturation resistance $r_{s1}$. The new loss factor, taken from Appendix I is

$$D' = \omega_\alpha R_L (C_c + C_3) \qquad \text{(III. 13)}$$

Writing Equation III. 12 in terms of S gives

$$I_2(s) = I_d \frac{(S + Z_2)}{S(S + P_2)} \qquad \text{(III. 14)}$$

where

$$P_2 = \omega_\beta \qquad \text{(III. 15)}$$

$$Z_2 = \frac{P_2 \beta_2 I_{x2}}{I_d} \qquad \text{(III. 16)}$$

When the drive current "$I_{x1}$" is large $Z_2 \gg P_2$, and there is no need to go through the time shifting. Under this condition the inverse Laplace of III. 11 may be used directly.

$$I_{c2(s)} = I_{x2} \beta_2 P_2 \frac{1}{S(S + P_2)} \qquad \text{(III. 17)}$$

The saturated transistor may be represented by a simple one pole expression.

$$I_{c1(s)} = I_{B1(s)} \beta_1 \frac{P_3}{S + P_3} \tag{III.18}$$

where

$$P_3 = \frac{\omega_n \omega_i}{\omega_n + \omega_i} (1 - \alpha_n \alpha_i) \tag{III.19}$$

$\omega_n$ and $\omega_i$ are the forward and reverse alpha cut-off frequencies of the saturated transistor, and $\alpha_n$ and $\alpha_i$ are the d-c alphas in the forward and reverse direction of the saturated transistor, taken at zero collector voltage.

The collector current of the saturated transistor may now be found by combining Equations III. 6, III. 17, and III. 18 giving

$$I_{c1(s)} = \frac{I_{x1} \beta_1 \beta_2 P_2 P_3}{\left(1 + \frac{C_L}{C_3} + \frac{R_{B1}}{R_L}\right)} \frac{S + Z_1}{S(S + P_1)(S + P_2)(S + P_3)} \tag{III.20}$$

Transforming this into the time domain gives

$$I_{c1(t)} = H (K_o + K_{1e}^{-P_1 t} + K_{2e}^{-P_2 t} + K_3 3^{-P_3 t}) \tag{III.21}$$

where

$$H = \frac{I_{x1} \beta_1 \beta_2 P_2 P_3}{1 + \frac{C_L}{C_3} + \frac{R_{B1}}{R_L}} \tag{III.22}$$

$$K_o = \frac{Z_1}{P_1 P_2 P_3} \tag{III.23}$$

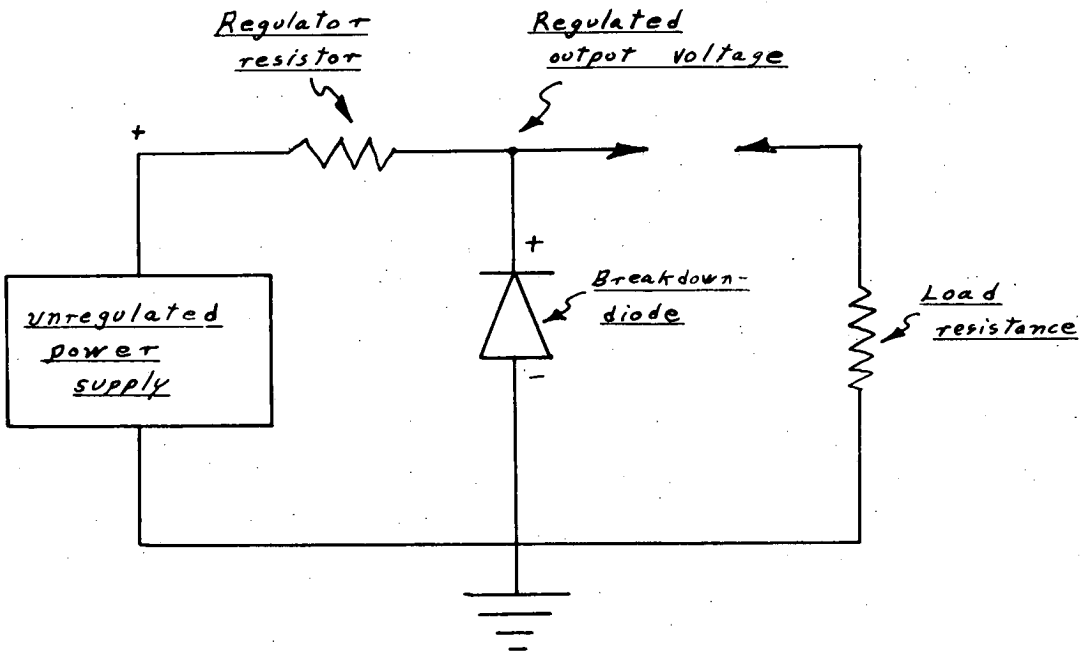
$$K_1 = \frac{P_1 - Z_1}{P_1(P_2 - P_1)(P_3 - P_1)} \qquad \text{(III. 24)}$$

$$K_2 = \frac{P_2 - Z_1}{P_2(P_1 - P_2)(P_3 - P_2)} \qquad \text{(III. 25)}$$

$$K_3 = \frac{P_3 - Z_1}{P_3(P_1 - P_3)(P_2 - P_3)} \qquad \text{(III. 25)}$$

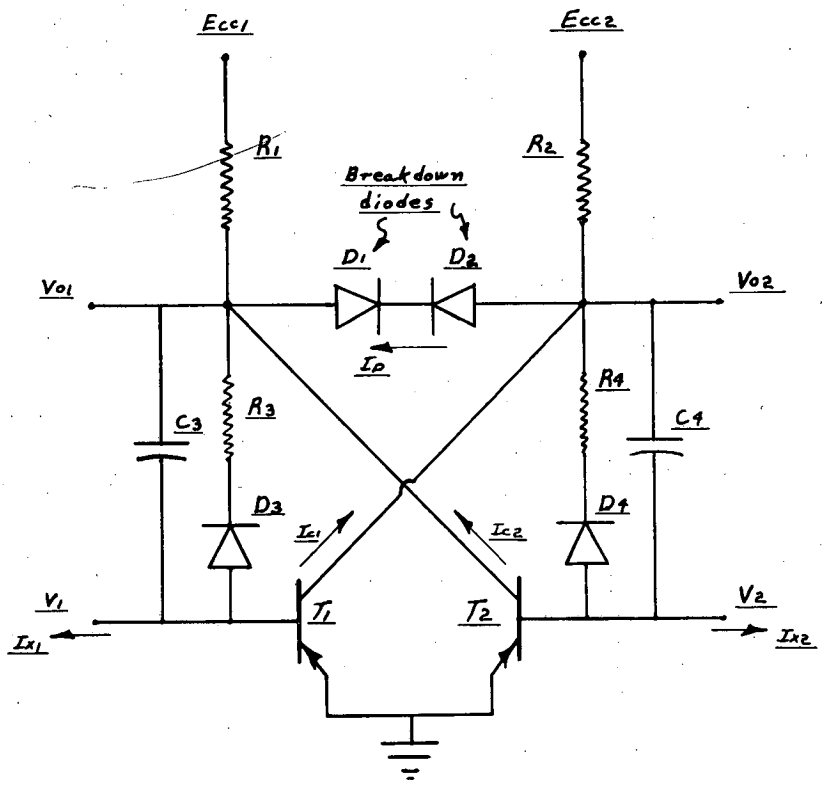
When the delay time is small in comparison with the three poles, i.e., $t < \frac{1}{P_1}$; $t < \frac{1}{P_2}$; and $t \ll \frac{1}{P_3}$, an approximate series expansion of III. 21 may be made giving for the delay time

$$t_3 = \sqrt{\frac{2\, I_{c1(t)}}{H\,(K_1 P_1^{\,2} + K_2 P_2^{\,2} + K_3 P_3^{\,2})}} \qquad \text{(III. 27)}$$



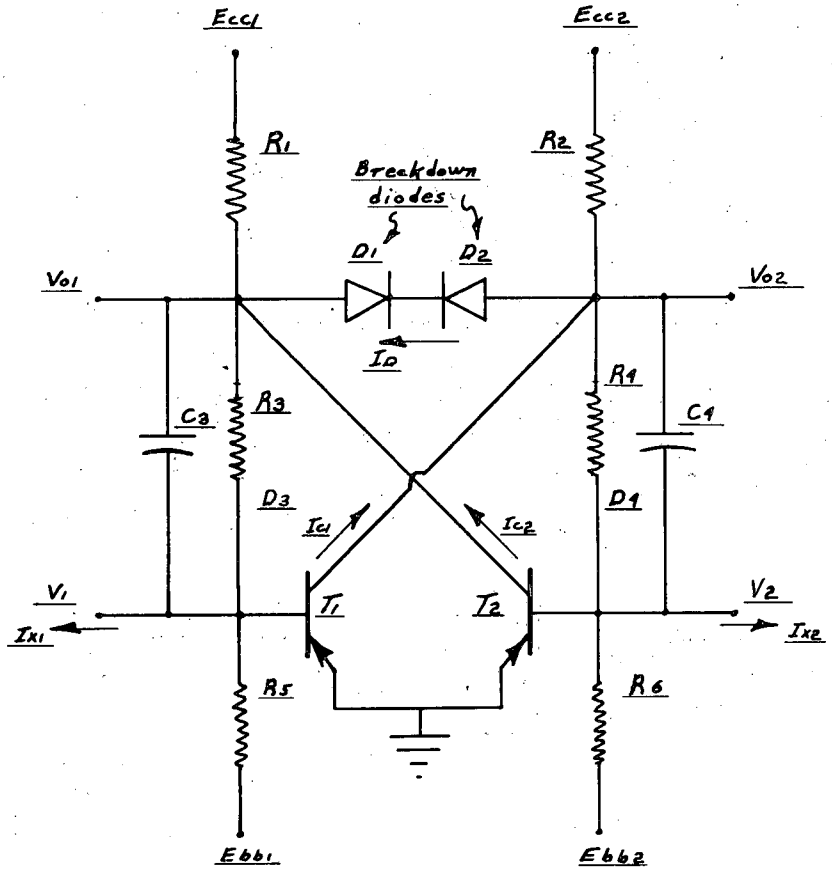

MU-19091

Fig. 2.1. Breakdown-diode regulator circuit.



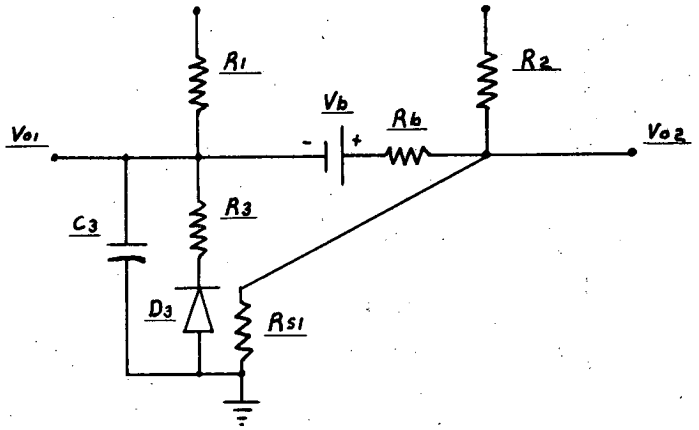

MU-19092

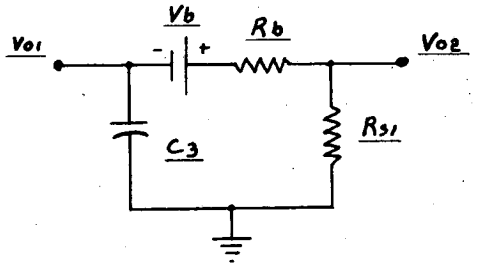
Fig. 2.2. Flip-flop employing breakdown-diodes.




MU-19093

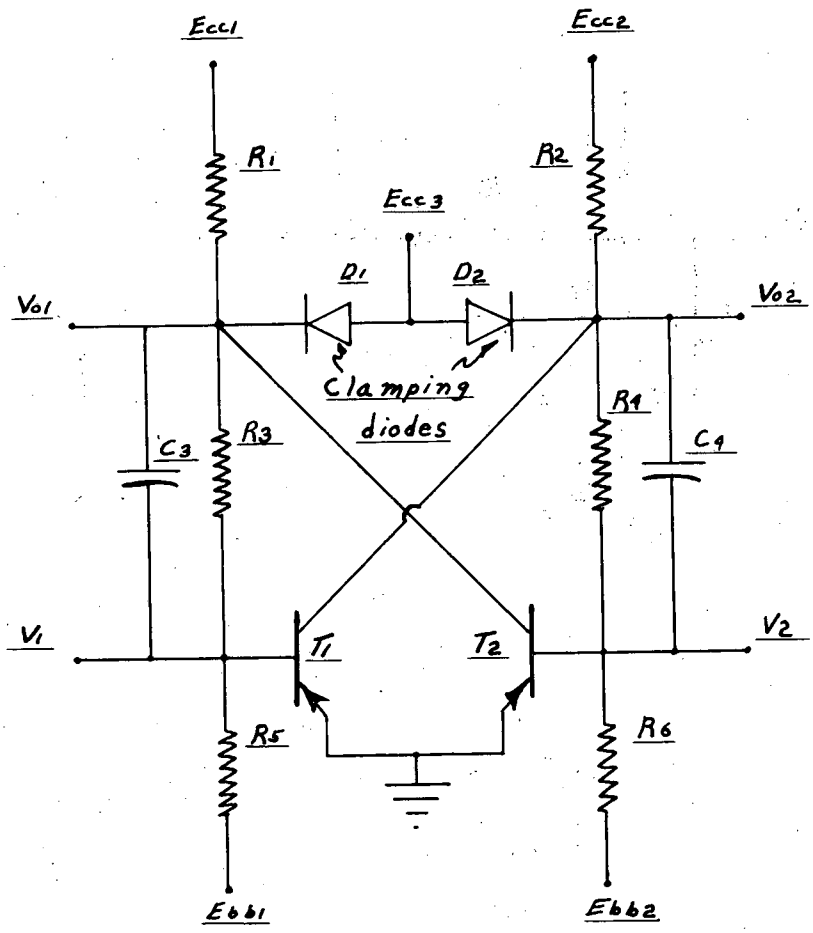
Fig. 2.3. Supplementary flip-flop circuit.



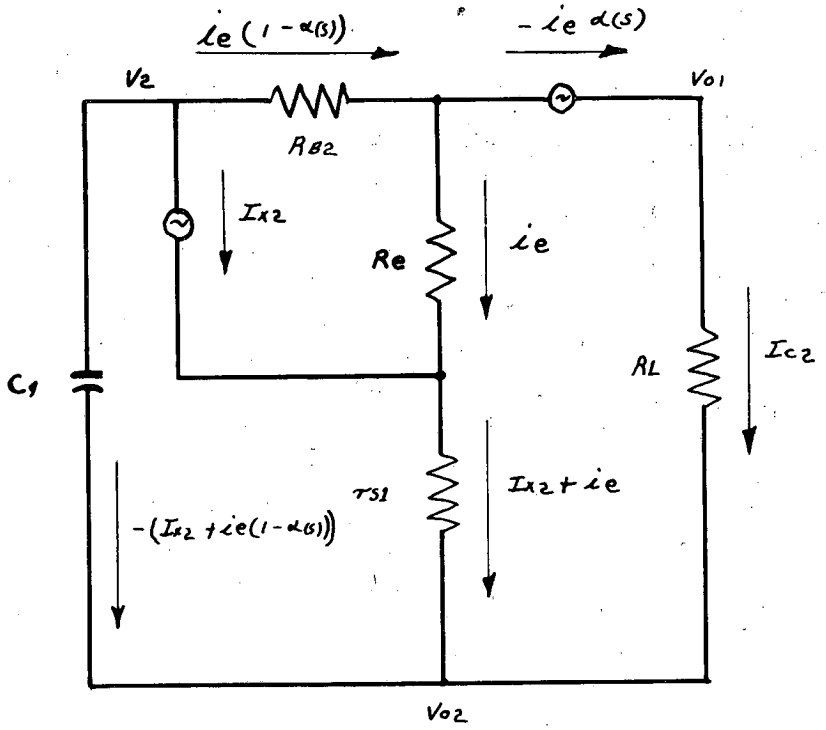

MU-19094

Fig. 2.4. Output characteristics equivalent circuits.



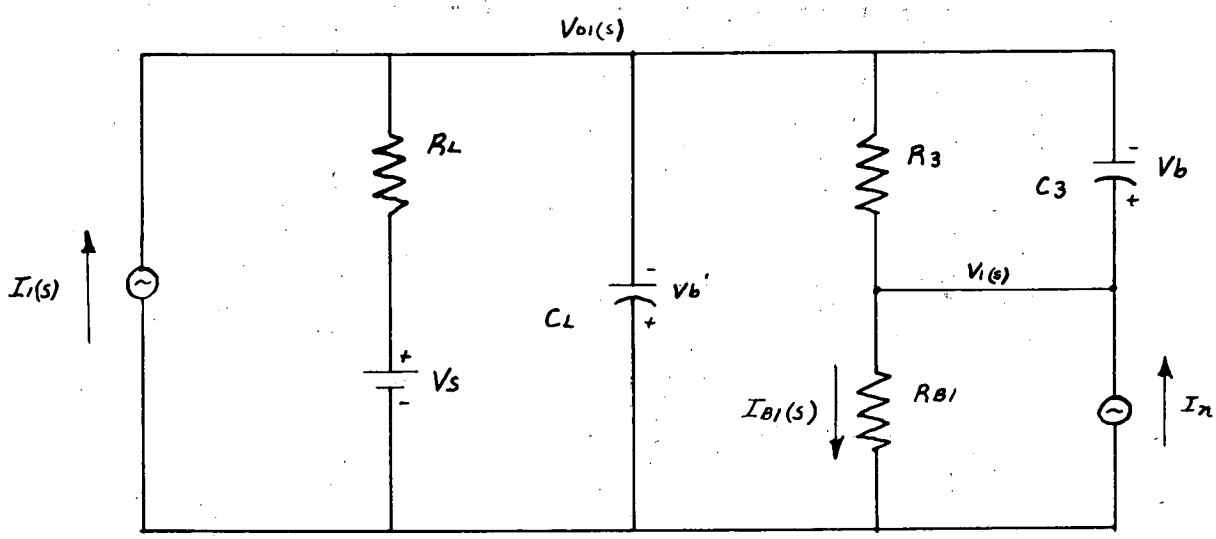

MU-19095

Fig. 2.5. Saturated Eccles Jordan FF using clamping diodes.




MU-19096

Fig. 3.1. Equivalent circuit for delay time $t_2$.




MU-19097

Fig. 3.2. Driving circuit of the saturated transistor.

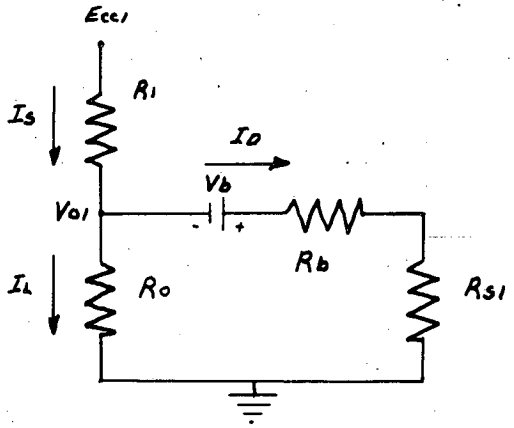



Fig. 4.1 - a

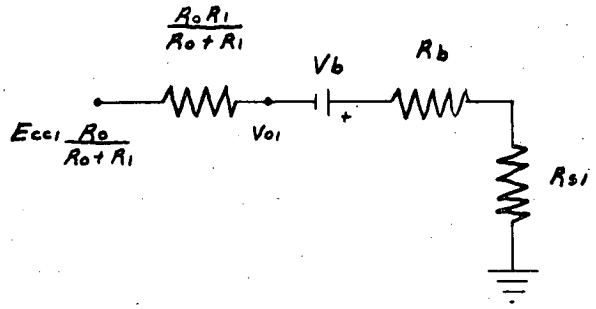
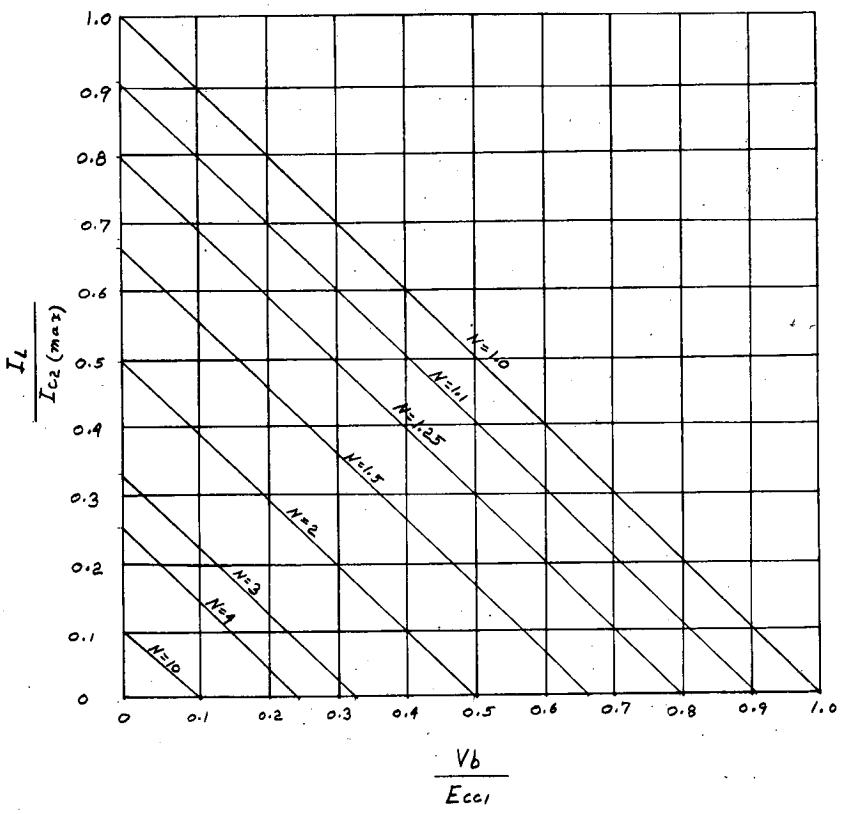



Fig. 4.1 - b

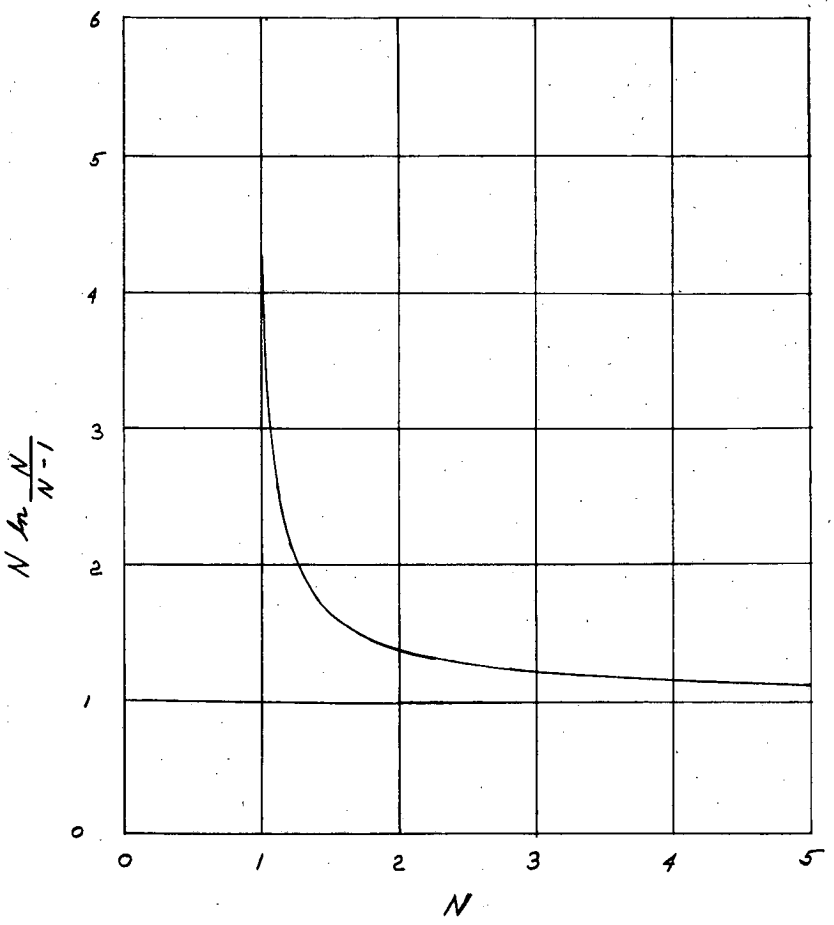
MU - 19098

Fig. 4.1. Static load circuit.




MU-19099

Fig. 4.2.




MU-19100

Fig. 4.3.

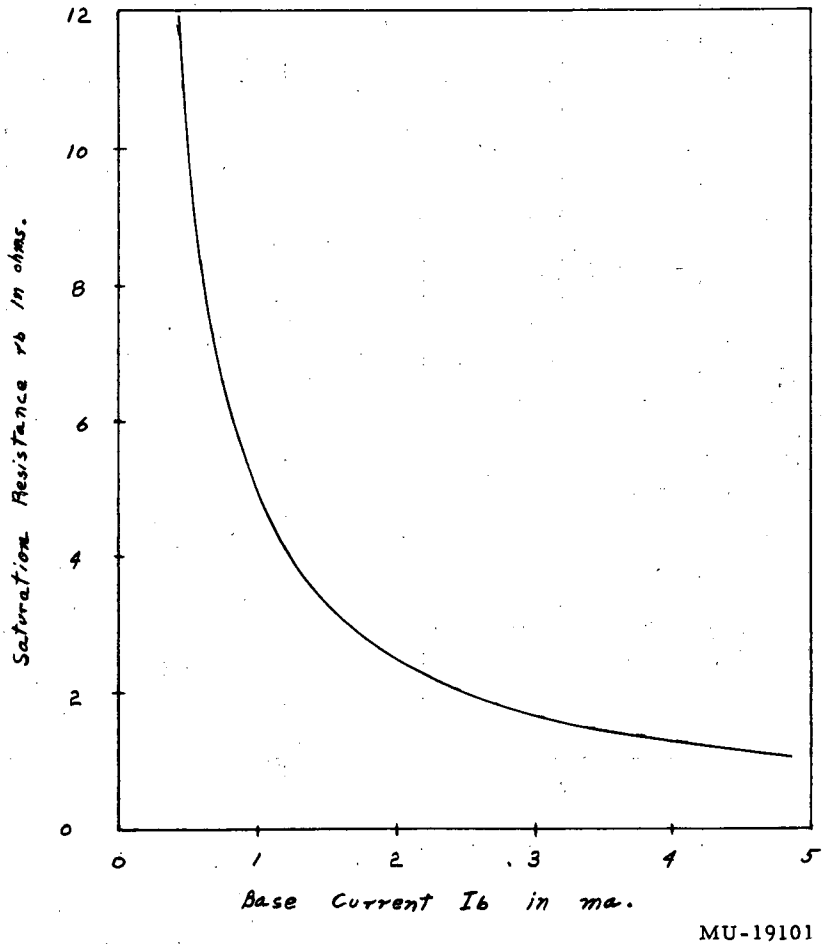
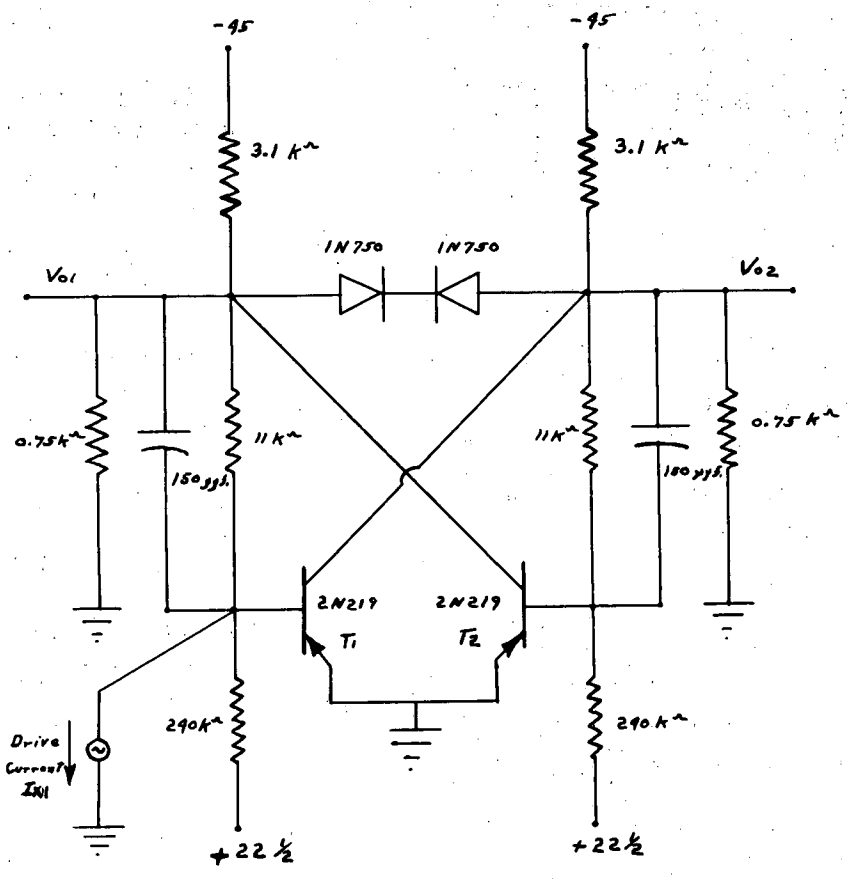
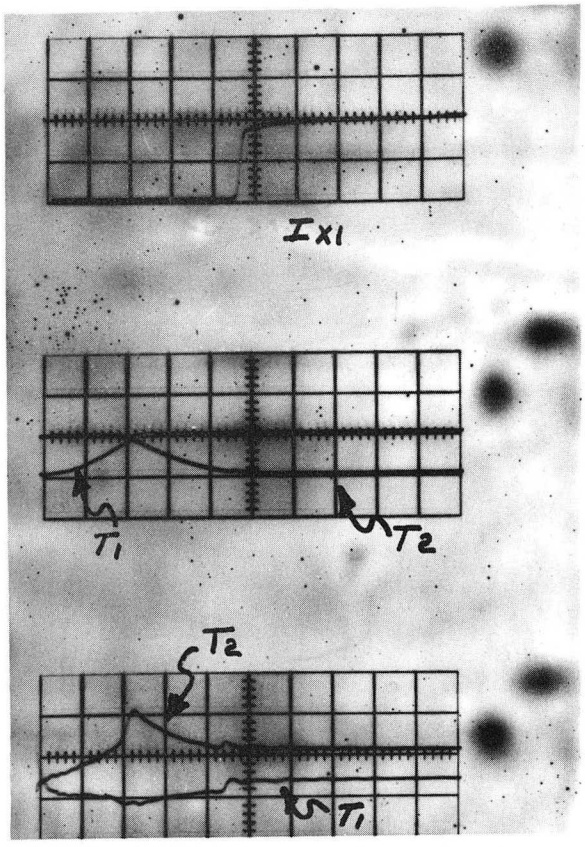



Fig. 4.4. Small signal intrinsic junction saturation resistance for RCA 2N219 transistors.




MU-19102

Fig. 5.1. Experimental flip-flop circuit.




(1)

Driving current of the saturated transistor.
2 ma/cm

(2)

Collector voltages
5 V/cm

(3)

Base voltages.
0.5 V/cm

Time scale 0.1 μ-sec/cm (All photos have the same time base.)

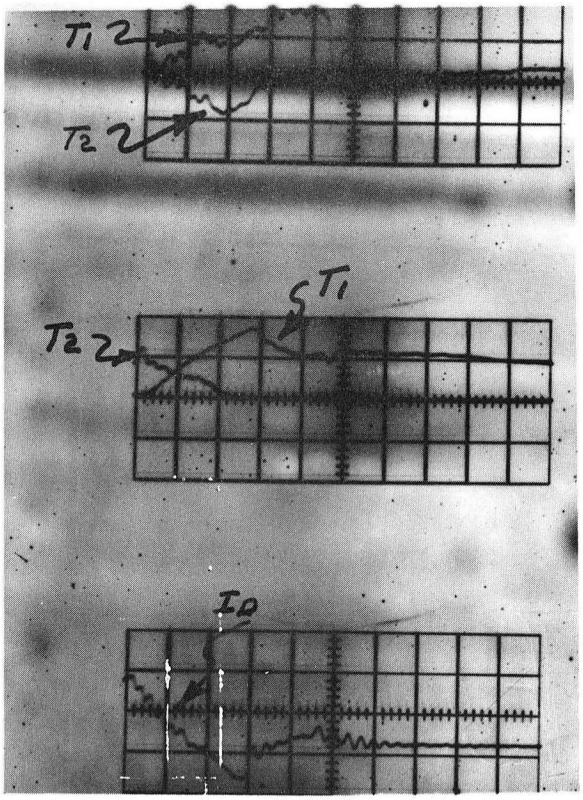
$T_1$ going "on" transistor.

$T_2$ going "off" transistor.

STEP RESPONSE TEST

Fig. 5.2

ZN-2309




(1)

Base currents.
5 ma/cm

(2)

Collector currents
20 ma/cm

(3)

Breakdown-diode current
5 ma/cm

Time scale 0.1 μ-sec/cm (All photos have the same time base.)

$T_1$ going "on" transistor.

$T_2$ going "off" transistor.

STEP RESPONSE TEST

Fig. 5.3