Title

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A High Performance 48-to-6 V Multi-Resonant Cascaded Series-Parallel (CaSP) Switched-Capacitor Converter

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A High Performance 48-to-6 V Multi-Resonant Cascaded Series-Parallel (CaSP) Switched-Capacitor Converter

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***Abstract*—Switched-capacitor (SC) converter topologies can achieve high efficiency and high power density due to their efficient switch utilization and use of high energy density capacitors. The use of resonant inductors can further improve efficiency by enabling soft-charging and soft-switching operations. However, the number of components (switches and capacitors) increases proportionally with the conversion ratio, increasing circuit complexity and potentially reducing performance. Because of this, SC converters with multiple operating states per switching cycle are attractive for high-step down applications as they can achieve the same conversion ratio as two-phase SC converters with fewer components. This work proposes and explores a new multi-phase resonant cascaded series-parallel (CaSP) topology, comprising a cascaded 2-to-1 SC stage with a 4-to-1 series-parallel stage. A 48-to-6 V prototype design for data center applications was built and tested, and achieved 98.6% peak efficiency (98.1% including gate drive loss), 95.3% full-load efficiency (95.2% including gate drive loss) at 70 A output, and 2140 W/in^3 power density by box volume.**

I. Introduction

As data center power consumption continues to grow due to increased computational demand, industry has shifted towards distributing power to servers at higher voltages (i.e. 48 V) in order to reduce conduction losses [1]. This 48 V bus must then be converted to the extreme low voltages and high currents at the point-of-load (PoL) CPUs and GPUs. One common approach is to use a two-stage architecture, in which the 48 V bus is first stepped down to an intermediate bus voltage (5-12 V) that is then stepped down to the PoL voltage. Recent research has shown that using an intermediate bus voltage lower than 12 V can result in better overall system efficiency, as the second-stage buck converter can operate at higher efficiency at a lower input voltage [2]–[4].

Hybrid and resonant switched-capacitor (SC) converters are very attractive for these applications, as they not only combine the traditional benefits of SC converters, such as efficient utilization of switches [5] and the use of energy dense capacitors for power conversion [6], but also allow for soft-charging and soft-switching operations [7]–[10]. In addition, these intermediate bus voltage converters can be fixed-ratio, as the second-stage buck converter can provide the regulation needed at the PoL.

This work proposes and analyzes the performance of an 8-to-1 multi-resonant SC converter topology that can achieve high efficiency and power density across a wide load range. It comprises a cascaded 2-to-1 SC stage and a 4-to-1 series-parallel stage, which due to its multi-phase operation, can achieve an 8-to-1 conversion ratio with a lower number of components than standard two-phase SC circuits [11]. Here, multi-phase operation refers to SC converters that have more than two switching states, as discussed in [11].

A 48-to-6 V, 70 A, fixed-ratio prototype was designed and tested, and achieved 98.6% peak efficiency (98.1% with gate drive loss), 95.3% full-load efficiency (95.2% with gate drive loss), and 2140 W/in^3 power density. The converter can also operate over a wide range of input voltages (40 - 60 V), as may occur in a 48 V nominal data center application. Practical design considerations such as component selection and tolerance requirements are also discussed. The prototype displays some of the highest output current and power density among existing 8-to-1 converters.

II. Multi-Resonant Cascaded Series-Parallel (CaSP) Converter

A. Proposed topology and operating principle

Fig. 1 shows the schematic drawing of the proposed 8-to-1 cascaded series-parallel topology, with an output voltage $V_\mathrm{o} = \frac{V_\mathrm{in}}{8}$. Theoretical switch and capacitor voltage ratings, as well as gate control signals for each switch, are labeled. The current waveforms for the inductor and flying capacitors $C_1 - C_4$, gate signals, and equivalent circuits for each phase are shown in Fig. 2. During Phases 1 and 2, the front-end stage of the converter ($Q_1 - Q_4$, and C_1) achieves a 2-to-1 step down. During Phase 3 the converter operates with a 4-to-1 parallel-mode operation, resulting in an overall conversion ratio of 8-to-1.

- From $t = 0$ to $t = \frac{T}{8}$ (Phase 1), the flying capacitors are connected in series and charged by the input voltage. The resonant frequency of this phase is determined by the series combination of C_1, C_2, C_3, and C_4, and the inductor, L. Therefore, $f_{\mathrm{res},1} = \frac{1}{2\pi\sqrt{LC_\mathrm{eq}}}$, where $\frac{1}{C_\mathrm{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}$.
- From $t = \frac{T}{8}$ to $t = \frac{T}{4}$ (Phase 2), C_1 discharges into the series connection of C_2, C_3, and C_4. The resonant frequency is still the same as in Phase 1, so that $f_{\mathrm{res},2} = f_{\mathrm{res},1}$.

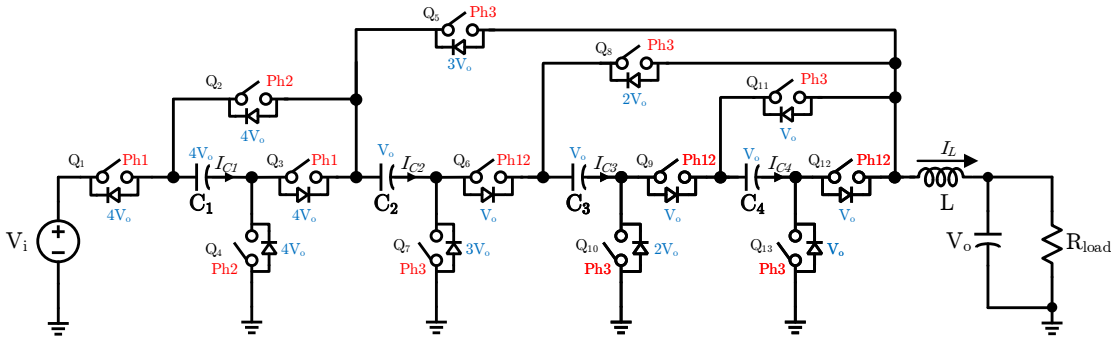

Fig. 1: Schematic drawing of the proposed multi-resonant SC converter with switch and capacitor voltage ratings labeled.

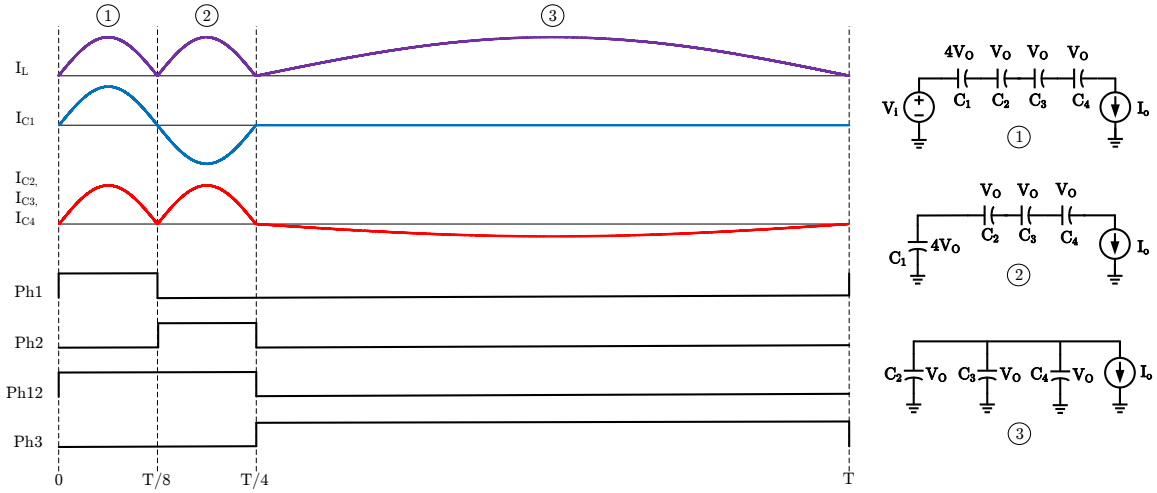

Fig. 2: Key current waveforms and control signals for the multi-resonant converter.

- From $t = \frac{T}{4}$ to $t = T$ (Phase 3), C_1 is disconnected and C_2, C_3, and C_4 are now connected in parallel and discharge into the load. In order to maintain capacitor charge balance, the duration of this phase compared to Phase 1 and 2 is tripled to $\frac{3}{4}$ of the total switching period. The resonant frequency is determined by the parallel combination of C_2, C_3, and C_4, and the inductor, L, so that $f_{\text{res},3} = \frac{1}{2\pi\sqrt{L(C_2+C_3+C_4)}}$.

By using the relative length of the different phases and their corresponding resonant frequencies, the required ratio of flying capacitors can be found. As C_2, C_3, and C_4 are connected in parallel during Phase 3, $C_2 = C_3 = C_4 = C$ for capacitor charge balance.

The duration of Phase 1 and Phase 2 can be written as:

$$T_1 = T_2 = \frac{T}{8} = \frac{1}{2} \cdot 2\pi \sqrt{L\left(\frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}\right)} \quad (1)$$

where T is the switching period. T_1 has a factor of π rather than 2π at it represents a half cycle of the resonant period determined by $f_{\text{res},1}$.

The duration of Phase 3 can similarly be written:

$$T_3 = \frac{3T}{4} = \frac{6T}{8} = \frac{1}{2} \cdot 2\pi \sqrt{L(C_2 + C_3 + C_4)} \quad (2)$$

As the duration of Phase 3 is six times that of Phase 1 or Phase 2, the required capacitor values for perfect resonant operation are $C_2 = C_3 = C_4 = C$ and $C_1 = \frac{C}{9}$.

C_1 requires a lower capacitance because it is charged and discharged at a higher frequency than the other capacitors. These capacitor ratios must be exactly met in order to achieve perfect resonant operation and therefore zero-current switching (ZCS) for all switches. However, these ratios only determine the minimum capacitor values needed to achieve soft-charging. Therefore, if ZCS is sacrificed by operating the converter slightly above resonance (so that the inductor current never reaches zero at transitions between operating phases), then the converter can still be soft-charged while removing any strict requirements on capacitor ratios. As demonstrated in [12], operating above the resonant frequency pushes the converter farther into the fast-switching limit (FSL), reducing the output

impedance slightly and making it less sensitive to component variations. Operating in this manner makes the converter easier to control and allows for the use of Class-II ceramic capacitors, despite their dc-bias and temperature-varying characteristics. In addition, the loss of ZCS has a minimal effect on the efficiency of the converter at mid to heavy load, as operating slightly above resonance also results in a smaller rms current value and lower conduction losses [9] [12].

B. Comparison with other 8-to-1 Topologies

Table I compares the component count and output impedance for several different resonant 8-to-1 SC topologies. For simplicity, the same on-resistance is assumed for all switches, but this can be adjusted based on available switch technology for the required operating voltages. The component count (and number of required gate drivers) can greatly affect the power density and volume that a converter can achieve. The output impedance of the converter directly relates to the efficiency of the converter, and incorporates both conduction loss and the capacitor charging/discharing loss. For soft-charged SC converters, the capacitor charging/discharging loss is no longer present and the output impedance will depend on the conduction losses due to the resistance of the switches, as well as the ESR of the capacitors and the PCB trace resistance [9].

While the proposed topology has three more switches and one more capacitor than the topology presented in [13], it has a much lower output impedance. This is due to the fact that the converter operates in the parallel mode for a greater proportion of the switching cycle, and has three parallel conduction paths compared to only one in [13].

The 8-to-1 Fibonacci converter uses the minimum possible number of switches and capacitors to achieve this conversion ratio in a two-phase SC converter. Although the proposed topology has the same number of components as the Fibonacci, its multi-phase operation allows it to achieve a lower output impedance. The proposed topology also only requires about half the number of switches and capacitors as the series-parallel and switched-tank (Dickson) converter [14]. However, the proposed converter's output impedance is only slightly higher than that of the series-parallel topology. While the switched-tank topology's output impedance is slightly less than half of that of the proposed converter, it requires higher voltage-rated capacitors, which can negatively impact power density.

In summary, this work demonstrates a converter topology that achieves a good balance between output impedance (and therefore efficiency) and number of components (and therefore power density).

III. Hardware Implementation and Experimental Results

A. Hardware Performance

Fig. 3 shows an annotated photograph of the hardware prototype. The PCB stack-up consists of 6 layers, with 4 oz copper on the output layers (where the primary current conduction paths are located) and 2 oz copper on the inner layers. As the inductor is the tallest component, a hole was routed in the PCB to recess the inductor in order to achieve a more uniform height, and thereby improve the power density as calculated by box volume.

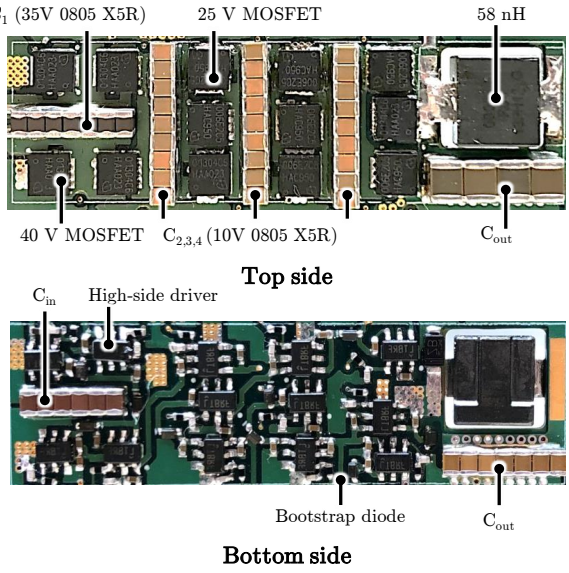

Fig. 3: Photograph of the converter. Dimensions: 1.76 × 0.51 × 0.21 inch (4.47 × 1.30 × 0.53 cm).

The power-stage and gate drive components are listed in Table II. 40 V and 25 V Si devices are used since eGaN FETs do not generally outperform silicon MOSFETs significantly at these low voltages, as they have similar on-resistance and footprints and only slightly lower input-output capacitance [12]. Lower on-resistance devices compared to those used in [13] were used, further improving high-load efficiency. Although these devices have slightly higher output capacitance, the operating frequency of the converter is relatively low (50 kHz), so switching losses are not a dominating factor over the converter operating range.

Although Q_5 and Q_7 have an ideal voltage rating of $3V_o$ (or 18 V for V_{out} = 6 V), 40 V devices were used in the physical implementation. This was done to take advantage of the ability to operate soft-charged SC converters with high capacitor ripple without sacrificing efficiency, as the switches see the capacitor voltage ripple on top of their theoretical blocking voltage. Increasing the voltage rating of the devices increases the energy utilization of the capacitors and allows for lower capacitance to be used, increasing power density. Additionally, this allows for more headroom on the devices when operating at the high end of the input voltage (e.g. at 60 V the devices must block 22.5 V).

Each floating switch is driven by a floating high-side gate driver powered by the cascaded bootstrap method [15] [16], derived from a single ground-referenced 9 V supply.

TABLE I: Comparison of number and voltage rating of components for 8-to-1 resonant switched-capacitor converters

Topology	Number of Switches	Switch Rating	Number of C_{fly}	C_{fly} Rating	Number of Inductors	R_{out}
Proposed Topology	13	$4 \times 4V_o$, $2 \times 3V_o$, $2 \times 2V_o$, $5 \times V_o$	4	$1 \times 4V_o$, $3 \times V_o$	1	1.75
Multi-Resonant-Doubler [13]	10	$4 \times 4V_o$, $3 \times 2V_o$, $3 \times V_o$	3	$1 \times 4V_o$, $1 \times 2V_o$, $1 \times V_o$	1	2.75
Series-Parallel	22	$3 \times 7V_o$, $2 \times (7V_o, 6V_o, ...2V_o)$, $9 \times V_o$	7	$7 \times 7V_o$	1	1.25
Switched Tank [14] (Dickson)	22	$6 \times 2V_o$, $16 \times V_o$	7	$1 \times (7V_o, 6V_o, ...V_o)$	4	0.8
Fibonacci	13	$2 \times 5V_o$, $4 \times 3V_o$ $3 \times 2V_o$, $4 \times V_o$	4	$1 \times (4V_o, 3V_o, ...V_o)$	1	2.165

TABLE II: Main Component Listing for Prototype converter

Component	Device	Parameters
Switch Q_1-Q_4, Q_5, Q_7	Infineon IQE013N04LM6CG	40 V, 1.35 mΩ
Switch Q_6, Q_8-Q_{13}	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
Resonant inductor L	Pulse FP0805R1-R06-R	58 nH, 83 A I_{sat}, 0.17 mΩ
Flying Capacitor C_1	TDK C2012X5R1V226M125AC	14 × 22 μF* ±20% 35 V X5R 0805
Flying Capacitor C_2	Murata GRM21BR61A476ME15L	18 × 47 μF* ±20% 10 V X5R 0805
Flying Capacitor C_3	Murata GRM21BR61A476ME15L	18 × 47 μF* ±20% 10 V X5R 0805
Flying Capacitor C_4	Murata GRM21BR61A476ME15L	18 × 47 μF* ±20% 10 V X5R 0805
Input Capacitor C_{in}	TDK C2012X7S2A105M125AB	6 × 1 μF* ±20% 100 V X7S 0805
Output Capacitor C_{out}	Murata GRM21BR61A476ME15L	7 × 47 μF* ±20% 10 V X5R 0805
	Kemet C1210C107M4PAC7800	4 × 100 μF* ±20% 16 V X5R 1210
Gate driver	Analog Devices LTC4440-5	80 V, high-side
Bootstrap diode	ON Seminconductor NSR0340V2T1G	40V, 250 mA, Schottky
Controller	TI TMDSDOCK28379D Experimenter Kit	

* The capacitance listed here is the nominal value before dc derating.

Table III lists the main operating parameters of the converter. The minimum switching frequency is determined by the value of the flying capacitors and the inductor. However, as discussed previously, the prototype is operated at a frequency slightly higher than resonance to counteract the effects of component tolerance variations, as well as to to reduce the RMS current of the switches, capacitors, and inductor. Although this results in the loss of ZCS, the converter is conduction loss limited at heavy load, so ZCS is not essential for obtaining high efficiency. For the capacitor values used in the prototype, $f_{res} = f_{sw,min} = 40$ kHz. The actual operating frequency for the converter at 48-to-6 V conversion was selected as 50 kHz, as it resulted in the the best efficiency performance while still operating sufficiently above f_{res}.

TABLE III: Converter Operating Conditions

Parameter	Nominal	Range
Input Voltage	48 V	40 - 60 V
Output Voltage	6 V	5 - 7.5 V
Output Current	70 A	
Measured P_{out}	400 W	330 - 500 W
Switching Frequency	50 kHz	50 - 55 kHz

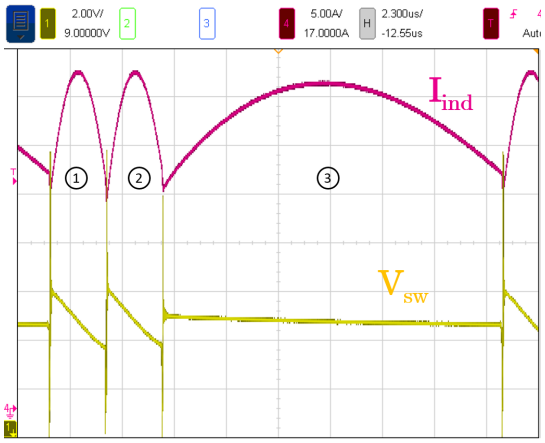

Fig. 4: Inductor current and switch node voltage for 48-to-6 V operation at 30 A.

Measured operating waveforms of the inductor current and switch node voltage are shown in Fig. 4. The operating phases are labeled according to Fig. 2. As can be seen, the inductor current does not reach zero before the next operating phase begins, illustrating the reduced ripple current resulting from operating slightly above resonance.

During Phase 1 and 2 the switch-node voltage slopes downwards due to the increasing voltage across the series-connected flying capacitors as they are being charged. The negative spikes in V_{sw} at the switching transitions are due to body diode conduction in Q_{12} and Q_{13}. These switches can achieve zero-voltage switching (ZVS) during the deadtime due to their proximity to the resonant inductor.

The converter efficiency was measured up to 70 A for 40 - 60 V input, the expected range of a 48 V nominal bus for data center applications. The power stage voltage, current, and efficiency were measured with a Yokogawa WT3000E precision power meter to ensure accurate results at the high efficiencies obtained.

At 48-to-6 V operation, the converter reached a maximum output power of 400 W, resulting in a power density of 2140 W/in^3 as calculated by the box volume of the converter power stage and gate drive circuitry. Fig. 5 shows the efficiency curves for this operating point with and without gate drive losses. The converter achieved a peak efficiency of 98.6% (98.1% with gate drive loss included) and a full-load efficiency of 95.3% (95.2% with gate drive loss included).

The system efficiency curves (including the gate drive loss) are also given for V_{in} = 40 V to V_{in} = 60 V in Fig. 6. At 60-to-7.5 V operation, the converter reached a maximum output power of 500 W, resulting in a power density of 2680 W/in^3. At this operating point, the converter was able to achieve a peak efficiency of 98.4% (97.9% with gate drive loss included) and a full-load efficiency of 96.0% (95.9% with gate drive loss included). The full-load efficiency is improved at higher input voltages compared to the 48 V nominal input, as the increased output voltage means the conduction loss for a given load current will be a smaller proportion of the overall converter power. Table IV lists the power stage and system efficiencies (including gate drive losses) for V_{in} = 40 V to V_{in} = 60 V.

The operating frequency of the converter at 54 V and 60 V input was increased (from 50 kHz to 55 kHz) to account for a slightly higher resonant frequency due to capacitor derating at increased voltage. In [13] the switching frequency was also increased in order to reduce the capacitor ripple seen by the switches. As 40 V FETs were used for the $3V_{\text{o}}$-rated switches in this prototype, there is still significant margin between these devices' peak operating voltages and the rated switch voltage.

Fig. 7 shows the load regulation curve for the converter operating at 48-to-6 V operation. Even though the converter operates in an open-loop fixed-ratio mode, its high efficiency helps to decrease the impact of load regulation. At 48 V input, the converter exhibits a low output impedance of 4.2 mΩ and an output droop of 292 mV (4.9% of V_{out}) across the entire load range.

TABLE IV: Converter Efficiency Across V_{in}

V_{in}	Peak Efficiency (%)	Full-Load Efficiency (%)
40 V	98.6% (98.0% with gate drive)	94.6% (94.5% with gate drive)
48 V	98.6% (98.1% with gate drive)	95.3% (95.2% with gate drive)
54 V	98.4% (98.0% with gate drive)	95.7% (95.6% with gate drive)
60 V	98.4% (97.9% with gate drive)	96.0% (95.9% with gate drive)

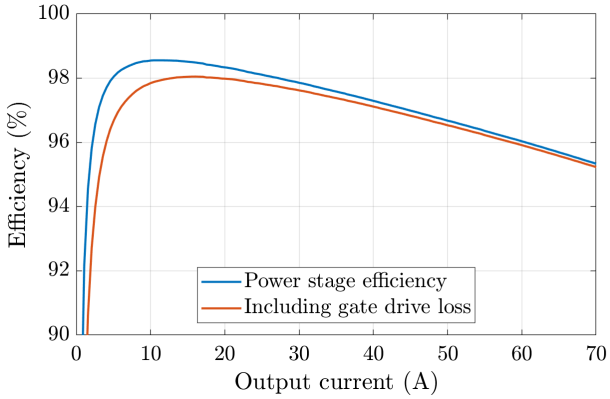

Fig. 5: Measured efficiency at 48 to 6 V, f_{sw} =50 kHz.

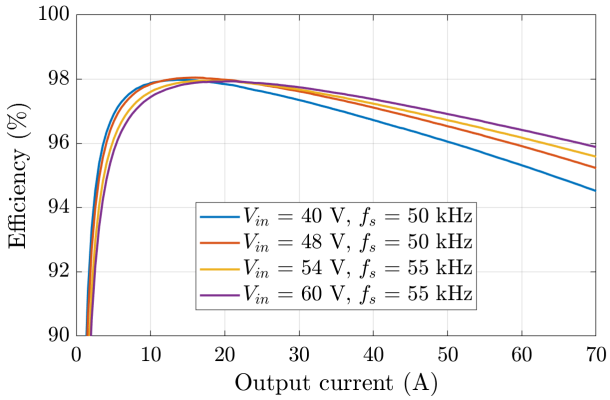

Fig. 6: Efficiency curves including gate drive loss for V_{in} = 40 V to V_{in} = 60 V.

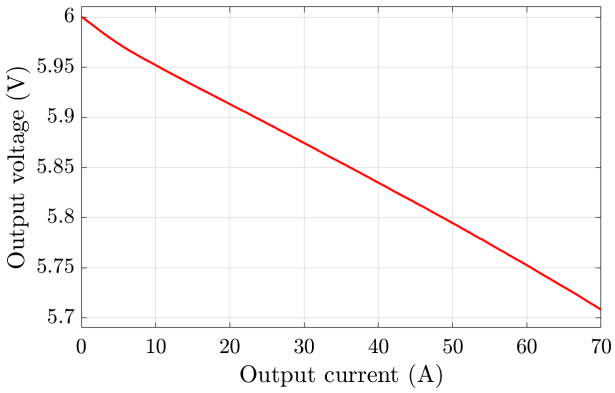

Fig. 7: 48-to-6 V load regulation curve.

Fig. 8 shows a thermal image of the converter operating at full-load at 48 V input. The temperature of the prototype

remained under 59°C during the entire load sweep when using a bench-top CPU fan to air cool the PCB.

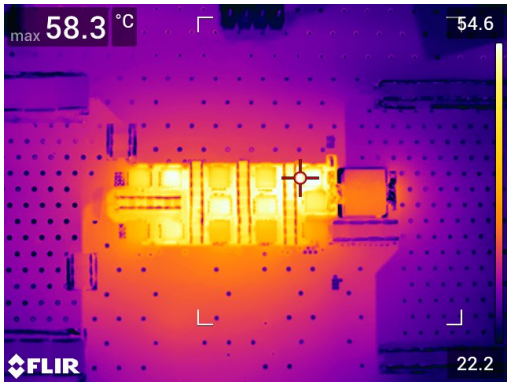

Fig. 8: Thermal image at 48 V_{in} and 70 A.

The converter was also able to handle large load transients, as shown in Figs. 9 and 10. The output voltage did not show significant undershoot or overshoot, and both it and the inductor current waveforms stabilized on the order of 100 μsec.

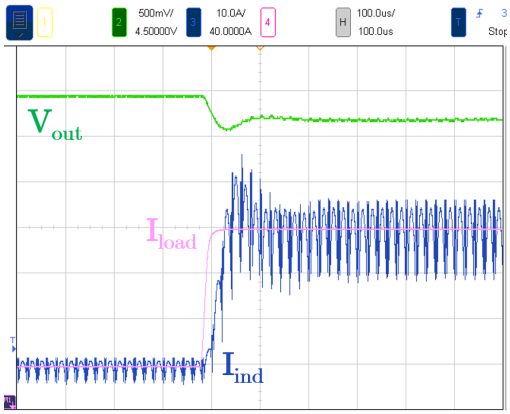

Fig. 9: Load-step from 10 A to 40 A for 48-to-6 V.

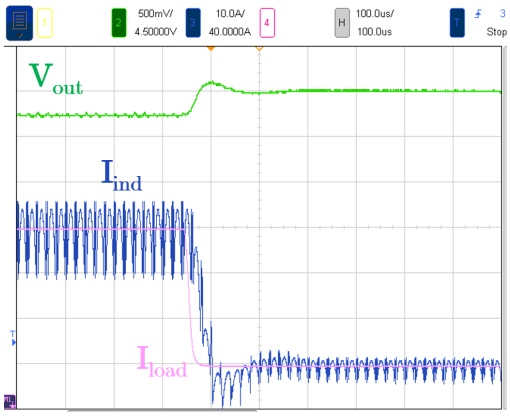

Fig. 10: Load-step from 40 A to 10 A for 48-to-6 V.

B. Capacitor Tolerances

As shown in Table II, all flying capacitors used are Class-II ceramic capacitors and have a tolerance of ±20%. As the converter is always operated above resonance, the capacitor values do not have to be perfectly matched.

To demonstrate the converter's robustness to capacitance variation, the board was tested with 2× additional 0805 capacitors for C_1, representing roughly a 15% increase in capacitance. The converter efficiency was then measured across V_{in} = 40 - 60 V at the same operating frequencies as shown in Fig 6. At all operating conditions, the new efficiency curves were within 0.05% of the original curves.

C. Comparison with Existing Works

Table V compares this work with some of the best existing 8-to-1 works. The proposed converter can achieve a similar peak efficiency to [13], but can obtain higher output current (70 A compared to 40 A) and greater power density. Additionally, at 40 A the proposed converter has a system efficiency of 97.3%, compared to 95.9% [13]. Ref [17] takes advantage of a large step-down transformer to achieve a high full-load efficiency at a very high output current; however its power density is not as high as the hybrid SC topologies in this paper. Both the hybrid SC topologies and the LLC topology can achieve higher output current, power density, and efficiency compared to the buck topology presented in [18], showcasing the limitations of conventional buck topologies in high step-down applications.

IV. Conclusion

This paper presents an 8-to-1 multi-resonant cascaded series-parallel (CaSP) converter designed for 48 V to intermediate bus voltage applications in data center power delivery systems. The converter achieves a good balance of low component count and low output impedance, thereby allowing for high efficiency and high power density. A 48-to-6 V, 70 A converter prototype was built and tested, with 98.6% peak efficiency (98.1% with gate drive loss), 95.3% full-load efficiency (95.2% with gate drive loss), and a power density of 2140 W/in^3. The converter can also operate over a wide input voltage range (40 - 60 V), and demonstrates good robustness to capacitor variation.

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TABLE V: Comparison of this work and existing 8-to-1 converters

Reference	Topology	Voltage ratio	Output current (A)	Power density (W/in^3)	System Efficiency (%) (including gate drive loss)
This Work	Cascaded Series-Parallel	48-to-6 V	70 A	2140	full load: 95.1%, peak: 98.0%
MRD-SCC [13]	Multi-Resonant-Doubler	48-to-6 V	40 A	1675	full-load: 95.9%, peak: 98.0%
EPC AppNote014 [17]	LLC	48-to-6 V	150 A	1100	full-load: 96.9%, peak: 98.0%
EPC9205 [18]	Buck	48-to-6 V	14 A	$\leq$900	full-load: 91.8%, peak: 93.9%

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