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Electronic Transport and Switching Phenomena in Low-Dimensional Materials

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Adane K. Geremew

September 2019

Dissertation Committee:
Professor Alexander A. Balandin, Chairperson
Professor Roger Lake
Professor Alexander Khitun

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The Dissertation of Adane Kahsay Geremew is approved by:

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Committee Chairperson

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Dedication

To my parents

Kahsay Geremew Reda and Kaleyta Giday Weldeyesus

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ABSTRACT OF THE DISSERTATION

Electronic Transport and Switching Phenomena in Low Dimensional Materials

by

Adane K. Geremew

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, September 2019
Prof. Alexander A. Balandin, Chairperson

This dissertation reports results of an investigation of electron transport in two classes of layered van der Waals materials: quasi-one-dimensional (1D) transition metal trichalcogenides (TMTs) and quasi-two-dimensional (2D) transition metal dichalcogenides (TMDs). Practical motivations for this study include the search for (i) materials, which can be used in ultimately downscaled interconnects in the next generations of electronics, and (ii) materials revealing low power switching phenomena, which can be used in future logic circuits. TMTs have strong covalent bonds in one direction and weaker bonds in cross-plane directions. They can be prepared as crystalline nanoribbons consisting of 1D atomic threads, i.e. chains. I have examined the current carrying capacity of $ZrTe_3$ nanoribbons using structures fabricated by the shadow mask method. It was found that $ZrTe_3$ nanoribbons reveal an exceptionally high current density, on the order of ~100 MA/cm^2, at the peak of the stressing current. I have investigated the low-frequency electronic noise in such nanoribbons. The low-frequency noise data were used to determine the activation energy for electromigration. TMDs reveal interesting charge-density-wave (CDW) effects, which can be triggered by electric bias even at various temperatures. I investigated

switching among three CDW phases – commensurate, nearly commensurate, incommensurate – and the normal metallic phase in $1T-TaS_2$ devices induced by application of an in-plane bias voltage. The switching among all phases was achieved over a wide temperature range, from 77 K to 400 K. The electronic noise spectroscopy was used as an effective tool for monitoring the transitions. The noise exhibits sharp increases at the phase transition points, which correspond to the step-like changes in resistivity. The possibility of the bias-voltage switching among four different phases of $1T-TaS_2$ is a promising step toward nanoscale device applications. The results also demonstrate the potential of noise spectroscopy for investigating and identifying phase transitions in the materials.

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1. Charge density waves in van der Waals materials

1.1 Introduction to charge density waves

Certain transition metal dichalcogenides (MX_2 where M is metal: Nb, Ta, Ti etc. and X is Se, S, Te etc.) undergo charge density waves (CDW) transitions at different temperature.[1] The first theoretical work of the charge dynamics instability at low temperature in one dimensional metallic wires was demonstrated by Peierls in 1955.[2] In the absence of interaction with the underline lattice, termed as electron-phonon coupling, Fermi level is continuous and all energy levels up to the Fermi level are occupied by electrons. In this configuration, the lattice spacing *a* is a uniform periodic array of atoms throughout the metallic chain.[2,3] However, in the presence of electron-phonon interaction of any strength, the system becomes unstable and the lattice distorts periodically to minimize the total energy of the system. This distortion has a periodicity of λ with respect to the Fermi wave vector K_f as $\lambda = \pi/K_F$.[2,3] This lattice distortion opens a gap at the Fermi surface where states up to $\pm K_F$ are filled. The elastic energy increases as a result of strain induced by lattice distortion. However, in 1D systems, the CDW ground state has lower energy than the undistorted chain due to the divergence of Lindhard function seen at $q = 2K_F$. As a result, it is common that material systems with anisotropic electronic and crystal structure, predominantly nanowires or quasi 1D systems, show a CDW transition. In the single particle excitation spectrum, the system has a gap, and this leads to modification of the density of electrons. The new charge density will be modulated periodically with period of $\lambda = \pi/K_F$[2,3]. At a finite temperature, charge carriers excited across the single particle gap

effectively screen the electron-phonon interaction, which lowers the energy of the gap and causes second order phase transition. This phenomenon of thermally excited semiconductor to metal transition is referred as Peierls transition[2]. Below the transition temperature, the material that undergoes phase transition is semiconducting because of the gap in the single particle excitation spectrum. Since the lattice periodicity is incommensurate with the modulated CDW, it can carry current by sliding without any activation. The interation of the moving CDW with defect, phonons, and impurities will trap the CDW pinning.[4] However, depending the concentration, capture cross section, and trapping efficiency of the imperfection in the lattice, the resulting current response of the system for the applied DC or AC voltage input is predominantly determined by the behaviour of the total collective mode of the system. In bulk quasi-1D materials, there is a sharp threshold electric field below which conductivity is due to the normal electrons excited across the single particle gap. Above E_T, the strongly nonlinear conduction is due to moving CDW sliding. In the high concentration of impurities, strongly pinned CDW, the elastic energy of CDW is neglected and the phase of the CDW is fully adjusted to the pinning sites. Where as during low concentration of impurities, the CDW can not be fully adjusted to the imperfect sites such as defects, impurity and traps but over a long range. An applied electric field can depin the locked CDW if the energy gain for displacement of the CDW exceedes the pinning energy.[5,6]

1.2 CDW in quasi-1D and 2D transition metal chalcogenides

CDW quasi 1D and 2D materials can be found in different atomic and electronic phases[7]. Such diverse structural and electronic phases promoted investigation of spin orbit interaction, superconductivity and valleytronics.[8,9] It is widely reported that several mechanisms can trigger phase transformations in transition metal trichalcogenides (MX_3; M= Ta, Ti, Nb, X= S, Se) including: strain, temperature, doping and chemical treatments.[10–14] A typical characteristic of CDW transition in quasi 1D transition metal trichalcogenides is their ability to slide above the threshold electric field, which causes nonlinear property near room temperature.[15] This phenomenon is observed below the transition temperature where the electric field exceeds the threshold value, and the resistance drops sharply. The threshold voltage measures the critical force on the CDW phase to depin from randomly distributed impurity centers.[16] Several studies reported non-linear current voltage characteristics associated with the CDW transitions for different poly types of NbS_3 (Phase I, II, III).[15,17] NbS_3 phase I is triclinic with two chains parallel to b axis where Nb atoms form alternative short and long bonds on the order of 3.04 Å and 3.69 Å respectively. This structure does not show any CDW transition.[16] However, NbS_3 phase II does not have Nb-Nb pairs along the b axis but undergoes Peierls distortion with an incommensurate period of nearly 3 atomic distances.[16] The crystal structure of NbS_3 phase III is ambiguous whether it is a sub phase of NbS_3 phase II or a unique structure of its own.[18,19] The newly discovered NbS_3 phase V has a monoclinic phase and structurally similar to triclinic NbS_3, phase I, but has a halved b-axis, where the lattice parameter can be expressed as a, b/2, c, β based on the NbS_3 phase-I unit cell. These dimensions result in

two chains per unit cell and maintain fixed Nb-Nb bond distance of 3.36 Å along the chains. Like NbS_3 phase I, NbS_3 phase V also has an ABCDE repeating sequence of chain bilayers. NbS_3 phase II shows a series of CDW transitions both above and below room temperature. Recently, it was reported that NbS_3 phase II shows a series of Peierles transition at temperature of 150 K, 350 K and 620 K. The coherence of CDW depinning and sliding in the electric field is significantly increased by rf irradiation.[18] Both CDW transitions at temperatures of 150 K and 350 K of NbS_3 phase II show sharp threshold fields, termed as Shapiro steps.[20] Furthermore, it was reported electron diffraction study on NbS_3 phase II demonstrates a CDW transition at 340 K and phase I does not demonstrate CDW transitions.[18] However, almost all the CDW transition on polytypes of NbS_3 are observed far from room temperature. $ZrTe_3$, another member of the TMT family, crystalizes in monoclinic space group $p2_1/m$ (a = 5.87 Å, b = 3.94 Å, c = 11.11 Å and $\beta = 97.82^0$).[21,22] $ZrTe_3$ is semi-metallic and shows CDW transition at temperature of 63 K. $ZrTe_3$ also shows anisotropic transport properties ($\rho_a = 1.8\times10^{-4}$ Ωcm, $\rho_b = 2.5\times10^{-4}$ Ωcm and $\rho_c = 20\times10^{-4}$ Ωcm).[22–24] In contrast to other V-MX_3 (group 5 transition metal trichalcogenides), $ZrTe_3$ has smaller value of ρ_a because of strong coupling between chains and has CDW wave vector perpendicular to the chain direction.[23–26] The resistivity versus temperature of $ZrTe_3$ shows a bump at ~ 63 K in support of CDW transition.[27] Later, coexistence of CDW and superconductivity in Cu intercalated quasi-two-dimensional crystals of $ZrTe_3$ was reported.[25] Studies on optical properties of $ZrTe_3$ also demonstrated anisotropic behavior as shown in the effective mas of electrons in different directions ($m^*_{ae} = 0.2\ m_o$, $m^*_{be} = 0.3\ m_o$).[28] The detail discussion of application of $ZrTe_3$ for interconnect technologies will be

discussed. Owing these interesting optical and electronic properties, TMDs are also ideal candidates for future electronics.[7] 1T-TaS_2 is a 2D CDW van der Waals material exhibiting periodic modulation of CDW due to interplay between electron-electron and electron-phonon interactions.[29–37] As a result of Fermi surface driven instabilities, 1T-TaS_2 undergoes a lattice distortion and subsequent periodic modulation of CDW below 600 K.[2] The CDW becomes fully commensurate with the lattice below 180 K,[38–40] below this temperature the electron-electron interaction forms a high resistance state by forming "David star", connecting 12 neighboring "Ta" atoms pulling towards a central "Ta" atom with only one electron per star and the rest of the electrons are confined in the valence band, leading to an increase in electrical resistance.[38,41,42] Periodic lattice reconstruction is the result of Fermi-surface nesting where coordinating S atoms form out-of-plane distortions whereas 12-Ta atoms pulled in plane to the center of Ta atom.[38,43,44] As temperature increases, the insulating phase changes to a conductive phase where the CDW order melts into small islands textured by nearly commensurate domain wall networks.[45] This transition is revealed as two big hysteresis windows in resistance profile at 180 K (C-NC) and 355 K (NC-IC) by following different path during cooling and heating process followed by IC-M transition at 550 K.[46,47]

1.3 Basics of low-frequency electronic noise

Electronic noise is macroscopic effect induced by collective fluctuations occurring in the device volume, also referred as microscopic noise source.[48] Electronic noise is the consequence of single-particle fluctuations due to scattering events.[48] Low-frequency noise ($f \leq 100$ kHz) is a figure of merit and limiting factor for high frequency field effect transistors (FET) including complementary-metal-oxide-semiconductor (CMOS), heterostructure field effect transistor (HFETs) and metal–semiconductor field-effect transistor (MESFETs).[49,50] Low-frequency noise analysis is a powerful tool for examining compound semiconductors and yielding information about crystal defects and interface. The smaller is the device the higher is the noise: $S_I/I^2 \sim 1/V$ or $1/A$ where V and A represents volume and area respectively. It is also used as a diagnostic and prediction tool to study devices and structural quality of the materials including but not limited to deep trap levels in bulk semiconductors, traps in the oxides of MOSFETs, degradation, contacts, and substrate quality.[50] The up conversion of 1/f noise to the phase noise of generators, amplifiers, and mixers causes performance degradation.[50] 1/f noise is upconverted to high frequencies limiting the performance of the transistors in the microwave range and limits the phase noise characteristics and degenerates the performance of the electronic system.[50] In cellular phones, a loop bandwidth of <1 MHz, phase locked loop (PLL) resulting from $1/f^3$ phase noise (PN) can be an issue.[50] An oscillators phase noise is effected by the noise of the open-loop amplifier and by the half-bandwidth of the resonator. If the amplifier has no 1/f noise region, the oscillator will have $1/f^2$ noise below the half-bandwidth. In electronic devices components, all the active devices have 1/f region.[50] Frequency stability

is a measure of the degree to which an oscillator maintains the same value of frequency over a given time and phase noise is a measurement of uncertainty in phase of a signal. The effect of slope and amplitude of 1/f noise on frequency shift is presented in schematic Figure 1.1. Owing to extremely large number of carriers participating in the motion, the individual behavior of each carrier is immaterial. Only average quantities have impact on the circuit variables (for example, current density and therefore the total current is proportional to the average electron velocity). From a device and circuit point of view, collective fluctuations, albeit small, propagate to the external terminals of the device thus originating electrical noise. The operation of semiconductor devices is based on charge transport, *i.e*. on the motion of free carriers in the conduction and valence bands. Under the effect of applied external forces and of the interaction with lattice perturbations or other carriers, electrons and holes undergo a kind of Brownian motion whereby the velocity of each carrier exhibits large fluctuations, As already recalled, two main fluctuations occur in semiconductor materials and, therefore, in devices: fluctuations of carrier velocity or diffusion noise, associated to the Brownian motion of free carriers in the conduction or valence band, and fluctuations of carrier number or generation-recombination (G-R) noise, due to transitions between conduction and valence bands, either direct or trap-assisted.

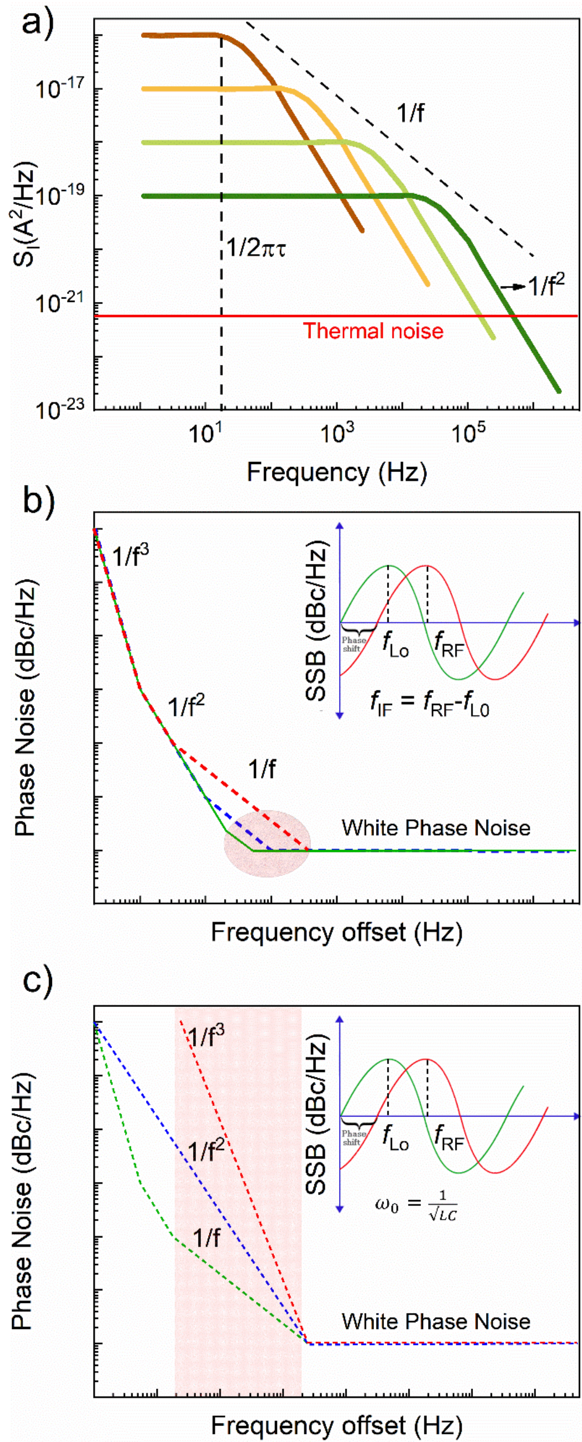

Figure 1.1 Types of electronic noise: G-R noise, 1/f noise and thermal noise. b) Schematics showing upconverting of 1/f noise to phase noise. c) Effect of the strength of 1/f noise on shifting the frequency.

1.4 Noise measurement setup and procedures

The noise spectra were measured with an in-house built experimental setup, using a dynamic signal analyzer (CR 7458) which as in-built low signal amplifier and a separate portable signal analyzer with its low signal amplifier (Stanford Research 560). In order to minimize the 60 Hz noise and its harmonics, the voltage bias to the devices was applied using a battery biasing circuit. The devices were connected with the Lakeshore cryogenic probe station (TTPX). All current-voltage characteristics were measured in the Lakeshore cryogenic probe station with a semiconductor device analyzer (Agilent B1500). The dynamic signal analyzer measured the absolute voltage noise spectral density, S_V, of a parallel resistance network of a load resistor, R_L, and device under test, R_D. The normalized current noise spectral density, S_I/I^2, was calculated from the equation:

$$S_I/I^2 = S_V\times[(R_L+R_D)/(R_L\times R_D)]^2/(I^2\times G^2), \qquad \text{(I)}$$

where G is the amplification of the low-noise amplifier. The noise measurement system and experimental procedures have been validated with the experiments on other materials and devices[51–59]. The low-frequency noise setup and simplified circuit schematic is shown in Figure 1.2 and 1.3, respectively.

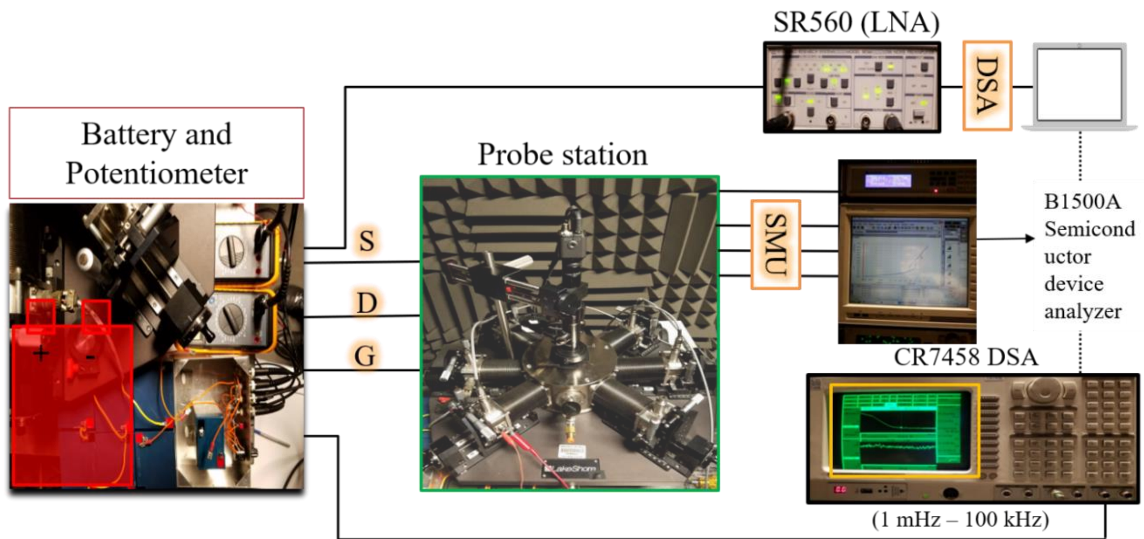

Figure 1.2 Schematic of the low-frequency noise set up used for electronic noise measurements of quasi-1D and 2D FET devices. The components include, a battery source, potentiometer, cryogenic probe station, low signal amplifier and dynamic signal analyzer.

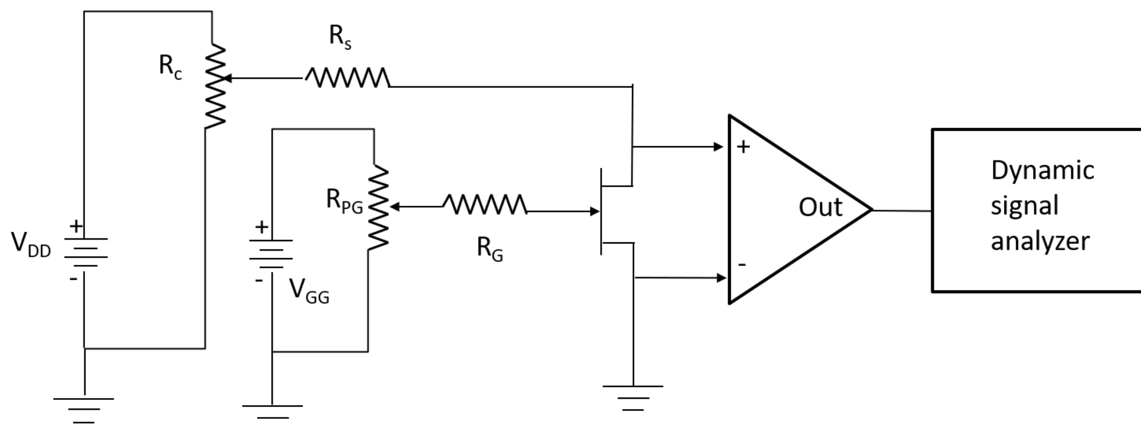

Figure 1.3 Circuit configuration of the low-frequency noise setup. A three terminal device is biased by a battery and the voltage fluctuation signal is amplified and analyzed using a dynamic signal analyzer.

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2. Transition metal trichalcogenide interconnects

2.1 Introduction to the transition metal trichalcogenide interconnects

As aggressive scaling in the CMOS technology continues[1], there is a growing need to examine new materials that can be used for nanometer-scale local interconnects or device channels.[1,2] More than a decade ago, the industry moved from aluminum (Al) to copper (Cu) to lower resistivity and improve reliability via reduced electromigration. Recently, it has been reported that the 10-nm logic technology node features local interconnects made of cobalt (Co), which enables a 10-fold reduction in electromigration.[2] At present, the current density sustained by Cu interconnects in state-of-the-art CMOS technology is on the order of 2-3 MA/cm^2.[3,4] It was recently proposed that quasi-one-dimensional van der Waals materials, such as transition metal trichalcogenides (TMTs) with formula MX_3 (where M = Nb, Ta, Ti, Zr, and other transition metals; X = S, Se, Te), have properties attractive for applications in nm-scale electronics.[5] In a way similar to TMDs, which exfoliate into 2D layers,[5,6] TMTs exfoliate into quasi-1D atomic thread bundles.[7–9] It was previously reported that metallic $TaSe_3$ nanowires have breakdown current density, at the peak of the stressing DC current, on the order of ~10 MA/cm.[2,7,8] In principle, such quasi-1D materials could be ultimately downscaled by exfoliation, or grown directly, into nanowires with a cross-section of ~1 nm × 1 nm, which corresponds to an individual atomic thread, *i.e.* chain. In this dissertation another member of the TMT family, nanoribbons

[1]The text of this chapter is, in part, reprinted from A. Geremew, M.A. Bloodgood, E. Aytan, B.W. Woo, S.R. Corber, G. Liu, K. Bozhilov, T.T. Salguero, S. Rumyantsev, M.P. Rao, and A.A. Balandin, IEEE Electron Device Lett. 39, 735 (2018).

made of $ZrTe_3$, reveal exceptionally high current density, on the order of ~100 MA/cm^2, at the peak of the stressing DC current. Our experimental data also indicate that the low-frequency noise (LFN), another important metric of the material's applicability in electronics, is relatively low, and scales down with the resistance, following the trend found for some other low-dimensional materials.

2.2 Material synthesis and characterization

The selection of $ZrTe_3$ was based on reports indicating that $ZrTe_3$ has better electrical conduction properties than other MX_3 materials.[10] In this dissertation, $ZrTe_3$ crystals were synthesized by the chemical vapor transport (CVT) method.[7,8,11,12] $ZrTe_3$ crystallizes in the monoclinic space group $P2_1/m$. It has strongly anisotropic electronic transport properties, and its bulk electrical resistivity is lower than that of $TaSe_3$ and several other MX_3.[13–16] However, there are inconsistencies in the literature with respect to the reported electronic band structure of $ZrTe_3$, *i.e.* metallic *vs.* semiconducting, type of conduction, as well as in the transition temperatures to the CDW and superconducting phases.[10,13–18] These issues are not directly related to the present study, which is focused on the current carrying capacity of $ZrTe_3$ nanoribbons. Figure 2.1 shows crystal structure of exfoliated $ZrTe_3$ threads CVT-grown material and a reference commercial sample (HQ Graphene)[2]. All X-

[2]Transmission electron microscopy and electron energy loss spectroscopy (TEM-EELS) analysis is courtesy of Dr. Krassimir Bozhilov, University of California Riverside.

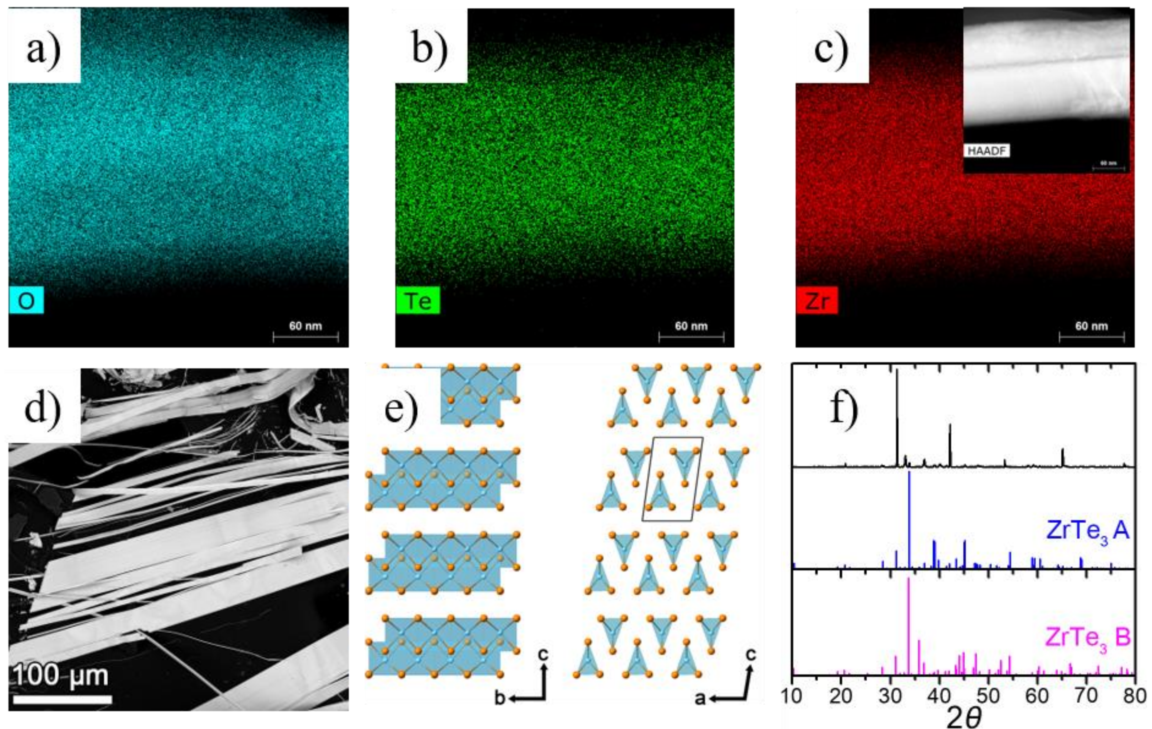

Figure 2.1 TEM-EELS elemental map analysis and X-ray diffraction characterization of $ZrTe_3$. a) Elemental analysis for Oxygen, b) Tellurium and c) Zirconium. Inset shows HAADF image. d) SEM image of bulk crystal. e) Crystal structure showing spatial arrangement of atoms, f) Comparison of simulated and experimental X-ray diffraction of type A and type B phases of $ZrTe_3$. Results a-c were acquired with the help of Dr. Krassimir Bozhilov (UC Riverside) and Figures d-f are courtesy of Professor Tina Salguero (University of Georgia).

ray diffraction peaks are consistent and in agreement with the literature.[19,20] Mechanical exfoliation onto a Si/SiO_2 substrate was used to obtain $ZrTe_3$ nanoribbons. One should note that $ZrTe_3$ occupies an intermediate position between quasi-2D and quasi-1D materials, owing to its structure and bonding characteristics.[13–16] For this reason, it exfoliates into ribbon-like structures with widths larger than thicknesses; referred as nanoribbons of $ZrTe_3$ *vs.* nanowires of $TaSe_3$. The length of the exfoliated nanoribbons could reach hundreds of µm. While exfoliation can often yield nanoribbons with few-nm lateral dimensions, on the thickness range ≤50 nm and the width range ≤500 nm.

2.3 Device fabrication

I utilized the shadow mask method to directly deposit transmission line measurement (TLM) structures onto pre-selected $ZrTe_3$ nanoribbons. This method was used because it avoids the damage and chemical contamination typically associated with conventional lithographic lift-off processes. It also drastically reduces the total air exposure time. The shadow masks were fabricated using double-side polished Si wafers with 3 µm thermally grown SiO_2 (Ultrasil Corp.; 500-µm thickness; P-type; <100>). The shadow mask fabrication process began with evaporation of 200 nm chromium (Cr) on the front side of the wafer (200-nm thickness), followed by a combination of electron beam lithography (EBL) and Cr etchant (1020A) to create a stencil of the TLM pattern. This was followed by fluorine-based reactive ion etching (RIE) to transfer the pattern to the underlying SiO_2. Finally, the pattern was transferred into the underlying Si substrate using the deep reactive ion etching (DRIE) (Oxford Cobra). The DRIE etch step was timed to break through to a large backside window that was previously defined using lithographic patterning, RIE, and DRIE. The shadow masks were used to fabricate $ZrTe_3$ devices by aligning them with pre-selected nanoribbons on the device substrate, clamping the aligned mask and device substrate together, and placing the clamped assembly in an electron beam evaporator (EBE) for contact deposition (10 nm Ti and 100 nm Au) through the shadow mask openings. The completed devices were then transferred to another vacuum chamber for electrical characterization. The thickness and width of $ZeTe_3$ nanoribbon were determined from the

atomic force microscopy (AFM) inspection. Figure 2.2 shows scanning electron microscopy (SEM) images of representative Si shadow masks, as well as AFM and SEM images of the $ZrTe_3$ nanoribbon devices fabricated with the masks.

2.4 Results and discussion

The current-voltage characteristics were measured using a probe station (Lakeshore) and a semiconductor analyzer (Agilent B1500). The low-field I-V characteristics of the devices were linear, indicating the Ohmic nature of the contacts and $ZrTe_3$ channels (see inset to Figure 2.3). The extracted contact resistance for typical devices was $2R_C \approx 18\ \Omega$, *i.e.* less than 3% of the total $ZrTe_3$ channel resistance. In Figure 2.3, Ipresent I-V characteristics of

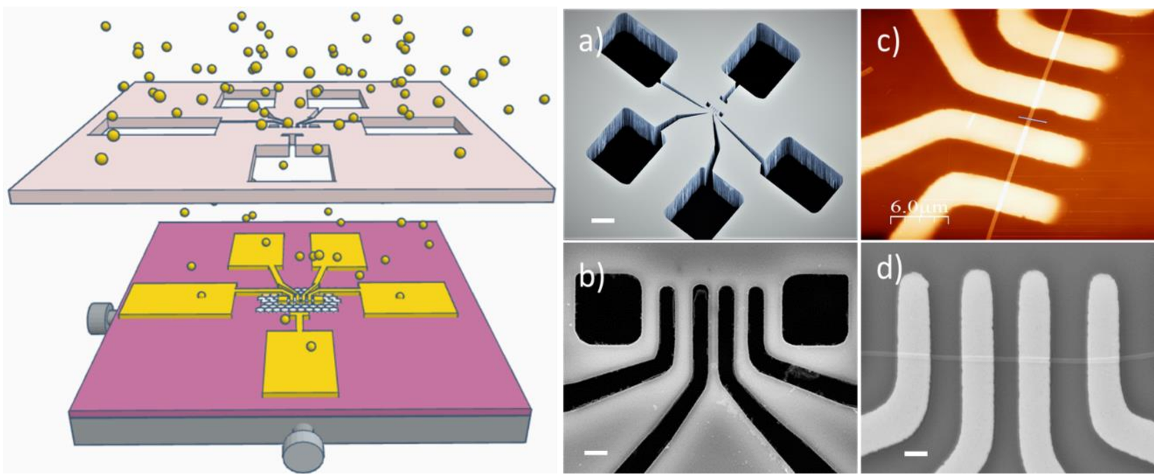

Figure 2.2 Left panel is a schematic of the evaporation process through shadow mask. Right panel shows microscopy images. (a) SEM image of a shadow mask with TLM stencil structure patterned on 500-µm thick Si/SiO_2 wafer. (b) Top-view SEM image of the pattern for Ti and Au evaporation to create the source and drain contacts. (c) AFM image of the quasi-1D $ZrTe_3$ nanoribbon device, fabricated using the shadow mask. AFM characterization was used to determine the nanowire width and thickness (~ 33-nm in the present case). (d) SEM image of another quasi-1D $ZrTe_3$ nanowire device with a different cross-sectional area. The scale bars in (a), (b) and (d) are 50 µm, 2 µm and 1 µm respectively. The right panel is reprinted with permission from A. Geremew, M.A. Bloodgood, E. Aytan, B.W. Woo, S.R. Corber, G. Liu, K. Bozhilov, T.T. Salguero, S. Rumyantsev, M.P. Rao, and A.A. Balandin, IEEE Electron Device Lett. 39, 735 (2018). Copyright (2018) IEEE.

a representative quasi-1D $ZrTe_3$ nanoribbon device, which was biased up to its complete breakdown. In these devices, the peak of the stressing DC current reached ~15.8 mA at the bias voltage of ~1.6 V. This corresponds to a maximum breakdown current density on the order of 100 MA/cm^2. Four other tested devices revealed similar current densities. The electrical resistivity did not show a clear scaling trend, fluctuating in the range from $\sim 3\times10^{-4}$ Ω-cm to $\sim 7\times10^{-4}$ Ω -cm. The obtained values are in line with the data reported in literature for bulk crystals.[14,16] One should note that there have been reports suggesting that $ZrTe_3$ can crystalize in two polymorphs, which have either metallic or semiconducting behavior.[17] However, conditions for phase pure growth have not yet been established, in part because the structural differences between the proposed polymorphs are subtle, making the polymorphs difficult to distinguish by powder X-ray diffraction. It is likely that CVT conditions yield a mixture of polymorphs, and thus one can expect a variation in resistivity depending on the dominant phase of the atomic threads. The breakdown current density obtained for $ZrTe_3$ is a factor ×10 larger than the current density at the maximum stressing current measured for Cu wires, tested before Cu introduction in the interconnect technology.[21] It is also a factor of ×3 larger than the current density at the maximum stressing current for the best $TaSe_3$ nanowire devices reported to date.[7] Overall, the current density achieved in $ZrTe_3$ nanoribbons is extremely high. This can be attributed to the specific single crystalline structure of quasi-1D van der Waals materials, which minimizes electron scattering at grain boundaries and by interface dangling bonds. Measurements of the low-frequency noise (LFN) are often used to assess the material quality and reliability.[22,23]

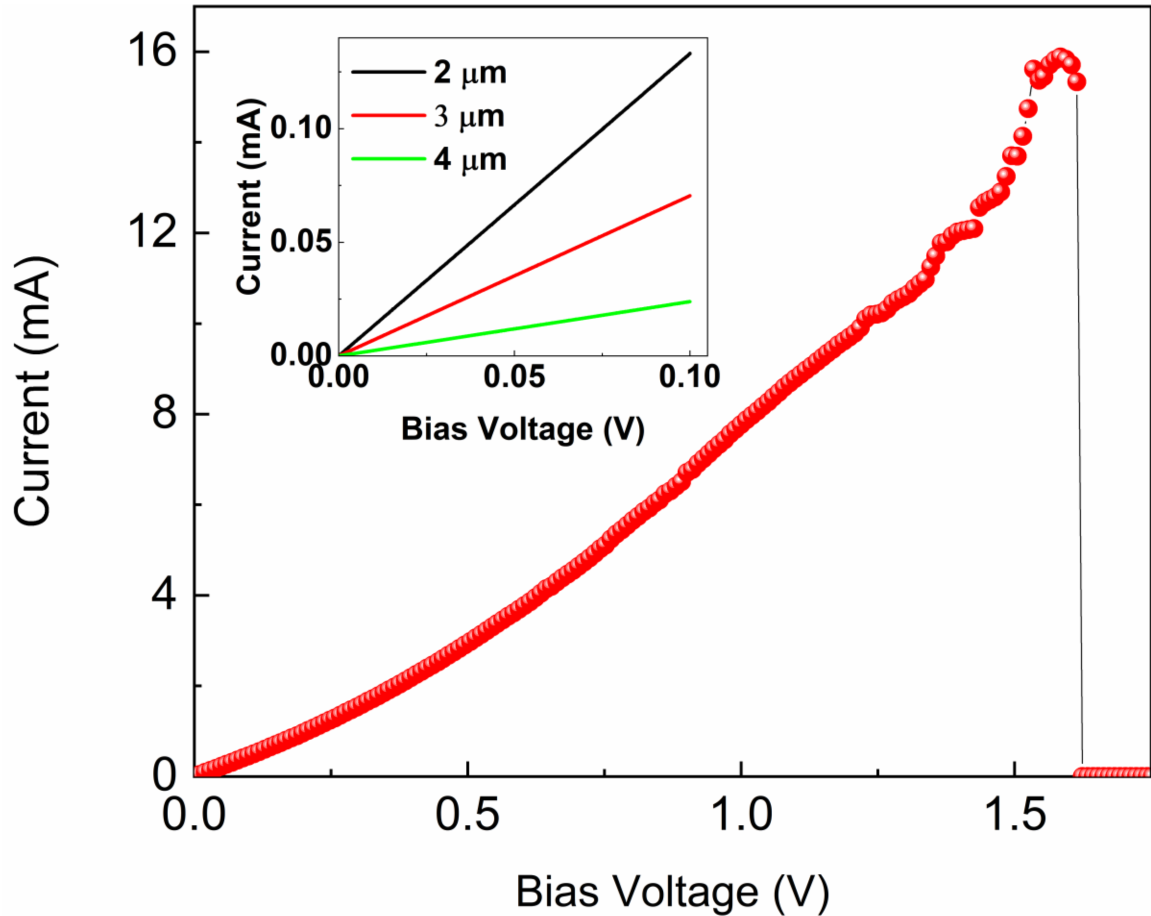

Figure 2.3 High field I-V characteristics of the best quasi-1D $ZrTe_3$ nanoribbon device. The apparent breakdown current density, calculated with the AFM measured thickness and SEM measured width, corresponds to ~10^8 A/cm^2, reached at the voltage bias of ~1.6 V (with a nanoribbon cross-section of ~27 nm × 450 nm). The current shows some signs of instability at V≈1.2 V indicating that some atomic threads started to break. The inset shows low-field I-V characteristics of quasi-1D $ZrTe_3$ devices with different channel lengths used for the contact resistance extraction. The data in the inset indicate the Ohmic nature of the contacts and channel. Reprinted with permission from A. Geremew, M.A. Bloodgood, E. Aytan, B.W. Woo, S.R. Corber, G. Liu, K. Bozhilov, T.T. Salguero, S. Rumyantsev, M.P. Rao, and A.A. Balandin, IEEE Electron Device Lett. 39, 735 (2018). Copyright (2018) IEEE.

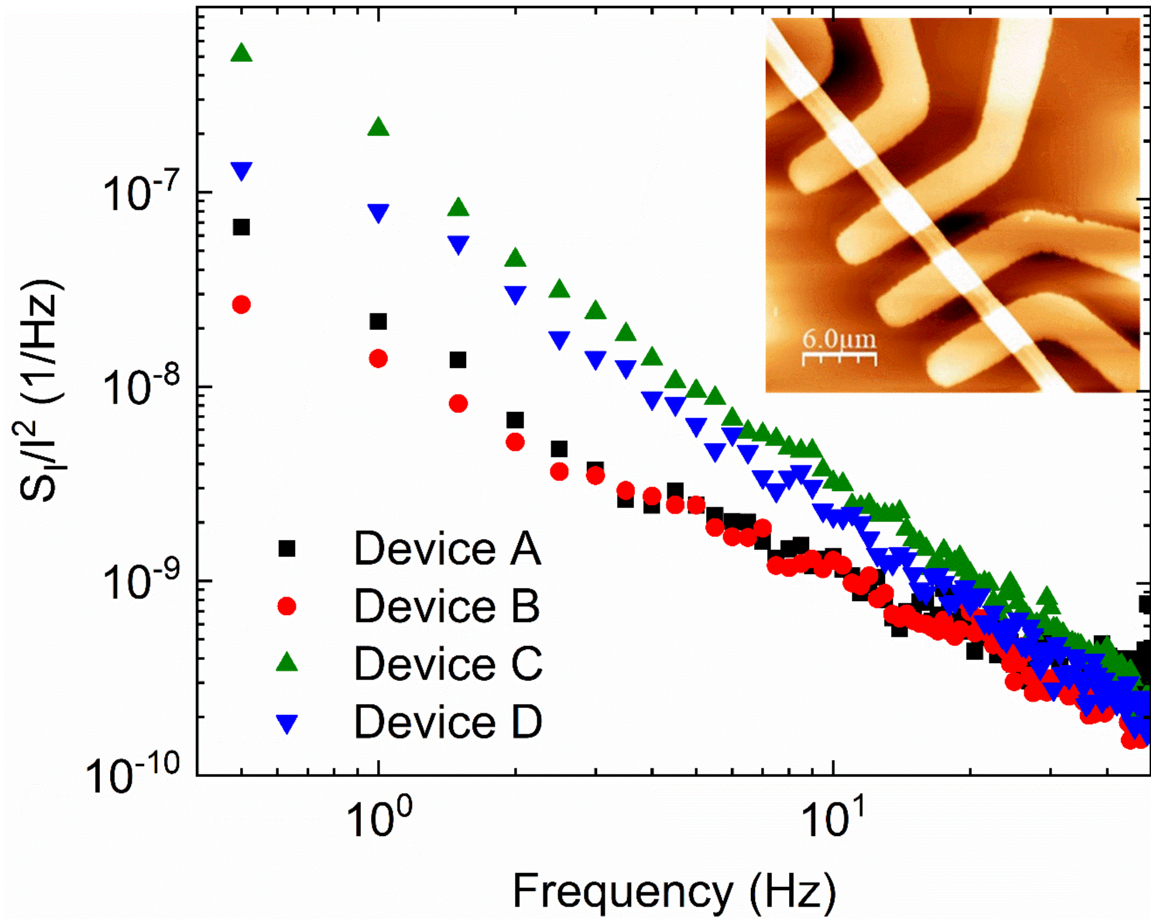

Figure 2.4 Normalized noise spectrum density as a function of frequency for $ZrTe_3$ nanoribbon devices with a cross-section ranging from ~27 nm × 450 nm to ~100 nm × 2000 nm. The inset shows an AFM image of the fabricated structure with the devices. Reprinted with permission from A. Geremew, M.A. Bloodgood, E. Aytan, B.W. Woo, S.R. Corber, G. Liu, K. Bozhilov, T.T. Salguero, S. Rumyantsev, M.P. Rao, and A.A. Balandin, IEEE Electron Device Lett. 39, 735 (2018). Copyright (2018) IEEE.

Figure 2.4 shows the noise characteristics of quasi-1D $ZrTe_3$ nanoribbons measured at room temperature. LFN is of 1/f type (f is the frequency). The noise spectral density $S_I/I^2 \approx 10^{-8}$ - 10^{-7} Hz^{-1} at f=1 Hz is comparable to that in some other low-dimensional materials. It scales with resistance, R, as $\sim 10^{-11} \times R$, following the trend observed for carbon nanotubes, graphene and metallic nanowires.[8] The noise level can be expected to decrease further with improved material quality. Figure 2.5 shows the normalized resistance versus

temperature of $ZrTe_3$ nanoribbon devices with different dimensions ranging from ~25 nm (thinnest) and as thick as ~105 nm. One should note that mechanical exfoliation is random in a sense it is practically difficult to precisely control both thickness and width simultaneously. In this report I focused on the effect of thickness on transport properties at different temperature. From the resistance versus temperature profile, one can see that the relative change of resistance with respect to temperature (dR/dT) varies among the different thickness nanoribbons. The slope of resistance versus temperature is steep for nanoribbons of ~25 nm thick and flat (dR/dT ~ 0) for ~105 nm thick nanoribbons which is bulk like property. For detail analysis, the curves were fit to power low ($R \sim T^{-\alpha}$) as is shown in Figure 2.5. Where α varies from 7 to 0 depending on the dimension of nanoribbons. For device A which is very thick (105 nm), α ~ 0 which can be seen from the dR/dT of the nearly flat curve which doesn't show a significant variation of resistance on temperature. For intermediate thickness nanoribbons (device, C, D and E) which are 70 nm to 88 nm thick, α ~ 3/2, and for thinner samples α ~ 4 (~33 nm to 50 nm) and for very thin quasi-1D $ZrTe_3$ nanoribbons (~25 nm), α ~ 7. This power-law dependence of resistance on temperature in quasi-1D system is expected but seen for the first time in quasi-1D $ZrTe_3$ nanoribbons. The temperature power α increases from 0 to 7 as thickness of nanowires decrease from ~105 nm to ~25 nm. Unlike $ZrTe_3$ phase, this model for 1D disordered conductor only applies to low electron density 1D systems. Another possibility is the effect of impurities and surface oxidation. If the impurity concentration in the channel is sufficient for overlapping of Friedel oscillation, then impurity induced CDW like state with a pseudo gap in the electron spectrum arises and a respective nonmetal temperature

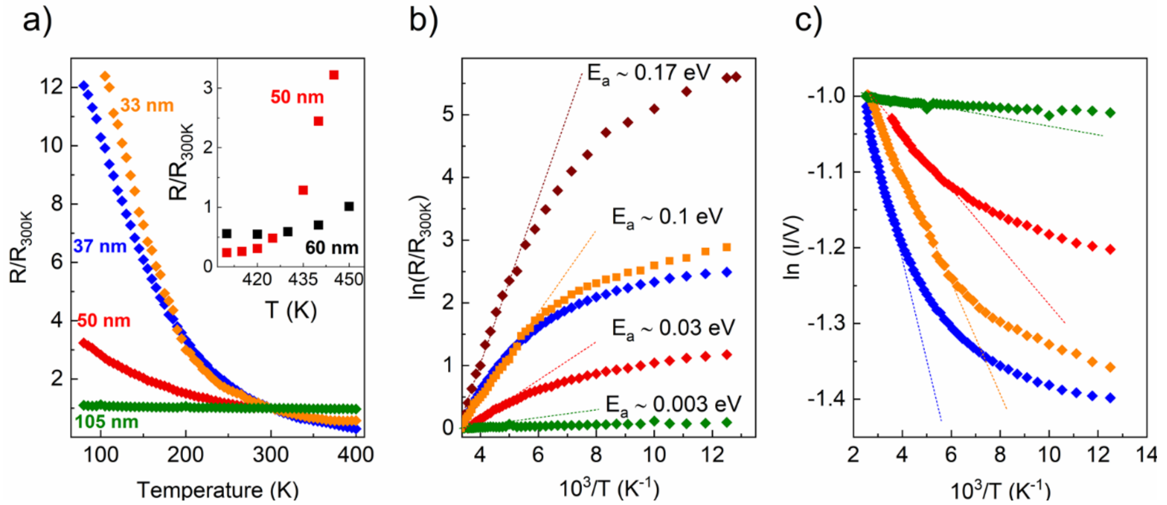

Figure 2.5 (a) Normalized resistance versus temperature of quasi-1D $ZrTe_3$ devices fabricated on different nanoribbons. The inset shows $ZrTe_3$ show the expected metallic property at room temperature and above. The most remarkable behavior is showing a strongly semiconducting behavior at low temperatures when the number of parallel chains decreases, i.e. as the dimension of the nanowires decrease, numerical fitting of resistance versus temperature profile and activation energies of $ZrTe_3$ phase-A devices. The thinner samples show lower exponent value in the power-law dependence.

performed under vacuum which means oxidation of sample is negligible. Hence, a comprehensive model for quasi-1D $ZrTe_3$ that includes parameters as interaction among metallic chains, dislocation, confinement, and the low electron concentration. Furthermore, IV curves of some of the very thin nanoribbons show some nonlinear property ($I \sim V^{\beta}$) and this non-linearity is significant at low temperatures (80 K). One can think that this IV non-linearity at low temperature could arise from the interface. However, the metal-nanoribbon interface is transparent. Ohmic characteristics of the IV curves at room temperature is also observed. Therefore, the non-metallic behavior at low temperature seen for the thin nanoribbons devices is not an effect of the interface. This could be explained by decreasing dimensions of quasi-1D $ZrTe_3$ nanoribbons leads to a decrease in the pinning energy per correlation volume, there by promoting the phase slip process which causes fluctuation of

conductivity and non-linearity.[24–26] The power-law dependence of resistance on temperature for quasi-1D $ZrTe_3$ arises from reduction of thickness below ~50 nm suggesting the low electron density at low temperatures dominate the transport property of the nanoribbon. Our transport data shows that these carriers govern the transport and the metal to nonmetal transition.

2.5 Conclusions

I investigated the current carrying capacity of nanoribbons made from $ZrTe_3$, a quasi-1D van der Waals material. The nanoribbon devices revealed an exceptionally high current density, on the order of ~100 MA/cm^2, at the peak of the stressing DC current. Our results suggest that quasi-1D van der Waals materials that consist of single crystals composed of MX_3 atomic threads have potential for applications in future downscaled electronic technologies. Furthermore, the dimension dependent transport properties for $ZrTe_3$ nanoribbons is observed at low temperature fit to the power-law dependence of resistance on temperature $R \sim T^{-\alpha}$ which is a characteristic of quasi-1D systems. Very thin nanoribbons (~25 nm) show the highest power factor of $\alpha \sim 7$, 33-50 nm nanoribbons show $\alpha \sim 4$, ~70-80 nm nanoribbons show $\alpha \sim 3/2$, and thickest nanoribbons (~105 nm) did not show significant temperature dependence. The physical mechanism of this phenomena could be explained by a combination of models but not a specific model can exactly explain our experimental results. Furthermore, the properties of the $ZrTe_3$ nanoribbons can be realized depending on which scattering mechanism is dominant among system parameters like, type of screening, impurity level, electron phonon, electron-electron interactions and other scattering mechanisms.[27–30]

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3. Low-frequency noise in quasi-1D materials

3.1 Introduction to low-frequency noise in quasi-1D $ZrTe_3$

Two-dimensional (2D) materials[3] such as graphene and TMDs with MX_2 type structure (where M = many transition metals; X = S, Se, Te) have revealed new physics and demonstrated potential for practical applications.[1–11] In recent years, interest in layered van der Waals materials has expanded to include quasi-one-dimensional (1D) structures and compositions. Unlike the layered MX_2 materials that yield 2D nanometer thickness sheets upon exfoliation, TMT contain 1D motifs, *i.e.* atomic threads, that are weakly bound together by van der Waals forces. Examples include TiS_3, NbS_3, and $TaSe_3$.[12–14] As a consequence of their structures, the mechanical exfoliation of MX_3 crystals results in nanowires and nanoribbons rather than 2D layers. In principle, the quasi-1D materials can be exfoliated or grown into ultimately downscaled nanowires, with the cross-sectional dimension of 1 nm × 1 nm, corresponding to the individual atomic thread. Some of the quasi-1D nanomaterials reveal an exceptionally high current density. For instance, quasi-1D $TaSe_3$ nanowires capped with *h*-BN layers have a breakdown current density exceeding J_B~10 MA/cm^2, which is larger than what can be sustained by the state-of-the-art Cu interconnects.[15] In a recent contribution, I reported uncapped $ZrTe_3$ nanoribbons with an even more impressive breakdown current density of J_B~100 MA/cm^2 [16], which is more than an order of magnitude larger than the value obtained in DC testing of Cu wires.[17,18] Results

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pertaining to the low-frequency current fluctuations, *i.e.* electronic noise, in $ZrTe_3$ nanoribbons are reported. The low-frequency noise is a ubiquitous phenomenon, present in all kinds of electronic materials and devices.[19–21] Practical applications, even for high-frequency devices, require the reduction of low-frequency noise to an acceptable level, due to possible up-conversion of the low-frequency noise to the phase and amplitude noise of the high-frequency devices. Additionally, the specific features of the low-frequency current fluctuations can provide valuable information about electronic transport, typical defects, grain boundaries, and charge carrier recombination dynamics.[20,22–26] The frequency, bias and temperature dependences of the low-frequency noise spectral density have been used as reliability metrics for devices and interconnects by the electronics industry.[27–30] For these reasons, our study is important for the proposed applications of quasi-1D $ZrTe_3$ nanoribbons in ultimately downscaled device channels and interconnects. From the fundamental science point of view, characterization of the low-frequency current fluctuations can shed light on the electron transport properties of $ZrTe_3$. The investigation is focused to room temperature (RT) and below to elucidate the physical mechanism of the current fluctuations and determine possible activation energies for various processes contributing to the noise. The results indicate that the normalized low-frequency noise spectral density, S_I/I^2, reveals 1/f behavior near RT (I is the current and f is the frequency). However, at lower temperatures, the noise spectral density is dominated by the Lorentzian bulges of the generation–recombination (G-R) noise. Interestingly, the corner frequency of the observed Lorentzian peaks shows strong sensitivity to the applied source–drain bias. Similar to the other group IV MX_3 materials, $ZrTe_3$ crystallizes in the monoclinic space

group $P2_1/m$ with Z = 2. Early work suggested the existence of $ZrTe_3$ polymorphs A and B. However, later studies confirmed only the original crystal structure A.[31–34] As illustrated in Figure 2.1a, this structure is composed of pairs of trigonal prismatic $ZrTe_3$ columns extending along the *b*-axis. These columns are stacked in layers along the *c*-axis, which are weakly bound by van der Waals forces. An additional unique feature is significant Te–Te···Te–Te interactions along the *a*-axis. As a result, $ZrTe_3$ exhibits more 2D character than many other MX_3 compositions and thus can be more completely considered a quasi-1D/2D material.

3.2 Experimental methods

$ZrTe_3$ nanoribbons were mechanically exfoliated from the bulk crystals and transferred to Si/SiO_2 substrate. I utilized the shadow mask method to fabricate the prototype interconnects. By allowing direct deposition of metallic contacts onto pre-selected $ZrTe_3$ nanoribbons, this method avoids the damage and chemical contamination typically associated with conventional lithographic lift-off processes, and it also drastically reduces the total air exposure time (<2 hrs., compared to 2 – 3 days for conventional lithography processes). The shadow masks were fabricated using double-side polished Si wafers with 3 µm thermally grown SiO_2 (Ultrasil Corp.; 500-µm thickness; P-type; <100>). The shadow mask fabrication process began with evaporation of 200 nm Chromium (Cr) on the front side of the wafer, followed by stencil mask patterning of this layer using a combination of electron beam lithography and Cr etchant (1020A). This was followed by fluorine-based reactive ion etching (RIE) to transfer the pattern to the underlying SiO_2. Finally, the pattern was transferred into the underlying Si substrate using deep reactive ion

etching (DRIE) (Silicon Trench Etch System; Oxford Cobra Plasma Lab Model 100). The DRIE etch step was timed to break through to a large backside window that was previously defined using lithographic patterning, RIE, and DRIE. The completed shadow masks were used to fabricate $ZrTe_3$ devices by aligning them with pre-selected nanoribbons on the device substrate, clamping the aligned mask and device substrate together, and placing the clamped assembly in an electron beam evaporator (EBE) for contact deposition (10 nm Ti and 100 nm Au). The completed devices were then transferred to another vacuum chamber for electrical characterization. Noise measurement procedures**:** The noise spectra were measured with an in-house built experimental setup, using a dynamic signal analyzer (Stanford Research 785), after signal amplification by the low-noise amplifier (Stanford Research 560). In order to minimize the 60 Hz noise and its harmonics, the voltage bias to the devices was applied using a battery biasing circuit. The devices were connected with the Lakeshore cryogenic probe station (TTPX). All current-voltage characteristics were measured in the Lakeshore cryogenic probe station with a semiconductor properties analyzer (Agilent B1500). The dynamic signal analyzer measured the absolute voltage noise spectral density, S_V, of a parallel resistance network of a load resistor, R_L, and device under test, R_D. The noise measurement system and experimental procedures have been validated with the experiments on other materials and devices [35–43].

3.3 Results and discussion

The intriguing properties of $ZrTe_3$ at low temperatures have been studied extensively. The bulk material is metallic with a CDW transition at 63 K and a superconducting (SC) transition at 2 K[16,44,45]. The electrical responses caused by the CDW and filamentary SC

states occur primarily along the *a*-axis, *i.e.* perpendicular to the $ZrTe_3$ columns, due to the pronounced Te–Te···Te–Te interactions. Numerous reports describe the effects of pressure,[46,47] magnetic field,[48] metal intercalation e.g., $Ni_{0.01}ZrTe_3$,[49] and chemical substitution e.g., $ZrTe_{3-x}Se_x$[50] on the CDW and SC properties of $ZrTe_3$. Notably, these studies were all based on bulk samples, thus the impact of nanoscale dimension on the properties of $ZrTe_3$ is not yet understood. Nanostructure–substrate interactions, strain, electron and phonon confinement, and defects can affect resistivity dependence on temperature and the type of electrical conduction, *e.g.* metallic *vs.* semiconducting. For this study, crystals of $ZrTe_3$ were prepared by iodine-mediated chemical vapor transport (CVT). The crystal structure was confirmed by single crystal X-ray diffraction. The resulting high-quality dataset provided a unit cell and atomic coordinates that are in excellent agreement with $ZrTe_3$ type A. Nanoribbons were obtained by the standard mechanical exfoliation method. The quality of $ZrTe_3$ nanoribbons was assessed by high-resolution transmission electron microscopy (HRTEM). As shown in Figure 3.1 b-c, HRTEM reveals large regions of defect-free $ZrTe_3$. The atomic distances are consistent with the angled array of $ZrTe_3$ columns illustrated in Figure 3.1 a. Figure 3.1d shows selected area electron diffraction (SAED) which is consistent with single crystalline nanoribbon quality. Furthermore, the material was evaluated by energy dispersive spectroscopy (EDS) and Raman spectroscopy.[16]

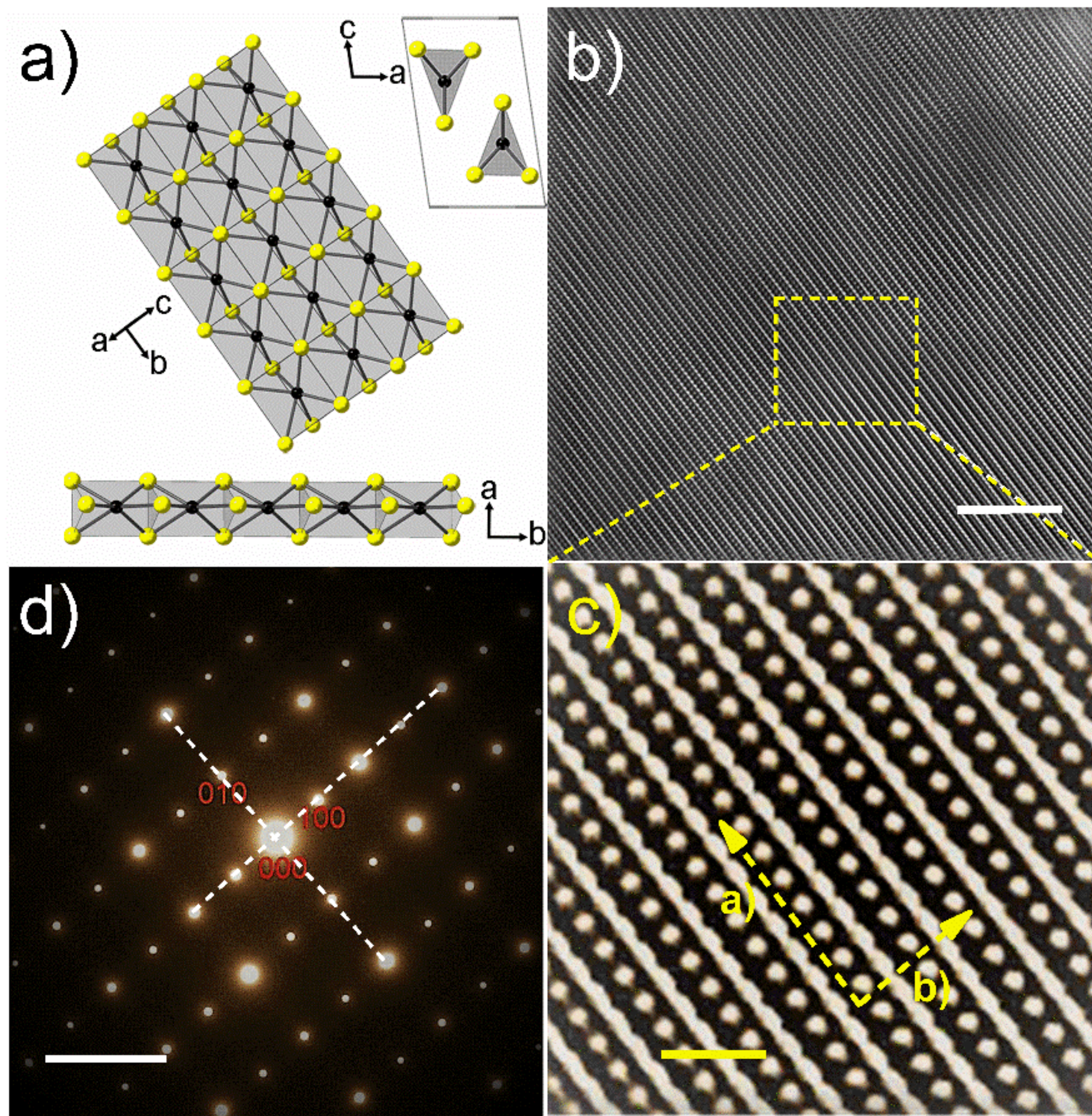

Figure 3.1 (a) Views of the structure of $ZrTe_3$. (b) HRTEM of a $ZrTe_3$ nanoribbon that shows a representative defect-free region. (c) Higher magnification HRTEM of $ZrTe_3$ with the orientation of atoms illustrated by the array of columns in panel a. (d) Selected area electron diffraction pattern along the (001) zone axis. This pattern was used to determine the lattice constants in the unit cell of $ZrTe_3$, which were consistent with the single crystal x-ray structure. The scale bar for (b), (c) and (d) are 7 nm, 1 nm and, 1 nm^{-1} respectively. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

The devices were fabricated by the shadow mask method on the mechanically exfoliated quasi-1D nanoribbons placed on a Si/SiO_2 wafer.[16] Owing to a direct deposition of the metal contacts onto the pre-selected $ZrTe_3$ nanoribbons, the shadow mask method allows one to avoid the damage and chemical contamination associated with the conventional lithographic lift-off processes. It also drastically reduces the total air exposure time during the fabrication. The shadow masks were fabricated using the double-side polished Si wafers with 3 μm thermally grown SiO_2 (Ultrasil Corp.; 500-μm thickness; p-type; <100>). The details of the shadow mask fabrication are provided in the Methods section. The contact metals Ti/Au (10:100 nm) were evaporated through a shadow mask, forming a testing device structure. The devices were transferred to another vacuum system for the electronic transport measurements. Figures 3.2 (a) and (b) show the optical microscopy of exfoliated nanoribbons of $ZrTe_3$ on Si/SiO_2 substrate and the atomic force microscopy (AFM) image of the fabricated device structure (device dimensions are approximately 50 nm × 200 nm), respectively. In Figure 3.2 (c), $ZrTe_3$ channel resistance, R, as a function of temperature, T is plotted. The inset shows the low-field current-voltage (I-V) characteristics of the device. The low-field I-Vs confirm the Ohmic characteristics of the contacts. The multi-gate design of the device under test allowed us to extract the contact resistance, R_C, confirming that it is negligible compared to the channel resistance: $2R_C \leq 1.1\% \times R_T$, where the total resistance $R_T = R + 2R_C$. As the temperature increases from T=100 K to T = 300 K, the resistance of $ZrTe_3$ nanoribbon decreases, suggesting semiconducting behavior. Although bulk $ZrTe_3$ has been described previously as metallic or semi-metallic,[33,44,51,52] a band gap may open due to tensile strain or other electronic effects

related to nanostructuring. Notably, $NbSe_3$ also exhibits a dramatic change from metallic behavior in the bulk state to nonmetallic in nanowire form.[53,54] The low-frequency noise measurements were performed in the temperature range from 77 K to 298 K under high vacuum. The devices were biased with a silent battery and a potentiometer biasing circuit and measured using a low noise amplifier and a spectrum analyzer. Details of our experimental procedures, in the context of different devices, were reported by us elsewhere.[35–40] The noise spectra were acquired at a low bias voltage to avoid Joule heating.

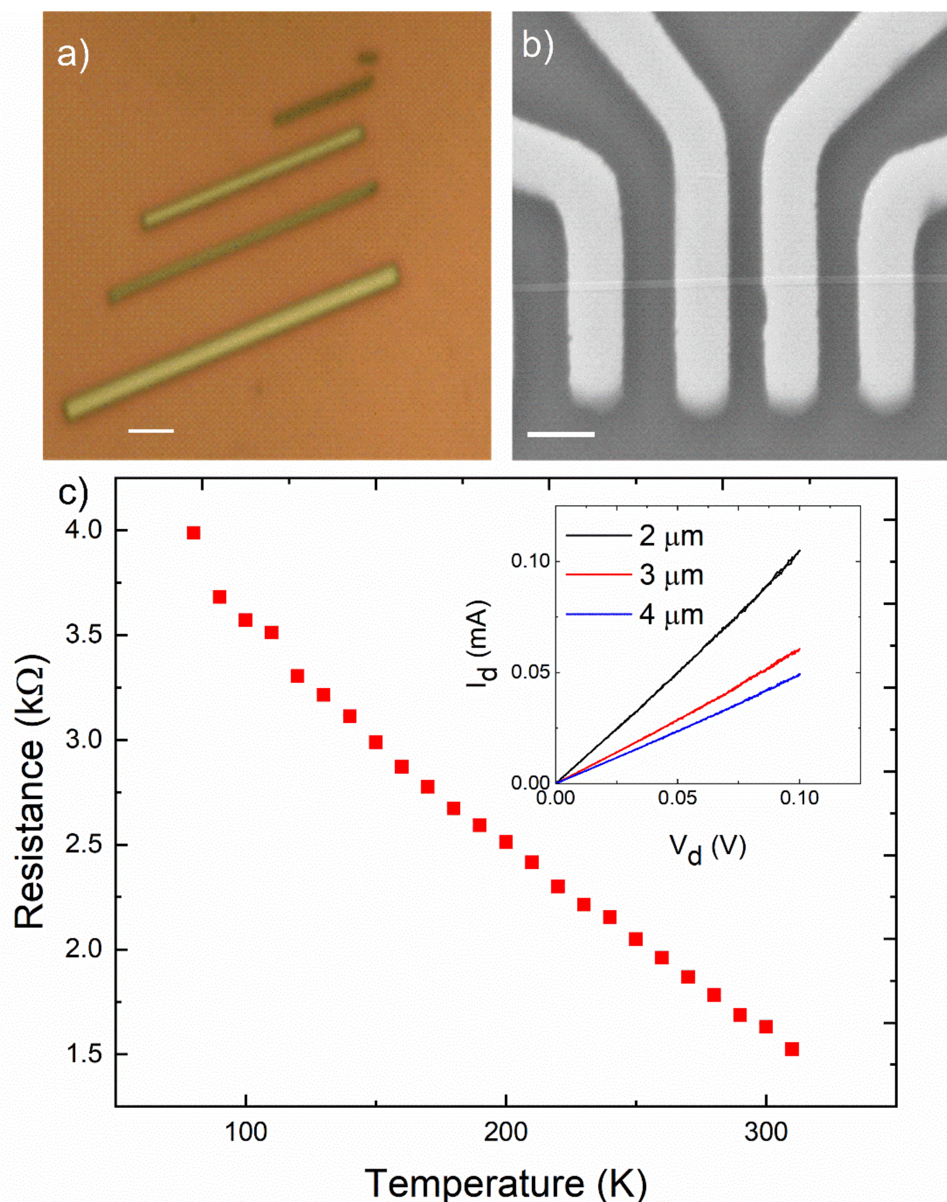

Figure 3.2 (a) Optical microscopy image of the mechanically exfoliated $ZrTe_3$ ribbons on SiO_2/Si substrate. Different colors, green vs. gold, indicate the variation in the thickness of the nanoribbons. The scale bar is 1 μm. (b) Scanning electron microscopy image of a device fabricated from the quasi-1D $ZrTe_3$ nanoribbon with the thickness of ~50 nm. The scale bar is 2 μm. (c) The resistance of the quasi-1D $ZrTe_3$ nanoribbon as a function of temperature. The inset shows low-field I-Vs for representative devices of different lengths, as proof that the fabricated contacts were Ohmic. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

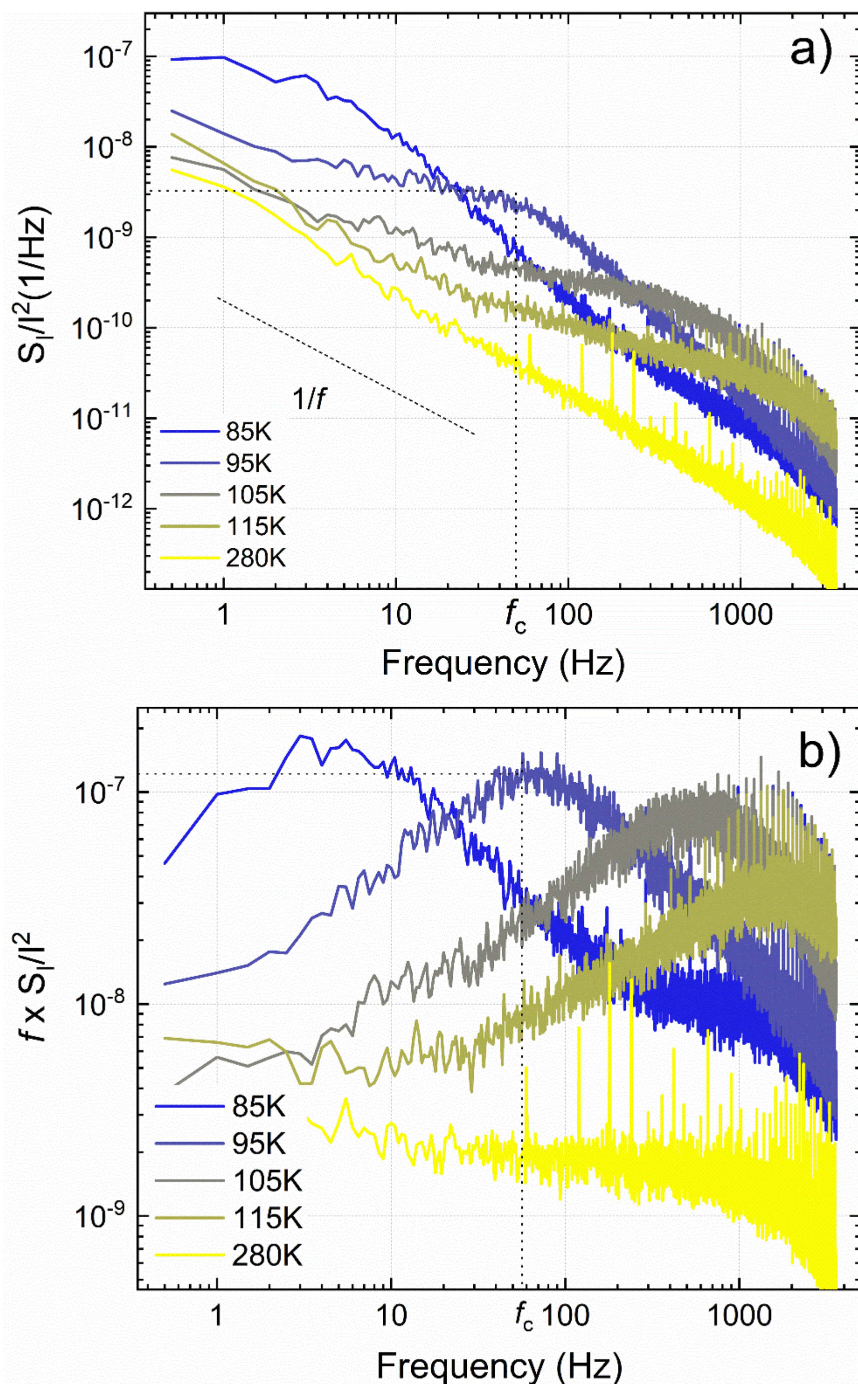

Figure 3.3 (a) Normalized noise spectral density, S_I/I^2, as a function of frequency of quasi-1D $ZrTe_3$ nanoribbon at temperatures from 85 K to 280 K. (b) Normalized noise spectral density multiplied by frequency, $S_I/I^2 \times f$, as a function of frequency. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

Figure 3.3 (a) shows the normalized noise spectral density, S_I/I^2, as a function of frequency at different temperatures. Since the contact resistance of the tested device was negligible, the noise response is dominated by the channel. The main observation is that at low temperatures the noise spectrum consists of the bulges of the G-R noise, typical for semiconductors.[55–57] As the temperature increases, the bulges shift to a higher frequency, eventually disappearing or moving outside of the examined frequency range, when temperature approaches RT. Near RT, the noise spectrum becomes $1/f^{\gamma}$ type with $\gamma \approx 1$, which is characteristic for both metals and semiconductors as well as majority of electronic devices.[25] In Figure 3.3 (b), $S_I/I^2 \times f$ as a function of temperature is plotted in order to compensate for 1/f noise background and make the G–R peak shift with the temperature more visible. The overall noise level is rather small. The normalized noise spectral density, $S_I/I^2 \approx 10^{-10}$ Hz^{-1} at f=10 Hz and temperature T=280 K. The existence of the G–R noise is independent proof that quasi-1D $ZrTe_3$ nanoribbons demonstrate semiconducting behavior within the given temperature range. In semiconductors, G–R noise is observed at low-frequency and its spectral density is described by the Lorentzian: $S_I(f) = S_0/[1 + (2\pi f\tau)^2]$, where S_0 is the frequency independent portion of $S_I(f)$ observed at $f << (2\pi\tau)^{-1}$ and τ is the time constant associated with the return to the equilibrium of the occupancy of the level. In a typical situation of the semiconductor doped with the shallow, fully ionized donor or acceptor, and another noisy deep level, the spectral density of the G–R noise is given by,[58]

$$\frac{S_I}{I^2} = \frac{4N_t}{Vn^2}\frac{\tau F(1-F)}{1+(\omega\tau)^2} \tag{3.1}$$

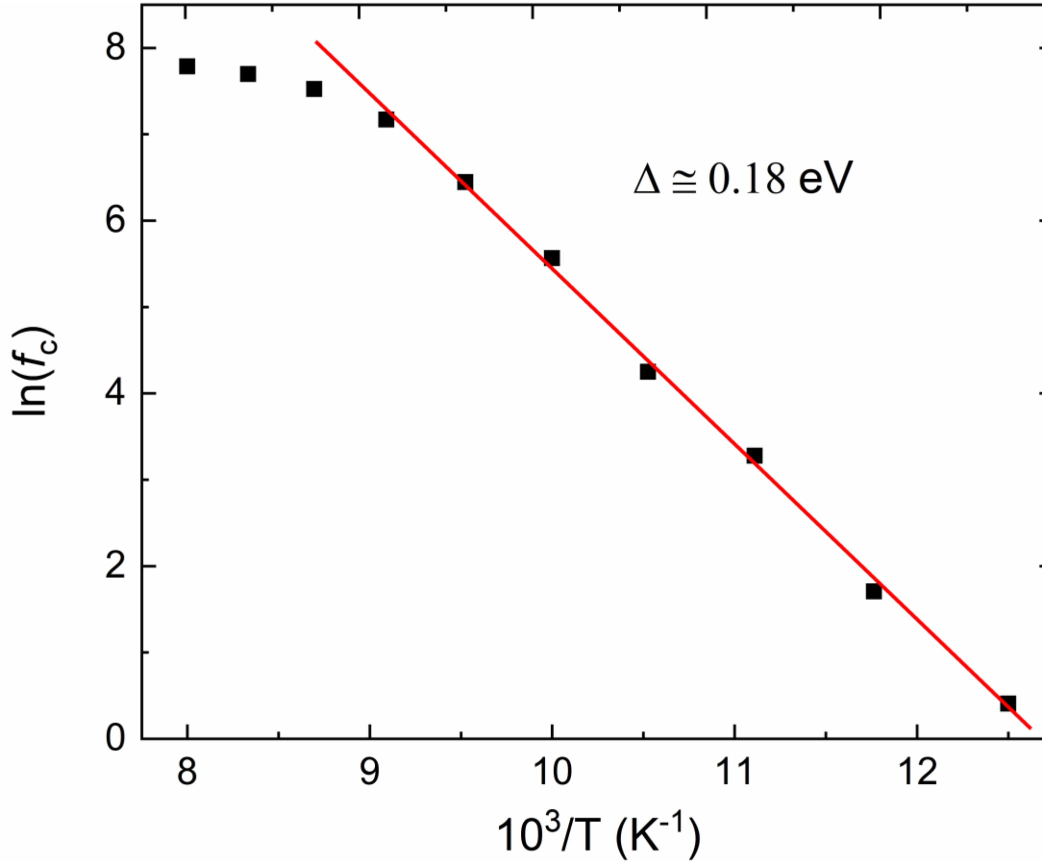

Figure 3.4 Arrhenius plot of the characteristics frequency, ln(f_c), as a function of the inverse temperature, in quasi-1D $ZrTe_3$ device. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

here ω = 2πf, V is the sample volume, n is the equilibrium electron concentration for the n-type semiconductor, and F is the trapping state occupancy function. The G–R noise time constant, τ, is expressed in terms of the trapping state capture, τ_c, and emission, τ_e, time constants:

$$\frac{1}{\tau} = \frac{1}{\tau_c} + \frac{1}{\tau_e} \tag{3.2}$$

which are given by:

$$\tau_c = \frac{1}{\sigma v_T n} \tag{3.3}$$

$$\tau_e = \frac{1}{\sigma v_T N_c \exp\left(-\frac{E_0}{kT}\right)} \tag{3.4}$$

Here σ is the capture cross section of the trap, v_T is the electron thermal velocity, N_c is the effective electron density of states (DOS) in the conduction band, and E_0 is the trap level position, relative to the conduction band. Note that Eqs. (3.2) - (3.4) are written for the n-type semiconductor. The equations for the p-type semiconductor are analogous. As seen from Eq. (3.4), if the emission time dominates, the characteristic time τ depends on temperature exponentially and the energy E_0 can be extracted from the experimental data. Usually ln(τ) or (f_c=(1/2πτ)) is plotted as a function of 1/T. If the temperature dependences of the thermal velocity and DOS are significant, $\ln(T^2\tau)$ can be plotted as a function of 1/T. The slope of this Arrhenius plot defines the energy E_0. Figure 3.4 shows the Arrhenius plot of the characteristics frequency f_c for the experimental data shown in Figure 3.3 (b). The trap activation energy, extracted from Figure 3.4, is $E_0 \cong 0.18$ eV. The activation energy obtained by this method is often associated with the energy level position of a given trapping state. However, this is not always the case. The caption cross-section of the trap levels, σ, often depends exponentially on temperature[26,59].

$$\sigma = \sigma_0 \exp\left(-\frac{E_1}{kT}\right) \tag{3.5}$$

In such cases, the procedure, described above, yields the sum of the activation energies, E_0+E_1, rather than E_0. The activation energies E_0 and E_1 cannot be found separately in this approach. The method to find the energies E_0 and E_1 separately was proposed in Ref.[55] This method requires to plot the spectral noise density versus temperature T at a series of

frequencies. The temperature dependence of the noise for each frequency has a maximum at $T=T_{max}$. As the next step, the dependence of the noise at the point of maximum, $\ln(S_{max})$, is plotted versus $\ln\omega$, where $\omega=2\pi f$. The slope of this dependence is defined by the energies E_0 and E_1, which can be found separately. This method was developed for the case when the semiconductor is doped with a shallow donor center, which is fully ionized at all temperatures of the experiment. The concentration of the traps at this level is high enough so that the electron concentration does not depend on temperature, and this concentration is much higher than the concertation of the noisy deep levels. As one can see from Figure 3.2 (c), the resistance of the sample decreases with increasing temperature, which is an indication of the free carrier concentration temperature dependence. However, while the characteristic frequency of the G–R noise changes with temperature more than two orders of magnitude the change of the resistance, and concertation, is only a factor of ×2.5. Therefore, the temperature dependence of the resistance can be neglected and concentration in our analysis and use the method of Ref. [46]. Figure 3.5 shows the normalized noise spectral density, S_I/I^2, as a function of temperature for different frequencies. As temperature increases, the noise peak shifts to higher temperatures. The blue line and data points in Figure 3.6 show the dependence of $\ln(S_{max})$ versus $\ln\omega$. The slope of this dependence $A=\delta(\ln(S_{max}))/\delta(\ln\omega)\cong1.24$. In accordance with the model of Ref. [55], $A>1$ is an indication that the level is located above the Fermi level and $A=(2E_0+E_1)/E_0+E_1)$. The red line and data points in Figure 3.6 shows the Arrhenius plot of the invers temperature (1/T) as a function of $\ln\omega$. The frequency of each red data point in Figure 3.6 corresponds to f_c at temperature T_{max}. The slope of the Arrhenius plot, $1/kT_{max}$

versus $\ln\omega$ is $B=\delta(1/T_{max})/\delta(\ln\omega)\cong 1/(E_0+E_1)$. The extracted activation energy from the linear fitting gives 0.19 eV, which, within the experimental error, matches the activation energy extracted from Figure 3.4. With the known A and B, the activation energy of the cross-section temperature dependence and level position can be extracted as E_1=0.144 eV and E_0=0.0456 eV. These data indicate that the activation energy of the characteristic frequencies of the G–R noise peaks in quasi-1D $ZrTe_3$ nanoribbons is dominated by the activation energy of the capture cross-section temperature dependence. I measured the noise at low temperature (T=77 K) as a function of the source – drain bias. Figure 3.7 (a) shows the normalized noise spectral density, S_I/I^2, as a function of frequency at different

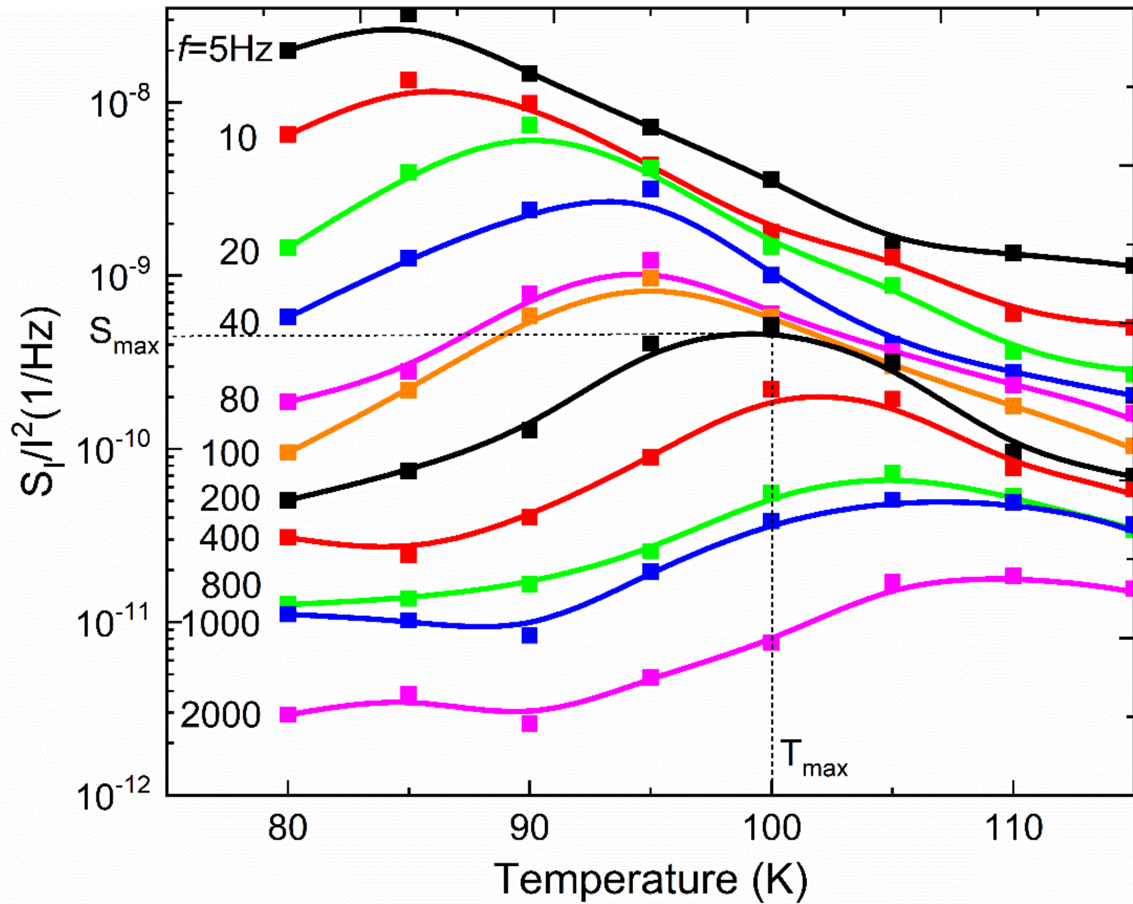

Figure 3.5 Normalized noise spectral density, S_I/I^2, as a function of temperature for different frequencies. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

source-drain voltages, V_{SD}. In Figure 3.7 (b), I present $S_I/I^2 \times f$ in order to compensate for 1/f noise background and make the peak shift with the electric bias more visible. As seen from Figure 3.7, the characteristic frequency f_c changes about three orders of magnitude when the bias voltage increases from 45 mV to 250 mV. In general, the shift of the Lorentzian peak in the noise spectrum with the applied electric field can be attributed to reduction of the impurity barrier potential in the high electric field, which is known as the Poole–Frenkel effect.[60]

$$\Delta E_{fp} = \left(\frac{q^3 F}{\pi \varepsilon_0 \varepsilon}\right)^{1/2} \qquad (3.6)$$

Here ΔE_{fp} is the reduction of the barrier, q is the charge of an electron, F is the electric field, ε_0 is the permittivity of free space, and ε is the relative dielectric constant. Assuming that the characteristic frequency depends on the energy exponentially, I estimated that the electric field required to shift this frequency by three orders of magnitude is on the order of 50 kV/cm. For the 2-μm length nanoribbon in our devices, the average field in the sample does not exceed ~1.25 kV/cm. However, the specific of the quasi-1D nanoribbon structure is that a defect can increase significantly the resistivity of the individual quasi-1D

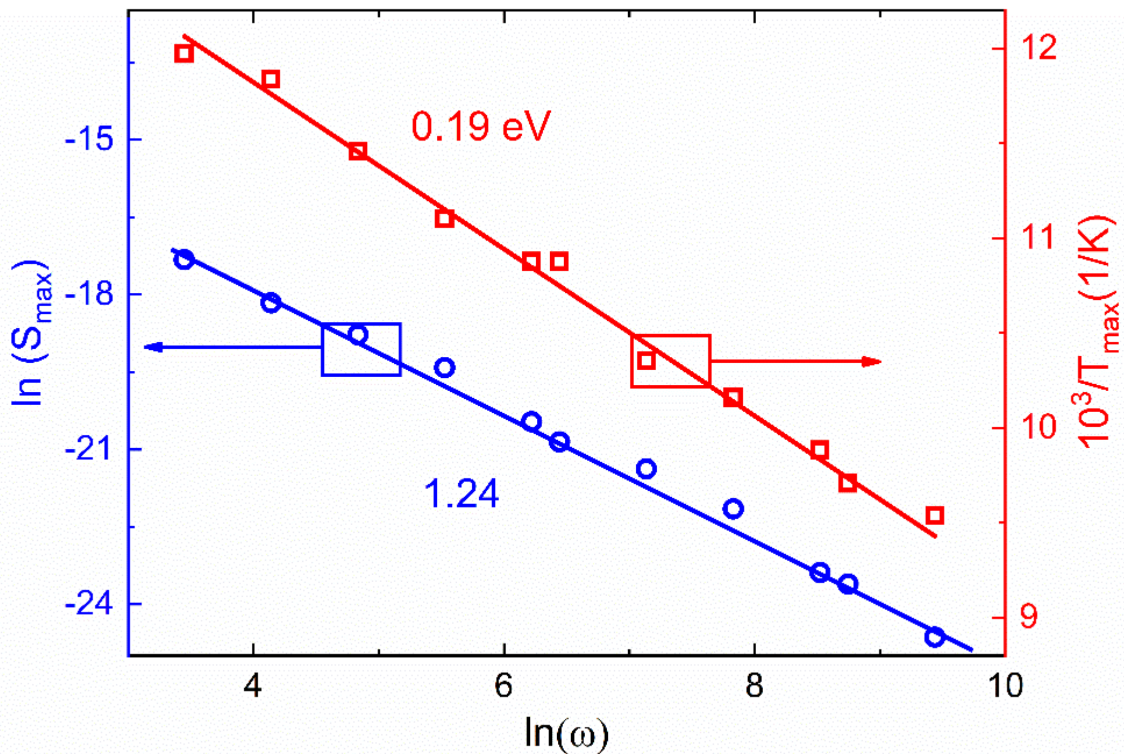

Figure 3.6 Maximum noise peak position, S_{max}, as a function of frequency (rad/sec) (blue curve). The extracted slope of the linear fitting is 1.24. The Arrhenius plot of the invers temperature (K^{-1}) as a function of frequency (rad/sec) (red curve). The extracted activation energy from the linear fitting is 0.19 eV. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

chains or even completely block it. Since the resistivity in the directions perpendicular to the atomic chain is much higher, the local field at a defect can be much higher than the average one. Most of the potential drop can happen on over the spatial extend of the defect. Assuming that the defect is a 1D line, the potential is estimated as $\varphi(x) \sim en(x) \ln (L_0/a)$, where n is the uncompensated charge in the wire, a is the diameter of the wire, and L_0 is the characteristic screening length which depends on the chain dimensions. The estimate is based on the gradual channel approximation.[60]

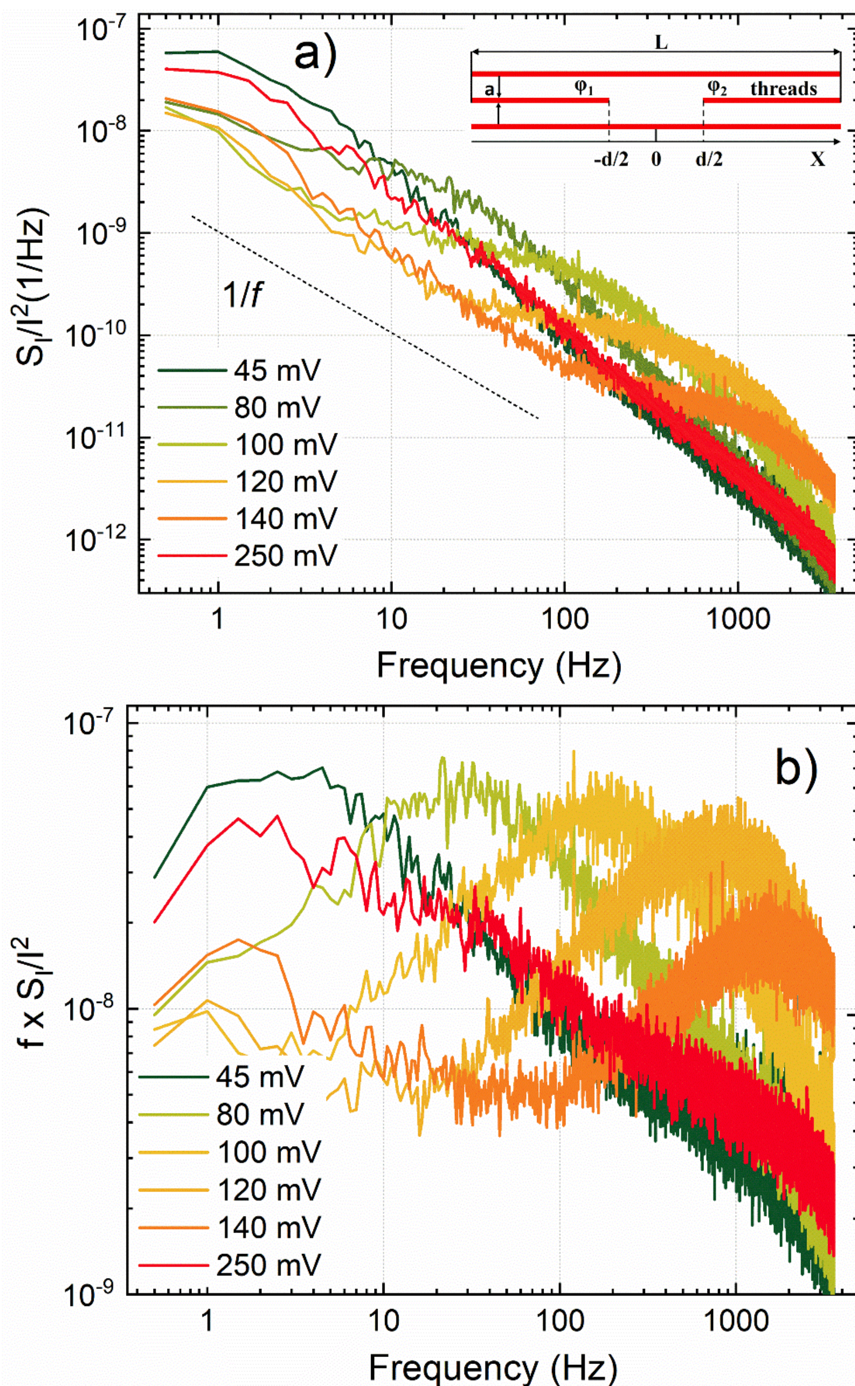

Figure 3.7 Normalized noise spectral density, S_I/I^2, as a function of frequency of quasi-1D $ZrTe_3$ at the bias voltage ranging from 45 mV - 250 mV. Inset shows a schematic of the atomic thread bundle with one broken thread. (b) Normalized noise spectral density multiplied by frequency, $S_I/I^2 \times f$, as a function of frequency. Reprinted with permission from A.K. Geremew, S. Rumyantsev, M.A. Bloodgood, T.T. Salguero, and A.A. Balandin, Nanoscale 10, 19749 (2018). Copyright (2018) Royal Society of Chemistry.

The electric field at the end of the defect is given by $F \sim en/(x - d/2)$. Then the electric field in the non-conducting gap, *i.e.* spatial extend of the defect, can be roughly estimated as:

$$F \cong \left(\frac{\varphi_1}{x+d/2} - \frac{\varphi_2}{-x+d/2}\right)\frac{1}{\ln L_0/a} \tag{3.7}$$

where φ_1 and φ_2 are the potentials on the wire (which represent a nanoribbon), and d is dimension of the non-conducting gap (see inset in Figure 3.7 (a)). From Eq. (6), the electric field in the middle of the gap, associated with the defect, is on the order of $2K(\varphi_1-\varphi_2)/d$, where $K \geq 1$ depends logarithmically on the specific geometry close to the defect. With the potential difference of 250 mV, the electric field of 50 kV/cm can be easily obtained for the gap of 100 nm. The actual defect size may be much smaller, and the electrical field, therefore, higher. This can explain the reduction of the barrier on the defect, and the resulting strong shift of the characteristic frequency as a function of bias, in accordance with the Poole–Frenkel effect. It is natural to assume that the observed strong bias dependence of the G–R noise can be a common feature of the quasi-1D crystals. It is interesting to note that the current-voltage characteristics are perfectly linear at the considered bias but the noise spectra clearly reveal this unusual effect.

3.4 Conclusions

I investigated the low-frequency electronic noise in quasi-1D $ZrTe_3$ van der Waals nanoribbons. Such nanostructures have recently attracted attention owing to their extraordinary high current carrying capacity. Whereas the low-frequency noise spectral

density, reveals 1/f behavior near RT, it is dominated by the Lorentzian bulges of G–R noise at low temperatures. The corner frequency of the Lorentzian peaks shows strong sensitivity to the applied source–drain bias. This dependence on electric field can be explained by the Frenkel–Poole effect if one assumes that the voltage drop mostly happens on the defects, which block the quasi-1D conduction channels. The observed strong bias dependence of the G–R noise can be a common feature of the quasi-1D crystals. The activation energy of the characteristic frequencies of the G–R noise in quasi-1D $ZrTe_3$ is primarily defined by the temperature dependence of the capture cross-section of the defects rather than by their energy position. The activation energy of the cross-section temperature dependence and level position were found to be E_1=144 meV and E_0=45.6 meV, respectively. These results are important for the proposed applications of quasi-1D van der Waals materials in ultimately downscaled electronics.

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4. Bias-voltage induced phase transitions

4.1 Bias-voltage induced phase transitions in 1T-TaS_2

Switching between various material phases at room temperature by the application of electric field has the potential of becoming a new device paradigm for future electronic and optoelectronic technologies.[1–4] Among the promising material candidates, which must exhibit phase changes characterized by abrupt resistivity changes and hysteresis, is the 1T polymorph of tantalum disulfide (TaS_2)[4]. The quasi-two-dimensional (2D) van der Waals layered crystalline 1T-TaS_2 exhibits CDW effects, *i.e.* periodic modulation of the charge density and the underlying lattice resulting from the interplay between the electron-electron and electron-phonon interactions.[5–13,14] The CDW state becomes fully commensurate with the lattice below ~ 200 K.[15–17] The commensurate CDW (C-CDW) consists of a $\sqrt{13} \times \sqrt{13}$ reconstruction within the basal plane that forms a star-of-David pattern in which each star contains 13 Ta atoms. The Fermi surface, composed of 1 *d*-electron per star, is unstable, so that the lattice reconstruction is accompanied by a Mott-Hubbard transition that fully gaps the Fermi surface and increases the resistance.[15,18–21] As the temperature increases above 180 K, the C-CDW phase breaks up into a nearly commensurate CDW (NC-CDW) phase that consists of ordered C-CDW regions separated by domain walls.[22] This C-CDW to NC-CDW transition is revealed as an abrupt change in the resistance with a large hysteresis window in the resistance profile at 200 K.

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As the temperature is increased to 350 K, the NC-CDW phase melts into an incommensurate CDW (I-CDW) in which the CDW wave vector is no longer commensurate with the lattice. This transition is accompanied by a smaller hysteresis window in the resistivity.[23,24] Only at high temperatures of 500 K – 600 K does the I-CDW phase melt into the metallic normal phase (NP) of 1T-TaS_2.[5] Until now, the transition from the I-CDW to the NP phases has been achieved only via heating of 1T-TaS_2 samples. Apart from temperature, various CDW phase transitions in 1T-TaS_2 and some related materials, *e.g.* 1T-$TaSe_2$, can be induced by external perturbations including doping,[7,17, 25–30] photoexcitation,[8,31] pressure,[5] carrier injection,[6,32] reduction of thickness,[33–35] electric field,[9,24,32] laser pulse,[8,36] and gate voltages.[32,37,38] The existence of several CDW phases, in addition to electrically driven switching among them within a short time scale, makes 1T-TaS_2 a particularly promising candidate for electronic device applications[6,32,39] even though the exact nature of these phases continues to be a subject of debate.[40–43] Major impetus for this research came from the demonstration of a 1T-TaS_2-based voltage controlled oscillator operating at room temperature (RT); this device utilizes the NC-CDW – I-CDW phase transition, which occurs at 350 K in the "low-bias" regime.[37] Here I refer to the resistivity as "low-bias" when it is measured at very low electric bias, *i.e.* few mV, to guarantee the absence of self-heating and thus preclude transitions induced entirely by the temperature change.[37,44] Subsequent work has focused on the implementation of such CDW devices for information processing[45,46] and radiation-hard applications.[47,48] It has been suggested that electric field and current not only interact with the CDW but also result in Joule heating, which in turn causes the phase transitions in 1T-

TaS_2.[49] The extent to which the electrical field by itself, versus self-heating associated with the current conduction, is responsible for inducing transitions between C-CDW and NC-CDW or NC-CDW and I-CDW is still under debate.[37,49,50] Moreover, although the electric field induced C-CDW to NC-CDW and NC-CDW to I-CDW phase transitions in 1T-TaS_2 have been reported by many groups[6,37,51] there have been no reports on the electric-field induced transition to the normal metallic phase. This situation can be attributed to the difficulty of reaching temperatures of T = 550 K - 600 K via self-heating due to the applied electric bias and the less pronounced change in the resistivity at the I-CDW – normal phase (NP) transition. The possibility of using the I-CDW – NP transition for devices is attractive, however, due to their anticipated radiation-hardness,[47,48] which stems from the inherent tolerance of metallic materials to radiation damage compared with semiconductors.

4.2 Synthesis of 1T-TaS_2 crystals

The samples for this study were provided by Professor Tina Salguero (University of Georgia). Briefly, tantalum (20.4 mmol, Sigma-Aldrich 99.99% purity), sulfur (41.1 mmol, J.T. Baker >99.9% purity), and iodine (J.T. Baker 99.9% purity, ~88 mg for an ampule with a ~14.0 cm^3 volume) were added to a ~18×1 cm^2 cleaned, dried, fused quartz ampule. After evacuation, filling with Ar, and sealing, the ampule was heated in a two-zone tube furnace at 10 °C min^{-1} to 975 – 875 °C (hot-cold gradient) for 1 week. The 1T-TaS_2 polymorph was isolated as golden, multi-millimeter-sized crystals by quenching the hot ampule in a water–ice–NaCl bath.

4.3 Device fabrication

I utilized the shadow mask method to directly deposit TLM structures onto pre-selected 1T-TaS_2 thin films obtained by mechanical exfoliation. The exfoliated layers of 50-60 nm were relatively stable in the air, which allowed us to use the shadow mask method.[52] The method allowed us to avoid the damage from chemical contamination, typically associated with conventional lithographic lift-off processes. It also drastically reduced the total air exposure time and the fabrication process. It takes less than an hour to fabricate a device by the shadow mask method, compared to 2-3 days required for the standard lithography process. The designed shadow masks of TLM configuration were fabricated using the double-side polished Si wafers with 3μm thermally grown SiO_2 on both sides (Ultrasil Corp.; 500 μm thickness; P-type; <100>). The shadow mask fabrication process began with evaporation of 200 nm thick chromium (Cr) film on the front side of the wafer, followed by a combination of electron beam lithography (EBL) and Cr etchant (1020A) to create TLM pattern. This was followed by the fluorine-based reactive ion etching (RIE) to transfer the pattern to the underlying SiO_2. Finally, the pattern was transferred into the underlying Si substrate using the deep reactive ion etching (DRIE) (Oxford Cobra). Since the 500 μm thick Si wafer is too bulky to etch through from the top, a large window was opened at the back side of the wafer by photolithography to remove the bulk Si until a thin Si membrane is left. Finally, The DRIE etch step was timed to break through the thin silicon membrane and release the stencil from the top. The shadow masks were directly used to fabricate plenty of devices by aligning them with pre-selected flakes on the device substrate using an optical microscopy, clamping the aligned mask and device substrate

together, and placing the clamped assembly in an electron beam evaporator (EBE) for contact deposition (10 nm Ti and 100 nm Au) through the mask openings. The completed devices were then transferred to another vacuum chamber for electrical characterization. The thickness and width of 1T-TaS_2 flakes were determined using AFM and SEM inspection.

4.4 Electronic noise measurements

The noise spectra were measured with a dynamic signal analyzer (CR 7458). To minimize the 60 Hz noise and its harmonics, I used a battery biasing circuit to apply voltage bias to the devices. The devices were connected to Lakeshore cryogenic probe station TTPX. All *I-V* characteristics were measured in the cryogenic probe station (Lakeshore TTPX) with a semiconductor analyzer (Agilent B1500). The noise measurements were conducted in the two-terminal device configuration but with different channel length to determine the contribution of contact noise. Since the contact resistance of the devices are very low, the extracted contact noise was lower than thermal noise and played has no significant contribution to the noise due to the channel. The dynamic signal analyzer measures the absolute voltage noise spectral density S_V of a parallel resistance network of a load resistor, R_L of 3.6 kΩ and device under test (DUT), R_D. The normalized current noise spectral density, S_I/I^2, is calculated after normalizing by the amplification of the low noise amplifier.

4.5 Finite-element simulations

To model the heat distribution in the TaS_2 channel, I used the finite element model,

implemented in COMSOL[5] Multiphysics package.[53] The simulated device geometry corresponds to an experimental sample, which has a 50 nm thick TaS_2 sample on top of a 4 μm thick Silicon substrate. Four 2.5 μm × 10 μm Au electrodes are placed on top of TaS_2, with inter-contact separations of 2.5 μm. Bias is applied between the two middle Au contacts. In the experiment, the C-CDW-NP transition happens for V= 1.69 V (19.25 mA) and 1.80 V (24.58 mA). Same electrical conditions are maintained in the simulation geometry. In case of thermal conduction, heat dissipation can be described by standard heat equation,

$$\rho C_p \frac{dT}{dt} = \nabla.(\kappa \nabla T) + q_e \qquad (4.1)$$

where, ρ is the mass density, C_p is the heat capacity, T is temperature, and κ is thermal conductivity. The left side of Eq. (4.1) will disappear under steady state condition. On the right side of Eq. (4.1), Joule heating is captured by the generation term, $q_e = J \cdot E = \sigma|\nabla V|^2$, where J is the current density, E is the electric field, σ is the electrical conductivity, and V is the applied bias. The generated heat will appear as an outward heat flux, giving rise to a thermal gradient, ∇T. The electrical conductivity of the TaS_2 channel is tuned to match the current and power density of the experimental sample. The thermal conductivity of TaS_2 is around 4-10 $Wm^{-1}K^{-1}$ [Ref. [54]]. For SiO_2 layer, the thermal conductivity is 1.4 $Wm^{-1}K^{-1}$ [Ref. [55]]. The metal contacts, as well as the bottom face of the Si substrate, are assumed to be always at room temperature. Radiating heat boundary conditions are applied

[5]The Finite-element simulations and analytical heat dissipation estimation are courtesy of Dr. Bishwajit Debnath, Laboratory for Terascale and Terahertz Electronics (LATTE), University of California Riverside and Dr Fariborth Kargar, Phonon Optimized Engineered Materials Center (POEM), University of California Riverside.

on the exposed TaS_2 and SiO_2 surfaces as, $\hat{n} \cdot \kappa \nabla T = \varepsilon\sigma(T_{env}^4 - T^4)$, where T_{env} is the ambient temperature, $\hat{n}$ is the surface normal and ε is the emissivity (0.8). All other surfaces are assumed to be thermally insulating ($\hat{n} \cdot \kappa \nabla T = 0$).

4.6 Results and discussion

In this section, I discussed inducing the I-CDW – NP transition by applying an in-plane electric field in 1T-TaS_2 devices on conventional Si/SiO_2 wafers, operating over a wide temperature range, including RT.[56] The measurements of the low-frequency electronic noise, i.e. current fluctuations, have been used to unambiguously observe the phase transitions, particularly the switching from the I-CDW to NP. The low-frequency noise, typically with the spectral density $S(f) \sim 1/f^{\gamma}$ (f is the frequency and parameter $\gamma \sim 1$), is found in almost all materials and devices.[57,58] Although practical applications can benefit from the reduction of the low-frequency noise, it also can be used as a characterization tool that reveals information about the physical processes in materials.[43,44,59,60] The electrical switching among three CDW phases and one normal phase of 1T-TaS_2 is demonstrated with the help of low-frequency-noise spectroscopy. The rest of the section is organized as follows. First, the material preparation, device fabrication, and resistivity measurements are briefly outlined. Second, low-frequency noise measurements are described in the context of monitoring phase transitions and carrier transport in CDW materials. Third, simulation of heat dissipation is used to assess the relative importance of the self-heating and electric field for inducing CDW and metallic phase transitions. Multi-millimeter-sized crystals of 1T-TaS_2 were synthesized by iodine-mediated CVT (Methods) and their quality was evaluated by X-ray diffraction, energy dispersive

spectroscopy, and other material characterization techniques, as previously detailed.[38,45] Thin layers of crystalline 1T-TaS_2 were cleaved by mechanical exfoliation and transferred to SiO_2/Si substrates. I intentionally used 1T-TaS_2 layers with thicknesses greater than 9 nm to preserve the C-CDW – NC-CDW phase transition. It is known that 1T-TaS_2 quasi-2D films with thicknesses approaching a monolayer do not reveal the C-CDW – NC-CDW transition.[23,37] The metal Ti/Au contacts were evaporated through a TLM structured shadow mask to avoid chemical contamination and oxidation during the fabrication process. After the contact evaporation, the devices were transferred to another vacuum chamber for transport measurement. A large number of 1T-TaS_2 devices were fabricated and tested. Figure 4.1 (a) shows optical microscopy image of a representative device. All current-voltage (I-V) characteristics and resistivities were measured in the cryogenic probe station with a semiconductor analyzer. The low-frequency noise experiments were conducted in the two-terminal device configuration but with different channel lengths. The detail IV and noise characterization method is as described on previous section of this dissertation.

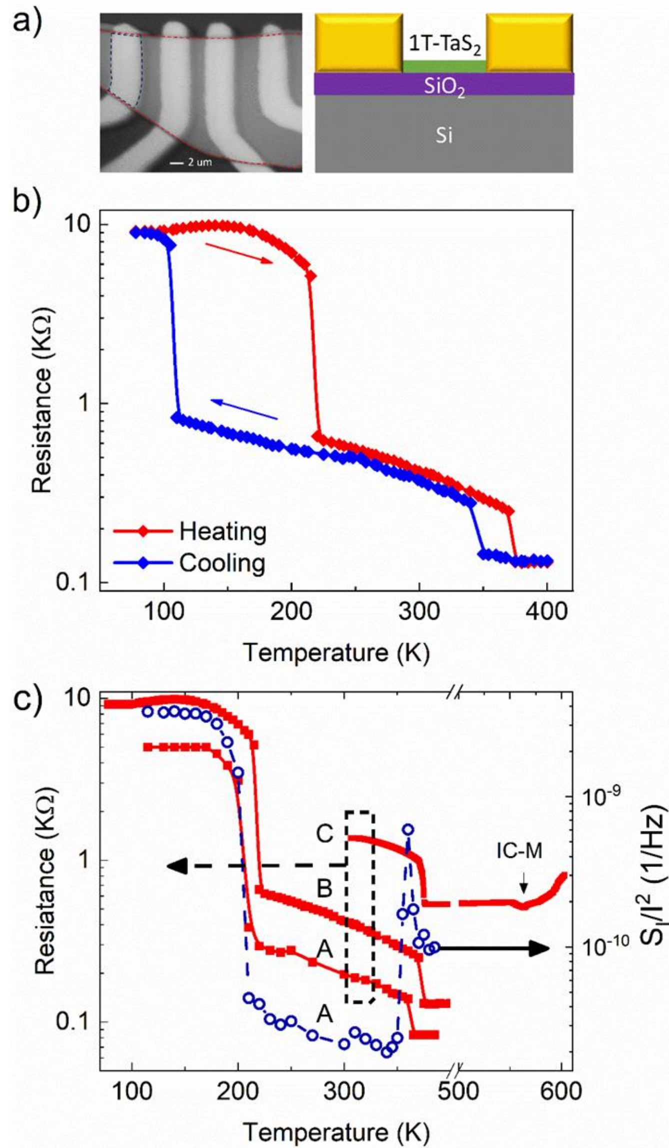

Figure 4.1 (a) Optical image of a representative device (left) and a schematic of the device layered structure (right). The scale bar is 2 μm (b) Resistance as function of temperature for cooling (blue curve) and heating (red curve). (c) Resistance (red curves) and normalized noise spectral density (blue curve), as function of temperature, measured in the heating cycle. The resistance is presented for three different 1T-TaS_2 devices (marked A, B, C). The noise spectral density, measured for device A. The device C was tested for higher temperatures to resolve the transition from incommensurate CDW to the normal metallic phase T = 550 K, marked as IC-M in the legend. All three devices show an abrupt resistance change at T = 355 K due to the transition from nearly commensurate to incommensurate CDW phase. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical Society.

Figure 4.1 (b) shows resistance as a function of temperature for both cooling and heating cycles for a representative 1T-TaS_2 device with a channel thickness of H = 60 nm. The data reveal two hysteresis windows at the C-CDW – NC-CDW phase transition (T = 200 K) and NC-CDW – IC-CDW phase transition (T = 355 K), in line with previous reports[5]. The well-resolved hysteresis windows and their temperature range attest to the high-quality of the fabricated devices. In Figure 4.1 (c), the plot shows resistance in the heating cycle in a wider temperature range (red curves) and normalized noise spectral density, S_I/I^2 (f = 11 Hz) (blue curves) as the functions of temperature (I is the current through the two-terminal device). The resistance is presented for three different 1T-TaS_2 devices (marked A, B and C) to illustrate reproducibility. The resistance and noise spectral density were measured at temperatures changing from low to high, with the heating rate of 2 K/min. The resistance and noise spectral density experience abrupt changes at the expected phase transition of 1T-TaS_2, *i.e.* C-CDW – NC-CDW near 200 K, NC-CDW – I-CDW near 350 K, and, finally, I-CDW – NP near 550 K. Note that the NP (normal phase) and M (metallic) symbols and terminology are used interchangeably in the text and figures. The noise level decreases by two orders of magnitudes, from 4×10^{-9} Hz^{-1} to 4×10^{-11} Hz^{-1} at the C-CDW – NC-CDW phase transition near 200 K, and it reveals a sharp, one order-of-magnitude peak at the NC-CDW – I-CDW phase transition near 350 K. The appearance of the C-CDW – NC-CDW transition indicates that the selected 1T-TaS_2 thickness range is appropriate.[23,37] The abrupt changes in the noise spectral density happen at the same temperatures as the corresponding steps in the electrical resistance. Our measurements in the low-bias regime prove that the noise spectroscopy can be used as an

efficient tool for monitoring the phase transitions in a 1T-TaS_2 device.[44] Irrespective of the exact physical mechanism of the phase transitions in thin films of 1T-TaS_2, *i.e.* pure electric field effect, Joule self-heating or both, the electrical bias, V_T, required to induce the transitions should depend on the device geometry and design details. To induce the I-CDW – NP transition by the electric field, at reasonably low V_T, I fabricated devices with different geometries, channel lengths, and thicknesses. The strength of the applied field was varied from low to high (up to 35 KV/cm). The *I-V* characteristics and noise spectral density were measured as the functions of the electric field at different temperatures. Figure 4.2 shows the resistance and noise characteristics of a 1T-TaS_2 device with 60-nm-thick channel, measured at RT. The resistance as a function of the applied electric field, E, is presented in Figure 4.2 (a). It drops sharply at the field of 3.6 KV/cm, which corresponds to the NC-CDW – I-CDW phase transition. At E = 6 KV/cm, there is another relatively small step-like decrease in the resistance suggesting the I-CDW – NP transition. Although the change in the resistance is small, it is reproducible. The normalized current noise spectral density, S_I/I^2, near the I-CDW – NP transition is shown in Figure 4.2 (b). The data are presented for different values of the electric field. Away from the phase-transition field, the noise spectra are of $1/f^\gamma$ type ($\gamma \sim 1$), indicating that there were no electromigration or dominant defect states, *i.e.* trap levels, with characteristic time constants. The noise increases with the trace of a Lorentzian peak at the transition bias, which corresponds to the onset of the I-CDW – NP transition. The evolution of the noise spectral density over the entire range of electric bias can be seen in Figure 4.2 (c), which shows S_I/I^2 (f = 10 Hz) as a function of electric field. There are three abrupt noise peaks.

The peaks at E = 3.6 KV/cm and E = 6 KV/cm correspond to the NC-CDW – I-CDW and I-CDW – NP transitions, respectively. The noise level increases near or at the phase transition points owing to the lattice reconstruction. One should note that noise peak at the transition to the normal phase is much more clear than the slight step in the resistance at the same value of the electric field. The latter proves the usefulness of the noise spectroscopy for monitoring phase transitions. There is another peak in the noise spectral density at the applied field E = 1 KV/cm. This peak attributed to the onset of CDW de-pinning, in line with our previous finding.[44] For some devices, the electric field to induce the phase transition, determined from the noise measurements, was somewhat lower than that from I-V characteristics. This difference can be attributed to the differences in sweep rates utilized for the I-V and noise measurements. This conclusion is in agreement with literature reports, which found a dependence of the NC-CDW – I-CDW transition on the voltage sweep rate.[49,61] To investigate in detail the I-CDW – NP transition specifically, several 1T-TaS_2 devices were heated to 400 K, which is well above the NC-CDW – I-CDW phase transition temperature but substantially below the I-CDW – NP transition temperature of 550 K (see resistance data for device C in Figure 4.1). The tested devices had different channel lengths and widths in order to alter the electric bias, V_B, needed to induce the I-CDW – NP transition either through the field strength or Joule heating. The evolution of electric current through the device and the normalized noise spectra density in one of the devices are shown in Figures 4.3 (a), and 3 (b), respectively. The transition to metal phase is clearly seen as the step-like jump in the current, I, resistance, R= V_B/I and as the peak in the normalized noise spectral density S_I/I^2. In this specific device, with

larger dimensions, an electric field E = 10.6 KV/cm is required to induce the transition to the metallic state. Note a pronounced noise peak at this value of the electric field, which exactly corresponds to the field of the jump in current to a lower resistivity state (see inset to Figure 4.3 (c)). In other devices, the changes in the current were small, and the I-CDW – NP transition could be unambiguously determined only from the peak in the noise spectral density (see Figure 4.3 (c)).

A possibility of switching a CDW device to multiple resistive states by application of a small electric bias, *e.g.* below 3V at RT, is important for information processing and memory applications.[62,63] To demonstrate switching among all three CDW phases and one normal phase, the 1T-TaS_2 device set to the C-CDW state by cooling it below 200 K. In a device with properly selected dimensions, the application of a relatively small electric bias can induce all three transitions. Figure 4 (a) shows current as a function of the applied in-plane electric field at T= 77 K. The current shows three consecutive hysteresis windows at the electric fields of 25.0 KV/cm, 31.3 kV/cm, and 32.1 kV/cm, which

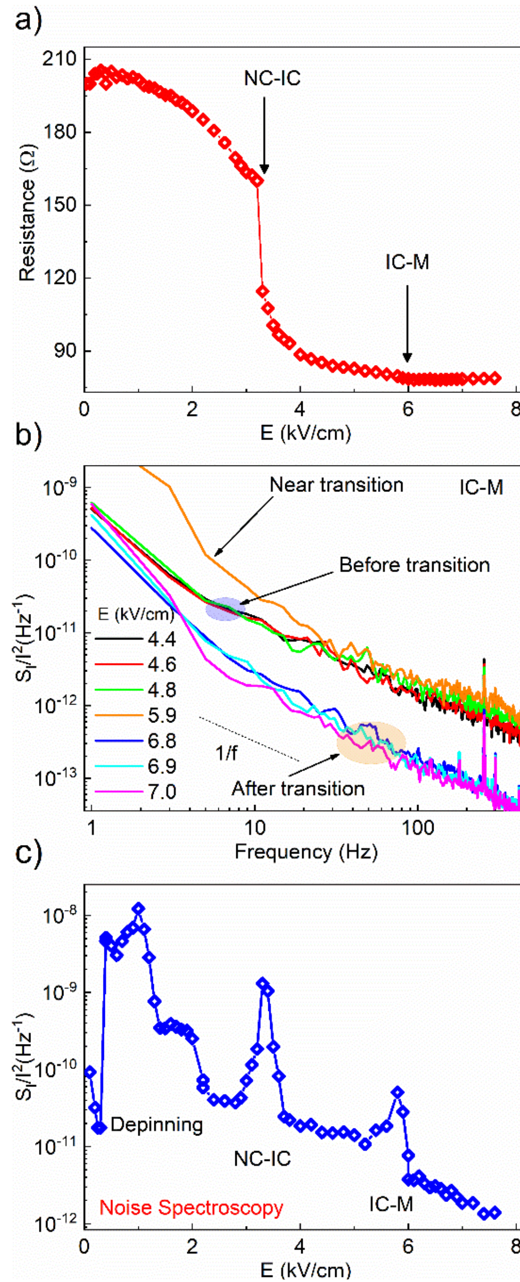

Figure 4.2 (a) Resistance as a function of the applied electric field for 1T-TaS_2 device measured at room temperature. The resistance drops sharply at E = 3.6 kV/cm to the nearly commensurate to incommensurate CDW phase transition, marked as NC-IC in the legend. (b) Normalized current noise spectral density as the function of frequency for several values of the electric field, (c) Normalized current noise spectral density as the function of the electric field. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical Society.

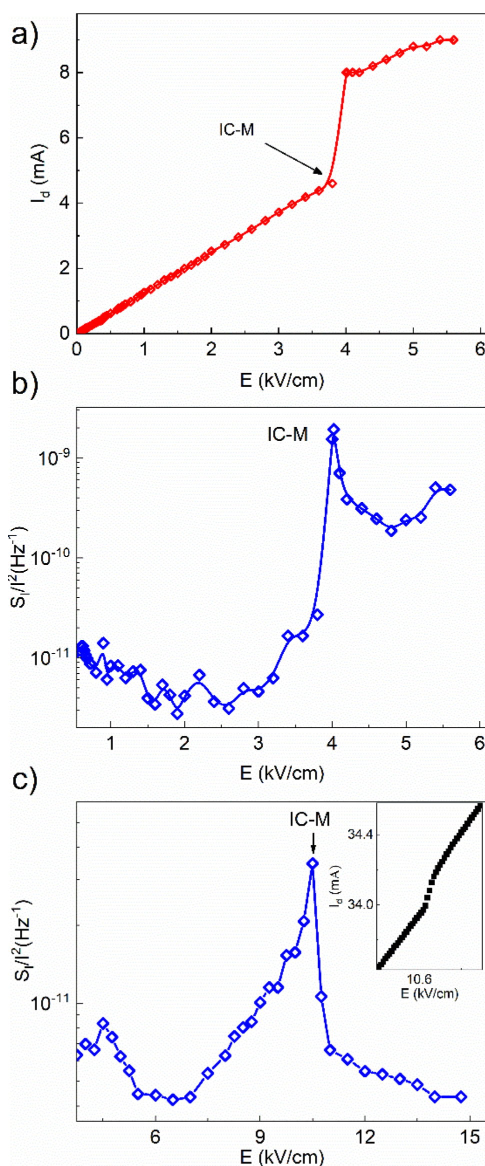

Figure 4.3 (a) Current through the device channel as a function of the applied electric field. (b) The normalized current noise spectral density as a function of the electric field for the same device and temperature as in (a). The noise spectral density reveals a well-resolved peak at the transition point, marked as IC-M in the legend. (c) The normalized current noise spectral density, as a function of the electric field for a different device with larger channel dimensions. The inset shows the current for this device with the distinguishable change at the transition point to the metallic phase. The data attests to the potential of the low-frequency noise spectroscopy for monitoring phase transitions in CDW materials. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical Society.

correspond to the C-CDW – NC-CDW, NC-CDW – I-CDW, and I-CDW – NP transitions, respectively. Field-induced resistive switching is often dependent on the sweep rates because the CDW states require time to reorder, regardless of the mechanism. In Figure 4.4 (b), the plot shows the current versus applied in-plane electric field at different voltage sweep rates, focusing on the E > 30 KV/cm range to better resolve the overlapping hysteresis region. One can see that the shapes of the hysteresis windows strongly depend on the scan rates. The possibility of inducing all three transitions with applied electric bias can be further confirmed with the low-frequency noise measurements. Figure 4.5 (a) shows the noise spectral density, S_I/I^2 (f = 10 Hz) as a function of the applied electric field for a different device. The measurements were conducted at T = 77 K to ensure that the C-CDW phase is the initial state of the device. The well-resolved peaks in the normalized noise spectral density at the field of 5 KV/cm, 8 KV/cm and 12.5 KV/cm correspond the C-CDW – NC-CDW, NC-CDW – I-CDW, and I-CDW – NP transitions, respectively. One can notice that the noise spectral density, S_I/I^2, is a more accurate metric of all phase transitions than the resistivity, R (see inset for comparison). It is interesting to note that the overall increase in the noise spectral density near the phase transition is often accompanied by the appearance of Lorentzian bulges in the noise frequency spectrum. In Figure 4.5 (b) and 5 (c), the noise spectral density as a function of frequency is plotted for several values of the electric field near the C-CDW – NC-CDW and NC-CDW – I-CDW transitions. The Lorentzian in Figure 4.5 (b) reveals itself as a $1/f^2$ shoulder because its central frequency is below the measurement range. The Lorentzian in Figure 4.5 (c) has a central frequency f_0 = 30 Hz.

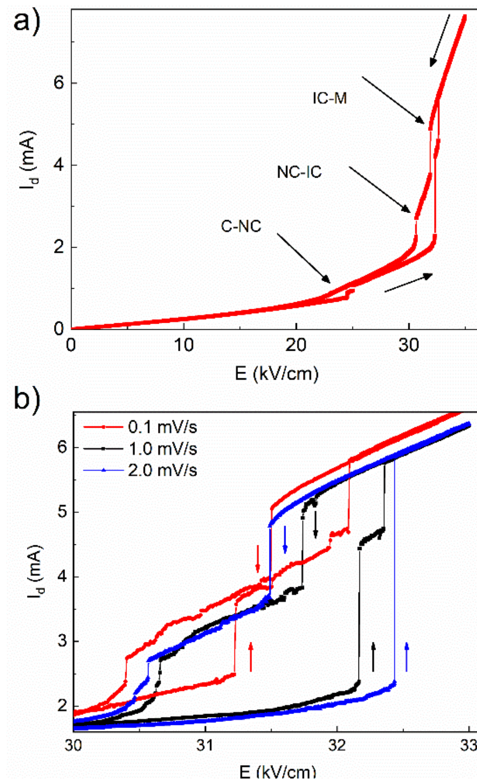

Figure 4.4 (a) Current through the device channel as a function of the applied bias electric field. (b) Current though the same device measured in high-field region at different bias voltage sweep rates. The slower sweep rates allow for better resolution of the phase transitions. Note the sweep-rate dependence of the field, required to induce the transitions. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical Society.

The resistance changes near the I-CDW – NP transition can vary over a large range depending on the device structure and size. Figure 4.6 (a) shows the resistance in the "low-bias" regime near the I-CDW – NP transition induced by temperature. The resistance changes in two other devices induced by the applied in-plane electric field are presented in Figure 4.6 (b). Utilizing many 1T-TaS_2 devices on Si/SiO_2 substrate with different channel geometry and sizes, the switching among three CDW and one metallic phase can be achieved in a wide temperature range. Figure 4.6 (c) summarizes the results of the

phase-transition switching with an applied electric filed. One can see that the spread of the required electric field can be as high as 10 kV/cm. The electric field required for switching is determined by the device design and geometry, which affects the strength and distribution of electric field at a fixed bias voltage, and the dynamics of heat dissipation for a given input power. It is important to note that all the phase transitions considered here for 1T-TaS_2 can be induced by technologically feasible, small voltage biases. For most of the fabricated devices tested at RT, the I-CDW – NP transition was achieved at 2 V-3 V bias, and the bias voltage required for the NC-CDW – I-CDW phase transition was substantially lower. I now examine the role that Joule heating of the device channel plays in the phase transitions. First, a simple analytical model is used to estimate the temperature in a representative device with the lateral dimensions, W×L, of 10 μm ×2 μm, and thickness t_f = 50 nm (W and L are the width and length of the channel, respectively). At room temperature, T_{amb}, the I-CDW–NP phase transition occurs at V_d = 1.75 V and I_d = 17.5 mA, which corresponds to the total Joule heating power of $P = V_d I_d$ = 30.6 mW. The generated power is dissipated through the underlying SiO_2 layer with a thickness of t_{ox} = 300 nm and a thermal conductivity of k_{ox} = 1.4 $Wm^{-1}K^{-1}$. Although the in-plane thermal conductivity of the TaS_2 is approximately a factor of ×3 larger than that of the SiO_2 layer, owing to the small cross-section of the TaS_2 channel, $A_{f,\parallel} = t_f \times W$, the total in-plane thermal resistance of the TaS_2 layer, $R_{th,\parallel} = L/(k_f \times A_{f,\parallel})$ is about two orders of magnitude greater than the total

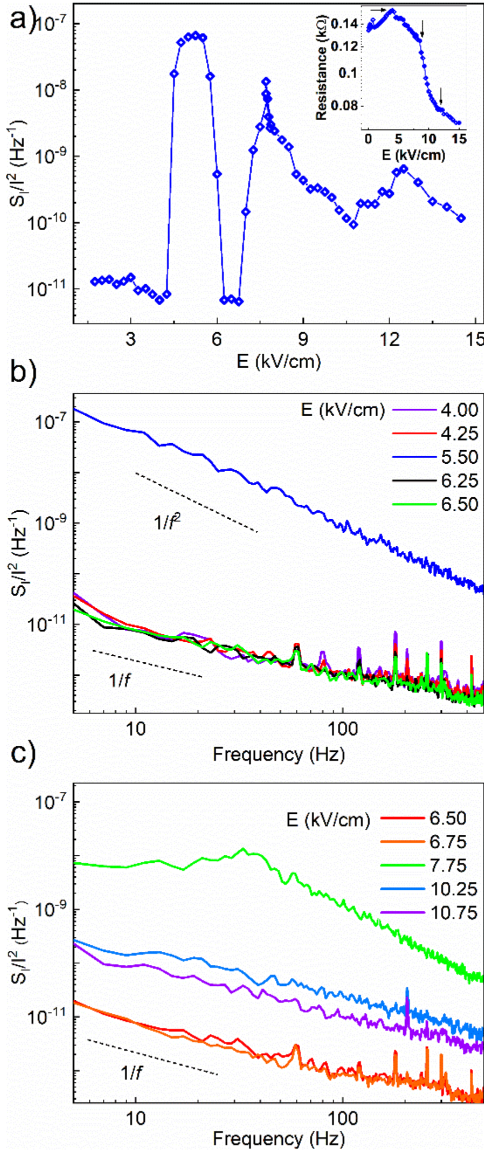

Figure 4.5 (a) Normalized current noise spectral density as a function of electric field applied to the device kept at 77 K. The inset shows the channel resistance as a function of the electric field for the same device. The transition points are indicated with the arrows. (b) The noise spectral density as a function of frequency for several values of the electric field near the commensurate to nearly commensurate phase transition. (c) The same as in (b) but for the electric field, which correspond to the transition from the nearly commensurate to incommensurate phase. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical Society.

cross-plane thermal resistance, $R_{th,\perp}$, of the underlying SiO_2/Si layers. For this reason, almost all dissipated heat diffuses through the SiO_2/Si substrate. The total cross-plane thermal resistance is a sum of three terms, $R_{th,\perp}= R_c+ R_{SiO2}+ R_{Si}$, where R_c, R_{SiO2} and R_{Si} are the thermal contact resistance at the TaS_2–SiO_2 interface, the thermal resistance of the SiO_2 layer, and the thermal resistance of the Si substrate, respectively. The thermal contact resistance at the interface and the thermal resistance of the SiO_2 layer are $R_c = (G_{int}\times A_{f,\perp})^{-1}$ and $R_{SiO2}= t_{ox}/(k_{ox}\times A_{f,\perp})$, where $A_{f,\perp} = W\times L$ is the device cross-plane surface area. The G_{int} (interfacial thermal conductance) values reported for typical van der Waals materials on standard substrates vary in relatively small range and mostly depend on the quality of the interface[64–68], e.g. 50 MW/m^2K for graphene, 33 MW/m^2K for WTe_2, and 15 MW/m^2K for MoS_2, respectively. An analytical estimate of the device average temperature rise across the SiO_2 layer is $\Delta T \approx P\times R_{SiO2}$, without taking into account the thermal contact resistance. This result suggests that the I-CDW–NP phase transition can take place due to the Joule heating, since the device temperature, $T = Tamb + \Delta T = 628$ K, which exceeds the I-CDW–NP phase transition temperature of 550 K. Taking into account R_c will add ~100–200 K to the temperature rise depending on the value for G_{int} assumed for the device structure.

To further understand the phase transition mechanism and separate out the temperature effect from the field effect, the heat diffusion is modeled in the experimentally tested sample, using the finite-element method implemented in COMSOL (see METHODS for details). The heat generation from Joule heating in the TaS_2 channel

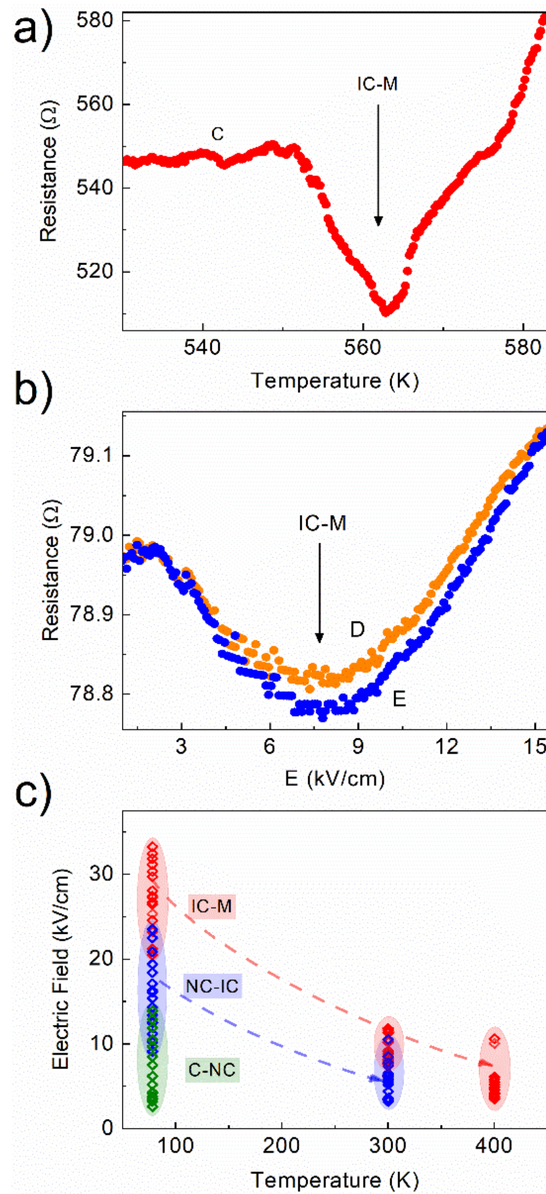

Figure 4.6 (a) Device channel resistance as a function of temperature near the transition from the incommensurate CDW phase to normal metallic phase. (b) Resistance as a function of applied electric field near the transition from the incommensurate CDW phase to normal metallic phase. The data are shown for two other devices with smaller geometries. (c) Summary of electric field induced phase transitions at different temperatures for 1T-TaS_2 devices. The variation in the electric field required to include the phase transitions is due to different device geometries, thickness of the layers in the device structures, and other variations in the device designs. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical society.

region is sensitive to the sample geometry, material properties, and ambient conditions. The effective electric field, E, and the current density, J, in the channel are taken to be same as in the experiment by tuning the sheet resistance of the TaS_2 active layer. The latter ensures that the Joule heating power, $P = V_d I_d$, corresponds to that of the experimental setup. I focus on the temperature distribution near two critical transition points: (i) just before IC-CDW − NP (E ~ 8.45 KV/cm), and (ii) just after IC-CDW − NP (E ~9 kV/cm) Since the current is localized between the inner contacts, significant heating happens in the active region between two bias, *i.e.* source – drain, contacts. Our simulations show that just before the phase transition, the temperature of the hotspot can rise as high as ~739 K, well exceeding the C-CDW-NP transition temperature. After the phase transition, the temperature of the sample increases even more, up to ~864 K. Figure 4.7 (a)-(b) show the temperature profile along the cross-section of the device channel (see inset to Figure 4.7 (a)). The generated heat in the hotspots, indicated as red color regions at the middle of the channel, dissipates mainly through the SiO_2 layer and Si substrate. Owing to its low thermal conductivity, the SiO_2 layer acts as an effective thermal barrier, and prevents effective heat dissipation to the Si substrate. The latter results in substantial heating, which drives the phase transitions. The obtained numerical data for the specific device geometry is in agreement with the analytical estimate above. The radiation loss from the top surface becomes important at elevated temperature. However, it is not significant enough to change the conclusion that Joule heating is the reason behind the C-CDW−NP phase transition in TaS_2 devices of the considered geometry, on SiO_2/Si substrate.

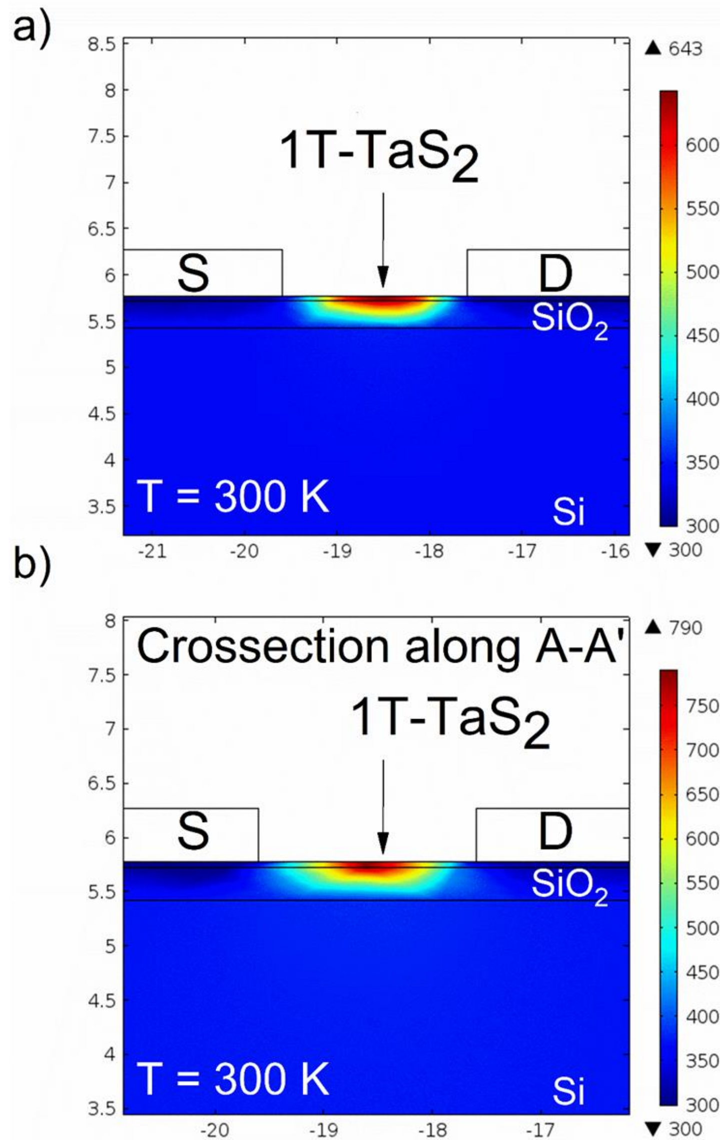

Figure 4.7 (a) Simulated temperature distribution profile along the cross-section of the device channel for the voltage bias just before the C-CDW-NP transition. (b) The same as in (a) but for the voltage bias, which corresponds to the regime above the C-CDW-NP phase transition. The temperature increases owing to the lower resistance of 1T-TaS_2 in the metallic NP, which results in stronger Joule heating. Reprinted with permission from A.K. Geremew, S. Rumyantsev, F. Kargar, B. Debnath, A. Nosek, M.A. Bloodgood, M. Bockrath, T.T. Salguero, R.K. Lake, and A.A. Balandin, ACS Nano, 13, 7231 (2019). Copyright (2019) American Chemical society.

4.7 Conclusions

In conclusion, I investigated switching among three CDW phases – commensurate, nearly commensurate, incommensurate – and the normal metallic phase in thin films of 1T-TaS_2 induced by an in-plane electric field. The electric field switching among all four phases has been achieved, which is a key prerequisite for nanoscale device applications. I have demonstrated that an application of small voltage bias to a device kept at room temperature can induce the transition from the nearly commensurate and incommensurate phases to the normal metallic phase. The low-frequency electronic noise spectroscopy was used as an effective characterization tool for monitoring the transitions, particularly the switching from the incommensurate CDW to the normal phase. The noise spectral density experiences sharp increases at the phase transition points, which correspond to the step-like changes in resistivity. The assignment of the phases has been confirmed by the low-field resistivity measurements over the temperature range from 77 K to 600 K. Analysis of the experimental data and simulations of heat dissipation suggests that self-heating plays a dominant role in the electric-field induced transitions. Furthermore, the results demonstrate the potential of the noise spectroscopy for investigating phase transitions in low-dimensional CDW materials.

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5. Summary

This dissertation described results of investigation of electron transport in two classes of layered van der Waals materials: quasi-one-dimensional (1D) transition metal trichalcogenides (TMTs) and quasi-two-dimensional (2D) transition metal dichalcogenides (TMDs). Practical motivations for this study included the search for materials, which can be used in ultimately downscaled interconnects in the next generations of electronics, and materials revealing low power switching phenomena, which can be used in future logic circuits. TMTs have strong covalent bonds in one direction and weaker bonds in cross-plane directions. They can be prepared as crystalline nanoribbons consisting of 1D atomic threads, i.e. chains. Here I provide a brief summary of the main results of the dissertation. I have examined the current carrying capacity of $ZrTe_3$ nanoribbons using a set of structures fabricated by the shadow mask method. The bulk crystals were synthesized by the chemical vapor transport method and exfoliated onto Si/SiO_2 substrates. It was found that $ZrTe_3$ nanoribbons reveal an exceptionally high current density, on the order of ~100 MA/cm^2, at the peak of the stressing DC current. The high current density in $ZrTe_3$ can be attributed to the single-crystal nature of quasi-1D van der Waals materials. The low-frequency noise was of 1/f type near room temperature (f is the frequency). The noise amplitude scaled with the resistance, following the trend established for other low-dimensional materials. Whereas the low-frequency noise spectral density, S_I/I^2, reveals 1/f behavior near room temperature, it is dominated by the Lorentzian bulges of the generation–recombination noise at low temperatures (I is the current and f is the frequency). Unexpectedly, the corner frequency of the observed Lorentzian peaks shows strong sensitivity to the applied source–

drain bias. This dependence on electric field can be explained by the Frenkel–Poole effect in the scenario where the voltage drop happens predominantly on the defects, which block the quasi-1D conduction channels. I also have found that the activation energy of the characteristic frequencies of the G-R noise in quasi-1D $ZrTe_3$ is defined primarily by the temperature dependence of the capture cross-section of the defects rather than by their energy position. These results are important for the application of quasi-1D van der Waals materials in ultimately downscaled electronics.

I have investigated switching among three CDW phases – commensurate, nearly commensurate, incommensurate – and the high-temperature normal metallic phase in thin-film 1T-TaS_2 devices induced by application of an in-plane bias voltage. The switching among all phases has been achieved over a wide temperature range, from 77 K to 400 K. The low-frequency electronic noise spectroscopy has been used as an effective tool for monitoring the transitions, particularly the switching from the incommensurate CDW phase to the normal metal phase. The noise spectral density exhibits sharp increases at the phase transition points, which correspond to the step-like changes in resistivity. Assignment of the phases is consistent with low-field resistivity measurements over the temperature range from 77 K to 600 K. Analysis of the experimental data and calculations of heat dissipation indicate that Joule heating plays a dominant role in the voltage induced transitions in the 1T-TaS_2 devices on Si/SiO_2 substrates, contrary to some recent claims. The possibility of the bias-voltage switching among four different phases of 1T-TaS_2 is a promising step toward nanoscale device applications. The results also demonstrate the

potential of noise spectroscopy for investigating and identifying phase transitions in the materials.